AN124: Pin Sharing Techniques for the C2 Interface

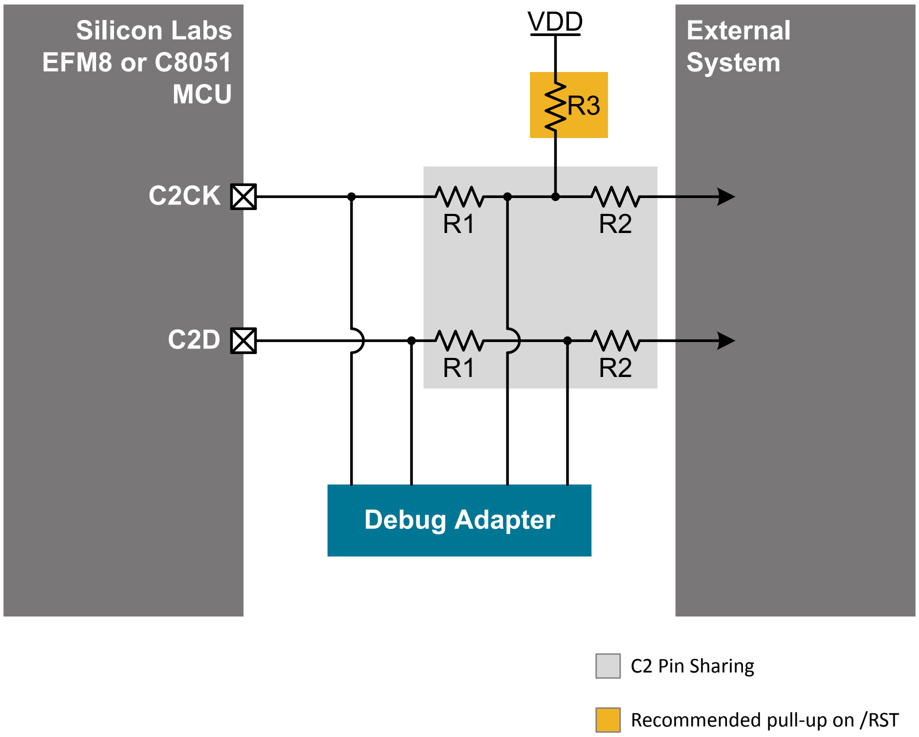
All of the Silicon Labs EFM8 8-bit MCUs and some of the C8051 8-bit MCUs (e.g. C8051F85x) include an on-chip 2-Wire (C2) interface for in-system programming and debugging.

Two signals are associated with the C2 Interface: C2 Clock (C2CK) and C2 Data (C2D). To preserve package pins, the C2CK and C2D pins typically also function as the user pins RSTb or /RST and a GPIO pin, respectively. To enable in-system programming or debugging, external resistors are typically used to isolate C2 traffic from the external system. The isolation configuration depends on the user function associated with the pins on the target device. This application note discusses C2 isolation configurations for each user function. If the /RST or RSTb and GPIO are not occupied by user functions, no isolation circuitry is needed.

Additional information on the C2 programming interface itself can be found in AN127: "Flash Programming via the C2 Interface", available on the Silicon Labs website: http://www.silabs.com/8bit-appnotes.

KEY POINTS

- Typically, two pins (RSTb or /RST and a GPIO) are borrowed by the C2 interface during C2 communication.
- Isolation resistors are typically required to perform in system programming or debugging via C2.
- The C2 isolation configuration depends on the user function associated with the RSTb or /RST and GPIO pins.



1. About the C2 Pins

When C2 communication is idle, the C2 pins (C2CK and C2D) typically function as user pins RSTb or /RST and a GPIO, respectively. The interface master initiates C2 communication by generating an active-low strobe on the C2CK pin. Following this strobe, the interface master may safely borrow the C2 pins without disturbing the user functions.

1.1 C2CK (RSTb or /RST)

The C2CK signal provides the clock for all C2 communications. When C2 communication is idle, the C2CK pin functions as the active-low reset I/O pin (RSTb or /RST).

As a user input, the C2CK pin is used to generate a device reset when held low for more than 20 µs. As a user output, the C2CK pin may be driven low by the on-chip VDD monitor. When the C2CK pin is not being driven, an internal (weak) pull-up resistor pulls the C2CK pin high. For in-system debugging, an external pull-up resistor is required (see Figure 3.1 Debug Adapter Connections on page 5).

C2 events on C2CK are ignored by the reset hardware as long as C2CK is low for less than 5 µs. Since the C2CK pin is always an open-drain output, the interface master may initiate C2 communication at any time with an active-low strobe on C2CK.
Note: The USB Debug Adapter uses the C2CK pin to sense the communication voltage for the 8-bit MCU.

1.2 C2D (GPIO)

The C2D signal serves as the data bus for all C2 communications. When C2 communication is idle, the C2D pin typically functions as a standard GPIO. When a C2 event is detected on the C2CK pin, the target device automatically configures the C2D pin to accept C2 data. During C2 communication, the C2 Interface controls the C2D pin; following each C2D communication frame, the C2D pin is restored to the user-defined (GPIO) state.

Some devices do not share the C2D pin with a GPIO. In these cases, no isolation circuitry is needed, and the C2D pin can be connected directly to the debug adapter.

2. Pin Sharing Configurations

Each of the following illustrations describes the pin sharing configuration for a single C2 pin; these illustrations may be applied to C2CK and/or C2D.

The required isolation configuration depends on the signal direction of the associated user pin. Each signal direction (input, output, and bi-directional) is discussed.

Resistors R1 and R2 serve to limit the current sunk or sourced by the interface master and external system; resistor values should be chosen according to the capabilities of the interface master and external system drivers (if applicable). For applications using the Silicon Labs USB Debug Adapter as the interface master, resistors R1 and R2 should be a minimum of 1 kΩ.

2.1 Input Only

A pin is considered an input if the target device never drives the logic level of the pin. For the input only case, one resistor is required.

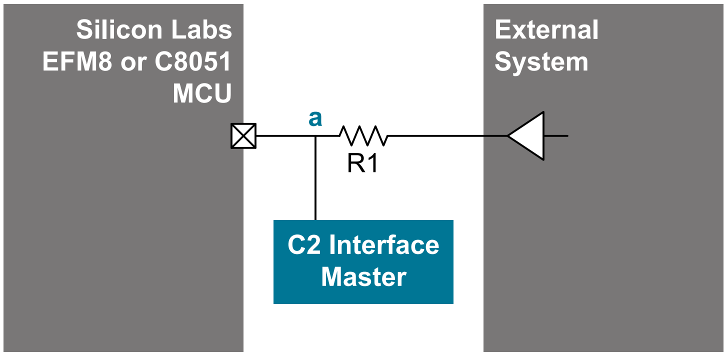


Figure 2.1. Input-Only Configuration

The interface master controls the logic level at node **a** during C2 communication; the isolation resistor R1 ensures that no contention occurs between the interface master and the external system.

2.2 Output Only

A pin is considered an output only if the external system never drives the logic level of the pin. The typical output case is shown in Figure 2.2 Output-Only Configuration — Case 1 on page 3.

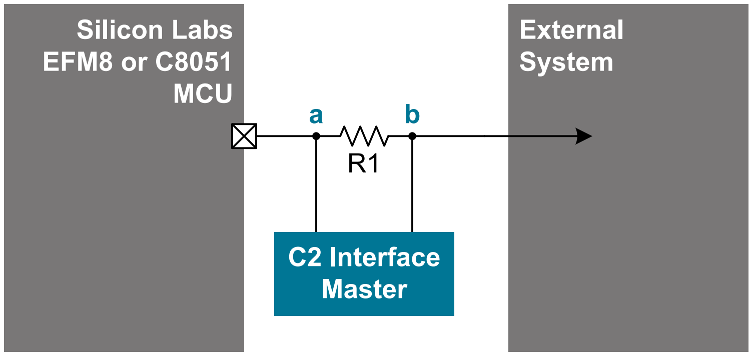


Figure 2.2. Output-Only Configuration — Case 1

The configuration in Figure 2.2 Output-Only Configuration — Case 1 on page 3 assumes that the logic level seen by the external system should not change during C2 communication (toggling at node **b** during C2 communication would disturb the external system). In this case, the interface master samples the logic level at node **a** and drives the same logic level at **b** before initiating C2 communication at node **a**. The master may then communicate with the target device at node **a** while the isolation resistor R1 ensures that the external system is not disturbed.

If the logic level seen by the external system is allowed to change during C2 communication, the pin sharing configuration reduces to that shown in Figure 2.3 Output-Only Configuration — Case 2 on page 3.

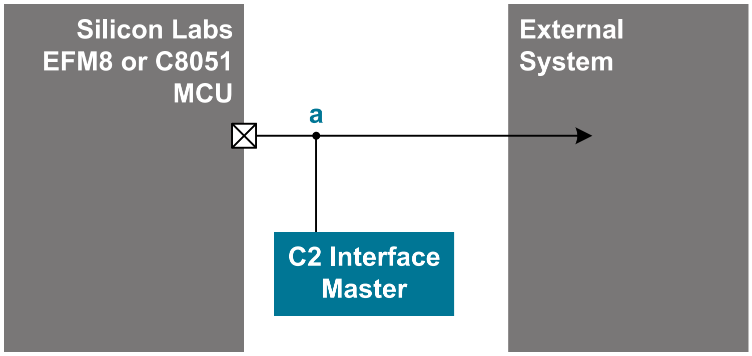


Figure 2.3. Output-Only Configuration — Case 2

2.3 Bi-Directional

A pin is considered bi-directional if both the target device and the external system may drive the pin. In this case, two isolation resistors are typically required, as shown in Figure 2.4 Bi-Directional Configuration — Case 1 on page 4.

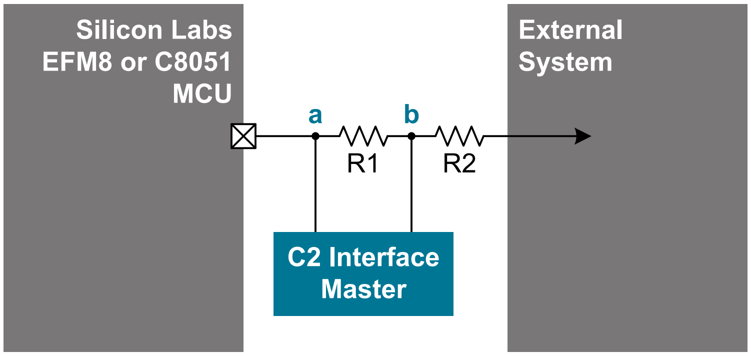


Figure 2.4. Bi-Directional Configuration — Case 1

This configuration assumes that the logic level seen by the external system should not change during C2 communication. In this case, the interface master samples the logic level at **a** and then drives that logic level at **b** before initiating C2 communication at node **a**. Isolation resistor R2 ensures that no contention occurs between the interface master and the external system at node **b**. If the logic level seen by the external system is allowed to change during C2 communication, the pin sharing configuration reduces to that shown in Figure 2.5 Bi-Directional Configuration — Case 2 on page 4.

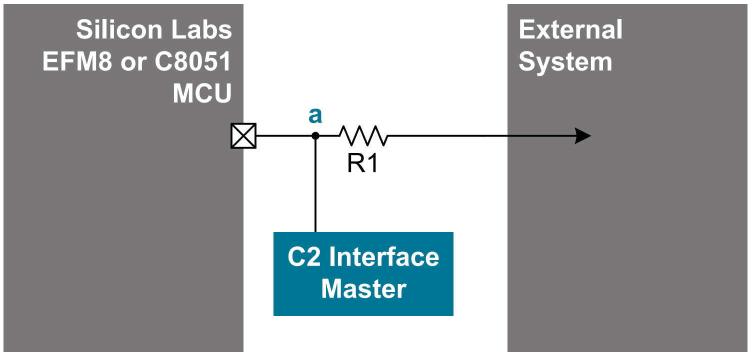


Figure 2.5. Bi-Directional Configuration — Case 2

Here, the interface master may communicate with the target device at node **a**, while isolation resistor R1 ensures that no contention occurs between the interface master and the external system.

3. About the Interface Master

C2 pin sharing is applicable to the following: in-system programming and in-system debugging. Each task includes C2 communication between a target Silicon Labs C2 device and a C2 interface master.

- For in-system programming, the interface master may be the Silicon Labs USB Debug Adapter, on-board EFM8 STK debug adapter, or any user device configured to operate as a C2 master.
- For in-system debugging, the interface can be the Silicon Labs USB Debug Adapter or on-board EFM8 STK debug adapter.

Figure 3.1 Debug Adapter Connections on page 5 shows the necessary connections for either programming or debugging using the C2 interface. Note that to perform in-system debugging, an external pull-up resistor should be connected between the C2CK pin and VDD. The C2CK pull-up resistor R3 should be a maximum of 10 kΩ, and a value of 1 kΩ is strongly recommended. Shaded areas in the figure indicate connections/components that are application-dependent (see 2. Pin Sharing Configurations). All other connections are required.

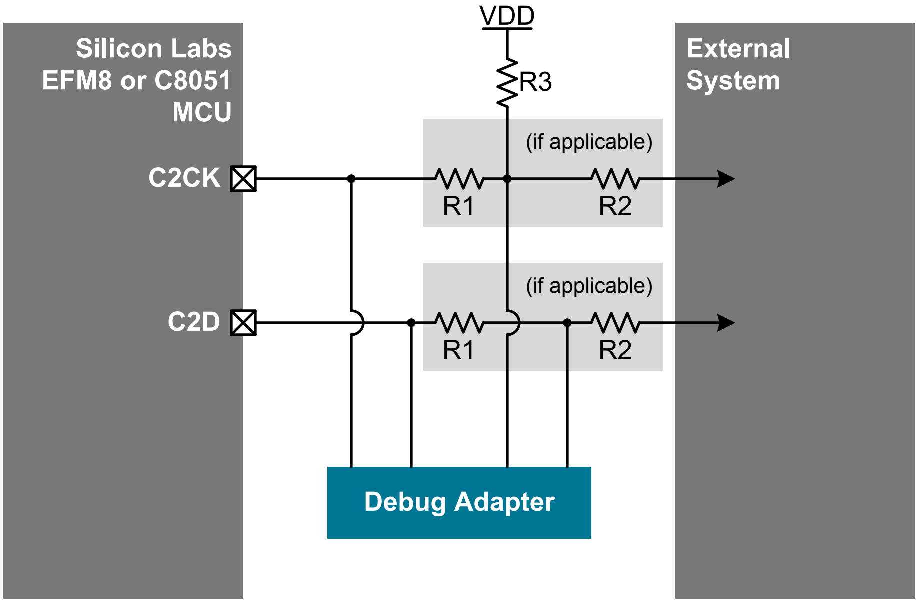
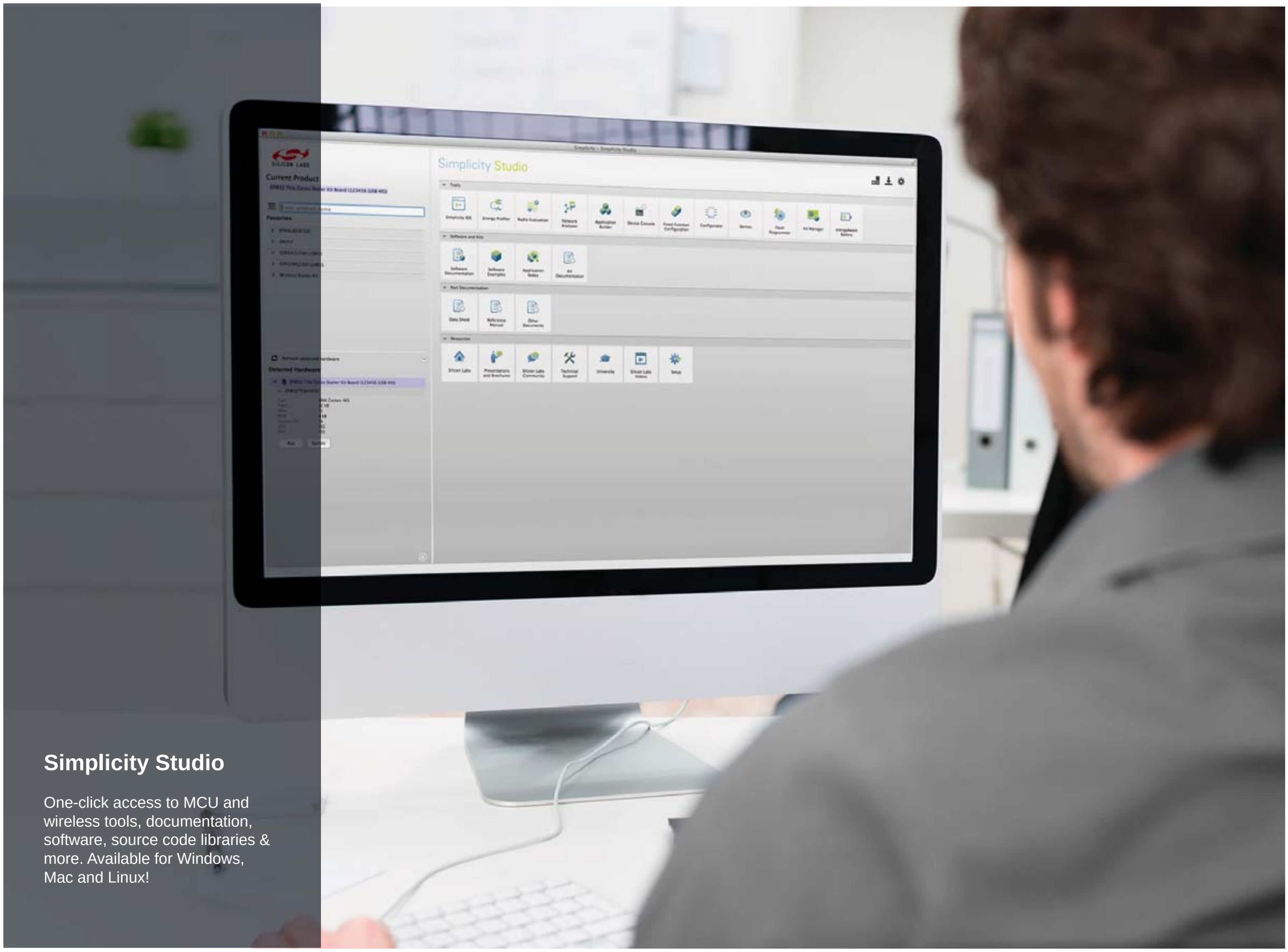


Figure 3.1. Debug Adapter Connections



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