Silicon Labs Quality and Operations Overview

November 2023

Content

Corporate Identity

- **Corporate Overview**
  - Click here for Silicon Labs' Corporate Overview homepage
- **Quality and Environmental Information**

  Highlights
  - ISO 9001:2015 & ISO 14001:2015 Certificates
  - Sony Green Partner Certificate
  - Quarterly Quality & Reliability Report
  - Additional information here
- **Investor Relations, Annual Report and Recent News**
  - Click here for Silicon Labs' Investor Overview homepage

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- Development Process
- Qualification Process
- Manufacturing Process
- Supplier/Technology Selection Strategy, Supply Chain Management
- Quality Overview
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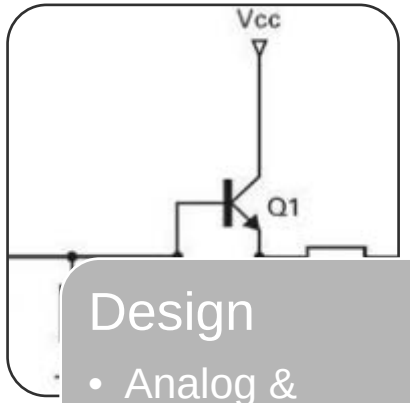
New Product Development Major Milestones

Concept & Planning

- Customer
- Sales
- Design & Apps
- Manufacturing

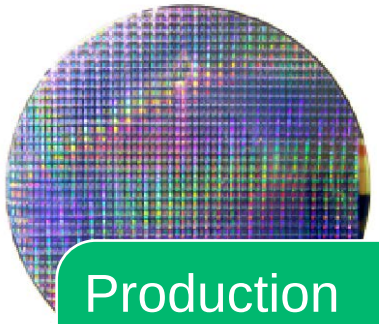


Design

- Analog & Digital
- Software
- Test

Verification

- Applications
- Qualification
- Customer Sampling
- Launch



Production

- Foundry
- Assembly
- Test
- Pack & Ship

Product Development & Release to Manufacturing

Product Development & Release to Manufacturing follows a rigorous process with Management Review & Approval at key milestones

- **Product Development Process**
  - Concept, Architecture, Design and PG (Tapeout) – reviews and checklists at each stage
- **Release to Manufacturing (RTM) Process**
  - Engineering > Initial Production > Full Production
    - Formal reviews and checklists at each stage
    - Ship quantity limits increase with each phase
  - RTM addresses the following (not inclusive)
    - Probe – HW and SW
    - Final Test – HW and SW
    - Qualification
    - Validation & Verification
    - Test Optimization, offshore transfer
    - Cpk and statistical baselines for maverick lot detection

Design for Cost, Test and Manufacturing

- **Every design is reviewed to assure robust manufacturability, testability, and cost optimization**
- **Any risks identified are removed or minimized by methods such as:**
  - Design changes
  - Extra qualification
  - Improved manufacturing capability or controls
  - Increased monitoring
- **Reviews are held at the following milestones at a minimum**
  - NPI1
  - Pre-PG
  - Initial Production

Test Strategy

- **Design for Test Strategy**
  - Scan used for synthesized logic
  - Functional test modes employed to isolate functional blocks
  - Built in Self Test (BIST) features also utilized
- **Fault Coverage**
  - Minimum fault coverage required for production test release
- **At Speed Testing**
  - Analog, Functional, and Memory tests are tested at datasheet speeds
- **Test Insertions**
  - Each product is tested at its worst-case temperature at a minimum
  - Promotion to single temperature test from multi-temperature test follows a rigorous process

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Product and Process Qualification & Criteria

Silicon Labs uses industry standard test methods to evaluate products and follows the guidelines of:

EIA/JESD 47 - Stress-Test-Driven Qualification of Integrated Circuits

AEC-Q100 - Stress Qualification For Integrated Circuits

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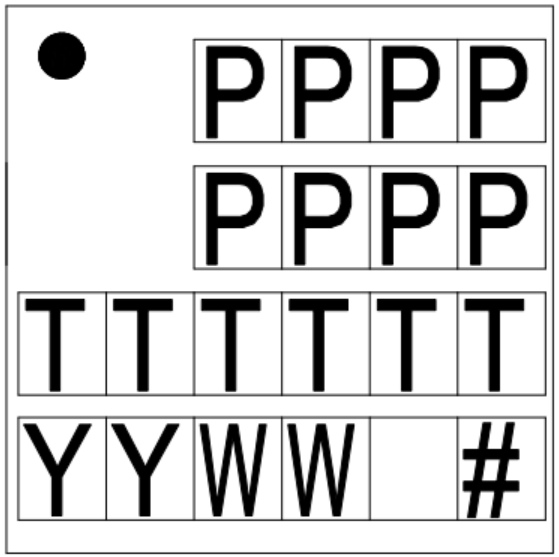
Statistical Bin Limits (SBL)

- **SBLs are used at these process steps**
  - Foundry Wafer Acceptance Test (WAT)
  - Wafer Probe
  - Final Electrical Test
- **Limits are established to identify abnormal (maverick) material lots**
- **Limits are based on overall yields or on specific tests or test groups**
- **The manufacturing requirements system (MRP) system automatically places on hold lots that fail to meet limits**
- **There are two levels of hold/notification**
  - Level 1 – Engineering: held for product engineer investigation and validation before release
  - Level 2 – Material review board (MRB): held for product engineer and quality manager investigation and validation before release

Product Traceability

- **Device packages are marked with a product identification number and a tracecode captured in our ERP system**
- **Tracecode is also marked on the packing labels**
- **Tracecode provides a link to the processing history, from wafer number to shipment**



EXAMPLE: EFM8BB21F16I-C-QFN20R

- Package Type: 20-QFN-3x3
- Mark Method: Laser
- Logo: None
- Tracecode Type: Standard
- Pin 1 Mark: Circle = 0.25mm diameter (Top Left corner)
- Font Size (mm): 0.50mm Right-Justified
- Line 1 Mark Format: Device Number (BB21)
- Line 2 Mark Format: Device Number (F16I)
- Line 3 Mark Format: TTTTTT = Mfg Code (from the Assembly PO)
- Line 4 Mark Format:
  - YY = Year of the packaging/assembly start
  - WW = Work Week of the packaging/assembly start
  - # = Device revision (A, B, etc.).

Quality Monitoring

Silicon Labs follows JEDEC as the preferred industry standard

Quality Monitors

- **Electrical: production samples are retested to datasheet limits. This sample method identifies defects introduced at the test process step or that have escaped the test process.**
- **Visual/Mechanical: production is sampled prior to final pack. Inspections coverage includes mark, count, label, cover tape workmanship, moisture barrier bag visual, lead location, part placement, and other workmanship items.**
- **Reporting: failures drive corrective actions and process/product improvements**
- **Quality data is reported in quarterly Quality & Reliability Report**

Reliability Monitoring

Silicon Labs follows JEDEC as the preferred industry standard

- **Failure Rate Estimation: A long-term, steady-state failure rate calculation allows circuit and system engineers to allocate failure rates at the component level during system design.**
- **Failure in Time (FIT): FIT represents the number of failures in a billion hours of operation. Silicon Labs reports FIT rates in its quarterly Quality & Reliability Report as curves and in tables for specific temperatures and assumptions.**
- **Mean Time To Failure (MTTF): inverse of FIT rate (1/FIT)**
- **Failure Rate Calculation Method: Long-term failure rates are estimated by applying the Arrhenius equation to data collected from long term operating life tests. Confidence factors of 90% and 60% are reported**

Process Control Points

- **Critical to Quality (CTQ) parameters are controlled by Silicon Labs' assembly partners**
- **Their performance is reported quarterly in CpK reports and reviewed by the Silicon Labs Supplier Managers**

Process	CTQ Parameter
Wire Bond	Wire pull strength (g) Ball shear strength (g)
Lead plating	Thickness (µ")
Saw/Singulation	Package Dimension (mm)

Change Management

- **Silicon Labs follows the principles of JEDEC J-STD-046 for change management and notification**
- **Change Action Boards review and assure compliance for both supplier and internally initiated changes**
  - Wafer Fab Changes
  - Assembly Changes
  - Materials Changes
  - Qualification of changes to JEDEC requirements if applicable
- **Customer Notification**
  - PCN – 90 day notification provided to customer
  - EOL – 180 for last orders, 360 days for final delivery to customer
  - Exceptions require cross-functional review and approval

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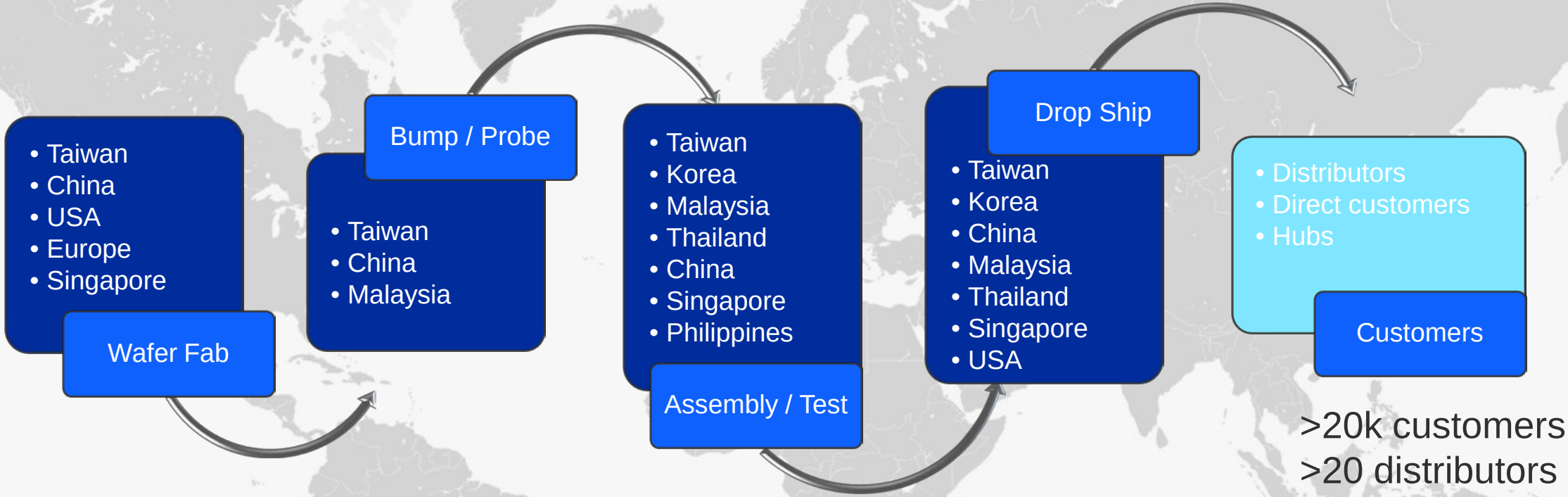
Supply Chain Process Overview

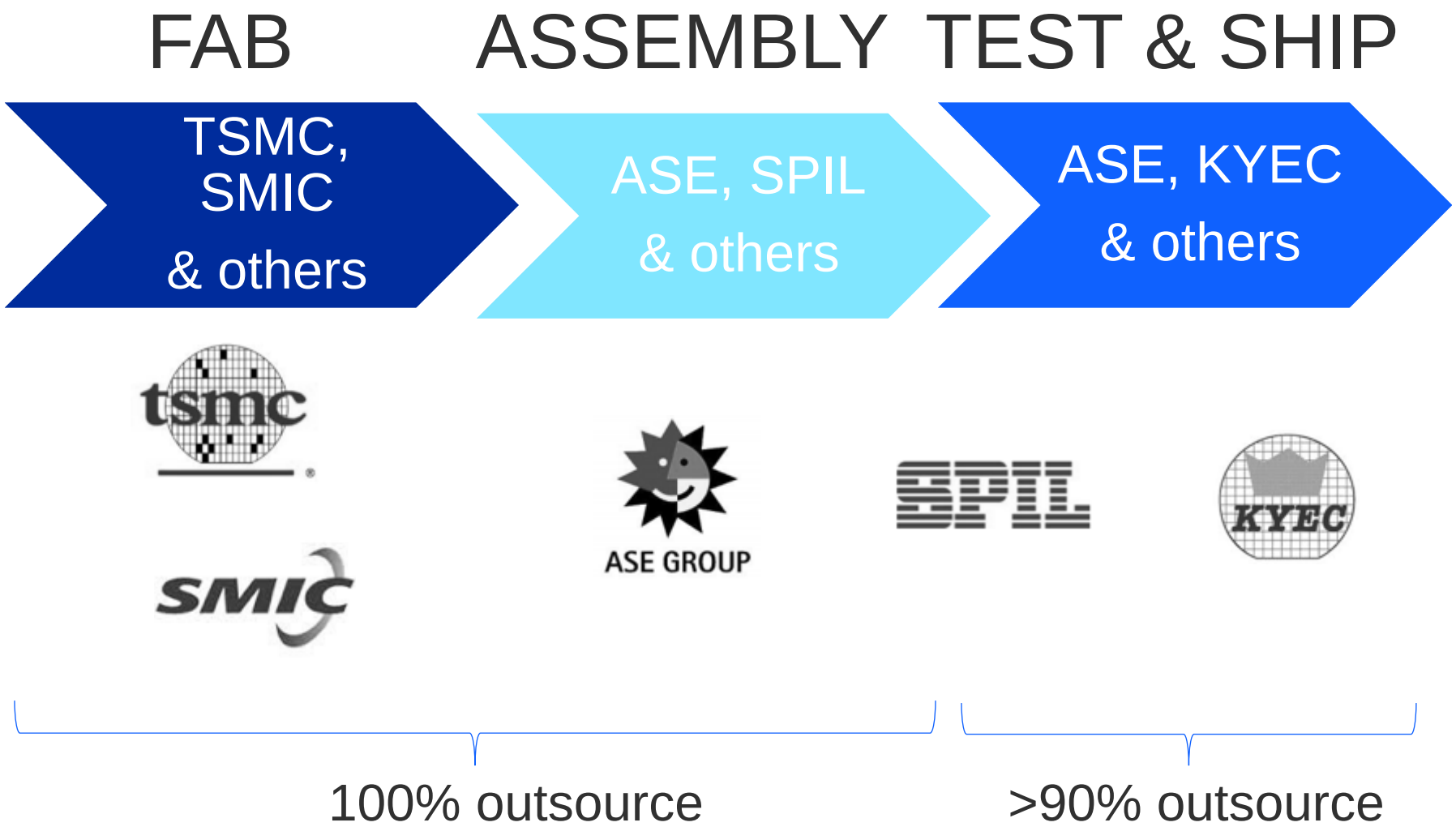
- Partner with world-class suppliers
- Manage products from development to customer delivery
- Support unexpected surges in demand
- Reliable, high volume supply
- Quality-centered assembly and test
- Dual sourced for capacity assurance
- Silicon Labs is ISO9001:2015 & 14001:2105, certified by TUV Rheinland of North America and conforms to IATF 16949:2016

Global Supply Chain



>20k customers
>20 distributors

IC Manufacturing Model- Fabless and Outsourced



Module Manufacturing Model – Outsourced Assembly

>90% outsource | 100% outsource | >90% outsource

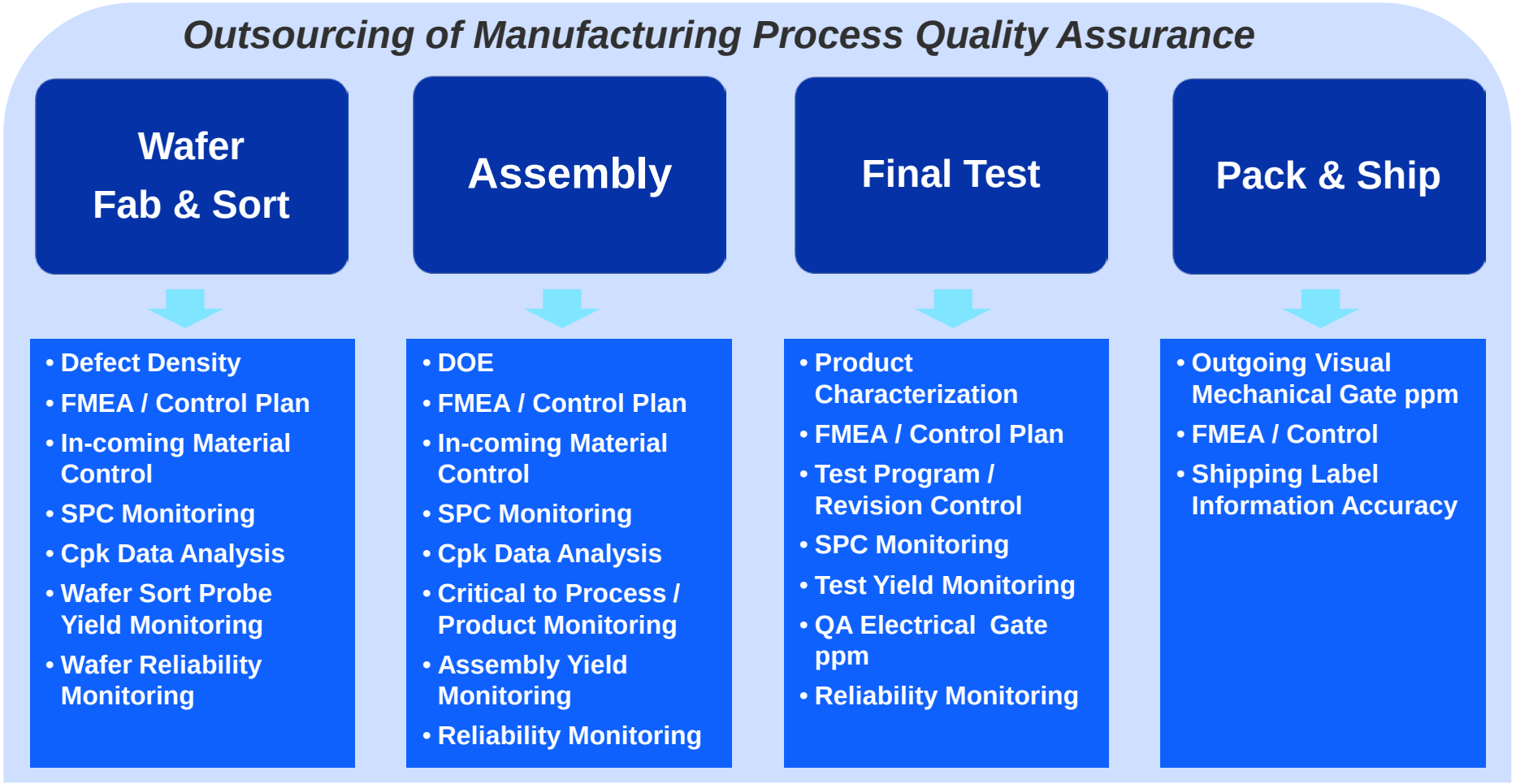
Supplier & Technology Selection

- **Process technology, package choice and test platforms are carefully chosen based on:**
  - Technology availability and maturity at suppliers
  - Technology roadmap of suppliers
  - Technology reliability of suppliers
  - Past and present execution (quality, cycle time, deliveries, operational efficiencies) from suppliers
  - Material cost from the supplier and
  - Cost of doing business with that supplier
- **Technology choices are made during development phase**
- **Silicon Labs provides a second source when appropriate to ensure continuity of supply**

Supplier Management

- **Asia-based Assembly and Test Supplier Management**
  - Provides Supplier initial Evaluation, Selection, and on-going Assessment
  - Performs Semiannual Strategic Business Reviews (SBRs) with key suppliers to review overall business, market trends, performance, cost reduction, capacity plans, product roadmaps and specific projects
- **Austin-based Foundry Engineering manages the above for the wafer fab suppliers**
- **Key Suppliers are audited at least annually**
  - Quality management systems (ISO 9001:2015 and IATF 16949:2016)
  - Environmental, Health & Safety (including ISO 14001:2015)
  - Social Accountability (RBA Code of Conduct)
  - Business parameters (delivery, cost, service, capacity)
  - Technology
  - Self assessment from a supplier is occasionally deemed adequate

Supplier Quality Assurance Monitoring Process



Supply Chain Planning Process Overview

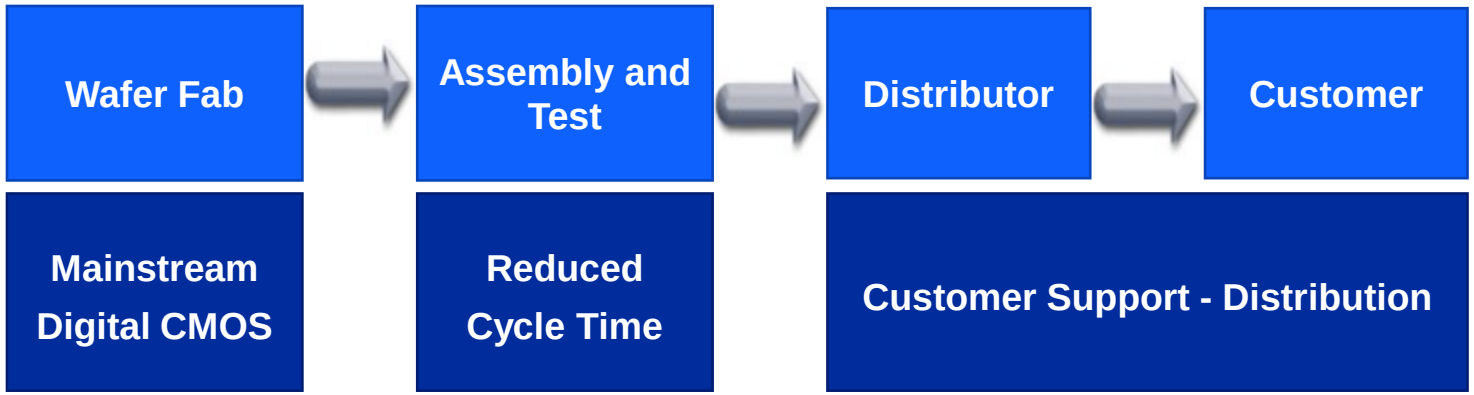
- **Silicon Labs conducts formal, monthly forecast meetings**
  - Distributors/Sales/Representatives required to give 12-month rolling forecast secured from Customers
- **Forecast provides base line for Silicon Labs supply chain**
  - Drives material starts, such as wafer
  - Triggers capacity planning activities
  - Identifies gaps in supply / demand
  - Provides demand snap-shot for inventory management
  - Provides supply / demand snap-shot for product / process management (e.g., PCN planning)
- **Supplier commitments input into the planning system**
  - Commitment is measured to On Time Delivery to First Commit Date in SAP
- **Real-time B2B process flows with key Suppliers and Distributors**

Demand/Supply Performance

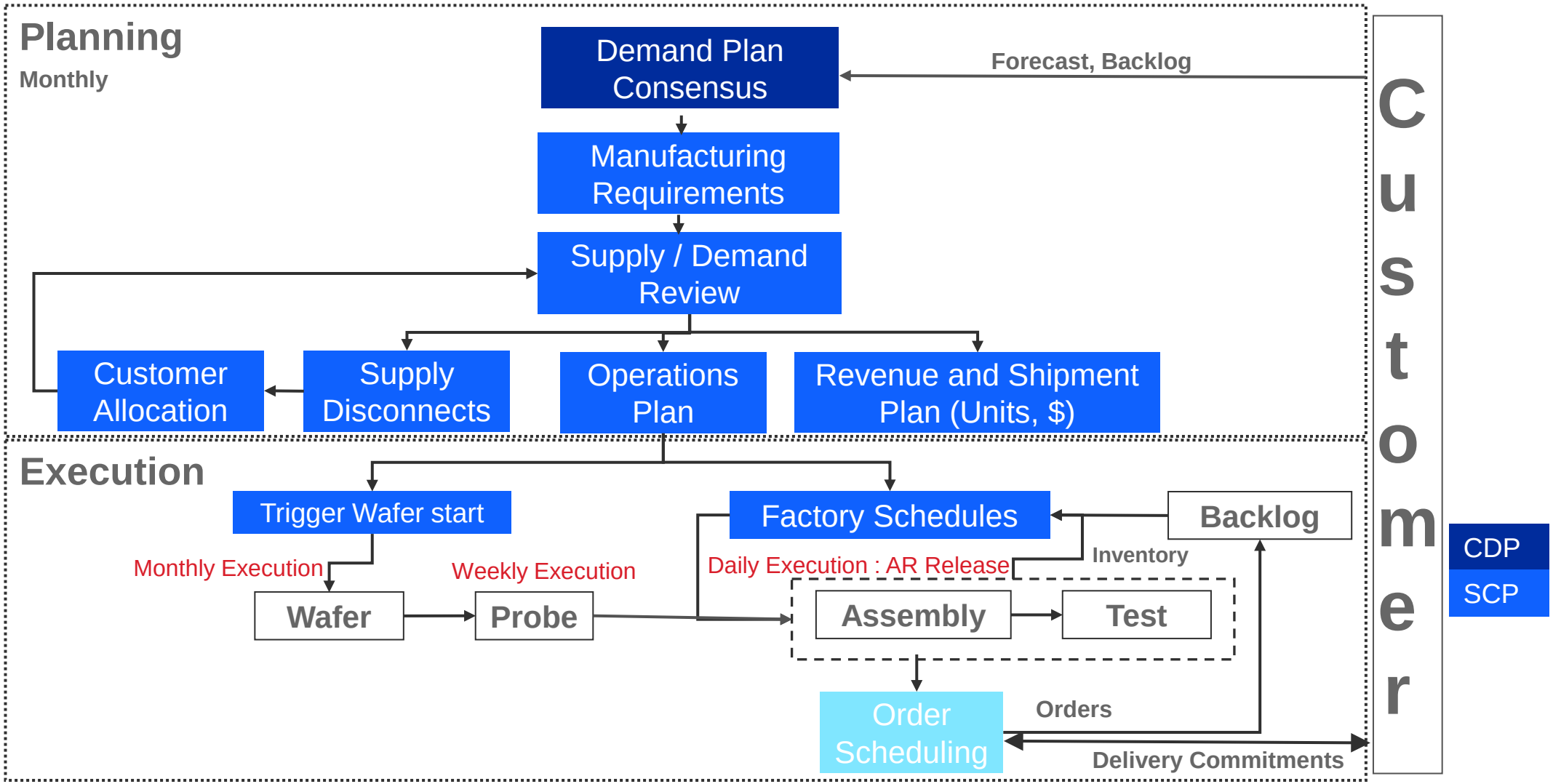
- **Demand**
  - Demand monitoring performed on an on-going, daily basis
  - Review of backlog against the build plan
  - Build plan adjustments made in real time to manage changes at the Customer/part level
- **Supply Chain Metrics**
  - On time delivery to the Customer Requested Dock Date
  - On time delivery to the First Commit Date
  - Units committed vs. units produced
  - Cycle time
  - Early warning (Planned Finish Date <> Scheduled Commit Date)

Silicon Labs Distribution Support

- **Receive weekly POS reports from Distributor**
  - Includes shipments, backlog and forecast
- **Monitor inventory at Distributor monthly**
- **Daily/Weekly communication with Distributor on current issues**
- **Provide latest delivery dates to Distributors on demand via reporting portal**



Supply Chain Process Overview



Packing & Labeling

- **Packing media available: tape & reel, tray and tube**
- **All finished goods are packed in a vacuum sealed Moisture Barrier Bag (MBB), including a Humidity Indicator Card (HIC) and desiccant**
- **Labels are automatically printed from the ERP System (SAP)**
- **Handling Units (HUs) may not contain more than two Batches**

Reel / MBB Inner Box / HU Label	Outer Box Shipping Label
Customer and/or Silicon Labs P/N	Supplier Address
Trans ID#	Customer Address
Date Code / Trace Code	Customer or Silicon Labs P/N
Seal Date	Handling Unit #
Assembly Country	Assembly Country
Quantity	Quantity
MSL, Reflow Temperature, Bake Time, RoHS, “HF” and “Pb-Free” (if applicable) & Plating Type (e#)	“RoHS”, “HF” and “Pb-Free” symbol (if applicable)

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Quality & Environmental Systems

- **Registered to ISO 9001 since Jun'00. Certified to ISO9001:2015 by TUV Rheinland of North America (link)**
- **Registered to ISO14001 since Dec'06. Certified to ISO14001:2015 by TUV Rheinland of North America (link)**
- **Certified Sony Green Partner since Aug'08 (link)**

Quality Policy

Silicon Labs is committed to total customer satisfaction by:

- Providing differentiated products, solutions and services for a more connected world
- Exceeding customer needs through innovation and simplicity
- Continually improving our world-class quality management system

Environmental Policy

At Silicon Labs, we manage environmental matters as an integral part of our business by our commitment to:

- Designing, marketing, and selling environmentally friendly products,
- Continually improving our environmental performance and pollution prevention,
- Complying with applicable legal and other requirements that relate to our environmental aspects, and
- Minimizing the negative environmental impact of our business activities.

Quality Organization

Department Head

- **Senior VP Worldwide Operations**
  - Vice President and Business Executive
    - Quality & Environmental Systems Manager
    - Product Quality Engineering Manager
    - Device Analysis Lab Manager
  - Senior Director, Manufacturing & Quality
    - Supplier & Asia Quality Manager
- **Location**
    - Austin
    - Singapore

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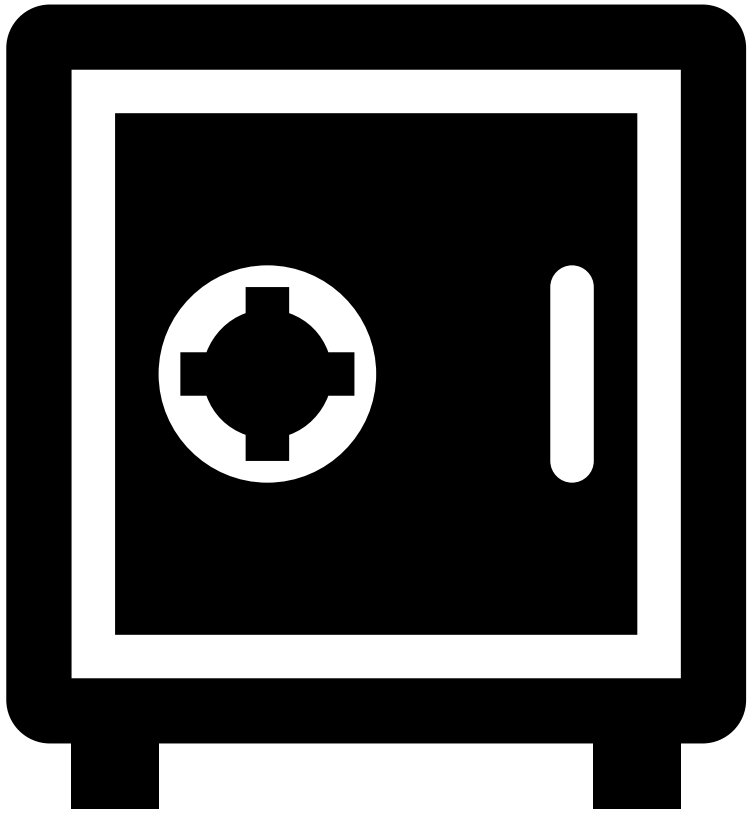
Software Quality Summary

Software Quality Activities

- Software Development is driven by internal Software Quality Policy
- Practices are compatible with multiple standards (e.g., ISO 9001:2015)
- Execution of development is driven by business units
- Software Quality Compliance is assessed by the Quality team
- Evaluation methods include:
  - Internal Audits
  - Metrics, Key Product Indicators (KPIs)
  - Quality Incidents (QIs) and Software Quality Incidents (SQI)
  - Corrective Action Preventive Actions (CAPAs)
  - 3rd party Audits
  - Customer feedback
  - Customer Audits

Secure Software practices



- Silicon Labs has a Product Security Incident Response Team (PSIRT) and Process
- Product Incidents are tracked across business areas, by rate of arrivals, source of discovery, etc.
- Security advisories are issued based on multiple factors of issue involved
- Several security policies and procedures are in place and overseen by our Corporate Security team
- Internal initiatives drive improvements for secure software life cycle activities

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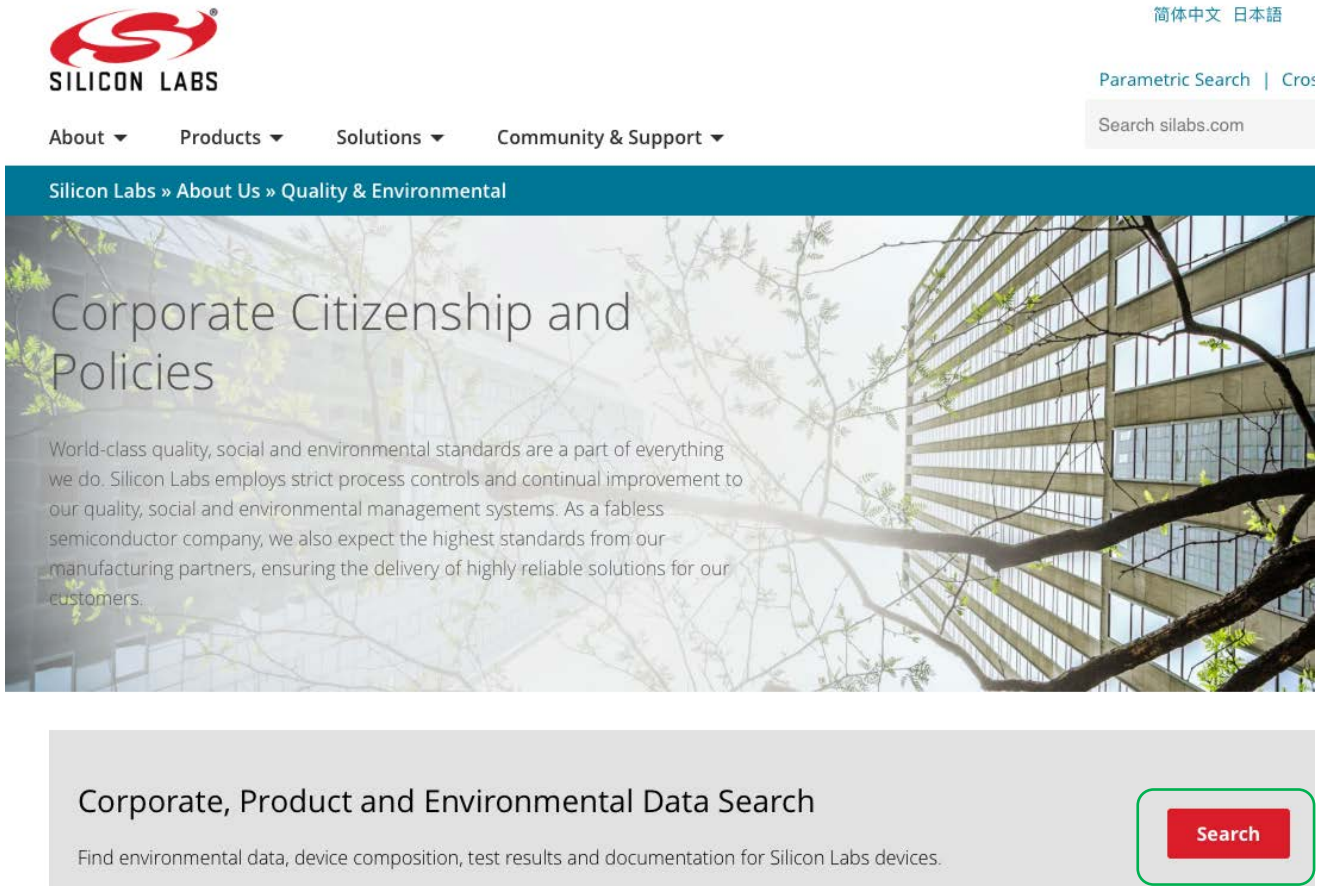
Customer Support – Analysis & Response

- **Corrective Action & Continual Improvement**
  - Based on the Eight Discipline (8D) methodology
- **World Class In-House FA lab**
  - Decap, SEM, FIB capabilities
  - Cooperative with supplier FA capabilities as needed
- **Standard FA and 8D response times per JESD671**
  - Initial Failure Analysis: 7 workdays from suspect product receipt
  - 8D Containment: 5 workdays from customer notification or proof of failure (after Initial FA)
  - Final Failure analysis: 22 workdays from suspect product receipt
  - 8D Root Cause and Corrective Action Plan: 14 workdays from customer notification or root cause discovery (after Final FA)

Customer Support – Materials Data



Self-Serve Part Homogeneous Materials Data

Location: www.silabs.com/quality

(requires registration and login)

After registration, you can access:

- RoHS, Halogen-free, PFOS/PFOA and REACH quick results and Certificates of Compliance
- Downloadable Material Declaration Data sheets (Acrobat pdf sheet or IPC 1752 class 6 XML format)
- Downloadable Homogeneous Materials test results

Customer Support – DA Lab Capabilities

Facility: 1580 sq.ft.

Debug

- 2 u-Probe Stations with various Semiconductor Parameter Analyzers and miscellaneous bench equipment
- QFI Scanning Optical Laser (1064nM & 1340nM) for TIVA/LIVA fault isolation
- QFI Photo Emission Si-CCD (500nm –1000nm)
- QFI MWIR-512 Thermography tool
- Hamamatsu Phemos 1000 EMMI/OBIRCH tool
- Multiprobe AFM Nanoprober
- Kleindieck SEM nanprober
- Optotherm Thermal Camera

ESD Characterization and Qualification

- Barth Transmission Line Pulse Tester
- 2 MK2 ESD and Latchup Testers
- Orion CDM Tester
- HPPI VF-TLP Tester

Imaging Equipment

- 3 High Power Optical Microscopes (1 with confocal capability)
- 2 Low Power Stereo Zoom Microscopes
- Image capture HW/SW for above
- Dual Beam FIB; FEI Helios Nanolab 660
- Jeol 7600 FE-SEM (750 KX max) with EDAX EDS System
- GE Micromex X-ray with 3D-CT capability
- OKOS Scanning Acoustic Microscope (C-SAM)
- Zygo Nexview Optical Surface Profiler

Deprocessing

- Reactive Ion Etcher
- 3 Polishing/Cross-section Stations and 2 ASAP backside milling machines
- Full wet lab for chemical deprocessing, etc.

Customer Support – FAQs

Several categories of frequently asked questions and answers can be found at www.silabs.com/quality including:

- **Corporate** (e.g. Governance, Locations, Financials)
- **Product** (e.g. Qualification, Traceability, Reporting)
- **Environmental** (e.g. Substance Database, Awards)
- **Quality** (e.g. Failure Analysis, 8Ds, ISO 9001:2015 & ISO 14001:2015 Registrations)
- **Operations** (e.g. Logistics, Supplier Management, Ordering)

Thank you!

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