

# Any-Rate Precision Clock Solutions

## ANY-RATE FREQUENCY FLEXIBILITY

**REPLACE** low jitter VCXO-based PLLs

**RECONFIGURE** to support multi-rate applications

**REUSE** simplified by any-rate frequency synthesis



## FEATURES

- Generates any frequency from 2 kHz to 945 MHz and select frequencies to 1.4 GHz from an input frequency of 2 kHz to 710 MHz
- Ultra-low jitter clock outputs with jitter generation as low as 0.3 ps<sub>RMS</sub> (12 kHz to 20 MHz)
- Integrated loop filter with user-selectable loop bandwidth (60 Hz to 8.4 kHz)
- Meets OC-192 GR-253-CORE jitter generation specifications
- Support for ITU G.709 (255/238, 255/237, 255/236) and custom FEC ratios
- Manual or automatic (revertive, non-revertive) input clock selection
- Hitless switching between input clocks in compliance with GR-253-CORE and GR-1244-CORE MTIE specifications
- LOL, LOS and FOS alarm outputs
- User-selectable output clock signal format (LVPECL, LVDS, CML, CMOS)
- Digitally-controlled output phase adjust in 200 ps steps
- I<sup>2</sup>C/SPI programmable or pin controlled
- 1.8, 2.5 or 3.3 V ±10% operation
- Pb-free, RoHS compliant

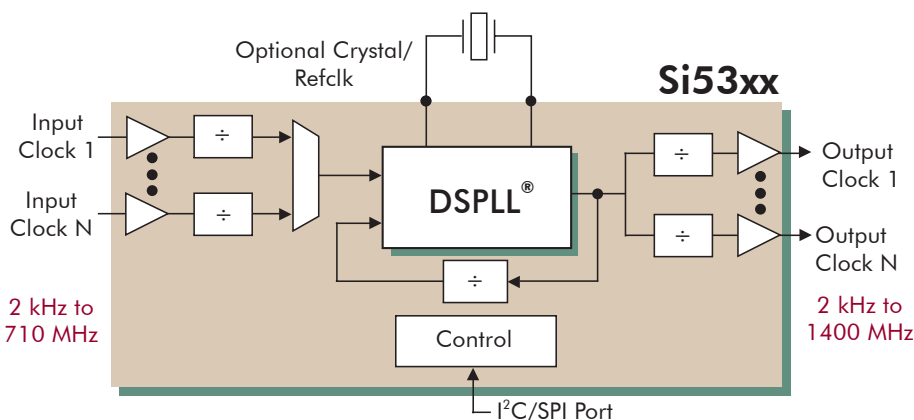
## APPLICATIONS

- SONET/SDH OC-48/OC-192 line cards
- GbE/10GbE, 1/2/4/8/10GFC line cards
- ITU G.709 and custom FEC line cards
- Wireless base stations
- Test and measurement equipment
- Data converter clocking
- DSLAM equipment
- Cable infrastructure
- Optical modules
- SONET/SDH + PDH clock synthesis

## DESCRIPTION

Silicon Laboratories' Any-Rate Precision Clocks provide clock multiplication, jitter attenuation and clock distribution in high-performance timing applications requiring sub 1 ps jitter performance. The devices accept multiple clock inputs ranging from 2 kHz to 710 MHz and generate multiple independent, synchronous clock outputs ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. Microprocessor controlled devices provide virtually any frequency translation combination across this operating range. For ease of use, pin-controlled devices are preconfigured to support popular SONET/SDH, Ethernet, Fibre channel and HDTV frequencies. The any-rate precision clocks are based on Silicon Labs' third-generation DSPLL<sup>®</sup> technology, which provides any-rate frequency synthesis and 0.3 ps<sub>RMS</sub> jitter performance in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components.

## Si53xx BLOCK DIAGRAM



## SOLUTIONS GUIDE

**ANY-RATE  
FREQUENCY SYNTHESIS  
IN A SINGLE IC**



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## ANY-RATE FREQUENCY FLEXIBILITY

### High Performance

The Si53xx is the industry's first jitter attenuating clock multiplier IC that provides any-rate frequency synthesis. With jitter performance of 0.3 ps<sub>RMS</sub> typ, the Si53xx rivals the best jitter performance available using discrete analog PLL technology.

### Highly Integrated

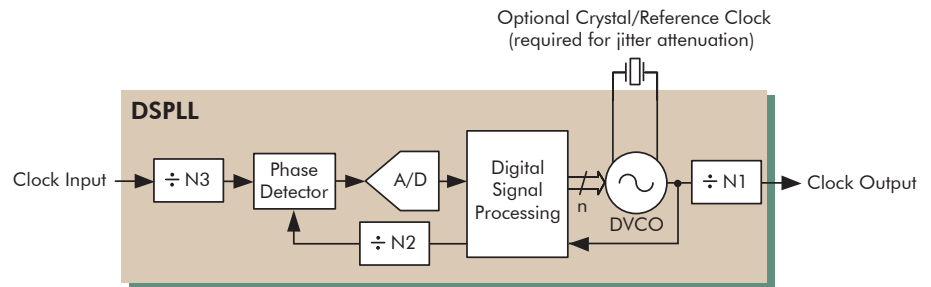
The highly integrated Si53xx contains all the key components of a high-performance analog PLL on chip, including an ultra-low phase noise voltage-controlled oscillator (VCO), loop filter, phase detector, divider and buffers. Because all PLL components are integrated, board-level noise immunity is improved versus discrete solutions. With up to four clock inputs and five differential clock outputs available, the Si53xx eliminates the need for external muxes and clock distribution buffers, further reducing BOM part count and cost.

### Easy-to-Use

The Si53xx frequency plan is easily reconfigurable using pins or an I<sup>2</sup>C/SPI interface, simplifying design reuse. The Si53xx integrates system-level clock features including hitless switching, automatic (revertive, non-revertive) clock control, holdover, selectable output clock signal formats and programmable output clock phase control.

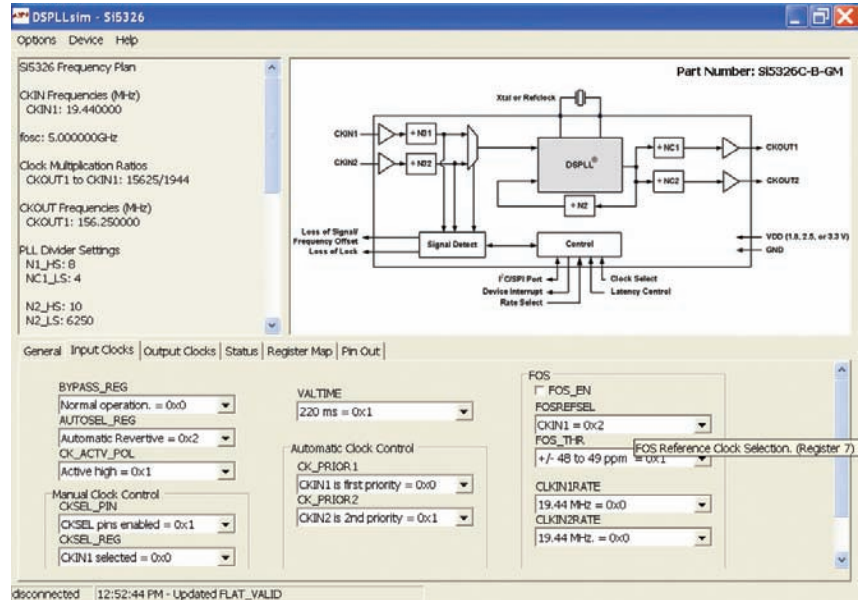
## Innovative DSPLL Technology

Silicon Labs' proprietary DSPLL technology uses digital signal processing (DSP) techniques to move traditionally analog PLL functions into the digital domain. The Si53xx integrates a high-performance, low phase noise VCO, loop filter, phase detector, dividers, input clock selection mux, and flexible output buffers on-chip, replacing discrete analog PLL implementations.



### DSPLLsim

DSPLLsim is a PC-based software utility used to simplify device selection and configuration. It also determines valid frequency plans and optimum PLL divider and loop bandwidth settings.



## Any-Rate Jitter Attenuating Clock Multipliers

| Part Number | Clock Inputs | Clock Outputs | Control                 | Jitter Gen (12 kHz to 20 MHz) | Programmable Loop Bandwidth | Clock Multiplication | Hitless Switching | Alarms        | Package                |
|-------------|--------------|---------------|-------------------------|-------------------------------|-----------------------------|----------------------|-------------------|---------------|------------------------|
| Si5316      | 2            | 1             | Pin                     | 0.3 ps <sub>RMS</sub> typ     | 60 Hz – 8.4 kHz             | —                    | —                 | LOL, LOS      | 6x6 mm, 36-pin QFN     |
| Si5323      | 2            | 2             | Pin                     | 0.3 ps <sub>RMS</sub> typ     | 60 Hz – 8.4 kHz             | Yes                  | Yes               | LOL, LOS      | 6x6 mm, 36-pin QFN     |
| Si5326      | 2            | 2             | I <sup>2</sup> C or SPI | 0.3 ps <sub>RMS</sub> typ     | 60 Hz – 8.4 kHz             | Yes                  | Yes               | LOL, LOS, FOS | 6x6 mm, 36-pin QFN     |
| Si5366      | 4            | 5             | Pin                     | 0.3 ps <sub>RMS</sub> typ     | 60 Hz – 8.4 kHz             | Yes                  | Yes               | LOL, LOS, FOS | 14x14 mm, 100-pin TQFP |
| Si5368      | 4            | 5             | I <sup>2</sup> C or SPI | 0.3 ps <sub>RMS</sub> typ     | 60 Hz – 8.4 kHz             | Yes                  | Yes               | LOL, LOS, FOS | 14x14 mm, 100-pin TQFP |

## Low Jitter Clock Multipliers

| Part Number | Clock Inputs | Clock Outputs | Control                 | Jitter Gen (12 kHz to 20 MHz) | Programmable Loop Bandwidth | Clock Multiplication | Hitless Switching | Alarms   | Package                |
|-------------|--------------|---------------|-------------------------|-------------------------------|-----------------------------|----------------------|-------------------|----------|------------------------|
| Si5322      | 2            | 2             | Pin                     | 0.6 ps <sub>RMS</sub> typ     | 30 kHz – 1.3 MHz            | Yes                  | —                 | LOS      | 6x6 mm, 36-pin QFN     |
| Si5325      | 2            | 2             | I <sup>2</sup> C or SPI | 0.6 ps <sub>RMS</sub> typ     | 30 kHz – 1.3 MHz            | Yes                  | —                 | LOL, FOS | 6x6 mm, 36-pin QFN     |
| Si5365      | 4            | 5             | Pin                     | 0.6 ps <sub>RMS</sub> typ     | 30 kHz – 1.3 MHz            | Yes                  | —                 | LOL, FOS | 14x14 mm, 100-pin TQFP |
| Si5367      | 4            | 5             | I <sup>2</sup> C or SPI | 0.6 ps <sub>RMS</sub> typ     | 30 kHz – 1.3 MHz            | Yes                  | —                 | LOL, FOS | 14x14 mm, 100-pin TQFP |