

Optimizing System Operation Using a Flexible Digital PWM Controller

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Abstract - This paper describes a mixed-signal integrated circuit implemented in low-cost CMOS technology optimized for dc/dc and ac/dc converter applications. The device is partitioned into a hardware digital controller comprised of a digital signal processor (DSP) controller and an instruction-based microcontroller (MCU) system management processor section. The hardware digital controller includes a high-speed differential analog-to-digital converter (ADC), a low temperature-coefficient voltage-reference digital-to-analog converter (DAC), a programmable infinite-impulse response compensator, a digital pulse width modulator (DPWM) finite state machine and necessary protection circuits (e.g., current limiting circuits) to perform a high-bandwidth fully independent control loop function. The MCU-based system management processor section includes an 8-channel self-sequencing ADC, a 50 MIPS 8051-based MCU with 64K bytes of program memory and four 16-bit timers to perform medium bandwidth control loop and system monitoring functions. Other system functions include a high-precision oscillator, phase-locked-loop (PLL) based clock multiplier, UART and GPIO ports making a flexible system-on-a-chip solution for a wide range of power supply applications. This architecture generates a throughput that exceeds a DSP-only solution by moving system task loading away from the processor. Examples of several applications are also presented.

Introduction

Digital power supply control offers system performance, efficiency and cost advantages over traditional analog approaches. Performance gain is made possible through adaptive and non-linear control response, such as manipulating switching waveforms on-the-fly to achieve dynamic performance optimization. Higher efficiency is obtained through digital optimization, compensation and mode switching. From the power supply manufacturer's point-of-view, cost reduction results from a lower external component count. At the same time, reliability is improved with the elimination of external analog components, which pose aging and drifting concerns. In-system programmability provides the manufacturer the ability to generate more product variants primarily through software modifications. A fully independent hardware-based digital controller provides a stable digital control loop that has user definable parameters that, once defined, are determinative of the overall power supply operation. The on-chip MCU adds intelligence to the power supply by monitoring the operation of the digital controller during operation and, if necessary, reparameterizing the digital controller to effect temporary or permanent changes to the operation thereof. The MCU operates to: 1) monitor fault situations such as over current, under voltage, over voltage and over temperature, 2) control power supply start up, shut down and current sharing, etc.

Digital control has been widely used in motor applications where control complexity and monitoring features are high. Because of lower operating switching frequencies, a general purpose MCU or a DSP is ideal for this type of application. For practical reasons, in switched-mode power supplies it is desirable to reduce both passive component size and transient response time. Thus, the operating switching frequency has to be increased to a range of hundreds of kilohertz to megahertz. Smaller inductor size and faster dynamic response associated with such applications demands that the digital controller operate at higher processing speeds. However, in order to be commercially successful, the digital controller must be low cost and low complexity (to minimize the learning curve of system design-in) and still deliver high performance. This argues against a fully DSP solution, with its inherent time consuming and complex programming requirements

The first section of this paper describes the detailed chip architecture and demonstrates its control flexibility. The last section describes four digital-control power supply applications: dynamic power efficiency optimization, digital current sensing, transient-triggered non-linear control and digital power-factor correction.

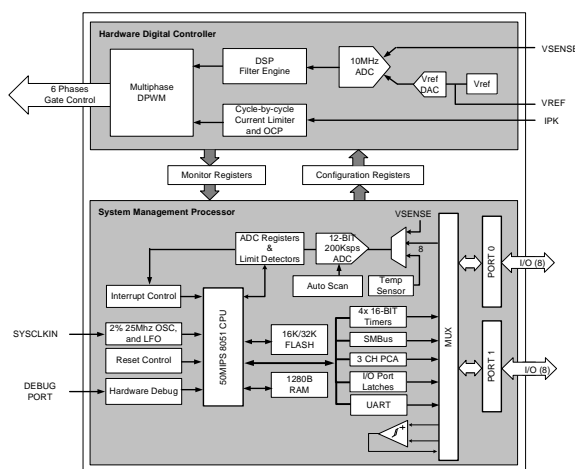


Fig. 1. Digital Power Supply Controller Block Diagram

Chip Architecture

Figure 1 shows a block diagram of a flexible digital power supply controller designed to address a wide range of switched mode power supplies applications including isolated dc-dc converters, non-isolated dc-dc converters and power factor correction rectifiers. The device is partitioned into a power supply specific hardware block DSP to provide a high bandwidth, fully independent digital control loop function and a software programmable system management processor

and input of reference DAC. Channel 1 is useful in standby or soft start applications where lower bandwidth control is preferable. Channel 2 is a 2's complement zero input for use in system debug. Channel 3 is written directly by the MCU for low bandwidth control loop applications.

DSP Filters and Dithering

The digital control loop front-end data at the output of the differential ADC is processed by a DSP filter, which provides necessary compensation to maintain adequate control-loop phase margin. The DSP filter consists of a cascade of a proportional-integral-derivative (PID) filter and low-pass filter as shown in Figure 4. All coefficients are dynamically programmable enabling the system management processor section to optimize control loop response in situations such as changes in loading conditions and input voltage. One of two low-pass filters can be selected through the configuration register for use by the PID filter. Both low-pass filters are useful in removing high frequency power supply noise caused by the zeros of the PID filter.

The PID filter output is a sum of the proportional gain (K_p), the integration gain (K_i) and the derivative gain (K_d) terms derived from the error signal of the differential ADC. Increasing the proportional gain increases the power supply response to changes in the error signal but decreases system damping and stability. Step response overshoot and ringing could be caused by too large a value of the proportional gain term. Unlike proportional gain (which reduces instantaneous error), integral gain reduces steady state error to zero. The amount of time the power supply takes to reach its steady state condition is inversely proportional to the integral gain. Instability and oscillation can also be caused by too large a value of the integral term. Should the integrator input not achieve a zero value, integration will continue until the integrator output is saturated at a maximum or a minimum. This integrator wind-out adversely affects control loop response because the integrator requires additional recovery time to return to its normal operating range as the loop attempts recovery. One cause of wind-out is cycle-by-cycle current limiting which truncates the PWM duty cycle. During this event, the integration action can be inhibited. The derivative term improves stability, reduces step-response overshoot and reduces step-response time. The derivative term is proportional to the rate of change of the error signal and therefore improves controller reaction time by predicting changes in the error. Following an output disturbance, the supply output returns to its nominal value at a faster rate as K_d increases. However, output overshoot can be caused by too much damping from the derivative term. An output disturbance is introduced when the load is suddenly connected to the supply output, causing an increase in output current and a decrease in output voltage. The proportional and derivative outputs react immediately to correct the error. By comparison, the integrator output moves slower, but provides precise control to return the output of the supply to its nominal value.

The PID transfer function provides one pole and two zeros. The output of the PID filter is passed to one of two low-pass filters. The first low-pass filter has two programmable poles and one zero at one-half of the sampling frequency. This filter's high sampling rates, typically 10MHz, updates the

DPWM multiple times in a given switching cycle to provide for fast transient response. This filter also has a non-unity DC gain to allow a transient interrupt routine to temporarily boost control loop gain for faster recovery. The second low-pass filter, also known as decimation SINC filter, has multiple zeros, which can be chosen to place at the DPWM switching frequency and its harmonics to minimize switching noise of the power supply in the control loop.

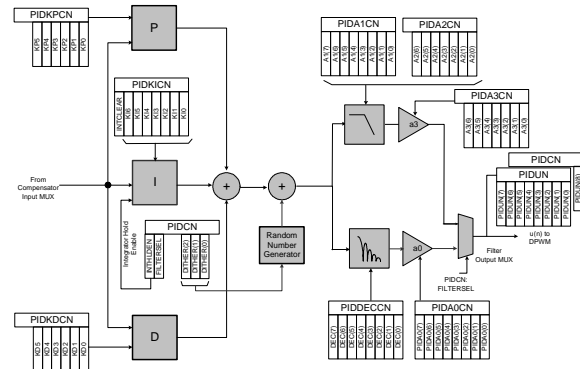


Fig. 4. DSP compensator block diagram

Dithering controls low frequency oscillation tones by breaking up limit cycle sequence and improves effective resolution of the DPWM without increasing clock frequency beyond practical levels. The dither has a Gaussian noise distribution property and is generated digitally by a linear feedback shift register.

DPWM

The DPWM generates up to six timing phases that can be hardware or software modulated in real time. The DPWM is designed to accommodate an isolated or non-isolated power supply topology, which provides the user the flexibility to apply different phase modulation schemes to the power supply. The flexibility of the DPWM relies on the fact that phase-to-phase timing can be programmed for a fixed dead time, or the system management processor section can dynamically vary the dead time during converter operation to account for temperature, loading and input voltage variation. The DPWM can be clocked at 25MHz, 50MHz or 200 MHz.

As shown in Figure 5, the main input of the DPWM is $u(n)$ from the compensator output MUX, this value representing a duty cycle. The multiplexer, the DPWM input MUX, selects either the output of the DSP filter or a software generated output from the system management processor section as the DPWM modulation source. The MUX input is connected to a pair of registers to control a symmetry locking function. This symmetry locking function is useful in applications where the duty cycle of the DPWM is slaved to a selected master pulse. The symmetry lock output is connected to a plurality of limiter circuits which allows the system management processor section the ability to offset and set limits of $u(n)$, which results in setting minimums and maximums for the duty cycle of the output gating pulse. This results in up to four individual corrected $u(n)$ functions. The heart of the DPWM is a finite-state-machine (FSM) based timing generator, each edge of each phase of the DPWM having a separate FSM provided for the control thereof. Each edge of each phase output of

DPWM has a timing dependency on any of the other DPWM phases or on itself. The dependency is set up by initiation of individual configuration registers for each FSM. Once initialized, the input to each FSM is hardware-modulated to select from one of the four corrected $u(n)$ functions, and each $u(n)$ can be fed into the timing generator of each FSM. Positive, negative or MCU-controlled phases, overlapping or non-overlapping, can be implemented with this architecture.

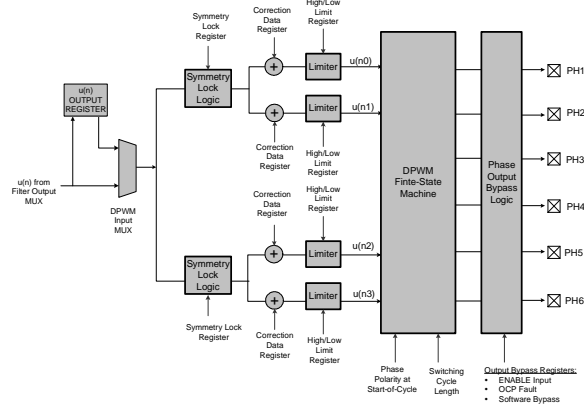


Fig. 5. DPWM block diagram

As shown in Figure 6, each edge of each phase is controlled by one of either a $u(n)$ -modulated, an absolute or a relative command to construct the output pulse of each phase. By providing this FSM-based architecture, each edge of each phase output pulse can be defined separately so as to generate the associated edge virtually independent of the other edges. With such an architecture based in hardware, each FSM decision requires only one or two clock cycles as compared to an instruction-based engine.

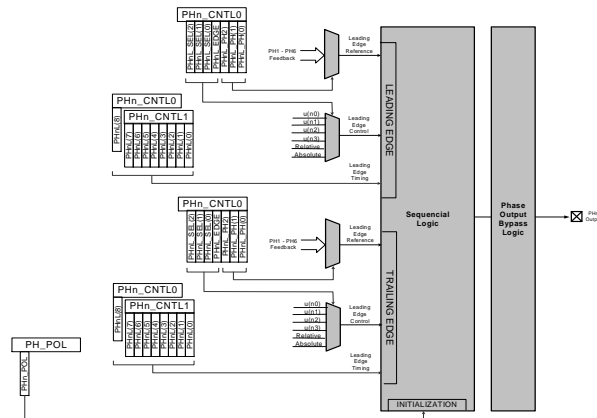


Fig. 6. DPWM finite-state machine block diagram ($n=1, 2, 3, 4, 5$ or 6)

Phase output bypass logic provides safe stop states for all phase outputs in the event of a predetermined existing condition. When this predetermined condition occurs, the bypass logic overrides the DPWM output by forcing each phase output into user-defined states during power supply shutdown, thus placing the power supply in a “known safe state.” The bypass logic can be programmed to occur

automatically during over-current protection or when an external pin is enabled. The bypass operation can also be initiated by the system management processor section in software. Each of these bypass conditions have an associated programmable stop pattern.

System Management Processor Section

The system management processor section, shown in Figure 1, implements a standard 8051 organization and peripherals. The MCU core employs a pipelined architecture that executes most if its instructions in one or two system clock cycles; and the MCU is capable of running at 50MHz, and has a peak throughput of 50MIPS.

The analog front-end of the MCU consists of a 12-bit, 200ksps ADC and associated auto sequencing logic, limit registers and temperature sensor. The ADC has 8 input channels, and each channel has a corresponding output register and limit detector. The limit detectors compare the converted output to user-programmed limits and generate an MCU interrupt when these limits are exceeded. The ADC is also equipped with auto sequencing logic, which does not require MCU supervision during data conversion. The auto-sequencing feature automates the analog data acquisition process and enables system protection functions, such as input over-voltage protection, input under-voltage lockout, output voltage monitoring and over-temperature protections, to be implemented in firmware. The MCU has an internal temperature sensor, which monitors chip temperature from -55C to 125C. The temperature monitoring is also useful in providing necessary compensation to optimize power efficiency of switchers and gate drivers.

The system management processor section also features four counter/timers for use with device peripherals or for general purpose use. Other system functions include a high-precision oscillator, a PLL-based clock multiplier, a UART and two GPIO ports.

Application #1 - Power efficiency optimization

An integrated digital power supply controller has the potential to provide different ways to optimize power efficiency. In some digital-based systems, such as CPUs and DSPs, higher processing speed can be achieved with an increase in power supply voltage while standby-mode operation only requires a lower processing speed. In this case, power supply voltage can be dynamically adjusted to minimize total power consumption. In a switched mode power supply, it is desirable to maintain high power efficiency over a wide range of loads. The power saving operation could possibly be implemented by applying pulse skipping, pulse frequency modulation scheme, switching between buck and synchronous-buck conversion or switching between continuous and discontinuous conduction modes. The bypass logic in the device allows pulses to skip switching cycle(s). The programmable switching cycle length and DPWM input MUX provides a means to modulate the switching frequency under lighter loads. A discontinuous conduction mode at lighter loads is realized by turning the synchronous rectifier of the supply off when the inductor current crosses zero. In a low output voltage switched power supply based on synchronous buck, the adaptive dead-time adjustment can minimize loss due to body diode conduction

and short-circuit currents of power switches. Figure 7 illustrates a mesh plot of dead times of a synchronous buck when optimized by using a close-loop search algorithm for a minimum duty cycle.

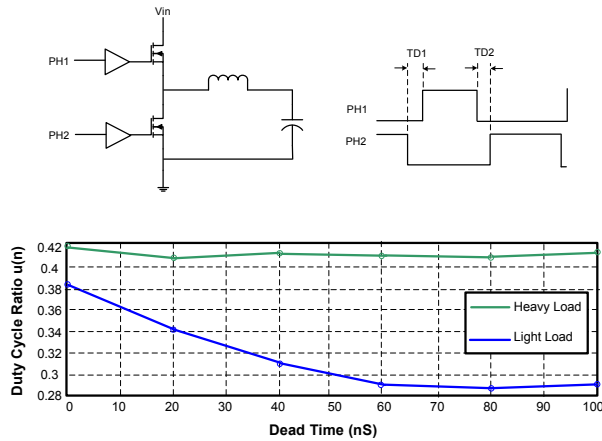


Fig. 7. Digital dead time optimization

Application #2 - Digital current sensing

Inductor current sensing is useful in applications such as over-current protection, current-mode control, current sharing and providing necessary information to optimize power supply efficiency. Figure 8 illustrates lossless current sensing by the technique of digital-filtering the voltage across the inductor of a bulk converter.

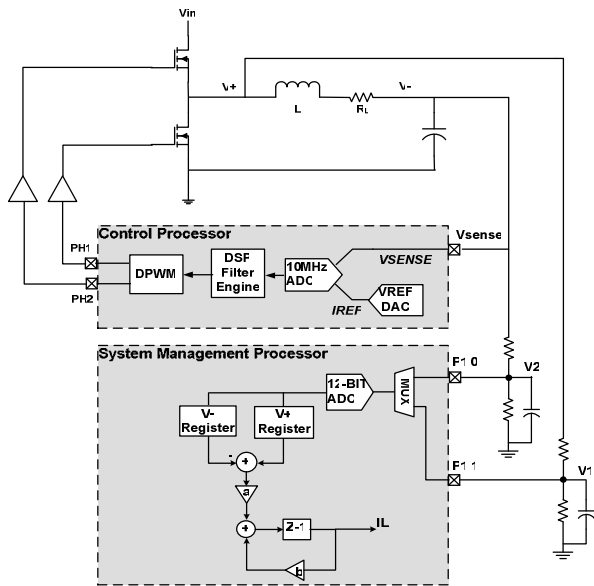


Fig. 8. Digital current sensing

Application #3 - Transient-triggered nonlinear control

In steady state operation, due to the high DC gain of PID filter integrator term, the output of the differential ADC will typically operate between ± 1 LSB range. A perturbation at the power supply output causes the ADC output to move beyond this range. In this case, the transient detector monitors

the output of the differential ADC and generates an interrupt to the system management processing section when the output of the differential ADC exceeds a user-defined range. The transient detector interrupt can trigger a change in loop compensation or simply increase the compensator gain. However, widening loop bandwidth can lead to instability. A detecting method shown in Figure 9 can be used to detect an actual onset of instability. The system management processing section monitors the pattern of the output voltage error signal after transient detection is executed. Upon detection of instability, the gain of the programmable DSP compensator is reduced and the system returns to a regulation with a slower dynamic response but with adequate phase margin.

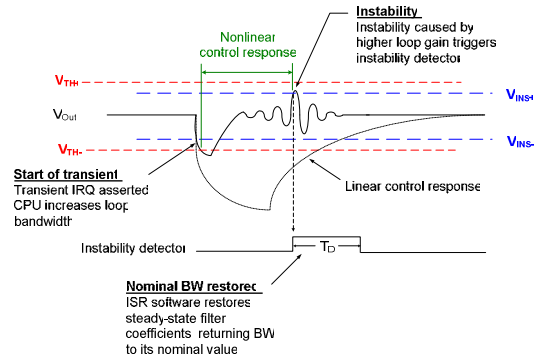


Fig. 9. Transient with nonlinear control

Application #4 - Digital power factor correction

Figure 10 illustrates an implementation of a digital power factor correction pre-regulator. The high bandwidth current loop is handled by the hardware digital controller while the slower voltage loop is handled by system management processing section.

Conclusion

In this paper, we discussed the architecture of a digital power supply controller chip, implemented in low-cost CMOS technology, consisting of a hardware-based mixed signal DSP providing the core digital control functionality and an instruction-based processing section having an 8051-based MCU at the heart. The hardware digital controller handles high-bandwidth control loop function. The MCU-based processing section handles the medium bandwidth control-loop and housekeeping functions. Other system functions include an internal oscillator, a PLL clock multiplier, a program storage non-volatile memory, a UART and GPIO ports making a complete highly versatile system-on-a-chip solution for a wide range of power supply applications. This architecture generates a throughput that exceeds a DSP-only solution by moving system task loading away from the instruction-based processor.

This flexible architecture allows applications in dc-dc converters, ac-dc power factor correction regulators, isolated and non-isolated switched power supplies where high efficiency, high speed, high dynamic response, control complexity and cost are critical.

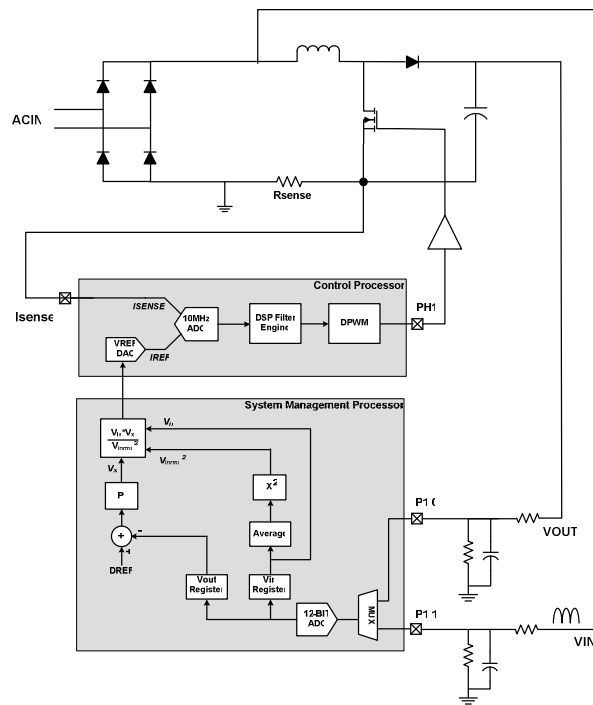


Fig. 10. Digital power factor correction rectifier