Si5315
Synchronous Ethernet
Jitter Attenuating Clock Multiplier IC

December 2008

One Stop for Customers' Timing Needs

Any-Rate Silicon Oscillators

Single/Dual/Quad/Any-Rate XO/VCXOs

Any-Rate Clock Generators/Buffers

Any-Rate Precision Clocks

Synchronous Ethernet Clocks

Broad portfolio based on proprietary DSPLL™ and MultiSynth technology: 51 patents issued, 36 pending

- **Only supplier serving both frequency control & clock markets**
- **Unique portfolio based on phase-locked loop (PLL) expertise**
  - Synchronous Ethernet clock multipliers / jitter attenuators
  - Any-rate clock multipliers / jitter attenuators
  - Any-rate clock generators / clock buffers
  - Precision, high frequency XO/VCXOs
  - Precision, I^2C programmable XO/VCXOs
  - All silicon crystal-less oscillators

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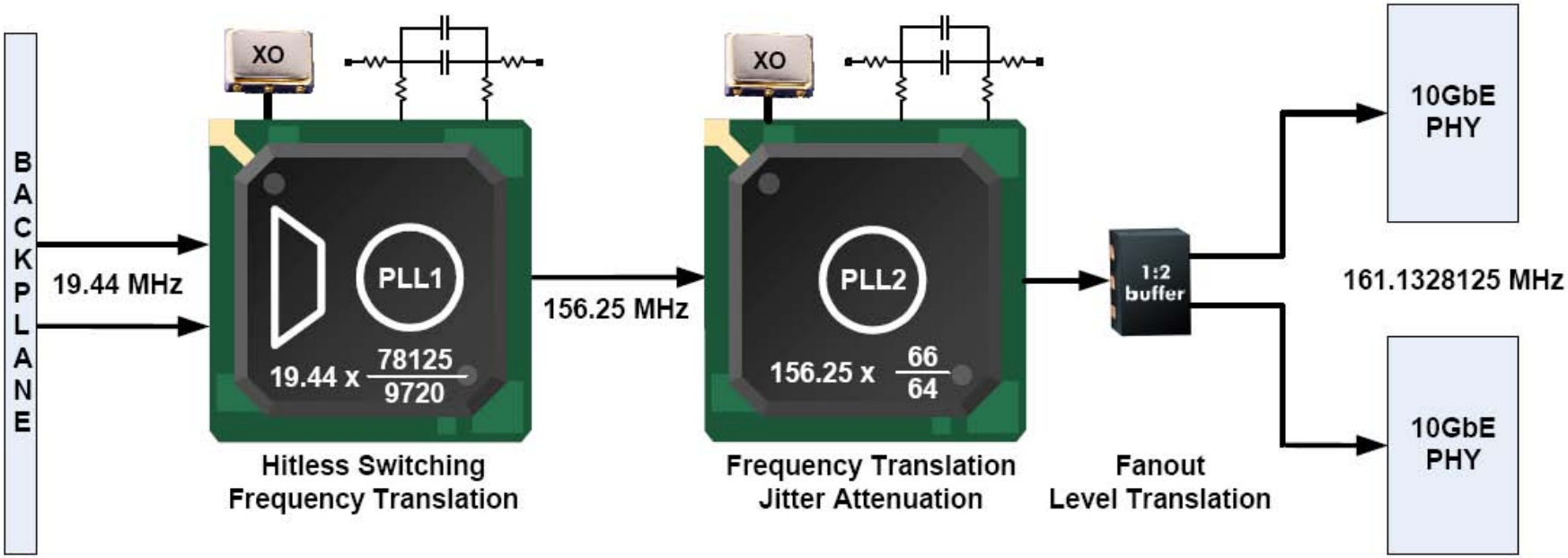
SyncE Line Card Timing Challenges



- Current architectures not optimized for frequency agility, performance or size
  - Frequency translation from telecom backplane clocks to 10GbE PHY reference clocks requires 2 PLLs
  - External components required to provide complete SyncE timing architecture
  - Limited frequency flexibility

Introducing the Si5315 SyncE Clock Multiplier

- **Single clock solution for all SyncE applications**
  - Frequency flexibility enables design reuse for Carrier Ethernet, Wireless Backhaul and Telecom Access
  - Frequency flexibility simplifies BOM by replacing multiple clock ICs
  - Industry's only SyncE clock IC supporting 10GbE line encoding rates
- **First SyncE clock solution providing margin to stringent jitter requirements of all GbE and 10GbE PHYs**
  - Insures first pass design success
- **Fully integrated and easy to use**
  - No external PLL components, simplifying layout & BOM
  - Immune to board level noise sources, eliminating possible board respins
  - Pin controlled, simplifying device configuration & improving time to market

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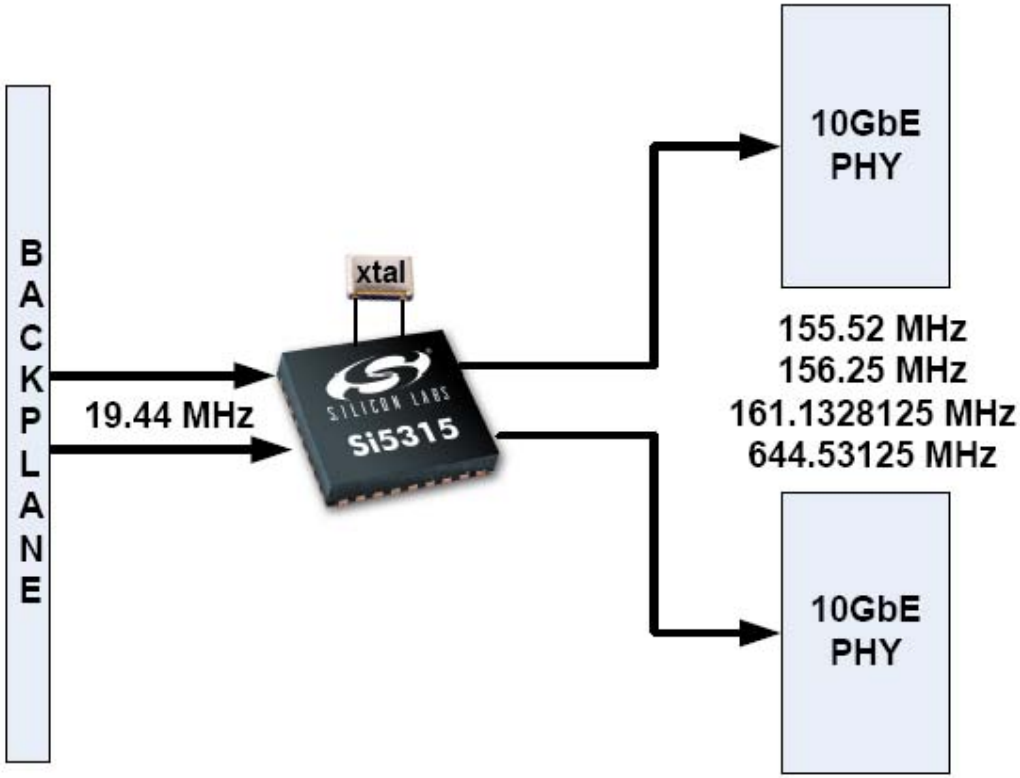
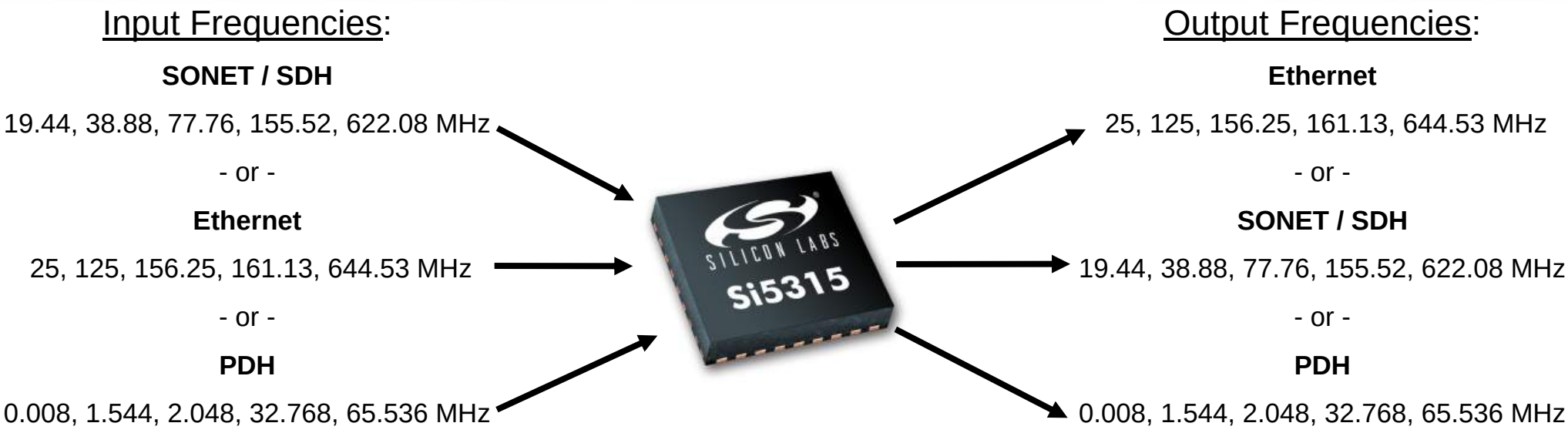
Si5315 Simplifies SyncE Line Card Design



- Frequency flexibility enables replacement of multiple clocks and XOs with a single device
- Ultra low jitter clocks provides extra jitter margin for 10GbE
- Simplifies design while minimizing space, cost

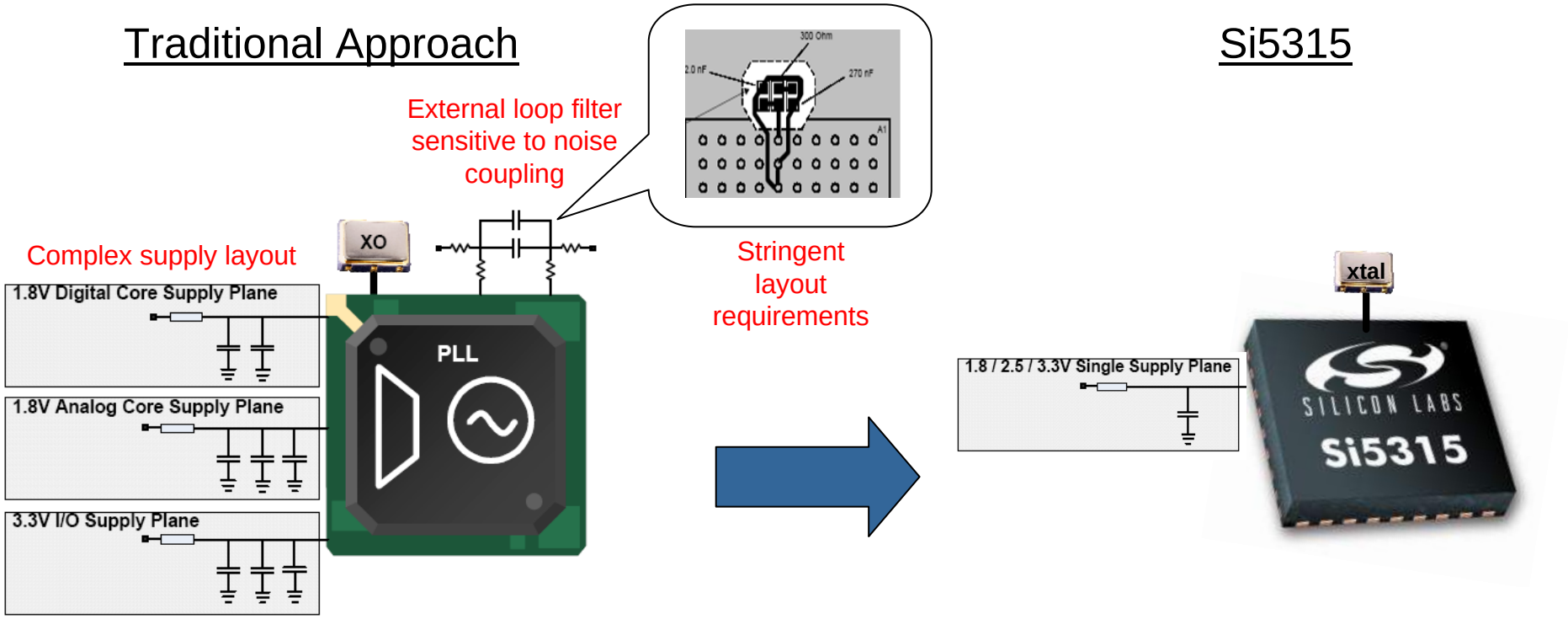
Frequency Flexibility Reduces Complexity



- **Easily bridges frequency translation between legacy telecom and Ethernet**
  - Single device supports all translations reducing BOM and design time
  - Supports 10GbE 66/64 line encoding rates, eliminating cost of expensive VCXO modules
  - Eliminates multiple PLLs saving board space and BOM

- **Industry's lowest jitter clock IC (25% less than existing solutions)**
  - Only solution supporting requirements of all GbE and 10GbE PHY solutions
  - Margin simplifies design and insures first pass success

Smallest Overall Footprint



- **Si5315 provides highly integrated solution**
  - Simplifies PLL design and layout
  - Improves noise immunity
  - Occupies 40% less PCB real estate than competitive solutions
  - Single supply operation

Si5315 Target Applications

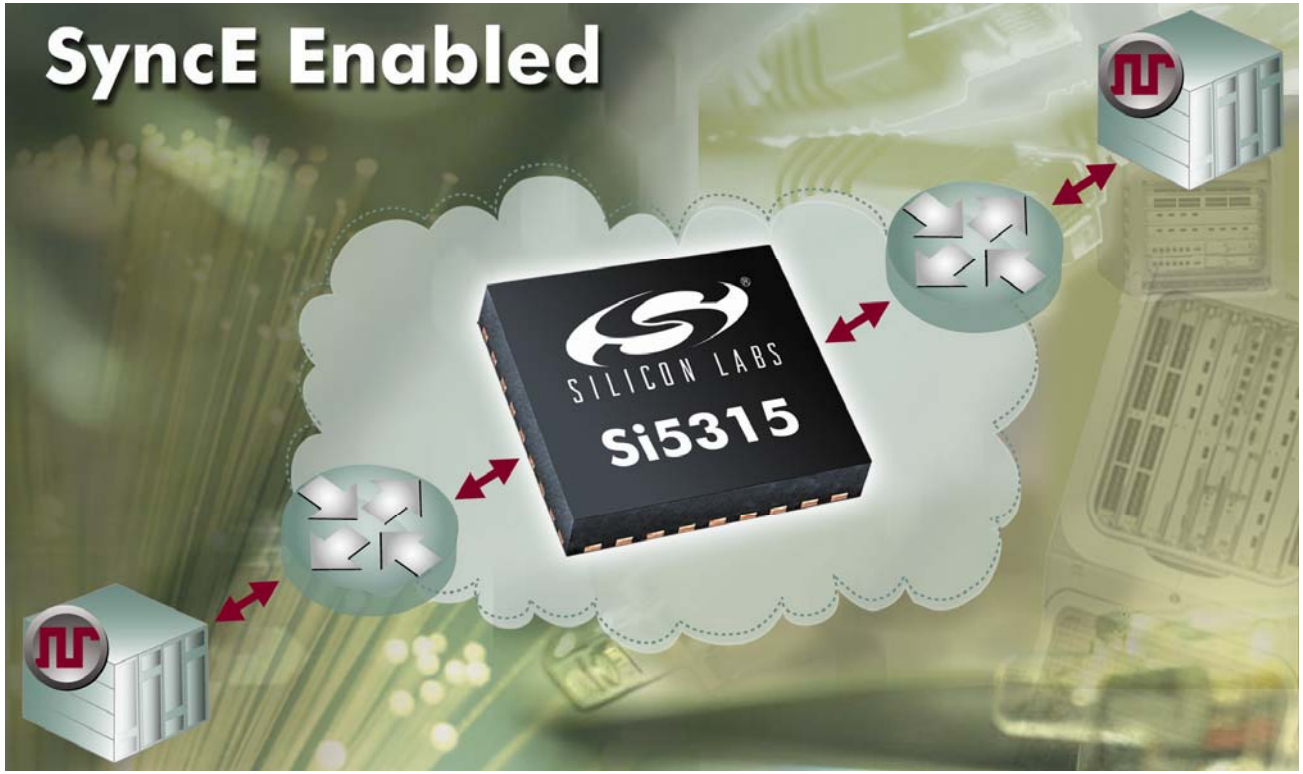
Passive Optical Networking

Carrier Ethernet Switches/Routers

Wireless Backhaul

- Si5315 addresses SyncE timing applications in Carrier Ethernet and rapidly growing PON and wireless backhaul

Summary



- **Industry's lowest jitter SyncE clock multiplier IC**
- **Simplifies SyncE frequency translation**
- **Easy to use and highly integrated in a small overall footprint**

www.silabs.com/timing