

A Versatile Monolithic Digital PWM Controller

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I. Introduction

Digital control promises significant system performance gains resulting from complex control algorithms that are difficult to implement in analog [1,2,7,12]. Digital control has reduced susceptibility to component tolerances. For example, a digital filter can precisely position poles and zeros to the frequency tolerance of the system clock, whereas component tolerances result in 10% or higher pole/zero variations in an analog controller. Another example is found in multiphase supplies, where a digital pulse width modulator (DPWM) can provide very accurate matching among duty cycles for different phases [2,3]. Other advantages include programmability, reduced development time, decreased component count, lower susceptibility to component aging and environmental conditions, improved manufacturing logistics and, ultimately, lower cost.

Unlike analog control, digital control introduces latency due to feedback parameter quantization and calculation times [2]. To minimize these delays, digital control functional blocks are characterized by high data throughput and low latency, in particular the loop compensation and DPWM modulation algorithms. While various implementations have been reported [1]-[12], the most common digital controller implementations can be grouped into three major types: programmable signal processor (typically a digital signal processor (DSP)), custom hardware, or some combination of both.

The DSP executes discrete time calculations of control variable values in real time [3]. Some suppliers offer DSPs with Flash memory allowing the user to address multiple system topologies and control strategies with a common processor platform. However, this approach is limited by DSP throughput, which, in turn, is limited by the DSP clock frequency and memory resources. These factors adversely impact cost, size, supply current and scalability at higher DPWM frequencies.

The dedicated hardware-based approach uses fixed-architecture state machines to execute the control algorithm [9, 12]. Hardware can be optimized for cost and performance making this a potentially lower-cost and more efficient approach than the DSP. However, this approach lacks flexibility because the control hardware cannot be significantly changed once fabricated. Therefore, the hardware must be designed for a specific end application, which adversely impacts non-recurring engineering cost and time-to-market and increases design risk.

The approach presented in this paper combines processor and fixed hardware architectures, extracting maximum benefit from each. The described architecture uses dedicated programmable signal processors to perform high-speed control calculations under the supervision of a Flash-programmable microcontroller (MCU). The signal processors provide minimum latency calculations and

offer excellent die area efficiency. The integrated MCU makes the controller very flexible and enables user firmware to precisely set and modify system attributes (i.e. frequency compensation and system protection) and enhance system performance using low-frequency control optimization (e.g. dead time control to enhance efficiency). Because the MCU does not perform high-bandwidth calculations, it can be lower cost and easier to program than a DSP for even greater commercial viability.

II. Controller IC Architecture

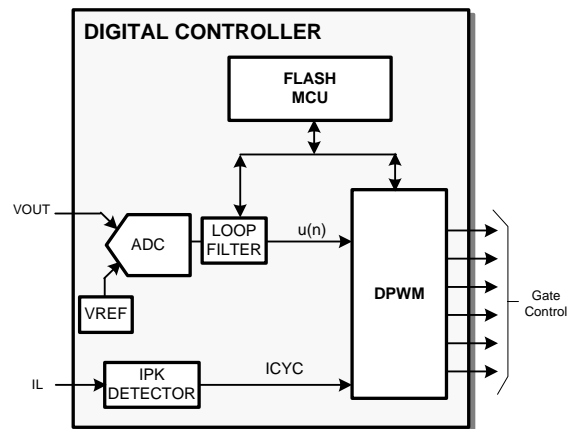


Fig. 1 Digital control IC block diagram

Figure 1 illustrates the top-level block diagram of the voltage-mode, monolithic digital controller. It consists of a high-speed, 8-bit MCU and two programmable signal processors: a proportional integral derivative-type programmable loop compensation filter (PID filter) and a DPWM. Once initialized by the MCU, the programmable signal processors perform real-time feedback control autonomously. Configuration and control registers within the signal processors are accessible to the MCU enabling real-time control optimization to be realized in firmware.

An expanded diagram of the front-end signal path is shown in Figure 2. The transient response requirements of modern supplies demand controllers with extremely fast response times. Since the analog-to-digital converter (ADC) is inside the feedback loop, conversion delay creates a phase shift that may degrade the loop response [2,9,12]. Consequently, a low-latency ADC is used to quantize ($V_{out} - V_{ref}$). The resulting digital error, D_e , is applied to the inputs of the PID filter and hardware transient monitor. The PID filter compensates (D_e) to form a calculated duty cycle ratio term $u(n)$.

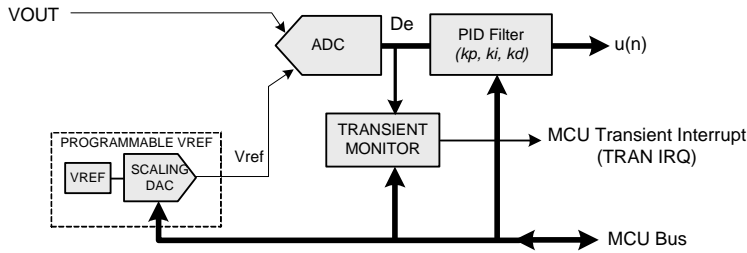


Fig. 2 Front end control signal path

While small transients are corrected by proportional and derivative loop response, the MCU may apply a nonlinear control response during excessively high di/dt load transients. Given the integrating action of the PID filter, De changes abruptly only when a load transient is present, which causes the transient monitor to interrupt the MCU. The MCU responds by adjusting loop gain and frequency control handles for faster loop response as needed to optimally resolve the load perturbation [4]. An example is described in the simulations presented in Section IV.

The DPWM is a multi-phase, programmable timing generator with a maximum PWM frequency of 1 MHz and minimum timing resolution of 5 nS. This DPWM is similar to other DPWM architectures that utilize high-speed counter-comparator circuits [2, 11]. The timing behavior of each output phase is specified in initialization firmware. Once initialized, the duty cycle of each modulation phase is determined by the magnitude of $u(n)$ as modified by the trim and limit logic shown in Figure 3.

Trim and limit logic scales and/or limits the value of $u(n)$ providing the MCU with a control handle to adjust control modulation gain and limits on a channel-by-channel basis. Under normal conditions, $u(n)$ modulates the output duty cycle; however, the output duty cycle may also be limited by the peak current detector or completely overridden by the MCU. The peak current detector shown in Figure 1 is an analog comparator with leading edge blanking logic. As in analog control systems, the peak current detector provides cycle-by-cycle current limiting by comparing the peak inductor (or transformer) current to an internally programmed threshold value. The ongoing portion of the PWM output duty cycle is immediately terminated when ICYC transitions to its active state.

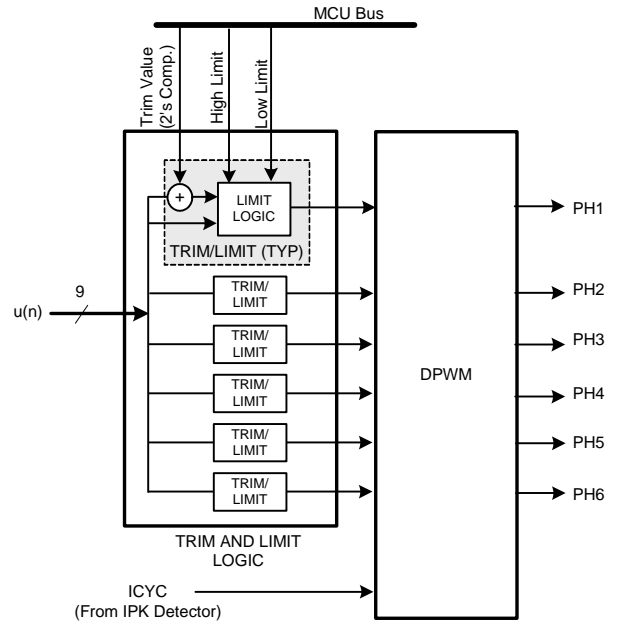


Fig. 3 DPWM trim and limit block diagram

The MCU shown in Figure 4 contains an 8051-compatible CPU core with supervisory circuits (VDD monitor, watchdog timer, missing clock pulse detector, FLASH error detector and look-ahead waveform pattern error).

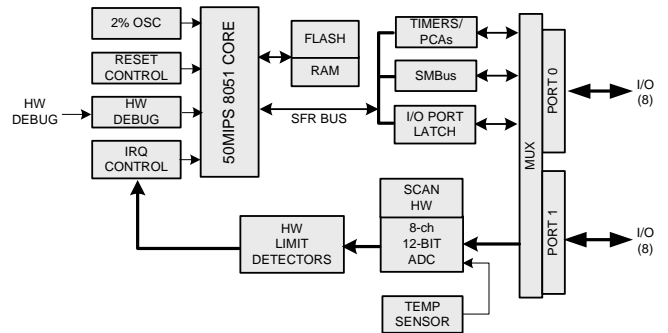


Fig. 4 MCU block diagram

The CPU has a maximum throughput of 50 million instructions per second (MIPS). The MCU peripherals consist of timers and serial ports. Of particular importance is a 12-bit, self-multiplexed ADC. Inputs are automatically multiplexed by hardware in a user-programmed order. Each converted result has an individual result register with a programmable hardware limit detector. The limit detectors generate vectored interrupts when the measured parameter is outside the user-programmed range. This hardware limit detection scheme minimizes response time, enabling system protection functions to reside within controller firmware and reducing the external component count while increasing flexibility.

III. Half Bridge Application Example

The half bridge converter in Figure 5 operates at a PWM frequency of 400 kHz and uses secondary-side control for optimum transient response [7]. The PH3 and PH4 outputs control the synchronous rectifiers via a dual driver IC. A small MCU on the primary side digitizes the input, capacitor node, and average primary current signals and transmits the results to the secondary-side controller via a single-chip digital isolator IC.

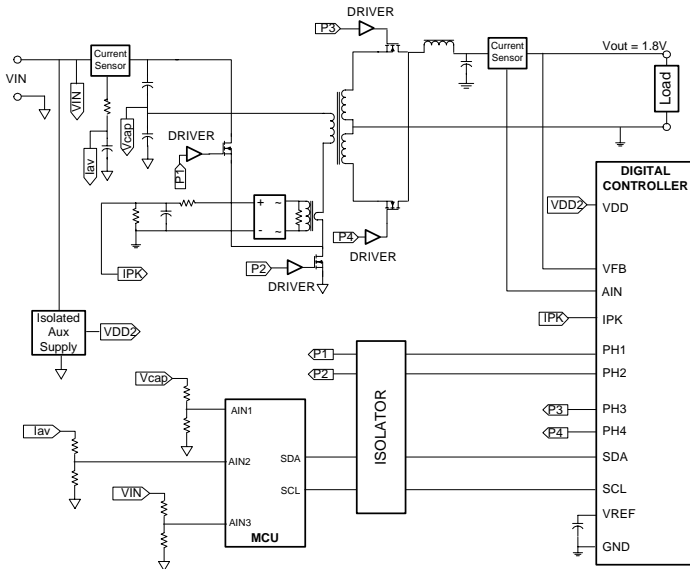


Fig. 5 Half-bridge application example

The isolator provides primary/secondary isolation for the primary side switch control signals and voltage measurements.

The peak current sensing circuit uses a current transformer specifically designed to meet isolation voltage requirements, and a full-wave rectifier and filter circuit. The output connects directly to the peak current detector input (IL) of the controller.

When power is applied, the controller executes an internal hardware reset followed by firmware initialization of all

register and RAM-based parameters. The controller remains in a low-power state monitoring digitized VIN data from the primary-side MCU. Controller firmware fully enables all peripherals and interrupts (including all system safeguards) and initiates soft-start when the value of VIN exceeds the UVLO threshold.

A general-purpose timer is used as a time base for soft-start. With each timer interrupt event, firmware increments the programmable VREF until the supply output voltage is within the specified range, at which time steady-state operation begins.

During steady-state operation (Figure 6), the MCU operates in interrupt mode where hardware events divert program execution to specific routines in priority order.

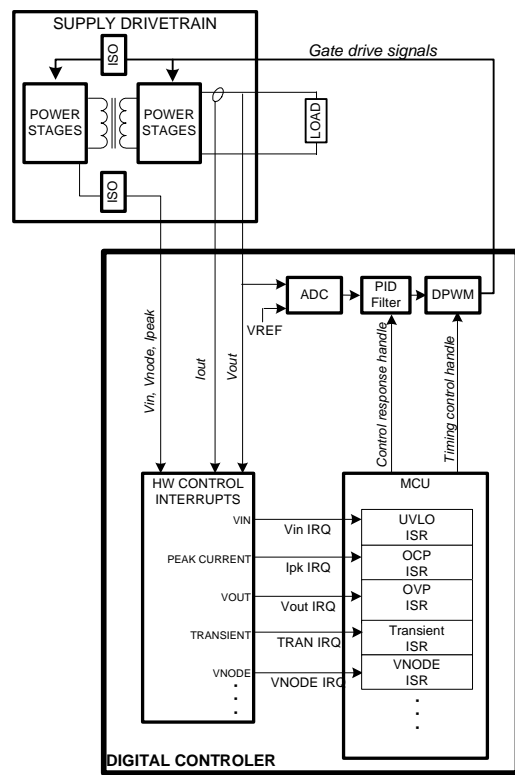


Fig. 6 Converter steady-state program flow

This scheme enables the MCU to respond to a prioritized hierarchy of system functions in minimum time. Specifically, hardware-generated interrupts divert firmware execution to ISRs that perform operations, such as nonlinear control response (as described in Section II).

During steady-state operation, the MCU manages relatively lower bandwidth tasks on an interrupt basis, and hardware performs the following operations in parallel:

- **Output voltage regulation:** The programmable signal processors update duty cycle every 100nS.
- **Current limiting:** The current detector provides cycle-by-cycle transformer current limiting.
- **Analog-to-digital conversion:** Input and output voltage, average current and local temperature are continuously scanned, digitized and stored by the self-scanned, 12-bit ADC.
- **Parametric limit monitoring:** Hardware limit detectors compare each converted parameter to prescribed limits and generate vectored interrupts when the parameter is out-of-range.
- **Background task scheduling:** a hardware timer (scheduler) generates periodic interrupts that vector the MCU to maintenance routines, such as statistical calculations, variable normalization, communication and other system management tasks.

System safeguards (e.g. OVP) are performed in much the same way as the transient response example previously described. When a measured parameter is out of range, an interrupt diverts firmware execution to a specific ISR. This is true for OVP, OCP, OTP and other system-related fault conditions.

MCU system management can also correct system anomalies. For example, the capacitive node voltage on a half-bridge converter will migrate from its nominal $V_{IN}/2$ value if the R_{DSon} of one of the primary-side switching transistors becomes abnormally high. Left unguarded, the capacitor node voltage will eventually migrate to either V_{IN+} or V_{IN-} , causing converter operation to cease. The MCU can compensate for the weak transistor by extending its duty cycle. This is accomplished by implementing a low-frequency feedback loop in firmware that applies a positive duty cycle offset to the weak transistor while using V_{NODE} (Figure 6) as the feedback variable. Loop feedback action will force the non-adjusted phase to reduce its duty cycle by an offsetting percentage to maintain output regulation.

Other system power management functions can be implemented in firmware. For example, voltage positioning involves setting the output voltage at the low end of its specified range during high-current operation to maintain V_{out} within tolerance in the event of a sudden negative di/dt . If optimal voltage positioning is used, the output capacitor can be made half the size required for stiff voltage regulator design, saving cost and circuit board area.[2]. Voltage positioning can be readily accomplished in firmware by reading I_{OUT} and adjusting V_{REF} to the optimum value. Other power management

functions include efficiency optimization (dead time control), load sharing and sequencing.

IV. Experimental Results

As shown in Figure 7, a hardware controller based on an FPGA was built as a proof-of-concept vehicle for the digital controller IC.

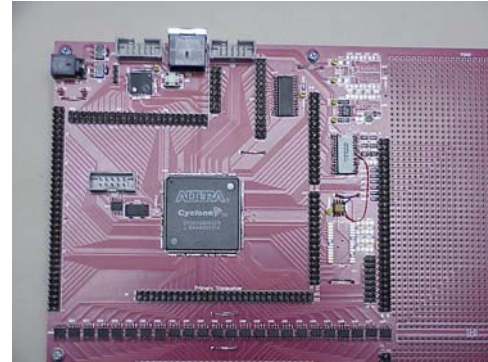


Fig. 7 Controller emulator

The programmable signal processors, DPWM and associated host interface logic were instantiated in the FPGA. The emulator has a commercially available, 50 MIPS MCU to emulate the MCU onboard the controller IC. Discrete circuitry (operational amplifiers, ADC and discrete passive components) provides the signal conditioning and data conversion functions. The emulator was connected to a separate board containing a half-bridge dc-dc converter circuit similar to the circuit shown in Fig. 6, and has an output voltage of 1 V and an input voltage range of 32 V to 72 V.

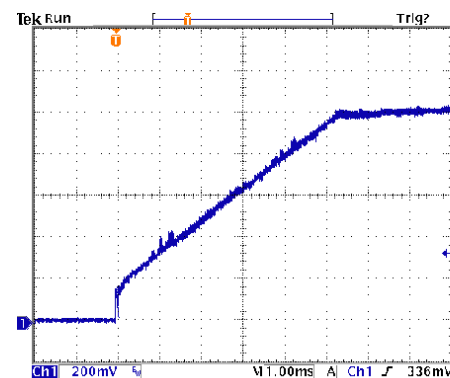


Fig. 8: Emulator start-up performance

An oscilloscope photo of power supply soft-start is shown in Figure 8. Note that the slope of the monotonic ramp can be varied over a wide range by changing the frequency of the soft-start timer. Line regulation was 0.01% (no load on the output) and load regulation was measured at 0.2% using a load range of 0 A to 30 A at an input voltage of 32 V.

At the time of this study, dynamic compensation was not implemented on the emulator. The simulations of Figure 9 and Figure 10 show the output response to a 30 A, 10 A/ μ S transient. Linear control response (i.e. transient interrupt disabled) was used in the transient of Figure 9. Note the maximum deviation is approximately 90 mV (9% relative to V_{out}). Fig.10 demonstrates a very simple example of nonlinear control by increasing the PID filter kd term when the output transient is initially detected. Notice that the max deviation is reduced to approximately 50 mV (5% relative to V_{out}). More sophisticated loop adjustments can be applied to achieve greater response improvements than shown in this example.

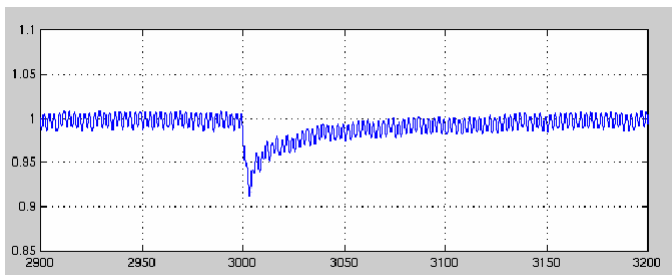


Fig. 9: Transient with linear control response

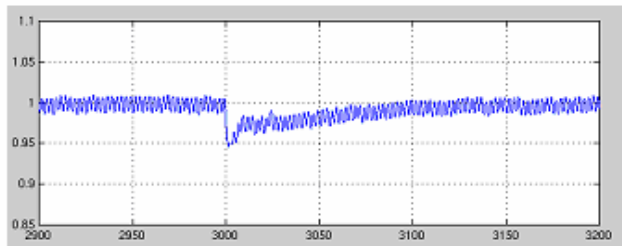


Fig. 10: Transient with nonlinear control response

V. Conclusion

A competitive digital controller that offers the performance and economy of a hardware-based solution with the flexibility of a processor-based solution has been presented, and hardware and simulation results have been given to verify its feasibility. Its fully digital architecture uses hardware signal processing for real-time control and a Flash-based MCU for system supervisory and control optimization functions. It promises enhanced system performance, added flexibility, reduced size and ultimately lower cost.

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