



S I L I C O N   L A B S

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# Business Introduction

2011

# Purpose

**Silicon Laboratories offers a wide variety of semiconductor products and peripheral items within many segments of the electronics, equipment, and automotive industries.**

**To better serve our broad customer base, this packet of information was developed to showcase the Silicon Labs methods for doing business.**

**This packet's intent is twofold: (1) to help answer questions customers may have regarding Silicon Labs' operations, and (2) to assure the Silicon Labs' way of doing business is aligned with customers' business expectations.**

**Please consult our external website ([www.silabs.com](http://www.silabs.com)) for any additional information you might require. Our Sales team can help you with any questions not answered there or within this packet.**

# Content

- **Corporate Overview**
- **Development Process**
- **Qualification Process**
- **Manufacturing Process**
- **Supplier and Technology Selection Strategy**
- **Quality Overview**
- **Customer Support**

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# Corporate Identity

## ➤ Corporate Overview

- Click [here](#) for Silicon Labs' Corporate Overview homepage

## ➤ Quality and Environmental Information

### *Highlights*

- ISO Certificates
- Sony Green Partner Certificate
- Quarterly Quality & Reliability Report
- Additional information [here](#)

## ➤ Investor Relations, Annual Report and Recent News

- Click [here](#) for Silicon Labs' Investor Overview homepage

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# Product Development & Release to Mfg.

**Product Development & Release to Manufacturing follows a rigorous process with Management Review & Approval at key milestones**

## ➤ **Product Development Process**

- Concept, Architecture, Design and PG (Tapeout) – reviews and checklists at each stage

## ➤ **Release to Manufacturing (RTM) Process**

- Pre-Production > Initial Production > Full Production
  - Formal reviews and checklists at each stage
  - Ship quantity limits increase with each phase
- RTM addresses the following (not inclusive)
  - Probe – HW and SW
  - Final Test – HW and SW
  - Qualification
  - Validation & Verification
  - Test Optimization, offshore transfer
  - Cpk and statistical baselines for maverick lot detection

# Design for Cost, Test and Manufacturing

- **Every design is reviewed to assure robust manufacturability, testability, and cost optimization**
  
- **Any risks identified are removed or minimized by methods such as:**
  - Design changes
  - Extra qualification
  - Improved manufacturing capability or controls
  - Increased monitoring
  
- **Reviews are held at the following milestones at a minimum**
  - Project approval
  - Architecture
  - Pre-PG
  - Initial Production

# Test Strategy

## ➤ Design for Test Strategy

- Scan used for synthesized logic
- Functional test modes employed to isolate functional blocks
- Built in Self Test (BIST) features also utilized

## ➤ Fault Coverage

- Minimum fault coverage required for production test release

## ➤ At Speed Testing

- Analog, Functional, and Memory tests are tested at datasheet speeds

## ➤ Test Insertions

- Each product is tested at its worst-case temperature at a minimum
- Promotion to single temperature test from multi-temperature test follows a rigorous process

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# Product Qualification

- **All products are qualified to JEDEC JESD47**
- **Three lots of material are used for qualification**
- **Qualification by Similarity:** Silicon Labs limits use of family data; one lot is always required for each device in the family
  - **Silicon Tests**
    - HTOL – High Temp Operating Life (1000h @ 125°C min)
    - ELFR – Early Life Failure Rate (48h @ 125°C min)
    - HTSL – High Temp Storage Life (1000h @ 150°C)
    - NVCE, HTDR – Non-Volatile Memory Tests
    - LU – Latchup (200ma @ max operating temp)
    - ESD – HBM target = 2000V, MM target = 200V, CDM target = 500V
  - **Package Tests**
    - HAST – Highly Accelerated Stress Test (replaces THB and Autoclave)
    - MSL to J-STD-020 (target = Level 3/260)
    - TC – Temperature Cycling (500~ of Condition C)

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# Statistical Bin Limits (SBL)

- **SBLs are used at these process steps**
  - Foundry Wafer Acceptance Test (WAT)
  - Wafer Probe
  - Final Electrical Test
- **Limits are established to identify abnormal (maverick) material lots**
- **Limits are based on overall yields or on specific tests or test groups**
- **The MRP system automatically places on hold lots that fail to meet limits**
- **There are two levels of hold/notification**
  - Level 1 – Engineering: held for product engineer investigation and validation before release
  - Level 2 – MRB: held for product engineer and quality manager investigation and validation before release

# Traceability

- **All parts are marked with a trace code that can be decoded by Silicon Labs to identify:**
  - Wafer lot
  - Wafer or group of wafers for high volume parts
  - Assembly lot
  - Test revisions used in manufacturing
- **Traceability is maintained at each supplier for specific process details**

# Quality Monitoring

Silicon Labs follows [JEDEC](#) as the preferred industry standard

## Quality Monitors

- **Electrical:** production samples are retested to datasheet limits. This sample method identifies defects introduced at the test process step or that have escaped the test process.
- **Visual/Mechanical:** production is sampled prior to final pack. Inspections coverage includes mark, count, label, cover tape workmanship, moisture barrier bag visual, lead location, part placement, and other workmanship items.
- **Reporting:** failures drive corrective actions and process/product improvements.

# Reliability Monitoring

Silicon Labs follows [JEDEC](#) as the preferred industry standard

- **Failure Rate Estimation:** A long-term, steady-state failure rate calculation allows circuit and system engineers to allocate failure rates at the component level during system design.
- **Failure in Time (FIT):** FIT represents the number of failures in a billion hours of operation. Silicon Labs reports FIT rates in its quarterly [Q&R Report](#) as curves and in tables for specific temperatures and assumptions.
- **Mean Time To Failure (MTTF):** inverse of FIT rate ( $1/\text{FIT}$ )
- **Failure Rate Calculation Method:** Long-term failure rates are estimated by applying the Arrhenius equation to data collected from long term operating life tests. Confidence factors of 90% and 60% are reported.

# Process Control Points

## Critical to Quality (CTQ) Parameters

CTQ parameters are controlled by Silicon Labs' assembly partners. Their performance is reported quarterly in CpK reports and reviewed by the Silicon Labs Supplier Managers.

Process	CTQ Parameter
Wire Bond	Wire pull strength (g)
	Ball shear strength (g)
Lead plating	Thickness ( $\mu$ "
Saw / Singulation	Package Dimension (mm)

# Change Management

- **Silicon Labs follows the principles of JEDEC JESD46 for change management and notification**
  
- **Change Action Boards review and assure compliance for both supplier and internally initiated changes**
  - Wafer Fab Changes
  - Assembly Changes
  - Materials Changes
  - Qualification of changes to JEDEC requirements if applicable
  
- **Customer Notification**
  - PCN – 90 day notification provided to customer
  - EOL – 180 for last orders, 360 days for final delivery to customer
  - Exceptions require cross-functional review and approval

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# Supplier and Technology Selection

- **Process technology, package choice and test platforms are carefully chosen based on:**
  - Technology availability and maturity at suppliers
  - Technology roadmap of suppliers
  - Past and present execution (quality, cycle time, deliveries, operational efficiencies) from suppliers
  - Material cost from the supplier and
  - Cost of doing business with that supplier
- **Technology choices are made during development phase**
- **Silicon Labs provides a second source when appropriate to ensure continuity of supply**

# Supplier Management

## ➤ **Asia-based Assembly and Test Supplier Management**

- Provides Supplier initial Evaluation, Selection, and on-going Assessment
- Performs Semiannual Strategic Business Reviews (SBRs) with key suppliers to review overall business, market trends, performance, cost reduction, capacity plans, product roadmaps and specific projects

## ➤ **Austin-based Foundry Engineering manages the above for the wafer fab suppliers**

## ➤ **Key Suppliers are audited at least annually**

- Quality management systems (ISO9001 and TS 16949)
- Environmental, Health & Safety (including ISO14001)
- Social Accountability (EICC [Code of Conduct](#))
- Business parameters (delivery, cost, service, capacity)
- Technology
- Self assessment from a supplier is occasionally deemed adequate

# Supplier Management Turtle Diagram

## Monitoring tools

1. Scorecard – semi-annually
2. Weekly report
3. 8D report for significant issues
4. Corrective Action Report (CAR)
5. Cpk report – monthly or quarterly
6. SAP and Tester snapshot @ Test sites – real time
7. Inventory cycle count & aged inventory audit – quarterly

## Input

1. Approved Supplier List
2. SBR Feedback
3. Audit/assessment feedback
4. Experience with supplier
5. Scorecard feedback
6. Specific requirements:
  - a. Technical capability
  - b. Capacity constraint
  - c. Pricing
  - d. Sourcing strategy
  - e. Quality system

## Review methodology

1. Strategic Business Review -minimum 2/yr
2. Weekly conference call
3. Annual Process/Quality/EHS audit
4. Manufacturing readiness audit for any new package introduction or new test site

## Silicon Labs Supplier Management

## Output

1. Supplier status (primary /2<sup>nd</sup> source) logged in supplier database.
2. Supplier award

# Packing & Labeling

- Packing media available: tape & reel, tray and tube
- All finished goods are packed in a vacuum sealed Moisture Barrier Bag (MBB), including a Humidity Indicator Card (HIC) and desiccant
- Labels are automatically printed from the MRP System (SAP)
- Handling Units (HUs) may not contain more than two Batches

<b>Reel / MBB Inner Box / HU Label</b>	<b>Outer Box Shipping Label</b>
Customer or Silabs P/N	Supplier Address
Handling Unit #	Customer Address
Date Code / Trace Code	Customer or Silabs P/N
Seal Date	Handling Unit #
Assembly Country	Assembly Country
Quantity	Quantity
MSL, Reflow Temperature, Bake Time	“Pb-Free” symbol (if applicable)
“Pb-Free” (if applicable) & Plating Type (e#)	

# Quality & Environmental Systems

- Registered to **ISO 9001:2008** since Jun'00 ([link](#))
- Registered to **ISO/TS 16949:2009** since Jan'08 ([link](#))
- Registered to **ISO14001:2004** since Dec'06 ([link](#))
- **Certified Sony Green Partner** since Aug'08 ([link](#))

## *Quality Policy*

Silicon Labs is committed to Total Customer Satisfaction. We accomplish this by:

- ◆ Providing excellent products, support and service
- ◆ Exceeding customer needs and requirements
- ◆ Meeting the requirements and continually improving our world-class quality management system and its processes

## *Environmental Policy*

At Silicon Labs, we manage environmental matters as an integral part of our business by our commitment to:

- ◆ Continually improving our environmental performance and pollution prevention,
- ◆ Complying with applicable legal and other requirements that relate to our environmental aspects, and
- ◆ Minimizing the environmental impact of our business activities.

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# Customer Support – Analysis & Response

## ➤ **Corrective Action & Continual Improvement**

- Based on the Eight Discipline (8D) methodology

## ➤ **World Class In-House FA lab**

- Decap, SEM, FIB capabilities
- Cooperative with supplier FA capabilities as needed

## ➤ **Standard FA and 8D response times**

- Initial Failure Analysis: 2 workdays from suspect product receipt
- 8D Containment: 2 workdays from customer notification *or* proof of failure (after Initial FA)
- Final Failure analysis: 12 workdays after Initial Failure analysis
- 8D Root Cause and Corrective Action Plan: 10 workdays from customer notification *or* root cause discovery (after Final FA)

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# Customer Support – Substance Data

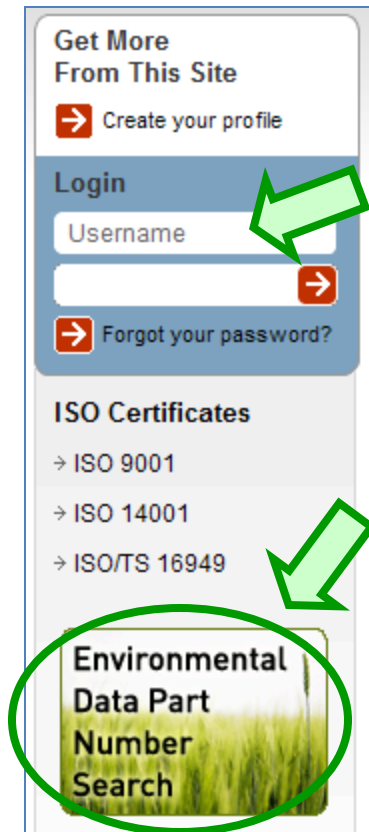
## Self-Serve Part Substances Data

Location: [www.silabs.com](http://www.silabs.com) > [Quality & Environmental](#)

(requires login)

After website registration, you can access:

1. RoHS, Halogen-free, PFOS/PFOA and REACH quick results and Certificates of Compliance
2. Downloadable Material Declaration Data sheets (Acrobat pdf sheet or IPC 1752 XML format)
3. Downloadable Homogeneous Materials test results



# Customer Support – FAQs

Several categories of frequently asked questions and answers can be found at [www.silabs.com](http://www.silabs.com) > [Quality & Environmental](#) including:

- **Corporate** (e.g. Governance, Locations, Financials)
- **Product** (e.g. Qualification, Traceability, Reporting)
- **Environmental** (e.g. Substance Database, Awards)
- **Quality** (e.g. Failure Analysis, 8Ds, ISO Registrations)
- **Operations** (e.g. Logistics, Supplier Mgmt, Ordering)