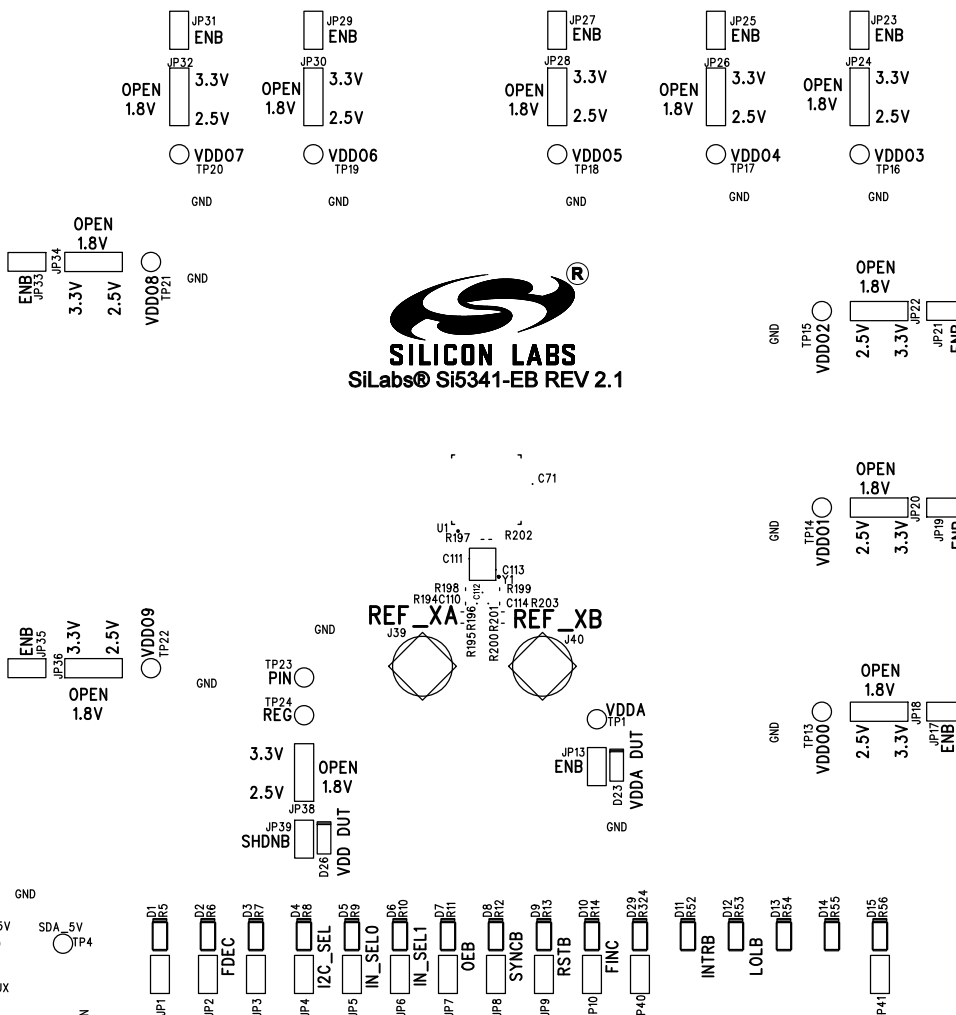


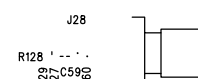


OUT3B J14
R98
RC31C

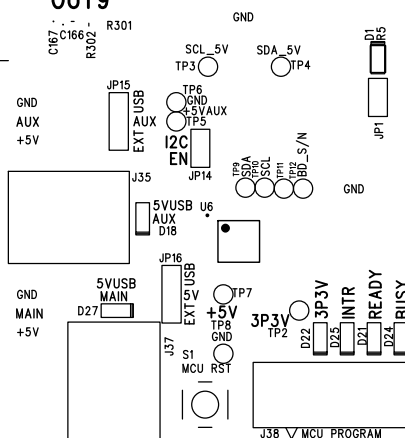
J22
OUT7B
C48 C47 R114 R115



SILICON LABS
SiLabs® Si5341-EB REV 2.1



GND



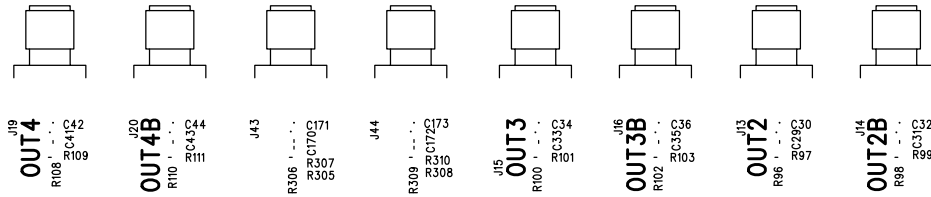
IN1B



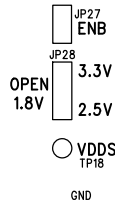
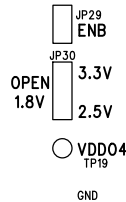
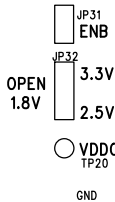
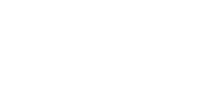
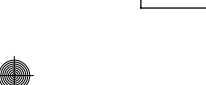
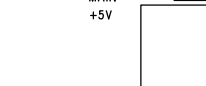
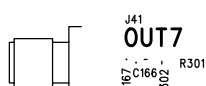
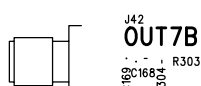
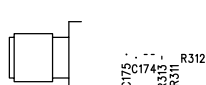
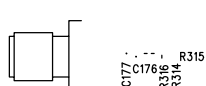
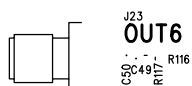
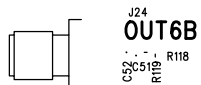
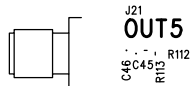
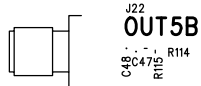
GND



PRIMARY SILKSCREEN



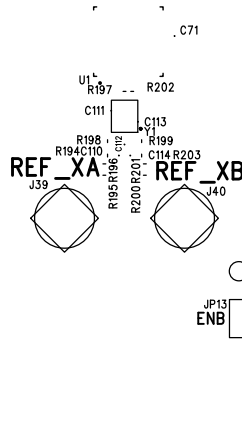
GND



IN2B

IN2

GND



IN3

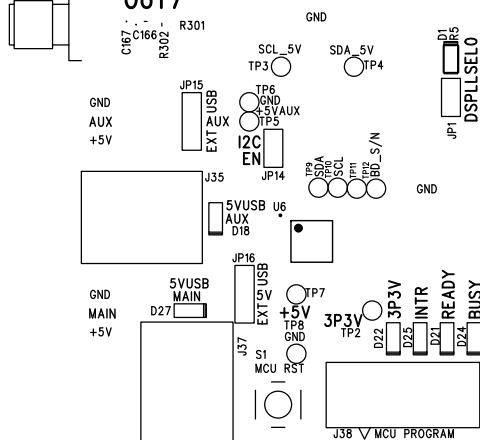
IN3B

IN0

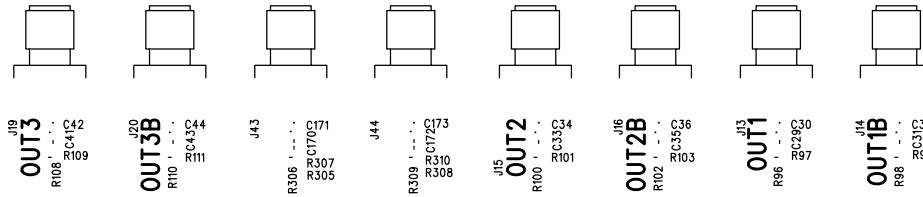
IN0B

IN1

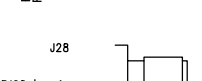
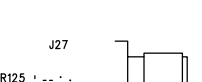
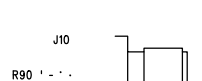
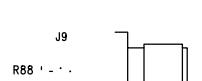
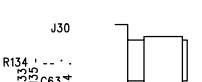
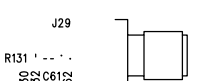
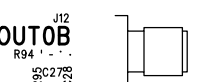
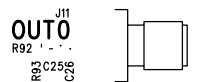
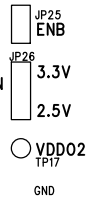
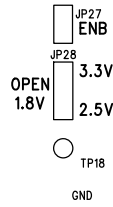
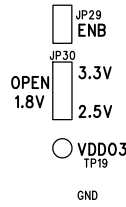
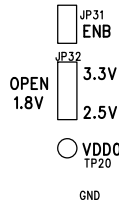
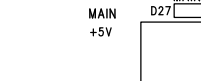
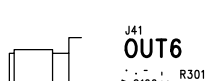
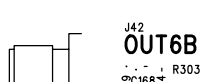
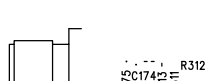
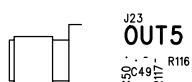
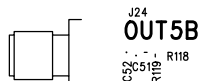
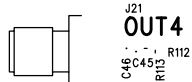
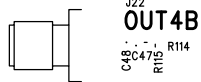
IN1B



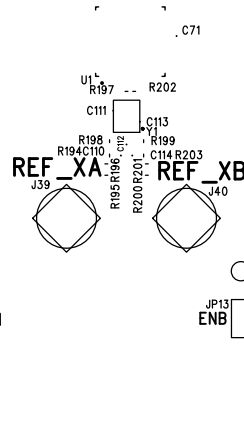
PRIMARY SILKSCREEN



GND



SILICON LABS
SiLabs® Si5348-EB REV 1.1



REF

REFB

INO

INOB

IN1

IN1B

IN3

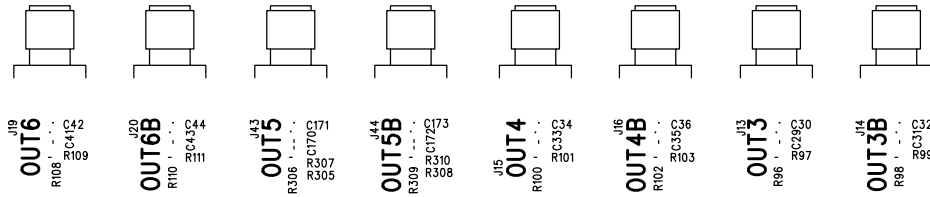
IN4

IN2B

IN2

GND

PRIMARY SILKSCREEN



GND



OUT7B
J22
C48
C47
R114



OUT7
J21
C46
C45
R112



OUT8B
J24
C50
C49
R118



OUT8
J23
C50
C49
R116



OUT9B
J25
C177
C176
R316
R314
R315



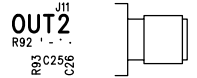
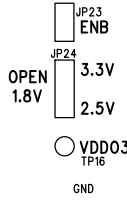
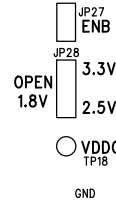
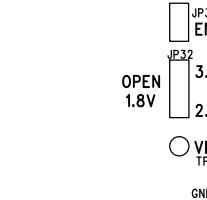
OUT9
J26
C175
C174
R312



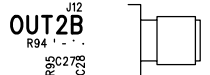
OUT9AB
J42
C160
C168
R304
R303



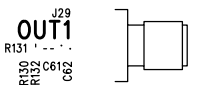
OUT9A
J41
C167
C166
R302
R301



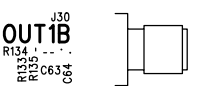
OUT2
J11
R92
C25
C26



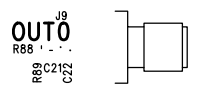
OUT2B
J12
R94
C27
C28



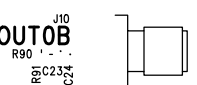
OUT1
J29
R131
C61
C62



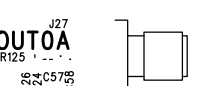
OUT1B
J30
R134
C63
C64



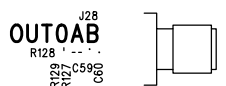
OUT0
J9
R88
C21
C22



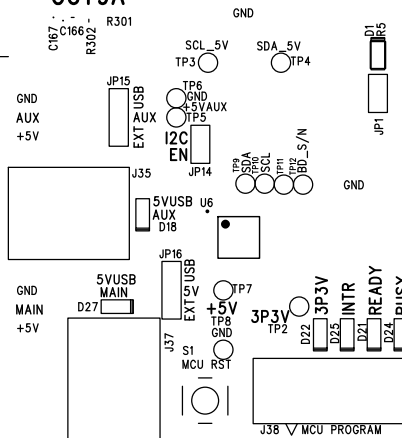
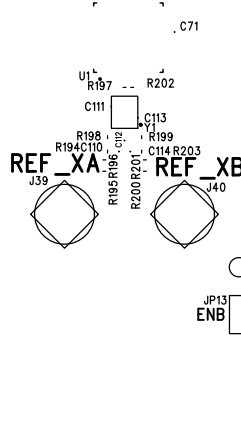
OUT0B
J10
R90
C23
C24



OUT0A
J27
R125
C57
C58



OUT0AB
J28
R128
C59
C60



IN3

IN3B

IN0

IN0B

IN1

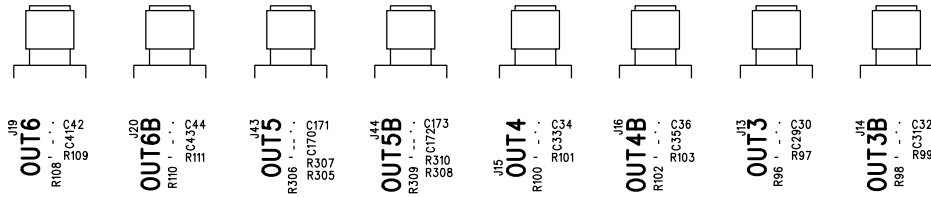
IN1B

IN2B

IN2

GND

PRIMARY SILKSCREEN



GND



J22
OUT7B
C48
C47
R114



J21
OUT7
C46
C45
R112



J24
OUT8B
C50
C49
R118



J23
OUT8
C50
C49
R116



OUT9B
C177
C176
R316
R314
R315
C46



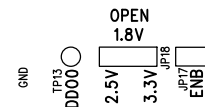
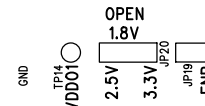
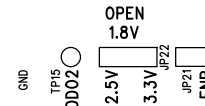
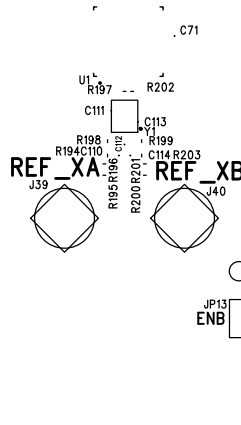
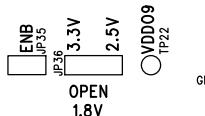
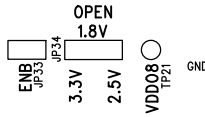
OUT9
C175
C174
R312
R310
R313
C45



J42
OUT9AB
C160
C168
R304
R303



J41
OUT9A
C167
C166
R302
R301



J11
OUT2
R92
C25
C26

J12
OUT2B
R94
C27
C28
C29

J29
OUT1
R131
R130
R129
C61
C62

J30
OUT1B
R134
R133
R132
C63
C64

J9
OUT0
R88
R89
C21
C22

J10
OUT0B
R90
R91
C23
C24

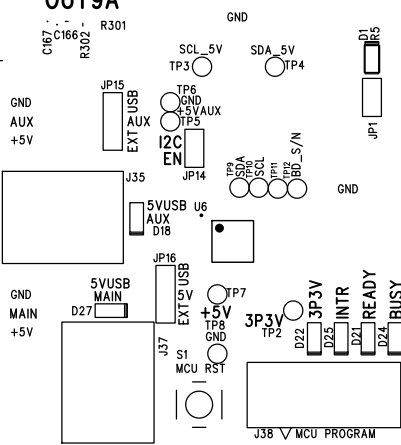
J27
OUT0A
R125
R126
R124
C57
C58

J28
OUT0AB
R128
R129
R127
C59
C60

IN2B

IN2

GND



IN3

IN3B

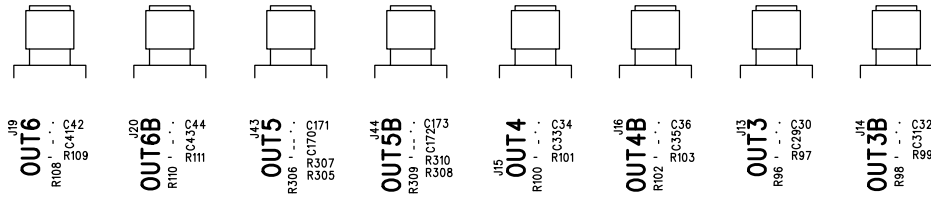
IN0

IN0B

IN1

IN1B

PRIMARY SILKSCREEN



GND



J22
OUT7B
C48 C47 R114
R115



J21
OUT7
C46 C45 R112
R113



J24
OUT8B
C50 C49 R118
R119



J23
OUT8
C50 C49 R116
R117



OUT9B
C177 C176 R315
R316 R314



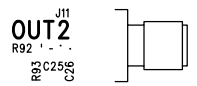
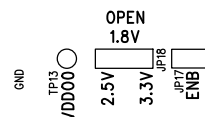
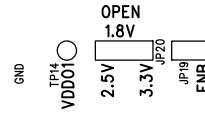
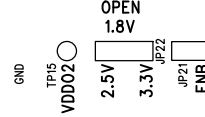
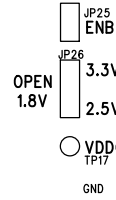
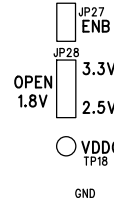
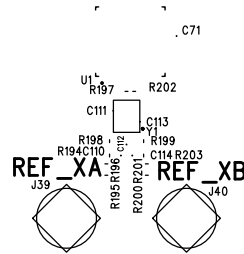
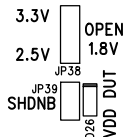
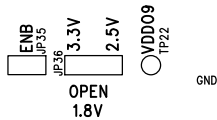
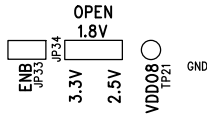
OUT9
C175 C174 R312
R313 R311



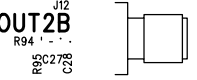
J42
OUT9AB
C160 C168 R303
R304



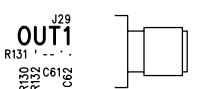
J41
OUT9A
C167 C166 R301
R302



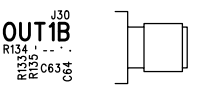
J11
OUT2
R92 C25 C26
R93



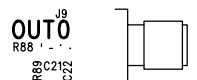
J12
OUT2B
R94 C27 C28
R95 C29 C30



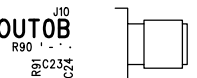
J29
OUT1
R131 C61 C62
R132 C63 C64



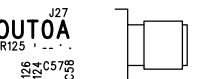
J30
OUT1B
R133 C65 C66
R134 C67 C68



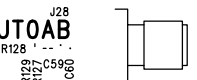
J9
OUT0
R88 C21 C22
R89



J10
OUT0B
R90 C23 C24
R91



J27
OUT0A
R125 C57 C58
R126 C59 C60

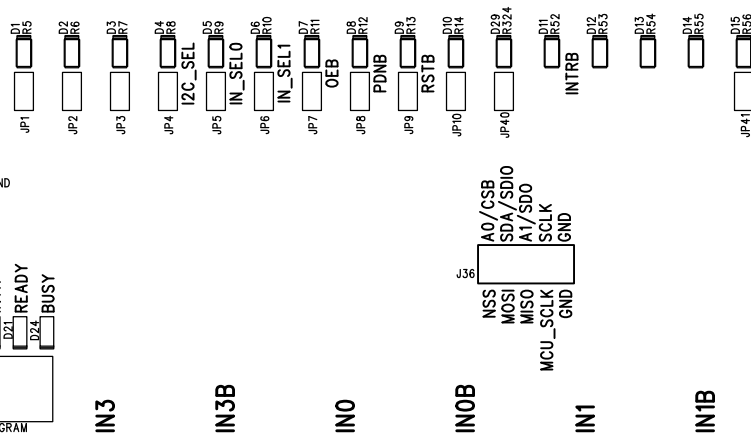
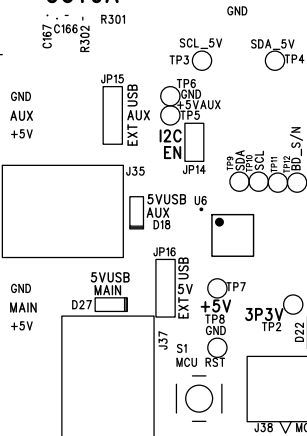


J28
OUT0AB
R128 C59 C60
R129 C61 C62

IN2B

IN2

GND



IN3

IN3B

IN0

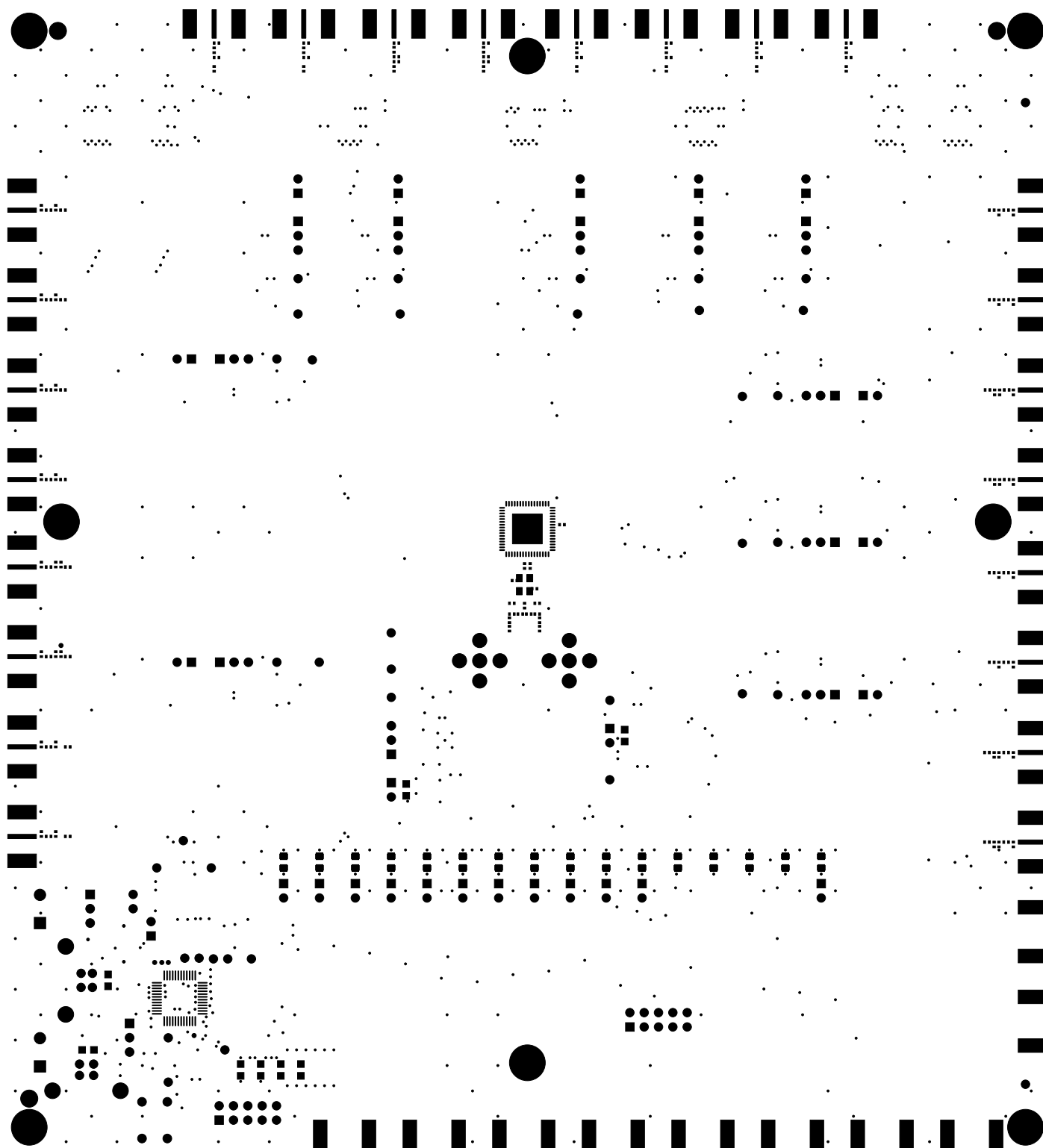
IN0B

IN1

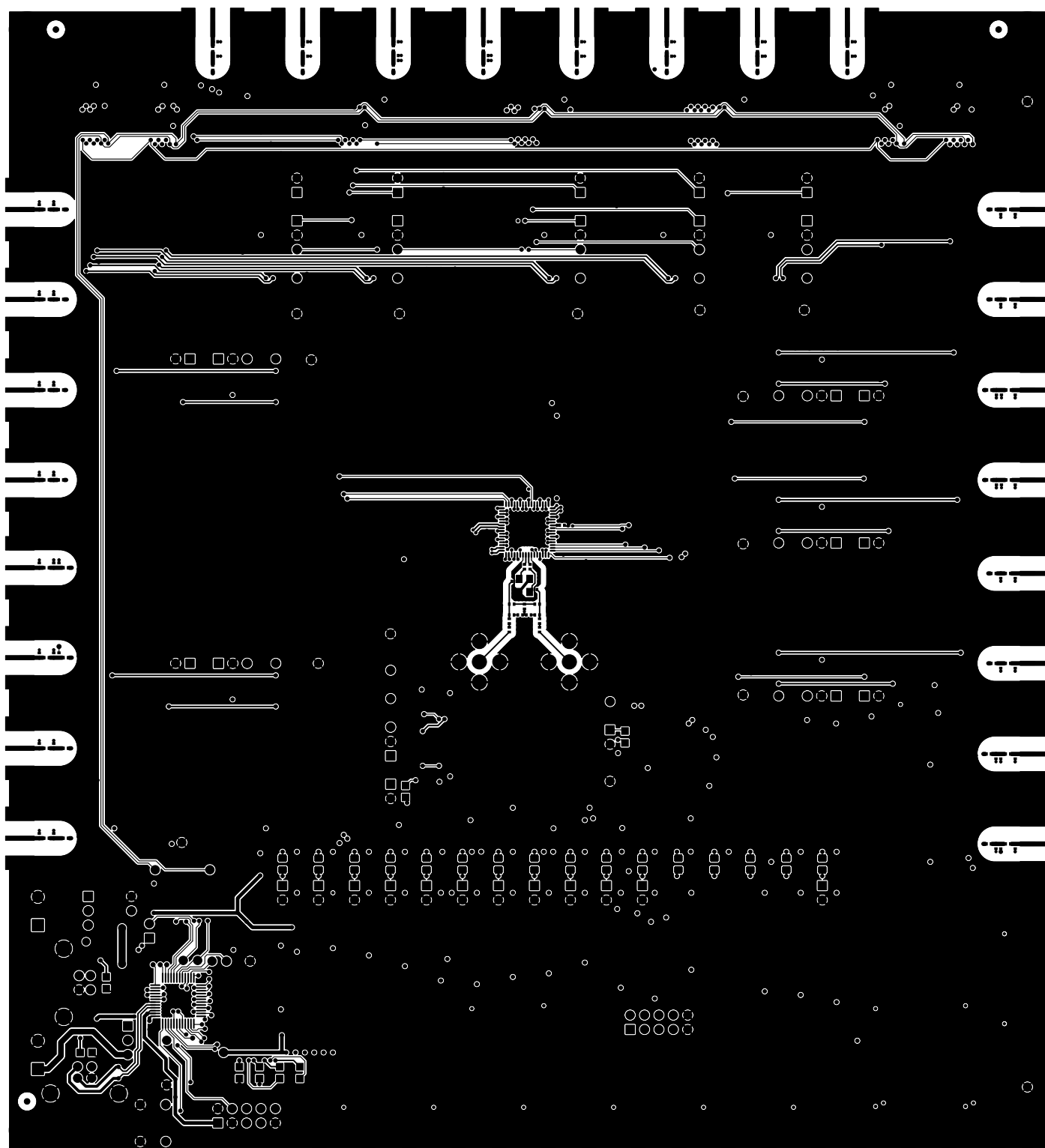
IN1B



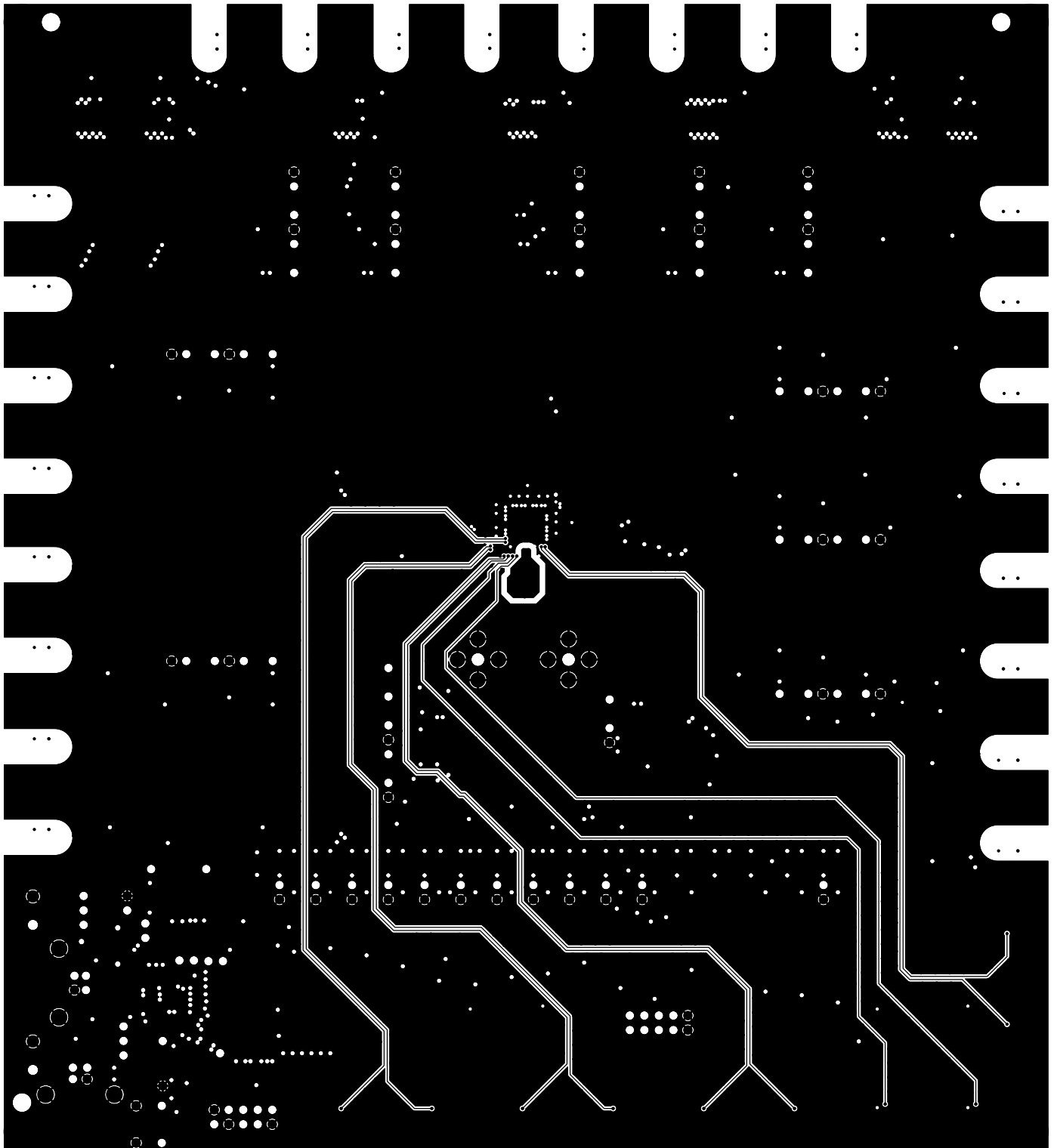
PRIMARY SOLDER MASK



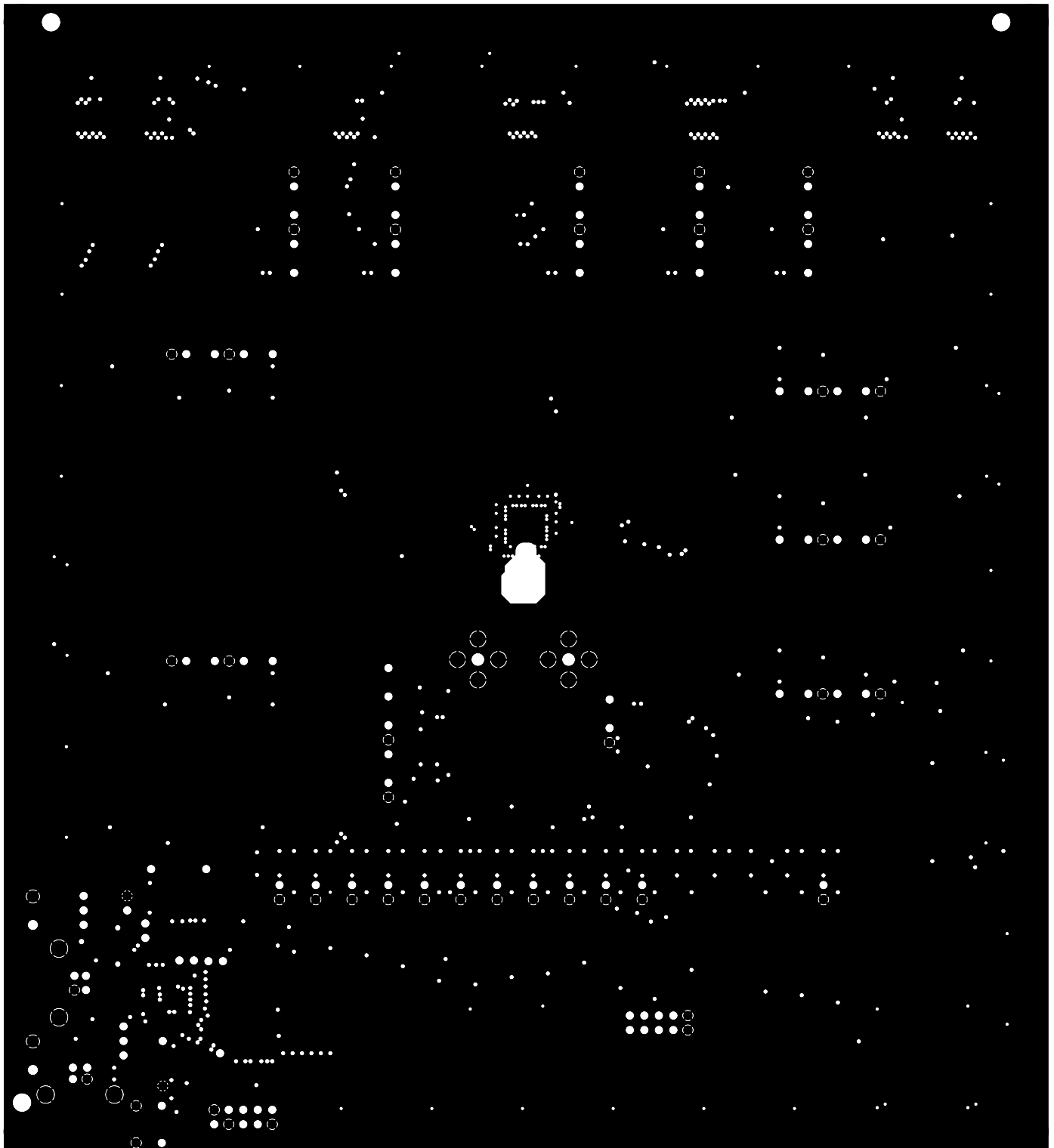
PRIMARY SIDE



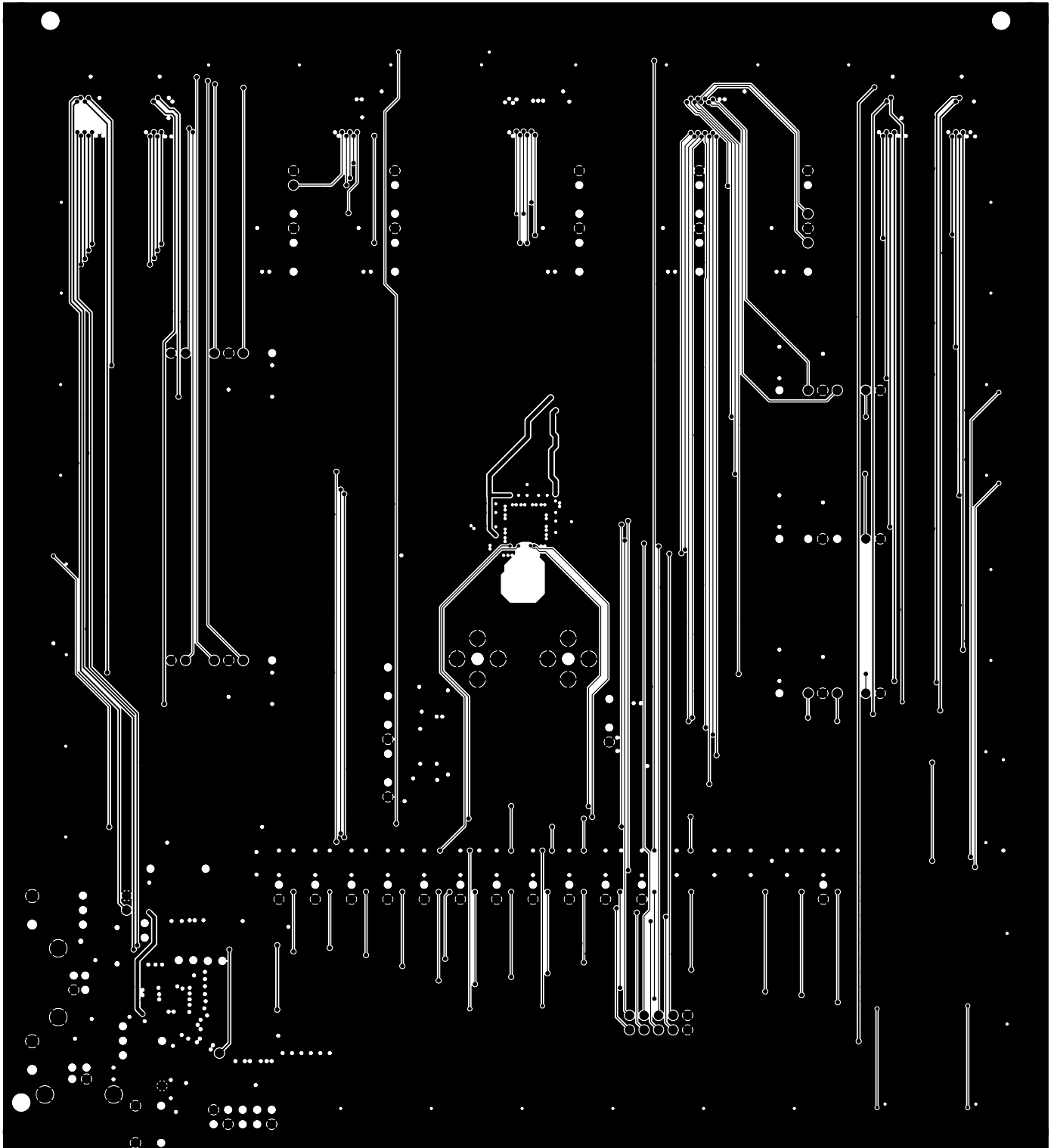
LAYER 02



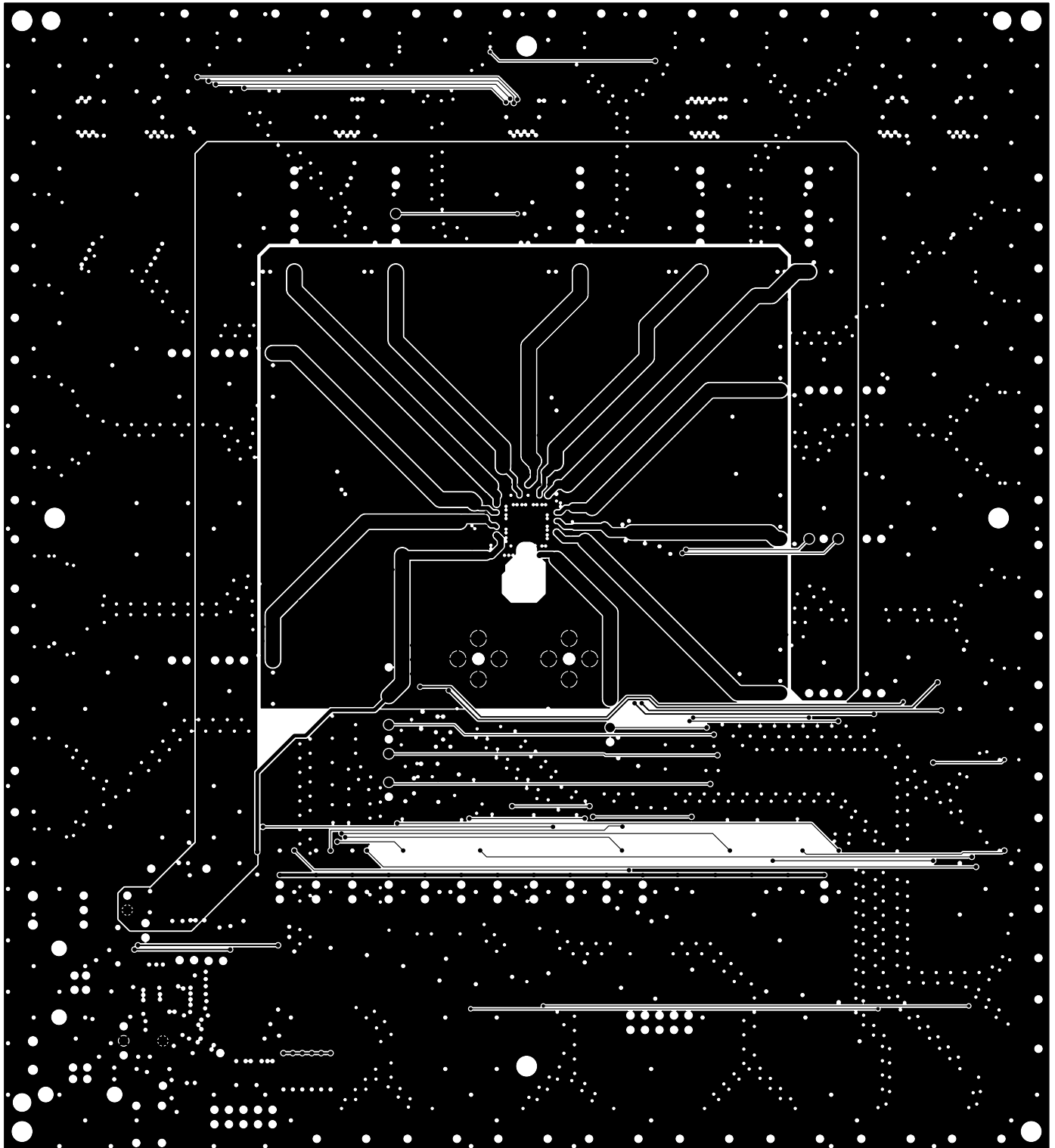
LAYER 03



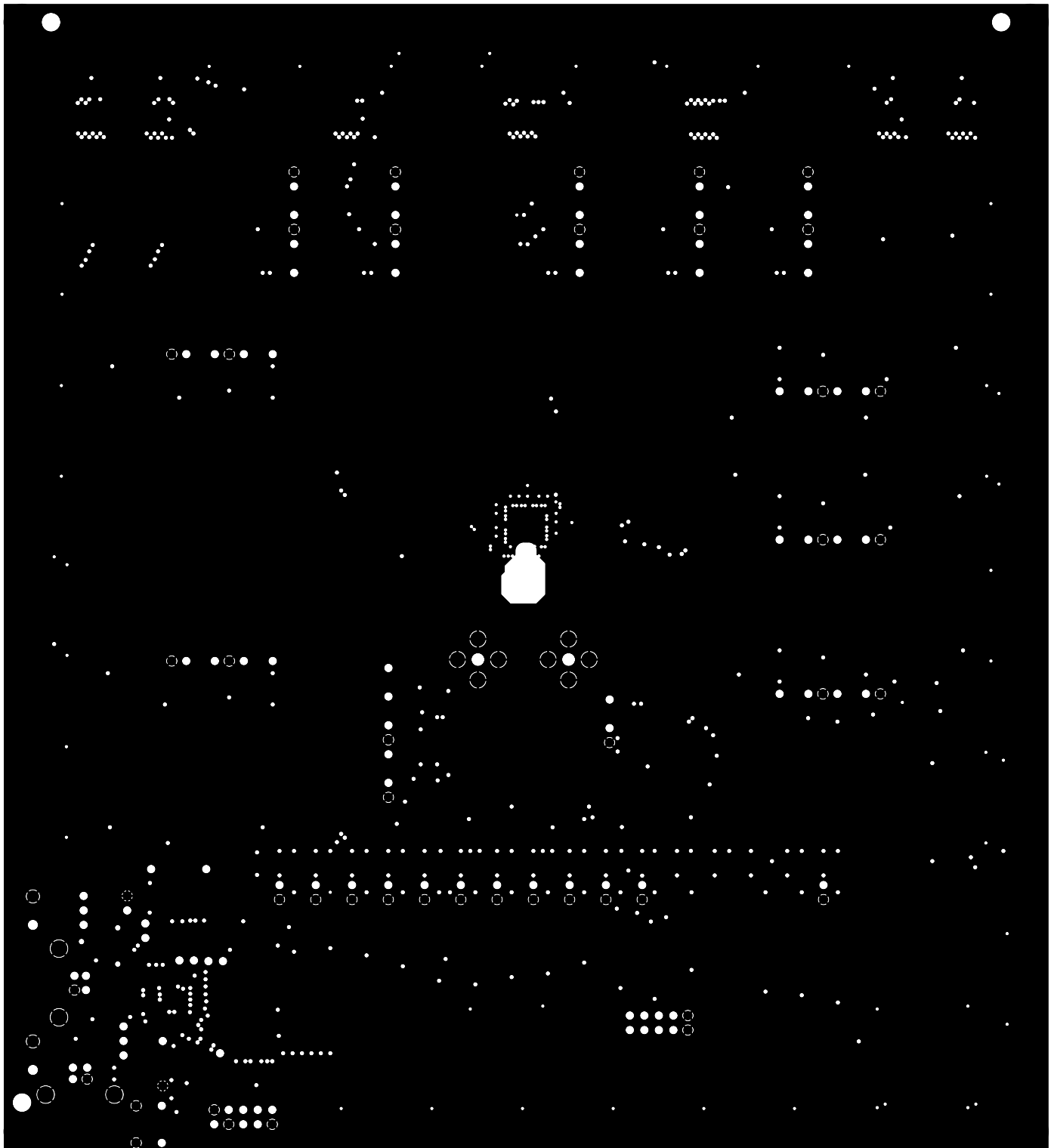
LAYER 04



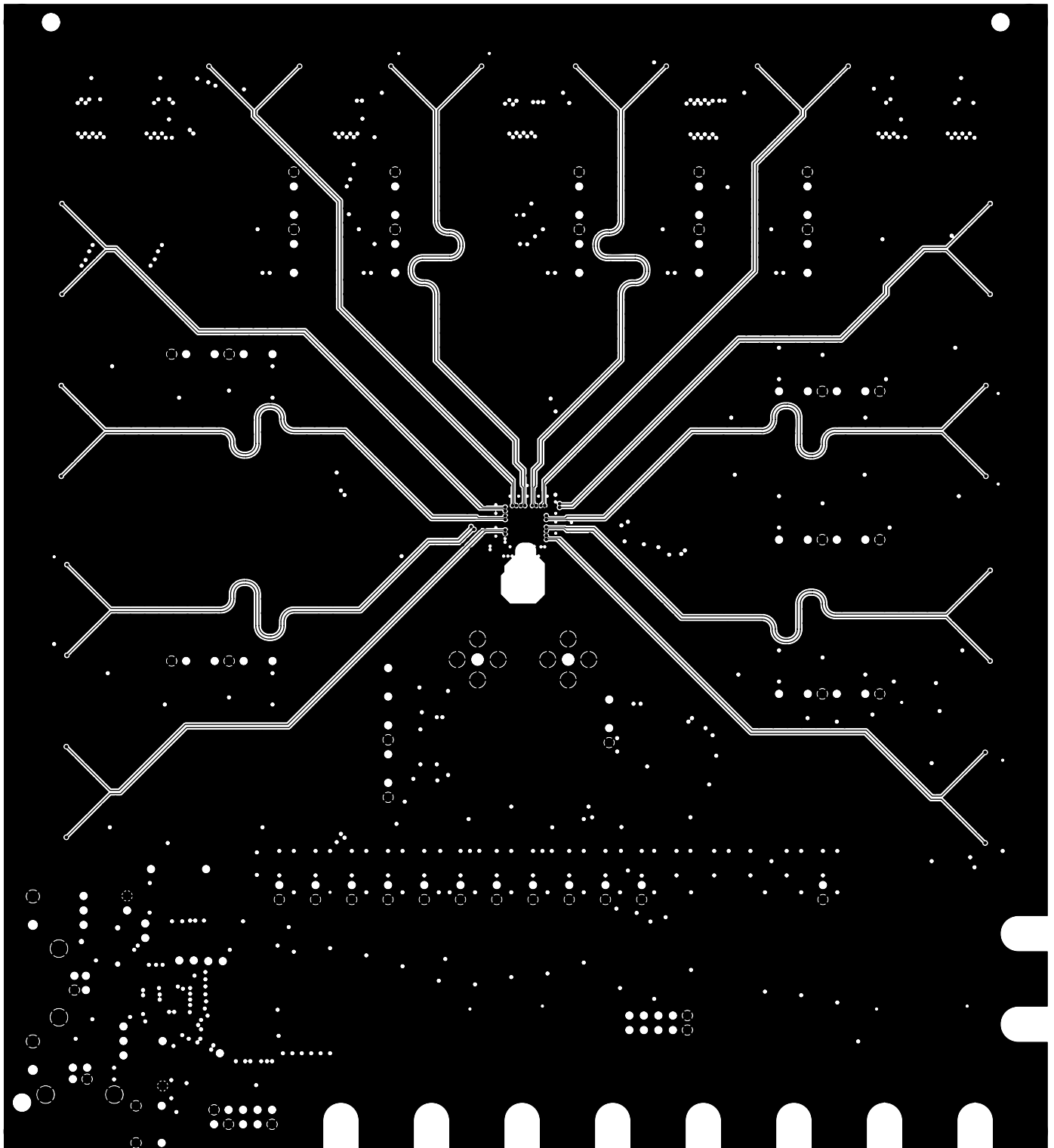
LAYER 05



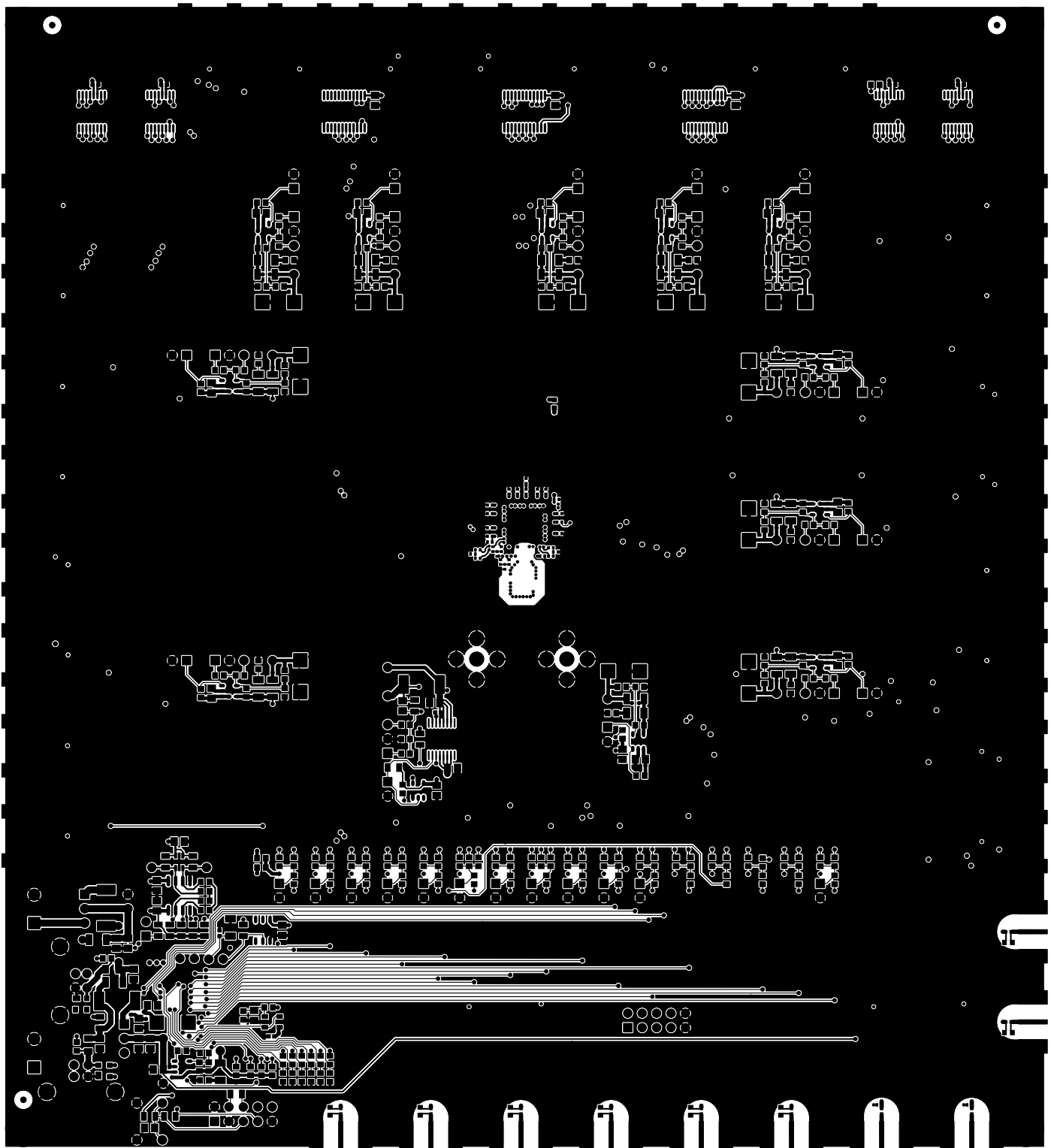
LAYER 06



LAYER 07

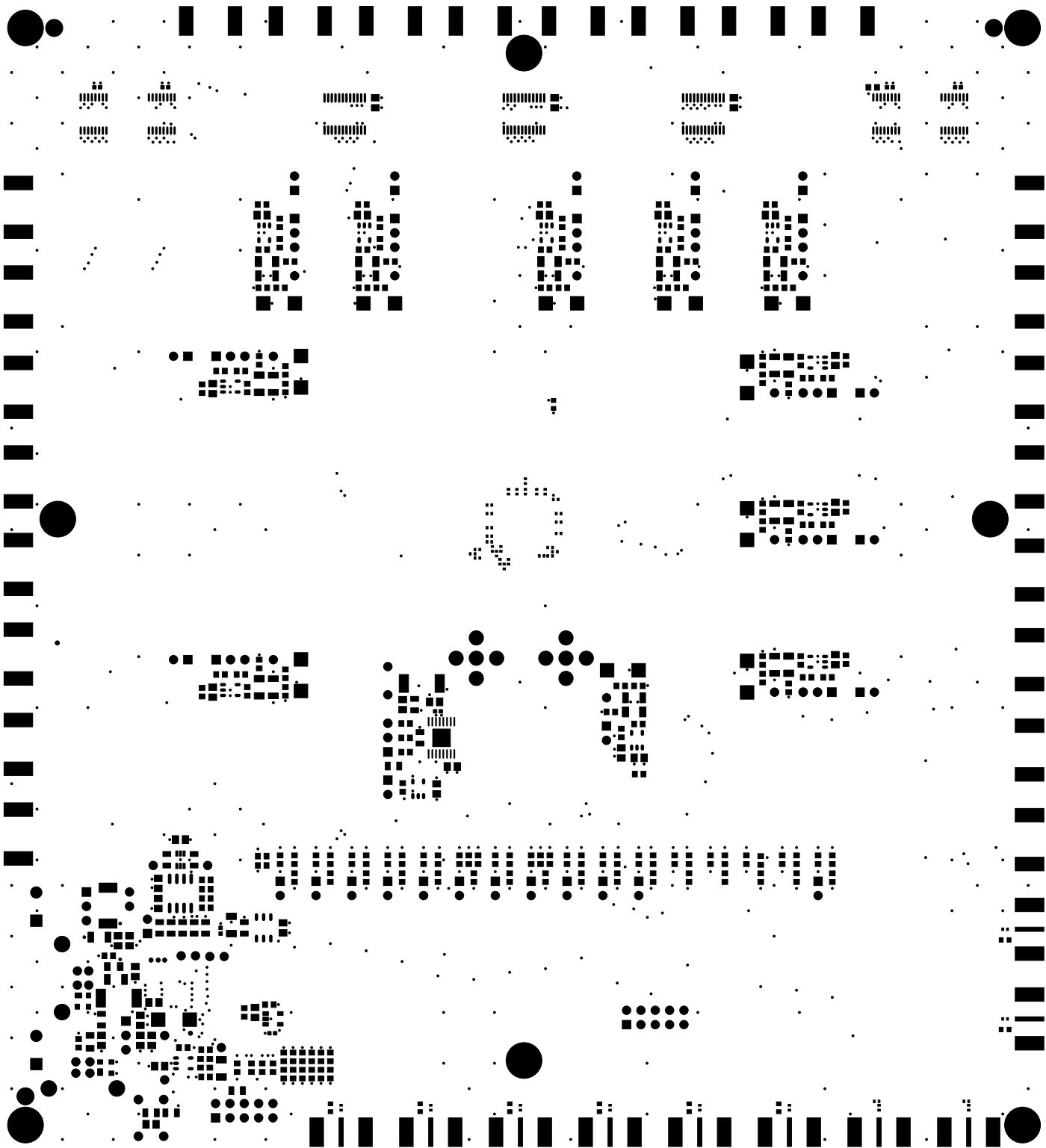


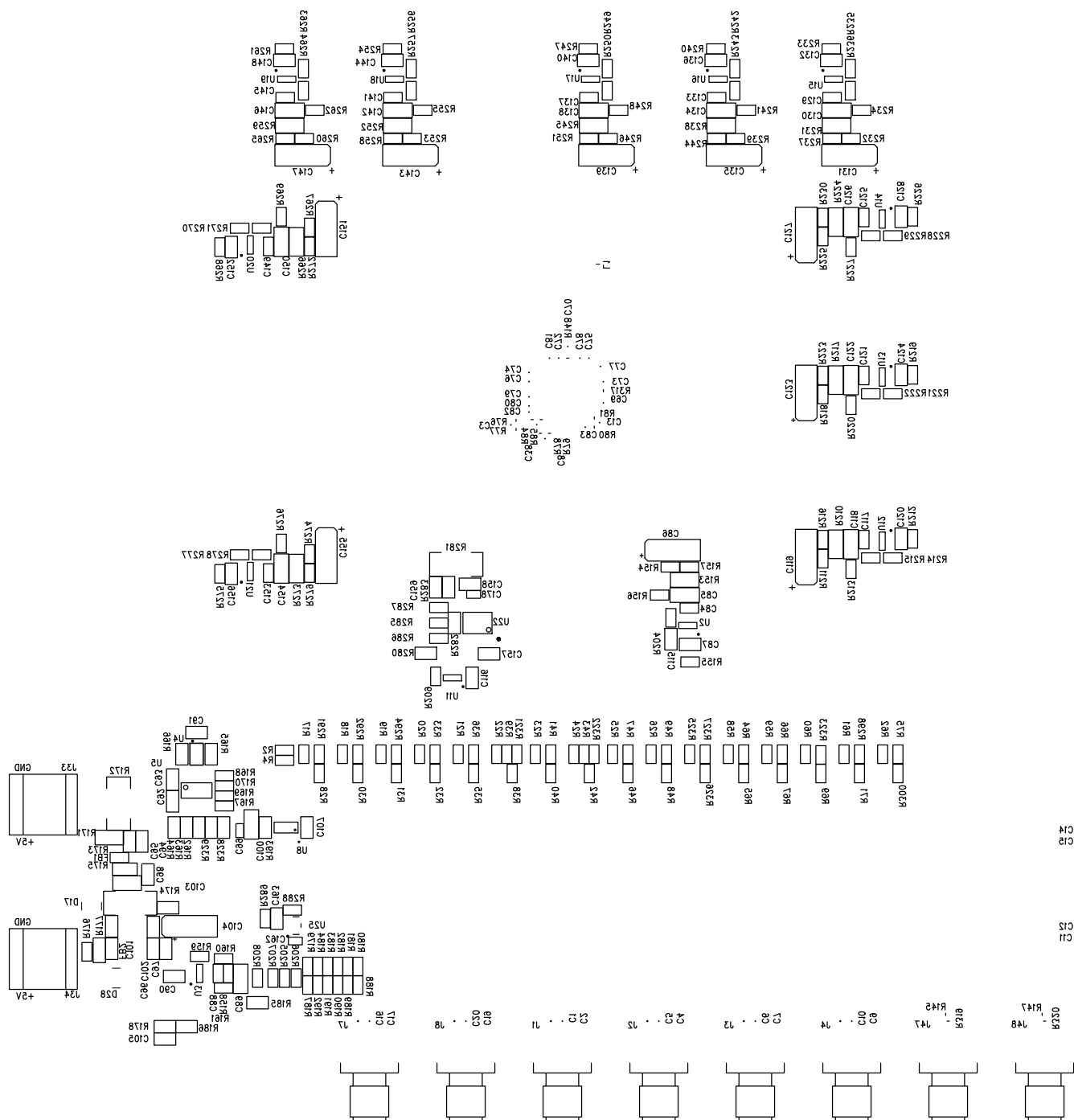
SECONDARY SIDE





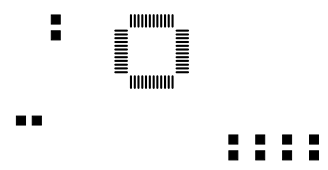
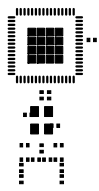
SECONDARY SOLDER MASK





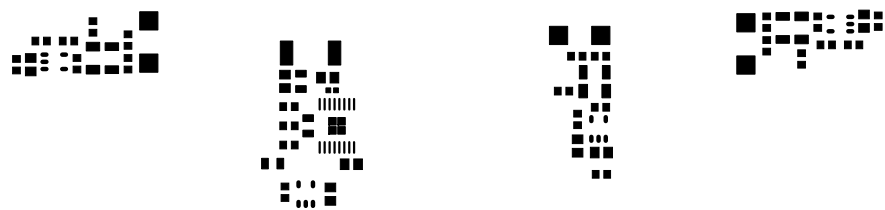
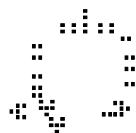
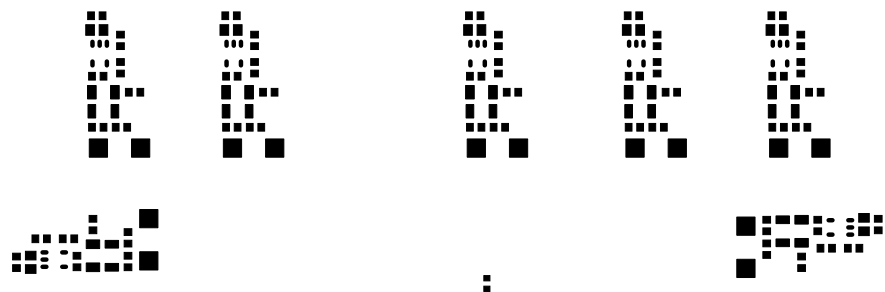


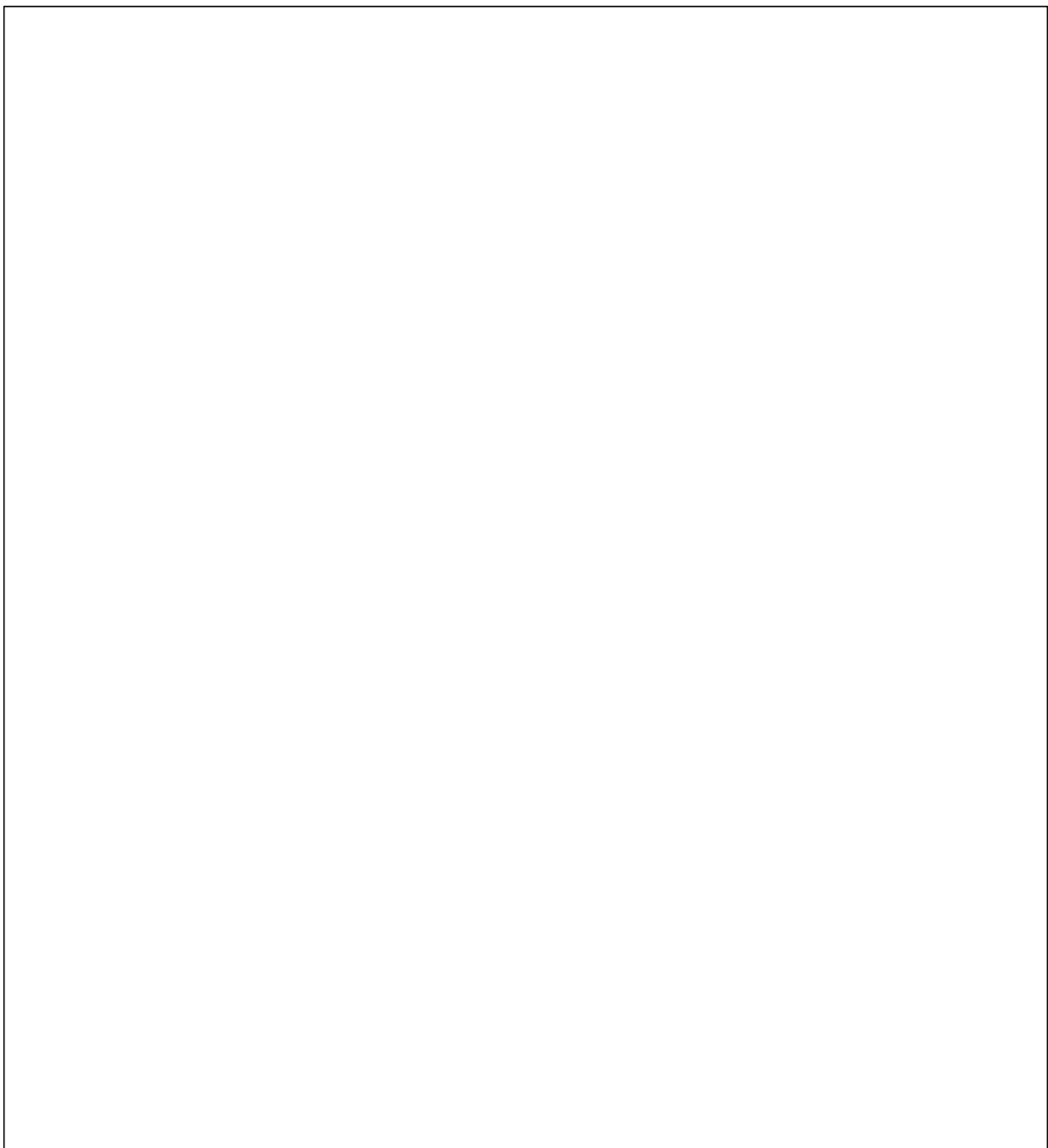
PRIMARY SOLDER PASTE

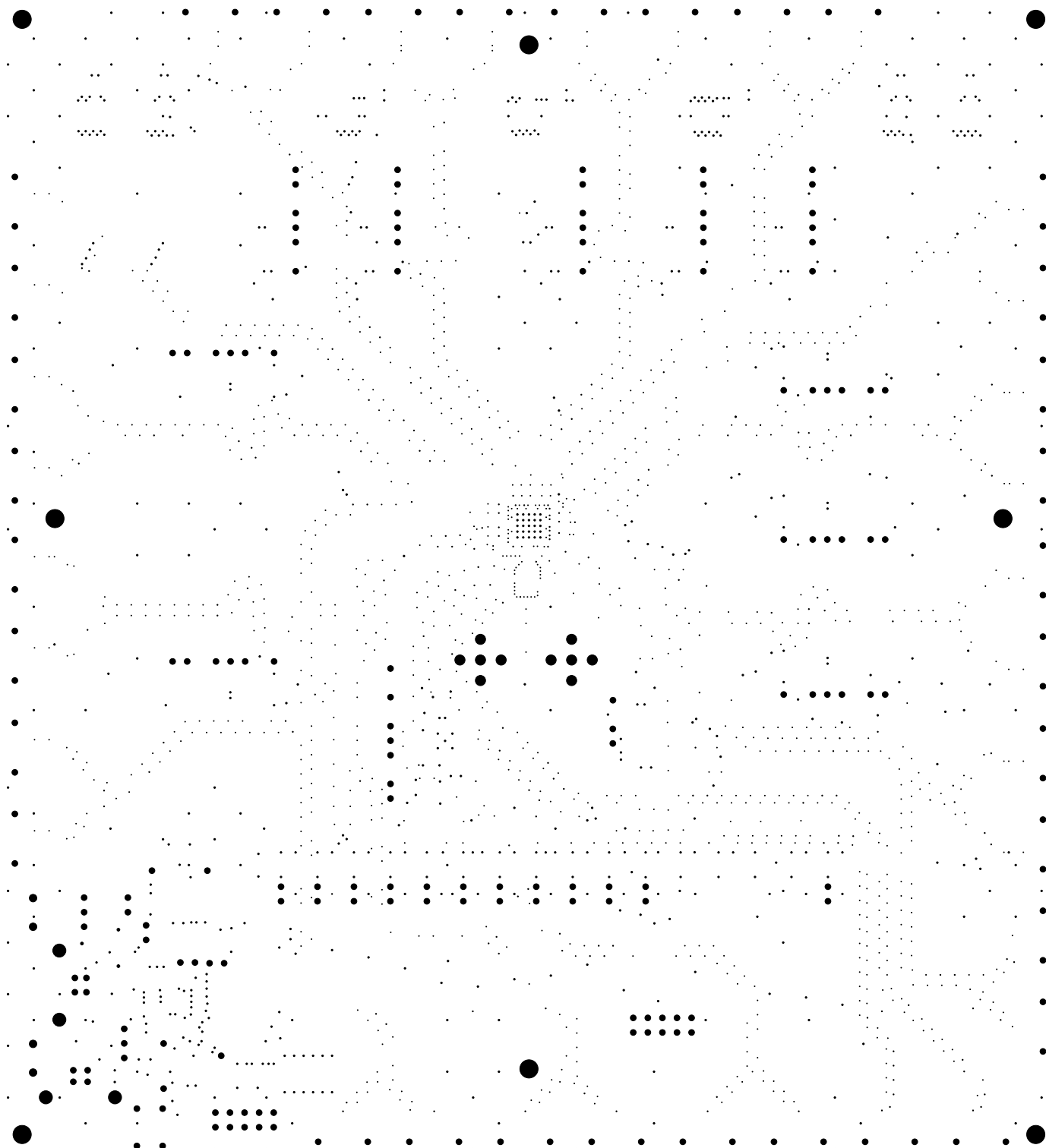




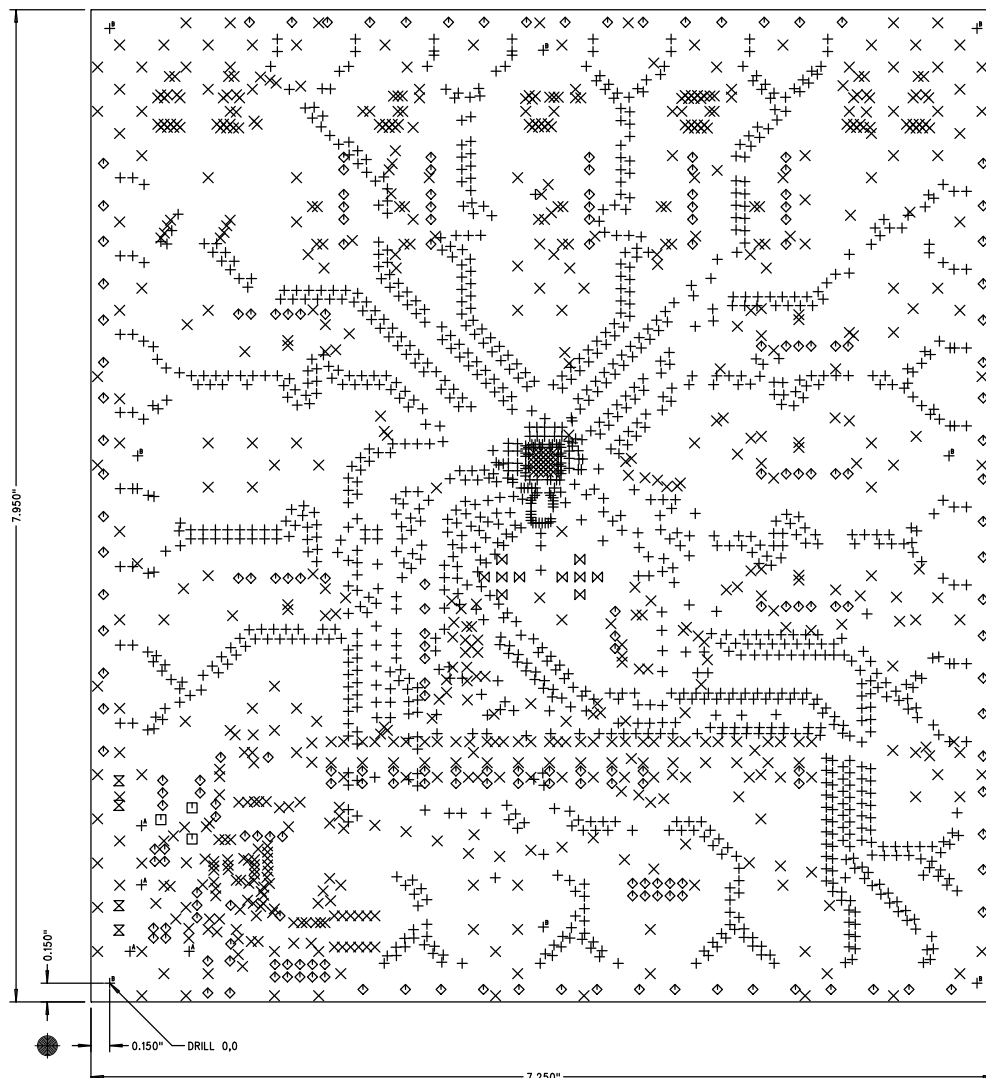
SECONDARY SOLDER PASTE







PRIMARY DRILL



NOTES : UNLESS OTHERWISE SPECIFIED


1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. MATERIAL SHALL BE COPPER CLAD ISOLA FR-406, Dk=3.9 & ISOLA FR-406 PREPREG, Dk=3.9 w/BALANCE OF MATERIAL TO BE COMPATIBLE FR-4 MEETING IPC-4101/26, PER LAYER STACKUP DETAIL.
4. COPPER WEIGHT SHALL BE 0.5 OZ./SQ. FT. BEFORE PLATING.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE ± 0.003 ".
7. MINIMUM ANNULAR RING SHALL BE 0.001".
8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE 0.062" $\pm 10\%$.
10. WARP/TWIST SHALL NOT EXCEED 1.0X.
11. FINISH SHALL BE LPI, BLUE SMOBC, ENIG BOTH SIDES.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. INTERNAL 0.175MM TRACES TO BE 50 OHM $Z_0 \pm 5\%$.
EXTERNAL 0.275MM TRACES TO BE 50 OHM $Z_0 \pm 5\%$.
TOP 0.762MM TRACES TO BE 50 OHM $Z_0 \pm 5\%$ REF TO L03.
BOTTOM 0.762MM TRACES TO BE 50 OHM $Z_0 \pm 5\%$ REF TO L06.
14. VENDOR TO PROVIDE PCB MICRO-SECTION OF COUPON AREA & TDR TEST REPORT.
15. REFERENCE ADDITIONAL FAB NOTES IN FILE README.TXT

LAYER STACKUP FILE NAMES

PRIMARY SILKSCREEN	534x-EB_PSS.PHO
PRIMARY SOLDERMASK	5345-EB_PSM.PHO
PRIMARY SIDE	5345-EB_PRI.PHO
FR-406 - 7MIL THK	
RF ROUTE/GND	5345-EB_L02.PHO
FR-406 - 7MIL THK	
GROUND PLANE	5345-EB_L03.PHO
FR-4 IPC-4101/26	
DIGITAL ROUTE/GND	5345-EB_L04.PHO
FR-4 IPC-4101/26	
VDD0x, VDD0UT, GND	5345-EB_L05.PHO
FR-4 IPC-4101/26	
GROUND PLANE	5345-EB_L06.PHO
FR-406 - 7MIL THK	
RF ROUTE/GND	5345-EB_L07.PHO
FR-406 - 7MIL THK	
SECONDARY SIDE	5345-EB_SEC.PHO
SECONDARY SOLDERMASK	5345-EB_SSM.PHO
SECONDARY SILKSCREEN	5345-EB_SSS.PHO

SCALE: NONE

SIZE	QTY	SYM	PLT	TOOL	TOL
0.006	1379	+	P	1	+0/-0.006
0.012	699	X	P	2	+0/-0.012
0.020	3	□	P	3	+/-0.003
0.040	213	◇	P	4	+/-0.003
0.052	4	⊗	P	5	+/-0.003
0.070	10	⊗	P	6	+/-0.003
0.091	4	A	P	7	+/-0.003
0.125	8	B	P	8	+/-0.003

UNLESS OTHERWISE SPECIFIED		THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART, WITHOUT THE WRITTEN CONSENT OF SILICON LABORATORIES, INC.		COMPANY:  400 W CESAR CHAVEZ ST. AUSTIN, TX 78701 (512)416-8500 www.silabs.com	
DIMENSIONS ARE IN INCHES AND APPLY AFTER FINISH DIMENSIONS IN BRACKETS () ARE IN MILLIMETERS INTERPRET DRAWING PER MIL-D-1000				NAME: Si534x-EB64	
TOLERANCES				REV: 2.1	
HOLE TOLERANCES PER 78027				SIZE: B PART NUMBER:	
DECIMALS .XX +/- .XXX +/-	ANGLES +/-	SURFACES MICRONCHES	DESIGN LAYOUT	KS/TT CT	03NOVP2014 04NOVP2014
PART TO BE FREE OF BURRS				DO NOT SCALE DRAWING	
BREAK EDGES	BEND RADIUS	BEND RELIEF	SCALE: 1:1 FABRICATION DRAWING SHEET 1 OF 1		
MAX	MAX	MAX			