AN0948: EFM32 and EFR32 Series 1 Power Configurations and DC-DC

This application note provides an overview of the integrated DC-to-DC converter (DCDC) on the EFM32 and EFR32 Series 1 devices. In addition, it describes the available hardware configurations and programming steps for each.

The EFM32 Series 1 consists of:

- EFM32 Jade Gecko (EFM32JG1/EFM32JG12/EFM32JG13)
- EFM32 Pearl Gecko (EFM32PG1/EFM32PG12/EFM32PG13)
- EFM32 Giant Gecko (EFM32GG11)

The EFR32 Wireless Gecko Series 1 consists of:

- EFR32 Blue Gecko (EFR32BG1/EFR32BG12/EFR32BG13)
- EFR32 Flex Gecko (EFR32FG1/EFR32FG12/EFR32FG13)
- EFR32 Mighty Gecko (EFR32MG1/EFR32MG12/EFR32MG13)

KEY POINTS

- DC-DC converters can improve overall system efficiency.
- EFM32 and EFR32 Series 1 devices integrate a DC-DC converter with flexible configuration options.
- EMLIB functions fully support the DC-DC converter and provide the optimal configuration for most cases.

1. DC-DC Buck Converter Theory

A DC-DC buck converter is a type of switching regulator that efficiently converts a high input voltage to a lower output voltage. A DC-DC converter is generally much more efficient than a low-dropout (LDO) regulator. For an LDO regulator, the input current generally equals the output current. As the difference between the input voltage and output voltage increases, the power efficiency decreases as more power is dissipated as heat. For the DC-DC converter, power output is proportional to power input based on an efficiency rating determined by the load current and switching losses. A DC-DC converter's efficiency may typically reach 90% under normal operating conditions, whereas the LDO peak efficiency is directly proportional to the output voltage over the input voltage (i.e., if the input is 3.3 V and output is 1.8 V, then the LDO efficiency is approximately 1.8 V/ 3.3 V, or 54%).

A basic block diagram of a generic DC-DC buck converter is shown below:

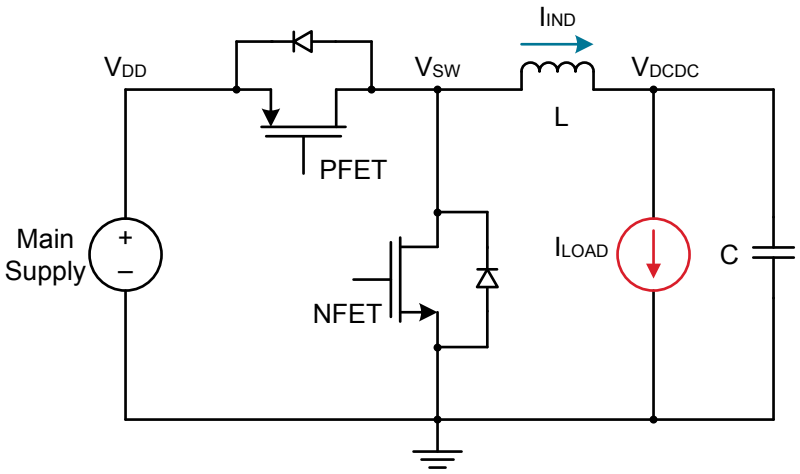


Figure 1.1. Basic DC-DC Buck Converter Block Diagram

DC-DC converters typically use one of two modulation schemes: PWM (pulse width modulation) or PFM (pulse frequency modulation). A PWM DC-DC converter modulates the on-time of the PFET switch with a constant switching frequency. This method concentrates the noise from the DC-DC converter into a single, filterable band. A PFM DC-DC converter modulates the switching frequency. While this can be more efficient, it spreads out the noise spectrum, making it harder to filter.

Continuous Conduction Mode (CCM)

Continuous Conduction Mode (CCM) occurs when the DC-DC converter's PFET and NFET switches are turned on complimentarily. In this mode, the power transfer occurs in two phases by, first, storing energy in the inductor, and, then, transferring the stored energy to the load.

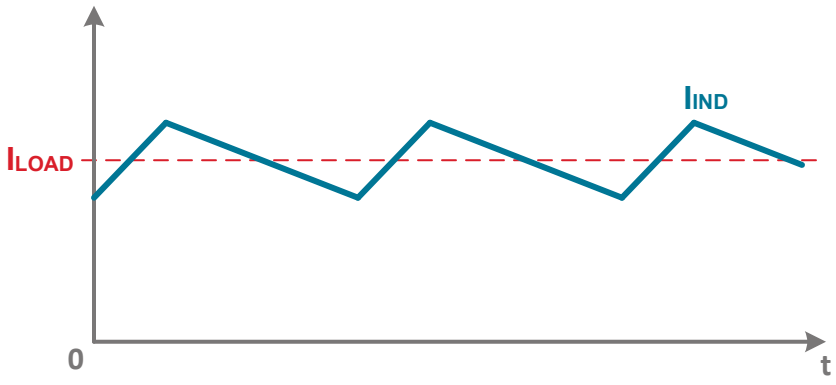


Figure 1.2. DC-DC Converter Current in Continuous Conduction Mode (CCM)

Forced Continuous Conduction Mode (FCCM)

Forced Continuous Conduction Mode (FCCM) occurs when the DC-DC converter's PFET and NFET switches are turned on complimentarily but the current to the load can be negative.

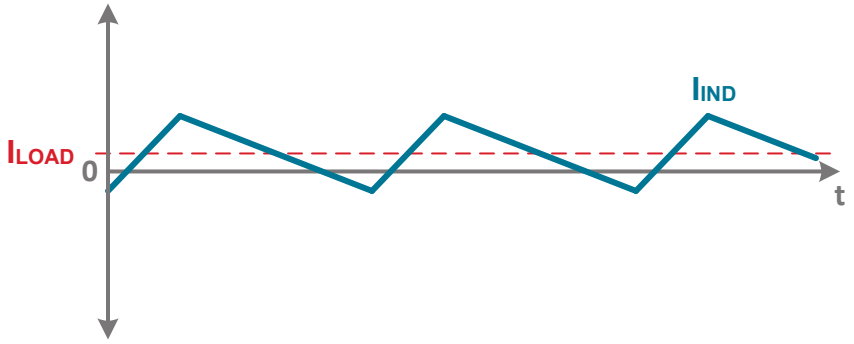


Figure 1.3. DC-DC Converter Current in Forced Continuous Conduction Mode (FCCM)

Discontinuous Conduction Mode (DCM)

Discontinuous Conduction Mode (DCM) is similar to CCM except the charge stored in the inductor is allowed to be depleted. A third phase of operation occurs when the inductor current is depleted before the next switching cycle starts. DCM can occur when the peak-to-peak inductor-current ripple (I_{IND_pp}) exceeds twice the average load current (I_{LOAD}):

$$I_{IND\_pp} > 2 \times I_{LOAD}$$

$$I_{IND\_pp} = \left(1 - \frac{V_{DCDC}}{V_{DD}}\right) \times \frac{V_{DCDC}}{f_{SW} \times L}$$

Where f_{SW} is the controller's switching frequency.

To ensure that the current to the load remains positive or zero, the hardware uses a comparator on the output to turn off the NFET switch when the current to the load starts to go negative. This ensures that charge is not being pushed back into the main supply (e.g., battery), as some supplies cannot tolerate this condition.

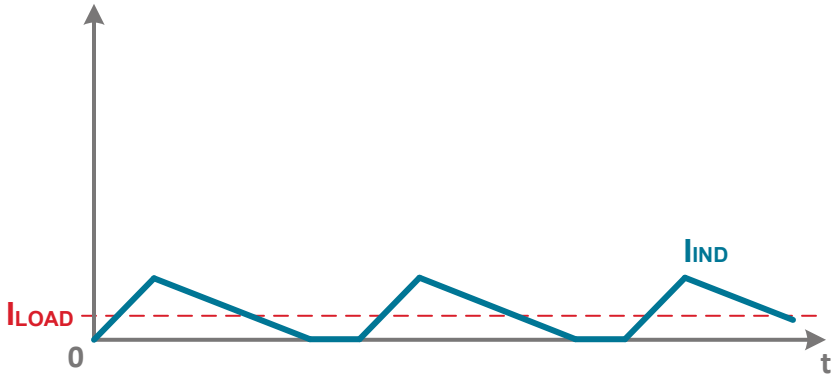


Figure 1.4. DC-DC Converter Current in Discontinuous Conduction Mode (DCM)

2. DC-DC Converter Module Overview

The EFM32 and EFR32 Series 1 devices feature a DC-to-DC buck converter which requires a single external inductor and a single external capacitor. The converter takes the VREGVDD input voltage and converts it down to an output voltage between VREGVDD and 1.8 V with a peak efficiency of approximately 90% in Low Noise (LN) mode and 85% in Low Power (LP) mode. See the datasheet for full DC-DC specifications.

The DC-DC converter operates in either Low Noise (LN) or Low Power (LP) mode. LN mode is intended for higher current operation (e.g., EM0), whereas LP mode is intended for very low current operation (e.g., below 10 mA). The DC-DC may be configured to automatically transition from LN mode in EM0/EM1 to LP mode in EM2, EM3, or EM4H. The DC-DC is always off in EM4S, and will be reset to its default (i.e., "Startup/Unconfigured") configuration.

In addition, the DC-DC converter supports an unregulated Bypass mode, in which the input voltage is directly shorted to the DC-DC output.

2.1 Major EMU and DC-DC Differences

There have been several major DC-DC and EMU changes between the first generation devices (e.g., EFM32xG1 and EFR32xG1) and the later generations (e.g., EFM32xG11/12 and EFR32xG12/13/14).

LP Mode in EM0/1

- On EFM32xG1 and EFR32xG1 devices, LP mode is not supported in EM0 or EM1. This is due to difficulties resulting from the fact that these devices have only a single LP mode configuration register (for hysteresis selection and comparator bias) that is used in all energy modes
- On EFM32xG11/12 and EFR32xG12/13/14 devices, LP mode is supported for light loads (<10 mA) in EM0 or EM1. For these devices, it is recommended to switch to LP rather than LN DCM when the EM0/1 current is below 10 mA. The LP configuration for EM0 and EM1 is set in the EMU_DCDCLPEM01CFG register. The LP configuration for EM2, 3, 4 is set in the EMU_DCDCMISCCTRL register (comparator bias) EMU_DCDCLPCTRL register (hysteresis). Unless otherwise specified, all other LP configuration control bits apply to LP mode cross energy modes.
- For more information, see 5.5 Low Power Mode Hysteresis

PFETCNT / NFETCNT Bitfields

- On EFM32xG1 and EFR32xG1 devices, the PFETCNT / NFETCNT bitfield settings affect both LP and LN modes. Therefore, when transitioning from LN to LP mode, software may need to update the PFETCNT setting desired for LP mode while still in LN mode, potentially resulting in a momentary efficiency hit.
- On EFM32xG11/12 and EFR32xG12/13/14 devices, the PFETCNT / NFETCNT bitfield settings only affect LN mode. The LP mode PFETCNT / NFETCNT settings are fixed in hardware.

State of the DC-DC Output (V_{DCDC}) after Power-On

- After power-on, EFM32xG1 and EFR32xG1 devices enter the "Startup" configuration. In this state, V_{DCDC} is shorted to the VREGVDD pin. If IOVDD is powered from the DC-DC, then any circuit attached to IOVDD will also powered at startup (although at the higher VREGVDD voltage). Upon entry into EM4 Shutoff, the DC-DC converter configuration is reset to its default "Startup" configuration with VREGVDD shorted to V_{DCDC}. This means that any circuitry attached to V_{DCDC} will also be powered up in EM4 Shutoff.
- After power-on, EFM32xG11/12 and EFR32xG12/13/14 devices enter the "Unconfigured" configuration. In this state, V_{DCDC} is unconnected internally. If IOVDD is powered from the DC-DC, then any circuit attached to IOVDD will not be powered until the DC-DC is configured (or the bypass switch is enabled). Likewise, upon entry into EM4 Shutoff, the DC-DC converter configuration is reset to its default "Unconfigured" configuration. If IOVDD = V_{DCDC}, then any circuits attached to IOVDD will remain unpowered until the system is reset to exit EM4 Shutoff, and the DC-DC is configured (or the bypass switch is enabled).
- For more information and block diagrams, see 3.1 "Startup" or "Unconfigured" Configuration

Digital LDO Input Supply Voltage

- On EFM32xG1 and EFR32xG1 devices, the Digital LDO input is always the DVDD pin. For this reason, the DVDD pin must always be powered at startup.
- On EFM32xG11/12 and EFR32xG12/13/14 devices, the Digital LDO may be powered from either AVDD or DVDD, depending on the configuration of the REGPWRSEL bit in the EMU_PWRCTRL register. By default, the Digital LDO is powered from the AVDD pin and the total LDO current is limited to 20 mA. Out of startup, firmware should configure and enable the DCDC (if desired) and then configure the Digital LDO input to "DVDD" (REGPWRSEL=1) before increasing the core clock frequency.

Digital LDO Voltage Scaling

- EFM32xG1 and EFR32xG1 do not support Digital LDO Voltage Scaling. The Digital LDO output voltage is fixed at 1.2V.
- EFM32xG11/12 and EFR32xG12/13/14 devices support Digital LDO Voltage Scaling. For additional power savings, the Digital LDO output voltage may be scaled based on processor frequency. Please refer to the Datasheet for maximum supported system frequencies for different Voltage Scaling Levels.

Table 2.1. Summary of Major EMU and DC-DC Converter Differences

Device	LP Mode Allowable Energy Modes	DC-DC Output (V_{DCDC}) State At Power-On	Digital LDO Input Supply At Power-On	Digital LDO Voltage Scaling
EFM32xG1 and EFR32xG1	EM2/3/4	Shorted to VREGVDD	DVDD pin	Not Supported
EFM32xG11/12 and EFR32xG12/13/14	EM0/1/2/3/4	Floating	AVDD pin	Supported

2.2 Bypass Mode

In Bypass mode (i.e., bypass switch is on), the VREGVDD input voltage is directly shorted to the DC-DC converter output through an internal switch. See the datasheet for the Bypass switch impedance specification.

The Bypass Current Limit limits the maximum current drawn from the input supply in Bypass mode. This current limit is enabled by setting the BYPLIMEN bit in the EMU_DCDCCLIMCTRL register, and the limit value may be adjusted between 20 mA and 320 mA using the BYPLIMSEL bitfield in the EMU_DCDCMISCCTRL register. When the difference between the DC-DC output voltage (V_{DCDC}) and the DC-DC input voltage (VREGVDD) is large, applications should enable the Bypass Current Limit before enabling Bypass mode. For example, if Bypass mode is enabled with VREGVDD=3.8 V and V_{DCDC}=1.8 V with a 4.7 µF capacitor, the peak current draw may be quite large as it is limited only by the bypass switch on-resistance, which could result in drooping on the input supply voltage. For smaller input / output voltage differences (e.g., VREGVDD=2.4 V and V_{DCDC}=1.8 V), it may not be necessary to enable the Bypass Current Limit at all.

Note that the device will see an additional ~10 µA of current draw when both the Bypass Current Limiter and Bypass Mode are enabled. Applications should therefore disable the Bypass Current Limiter (i.e., set BYPLIMEN = 0) after the DVDD voltage has reached the main supply voltage in Bypass Mode. By default, the EMLIB functions to enable Bypass Mode do not ever enable the Bypass Current Limiter, to avoid inadvertently causing the additional ~10 µA current draw.

On EFM32xG1 and EFR32xG1 devices, the DC-DC converter has its bypass switch ON out of reset. On EFM32xG11/12 and EFR32xG12/13/14 devices, the DC-DC converter has its bypass switch OFF out of reset..

2.3 Low Power (LP) Mode

The Low Power (LP) controller operates in a hysteretic mode to keep the output voltage within a defined voltage band. Once the DC-DC output voltage drops below a programmable internal reference, the LP controller generates a pulse train to control the powertrain PFET switch, which charges up the DC-DC output capacitor. When the output voltage is at the programmed upper level, the powertrain PFET is turned off. The output ripple voltage may be quite large (>100 mV) in LP mode.

The LP controller supports load currents up to approximately 10 mA. On EFM32xG1 and EFR32xG1 devices, LP mode can only be used EM2, EM3, or EM4H energy modes. On EFM32xG11/12 and EFR32xG12/13/14 devices, LP mode can be used in any energy mode besides EM4S, as long as the current is below 10 mA.

2.4 Low Noise (LN) Mode

The Low Noise (LN) controller continuously switches the powertrain NFET and PFET switches to maintain a constant programmed voltage at the DVDD pin. The LN controller supports load current from sub-mA up to 200 mA.

The LN controller switching frequency is programmable using the RCOBAND bitfield in the EMU_DCDCLNFREQCTRL register. See below for recommended RCOBAND settings for each mode.

The DC-DC Low Noise controller operates in one of two modes:

1. Continuous Conduction Mode (CCM)
2. Discontinuous Conduction Mode (DCM)

2.4.1 Low Noise (LN) Continuous Conduction Mode (CCM)

CCM operation is configured by setting the LNFORCECCM bit in the EMU_DCDCMISCCTRL register. CCM can be used to improve the DC-DC converter's output transient response time to quick load current changes, which minimizes voltage transients on the DC-DC output.

Note that all references to CCM in the documentation actually refer to Forced Continuous Conduction Mode (FCCM) - that is, if the LNFORCECCM bit is set and the output load current is very low, the DC-DC is forced to operate in CCM. In this case, the current through the inductor may be negative and current may flow back into the battery.

CCM is required for radio applications because it allows use of the EFR32 Series 1 device's radio interference minimization features. These features are not available in DCM.

In CCM, the recommended DC-DC converter switching frequency is 6.4 MHz (RCOBAND = 4) . Note that when the radio's interference minimization features are enabled, RCOBAND = 4 corresponds to a DC-DC converter switching frequency of 7 MHz.

2.4.2 Low Noise (LN) Discontinuous Conduction Mode (DCM)

To enable DCM, the LNFORCECCM bit in EMU_DCDCMISCCTRL must be cleared before entering LN. Typically, this configuration occurs while the part is in Bypass mode. Once DCM is enabled, the DC-DC should operate in DCM at light load currents. However, as the load current increases, the DC-DC automatically transitions into CCM without software intervention.

The advantage of DCM is improved efficiency for light load currents. However, the disadvantage is that DCM increases the potential RF switching interference, because in DCM the DC-DC switching events are load dependent and can no longer be synchronized with radio operation. In addition, the DC-DC in DCM has poorer dynamic response to changes in load current, leading to potentially larger changes in the regulated output voltage. For these reasons, DCM is not recommended for radio applications or for non-radio applications that expect large instantaneous load current steps. For example, if the DC-DC is in DCM, firmware may need to increment the core clock frequency in small steps to prevent a large sudden load increase.

In DCM, the recommended DC-DC converter switching frequency is 3 MHz (RCOBAND = 0).

2.5 Analog Peripheral Power Selection

The analog peripherals (e.g., ULFRCO, LFRCO, LFXO, HFRCO, AUXHFRCO, VMON, IDAC, ADC) are powered from an internal analog supply domain, VDDX_ANA. VDDX_ANA may be supplied from either the AVDD or DVDD supply pins, depending on the configuration of the ANASW bit in the EMU_PWRCTRL register. Changes to the ANASW setting should be made immediately out of reset (i.e., in the Startup or Unconfigured Configuration) before all clocks (with the exception of HFRCO and ULFRCO) are enabled. Once ANASW is configured, it should not be changed.

Table 2.2. Analog Peripheral Power Configuration

ANASW	Analog Peripheral Power Supply Source (VDDX_ANA)	Comments
0 (default)	AVDD pin	This configuration may provide a quieter supply to the analog modules, but is less efficient as AVDD is typically at a higher voltage than DVDD.
1	DVDD pin	This configuration may provide a noisier supply to the analog modules, but it is more efficient. However, because the maximum allowable input voltage to many of the analog modules using APORT is limited to MIN(VDDX_ANA,IOVDD), this setting could artificially limit your analog input range.

Note that the flash is always powered from the AVDD pin regardless of the state of the ANASW bit.

2.6 LN Efficiency Optimization vs. Load Current and DC-DC Mode

The DC-DC converter is designed to operate efficiently over a very wide range of current loads (<75 uA up to 200 mA). However, to optimize efficiency, the powertrain NFET and PFET switch configuration can be adjusted based on the load current, DC-DC mode (e.g., CCM vs. DCM), and switching frequency. The powertrain NFET and PFET switches, which allow a tradeoff between the powertrain switching loss and conduction loss, are configured using the NFETCNT and PFETCNT bitfields in the EMU_DCDCMISCCTRL register.

Table 2.3. Recommended PFET/NFET Settings vs. Load Current and LN DC-DC Mode

LN CCM 7MHz Load Current, I_{LOAD}	LN CCM 3MHz Load Current, I_{LOAD}	LN DCM 3MHz Load Current, I_{LOAD}	Recommended Drive Setting	Recommended PFETCNT/ NFETCNT Configuration
I_{LOAD}< 20 mA	(* Medium Drive always recommended for optimal efficiency)	I_{LOAD}< 10 mA	Light	3
20 mA ≤ I_{LOAD} < 40 mA	I_{LOAD}< 40 mA	10 mA ≤ I_{LOAD} < 20 mA	Medium	7
40 mA ≤ I_{LOAD}	40 mA ≤ I_{LOAD}	20 mA ≤ I_{LOAD}	Heavy	15

The plots below show the DCM Light Drive and CCM Light/Medium/Heavy Drive efficiencies vs load currents, for input voltages of 3.8 V, 3.3 V, and 2.4 V.

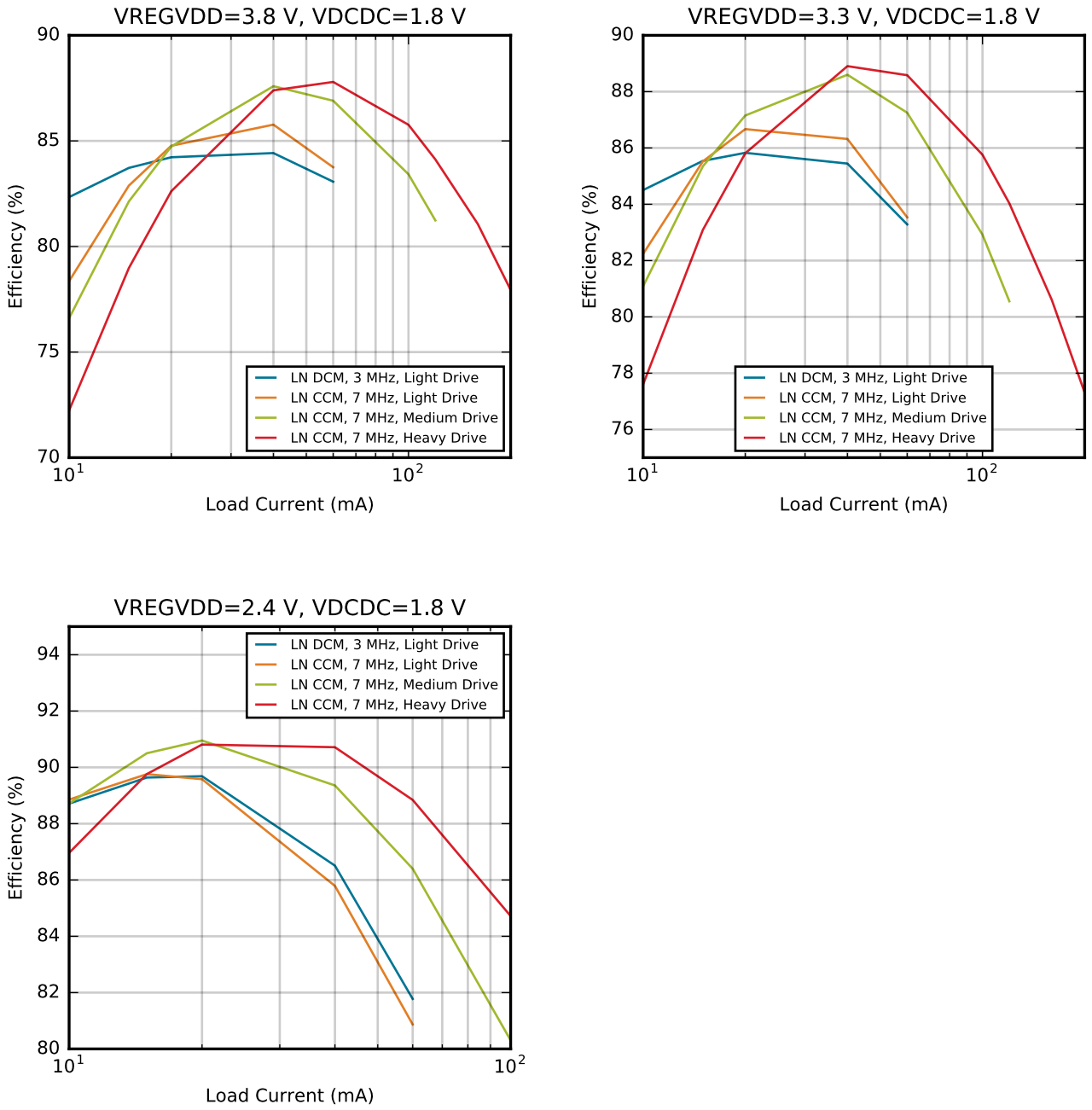


Figure 2.1. 3 MHz DCM Light Drive/ 7 MHz CCM Light/Medium/Heavy Drive Efficiency vs Load Current

2.7 DC-DC Maximum Output Current vs. Minimum Input Voltage

As the DC-DC input supply voltage decreases, consideration must be given to both the ambient temperature and the maximum load current. As the input voltage nears its minimum voltage, the DC-DC converter performance is impacted in two ways:

1. The DC-DC converter efficiency decreases to a point where it provides limited benefit compared to Bypass mode
2. The DC-DC converter eventually loses the ability to maintain a constant output voltage, and enters dropout. When dropout occurs, the DC-DC will no longer be in regulation and significant overshoot/undershoot will occur, which may cause the brown-out detectors to trip and reset the device.

To avoid dropout, the system should switch the DC-DC to Bypass mode when the input supply voltage drops to the minimum. Some hysteresis (e.g., 100 mV~200 mV) should be used to prevent the DC-DC from toggling back into switching mode due to small input supply voltage variations. Note that the DC-DC module doesn't provide a means to directly monitor the input supply voltage; however, input supply voltage monitoring may be implemented through other means, for example using the on-chip VMON supply monitor, the on-chip ADC, or using an off-chip voltage supervisor IC.

Low Noise Mode

Note: The guidelines below must be followed. Failure to follow these guidelines may result in inefficient DC-DC operation or DC-DC output supply brownouts and unintended resets.

The minimum input voltage in LN mode depends on both the DC-DC load current as well as the ambient temperature (T_{amb}), because the maximum DC-DC load current is limited to 100 mA above T_{amb}=85°C. See the table below for the recommended minimum VREGVDD input supply voltage to prevent dropout for particular conditions.

The powertrain NFET and PFET switches are configured by the NFETCNT and PFETCNT bitfields in the EMU_DCDCMISCCTRL register.

Table 2.4. DC-DC Configuration, Maximum Load Current, and Minimum Input Voltage in Low Noise Mode

Maximum Load Current, I_{LOAD}	Drive	Minimum VREGVDD Input Voltage	Maximum Ambient Temperature, T_{amb}	PFETCNT/NFETCNT Configuration
50 mA	Light	2.4 V	125°C	3
100 mA	Medium	2.4 V	125°C	7
200 mA	Heavy	2.6 V	85°C	15

Low Power Mode

Note: The guidelines below must be followed. Failure to follow these guidelines may result in inefficient DC-DC operation or DC-DC output supply brownouts and unintended resets.

The DC-DC Low Power controller comparator bias may be adjusted based on load current using the LPCMPBIAS bitfield in the EMU_DCDCMISCCTRL register. For EFM32xG1 and EFR32xG1 devices, the powertrain switches are always recommended to be set to 7 in Low Power mode (i.e., PFETCNT = NFETCNT = 7), regardless of load. On EFM32xG11/12 and EFR32xG12/13/14 devices, the PFETCNT / NFETCNT settings for LP mode are fixed in hardware and don't need to be set by firmware. See ● PFETCNT / NFETCNT Bitfields on page 4 for more details.

Table 2.5. DC-DC Configuration, Maximum Load Current, and Minimum Input Voltage in Low Power Mode

Maximum Load Current, I_{LOAD}	Minimum VREGVDD Input Voltage	Maximum Ambient Temperature, T_{amb}	LPCMPBIAS Configuration
75 µA	2.4 V	125°C	0
500 µA	2.4 V	125°C	1
2.5 mA	2.4 V	125°C	2
10 mA	2.4 V	125°C	3

Bypass Mode

After the DC-DC is switched to bypass mode, it can operate with a VREGVDD input as low as 1.85 V. However, because the internal bypass switch has a finite on-resistance (R_{BYP}, see the datasheet specification for the maximum value), the voltage at the DVDD pin may be below $DVDD_{min}$, depending on the load current.

The minimum VREGVDD input supply voltage may be determined using the following equation:

$$VREGVDD_{MIN} = DVDD_{MIN} + \left[I_{LOAD} \times \left(R_{BYP} + R_{PCB}\right)\right]$$

Users should apply some margin to this equation to account for variations in I_{LOAD}, R_{BYP}, and R_{PCB}. In addition, PCB designers should make an effort to reduce the parasitic trace resistance as much as possible on the power supply routing to minimize R_{PCB}.

2.8 DC-DC Efficiency Threshold

A DC-DC's efficiency peaks at high current loads, and drops off as the load current is reduced. Once the DC-DC converter efficiency drops below a certain threshold, not only is there no benefit to using it, but it is less efficient than turning off the DC-DC and powering the output directly from the main supply.

This efficiency threshold may be calculated by dividing the DC-DC output voltage by the DC-DC input voltage. For example, when the main supply is at 3.0 V and the DC-DC output is configured for 1.8 V, the DC-DC efficiency threshold is 60%. When the DC-DC converter is operating below the threshold, the firmware should put the device into bypass mode.

The table below shows the efficiency threshold for both DCM and CCM over a range of input voltages.

Table 2.6. DC-DC Converter Efficiency Threshold: Low Noise Mode, Light Drive

VREGVDD Input Voltage	V_{DCDC} Output Voltage	Efficiency Threshold	DCM, 3 MHz Load Current at Efficiency Threshold	CCM, 7 MHz Load Current at Efficiency Threshold
3.8 V	1.8 V	47.4%	1.0 mA	2.5 mA
3.3 V	1.8 V	54.5%	1.0 mA	2.5 mA
2.4 V	1.8 V	75%	2.0 mA	3.0 mA

The charts below show the DCM and CCM Light Drive efficiencies vs load currents, for input voltages of 3.8 V, 3.3 V, and 2.4 V.

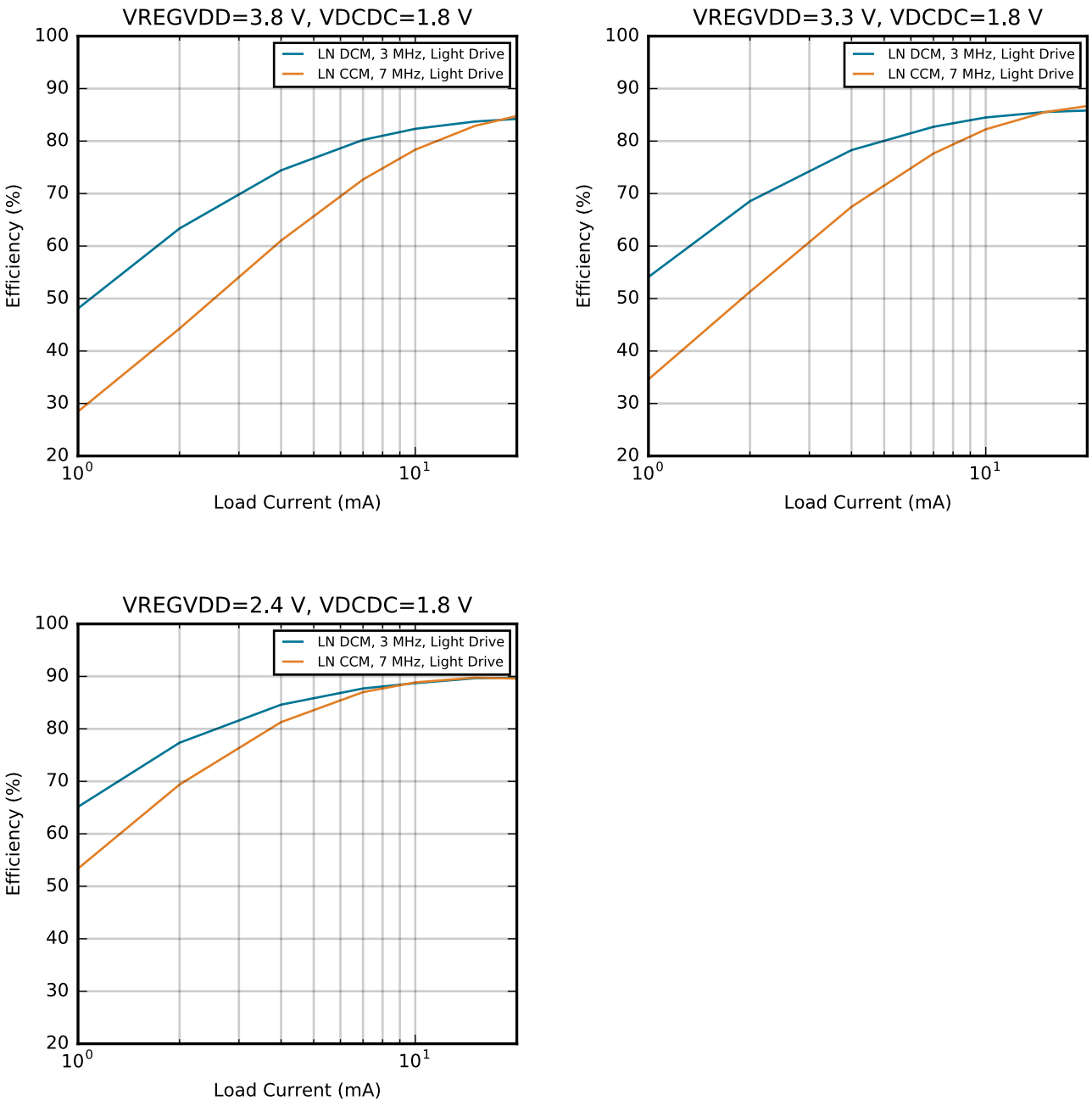


Figure 2.2. DCM/CCM Light Drive Efficiency vs Load Current

2.9 Using the DC-DC Converter to Power External Loads

While the DC-DC converter is primarily intended to power the internal, on-chip loads (e.g., radio and core), it may be used to power external devices as well. However, systems using the DC-DC converter to power external devices should consider the following:

1. The total worst-case maximum static DC-DC load currents, including both internal and external devices for active and low energy modes. The maximum total load current should be used when calling the EMLIB configuration and optimization functions (see section 2.7 DC-DC Maximum Output Current vs. Minimum Input Voltage).
2. The worst-case maximum transient load current, including both internal and external devices for active and low energy modes.
3. The maximum load current drawn in Bypass mode (see section 2.7 DC-DC Maximum Output Current vs. Minimum Input Voltage).
4. The required voltage-regulation accuracy and ripple voltage tolerance of the external devices.
5. The power-up/down timing requirements for external devices.

3. DC-DC Power Configurations

EFM32 and EFR32 Series 1 devices have a default startup configuration and three selectable power configurations. A power configuration is defined as a combination of hardware (i.e., PCB and schematic) connections and firmware (i.e., EMLIB).

EFM32 Series 1 Power Supply Requirements

- VREGVDD = AVDD (Must be the highest voltage in the system)
- VREGVDD >= DVDD
- VREGVDD >= IOVDD
- DVDD >= DECOUPLE

EFR32 Series 1 Power Supply Requirements

- VREGVDD = AVDD (Must be the highest voltage in the system)
- VREGVDD >= DVDD
- VREGVDD >= PAVDD (For 2.4GHz or Dual band devices, PAVDD refers to the device pin. For sub-GHz devices, PAVDD refers to the external power amplifier supply connection.)
- VREGVDD >= RFVDD
- VREGVDD >= IOVDD
- DVDD >= DECOUPLE

Power Supply Pin Overview

Note that not all supply pins exist on all devices. The table below provides a description of the available power supply pins.

Table 3.1. Power Supply Pin Overview

Pin Name	Product Family	Description
AVDD	All devices	Supply to analog peripherals
DECOUPLE	All devices	Output of the internal Digital LDO & Digital logic power supply
IOVDD	All devices	GPIO supply voltage
VREGVDD	All devices	Input to the DC-DC converter
VREGSW	All devices	DC-DC powertrain switching node
VREGVSS	All devices	DC-DC ground
DVDD	All devices	DC-DC feedback node and input to the internal Digital LDO
RFVDD	EFR32 Series 1 only	Supply to radio analog.
PAVDD	EFR32 Series 1 only	Supply to 2.4 GHz radio power amplifier

3.1 "Startup" or "Unconfigured" Configuration

During power-on reset (POR), the system boots up in a safe state that supports all available Power Configurations. On EFM32xG1 and EFR32xG1 devices, this state is called the "Startup" Configuration, and on EFM32xG11/12 and EFR32xG12/13/14 devices this state is called the "Unconfigured" Configuration.

Startup Configuration on EFM32xG1 and EFR32xG1

In the Startup Configuration:

- The DC-DC converter's Bypass switch is On (i.e., the VREGVDD pin is shorted internally to the DVDD pin).
- The analog blocks are powered from the AVDD supply pin (i.e., ANASW=0).

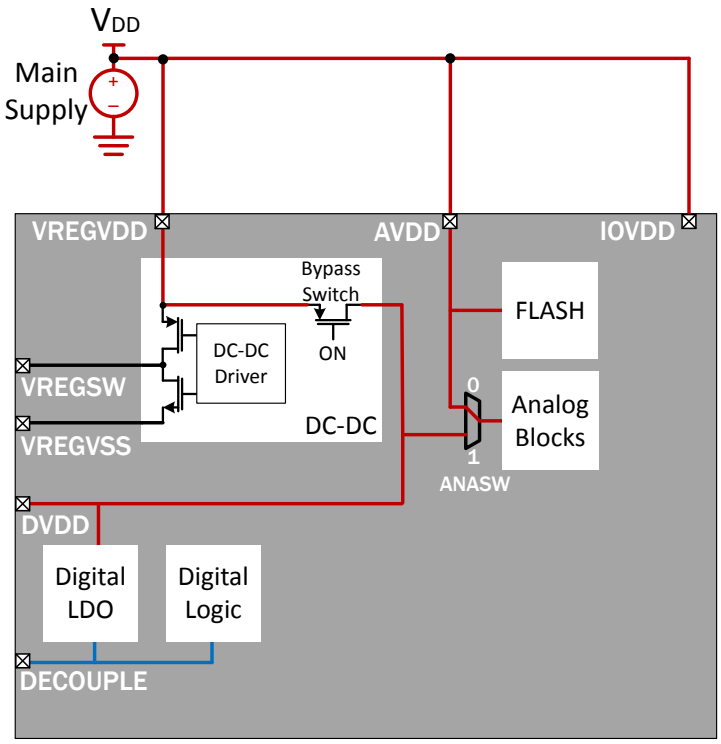


Figure 3.1. Startup Configuration

Unconfigured Configuration on EFM32xG11/12 and EFR32xG12/13/14

In the Unconfigured Configuration:

- The DC-DC converter's Bypass switch is OFF. The DVDD pin and DC-DC Output will be floating.
- The internal digital LDO is powered from the AVDD pin (i.e. REGPWRSEL=0 in EMU_PWRCTRL). Note the maximum allowable current into the LDO when REGPWRSEL=0 is 20 mA. For this reason, immediately after startup firmware should configure REGPWRSEL= 1 to power the digital LDO from DVDD.
- The analog blocks are powered from the AVDD supply pin (i.e., ANASW=0 in EMU_PWRCTRL).

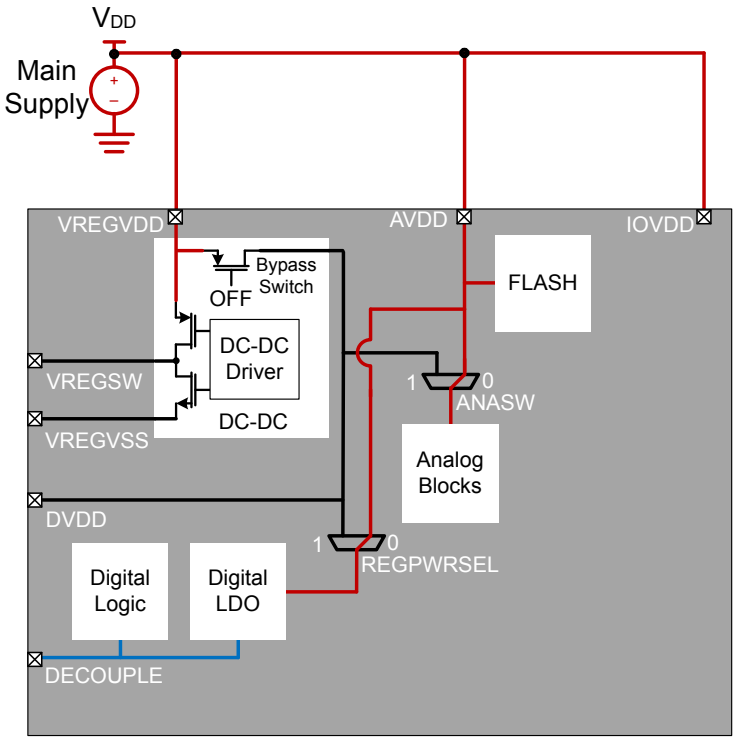


Figure 3.2. Unconfigured Configuration

3.2 Power Configuration 1: No DC-DC

In certain applications, use of the integrated DC-DC converter isn't ideal. For example:

- The application is extremely space-sensitive or cost-sensitive.
- The application's power efficiency isn't important.
- The application's expected EM0/EM1 currents are very low (i.e., ~3 mA or less). See section 2.8 DC-DC Efficiency Threshold.

In Power Configuration 1:

- The DC-DC converter is programmed in Off mode (see section 4.2 To initialize the DC-DC converter to OFF) and the Bypass switch is Off. The DVDD pin must be powered externally - typically, DVDD is connected to the main supply.
- DVDD powers the internal Digital LDO (i.e., REGPWRSEL=1 in EFR32xG12/13/14) which powers the digital circuits.
- RFVDD and PAVDD (EFR32 Series 1 only), which power the radio, are also shorted to the main supply.
- The IOVDD pin(s) are powered from the main supply.
- AVDD is powered from the main supply.
- VREGSW should be left disconnected in this configuration.

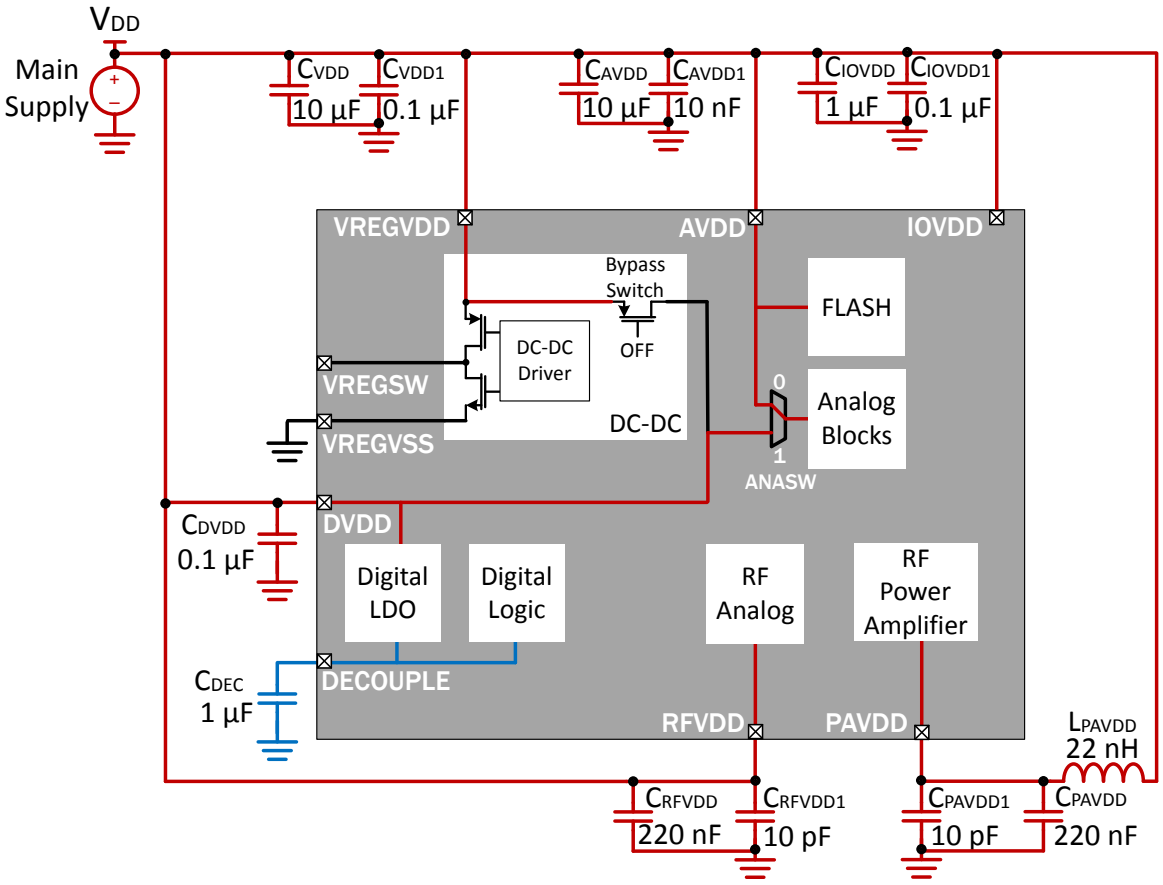


Figure 3.3. EFR32xG1 Power Configuration 1 — No DC-DC

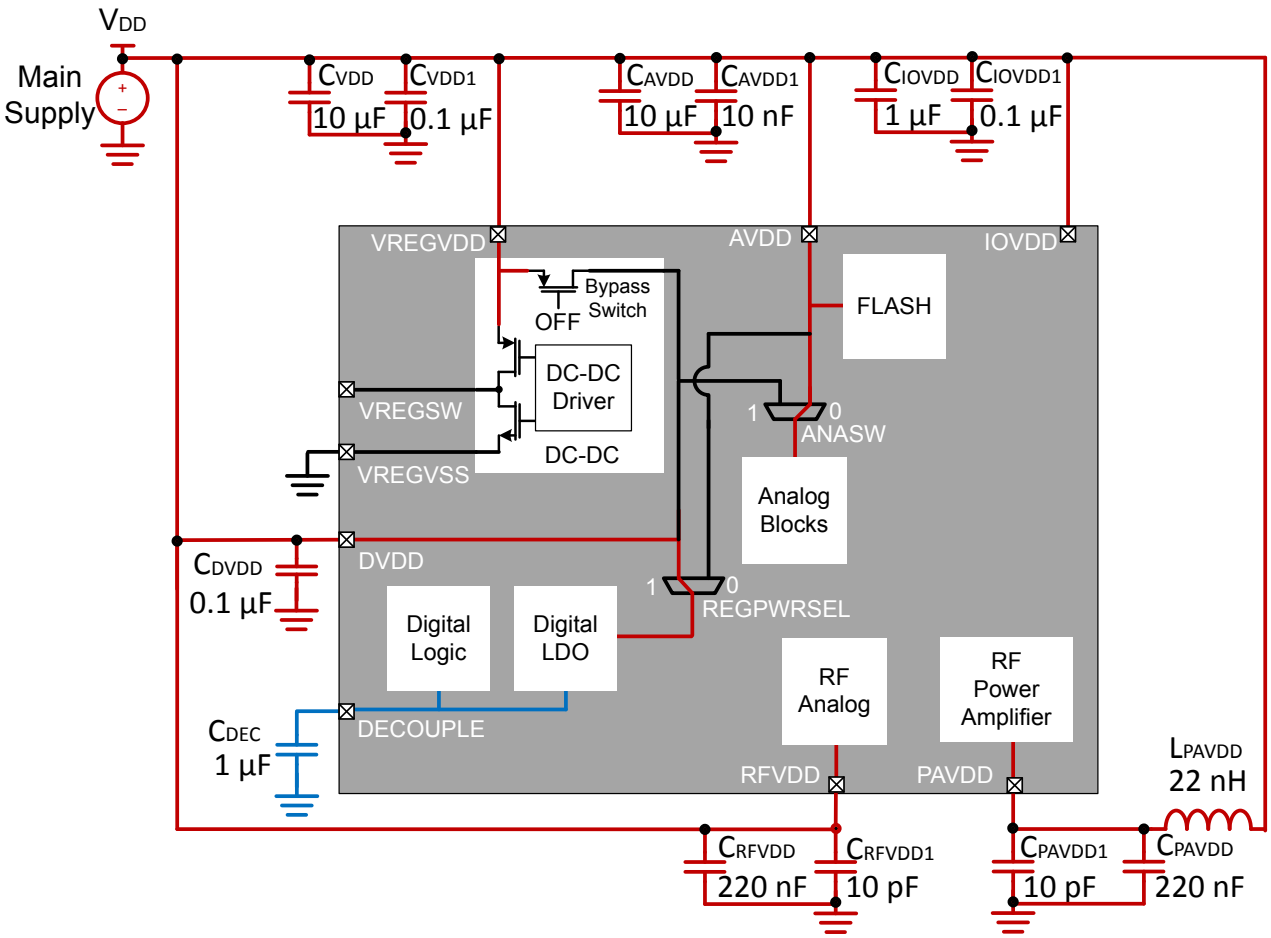


Figure 3.4. EFR32xG12/13/14 Power Configuration 1 — No DC-DC

3.3 Power Configuration 2: DC-DC

For the lowest power applications, the DC-DC converter can be used to power the DVDD supply, as well as the RFVDD and PAVDD supplies (EFR32 Series 1 only).

In Power Configuration 2:

- The DC-DC Output (V_{DCDC}) is connected to the DVDD. DVDD powers the internal Digital LDO, which powers the digital circuits.
- DVDD powers the internal Digital LDO (i.e., REGPWRSEL=1 in EFR32xG12/13/14) which powers the digital circuits.
- RFVDD (EFR32 Series 1 only) is also powered from the DC-DC Output. RFVDD powers the radio analog.
- PAVDD (EFR32 Series 1 only) is connected to the DC-DC output through a filter. PAVDD powers the power amplifier used for the radio.
- AVDD is connected to the main supply voltage. The internal analog blocks may be powered from AVDD or DVDD, depending on the ANASW configuration. Flash is always powered from the AVDD pin.
- The IOVDD pin(s) can be connected to either the main supply (as shown below) or to V_{DCDC}, depending on the system I/O requirements. However, on all devices except EFR32xG1, V_{DCDC} will be unpowered (i.e., floating) at startup. On those devices, if IOVDD is powered from the DC-DC converter, then any circuit attached to IOVDD will not be powered until the DC-DC is configured (or the bypass switch is enabled). This can result in a situation where the device cannot be programmed or the bootloader cannot be used (because both of those operations require IOVDD to be valid). Refer to the "IOVDD Connection" section of the Reference Manual EMU chapter for further details and issues that may result when connecting IOVDD to V_{DCDC}.

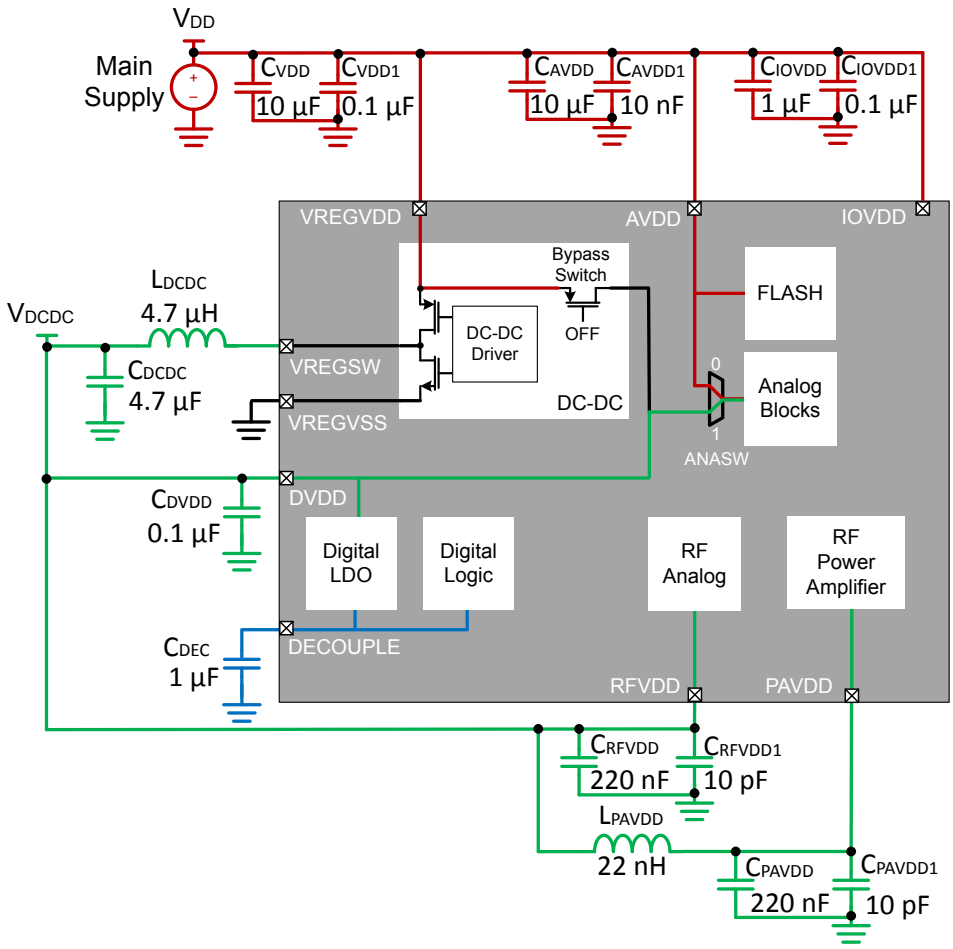


Figure 3.5. EFR32xG1 Power Configuration 2 — DC-DC Powers DVDD

Note: C_{DCDC} was 1.0 µF in some previous revisions of this application note. Although 1.0 µF may still be used, 4.7 µF is now recommended for new designs due to its improved performance under dynamic load conditions and during mode changes. Silicon Labs EFR32xG1 reference radio boards still use 1.0 µF; therefore, the EFR32xG1 software defaults to using 1.0 µF (use of emuDcdcLnCompCtrl_1u0F rather than emuDcdcLnCompCtrl_4u7F). Use of 4.7 µF on EFR32xG1 requires modification of the Low Noise Mode Compensator Control emuDcdcLnCompCtrl value. For EFR32xG12 and later, both the radio reference board hardware and the software default to 4.7 µF.

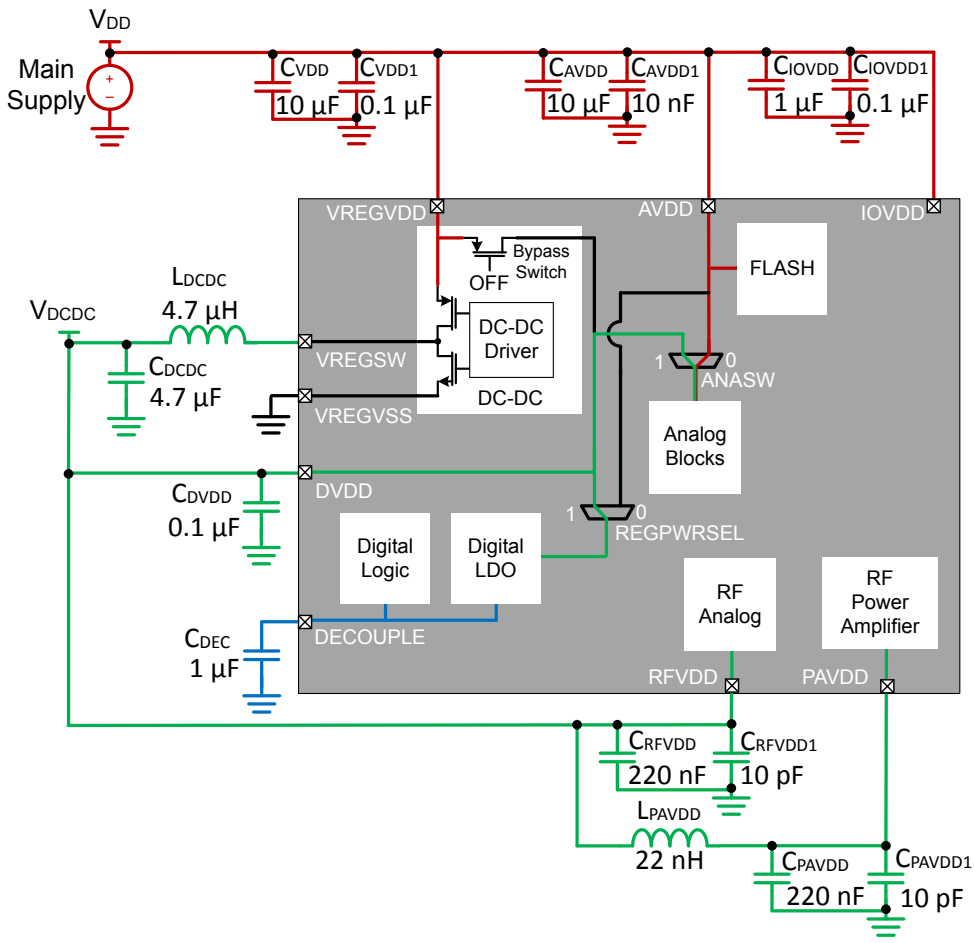


Figure 3.6. EFR32xG12/13/14 Power Configuration 2 — DC-DC Powers DVDD

3.4 Power Configuration 3: DC-DC (High Power RF)

For high-power radio applications (i.e., >13 dBm transmit power), it is necessary to power the radio power amplifier (PAVDD) from the main supply. In this configuration, the DC-DC converter can be used to power the DVDD supply and RFVDD.

In Power Configuration 3:

- The DC-DC Output (V_{DCDC}) is connected to DVDD. DVDD powers the internal Digital LDO which powers the digital circuits.
- DVDD powers the internal Digital LDO (i.e., REGPWRSEL=1 in EFR32xG12/13/14) which powers the digital circuits.
- RFVDD (EFR32 Series 1 only) is also powered from the DC-DC Output. RFVDD powers the radio analog.
- PAVDD (EFR32 Series 1 only) is connected to the main supply through a filter. PAVDD powers the power amplifier used for the radio.
- AVDD is connected to the main supply voltage. The internal analog blocks may be powered from AVDD or DVDD, depending on the ANASW configuration. Flash is always powered from the AVDD pin.
- The IOVDD pin(s) can be connected to either the main supply (as shown below) or to V_{DCDC}, depending on the system I/O requirements. However, on all devices except EFR32xG1, V_{DCDC} will be unpowered (i.e., floating) at startup. On those devices, if IOVDD is powered from the DC-DC converter, then any circuit attached to IOVDD will not be powered until the DC-DC is configured (or the bypass switch is enabled). This can result in a situation where the device cannot be programmed or the bootloader cannot be used (because both of those operations require IOVDD to be valid). Refer to the "IOVDD Connection" section of the Reference Manual EMU chapter for further details and issues that may result when connecting IOVDD to V_{DCDC}.

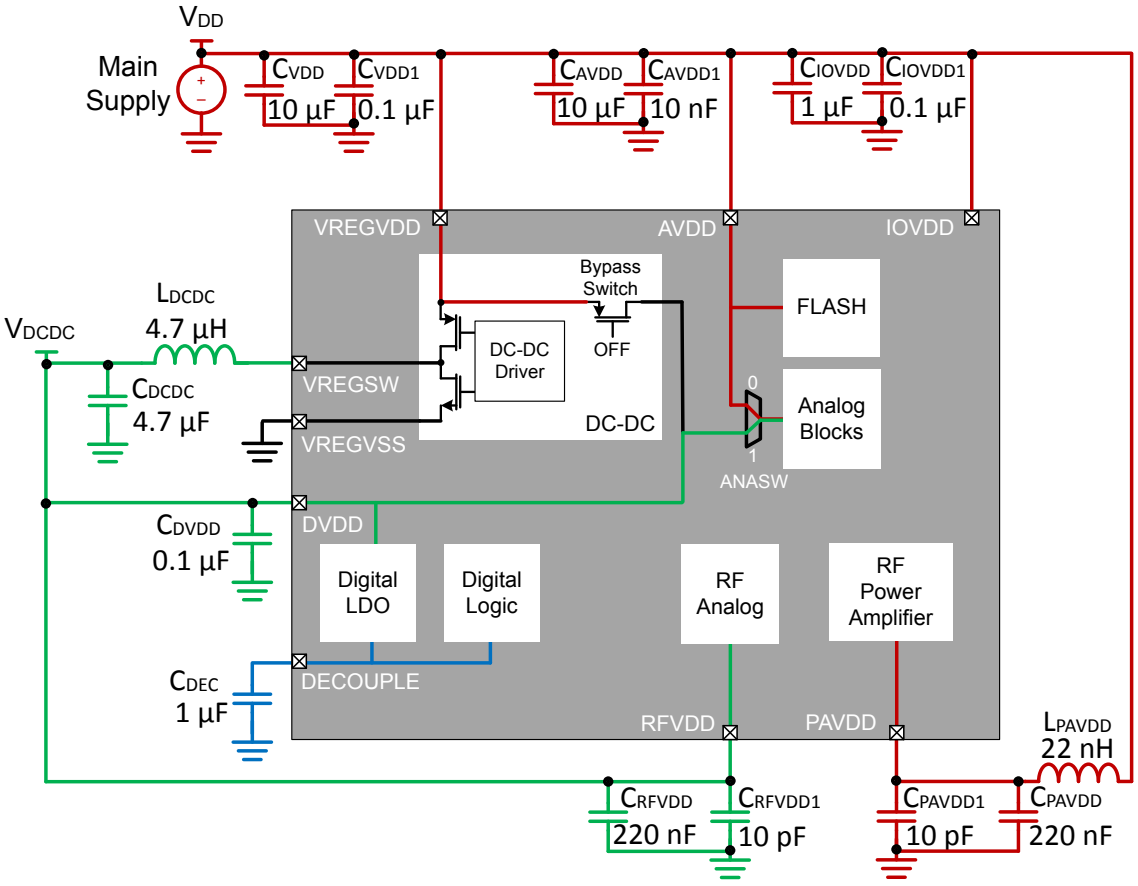


Figure 3.7. EFR32xG1 Power Configuration 3 — DC-DC powers DVDD, Main Supply powers PAVDD

Note: C_{DCDC} was 1.0 µF in some previous revisions of this application note. Although 1.0 µF may still be used, 4.7 µF is now recommended for new designs due to its improved performance under dynamic load conditions and during mode changes. Silicon Labs EFR32xG1 reference radio boards still use 1.0 µF; therefore, the EFR32xG1 software defaults to using 1.0 µF (use of emuDcdcLnCompCtrl_1u0F rather than emuDcdcLnCompCtrl_4u7F). Use of 4.7 µF on EFR32xG1 requires modification of the Low Noise Mode Compensator Control emuDcdcLnCompCtrl value. For EFR32xG12 and later, both the radio reference board hardware and the software default to 4.7 µF.

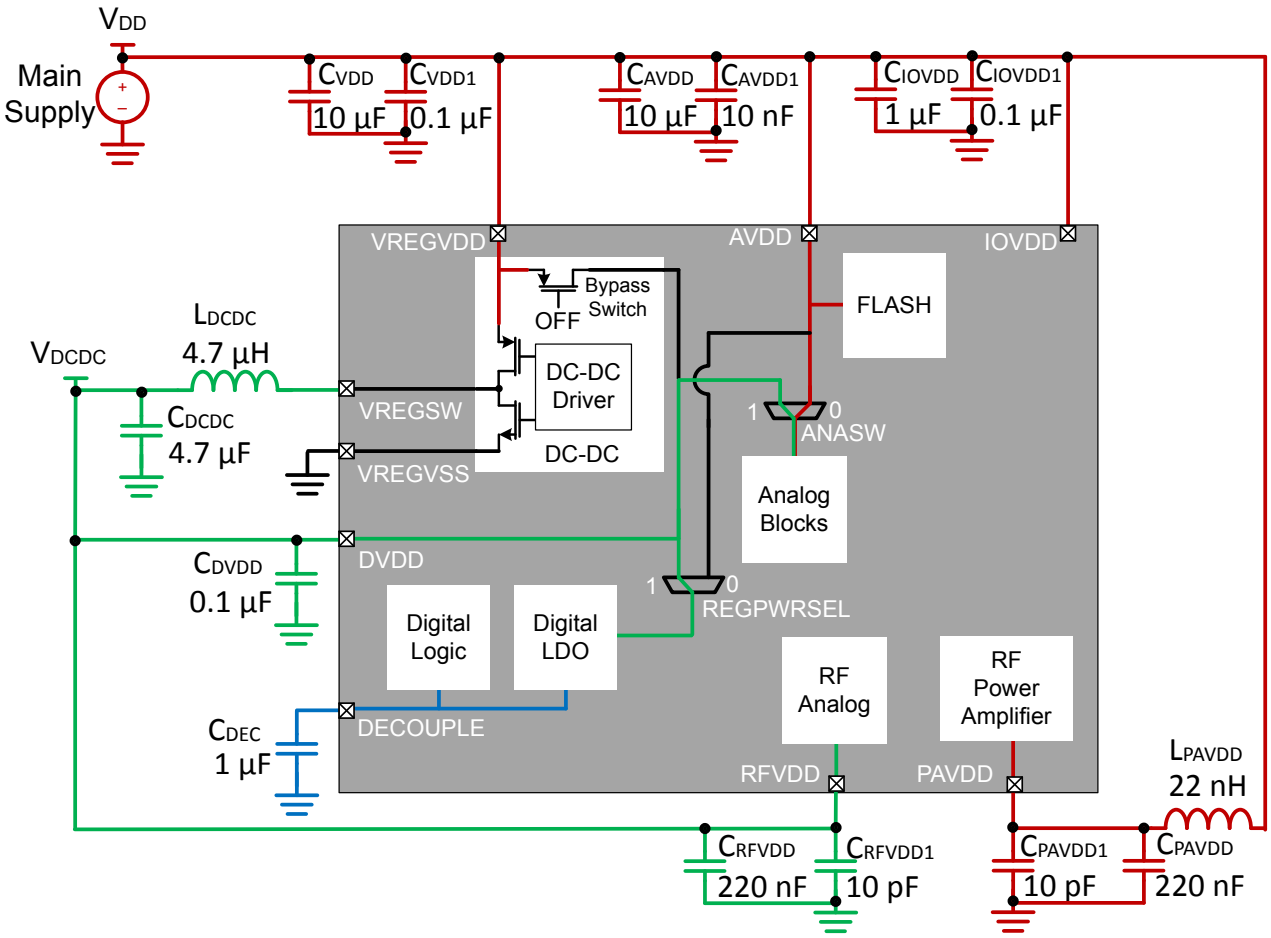


Figure 3.8. EFR32xG12/13/14 Power Configuration 3 — DC-DC powers DVDD, Main Supply powers PAVDD

4. DC-DC Programming Using EMLIB

To simplify use of the DC-DC converter, EMLIB contains functions which will properly configure the DC-DC for efficient operation. It is strongly recommended to take advantage of these functions. These EMLIB functions will also avoid or workaround any errata issues affecting the DC-DC converter. More information on the EMU EMLIB library can be found using the [**Gecko HAL and Driver API Reference Guide**] tile in Simplicity Studio.

4.1 To initialize the DC-DC converter to Low Noise, Low Power, or Bypass mode

1. Declare a structure of type `EMU_DCDCInit_TypeDef`.

```
typedef struct
{
        EMU_PowerConfig_TypeDef powerConfig;
        EMU_DcdcMode_TypeDef dcdcMode;
        uint16_t mVout;
        uint16_t em01LoadCurrent_mA;
        uint16_t em234LoadCurrent_uA;
        uint16_t maxCurrent_mA;
        EMU_DcdcAnaPeripheralPower_TypeDef anaPeripheralPower;
        EMU_DcdcLnReverseCurrentControl_TypeDef reverseCurrentControl;
        EMU_DcdcLnCompCtrl_TypeDef dcdcLnCompCtrl;
} EMU_DCDCInit_TypeDef;
```

Description of parameters:

- `powerConfig`: Should always be set to `emuPowerConfig_DcdcToDvdd`
- `dcdcMode`: May be set to
  - `emuDcdcMode_Bypass` — Enables Bypass mode (i.e., the DC-DC is not switching and the VREGVDD pin is shorted internally to the DVDD pin)
  - `emuDcdcMode_LowNoise` — Configures the DC-DC converter for Low Noise mode
  - `emuDcdcMode_LowPower` (supported on EFM32xG11/12 and EFR32xG12/13/14 devices only)— Configures the DC-DC converter for Low Power mode
- `mVout`: Target output voltage in mV's. To prevent risk of triggering the brown-out protection on the DVDD supply pin, do not set `mVout` lower than "1800" . See the datasheet DC-DC Regulation DC Accuracy specifications to ensure that the sufficient margin is allowed in the actual DC-DC output voltage.
- `em01LoadCurrent_mA`: Highest average load current in mA expected in either EM0 or EM1 modes. Used to optimize the DC-DC settings (e.g., PFETCNT and NFETCNT) for efficiency. The total must be less than "200" and should include both the internal current required by the EFM32 or EFR32 Series 1 device as well as current for any other devices attached to the DC-DC converter output. The default `em01LoadCurrent_mA` value for EFR32 Series 1 is "15" while the default for EFM32 Series 1 is "5".
- `em234LoadCurrent_uA`: Highest average load current in µA expected in EM2, EM3, or EM4. Used to optimize the DC-DC settings (e.g., LPCMPBIAS) for efficiency. The total must be less than "1000" and should include both the EFM32 or EFR32 Series 1 device current, as well as current for any other devices attached to the DC-DC converter output.
- `maxCurrent_mA`: Maximum peak load current in mA for any energy mode. The total must be less than "200", and should include both the internal current required by the EFM32 or EFR32 Series 1 device as well as current for any other devices attached to the DC-DC converter output.
- `anaPeripheralPower`: Changes to the `anaPeripheralPower` selection should be made immediately out of reset, before all clocks are enabled (with the exception of HFRCO and ULFRCO). Once set, it should not be changed. May be set to:
  - `emuDcdcAnaPeripheralPower_AVDD` — Selects the AVDD pin as analog power supply. Typically lower noise but less energy efficient.
  - `emuDcdcAnaPeripheralPower_DCDC` — Selects the DVDD pin (i.e., DC-DC output) as analog power supply. Typically more energy efficient but more noise.
- `reverseCurrentControl`: This parameter uses special encoding, defined as follows:
  - Set to "-1" to configure the DC-DC for Low Noise DCM.
  - Set to a value of 0 or greater to configure the DC-DC for Low Noise forced CCM, where the value of `reverseCurrentControl` is the reverse current limit in mA (see section 5.8 Low-Side (Zero Detector) Current Limiter for more details about the reverse current limit).
- `dcdcLnCompCtrl`: Low Noise Mode Compensator Control. The compensator must be configured based on the external DC-DC output capacitor value (either 1.0 µF or 4.7 µF).
  - `emuDcdcLnCompCtrl_1u0F` — Configure for 1.0 µF DC-DC Output Capacitor.
  - `emuDcdcLnCompCtrl_4u7F` — Configure for 4.7 µF DC-DC Output Capacitor. Use of a 4.7 µF capacitor is recommended for improved dynamic response

2. Call `EMU_DCDCInit()` passing the `EMU_DCDCInit_TypeDef` structure, created in step 1, as an argument. Alternately, there is a default `EMU_DCDCInit_TypeDef` structure provided that can be used. See ● Initialization Programming Examples on page 24 section below for examplese using the default structure. At the completion of this function call, the DC-DC should be in regulation. This function does the following:
   - Configures the PWRCFG register.
   - Loads the production calibration register values into the respective registers.
   - Configures the powertrain switches for optimal efficiency based on the `em01LoadCurrent_mA` and `em234LoadCurrent_uA` values.
   - Configures the High-Side Current Limits for both LN and LP modes (i.e., LNCLIMILIMSEL and LPCLIMILIMSEL).
   - Configures the DC-DC output target voltage, interpolating, if necessary, between the production-calibrated reference voltage levels.
   - Configures the analog power switch to either AVDD or DVDD, based on the `anaPeripheralPower` value. Once set, the analog power setting should not be changed.
   - Sets the DCDCMode bitfield to select either Low Noise (which initiates regulation) or Bypass.

Initialization Programming Examples

Initialization example using the DC-DC default configuration:

```
EMU_DCDCInit_TypeDef dcdcInit = EMU_DCDCINIT_DEFAULT;
EMU_DCDCInit(&dcdcInit);
```

Initialization example starting from the DC-DC default configuration, with one change to use AVDD as the analog supply:

```
EMU_DCDCInit_TypeDef dcdcInit = EMU_DCDCINIT_DEFAULT;
dcdcInit.anaPeripheralPower = emuDcdcAnaPeripheralPower_AVDD;
EMU_DCDCInit(&dcdcInit);
```

4.2 To initialize the DC-DC converter to OFF

To power off the DC-DC and set the internal Bypass switch to Off, call the `EMU_DCDCPowerOff()` function. Call this function only when using Power Configuration 1 (see section 3.2 Power Configuration 1: No DC-DC).

Note: Before calling this function, it is critical to ensure that the hardware provides an external power supply to DVDD. The internal bypass switch cannot be used when the DC-DC is powered off. As a result, if the DC-DC is powered off without DVDD being powered externally, there is a risk that the device could be put into an unrecoverable state.

4.3 To enter EM2, EM3, or EM4 low energy modes from Low Noise mode

To enter the low energy modes, call `EMU_EnterEM2()`, `EMU_EnterEM3()`, or `EMU_EnterEM4()`. The DC-DC converter automatically transitions to Low Power mode while the core is in low energy mode.

Note: The ARM Cortex™ SLEEPONEXIT functionality is not currently compatible with the EMLIB low energy mode functions. The SLEEPONEXIT feature allows the MCU to wakeup on an interrupt, service an interrupt routine, then immediately (and autonomously) go back to sleep. The SLEEPONEXIT interrupt routines are typically written only for the functional requirements of the module interrupt (e.g., LEUART) with no knowledge about the DC-DC or other power management systems. Because the integrated DC-DC converter requires firmware reprogramming before exiting or entering the low energy modes, it is not straightforward to use it with SLEEPONEXIT.

4.4 To optimize the powertrain switches in Low Noise mode

Once the DC-DC is configured and running, firmware may call `EMU_DCDCOptimizeSlice(loadCurrent)` to update the NFETCNT and PFETCNT settings for optimal efficiency, where the `loadCurrent` argument is the highest average expected EM0/EM1 load current in mA.

This function might be called whenever there is a substantial expected change in load current (e.g., between low-current radio receive and high-current radio transmit operations).

4.5 To enter Bypass mode from Low Noise or Low Power mode

After the DC-DC has already been initialized to Low Noise or Low Power mode, as described in section 4.1 To initialize the DC-DC converter to Low Noise, Low Power, or Bypass mode, firmware can call `EMU_DCDCModeSet(emuDcdcMode_Bypass)` to enter Bypass mode.

Note: The EMLIB routines do not enable the Bypass Current Limit, because of difficulties around determining when to subsequently disable it. See 2.2 Bypass Mode for more details.

Firmware may switch to Bypass mode for several reasons:

1. The VREGVDD input supply voltage is nearing the minimum input voltage for the DC-DC (see section 2.7 DC-DC Maximum Output Current vs. Minimum Input Voltage).
2. The DC-DC output load current has decreased to a point (e.g., ~2.5 mA < I_{LOAD} < ~ 18 mA) that the DC-DC should switch from CCM to DCM to improve efficiency (see section 4.7 To switch from Low Noise CCM mode to Low Noise DCM mode). Switching to Bypass mode is an intermediate step in the CCM-to-DCM transition.
3. The DC-DC output load current has decreased to a point (e.g., I_{LOAD} < ~2.5 mA) that the DC-DC is now operating below its efficiency threshold (see section 2.8 DC-DC Efficiency Threshold).

4.6 To re-enter Low Noise or Low Power mode from Bypass mode

If DC-DC has already been initialized but is currently in Bypass mode, firmware can call `EMU_DCDCModeSet()` to resume DC-DC operation, as described below:

- On all devices, if originally initialized in Low Noise mode, firmware can call `EMU_DCDCModeSet(emuDcdcMode_LowNoise)` to re-enter Low Noise mode.
- On EFM32xG11/12 and EFR32xG12/13/14 devices, if originally initialized in Low Power mode, firmware can call `EMU_DCDCModeSet(emuDcdcMode_LowPower)` to re-enter Low Power mode.

Note: The `EMU_DCDCModeSet()` command should only be used after the DC-DC has already been initialized, as described in section 4.1 To initialize the DC-DC converter to Low Noise, Low Power, or Bypass mode.

4.7 To switch from Low Noise CCM mode to Low Noise DCM mode

When the DC-DC output load current is less than ~18 mA, the DC-DC can switch from CCM to DCM to improve efficiency (see figure Figure 2.1 3 MHz DCM Light Drive/ 7 MHz CCM Light/Medium/Heavy Drive Efficiency vs Load Current on page 8).

There is no method to directly switch the DC-DC's configuration between CCM and DCM (or vice-versa). If the DC-DC converter is operating in CCM, firmware must first configure the DC-DC to Bypass mode before it can be configured for DCM. Note that this may result in a large and undesirable transient voltage on the DC-DC output, as the DC-DC output will be momentarily shorted to the VREGVDD input supply.

To switch between CCM and DCM (or vice-versa), call `EMU_DCDCConductionModeSet()` , passing either `emuDcdcConductionMode_ContinuousLN` or `emuDcdcConductionMode_DiscontinuousLN` as an argument. Note that this fuction will momentarilly enable Bypass mode.

5. DC-DC Configuration Reference

Note: EMLIB contains functions which properly configure the DC-DC for an efficient operation. It is strongly recommended to take advantage of these functions. These EMLIB functions also avoid or work around any errata issues affecting this block.

5.1 DC-DC Module Register Locks

The DC-DC module has several locks that can be used to prevent accidental changes to the EMU and DC-DC configuration registers. Note that these locks are unlocked by default and are not used by any of the EMLIB DC-DC configuration functions.

1. EMU_LOCK — All non-DC-DC, EMU, registers may be unlocked by writing 0xADE8 to LOCKKEY or locked by writing any other value to LOCKKEY.
2. EMU_PWRLOCK — All DC-DC registers may be unlocked by writing 0xADE8 to LOCKKEY or locked by writing any other value to LOCKKEY.

5.2 DC-DC Mode Selection

The DC-DC Mode has multiple mode configurations depending on which energy mode the device is in. Note that the below details are provided for reference only because the DC-DC Mode is configured automatically for all energy modes in the EMLIB DC-DC functions.

In EM0/EM1, the DC-DC mode may be configured by the DCDCMODE bitfield in the EMU_DCDCCTRL register to one of the following settings:

- BYPASS — Bypass switch is ON (i.e., VREGVDD is shorted internally to the DVDD pin).
- LOWNOISE — Bypass switch is OFF. The Low Noise controller is enabled.
- LOWPOWER — Bypass switch is OFF. The Low Power controller is enabled. Should only be used for maximum load current below 10 mA.
- OFF — Bypass switch is OFF. The DC-DC converter is disabled. This mode should only be used in Power Configuration 1 (see section 3.2 Power Configuration 1: No DC-DC). Hardware MUST supply DVDD externally if this configuration is selected. Selecting this mode without an external connection supplying DVDD may put the device into an unrecoverable state.

In EM2/EM3, the DC-DC mode may be configured by the DCDCMODEEM23 bitfield in the EMU_DCDCCTRL register to one of the following settings:

- EM23SW — DC-DC Mode is set according to the DCDCMODE configuration.
- EM23LOWPOWER — DC-DC Mode is set to Low Power.

In EM4, the DC-DC mode may be configured by the DCDCMODEEM4 bitfield in the EMU_DCDCCTRL register to one of the following settings:

- EM4SW — DC-DC Mode is set according to the DCDCMODE configuration.
- EM4LOWPOWER — DC-DC Mode is set to Low Power.

5.3 DC-DC Output Voltage Configuration

Note that the below details are provided for reference only because the output voltage settings are configured automatically in the EMLIB DC-DC functions.

In Low Noise Mode, the output voltage is controlled by the LNVREF and LNATT bitfields in the EMU_DCDCLNVCTRL register. LNVREF controls the voltage reference level and LNATT controls the attenuation . For 1.8 V output and greater, LNATT should always be set to 1. During production, each device has LNVREF calibration values stored in internal flash that correspond to a DC-DC output of 1.8 V and 3.0 V. For output voltages between 1.8 V and 3.0 V, the firmware should interpolate between calibration values.

In Low Power Mode, the output voltage is controlled by the LPVREF and LPATT bitfields in the EMU_DCDCLPVCTRL register. LPVREF controls the voltage reference level and LPATT controls the attenuation . For 1.8 V output and greater, LPATT should always be set to 1. During production, each device has multiple LPVREF calibration values (one per LPCMPBIAS setting) stored in internal flash that correspond to a DC-DC output of 1.8 V and 3.0 V. For output voltages between 1.8 V and 3.0 V, the firmware should interpolate between the calibration values corresponding to the desired LPCMPBIAS configuration.

5.4 Low Power Mode Duty Cycling

Firmware should set LPREFDUTYEN in EMU_DCDCLPCTRL to enable Duty Cycling for optimal efficiency in Low Power mode. Note that this configuration is handled automatically in the EMLIB DC-DC functions.

5.5 Low Power Mode Hysteresis

The Low Power Hysteresis configuration registers vary depending on which device is used.

For EFM32xG1 and EFR32xG1 devices:

- The LPCMPHYSSEL bitfield in EMU_DCDCLPCTRL configures the Low Power hysteresis in EM2, EM3, and EM4H.

For EFM32xG11/12 and EFR32xG12/13/14 devices:

- The LPCMPHYSSEL234H bitfield in EMU_DCDCLPCTRL configures the Low Power hysteresis in EM2, EM3, and EM4H.
- The LPCMPHYSSELEM01 bitfield in EMU_DCDCLPEM01CFG configures the Low Power hysteresis in EM0 and EM1.

All devices, however, have four hysteresis calibration values (one for each LPCMPBIAS setting) stored in internal flash during production test, corresponding to ~100 mV of hysteresis . The calibration values corresponding to the desired LPCMPBIAS configuration should be written to LPCMPHYSSEL,LPCMPHYSSEL234H, and/or LPCMPHYSSELEM01 during initialization. Note that this initialization is handled automatically in the EMLIB DC-DC functions.

5.6 Bypass Current Limiter

The DC-DC Bypass Current Limit limits the maximum current drawn from the main supply in Bypass mode. This current limit is enabled by setting the BYPLIMEN bit in the EMU_DCDCCLIMCTRL register. The limit value may be adjusted between 20 mA and 320 mA using the BYPLIMSEL bitfield in the EMU_DCDCMISCCTRL register.

The Bypass Current Limiter is beneficial when enabling the Bypass switch would cause the DVDD pin to experience a large voltage change. For example, if the DC-DC converter is enabled and regulating at 1.8 V, and then the Bypass switch is enabled while the main supply is at 3.8 V, the voltage at the DVDD pin (and across the DCDC output capacitor) will change from 1.8 V to 3.8 V. Because the Bypass switch on-resistance may be typically around 1.2 Ω, the main supply can see a current spike as large as 1.6 A when the Bypass switch is enabled (i.e., (3.8 V - 1.8 V) / 1.2 Ω = 1.6 A), which may cause the input supply to brownout. To avoid this, the Bypass Current Limiter can be enabled prior to enabling the Bypass switch.

Note that the device will see an additional ~10 uA of current draw when both the Bypass Current Limiter and Bypass Mode are enabled. Applications should therefore disable the Bypass Current Limiter (i.e., BYPLIMEN = 0) after the DVDD voltage has reached the main supply voltage in Bypass Mode.

By default, the EMLIB functions to enable Bypass Mode do **not** ever enable the Bypass Current Limiter, to avoid inadvertently causing the additional ~10 uA current draw.

5.7 High-Side Current Limiter

The DCDC High-Side Current Limiter includes two different programmable current limits (LNCLIMILIMSEL and LPCLIMILIMSEL) in the EMU_DCDCMISCCTRL register. An overlimit condition generates a PFETOVERCURRENTLIMIT interrupt in the EMU_IF register.

Depending on the DC-DC mode, these programmable current limits may serve different functions:

1. In LP mode, LPCLIMILIMSEL is used to adjust the DC-DC pumping current to optimize efficiency.
2. In LN modes, LNCLIMILIMSEL prevents the DC-DC from building up substantial current which would burn out the DC-DC switch in the unlikely event the DC-DC output or switching node were accidentally connected to ground or to a lower voltage power supply.
3. In LN modes, LNCLIMILIMSEL limits the magnitude of current the DC-DC will draw. Some batteries have a high internal impedance and the battery output voltage may droop severely under high transient current load.

Low Power

In LP mode, the current limiter is used to adjust the average pumping current to optimize the power efficiency. In LP mode, a constant configuration of PFETCNT=7 and LPCLIMILIMSEL=1 is recommended, which corresponds to a nominal 80 mA peak current.

Note: In LP mode, PFETCNT configuration is only required for EFM32xG1 and EFR32xG1 devices - see ● PFETCNT / NFETCNT Bitfields on page 4 for more details

Firmware may safely ignore the PFETOVERCURRENTLIMIT flag in the EMU_IF register in LP mode because this interrupt will trigger during normal LP operation.

Low Noise CCM/DCM

In LN modes, the High-Side Current Limiter is used to limit the maximum current drawn from the main supply. For example, if the main supply is a battery with a non-negligible output impedance, the current should be limited to prevent voltage droops at the DC-DC's input pin (VREGVDD). Otherwise, the High-Side Current Limiter is configured to protect the DC-DC powertrain switch from damage due to excessive current.

The following equation may be used to determine the appropriate LNCLIMILSEL setting:

$$LNCLIMILIMSEL = \frac{(I_{MAX} + 40mA) \times 1.5}{5mA \times (PFETCNT + 1)} - 1$$

Where:

- I_{MAX} is the lower of a) the maximum current the main supply can provide or b) 200 mA.
- 40 mA is an empirical value that represents the expected output current ripple with some margin.
- The 1.5 factor accounts for errors from input and output voltage variation, switching frequency variation, inductance variation, detection error, and so on.

For example, when PFETCNT=3, and I_{MAX}=20 mA, setting LNCLIMILIMSEL=3 equates to a peak current limit of 80 mA. Note that the actual expected load current should be lower than the current limit setting.

When the High-Side Current Limiter is triggered, it turns off the power train PFET and turns on the powertrain NFET earlier, which may result in sub-harmonics. Severe sub-harmonics could reduce the maximum average current. In normal Low Noise mode operation, the High-Side Current Limiter is not expected to trigger assuming it is configured to a level higher than necessary, with margin. However, significant changes in load current (e.g., entering LN mode from LP or bypass modes), may cause the current limiter to trigger occasionally even in normal operation. When the high side current limiter is triggered, the PFETOVERCURRENTLIMIT flag in the EMU_IF register is set.

5.8 Low-Side (Zero Detector) Current Limiter

The DC-DC Low-Side Current Limiter is also referred to as the Zero Detector, which serves multiple purposes depending on the DC-DC configuration. The current limit value is programmed by the ZDETILIMSEL bitfield in the EMU_DCDCZDETCTRL register. An overlimit condition generates an NFETOVERCURRENTLIMIT interrupt in the EMU_IF register.

Low Power

In LP mode, the Zero Detector is used to detect the end of each pumping process to turn off the powertrain NFET, so that all energy in the inductor is delivered to the load capacitor.

Firmware may safely ignore the NFETOVERCURRENTLIMIT flag in the EMU_IF register in LP mode.

Low Noise DCM

In LN DCM mode, the Zero Detector turns the powertrain NFET off when it detects the inductor current has dropped to zero.

Firmware may safely ignore the NFETOVERCURRENTLIMIT flag in the EMU_IF register in LN DCM.

Low Noise CCM

In LN CCM, the Zero Detector is reconfigured as a reverse current limiter to prevent current flowing back into the battery or main supply. The reverse current limit is set by the ZDETILIMSEL bitfield in EMU_DCDCZDETCTRL.

If the battery or main supply can safely tolerate reverse current, the reverse current limiter is configured to its maximum value (i.e., ZDETILIMSEL=7) to protect the DC-DC powertrain switch from damage due to excessive current. For example, in the unlikely event the DC-DC supply output were accidentally shorted to another higher voltage power supply, the DC-DC may sink large amounts of current in an attempt to regulate to its target.

The recommended ZDETILIMSEL setting may be determined by the following equation:

$$ZDETILIMSEL = \frac{(I_{RMAX} + 40mA) \times 1.5}{2.5mA \times (NFETCNT + 1)}$$

Where:

- I_{RMAX} is the lower of a) the maximum reverse current the main supply can tolerate or b) 280 mA.
- 40 mA is an empirical value that represents the expected output current ripple with some margin
- The 1.5 factor accounts for errors from input and output voltage variation, switching frequency variation, inductance variation, detection error, and so on..

For example, if NFETCNT=3 and I_{R_MAX} = 0 mA, ZDETILIMSEL=6. Note, the reverse current limit isn't very accurate and may have a >10 mA error.
In a normal Low Noise CCM operation, the Zero Detector interrupt is not expected to trigger. However, significant changes in load current (e.g., entering LN mode from LP or bypass modes) may cause the current limiter to trigger occasionally even in normal operation. When the Zero Detector is triggered, the NFETOVERCURRENTLIMIT flag in the EMU_IF register is set. If firmware sees this flag triggering frequently in LN CCM, this likely indicates that the ZDETLIMSEL threshold is set too low and should be raised. Otherwise, DC-DC efficiency may be impacted.

6. DC-DC Components Selection Guide

6.1 DC-DC Output Capacitor

The Murata GRM188R71A105KA61D 1.0 µF capacitor was used for all of the DC-DC validation and characterization testing for EFM32xG1 and EFR32xG1 devices. For all other devices (e.g., EFM32xG11/12 and EFR32xG12/13/14), the Samsung CL10B475KQ8NQNC 4.7µF capacitor was used. However, a 4.7 µF capacitor is recommended for new EFM32xG1 and EFR32xG1 designs due to its improved performance under dynamic load conditions and mode changes. Note that some firmware configurations differ based on the size of the DC-DC output capacitor - specifically, the `dcdcLnCompCtrl` parameter passed to `EMU_DCDCInit()` changes depending on the output capacitor value (see section 4.1 To initialize the DC-DC converter to Low Noise, Low Power, or Bypass mode for more details).

The output capacitor should have a temperature range reflecting the environment in which the application will be used. For example, a suitable choice might be X5R ceramic capacitors with a change in capacitance of ±15% over the temperature range -55 °C – +85°C (standard temperature range devices) or -55 °C – +125°C (extended temperature range devices).

The system designer should pay particular attention to the characteristics of the output capacitor over temperature and bias voltage. Some capacitors (particularly those in smaller packages) can experience a dramatic reduction in capacitance value as the temperature or bias voltage increases. A change pushing the DC-DC output capacitance outside the datasheet specified limits may result in output instability.

Table 6.1. Recommended DC-DC Output Capacitor

Manufacturer	Part Number	Value (µF)	Voltage Rating (V)	Dielectric	Operating Temperature (°C)	Package
Murata	GRM188R71A105KA61D	1±10%	10	X7R	-55 to +125	0603/1608
Samsung	CL10B475KQ8NQNC	4.7±10%	6.3	X7R	-55 to +125	0603/1608

6.2 DC-DC Inductor

The Murata LQH3NPN4R7MM0L or LQH3NPN4R7MMEL inductors are recommended as they were used for all of the DC-DC validation and characterization testing. The Murata LQH3NPN4R7MM0L part is being discontinued, and LQH3NPN4R7MMEL is the vendor's replacement part number. The LQH3NPN4R7MMEL device has been qualified to have similar characteristics and performance as the LQH3NPN4R7MM0L device.

Other inductors listed may be suitable as well, but only LN CCM efficiency was measured.

Note: Two of the inductors listed (Murata LQM18FN4R7M00D and LQM21FN4R7M80L) have a very low saturation current (e.g., 120 mA or lower). These typically cheaper inductors may be suitable for some very light-loaded applications but require extra attention to ensure the inductor does not saturate - an inductor at or near saturation may have poor transient response. Therefore, applications using these (or similar) inductors with a low saturation current must use appropriate settings for the powertrain current limiters to limit the inductor peak current and ensure the inductor does not saturate.

The maximum DC-DC output current (I_{LOAD_MAX}) for a given inductor saturation current (I_{SAT}) can be calculated using the following equation: $$I_{LOAD\_MAX} = I_{SAT} - \frac{V_{DCDC} * \left(1 - \frac{V_{DCDC}}{VREGVDD}\right)}{2 * L * f_{SW}}$$

In Figure 6.1 Low Saturation Current Inductor: Maximum DC-DC Output Current vs Input Voltage (CCM mode, L_{DCDC}=4.7 µH, V_{DCDC}=1.8 V) on page 31, the calculated maximum DC-DC Output Current is shown for two different low saturation current inductors (I_{SAT}=80 and 120 mA) for two switching frequencies (f_{SW}=7 MHz [Radio On] and 3 MHz [Radio Off]). Note that a 15% derating has been applied to the data plotted below to account for inductor tolerance.

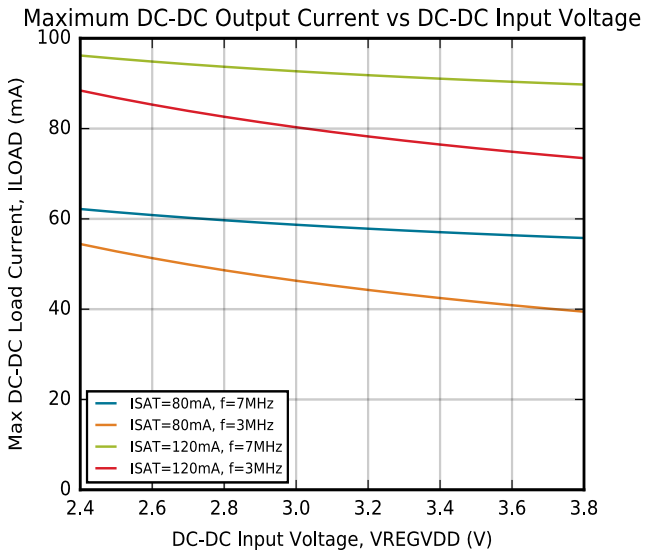
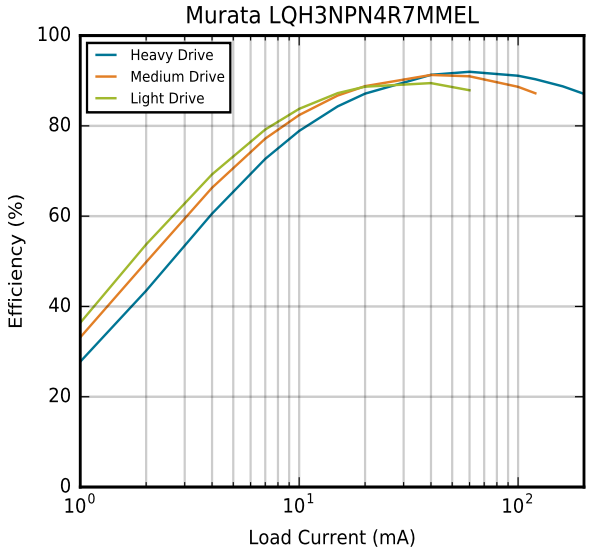


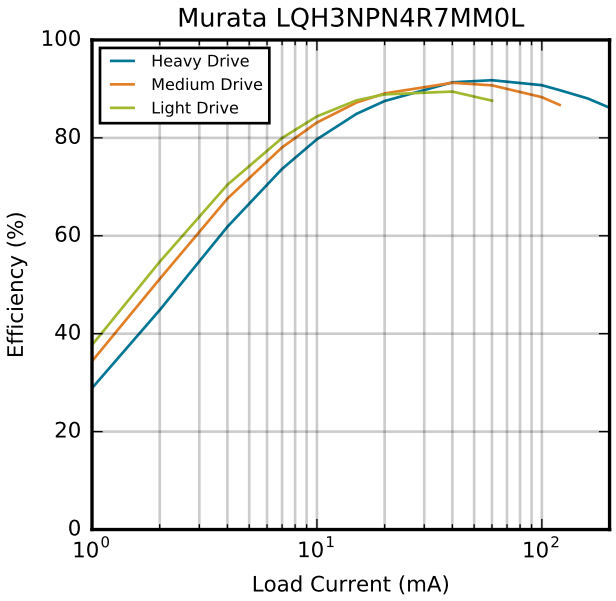
Figure 6.1. Low Saturation Current Inductor: Maximum DC-DC Output Current vs Input Voltage (CCM mode, L_{DCDC}=4.7 µH, V_{DCDC}=1.8 V)

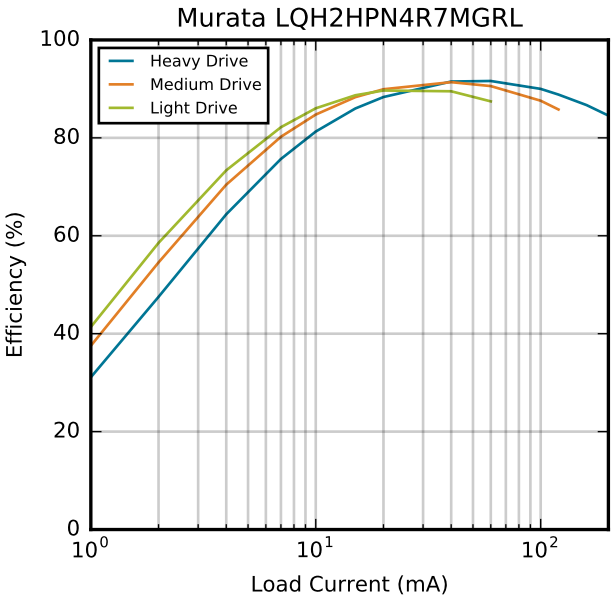
Table 6.2. DC-DC Inductors

Manufacturer	Part Number	Value (µH)	$I_{saturation}$ (mA)	DCR (Ω)	Operating Temperature (°C)	Package
Murata	LQH3NPN4R7MMEL	4.7±20%	1300	0.1±20%	-40 to +125	1212/3030
Murata	LQH3NPN4R7MM0L	4.7±20%	880	0.13±20%	-40 to +125	1212/3030
Murata	LQH2HPN4R7MGRL	4.7±20%	1090	0.30±20%	-40 to +105	1008/2520
Murata	LQM21FN4R7M80L	4.7±20%	120	0.18±30%	-55 to +125	0805/2012
Murata	LQM18FN4R7M00D	4.7±20%	80	0.60±30%	-55 to +125	0603/1608

Manufacturer	Part Number	Value (µH)	$I_{saturation}$ (mA)	DCR (Ω)	Operating Temperature (°C)	Package
Murata	LQH2HPN4R7MGRL	4.7±20%	1090	0.30±20%	-40 to +105	1008/2520
Murata	LQM21PN4R7MGRD	4.7±20%	800	0.23±20%	-55 to +125	0805/2012
Murata	LQM18PN4R7MFRL	4.7±20%	Unspecified	0.44±25%	-40 to +85	0603/1608







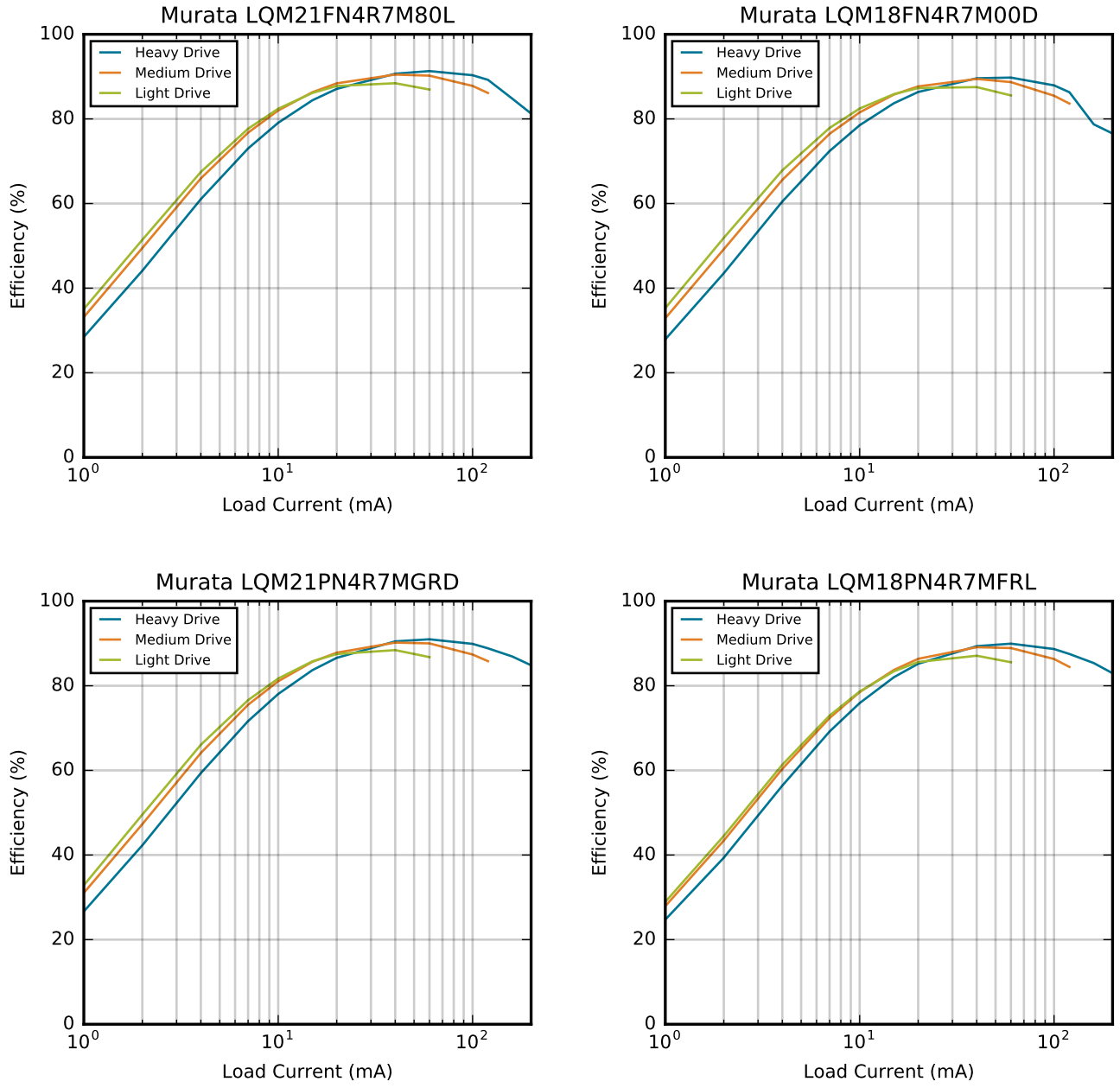


Figure 6.2. Inductor Efficiency Curves for CCM mode, L_{DCDC}=4.7 µH, VREGVDD=3.3 V, V_{DCDC}=1.8 V, F_{DCDC}=7 MHz

7. DC-DC Layout Considerations

Because the DC-DC converter is a high-frequency, high-current module, some special layout considerations are required for optimal operation:

- The following connections should be made on the PCB using minimum trace length and resistance
- - Between the VREGSW pin and the L_{DCDC} inductor
  - Between the L_{DCDC} inductor and the C_{DCDC} capacitor
  - Between the C_{DCDC} capacitor and the DVDD pin
  - Between the Main Supply and the VREGVDD pin
  - Between the VREGVSS pin and ground
- The L_{DCDC} inductor should be placed far away from any noise-sensitive circuitry (e.g., a radio antenna). The inductor should ideally be on the opposite side of the PCB, so that there is a solid ground plane shielding the noisy inductor from the sensitive circuitry.
- For more detailed radio-specific layout guidelines, see *AN928: EFR32 Layout Design Guide* .

8. DC-DC Software Examples

8.1 Software Example 1 — Bypass

This example enables the bypass switch, which shorts the VREGVDD pin to the DVDD pin internally within the DC-DC module. This mode is functionally compatible with the EFM32 Series 1 power configuration.

8.2 Software Example 2 — DC-DC to DVDD 1.8V

This example enables the DC-DC converter and sets the nominal output voltage to 1.8 V. This example requires an external inductor and capacitor (see section 3.3 Power Configuration 2: DC-DC).

The DC-DC is configured for Low Noise mode in EM0/1 and Low Power mode in EM2/EM3/EM4H. The example assumes the following load currents:

- EM0/1 load current — 5 mA
- EM2/EM3/EM4H load current — 10 uA
- Max Current — 160 mA

Analog peripherals are powered from the AVDD supply.

9. Revision History

9.1 Revision 0.8

2018-14-10

Corrected Efficiency Threshold Table 2.4V row. Threshold changed from 69.2% to 75%, and DCM /CCM currents updated accordingly.

Clarified PFETCNT and NFETCNT bitfield operation differences between devices in ● PFETCNT / NFETCNT Bitfields on page 4

9.2 Revision 0.7

2017-10-27

Updated 6.2 DC-DC Inductor section to add equations and plots to determine maximum output current for low saturation current inductors

Updated Table 2.2 Analog Peripheral Power Configuration on page 6 table to clarify that using DVDD as the analog supply voltage may limit your maximum usable analog input range.

Updated 3.3 Power Configuration 2: DC-DC and 3.4 Power Configuration 3: DC-DC (High Power RF) sections to clarify that powering IOVDD from the DC-DC converter output may have undesirable consequences.

9.3 Revision 0.6

2017-7-15

Updated 6.2 DC-DC Inductor section with Murata LQH3NPN4R7MMEL, the replacement inductor for the End-Of-Life'd Murata LQH3NPN4R7MM0L

Added details on use of the Bypass Current Limit to the 2.2 Bypass Mode section

Clarified that the EMLIB functions do not automatically enable the Bypass Current Limit in 4.5 To enter Bypass mode from Low Noise or Low Power mode section

Added additional clarification around the change from 1 µF to 4.7 µF capacitors in 6.1 DC-DC Output Capacitor and Figure 3.5 EFR32xG1 Power Configuration 2 — DC-DC Powers DVDD on page 18 sections

Added some example initialization code examples to 4.1 To initialize the DC-DC converter to Low Noise, Low Power, or Bypass mode section

9.4 Revision 0.5

2017-1-25

Added support for EFM32xG11/12 and EFR32xG12/13/14 devices.

Changed DC-DC output capacitor to 4.7 uF for all diagrams.

Added some clarification that the DC-DC can only be used in EM4H, and not in EM4S

Added summary of EMU and DC-DC differences between EFM32xG11/12 and EFR32xG12/13/14 devices and EFM32xG1 and EFR32xG1 devices: 2.1 Major EMU and DC-DC Differences

Added EFM32xG1 and EFR32xG1 block diagrams in 3.3 Power Configuration 2: DC-DC and 3.4 Power Configuration 3: DC-DC (High Power RF) sections.

Updated procedure in 4.7 To switch from Low Noise CCM mode to Low Noise DCM mode section to use the EMLIB `EMU_DCDCConductionModeSet()` function.

Updated description in 5.5 Low Power Mode Hysteresis section for EFM32xG11/12 and EFR32xG12/13/14

9.5 Revision 0.4

2016-10-25

Added 2.6 LN Efficiency Optimization vs. Load Current and DC-DC Mode section.

Added description of dcdcLnCompCtrl parameter in the DC-DC Programming Using emlib section.

Added 4.7 uF capacitor recommendation to the 6.1 DC-DC Output Capacitor section.

Added warnings about use of low saturation current inductors in the 6.2 DC-DC Inductor section.

9.6 Revision 0.3

2016-6-15

Overhaul of all Power Configuration diagrams

Added "Efficiency Threshold" section

Added "Maximum Output Current" section

Added "Programming using EMLIB" section

Added "Recommend Components" section

Added "Layout Considerations" section

Added "Configuration Reference" section

9.7 Revision 0.2

2015-11-13

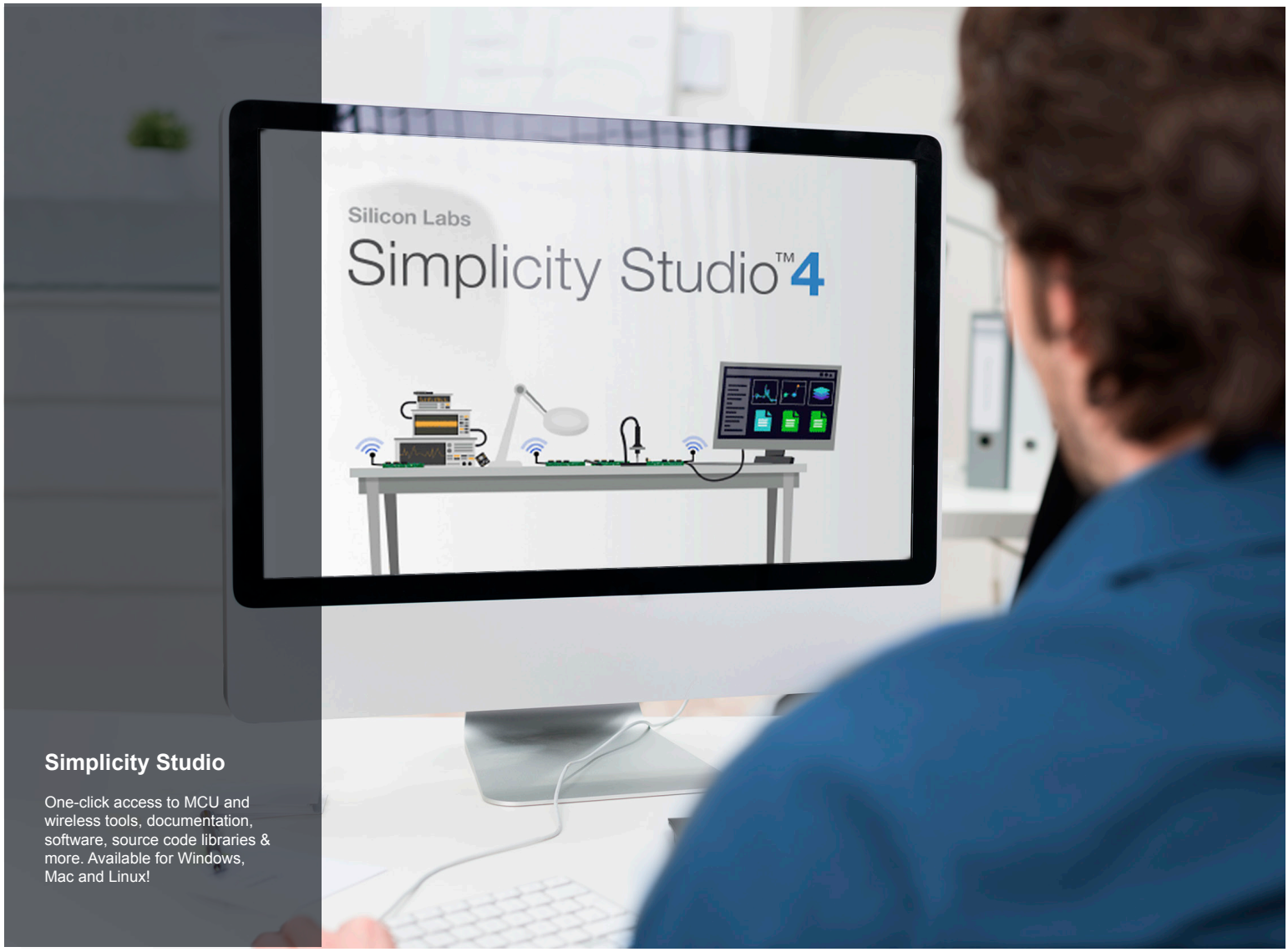
Added support for EFR32 Series 1 portfolio

Updated recommendations for NFETCNT in EM2/EM3/EM4H LP mode in the Load Current Selection table.

9.8 Revision 0.1

2015-11-6

Initial revision.



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