
WIRELESS MBUS IMPLEMENTATION USING EZRADIOPRO™ DEVICES

1. Introduction

This application note describes how to create a wireless MBUS compliant device using Silicon Labs' Si443x EZRadioPRO RF transceiver and C8051F9xx microcontrollers. Using the Si443x a cost effective, high-performance MBUS device can be achieved.

The Application note does not cover the duty cycle and other timing requirements of the standard, focusing on the RF related requirements for a wireless MBUS application.

2. Wireless MBUS Standard

The Wireless MBUS standard (EN 13757-4:2005 (E)) specifies two kinds of devices: "Meters" and "Others" (like mobile readout devices, data collectors, etc.). The standard also defines several types of communication between devices:

- Mode S ("Stationary mode"):
 - Mode S1: unidirectional link from the Meter to the Other device
 - Mode S1m: unidirectional link from the Meter to the Other device
 - Mode S2: bidirectional communication between the Meter and Other device
- Mode T ("Frequent transmit mode"):
 - Mode T1: unidirectional link from the Meter to the Other device
 - Mode T2: bidirectional link from the Meter to the Other device
- Mode R ("Frequent receive mode"): special, multi-channel receiving mode.
 - Mode R2: bidirectional link from Meter to Other device

The following tables list the radio requirements for the transmitter and receiver for Mode S and Mode T devices.

AN361

2.1. Radio Link Requirements of Mode S

Table 1. Transmitter Requirements of Mode S

Characteristic	Mode	Sym	Min	Typ	Max	Unit
Center Frequency ¹	S1, S1m		868.25	868.3	868.35	MHz
Center Frequency ²	S2		868.278	868.3	868.322	MHz
Frequency Deviation			±40	±50	±80	kHz
Chip Rate	f _{chip}		—	32.768	—	kcps
Chip Rate Tolerance			—	—	±1.5	%
Digital Bit Jitter			—	—	±3	µs
Data Rate (Manchester)			—	f _{chip} × 1/2	—	bps
Preamble Length, including Synchronization Word	S2, S1m		—	48	—	chips
Preamble Length, including Synchronization Word ³	S1		—	576	—	chips
Postamble (trailer) Length			2	—	8	chips
Response Delay	t _{RO}		3	—	50	ms
Notes:						
1. 60 ppm						
2. 25 ppm						
3. Optional for S2						

Table 2. Receiver Requirements of Mode S

Characteristic	Mode	Sym	Min	Typ	Max	Unit
Sensitivity (BER < 10 ⁻²) or (PER < 20%)	H _R	P _O	-100	-105	—	dBm
Blocking Performance	L _R		3	—	—	Class
Blocking Performance	M _R		2	—	—	Class
Blocking Performance	H _R		2	—	—	Class
Acceptable Chip Rate Tolerance		D _{fchip}	—	—	±2	%
Chip Rate		f _{chip}	—	32.768	—	kcps

2.2. Radio Link Requirement of Mode T

Table 3. Transmitter Requirements of Mode T

Characteristic	Mode	Sym	Min	Typ	Max	Unit
Center Frequency ¹ (Meter to Other)	T1, T2		868.9	868.95	869	MHz
Center Frequency ² (Other to Meter)	T2		868.278	868.3	868.322	MHz
Frequency Deviation (Meter to Other)	T1, T2		±40	±50	±80	kHz
Chip Rate (Meter to Other)	T1, T2	f _{chip}	90	100	110	kcps
Chip Rate Tolerance (Meter)	T1, T2	D _{rchip}	—	0	±1	%
Data Rate (Meter to Other, 3 out of 6 encoding)	T1, T2		—	f _{chip} × 2/3	—	bps
Chip Rate (Other to Meter)	T2	f _{chip}	—	32.768	—	kcps
Chip Rate Tolerance (Other to Meter)	T2	D _{rchip}	—	0	±1.5	%
Digital Bit Jitter (Other to Meter)	T2		—	—	±3	µs
Data Rate (Manchester)			—	f _{chip} × 1/2	—	bps
Preamble Length, Including Synchronization Word	T1, T2	PL	—	48	—	chips
Postamble (trailer) Length	T1, T2		2	—	8	chips
Acknowledge Delay	T2	t _{ACK}	2	—	3	ms
Notes:						
1. 60 ppm						
2. 25 ppm						

Table 4. Receiver Requirements of Mode T

Characteristic	Mode	Sym	Min	Typ	Max	Unit
Sensitivity (BER < 10 ⁻²) or (PER < 20%)	H _R	P _O	-100	-105	—	dBm
Blocking Performance	L _R		3	—	—	Class
Blocking Performance	M _R		2	—	—	Class
Blocking Performance	H _R		2	—	—	Class
Acceptable Chip Rate Tolerance (Other)	T1, T2	D _{fchip}	—	0	±2	%
Chip Rate (Meter)	T2	f _{chip}	—	32.768	—	kcps
Acceptable Chip Rate Tolerance (Meter)	T1, T2	D _{fchip}	—	0	±2	%

2.3. Radio Link Requirements of Mode R2

Table 5. Transmitter Requirements of Mode R2

Characteristic	Mode	Sym	Min	Typ	Max	Unit
Center Frequency (Other)	R2		—	868.33	—	MHz
Center Frequency* (Meter)	R2		—	868.03 + n x 0.08	—	MHz
Frequency Tolerance (Meter/Other)			—	0	±17	kHz
Frequency Deviation			±4.8	±6	±7.2	kHz
Chip Rate (Wakeup and Communication)		f _{chip}	—	4.8	—	kcps
Chip Rate Tolerance (Wakeup and Communication)				0	±1.5	%
Digital Bit Jitter			—	—	±15	µs
Data Rate (Manchester)			—	f _{chip} x 1/2	—	bps
Preamble Length, Including Synchronization Word	R2	P _L	96	—	—	chips
Postamble (Trailer) Length			2	—	8	chips
Response Delay (Other)		t _{RO}	3	—	50	ms
Response Delay (Meter)		t _{RM}	10	—	10000	ms

***Note:** ~20 ppm

Table 6. Receiver Requirements of Mode R2

Characteristic	Mode	Sym	Min	Typ	Max	Unit
Sensitivity (BER < 10 ⁻²) or (PER < 20%)	H _R	P _O	-105	-110	—	dBm
Blocking Performance	L _R		3	—	—	Class
Blocking Performance	M _R		2	—	—	Class
Blocking Performance	H _R		2	—	—	Class
Chip Rate (Meter)*		f _{chip}	4.7	4.8	4.9	kcps
Acceptable Chip Rate Tolerance (Meter)		D _{fchip}	—	0	±0.2	%

*Note: ~±2%

The radio link requirements can be separated into three categories: 32.768 kcps, 100 kcps and 4.8 kcps link settings. In addition to meeting the MBUS specification, Wireless MBUS devices must also comply with the ETSI wireless regulations.

2.4. Measurement Results

The radio link parameters were measured for both link requirements in the following configuration:

- The measurement setup consists of the following:
 - Si443x-B TX/RX Split Si443x TRX Test Card (High band)
 - ISM-DK3 Development Kit
 - The setup was controlled from the WDS chip configuration software.
- Measurements were done at room temperature.
- The receiver parameters were measured using Packet Error Rate as the figure of merit. The packets were transmitted by an RF Signal generator.
- The packet consists of the following:
 - Preamble
 - Wireless MBUS synchronization word
 - 20 bytes of payload
 - CRC

The tolerance extremes of the MBUS standard determines the receiver bandwidths for the different modes. If these tolerances could be relaxed then the 32k and 4.8k mode bandwidths could be narrowed resulting in improved filtering and adjacent channel rejection.

2.4.1. Measurement Results of the 32.768 kcps Mode

The following link parameters were used for the measurement:

- Center frequency: 868.3 MHz
- Chip rate: 32.768 kcps, 2 FSK modulation
- Frequency deviation: ±50 kHz
- Receiver filter BW: 232 kHz
- Packet Format: preamble(n=15) x (01) + sync word "00011011010010110" + 20 byte payload + CRC

2.4.1.1. Receiver Sensitivity

- The measured sensitivity for <20% PER is: -104.0 dBm.

2.4.1.2. Receiver Frequency Error Tolerance

Figure 1 shows the frequency error tolerance capability of the receiver. The plot shows the sensitivity of the receiver measured at 20% PER, versus frequency offset.

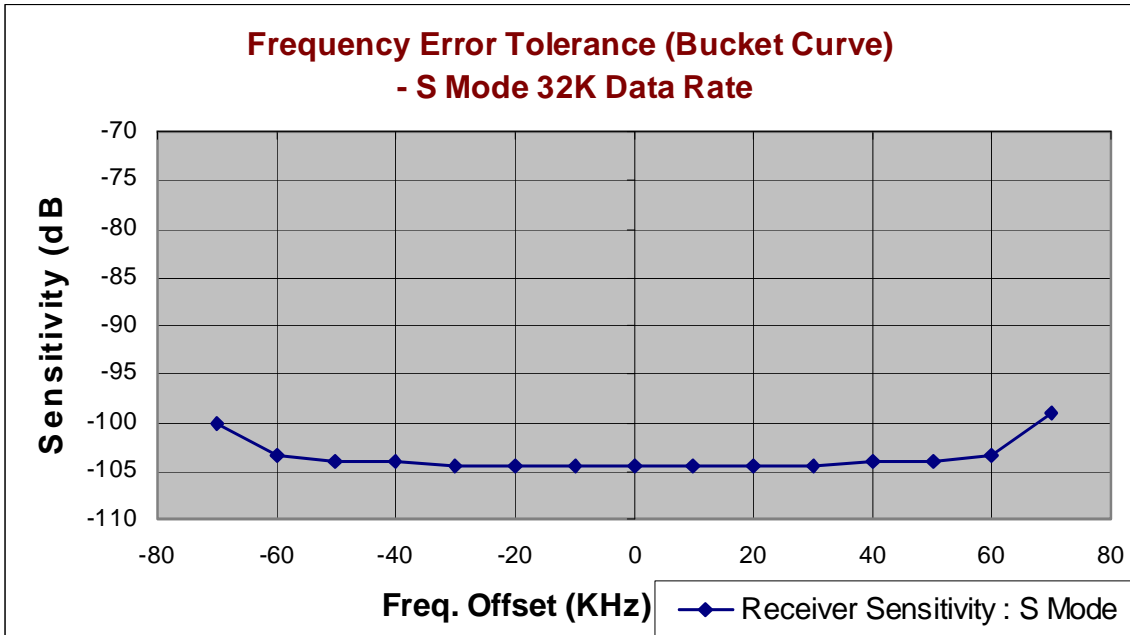


Figure 1. 32.768 kcps MBUS Sensitivity vs. Frequency Offset at 20% PER

2.4.1.3. Receiver Data Rate Error Tolerance

Figure 2 shows the Data rate error tolerance capability of the receiver. The plot shows the sensitivity of the receiver measured at 20% PER, versus data rate.

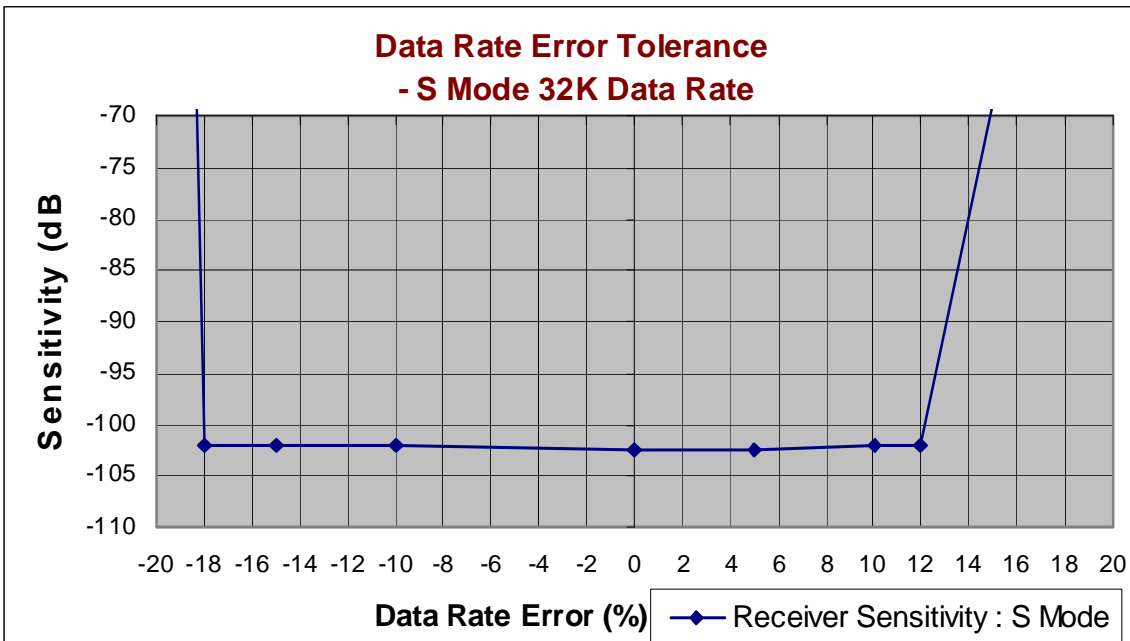


Figure 2. 32.768 kcps MBUS Sensitivity vs. Data Rate Variation at 20% PER

2.4.1.4. Receiver Deviation Error Tolerance

Figure 3 shows the data rate error tolerance capability of the receiver. The plot shows the sensitivity of the receiver measured at 20% PER, versus data rate.

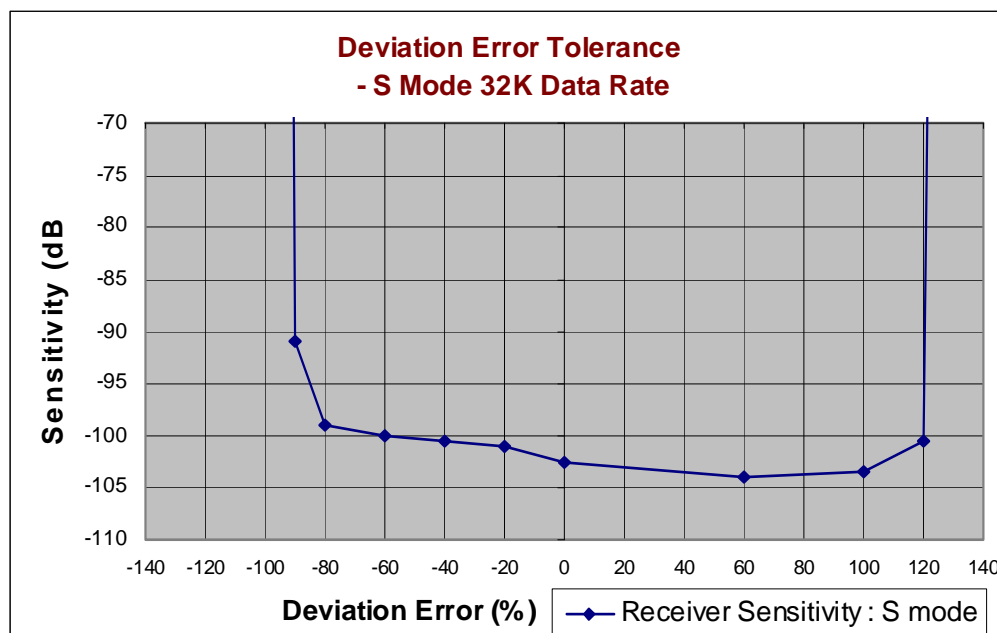


Figure 3. 32.768 kcps MBUS Sensitivity vs. Deviation Variation at 20% PER

2.4.1.5. Receiver Blocking Performance

Figure 4 shows the selectivity/blocking performance of the receiver.

The first plot shows the receiver selectivity with blocker on the positive frequency offset with respect to the receiver. The selectivity was measured at 20% PER at different frequency offsets.

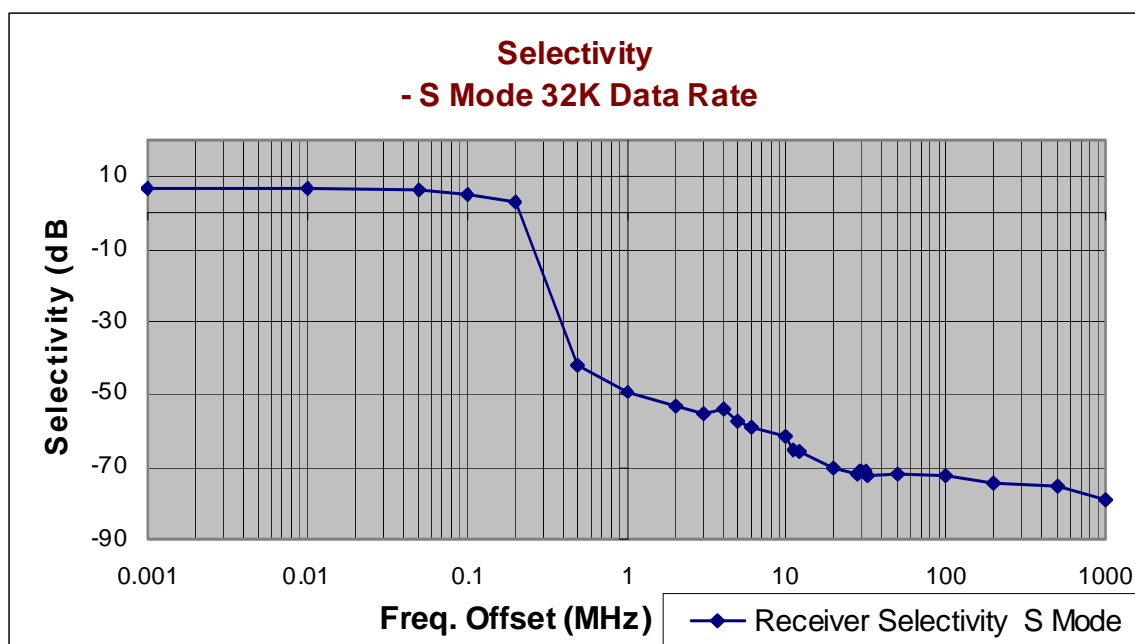


Figure 4. 32.768 kcps MBUS Selectivity at 20% PER

AN361

The second plot in Figure 5 shows the receiver selectivity with blocker on the negative/image frequency offset with respect to the receiver. The selectivity was measured at 20% PER at different frequency offsets.

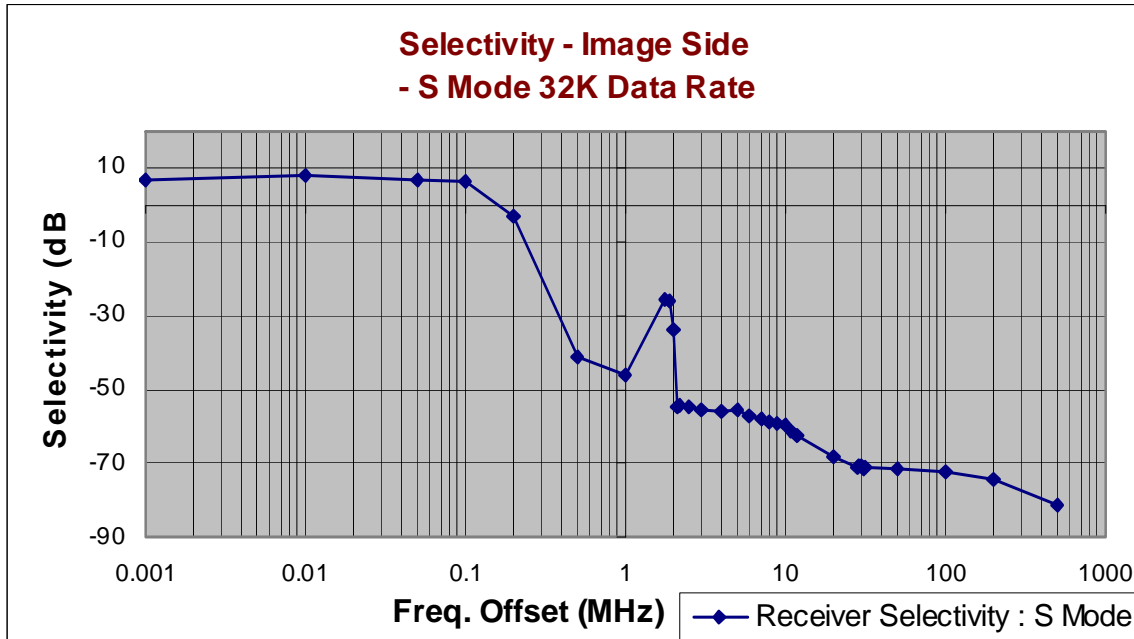


Figure 5. 32.768 kcps MBUS Selectivity (Image Side) at 20% PER

Conclusion:

- Si443x_B0 has -104.5 dBm sensitivity in 32.768 kcps W-MBUS mode, which is 4.5 dB better than the W-MBUS S mode requirements.
- Si443x_B0 meets all the corners vs. frequency error, data rate error, deviation error required by the W-MBUS standard.
- MBUS signal can be received with in-built Packet Handler in all the corner cases. This eliminates the need of any additional microcontroller for data recovery. It also simplifies the complexity of the packet handling code on the microcontroller.
- Si443x_B0 meets the ETSI Class2 blocking requirements.
- Si443x_B0 complies with the W-MBUS highest receiver performance class.
- S Mode requires support with short preamble. The chip requires to function in fast acquisition mode. This also requires a wider bandwidth in order to cover for the frequency offset error. Hence, a wider filter is used in S mode than that used in T mode.

2.4.2. Measurement Results of the 100 kcps Mode

The following link parameters were used for the measurement:

- Center frequency: 868.95 MHz
- Chip rate: 100 kcps, 2 FSK modulation
- Frequency deviation: ± 50 kHz
- Receiver Filter Bandwidth: 208 kHz
- Packet Format: preamble(n=19) x (01) + sync word "0000111101" + 20 byte payload + CRC

2.4.2.1. Receiver Sensitivity

The measured sensitivity for <20% PER is -103 dBm.

2.4.2.2. Receiver Frequency Error Tolerance

Figure 6 shows the frequency error tolerance capability of the receiver. The plot shows the sensitivity of the receiver measured at 20% PER, versus frequency offset.

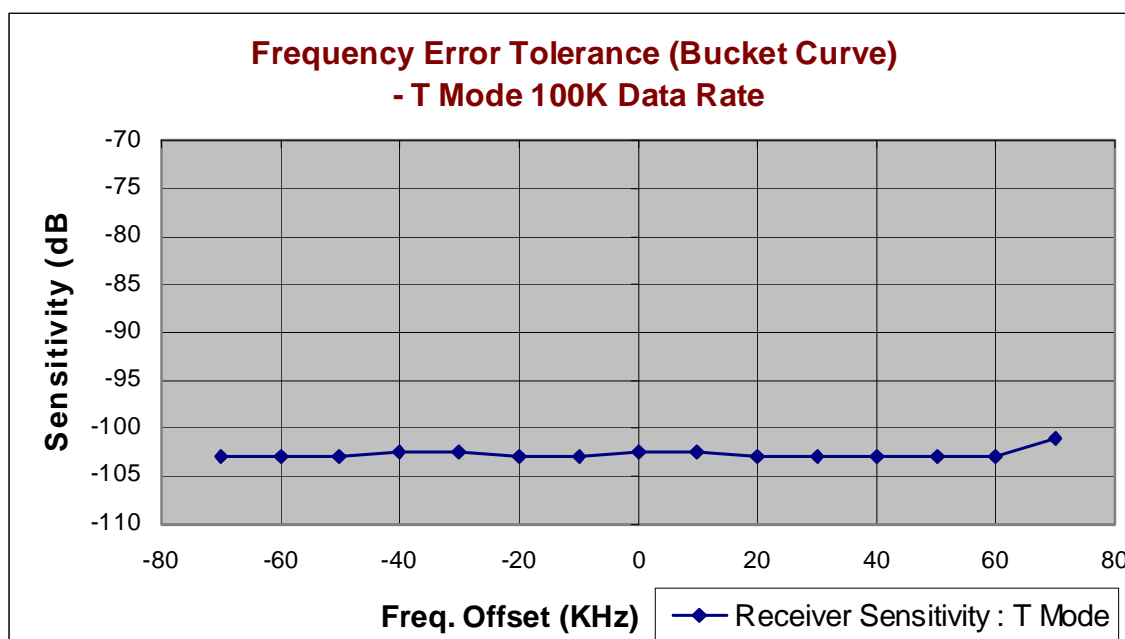


Figure 6. 100 kcps MBUS Sensitivity versus Frequency Offset at 20% PER

2.4.2.3. Receiver Data Rate Error Tolerance

Figure 7 shows the Data rate error tolerance capability of the receiver. The plot shows the sensitivity of the receiver measured at 20% PER, versus data rate.

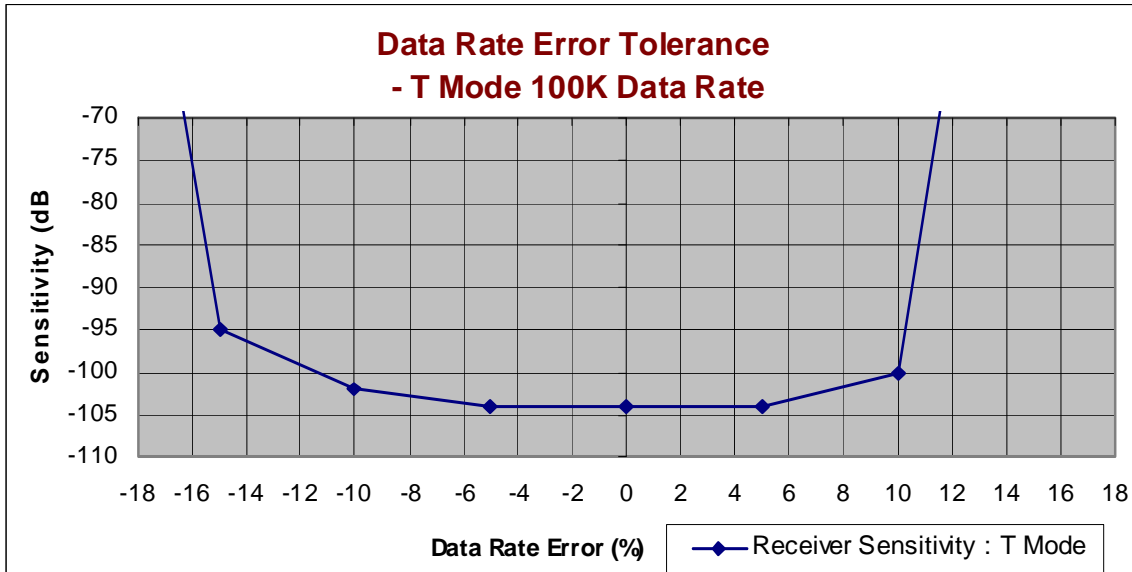


Figure 7. 100 kcps MBUS Sensitivity versus Data-Rate Variation at 20% PER

2.4.2.4. Receiver Deviation Error Tolerance

Figure 8 shows the Data rate error tolerance capability of the receiver. The plot shows the sensitivity of the receiver measured at 20% PER, versus data rate.

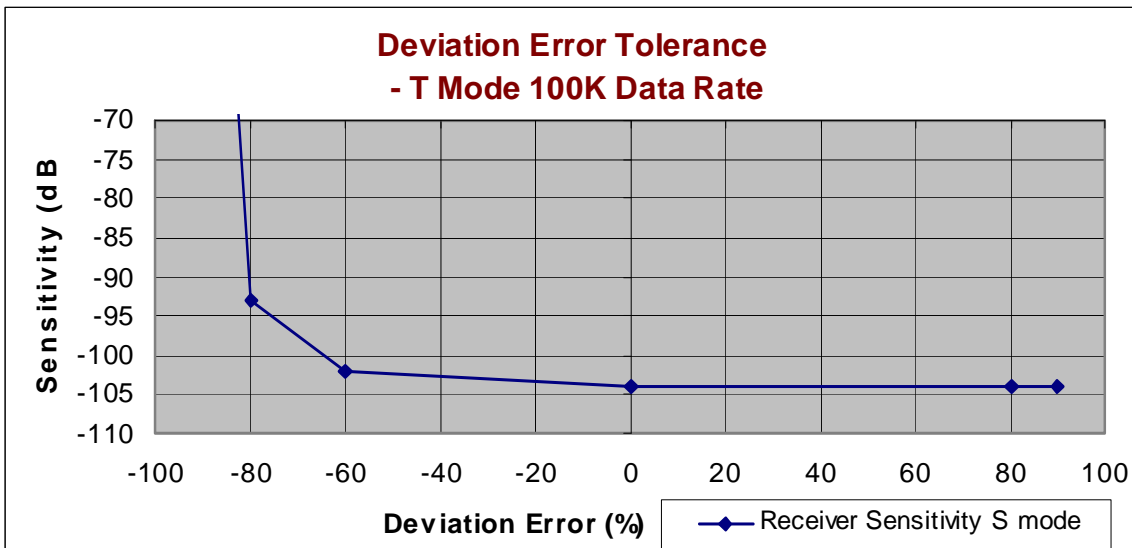


Figure 8. 100 kcps MBUS Sensitivity versus Deviation Variation at 20% PER

2.4.2.5. Blocking Performance

Figure 9 shows the selectivity/blocking performance of the receiver.

The first plot shows the receiver selectivity with blocker on the positive frequency offset with respect to the receiver. The selectivity was measured at 20% PER at different frequency offsets.

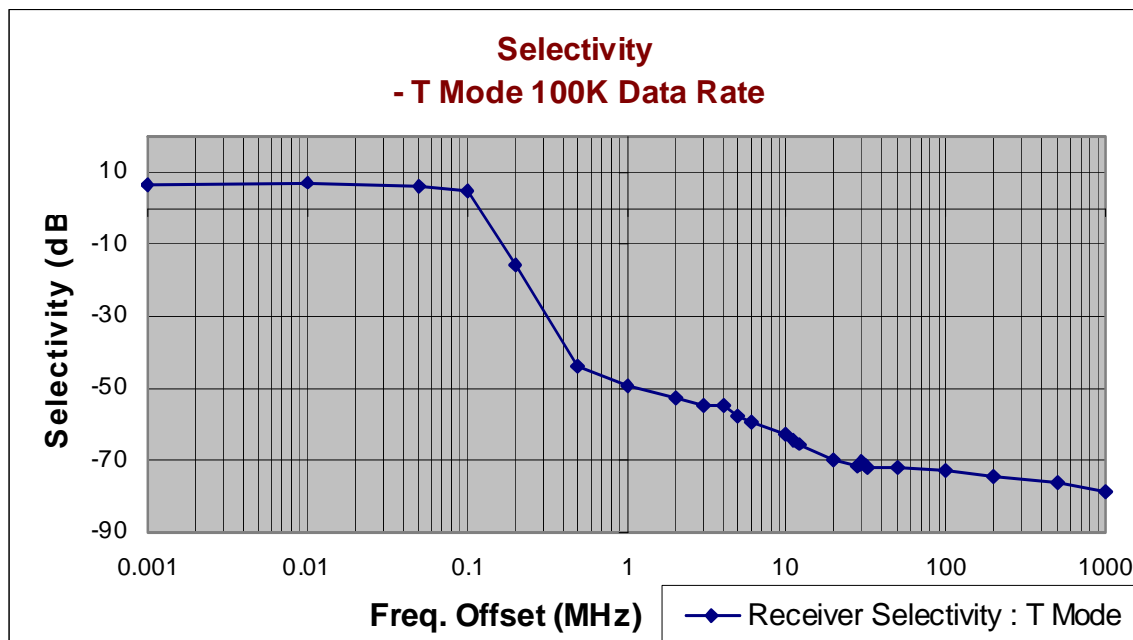


Figure 9. 100 kcps MBUS Selectivity at 20% PER

The next plot in Figure 10 shows the receiver selectivity with blocker on the negative/image frequency offset with respect to the receiver. The selectivity was measured at 20% PER at different frequency offsets.

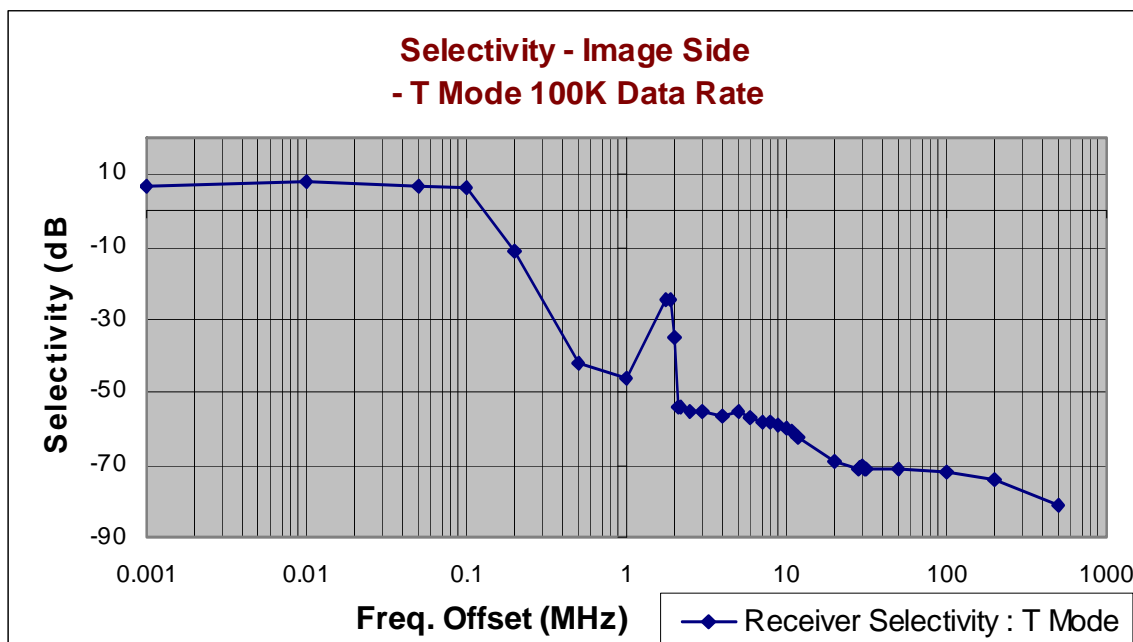


Figure 10. 100 kcps MBUS Selectivity (Image Side) at 20% PER

AN361

Conclusion:

- Si443x_B0 has -103 dBm sensitivity in 100 kcps W-MBUS mode, which is 3 dB better than the W-MBUS T mode requirements.
- Si443x_B0 meets all the corners viz. frequency error, data rate error, deviation error required by the W-MBUS standard.
- MBUS signal can be received with in-built Packet Handler in all the corner cases. This eliminates the need of any additional microcontroller for data recovery. It also simplifies the complexity of the packet handling code on the microcontroller.
- Si443x_B0 meets the ETSI Class2 blocking requirements.
- Si443x_B0 complies with the W-MBUS highest receiver performance class.

2.4.3. Measurement Results of the 4.8 kcps Mode

The following link parameters were used for the measurement:

- Center frequency: MHz
- Chip rate: 4.8 kcps, 2 FSK modulation
- Frequency deviation: ± 6 kHz
- Receiver Filter BW: 95.3 kHz
- Packet Format: preamble($n=39$) x (01) + sync word "000111011010010110" + 20 byte payload + CRC

2.4.3.1. Receiver sensitivity

- The measured sensitivity with 20 ppm crystals for $<20\%$ PER is -106.5 dBm.
- The measured sensitivity with 10 ppm crystals for $<20\%$ PER is -110.0 dBm.
- The measured sensitivity with 4 ppm crystals for $<20\%$ PER is -114.0 dBm.
- The measured sensitivity with 1 ppm crystals for $<20\%$ PER is -116.0 dBm.

A 20 ppm crystal was selected for remaining measurements. The selectivity will improve by decreasing the crystal tolerance as the required BW of the receiver decreases. This will allow us for smaller channel filters to be selected inside the chip.

2.4.3.2. Receiver Frequency Error Tolerance

Figure 11 shows the frequency error tolerance capability of the receiver. The plot shows the sensitivity of the receiver measured at 20% PER, versus frequency offset.

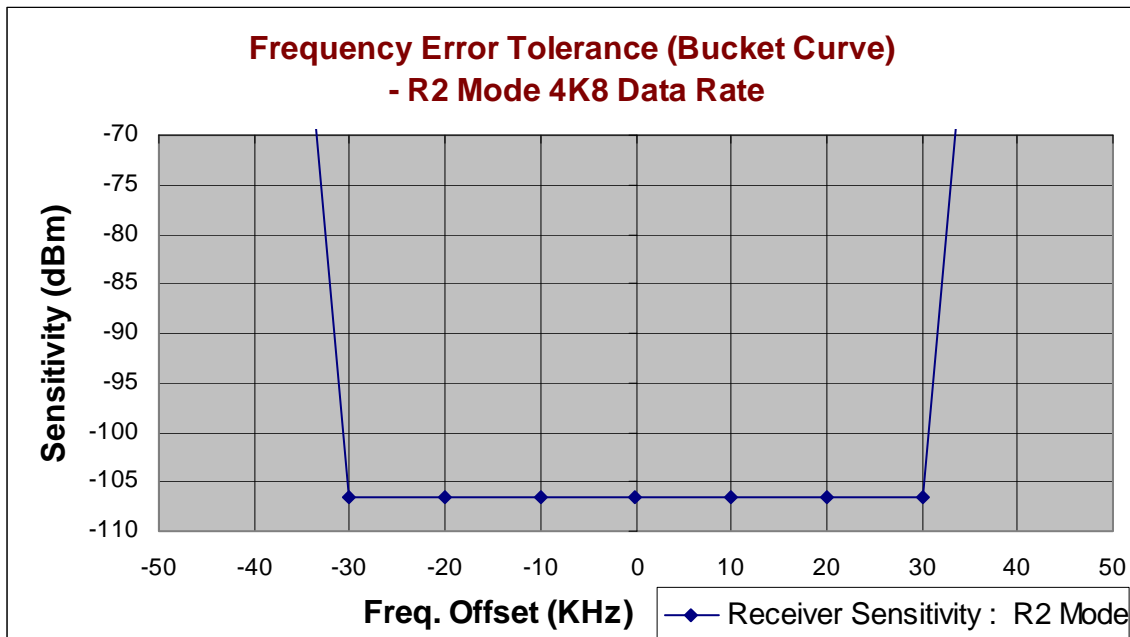


Figure 11. 4.8 kcps MBUS Sensitivity versus Frequency Offset at 20% PER

2.4.3.3. Receiver Data Rate Error Tolerance

Figure 12 shows the Data rate error tolerance capability of the receiver. The plot shows the sensitivity of the receiver measured at 20% PER, versus data rate.

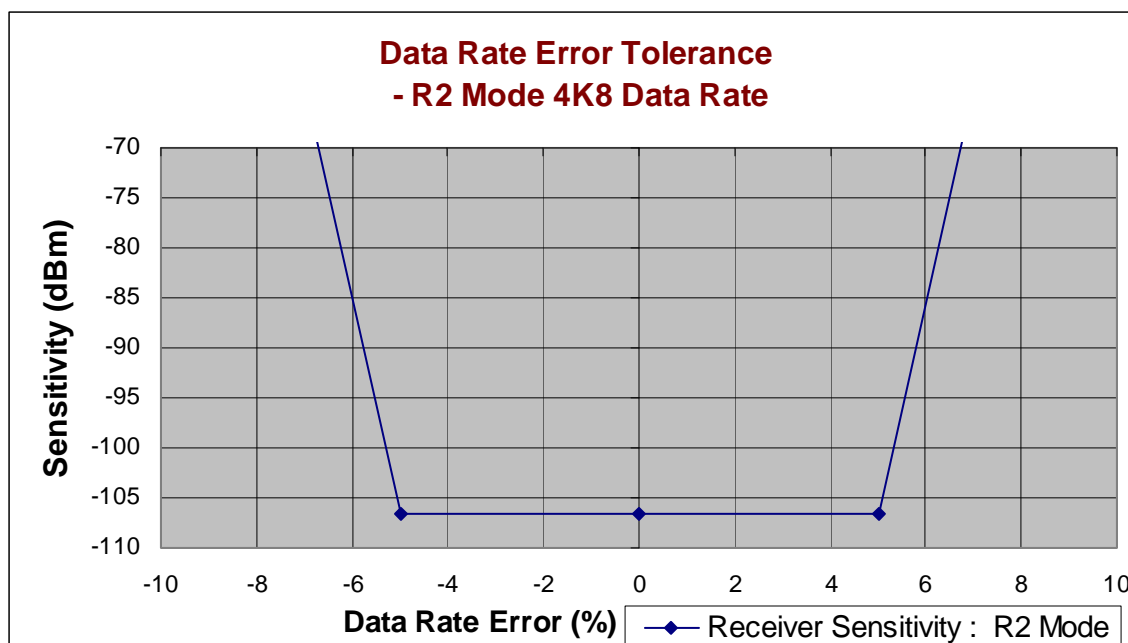


Figure 12. 4.8 kcps MBUS Sensitivity versus Data-Rate Variation at 20% PER

2.4.3.4. Receiver Deviation Error Tolerance

Figure 13 shows the Data rate error tolerance capability of the receiver. The plot shows the sensitivity of the receiver measured at 20% PER, versus data rate.

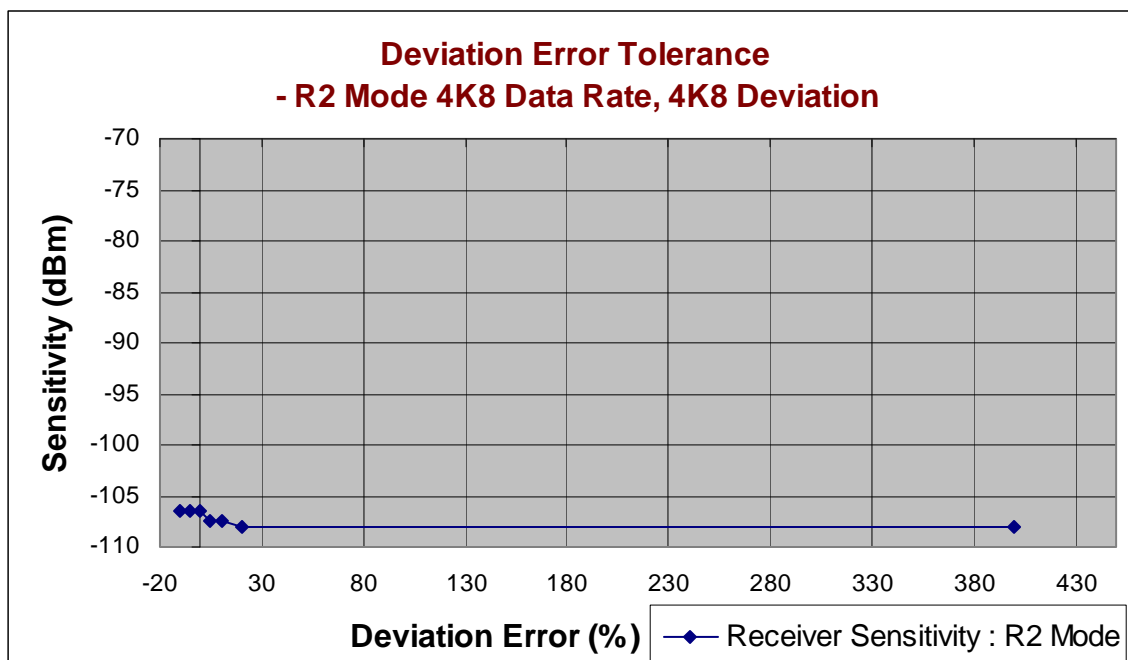


Figure 13. 4.8 kcps MBUS Sensitivity versus Deviation Variation at 20% PER

2.4.3.5. Blocking performance

Figure 14 shows the selectivity/blocking performance of the receiver.

The first plot shows the receiver selectivity with blocker on the positive frequency offset with respect to the receiver. The selectivity was measured at 20% PER at different frequency offsets.

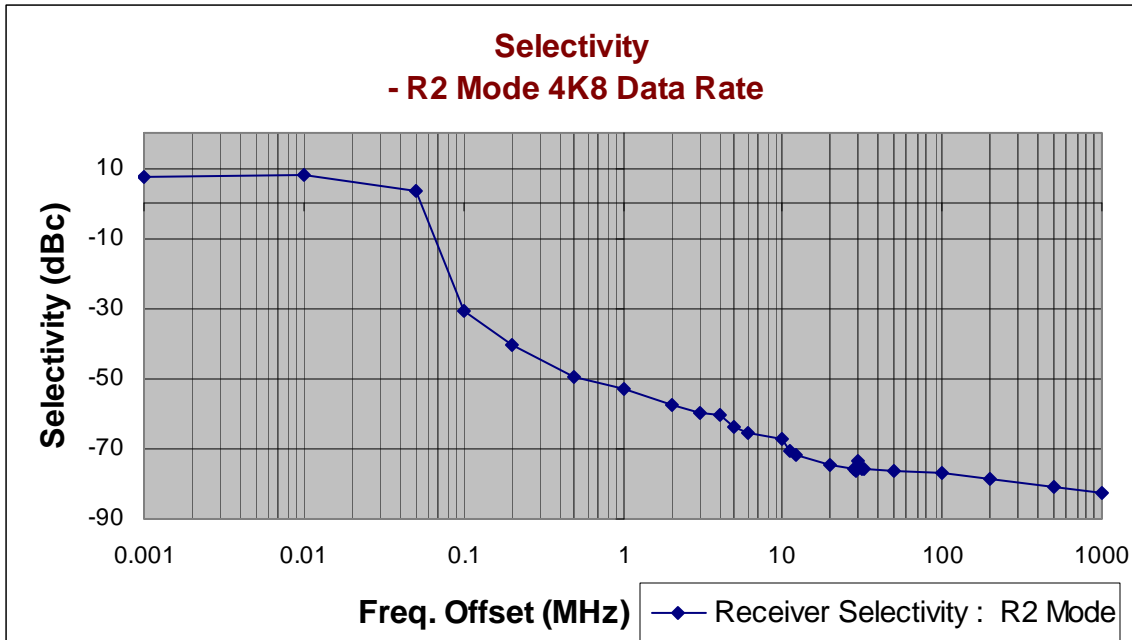


Figure 14. 4.8 kcps MBUS Selectivity at 20% PER

The second plot in Figure 15 shows the receiver selectivity with the blocker on the negative/image frequency offset with respect to the receiver. The selectivity was measured at 20% PER at different frequency offsets.

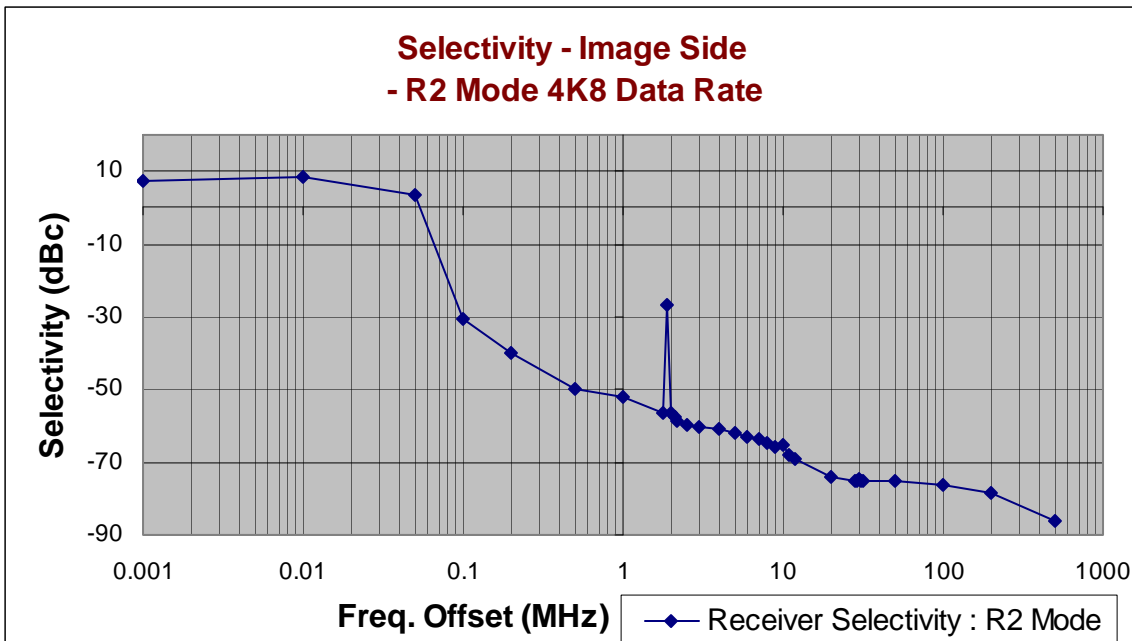


Figure 15. 4.8 kcps MBUS Selectivity (Image Side) at 20% PER

Conclusion:

- Si443x_B0 has -106.5 dBm sensitivity in 4.8 kcps W-MBUS mode with 20 ppm crystals, which is 1.5 dB better than the W-MBUS R2 mode requirements. Using better ppm crystals sensitivity up to 11 dB better can be achieved.
- Si443x_B0 meets all the corners vs. frequency error, data rate error, deviation error required by the W-MBUS standard.
- MBUS signal can be received with in-built Packet Handler in all the corner cases. This eliminates the need of any additional microcontroller for data recovery. It also simplifies the complexity of the packet handling code on the microcontroller.
- Si443x_B0 meets the ETSI Class2 blocking requirements.
- Si443x_B0 complies with the W-MBUS highest receiver performance class.

2.5. Data link layer support**2.5.1. Manchester Coding, Preamble and Synchron Word in Mode S**

The Si443x-B0 has a built-in Manchester coder and decoder circuit, removing the need to implement this function in the microcontroller.

Mode S requires the following preamble and synchronization word:

$n \times (01)000111011010010110$
 where n is the required preamble length

- For long header (Mode S1 or optional in Mode S2): $n \geq 279$
- For short header (Mode S2): $n \geq 15$

In the worst case situation the receiver will be able to receive the packet if the preamble is 30 bits long. The synchronization word is not a multiple of 8, but the radio can be configured to receive the preamble and synchronization word automatically.

The Si443x-B0 transceiver chip has a built in, configurable packet handler circuit: the preamble detection and synchronization word recognition circuit can be programmed in octets. If the wireless MBUS preamble and synchronization word are considered as one functional block and it is divided into octets, the Si443x_B0 transceiver can be configured to recognize the preamble and synchronization word automatically. In this case the internal FIFO can be used for receiving the entire packet. Using the FIFO will drastically decrease the load on the microcontroller removing the need to receive the packet one bit at a time and offloading preamble and synchronization word recognition.

Table 7. Preamble and Synchronization Word Specification of the Standard

Wireless MBUS specification	
Preamble (30bits)	Synchron word (18bits)
01010101010101010101010101010101	000111011010010110

If the preamble and the synchronization word are considered as in Table 7, and the packet handler of the Si443x-B0 is set according Table 8, the packet handler can receive and decode the MBUS packets.

Table 8. Si443x-B0 MBUS Compliance Settings

Preamble length	Synch Word 3	Synch Word 2	Synch Word 1
3 bytes	0x54	0x76	0x96

NOTES:

CONTACT INFORMATION

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page:
<https://www.silabs.com/support/pages/contacttechnicalsupport.aspx>
and register to submit a technical support request.

The information in this document is believed to be accurate in all respects at the time of publication but is subject to change without notice. Silicon Laboratories assumes no responsibility for errors and omissions, and disclaims responsibility for any consequences resulting from the use of information included herein. Additionally, Silicon Laboratories assumes no responsibility for the functioning of undescribed features or parameters. Silicon Laboratories reserves the right to make changes without further notice. Silicon Laboratories makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Silicon Laboratories assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Silicon Laboratories products are not designed, intended, or authorized for use in applications intended to support or sustain life, or for any other application in which the failure of the Silicon Laboratories product could create a situation where personal injury or death may occur. Should Buyer purchase or use Silicon Laboratories products for any such unintended or unauthorized application, Buyer shall indemnify and hold Silicon Laboratories harmless against all claims and damages.

Silicon Laboratories and Silicon Labs are trademarks of Silicon Laboratories Inc.
Other products or brandnames mentioned herein are trademarks or registered trademarks of their respective holders.