AN368

DIFFERENCES BETWEEN THE C8051F34A AND THE C8051T62X AND C8051T32X DEVICE FAMILIES

1. Introduction

The C8051T62x and C8051T32x devices are low-cost, electrically-programmable read-only memory (EPROM) microcontrollers based on the Silicon Laboratories CIP-51 microcontroller core. As with Silicon Laboratories' C8051F-series Flash-based microcontrollers, the C8051T62x and C8051T32x are highly-integrated, mixed-signal microcontrollers. The C2 2-wire debugging and programming interface included on each device allows designers to rapidly develop and debug firmware.

Because the devices in the C8051T62x and C8051T32x families cannot be erased, a new device is required for testing every time the firmware changes. This can make the code development process more difficult and time-consuming. Fortunately, the features found in the C8051T62x and C8051T32x families are closely related to the features of the Flash-based C8051F34A. The C8051F34A is included on an "emulation daughter card" in the development kit for the EPROM device families. In most cases, the C8051F34A can be used for the entire code development process, and the firmware image will be interchangeable between the two device families. For systems that take advantage of the additional features found in the C8051T62x or C8051T32x families, the majority of the firmware can still be developed on the C8051F34A device and then ported to the C8051T62x or C8051T32x during the final stages of code development.

This document details the hardware differences between the EPROM and Flash device families and provides some guidelines for using the C8051F34A to develop code for the C8051T62x and C8051T32x.

For porting guides for pin-compatible devices, refer to "AN455: Porting Code for C8051F320/1 Devices to C8051T320/1 Devices" and "AN456: Porting Code for C8051F326/7 Devices to C8051T326/7 Devices".

2. Key Points

- Although the majority of device features are identical between the C8051F34A, C8051T62x, and C8051T32x, there are some hardware differences.
- When developing code for the C8051T62x or the C8051T32x device families, the majority of the code development process can be done on one of the Flash-based counterparts, and the C8051F34A is the most functionally similar Flash-based relative.
- Each device family has a set of unique features that are not present on the other families. Recognizing these differences is the key to successfully developing common code (i.e., code that works across all families) or code that uses some of the additional features found on the C8051T62x and C8051T32x.

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3. Special Function Registers

The special function register (SFR) memory map of the C8051T62x and C8051T32x is very similar to the SFR memory map of the C8051F34A. However, there are a few differences related to functionality and features found only on certain devices. Fortunately, SFRs that exist in one family but not another can be safely written and read on the other devices without causing a problem. Likewise, certain registers have additional bits defined that are not present on all devices. In these cases, the default bit settings are safe to write, and the read values of those bits are defined in the data sheet. Figure 1 shows the combined SFR map of C8051T620/T621/T320/T321/T322/T323 and the C8051F34A. Figure 2 shows the combined SFR map of the C8051T622/T623/T326/T327 and the C8051F34A. The locations of SFRs that differ between the families and those with only bitwise differences are highlighted. The boxes with two SFRs listed show that two different families have exclusive SFRs at the same location; the C8051T62x and C8051T32x families are the registers not in parentheses while the C8051F34A registers are indicated within parentheses.

F8	SPI0CN	PCA0L	PCA0H	PCA0CPL0	PCA0CPH0	PCA0CPL4	PCA0CPH4	VDM0CN
F0	B	P0MDIN	P1MDIN	P2MDIN	PCA0PWM (P3MDIN)	IAPCN (P4MDIN)	EIP1	EIP2
E8	ADC0CN	PCA0CPL1	PCA0CPH1	PCA0CPL2	PCA0CPH2	PCA0CPL3	PCA0CPH3	RSTSRC
E0	ACC	XBR0	XBR1	XBR2	IT01CF	SMOD1	EIE1	EIE2
D8	PCA0CN	PCA0MD	PCA0CPM0	PCA0CPM1	PCA0CPM2	PCA0CPM3	PCA0CPM4	P3SKIP
D0	PSW	REF0CN	SCON1	SBUF1	P0SKIP	P1SKIP	P2SKIP	USB0XCN
C8	TMR2CN	REG01CN (REG0CN)	TMR2RLL	TMR2RLH	TMR2L	TMR2H	-	SMB0ADM (-)
C0	SMB0CN	SMB0CF	SMB0DAT	ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH	SMB0ADR (P4)
B8	IP	CLKMUL	P1MASK (AMX0N)	AMX0P	ADC0CF	ADC0L	ADC0H	-
B0	P3	OSCXCN	OSCICN	OSCICL	SBRLL1	SBRLH1	P1MAT (FLSCL)	MEMKEY (FLKEY)
A8	IE	CLKSEL	EMI0CN	-	SBCON1	-	P0MASK (P4MDOUT)	PFE0CN
A0	P2	SPI0CFG	SPI0CKR	SPI0DAT	P0MDOUT	P1MDOUT	P2MDOUT	P3MDOUT
98	SCON0	SBUF0	CPT1CN	CPT0CN	CPT1MD	CPT0MD	CPT1MX	CPT0MX
90	P1	TMR3CN	TMR3RLL	TMR3RLH	TMR3L	TMR3H	USB0ADR	USB0DAT
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	PSCTL
80	P0	SP	DPL	DPH	P0MAT (EMI0TC)	EMI0CF	OSCLCN	PCON
	0(8) Bit-Addressable	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)

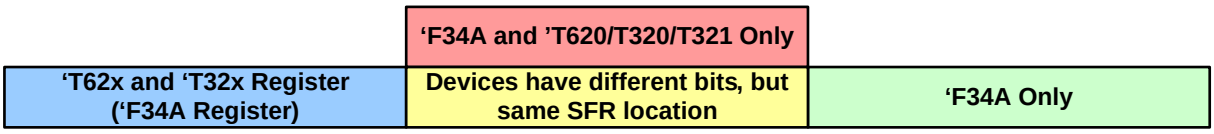


Figure 1. SFR Memory Map Differences between C8051T620/T621/T320/T321/T322/T323 and C8051F34A

F8	SPI0CN	PCA0L	PCA0H	PCA0CPL0	PCA0CPH0	PCA0CPL4	PCA0CPH4	VDM0CN
F0	B	P0MDIN	P1MDIN	P2MDIN	PCA0PWM (P3MDIN)	IAPCN (P4MDIN)	EIP1	EIP2
E8	ADC0CN	PCA0CPL1	PCA0CPH1	PCA0CPL2	PCA0CPH2	PCA0CPL3	PCA0CPH3	RSTSRC
E0	ACC	XBR0	XBR1	XBR2	IT01CF	SMOD1	EIE1	EIE2
D8	PCA0CN	PCA0MD	PCA0CPM0	PCA0CPM1	PCA0CPM2	PCA0CPM3	PCA0CPM4	P3SKIP
D0	PSW	REF0CN	SCON1	SBUF1	P0SKIP	P1SKIP	P2SKIP	USB0XCN
C8	TMR2CN	REG01CN (REG0CN)	TMR2RLL	TMR2RLH	TMR2L	TMR2H	-	SMB0ADM (-)
C0	SMB0CN	SMB0CF	SMB0DAT	ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH	SMB0ADR (P4)
B8	IP	CLKMUL	P1MASK (AMX0N)	AMX0P	ADC0CF	ADC0L	ADC0H	-
B0	P3	OSCXCN	OSCICN	OSCICL	SBRLL1	SBRLH1	P1MAT (FLSCL)	MEMKEY (FLKEY)
A8	IE	CLKSEL	EMI0CN	-	SBCON1	-	P0MASK (P4MDOUT)	PFE0CN
A0	P2	SPI0CFG	SPI0CKR	SPI0DAT	P0MDOUT	P1MDOUT	P2MDOUT	P3MDOUT
98	SCON0	SBUF0	CPT1CN	CPT0CN	CPT1MD	CPT0MD	CPT1MX	CPT0MX
90	P1	TMR3CN	TMR3RLL	TMR3RLH	TMR3L	TMR3H	USB0ADR	USB0DAT
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	PSCTL
80	P0	SP	DPL	DPH	P0MAT (EMI0TC)	EMI0CF	OSCLCN	PCON
	0(8) Bit-Addressable	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)

‘T62x and ‘T32x Register (‘F34A Register)	Devices have different bits, but same SFR location	‘F34A Only

Figure 2. SFR Memory Map Differences between C8051T622/T623/T326/T327 and C8051F34A

4. Code Memory Storage

The most obvious difference between the C8051F34A and the C8051T62x/T32x devices is the code memory storage technology. On the C8051F34A device, Flash memory is used, while on the C8051T62x and C8051T32x devices, a byte-programmable EPROM code memory architecture is used. EPROM memory can be programmed one byte at a time but cannot be erased. Table 1 details some parameters of interest related to the code storage technology.

Table 1. Code Memory Storage

Feature	C8051F34A	C8051T62x C8051T32x
Code memory can be erased and reprogrammed	Yes	No
Programming voltage (V_{PP}) required to program code memory	No	Yes
Code memory can be erased from firmware on the device	Yes	No
Code memory can be written from firmware on the device	Yes	
Code memory can be read from firmware on the device	Yes	

The impact of code storage technology on the development of T62x/T32x firmware is minimal. When developing firmware for the C8051T62x or C8051T32x on the C8051F34A or porting an existing design from any C8051F34x device, ensure that there are no firmware routines intended to erase areas of code memory, as they will not have any effect on the C8051T62x or C8051T32x. Firmware can write to code memory on the C8051T62x and C8051T32x using in-application programming; however, each bit can only be cleared once and can never be reset. A 4.7 µF capacitor is required between the V_{PP} pin and ground to use in application programming on the C8051T62x and C8051T32x devices.

5. ADC and Temperature Sensor

The ADC peripheral is different between the Flash and EPROM devices. The C8051F34A features a 10-bit, 200 ksps SAR, while the C8051T620/T320/T321 devices have a 10-bit, 500 ksps SAR. The C8051T621/T622/T623/T322/T323/T326/T327 devices do not have an ADC. A list of ADC differences that may affect the system and code design are detailed in Table 2.

Table 2. ADC and Temperature Sensor

Feature	C8051F34A	C8051T620/T320/T321
Output Word Resolution	10 bits	10 bits
Throughput (Sampling Rate)	200 ksps	500 ksps
Minimum Tracking Time	300 ns	300 ns
Maximum SAR Clock Speed	3 MHz	8.33 MHz
Gain Settings	1x	0.5x, 1x
Differential Inputs (AIN+ and AIN-)	Yes	No
Calibrated Temperature Sensor Offset	No	Yes
Voltage Reference (V_{REF}) Options	V_{DD}, External Pin, On-chip 2.4 V	V_{DD}, External Pin, LDO Output, On-chip 1.8, 1.2 V or 2.4 V

5.1. Analog Multiplexer and Gain Settings

The ADC on the C8051T620/T320/T321 contains a subset of the multiplexing features found on the C8051F34A. On the C8051T620/T320/T321, only the positive channel (AIN+) of the ADC is available, meaning that only single-ended measurements are possible (from AIN+ to GND). When developing code for the C8051T620/T320/T321 on the C8051F34A, the five LSBs of the AMX0N register should always be written to 11111b (binary). This will select GND as the negative input on the C8051F34A's ADC and perform a single-ended measurement the same way that the C8051T620/T320/T321 devices do by default. In addition to the 1x gain setting of the C8051F34A's ADC, C8051T620/T320/T321 devices have a gain setting of 0.5x.

5.2. SAR Timing

During a conversion, the SAR ADC is normally in one of two different phases, “tracking” or “converting” as shown in Figure 3.

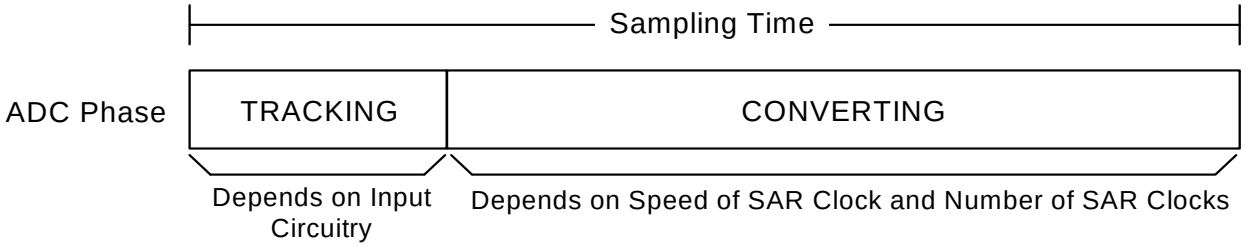


Figure 3. ADC Sampling Phases: Tracking and Converting

Establishing the faster conversion rate available on the T620/T320/T321 requires programming the device to a faster SAR clock frequency. During the tracking phase, the ADC's sampling capacitor is connected to the external pin input through the analog multiplexer. When a conversion is initiated by the selected start-of-conversion source, the sampling capacitor is disconnected from the input, and the SAR conversion is performed. To speed up the conversion time and allow enough tracking time, the SAR clock must be set to a higher rate.

The ADC on both devices requires a minimum 300 ns tracking time before each conversion, and additional tracking time may be necessary depending on the nature of the front-end circuitry and the supply voltage of the ‘T620/T320/T321 (see the “Settling Time Requirements” section of the data sheet for more details). The ‘T620/T320/T321 SAR can operate with a faster SAR clock than the C8051F34A to accommodate the higher sampling rate. If the application requires the 'T620/T320/T321 SAR clock speed to be faster than the C8051F34A SAR clock specification, the switch to the faster SAR clock should be implemented as one of the final development steps after the majority of other code development is completed on the C8051F34A. Making this firmware change at the end of the porting process can help reduce the number of devices programmed during firmware development.

5.3. Temperature Sensor

Use of the temperature sensor on the C8051T620/T320/T321 is very similar to that on the C8051F34A. However, the transfer functions of the temperature sensors on each device family are different. Different values for the offset and slope of the temperature sensor are necessary to accurately calculate the temperature on each device family. Additionally, to help remove some of the error due to part-to-part variations, the ‘T620/T320/T321 temperature sensor output has been measured during production test for each device. The results of the measurement are stored in EPROM at locations 0x3FFB (TOFFH) and 0x3FFA (TOFFL). The 10-bit calibration value is written to the two EPROM locations such that 0x3FFB (TOFFH) contains the eight most significant bits of the calibration value and bits 7 and 6 of 0x3FFA (TOFFL) contain the two least significant bits of the calibration value. These values represent the output of the temperature sensor at an ambient temperature of 0 °C, if measured with the ADC using the internal regulator as a reference voltage.

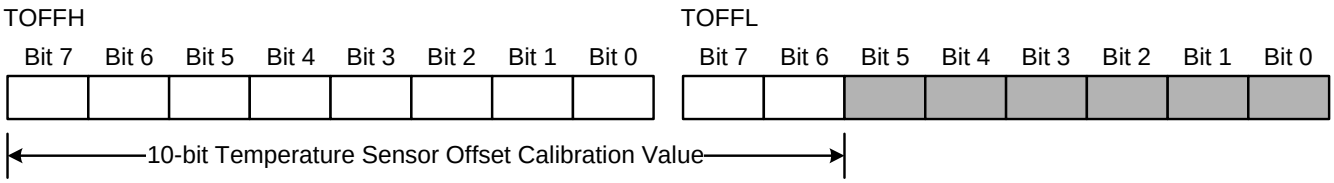


Figure 4. TOFFH and TOFFL Calibration Value Orientation

5.4. Voltage Reference Options

On the C8051F34A, the ADC can use one of three different voltage reference options: the VDD supply pin, an external reference applied to the VREF pin, or the on-chip 2.4 V reference voltage routed to the VREF pin. In the C8051T620/T320/T321 family, two additional voltage reference options are available. By setting the REGOVR bit in the REF0CN register, the ADC can use the internal regulator as the voltage reference for the ADC. If using the on-chip reference voltage generator, the REFBGS bit can also be used to switch between 1.2 V and 2.4 V.

5.5. External Conversion Start (CNVSTR) Timing

If the CNVSTR pin is used to begin conversions on the ADC, it is important to note the differences in timing between the C8051F34A and the C8051T620/T320/T321 family. On the C8051F34A, the rising edge of CNVSTR always ends tracking mode and begins a conversion. On the ‘T620/T320/T321 family, when the AD0TM bit is set to 0, conversions are initiated on the rising edge of CNVSTR, and tracking occurs when CNVSTR is low. On the ‘T620/T320/T321, if AD0TM is set to 1, tracking occurs any time a conversion is not in progress and lasts an additional three SAR clocks after the rising edge of CNVSTR.

6. Supply and I/O Pin Voltages

The C8051T62x and C8051T32x are implemented in a process technology different than that of the C8051F34A. Consequently, there are some additional features and restrictions related to the supply voltage and allowable I/O pin voltages; these are detailed in Table 3.

Table 3. Supply and I/O Pin Voltages

Feature	C8051F34A	C8051T63x C8051T32x
Supply Voltage Range	2.7–3.6 V	1.8–3.6 V
3.3 V Regulator for V_{DD}	Yes	No
3.45 V Regulator for V_{DD}	No	Yes
1.8 V Regulator for Internal Core Voltage	No	Yes
Maximum Voltage on any I/O Pin	5.8 V	V_{DD} + 3.6 V*
***Note:** Up to a maximum of 5.8 V		

The 3.3 V regulator on the F34A is used to output a 3.3 V signal on the V_{DD} pin that can be used to power external devices. On the F34A, the voltage source on the REGIN pin is regulated down to 3.3 V. The T62x and T32x families have a 3.45 V regulator instead of a 3.3 V regulator. In the T62x and T32x families, the voltage source on the REGIN pin is regulated down to 3.45 V and output on the VDD pin, which can be used to power external devices. The internal LDO regulator included on the T62x and T32x families is used to regulate the V_{DD} supply voltage down to 1.8 V for the controller core. The regulated core voltage is used only internally. All external voltages and analog circuits on the device are powered from the V_{DD} voltage; so, the I/O logic levels and the allowable ADC and comparator input ranges are all relative to V_{DD}. The LDO regulator can be bypassed if the external supply to the device is from a 1.8 V power source. The regulator output to the internal circuitry may also be turned off when the device enters Stop mode to conserve power.

6.1. In-System Code Development for Lower Voltage Systems (below 2.7 V)

In a system that uses a 2.7–3.6 V supply voltage, the C8051F34A can be used as a substitute for the C8051T62x and the C8051T32x for in-system code development. However, if the supply voltage in the final system using the C8051T62x or C8051T32x is less than 2.7 V, it may be necessary to add additional circuitry to the prototype board when using the C8051F34A to prevent damage to other devices in the system. Any required additional circuitry will be dictated by the specifications of the other circuits in the system.

1. If all of the other circuitry in the system can also operate at 2.7 V or higher, raising the supply voltage for the entire system during development is an easy solution.
2. If the other devices cannot operate at a higher supply voltage but the I/O pins connected to the C8051F34A are tolerant of higher voltages, simply using a separate regulator for the C8051F34A may be an option.
3. If the I/O pins of the other devices in the system also cannot tolerate higher voltages, level-shifting circuitry may be necessary. An alternative to level shifters would be to use the C8051F34A's outputs in open-drain mode with an external pull-up resistor to the lower supply voltage. Be aware that this will result in extra supply current on the C8051F34A as well as slower rise times of the C8051F34A output signals.

6.2. Separate Voltages for V_{DD} and V_{IO}

The term V_{IO} refers to the Voltage Input/Output level selector pin. The C8051T620/T621/T622/T623/T326 devices have separate voltages for V_{DD} and V_{IO} in case the port input/output voltages are required to be different from the V_{DD} that the device is operating. For example, if V_{DD} is 1.8 V, the device can still interface to 3 V parts by supplying 3 V to the V_{IO} pin. If 3 V is applied to the V_{IO} pin, a logic high output on any port pin will then be 3 V.

In all V_{IO}-capable devices, the V_{IO} pin is required to be supplied a voltage for any port input/output. For applications where a separate V_{DD} from V_{IO} is not required, these two pins can be shorted together. The F34A does not have a V_{IO} pin. This will not affect designs from a software perspective but is important to remember when designing hardware.

6.3. Special Considerations for Higher Voltage Systems (>3.6 V)

The C8051T62x and C8051T32x devices can interface to logic levels that are higher than its supply voltage. However, special care must be taken in any system where the C8051T62x or C8051T32x interfaces to logic that uses a supply voltage higher than 3.6 V. The C8051T62x and C8051T32x I/O pins can only tolerate up to 3.6 V above the voltage present at the V_{DD} pin, or 5.8 V, whichever is lower. This means that when the device is powered off, and V_{DD} is 0 V, the maximum voltage on any I/O pin is 3.6 V. When V_{DD} is 2.2 V or higher, the maximum voltage at any I/O pin is 5.8 V. It may be necessary to either control the order in which power supplies turn on in the system or add external protection circuitry to ensure that the pin voltages remain within tolerable limits at all times.

6.4. 1.8 V Regulator

The internal LDO regulator is an additional feature of the C8051T62x and C8051T32x that is not found on the C8051F34A. The special function register, REG01CN, is used to control some of the regulator's features. The REG01CN register is located at address 0xC9 in the C8051T62x and C8051T32x. The corresponding register on C8051F34A devices is called REG0CN and is located at address 0xC9. There are bit differences between the C8051F34A and the C8051T62x and C8051T32x for this special function register. Because of this, extra care must be taken when writing to this location. Making the necessary changes to allow the code written for the C8051F34A to work properly on the C8051T62x or C8051T32x should be one of the final steps in the code development process.

For slower clock frequencies (<2 MHz), the amount of current consumed by the device can be reduced by setting the Memory Power Control bit (MPCE) in register REG01CN to 1. This setting allows the device to save power by only turning on the read buffers for the amount of time necessary to read the memory contents. Note that when this feature is enabled, the ADC should use a SAR clock divider of 2 or more for proper operation.

On the C8051T62x and C8051T32x devices, there are two versions of Stop mode (as opposed to one on the C8051F34A). The normal Stop mode leaves the internal regulator on and is identical to the C8051F34A Stop mode in that any reset source will be accepted and bring the device back out of Stop mode. The contents of RAM are retained if the regulator is left on in Stop mode. However, for additional power saving, the output of the regulator may also be disabled when the device enters Stop mode. Writing a 1 to the STOPCF bit in the REG01CN register enables this feature. Only a reset initiated by the $\overline{\text{RST}}$ pin or a power-on reset can wake the device from this mode. Note that the contents of RAM are lost if this option is used since power to the internal RAM is supplied by the regulator.

6.5. V_{DD} Monitor/Brown-Out Detector

The /RST monitor behaves in the same way across device families, but the voltage level at which the /RST monitor trips is lower on the EPROM devices. Details of these differences are shown in Table 4.

Table 4. VDD Monitor Differences

Parameter	C8051F34A	C8051T62x C8051T32x
Upper V_{DD} Monitor Threshold	2.7 V	1.8 V
V_{DD} Monitor ON after Power-on Reset	Yes	Yes

7. Suspend Mode and Related Features

The C8051T62x, C8051T32x, and C8051F34A have a power-saving mode called Suspend Mode, which is a function of the internal 48 MHz oscillator and is entered by setting the SUSPEND bit in the OSCICN register to “1”. When placed into suspend mode, the 48 MHz oscillator reverts to a very low-power state where it is no longer oscillating but can wake quickly and begin clocking the device again on certain events. The C8051T62x and C8051T32x devices are able to wake-up from multiple sources, while the C8051F34A will only wake on a non-idle USB event or VBUS interrupt. On the ‘T62x and ‘T32x devices, one of the new wake-up events is the port match feature, which allows the device to wake on specified logic states of Port 0 and Port 1 pins. If Timer 3 is running from an external oscillator source or the internal low-frequency oscillator, a Timer 3 overflow can wake the device from suspend mode. USB transceiver resume signalling can also wake the device from suspend mode. The C8051T620/T621/T320/T321/T322/T323 families have an additional wake-up event, which is a logic low output from Comparator 0.

Conversely, the C8051F34A devices are able to wake from suspend mode on a non-idle USB event or VBUS interrupt event, but the device does not implement the port match feature, the ability to run Timer 3 from the internal low-frequency oscillator, or the Comparator 0 wake-up feature.

8. Clocking Options

The clocking options on the C8051T62x and C8051T32x are very similar to those offered on the C8051F34A. The only exceptions (shown in Table 5) are that the C8051F34A includes an external crystal oscillator fed into a clock multiplier option (which is not available on the C8051T62x or C8051T32x) and that the C8051T62x/C8051T32x use an internal 48 MHz oscillator versus the 24.5 MHz oscillator of the C8051F34A.

Table 5. Clocking Options

Feature	C8051F34A	C8051T62x C8051T32x
Internal Calibrated 24.5 MHz oscillator (divided by 1, 2, 4, or 8)	Yes	No
Internal Calibrated 48 MHz oscillator (divided by 1,2,4, or 8)	No	Yes
Internal 80 kHz oscillator (divided by 1, 2, 4, or 8)	Yes	Yes
External CMOS clock (digital input)	Yes	Yes
External oscillator in RC or Capacitor mode	Yes	Yes
External oscillator in Crystal Oscillator mode	Yes	Yes
External oscillator fed into Clock Multiplier	Yes	No

Because the external oscillator fed into a clock multiplier option is not offered on the C8051T62x or C8051T32x, any port of an existing C8051F34A design that relies on an external oscillator multiplied should be modified to use another clocking option available on the C8051T62x or C8051T32x.

9. Prefetch Engine

When the prefetch engine is enabled on the 'T62x and 'T32x devices, the 'T62x and 'T32x devices will have timing similar to the C805F34A device with the FLRT bit set to “0”. By default, the prefetch engine is enabled. If the prefetch engine is disabled, the timing will be similar to the 'F320/326 devices.

10. SMBus, PCA, Timer 3, Port Match

The C8051T62x and C8051T32x device families implement some digital peripheral enhancements not found on the C8051F34A device family. Specifically, the SMBus, PCA, and Timer 3 peripherals all have additional features. The Port Match feature is found in the C8051T62x and C8051T32x families but not in the C8051F34A family.

The SMBus peripheral additions are an optional hardware address recognition and automatic ACK feature using the SMB0ADR and SMB0ADM registers. Using these features, the firmware required to handle SMBus transfers is reduced, and the software overhead associated with accepting or rejecting slave addresses is eliminated.

The PCA enhancements include more options for PWM generation using the PCA0PWM register. In addition to the standard 8 or 16-bit PWM options found on the C8051F34A family, the C8051T62x and C8051T32x families include 9, 10, and 11-bit PWM options in hardware.

Timer 3 has also been enhanced on the C8051T62x and C8051T32x families. In addition to the functionality found on the C8051F34A, Timer 3 can be clocked by the internal oscillator divided by eight. This can be used as a wake-up source for the MCU from suspend mode after an overflow occurs. The C8051T62x and C8061T32x families both have the low-frequency oscillator capture mode but do not have the USB start-of-frame capture mode of the C8051F34A family.

The Port Match feature can be found on the C8051T62x and C8051T32x and allows system events to be triggered by a logic value change on Port 0 or Port 1. Software-controlled values in PnMATCH specify the expected value in Port 0 and Port 1, and PnMASK individually selects which bits to check against PnMATCH. The Port Match feature can be used to generate interrupts or wake the device from a low-power mode. This feature is not found on the C8051F34A; so, code written to implement Port Match cannot be tested on the C8051F34A.

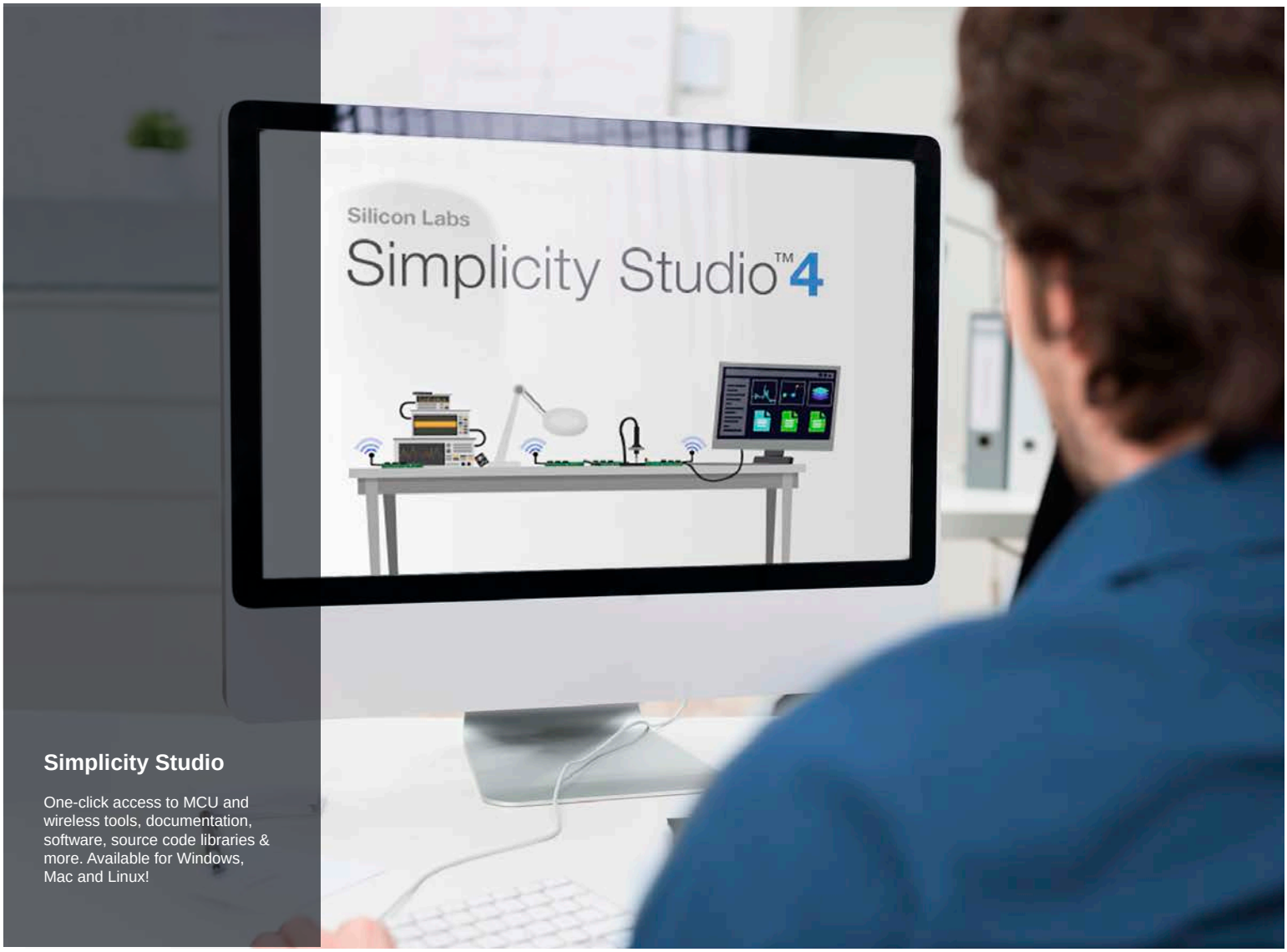
11. Other Peripherals

All other peripherals and features not discussed in the preceding sections are functionally the same between these device families. Code written for these peripherals will operate identically on all device families; therefore, there are no special considerations when developing code to utilize the other features.

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Updated Figure 1 on page 2.
- Added "9. Prefetch Engine" on page 9.



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