AN698

PCB DESIGN WITH AN EMBER® EM35X

(Formerly document 120-5060-000)

Silicon Labs provides a ZigBee product designer a number of paths towards the successful design of a ZigBee-compliant solution based upon Silicon Labs' EM300 Family of System on Chip (SoC) platforms. The lowest risk path begins with the purchase of an EM35x Development Kit (P/N: EM35X-DEV or EM35X-DEV-IAR). The Development Kit contains software, hardware, and documentation designed for developers to create applications efficiently on a tested and controlled platform. Once the design team is familiar with Silicon Labs' EM300 family of SoCs and EmberZNet PRO software, the next step in the design path involves designing application-specific hardware to meet the product requirements.

This application note is intended to accompany the Ember hardware reference designs and provide detailed information regarding the design decisions employed within them. In addition, it details the design guidelines for developing an application-specific, ZigBee design using an IC from the EM300 family. After reading this document, developers should be able to successfully implement a design involving the EM300 Series. For further information, visit www.silabs.com/zigbee-support.

New in This Revision

Rebranding for Silicon Labs.

Contents

1 Introduction

Due to the application-specific nature of the Ember hardware reference designs, Silicon Labs recommends that hardware designers familiarize themselves with each reference design available. Each EM35x reference design is bundled within the most recent release of Silicon Labs' EmberZNet PRO stack build, and each has been released to www.silabs.com/zigbee-support. This variety is intended to meet the design requirements for most ZigBee-based products and provides a lower risk and simplifies design and implementation.

Note: Due to the fact the EM351 and EM357 are pin-compatible, the EM35x Reference Designs can be used for either SoC. Also all EM35x Reference Designs are built on 4-layer, FR-4 material.

Silicon Labs has released the following EM35x-based Reference Designs:

- EM35x with a Ceramic Balun (EM35X_REF_DES_CER.zip)
- EM35x with Skyworks SKY65336/7 Front End Module (FEM) (EM35X_REF_DES_SKY6533X.zip)
- EM35x with RFMD RF6525 FEM (EM35X_ REF_DES_RF6525.zip)

Each Reference Design includes the following elements:

- Schematic (in .PDF and DX Designer formats)
- Schematic Netlist (in .ASC format)
- Bill of Materials (BOM)
- Layout file (Source in PADS 2005 and PADS 2007)
- Gerbers (in .PDF and .PHO formats)
- Layout Netlist (in .ASC format)
- Characterization data

While each Reference Design includes most of the information required to start an application-specific design, if there are additional items needed, visit the Customer Support portal at www.silabs.com/zigbee-support.

The next four sections of this document describe the RF guidelines in detail for each of the released reference designs. The remaining sections include items that are common to each of the EM35x reference designs.

2 EM35x with Ceramic Balun

Figure 1 illustrates a block diagram of the ceramic balun reference design.

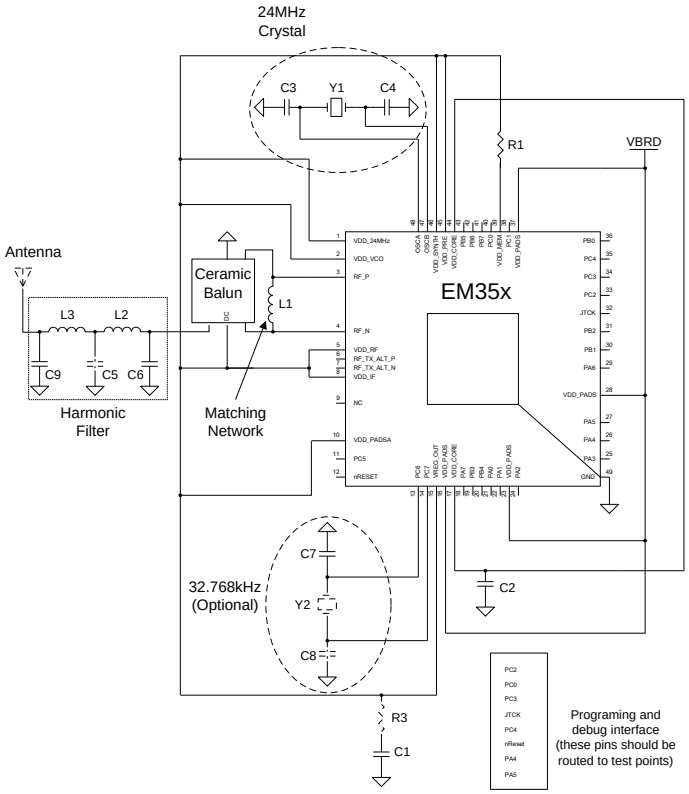


Figure 1. Block diagram of EM35x ceramic balun reference design

Silicon Labs' EM35x with ceramic balun reference design utilizes an external 0805 sized, ceramic balun as its primary RF component. A single inductor makes up the matching network and optimizes the RF performance. A five-element harmonic filter suppresses the conducted harmonics to below the FCC and ETSI limits.

Due to the market demand that ZigBee designs across all ZigBee profiles maximize their communication range, Silicon Labs has optimized their designs accordingly. In Boost mode, the EM35x ceramic balun design achieves a transmit output power close to 9 dBm across the 16 channels. This means the ceramic balun design can be used without external amplification in regions where regulations require the EIRP to be a maximum 10dBm, that is, EU countries.

This section describes the design decisions behind each of the items shown in Figure 1.

2.1.1 EM35x RF Ports

The EM35x's bi-directional RF port—RF_P (pin 3) and RF_N (pin 4)—provides access to a low noise amplifier (LNA) and a power amplifier (PA) through a shared differential interface. The disabled high-Z state of either the PA or the LNA allows transmitting and receiving through the shared port without the need for a conventional T/R switch.

An 'alternate' PA-only port—RF_TX_ALT_P (pin 6) and RF_TX_ALT_N (pin 7)—is also provided. This function is achieved via an additional PA. Design considerations for the alternate PA are not covered in this document.

Note: The on-chip parasitic capacitance is different between the two ports, which will alter the off-chip matching component values slightly.

2.1.2 Optimizing for TX (Boost Mode)

The EM35x Reference Design has been optimized for maximum transmitter (TX) output power in Boost mode using practical components and readily available printed circuit board (PCB) substrates. The optimum load at the PA on the silicon die is approximately 700 Ω when the PA/LNA device capacitance is resonated-out. This maximizes the voltage swing at the drains of the PA devices within the available supply voltage. Too large a load causes voltage limiting whereas too small a load does not make full use of the available supply voltage. Figure 2 illustrates a die level simulation of the load impedance and its effect on PA output power.

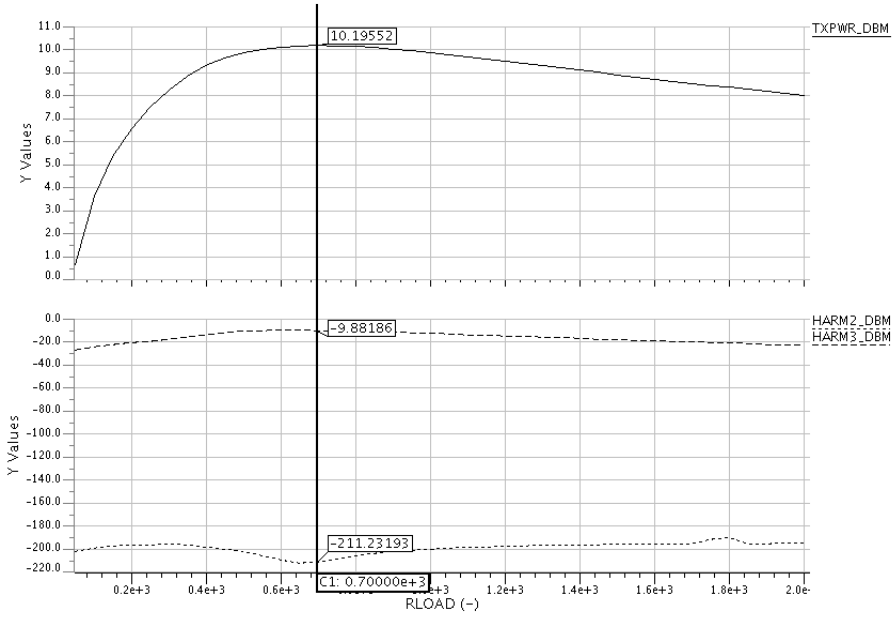


Figure 2. Simulated Boost output power with PA load resistance

Optimizing the TX output performance in Boost mode does not cause degradation in either Normal mode or RX Sensitivity. Because the receiver is CMOS-based, it amplifies the input signal voltage, rather than its current. The receiver noise is a fixed value of noise voltage that may be referred to its input. It might be expected that increasing the transformation would yield higher signal voltage swings at the LNA input, making the input referred noise less significant and thereby improving sensitivity. However, this also increases the source resistance, thereby increasing the source noise voltage. In practice at the 700Ω level, the improvement gradient is very small and the transmit output power exhibits far greater sensitivity to load variation than receiver sensitivity. The main objective for receive sensitivity is to minimize network loss, which is a common objective for transmit.

The optimum load presented to the pins of the EM35x SOC must take into consideration not only the optimum PA load but also on-chip parasitic capacitance and package bond-wire inductance. It is estimated that the optimum load presented to the pins is ***27 + j95 Ω*** (series impedance). This is equivalent to a parallel resistance of 368 Ω combined with a parallel inductance of 6.6nH.

Optimal Load for EM35x (series impedance)	27 + j95	Ohms

2.1.3 Matching Network Circuit Design

The term “matching” typically implies conjugate power matching. It is important to understand that the EM35x PA is *not* power matched according to the traditional definition. The term is used in this document to describe designing to optimal PA impedance.

The best way to understand Silicon Labs’ approach towards optimizing the EM35x “matching” is to plot the impedance of the ideal 700Ω PA load transformed by the chip/package parasitics on the Smith chart. The combination of the ideal load with the parasitics is the *conjugate* of the ideal load presented to the package pins. Knowing the combined load and its conjugate allows the designer to approach matching in a more traditional sense, namely, ‘How do we get to 50 Ω’?

It is also be necessary at some point in the network to include a balanced-to-unbalanced (balun) conversion. Use of a ‘proper’ balun has performance benefits related to common-mode suppression both on transmit and receive.

There are a variety of balun architectures and solutions available. The primary objective of any of the Ember hardware reference designs is to minimize design complexity and maximize time to market. Therefore, Silicon Labs decided to implement its primary reference design with a ceramic balun. The cost of ceramic baluns is low, and they are available from a number of vendors.

Ceramic baluns are available in 1:1 (50 to 50 Ω), 2:1 (100 to 50 Ω), and 4:1 ratios (200 to 50 Ω). Figure 3, Figure 4, and Figure 5 illustrate the ‘matched’ impedance normalized to these three ratios.

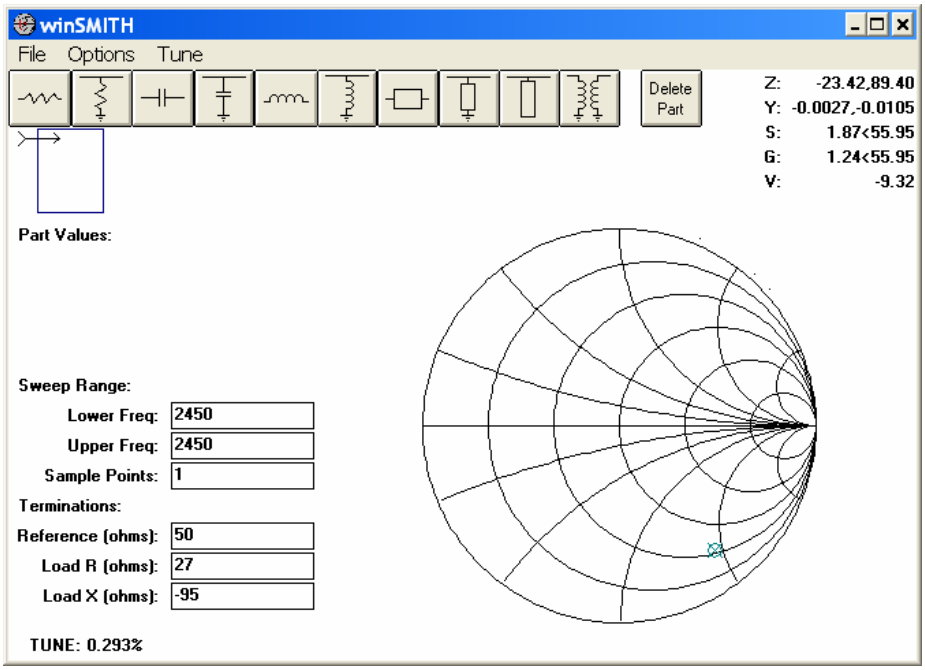


Figure 3. Conjugate of ideal EM35x load (normalized to 50 Ω)

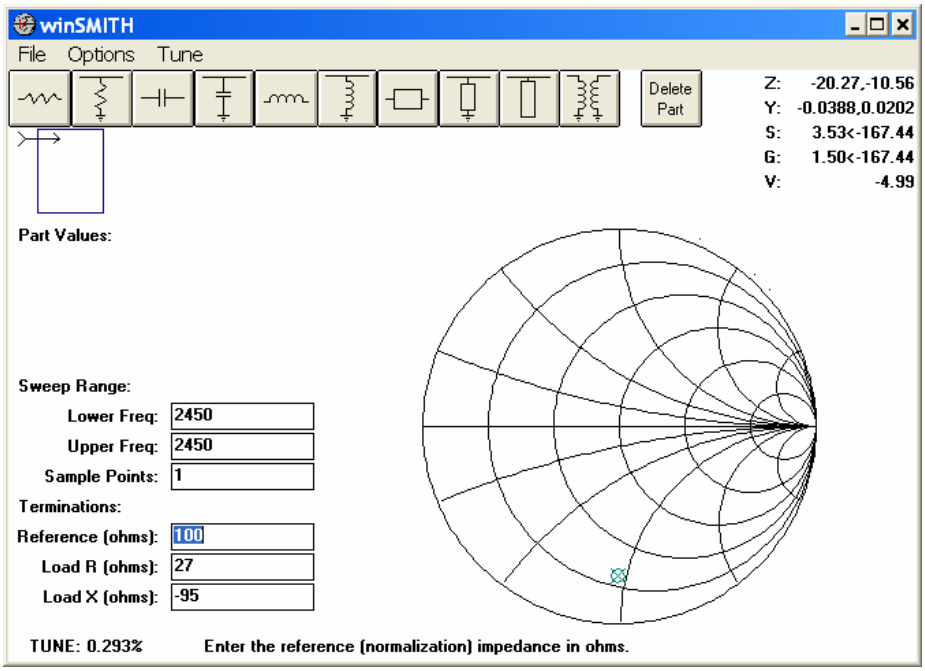


Figure 4. Conjugate of ideal EM35x load (normalized to 100 Ω)

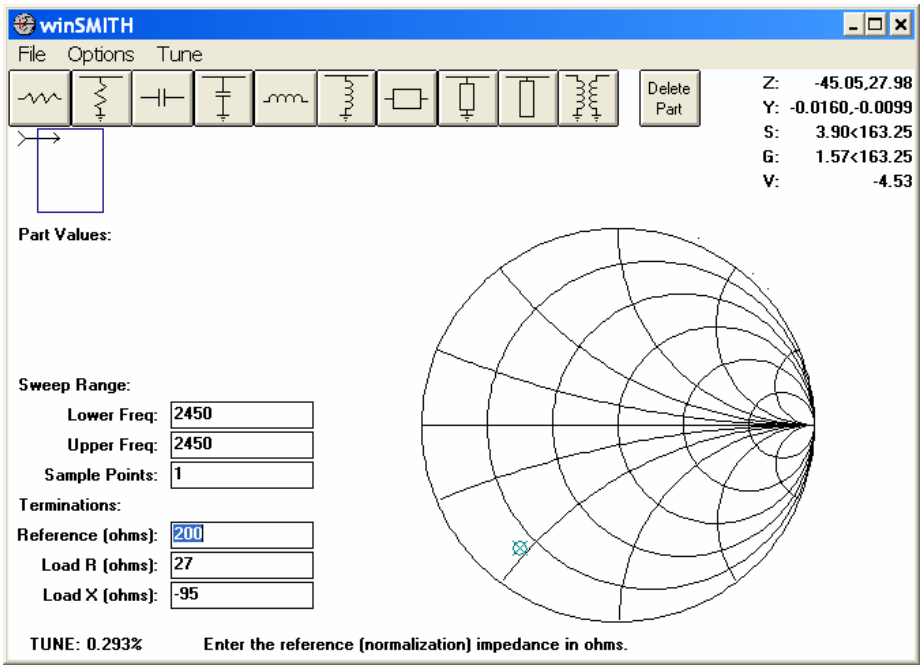


Figure 5. Conjugate of ideal EM35x load (normalized to 200 Ω)

The magnitude of the reflection coefficient, $|\Gamma_L|$, in these three cases is:

- 1:1 (50 Ω) → 0.8
- 2:1 (100 Ω) → 0.76
- 4:1 (200 Ω) → 0.8

This implies that a 2:1 ceramic balun should offer the lowest network loss, assuming identical balun loss because it requires the least transformation.

Investigation into ceramic balun performance from various vendors reveals that 1:1 and 2:1 ratio baluns often have about 0.3dB insertion loss advantage over a 4:1 ratio. Thus the 2:1 ceramic balun is preferred.

To minimize network loss, the matching topology should try to keep Smith chart loci towards the center of the Smith chart. To do that, the following impedance transformation options are available:

- Series inductance followed by Shunt capacitance
  - This option favors lower balun ratios.
  - It leads to comparatively large inductance values.
  - It requires either long PCB traces or two discrete inductors (balanced network) which means inductor Q becomes an issue.
- Series inductance followed by Shunt inductance
  - Akin to auto-transformer action.
  - Sweet-spot for 100 Ω balun if series inductance fabricated from PCB traces since not too long or too short.
- Shunt inductance followed by series capacitance
  - Not allowed because DC feed to PA is required from balun centre-tap.
- Shunt inductance followed by Series inductance
  - Favors lower balun ratios, but even at 1:1 the required series inductance is comparatively large.
  - It requires either long PCB traces or two discrete inductors (balanced network) which means inductor Q becomes an issue.

PCB parasitics play a part in the impedance transformation and that, even with the tightest of layouts, traces between the matching elements will add significant reactance at 2.4 GHz. In particular, there will be some series inductance between the package pins and the first matching element. This is significant when that element is in shunt because it cannot be absorbed into that reactance. Since this effect cannot be avoided, it is best to take advantage of it.

The lowest loss, least complex arrangement is ***series inductance followed by shunt inductance***. To make use of the PCB traces it must be recognized that they operate more like transmission lines, which travel slightly differently on the Smith chart compared with real inductors and this affects the shunt inductance value.

The Ember EM35x Ceramic Balun Reference Design uses 100 Ω traces which equate to 150µm wide on a 0.4 mm thick FR4 substrate. In the simple single-ended representation in WinSmith, the balanced pair must be modeled as a single 200Ω transmission line. Figure 6 illustrates the impedance transformation on a Smith chart.

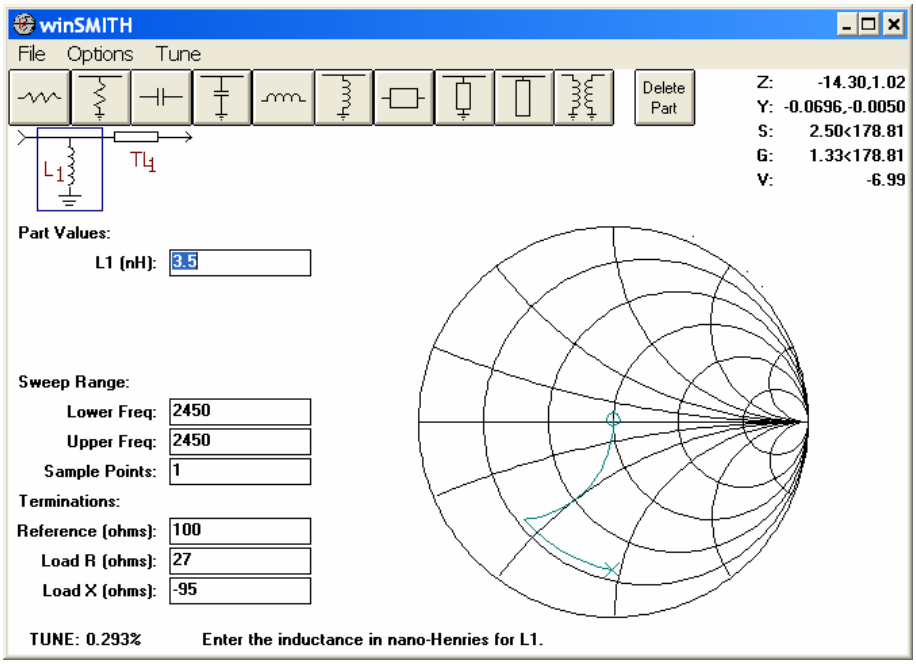


Figure 6. EM35x Ceramic Balun matching network

Figure 7 shows an extract of the EM35x Ceramic Balun Reference Design PCB layout (layer 1). It is important that the PCB designer notice the routes between the EM35x and the balun. Silicon Labs recommends the use of a 0603 inductor to allow ample space for the traces to go to the balun *first* with deterministic lengths. Trace inductance between the inductor and balun is then absorbed into the total shunt inductance, so it may be predictably offset by reducing the physical component value. The tuned value on the reference design came out to be 3.3 nH.

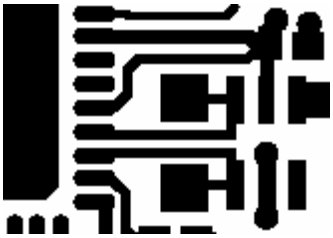


Figure 7. Layer 1 except showing the balun routes

The PCB designer has the option to route the traces to the inductor first and the balun second, but this has the effect of moving the components further away from the EM35x. By routing in this manner PCB area and cost are wasted. It also requires the model to be updated to a three-element match, generally making it more difficult to simulate.

An added benefit of using an 0603 inductor over an 0402 inductor is that better Q is obtainable. The EM35x Ceramic Balun Reference Design uses a Murata LQG18H series inductor which has a typical Q around 100 at 2.4GHz. Compare this to the commonly used LQP15M 0402 inductor, which has a typical Q around 50. This is worth nearly 0.2dB. The disadvantage is that it is not possible to get E24 values in 0603 style at these sorts of component values. So a small price is paid on design centering.

As previously mentioned, the balun center tap is fed with a 1.8V DC feed. A decoupling capacitor is required to define the common-mode RF potential. The balun decoupling capacitor needs to be as close as possible to the balun pins and with a high quality ground connection. Its value is chosen to be series resonant with its parasitic

inductance at 2.4GHz. While it would be possible to tune-out longer tracks by using a smaller capacitor value, this has the effect of making the decoupling more narrow-band, which can impact common-mode harmonic suppression. Therefore, Silicon Labs recommends that the EM35x layout is copied exactly in this area.

2.1.4 Harmonic Filter Design

FCC 15.35 allows for a duty-cycle relaxation to the regulatory limits. For EmberZNet PRO, the relaxation is 6.9 dB.

FCC 15.205 defines 'restricted bands' where harmonics must meet the levels set out in FCC 15.209. This is defined as -41.2 dBm/MHz up to 12.5 GHz. This applies to the 2nd, 3rd, and 5th harmonics, but not the 4th harmonic.

ETSI EN 300 440-1 requires spurious emissions to be less than -30 dBm/MHz, 1 GHz~24 GHz, so this becomes the default limit for the 4th harmonic.

Generally, if the FCC limits are met it is extremely unlikely that harmonics to 24 GHz would fail the ETSI requirements, so harmonics above the 5th will not be considered here.

The overall requirement is shown in Table 1.

Table 1. Harmonic power limits

Harmonic	Frequency	Limit
2nd	4810~4960MHz	≤-34.3 dBm/MHz
3rd	7215~7440MHz	≤-34.3 dBm/MHz
4th	9620~9920MHz	≤-30.0 dBm/MHz
5th	12025~12400MHz	≤-34.3 dBm/MHz

Figure 8 shows a network analyzer measurement of a 3-pole low-pass filter using 1p0, 2n7, 1p0. Murata LQP15M (0402) series inductors were used.

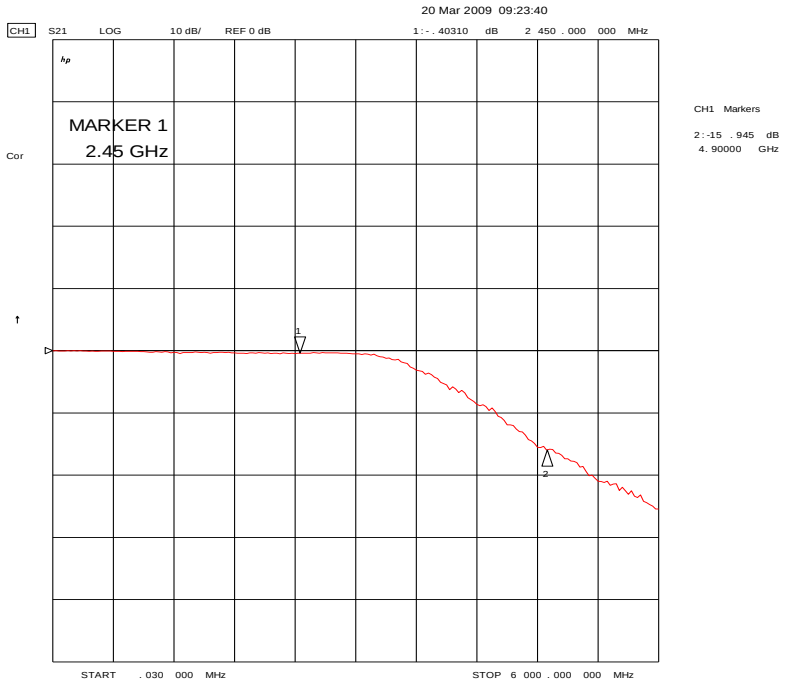


Figure 8. 3-pole Harmonic Filter performance

Figure 8 indicates the 3-pole filter can attenuate the 2nd harmonic by 15 dB. Initially this seems just enough, when you consider that the 2nd harmonic is typically -20 dBm in Boost mode, that is, -35 dBm plus any per MHz measurement benefit. However, this leaves little room for performance spread and in practice it was found that the aggregate harmonic levels were higher than expected. The higher harmonic levels were from practical layout effects (that is, the ground plane itself is not necessarily at zero RF potential at any point), and also because the PA's source impedance is not conjugately matched, so the filter is effectively mismatched.

To guarantee regulatory conformance it was decided that a 5-pole filter was needed. There is no real advantage in reducing to 4-poles because most of the loss resides in the inductors. Additionally, the 5-pole version yields more convenient values, which are 1p0, 2n7, 1p8, 2n7, 1p0. A network analyzer plot of a version using Murata LQP15M series inductors is shown in Figure 9.

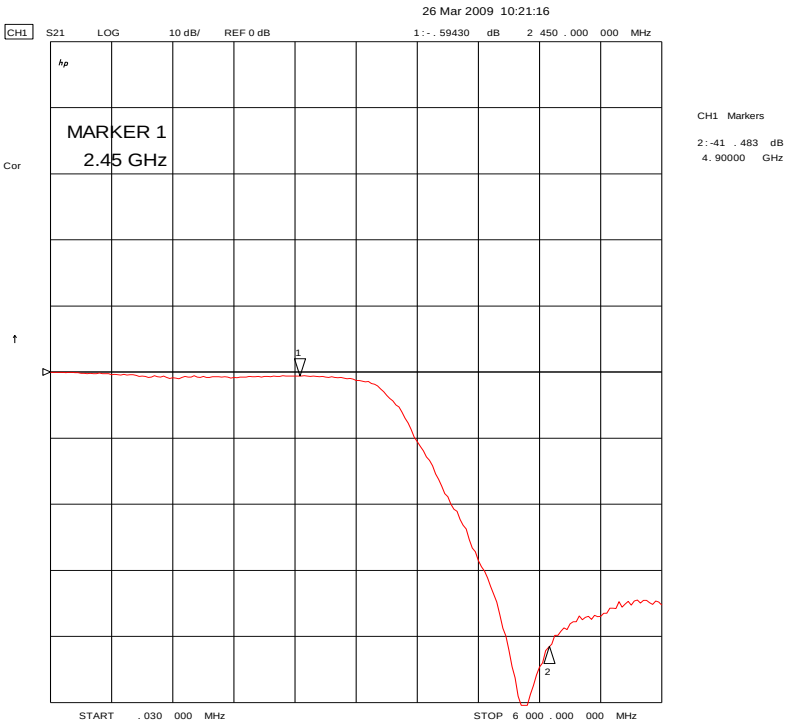


Figure 9. 5-pole Harmonic Filter Performance (with multi-layer inductors)

The same filter with Murata LQW15A (0402 wire-wound) series inductors is shown in Figure 10.

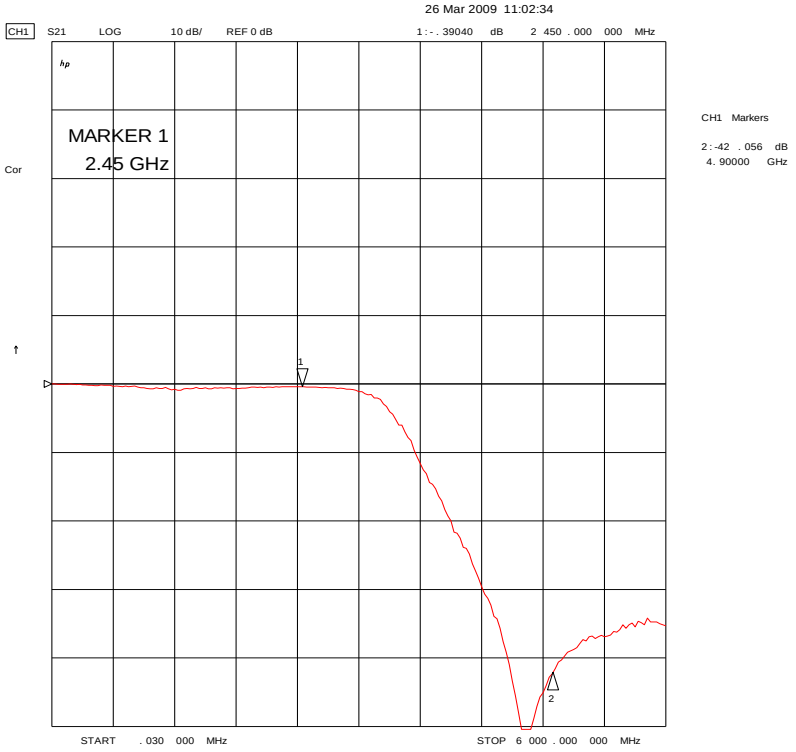


Figure 10. 5-pole Harmonic Filter Performance (with wire wound Inductors)

Comparing Figure 9 and Figure 10 indicates that there is a 0.2 dB penalty to using the LQP15M series inductors.

The position of the stop-band notch is controlled by the capacitor values together with ground via inductance. The above plots were recorded on boards that use one ground via per shunt capacitor.

Figure 11 plots the same LQW15A, 5-pole filter with two ground vias per capacitor.

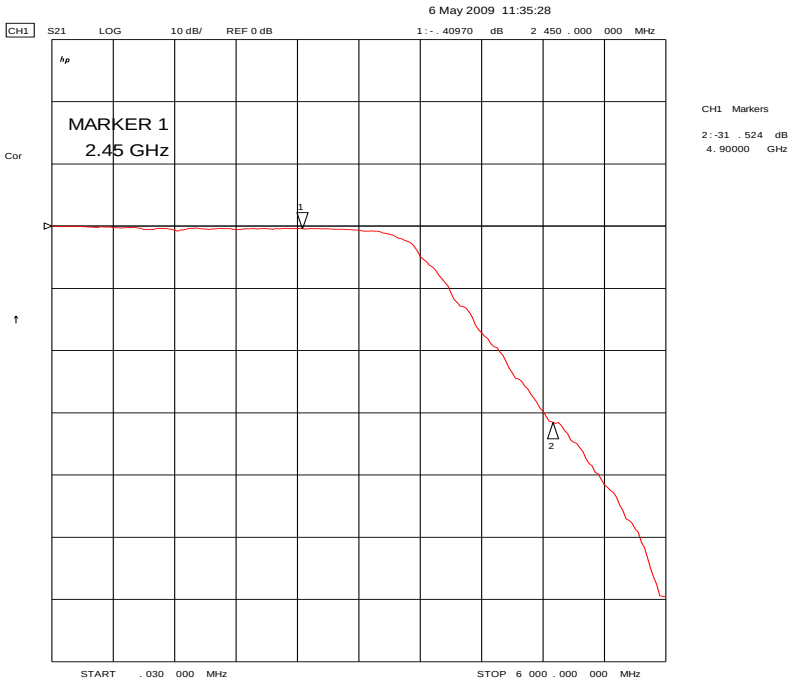


Figure 11. 5-pole Harmonic Filter performance (with two GND vias / shunt capacitor)

The loss is virtually identical but the stop-band notch has been moved to a higher frequency. The recommended filter layout uses double vias to diminish any PCB variations.

The effect of component tolerance can only be investigated by simulation. Generally for the small values of capacitance used in the filter there is a choice between ±0.25 pF and ±0.1 pF. Figure 12 and Figure 13 demonstrate the effect of capacitor tolerance on the in-band insertion loss. This was simulated within Eldo RF using a 100 run Monte Carlo simulation using uniform distributions. The inductors were fixed using Murata's S-parameter files.

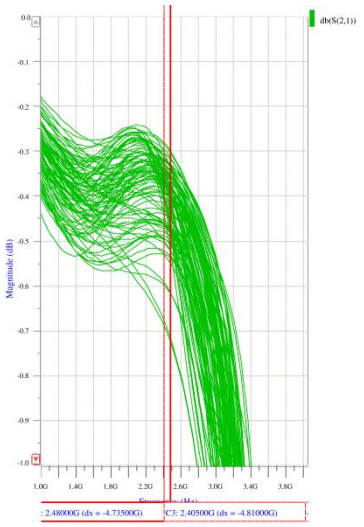


Figure 12. Filter Pass Band performance with +/- 0.25pF capacitor tolerance

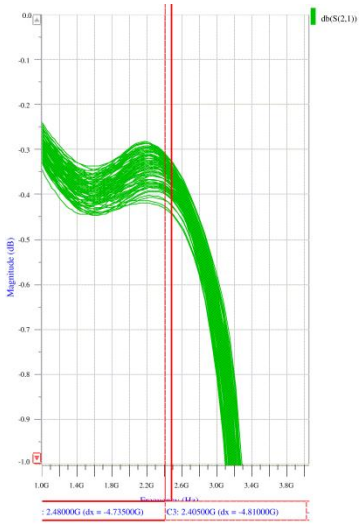


Figure 13. Filter Pass Band performance with +/- 0.1pF capacitor tolerance

A variation of 0.4 dB is considered unacceptable so the ±0.1 pF tolerance components are recommended.

Figure 14 shows the stop-band variation for the ±0.1 pF tolerance case with markers at the 2nd and 3rd harmonics. Clearly stop-band variation for a 5-pole filter is not a tolerance concern.

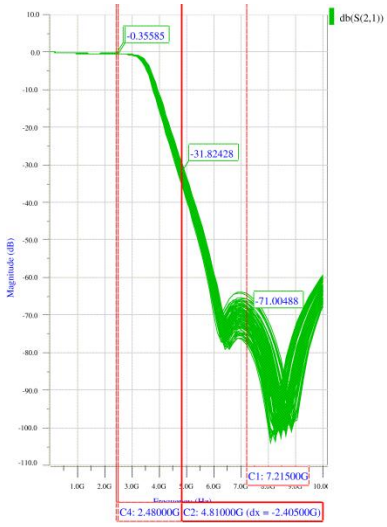


Figure 14. Harmonic Filter stop band performance

There are in fact three tolerance choices for the Murata LQW15A 2.7 nH inductors: ±0.1 nH (3.7%), ±0.2 nH (7.4%), ±0.5 nH (18.5%). To investigate these tolerances the S-parameter representations were replaced with lumped elements, which affect the shape slightly. Figure 15, Figure 16, and Figure 17 demonstrated the passband sensitivity to inductor tolerance.

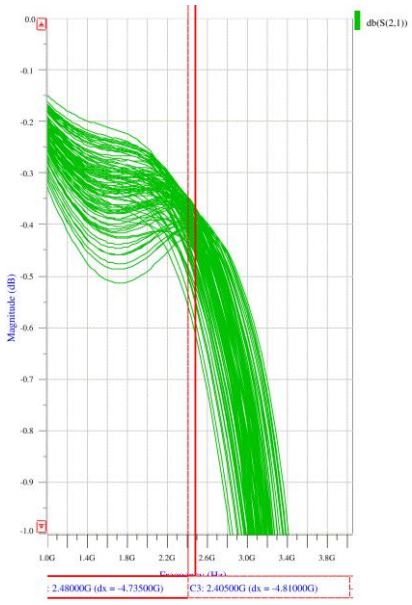


Figure 15. Filter passband performance with +/-0.5 nH tolerance

Figure 16. Filter passband performance with +/-0.2 nH tolerance

Figure 17. Filter passband performance with +/-0.1 nH tolerance

The simulations indicate that 0.03dB variation or less is achieved with ±0.2 nH inductors, which are recommended in the EM35x Ceramic Balun Reference Design. There seems little need to use ±0.1 nH tolerance, whereas 0.25 dB variation from the ±0.5 nH inductors is too much variation.

Figure 18 shows the aggregate performance with ±0.1 pF capacitors and ±0.2 nH inductors.

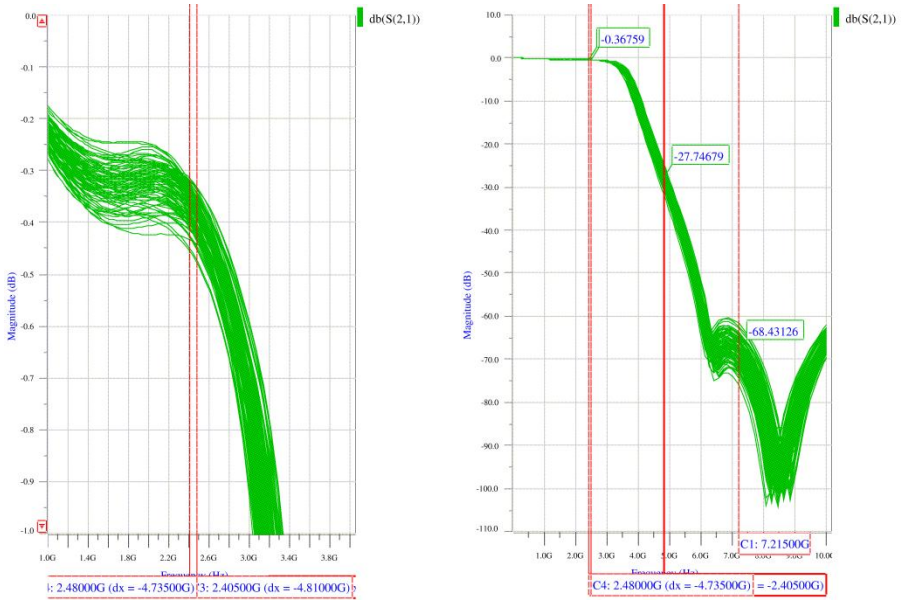


Figure 18. 5-Pole Harmonic Filter, Monte Carlo simulation

Another choice that must be made is whether or not to use high-Q capacitors. This was investigated by comparing the filter response with Murata's general purpose GRM series capacitors and their high-Q GJM counterparts. This was done by using Murata's S-parameter data. Note that PCB parasitic effects have been removed from this simulation. Figure 19 illustrates the difference between the two capacitor series.

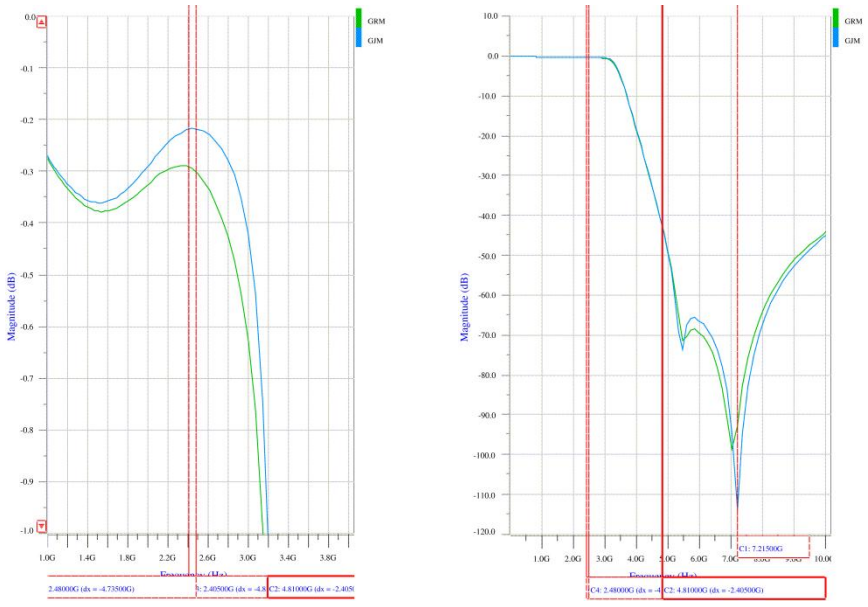


Figure 19. General purpose vs. High Q capacitor performance

The EM35x Ceramic Balun Reference Design specifies high-Q capacitors to achieve the best performance, but 0.1 dB may not be considered cost-effective in production designs.

2.2 RF Layout Guidelines

At 2.4 GHz it does not take much for a poorly designed PCB to build up enough parasitic reactance to noticeably compromise RF performance. The following notes describe how the PCB design was implemented and some of the pitfalls that could arise in transferring the design to a product.

2.2.1 Layer 1-2 Thickness

Because the EM35x Ceramic Balun Reference Design was principally designed to allow characterization of the EM35x, an SMA style RF connector was preferred. This has driven decisions on PCB layer 1-2 thickness because of the land pattern width required for the center-pin. It is preferable to be able to merge this land pattern within the width required for 50 Ω microstrip to maintain line impedance accuracy. The smallest pin width SMA available was the Emerson 142-0701-851 connector that has a flat tab center pin of width 0.51 mm. To simplify soldering this leads a minimum width of 0.6 mm.

In addition, choosing a width that allows the harmonic filter's 0402 footprints to be merged into the 50 Ω track width is also beneficial. A minimum width of 0.6 mm also achieves this.

The reference design PCB is fabricated using conventional FR4 material to demonstrate realistically achievable performance. FR4 would traditionally be expected to have a dielectric constant (εr) of 4.5, but a review of various manufacturers' materials at 2.4 GHz shows that on average it is about 4.0.

Microstrip width calculators are widely available on the internet (for example, http://emclab.mst.edu/pcbtlc2/microstrip/). Using a copper thickness of 35 µm (1oz), a minimum width of 0.6 mm requires a board thickness of 0.33 mm for a 50 Ω trace. To use a commonly available core thickness, it was decided to increase this to 0.4 mm (16-mil), increasing the required trace width to 0.75 mm.

2.2.2 Matching Network

The traces between the balun and the EM35x have a length and width that has been carefully optimized for 0.4 mm thick FR4, as discussed in the section "Matching Network Circuit Design." While it would be possible to reduce layer 1-2 thickness to 0.2 mm (8-mil), this reduces these trace widths to less than most PCB manufacturer's minimum track width capability (usually 3-mil or 75 µm). This would then lead to higher line characteristic impedance and a different line length. In addition, any parasitic capacitance from fixed size footprints would increase. Considerable simulation and/or PCB experimentation would then be required to achieve optimum performance.

This circuit area exhibits the greatest sensitivity to PCB variations, deliberate or otherwise. Therefore, Silicon Labs highly recommends that the PCB layout is copied exactly.

2.2.3 Harmonic Filter

The benefit of making the microstrip width at least as wide as the 0402 footprint width is that the 0402 pad does not then appear as a parasitic capacitance. This is especially useful when replacing the filter with 0Ω links to test unfiltered performance because line discontinuities are minimized. The spacing between components is also important because this can affect parasitic inductance in series with the lumped inductors. In fact, the layout design has taken advantage of this because 2.7 nH is very slightly smaller than ideal. Changing the layout, for example by turning a corner with the inductor, may therefore lead to poorer performance.

Grounding is crucial in obtaining satisfactory performance from the harmonic filter. The working assumption is that the ground-plane is at zero RF potential at any point on its surface. This would be true of an infinite extent ground plane, but isn't necessarily true on practical PCBs where there may be ground keep-outs and components close to the edge of the PCB. This is a common problem on PCBs that add a surface mount antenna, where ground must be relieved to allow the antenna to work properly. There needs to be enough ground 'mass' for the filter grounds to connect to, so placing the capacitors at the edge of a keep-out area is likely to affect performance.

The harmonic filter is laid-out with the first capacitor on the opposite side to the other two capacitors. This is critical to 2nd harmonic performance. Silicon Labs discovered that the first capacitor earth return needs to be close to the balun decoupler's earth return. Silicon Labs has proven that the top-side ground plane does not play a part in this effect. It seems most likely that the layer 2 ground dimensions are such that it is not quite the same ground potential at every location at the 2nd harmonic.

A general RF engineer's rule of thumb is that top-side ground should be at least three microstrip widths away from a microstrip trace. In commercial cost-sensitive designs this wastes too much PCB space and the EM35x Reference Design uses just a single width clearance. It has negligible effect on the line impedance. Nonetheless, it indicates the sphere of influence that the microstrip EM-field covers and where you may need to keep other tracks and components out of.

It is acceptable not to have a top-side ground, and this is preferable to having multiple small islands of ground. The EM35x Reference Design includes it mainly to help with experimentation. If a top-side ground is included, it must be adequately tied to layer-2 ground and not just at the fundamental frequency. This requires ground vias on a grid spacing that is smaller than 1/8th wavelength at the highest frequency of interest. The Radio Communications Module (RCM) uses a grid spacing of approximately 1.2 mm. It is vital that these vias run close to the edge of the copper adjacent to the microstrip. Otherwise the microstrip can excite the floating edge.

2.2.4 PCB Tolerance

Volume manufacturing requires the least expensive materials to be used while meeting an acceptable level of performance. The effects of component choice have already been discussed, but the PCB also plays a major part in the matching network and so you must consider its performance.

For the types of cost-sensitive applications targeted, a low-cost PCB substrate is mandatory, which means standard FR4. But within the FR4 classification there are cost trade-offs to be made against:

- Dissipation Factor, DF (also known as loss tangent, tanδ)
- Dielectric Constant, DK (also known as relative permittivity, εr)

Generally, materials are split into 'standard loss' and 'low loss' categories, with a corresponding cost penalty. Other product considerations such as flammability rating and lead free assembly will narrow these choices. These are beyond the scope of this document.

Modern PCB manufacturing achieves very accurate etching and so this is not considered as a performance variable. Z-axis expansion is really a function of the FR4 material and does not alter much between vendors' material.

Silicon Labs ran simulations in Eldo RF to investigate DF and DK variation, shown in Figure 20. Since the harmonic filter is modeled using S-parameters, it was replaced with 20 mm of 50 Ω track so that its PCB-based loss was included. The simulation measured S21 with the PA end terminated in the ideal 700 Ω load. As such it does not take into account the additional PA power variation with load resistance, which will add to the indicated loss.

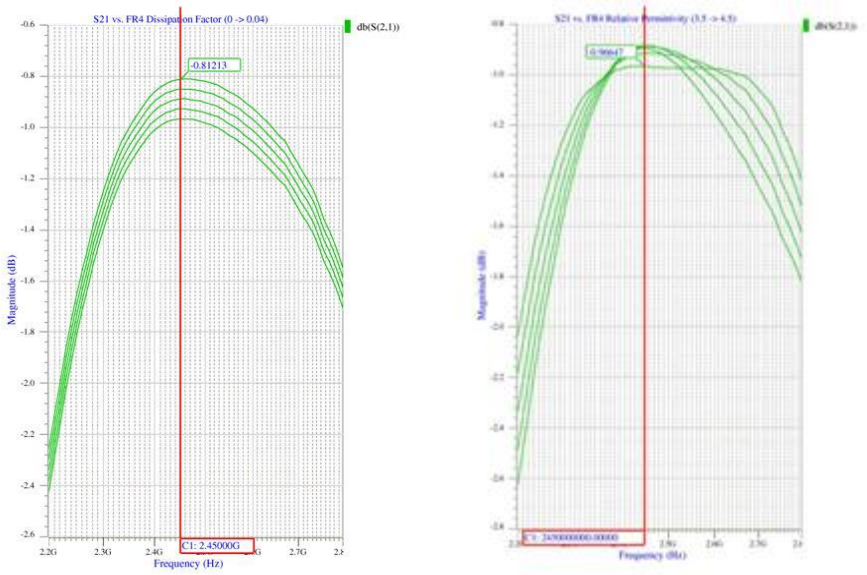


Figure 20. Effect of FR4 DF and DK variation

The simulations show that there is about 0.06 dB difference between a DF of 0.01 and 0.025. DK is more sensitive and there is nearly 0.1 dB difference between a DK of 3.5 and 4.0.

Silicon Labs recommends that the DK be 4.0±5% at or near 2.4 GHz. Note that the DK for FR4 typically reduces with increasing frequency, so the value at 1MHz cannot be used reliably.

A DF value of 0.025 does not appear to add any noticeable loss compared with low loss materials at the 0.01 level, so this is the recommended limit.

The recommended values for DF and DK encompass the majority of low cost FR4 materials available.

2.3 Other Design Considerations

Please refer to the section Non-RF Design Considerations for the non-RF requirements of the EM35x-based design.

3 EM35x with SKY6533X FEM Reference Design

3.1 RF Design Guidelines

To obtain the maximum allowable transmit power from a ZigBee system, Silicon Labs and Skyworks jointly specified a Front End Module (FEM) optimized for Silicon Labs' ZigBee SoCs. With the specification, Skyworks developed two FEMs, the SKY65336 and the SKY65337. These pin compatible designs offer ZigBee designers a unique opportunity to test their ZigBee enabled product with (SKY65336) or without (SKY65337) a Low Noise Amplifier (LNA).

To assist designers interested in the EM35x and SKY6533X solution, Silicon Labs developed a reference design around this two-chip solution. Figure 21 illustrates the Typical Application circuit of the reference design.

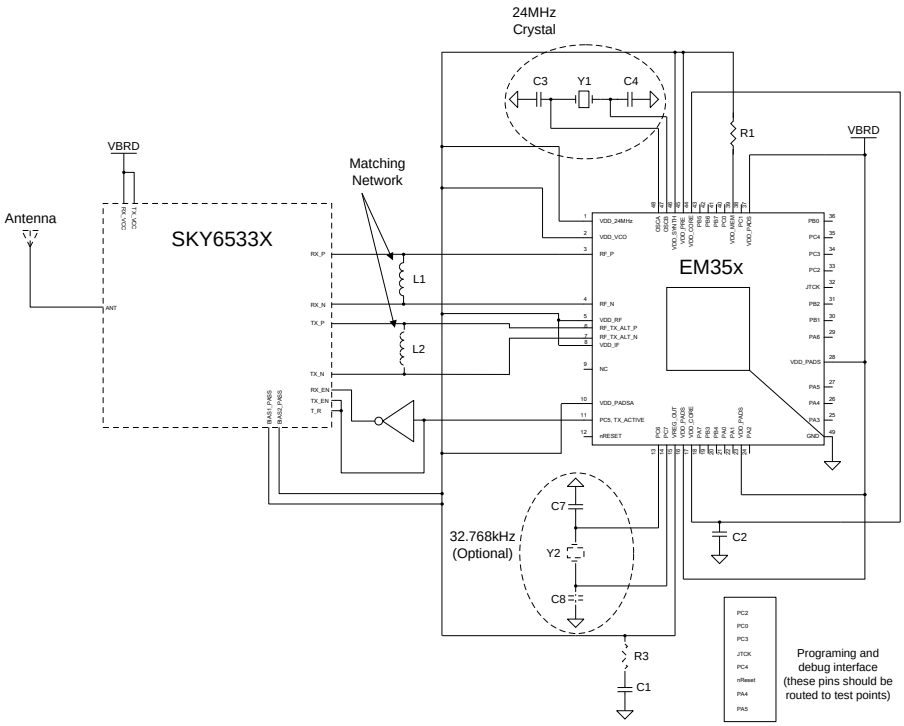


Figure 21. Block Diagram for the EM35x and Skyworks FEM

For detailed descriptions of the FEMs, please refer to Skyworks datasheets for the SKY65336 and SKY65337 chips.

- SKY65336 URL: http://www.skyworksinc.com/Product.aspx?ProductID=369
- SKY65337 URL: http://www.skyworksinc.com/Product.aspx?ProductID=370

3.1.1 EM35x RF Ports

The EM35x's bi-directional RF port—RF_P (pin 3) and RF_N (pin 4)—provides access to a low noise amplifier (LNA) and a power amplifier (PA) through a shared differential interface. The disabled high-Z state of either the PA or the LNA allows transmitting and receiving through the shared port without the need for a conventional T/R switch.

An 'alternate' PA-only port—RF_TX_ALT_P (pin 6) and RF_TX_ALT_N (pin 7)—is also provided. This function is achieved via an additional PA. The on-chip parasitic capacitance is different between the two ports, which will alter the off-chip matching component values, L1 and L2, slightly.

3.1.2 Optimizing for TX (Normal Mode)

The EM35x with SKY6533X Reference Design has been optimized for maximum transmitter (TX) output power in normal mode using practical components and readily available printed circuit board (PCB) substrates. The optimum load at the RF_TX_ALT ports of the EM35x silicon die is approximately 700Ω when the integrated PA/LNA device capacitance is resonated-out. This maximizes the voltage swing at the drains of the integrated PA devices within the available supply voltage. Too large a load causes voltage limiting whereas too small a load does not make full use of the available supply voltage.

Therefore, in order to maximize the TX power from the SKY6533X / EM35x reference design, Silicon Labs placed shunt inductor across the RF_TX_ALT differential ports. This inductance resonates with the parasitic capacitance of the EM35x package as well as the RF Traces and allows for a +3 dBm signal to be present at the TX port of the SKY6533X device.

3.1.3 Optimizing for RX (Normal Mode)

To minimize the RX path loss between the SKY6533X and the EM35x device, Silicon Labs has placed a shunt inductor across the differential RF input port. The value of the inductor was varied until the optimum RX Sensitivity (1% PER, 20 byte packet) was determined.

3.2 Antenna Port of SSKY6533X FEM

The Antenna port of the SKY6533X FEM presents a 50Ohm, single-ended impedance in order to connect to standard, off-the-shelf, singled port, 2.4 GHz antennas. Silicon Labs recommends the HW designer follow any and all application notes around their antenna of choice in order to maximize efficiency and directivity.

3.3 Digital Control of SKY6533X FEM

To control the configuration modes of the Skyworks FEM, Silicon Labs recommends using the TX_ACTIVE (PC5) and an inverting gate to drive TX_EN and RX_EN.

To put the FEM into deep sleep, both TX_EN and RX_EN must be driven low. This can be accomplished in a variety of ways. Silicon Labs recommends controlling the VDD input of the inverter with a second GPIO as well as adding a pull down resistor (10k) to the output of the inverter. When DEEP_SLEEP mode is initiated, the VDD can be disconnected from the inverter. The pull-down resistor would drive RX_EN low, and the EM35x in sleep mode would drive TX_EN low.

4 EM35x with RF6525 FEM

4.1 RF Design Guidelines

To obtain the maximum allowable transmit power from a ZigBee system, Silicon Labs and RFMD jointly specified a Front End Module (FEM) optimized for the EM35x family of SoCs. With the specification, RFMD developed one FEM, the RF6525. The RF6525 contains a Power Amplifier (PA), Low Noise Amplifier (LNA), integrated balun, RX/TX Switch for RF as well as a diversity switch for use with applications that require antenna diversity. In addition, the RF6525 allows designers a unique opportunity to characterize their design both with and without an LNA. This is due to the integrated LNA bypass mode.

To assist designers interested in the EM35x and RF6525 solution, Silicon Labs developed a reference design around this two-chip solution. Figure 22 illustrates the Typical Application circuit of the reference design.

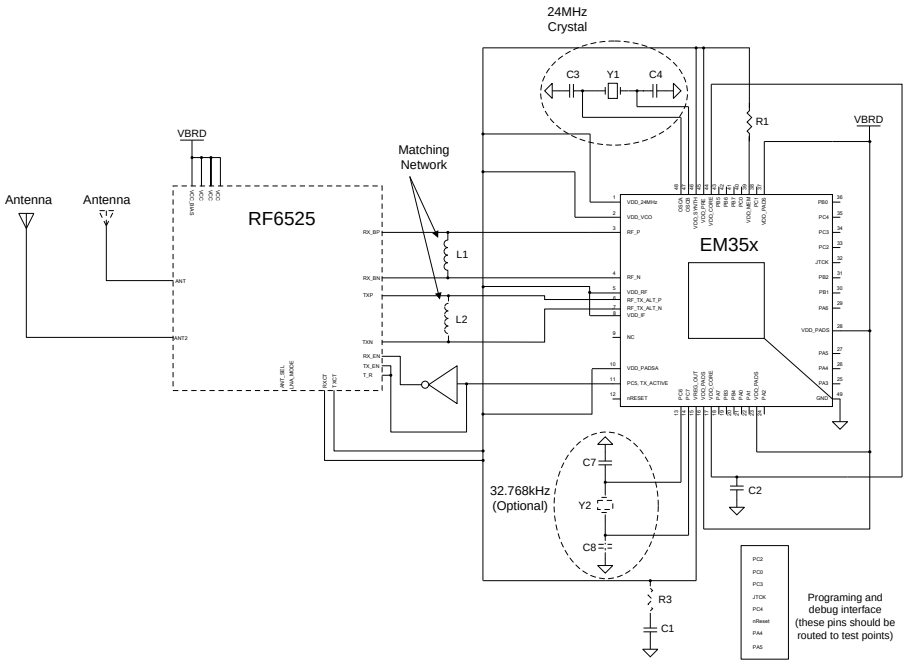


Figure 22. Block Diagram for the EM35x and RFMD FEM

For detailed descriptions of the FEMs, please refer to the datasheet for the RF6525 on the RFMD website.

RF6525 URL: https://estore.rfmd.com/RFMD_Onlinestore/Products/RFMD+Parts/PID-P_RF6525.aspx

4.1.1 EM35x RF Ports

The EM35x's bi-directional RF port—RF_P (pin 3) and RF_N (pin 4)—provides access to a low noise amplifier (LNA) and a power amplifier (PA) through a shared differential interface. The disabled high-Z state of either the PA or the LNA allows transmitting and receiving through the shared port without the need for a conventional T/R switch.

An 'alternate' PA-only port—RF_TX_ALT_P (pin 6) and RF_TX_ALT_N (pin 7)—is also provided. This function is achieved via an additional PA. The on-chip parasitic capacitance is different between the two ports, which will alter the off-chip matching component values, L1 and L2, slightly.

4.1.2 Optimizing for TX (Normal Mode)

The EM35x with RF6525 FEM Reference Design has been optimized for maximum transmitter (TX) output power in normal mode using practical components and readily available printed circuit board (PCB) substrates. The optimum load at the RF_TX_ALT ports of the EM35x silicon die is approximately 700Ω when the integrated PA/LNA device capacitance is resonated-out. This maximizes the voltage swing at the drains of the integrated PA devices within the available supply voltage. Too large a load causes voltage limiting whereas too small a load does not make full use of the available supply voltage.

Therefore, in order to maximize the TX power from the RF6525 / EM35x reference design, Silicon Labs placed shunt inductor across the RF_TX_ALT differential ports. This inductance resonates with the parasitic capacitance of the EM35x package as well as the RF Traces and allows for a +3dBm signal to be present at the TX port of the RF6525 device.

4.1.3 Optimizing for RX (Normal Mode)

To minimize the RX path loss between the RF6525 and the EM35x device, Silicon Labs has placed a shunt inductor across the differential RF input port. The value of the inductor was varied until the optimum RX Sensitivity (1% PER, 20 byte packet) was determined.

4.2 Antenna Port of RF6525 FEM

The Antenna port of the RF6525 FEM presents a 50Ohm, single-ended impedance in order to connect to standard, off-the-shelf, singled port, 2.4GHz antennas. Silicon Labs recommends the HW designer follow any and all application notes around their antenna of choice in order to maximize efficiency and directivity.

4.3 Digital Control of RF6525 FEM

To control the configuration modes of the RFMD FEM, Silicon Labs recommends using the TX_ACTIVE (PC5) and an inverting gate to drive TX_EN and RX_EN.

To put the FEM into deep sleep, both TX_EN and RX_EN must be driven low. This can be accomplished in a variety of ways. Silicon Labs recommends controlling the VDD input of the inverter with a second GPIO as well as adding a pull down resistor (10k) to the output of the inverter. When DEEP_SLEEP mode is initiated, the VDD can be disconnected from the inverter. The pull-down resistor would drive RX_EN low, and the EM35x in sleep mode would drive TX_EN low.

5 Non-RF Design Considerations

To operate properly, each of the EM35x Reference design contains additional, non-RF components. These include a 24 MHz crystal, appropriate decoupling capacitors and RF test point as well as a Packet Trace Port connector.

5.1 High-frequency (24 MHz) Crystal Reference (Y1, C11, and C12)

The EM35x requires a single, accurate 24 MHz crystal source in order to develop the proper EM35x clock distribution and IEEE 802.15.4 timing (see Figure 23).

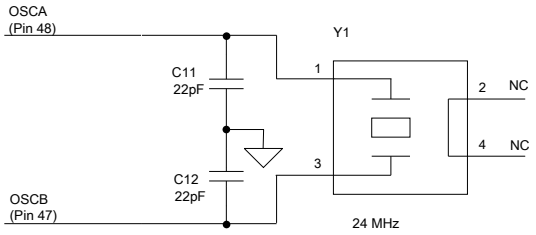


Figure 23. 24 MHz high-frequency crystal

Silicon Labs recommends that the shunt loading capacitors, C11 and C12, be located fairly close together and share a common ground via. The shunt capacitors and the crystal form a resonant circuit with a reasonably high Q, so the circulating currents are high. As a result, despite only consuming 1mA (for example), the circulating current through the shunt caps may be several mA. If the grounds of the capacitors are widely separated, this several mA loop current has to flow through the ground plane to get between the two capacitors. The high current causes voltage to be developed due to the via inductance, as well as potentially inducing a voltage in the ground plane. Bringing the capacitors together means the majority of the loop current flows in surface tracks—only imbalance current flows to ground, which should be small if the signal across the crystal is symmetric and sinusoidal. Whether this really makes a difference or not is difficult to say, and capacitors are commonly taken to ground separately.

However, the crystal is very near the RF and the VCO in particular, and 24MHz tones of the VCO are very detrimental, so the problem is best avoided.

Due to the timing requirements of the IEEE 802.15.4-2003 Standard, this crystal must meet an accuracy of +/- 40ppm over tolerance, temperature, and aging as listed in Table 3. In addition, the crystal must have a maximum ESR of 60Ω to control the integrated oscillator signal strengths.

A manufacturing token within the EM35x stores the crystal bias register setting. This setting is automatically determined during PCB manufacturing test when Silicon Labs' RangeTest or MFG Library SW is used, and it is dependent upon the crystal chosen. For more information on this token, refer to Document AN710, *Bringing Up Custom Devices for the EM35x SoC Platform*. Loading capacitors C11 and C12 should be chosen according to the crystal manufacturer's requirements, then optimized during characterization to minimize the normalized frequency offset. The EM35x Ceramic Balun reference design has been optimized with 11pF (two 22pF capacitors) even though the crystal specifies 18pF loading capacitance.

Table 2. High Frequency Crystal Requirements

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Frequency			24		MHz
Duty cycle		40		60	%
Phase noise from 1 kHz to 100 kHz				- 120	dBc/Hz
Accuracy	Initial, temperature, and aging	- 40		+ 40	ppm
Crystal ESR	Load capacitance of 10 pF			100	Ω
Crystal ESR	Load capacitance of 18 pF			60	Ω
Start-up time to stable clock (max. bias)				1	ms
Start-up time to stable clock (optimum bias)				2	ms

5.2 Optional Low-frequency Crystal Reference (Y2, C9 and C10)

The EM35x contains an integrated sleep timer that allows for SW configuration of sleep/wake cycles of the wireless node. There are two options for driving the sleep timer: a 32.768 kHz crystal oscillator or an internal RC oscillator. The crystal oscillator is more accurate but consumes more current than the RC oscillator. The RC oscillator is sufficient for operating the EmberZNet PRO stack. Therefore, the application's sleep timing accuracy will decide if a 32 kHz crystal is required.

Figure 24 illustrates the crystal oscillator with its loading capacitors. To reduce the effects of overdriving the oscillator circuit within the EM35x, Silicon Labs recommends an asymmetrical loading of the crystal.

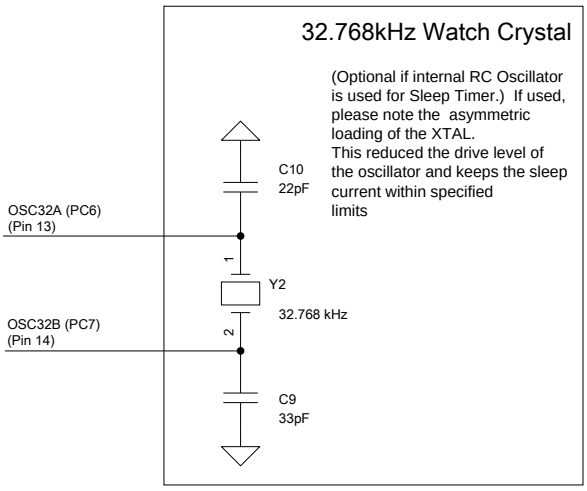


Figure 24. 32 kHz low-frequency crystal

If the application does not need the 32 kHz crystal, then the pins OSC32A (PC6) and OSC32B (PC7) can be used as General Purpose IO.

5.3 1.8 V Regulator Load Capacitor

The EM35x operates over a supply voltage (VBRD) of 2.1 to 3.6 V. An integrated 1.8 V regulator converts VBRD down to a trimmed 1.8 V. To stabilize the integrated regulator, a 2.2 µF ceramic loading capacitor is required on the output of VREG_OUT (Pin 16) of the EM35x. A series resistor (R7) is used to keep the minimum ESR of the loading capacitor below 1 Ohm. This is shown in Figure 25

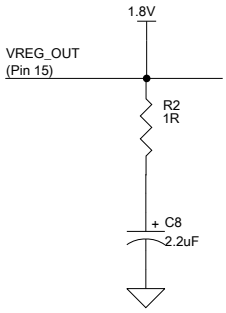


Figure 25. 1.8 V regulator loading capacitance

5.4 1.2 V Regulator Loading

The EM35x contains an integrated 1.2 V Regulator to drive the Core Logic. By driving the core at this lower VDD potential, significant current consumption is achieved. To utilize this regulated voltage, a PCB designer should connect pin 17 (VDD_CORE_0) to pin 44 (VDD_CORE_1). If you would like to drive the core at 1.8 V, then the 1.8 V net should be connected to both pins 17 and 44.

A 1 µF ceramic loading capacitor should be placed close to pin 17. In addition, a 10 nF decoupling capacitor should be place close to pin 44.

5.5 1.8 V Net Decoupling

To minimize noise and coupling paths into the EM35x, decoupling capacitance must be placed on each of the VDD pins. All decoupling capacitors should be placed as close to the EM35x as possible as well as in between the source point (via) and the EM35x pin. In addition, all values should be maintained as defined by the EM35X Reference Design.

5.6 1.8 V Analog to 1.8 V Digital Filtering

To keep the Radio Active current at 36 mA, Silicon Labs recommends adding a single element filter (resistor) between the digital and analog 1.8 V nets, 1.8 V_A and 1.8 V_D, respectively (see Figure 26). This resistor maintains a reduced bias current for the digital logic within the EM35x. If this resistor is not used, the RX current will increase by 1 mA to 37 mA.

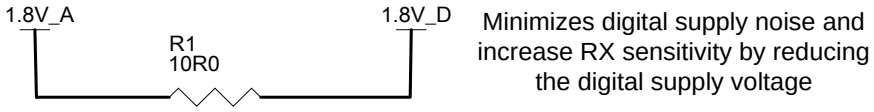


Figure 26. Digital VDD filter

The lower current consumption also allows for a reduction in the digital 1.8V Domain noise. This means the RX Sensitivity improves by 2 dB with the 10 Ohm resistor.

5.7 RF Test Connector

To assist with manufacturing test of the printed circuit assemblies, Silicon Labs recommends the use of a RF switch connector, such as the Murata RF switch connector. The RF switch connector allows an external 50 Ohm, RF cable to be connected during design verification testing. With the external RF cable connected to the RF switch connector, the antenna is isolated from the RF test measurement which provides for an accurate and repeatable RF Test. When the cable is not connected, the RF switch connector allows the antenna to be connected to the EM35x RF path.

The RF switch connector is in stock, low cost, and low loss. However, if a designer does not want to incur the extra cost, you can add the footprint for the RF switch connector along with two resistors to select the connector during prototyping phase and not populate when in higher volume manufacturing.

5.8 Debug and Programming Interface

To program the integrated flash and debug the software application within the EM35x, Silicon Labs recommends the designer incorporate the 10-pin Packet Trace Port connector. With this connector in place, the Ember Debug Adapter (ISA3) can connect directly to the ARM® Cortex™-M3 core and integrated memory bus.

To facilitate packet-level debugging of an EM35x-based application, Silicon Labs utilizes two GPIOs, PA4 and PA5, as well as nRESET. To use the full program and debug environment from Silicon Labs' tool chain (Ember Desktop), Silicon Labs recommends the designer route the following signals from the EM35x to either test points or to a connector:

- nRESET
- PA4
- PA5
- PC0
- PC2
- PC3
- PC4
- JCLK
- VDD (2.1V to 3.6V)
- GND

To allow for direct connection to a Debug Adapter (ISA3) with the Packet Trace Port cable, the designer should consider using a dual-row, 0.05″ pitch connector similar to the one used on the EM35x Radio Communication Module (RCM).

The connector used on the Ember EM35x Radio Communication Module (RCM) is from Samtec (MFG P/N: FTSH-105-01-F-DV-K). It is keyed to guarantee proper connection with the Packet Trace Port cable (Samtec P/N: FFSD-05-D-12.00-01-N). Figure 27 illustrates the pinout for the Packet Trace Port, and Table 3 describes the pins.

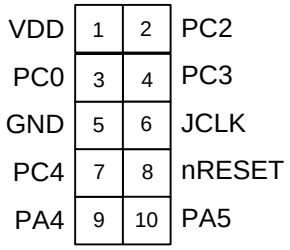
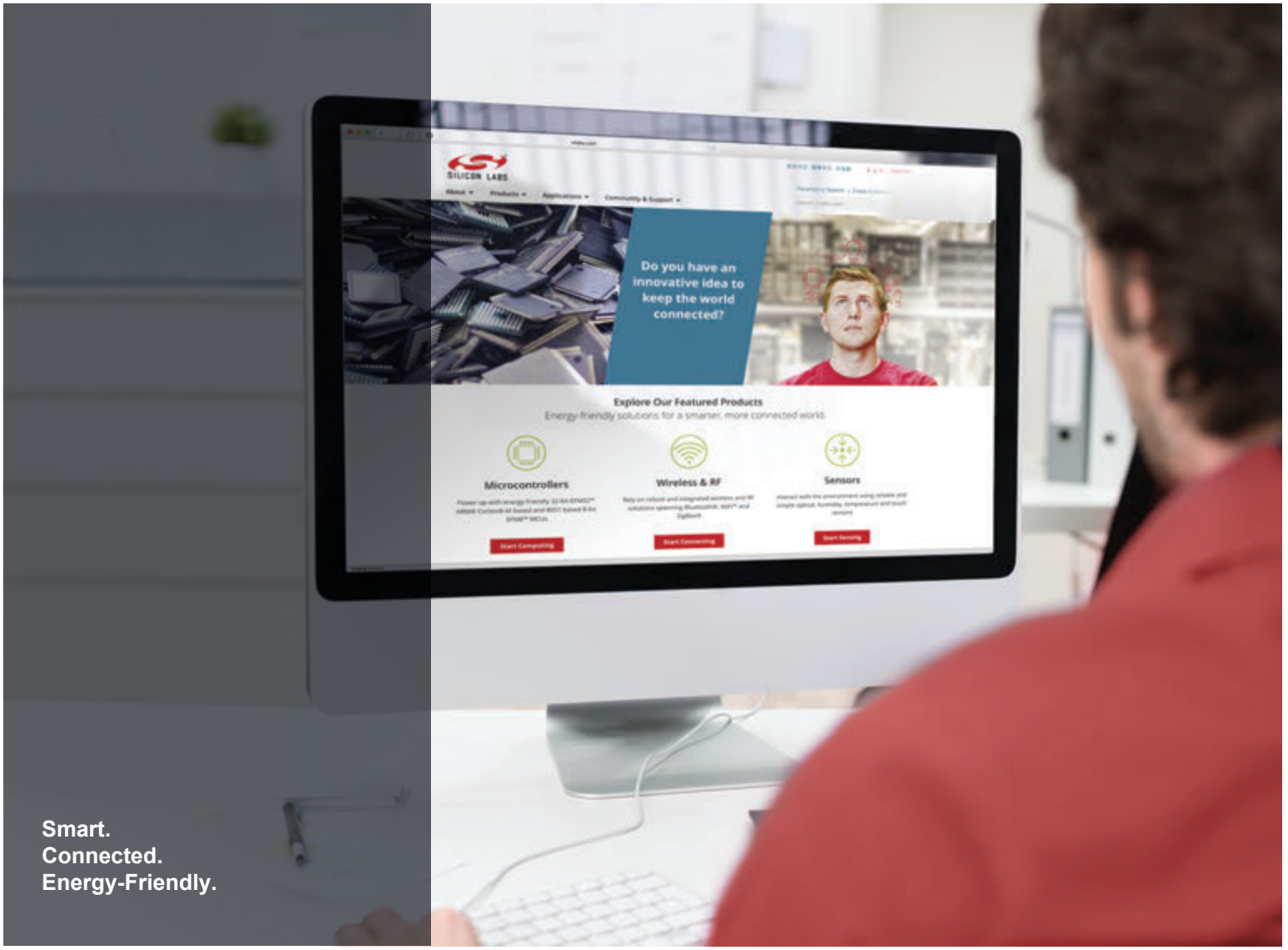


Figure 27. Packet Trace Port Pinout

Table 3. Packet Trace Port Pins

Pin #	Signal Name	Direction	Description
1	VBRD	Power	2.1 to 3.6V supply for the EM35x
2	PC2 (JTDO / SWO)	Output	JTAG JTDO, serial wire out
3	PC0 (nJRST)	Output	JTAG reset
4	PC3 (JTDI)	Input	JTAG Data In
5	GND	Power	Ground
6	JCLK / SWCLK	Input	JTAG clock, serial wire clock
7	PC4 (JTMS / SWDIO)	I/O	JTAG JTMS, serial wire data in / out
8	nRESET	Input	Active low, EM35x reset (internal pull-up within EM35x)
9	PA4 (PTF)	Output	Packet trace frame signal
10	PA5 (PTD)	Output	Packet trace data signal; 500kbps



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