USING THE SiM3L1xx ADVANCED CAPTURE COUNTER IN LC RESONANT DESIGNS

1. Introduction

The SiM3L1xx devices contain a low-power advanced capture counter module that runs from the RTC0 timer clock and can be used with digital inputs, switch topology circuits (reed switches), or with LC resonant circuits. For switch topology circuits, the module charges one or two external lines by pulsing internal pull-up resistors and detecting whether the reed switch is open or closed. For LC resonant circuits, the inputs are periodically energized to produce a dampened sine wave and configurable discriminator circuits detect the resulting waveform decay.

This document will focus on the LC resonant features of this module.

2. Relevant Documents

This document provides a hardware and software overview for the LC Resonant mode of the SiM3L1xx Advanced Capture Counter module. Additional documentation on the Precision32™ tools and MCUs can be found on the Silicon Laboratories website: www.silabs.com/32bit-appnotes, www.silabs.com/32bit-software, and www.silabs.com/32bit-mcu.

3. ACCTR0 Module Overview

The SiM3L1xx family of microcontrollers contains a low-power Advanced Capture Counter (ACCTR0) module designed to count pulses from many different types of sources including digital inputs, switch topology circuits (reed switches), LC resonant circuits and Wheatstone bridges. For switch topology circuits, it charges 1 or 2 external lines by pulsing different size pull-up resistors and then detects the reed switch's open or close state. It also supports external LC resonant circuits which are periodically energized to produce a dampened sine wave that can be used to count the number of peaks over a programmable threshold. A discriminator circuit then decides if a rotating wheel is in the dampened or non-dampened region based on the number of counted peaks being either above or below programmable digital thresholds. The ACCTR0 module also includes asymmetrical integrators for low pass filtering and switch debounce, single, dual, and quadrature modes of operation, flutter detection, two 24-bit counters, two 24-bit threshold comparators, and a variety of interrupt and sleep wake-up capabilities. This combination of features provides water, gas, and heat metering system designers with an optimal tool for saving power while collecting meter usage data.

ACCTR0 can operate in power mode 8 (PM8) to enable ultra-low power metering systems. The MCU does not have to wake up on every edge or transition and can remain in PM8 while ACCTR0 counts pulses for an extended period of time. The module includes two 24-bit counters. These counters can count up to 16,777,215 (2^{24}-1) transitions in sleep mode before overflowing. The module can wake up the MCU when one of the counters overflows. The ACCTR0 also has two 24-bit digital comparators. The digital comparators have the ability to wake up the MCU when either of the counters reaches a predetermined threshold.

The ACCTR0 uses the RTC0 timer clock for sampling, de-bouncing, managing the low-power pull-up resistors, and timing of stimulus pulses. The RTC0TCLK signal must be enabled when counting pulses. If desired, the RTC0 alarms can wake up the MCU periodically to read the pulse counters, instead of using the digital comparators. For example, RTC0 can wake up the MCU every five minutes. The MCU can then read the count values and transmit the information using the UART or a wireless transceiver before returning to sleep.

3.1. External Pin Connections

The external pin connections for the ACCTR0 module include up to four analog I/O and up to eight digital I/O. Not all pins are used in every mode or with every external circuit configuration. Any pins used by the ACCTR0 module should be configured to the appropriate mode (analog or digital) in the PBCFG module and skipped by the crossbar. See the SiM3L1xx device documentation (data sheet and reference manual) for more information on the mapping of these signals to physical pins.

Table 1. ACCTR0 External Pin Connections

ACCTR0 Signal Name	Type	Function
ACCTR0_IN0	Analog In	Switch Input 1 LC Comp0-
ACCTR0_IN1	Analog In	Switch Input 0 LC Comp1-
ACCTR0_STOP0	Digital In	LC Channel 0 Pulse Stop
ACCTR0_STOP1	Digital In	LC Channel 1 Pulse Stop
ACCTR0_LCIN0	Analog In	LC Comp0+
ACCTR0_LCIN1	Analog In	LC Comp1+
ACCTR0_LCPUL0	Digital Out	LC Channel 0 Pulse Out
ACCTR0_LCPUL1	Digital Out	LC Channel 1 Pulse Out
ACCTR0_LCBIAS0	Digital Out	LC Channel 0 Bias Out
ACCTR0_LCBIAS1	Digital Out	LC Channel 1 Bias Out
ACCTR0_DBG0	Digital Out	Debug Output 0
ACCTR0_DBG1	Digital Out	Debug Output 1

3.2. Analog Front End

The analog front end of the ACCTR0 module supports a wide variety of external circuits. The ACCTR0 module supports two major analog input modes: switch topology mode, and LC resonant mode. The LC resonant mode is more complex, and can be used with LC resonant circuits, capacitive circuits, Wheatstone bridges, continuous variable-frequency pulse trains, etc. The main focus in this documentation is LC resonant circuit usage, though other external circuits may be mentioned. The TOPMD bit in the CONFIG register selects between switch topology mode and LC resonant mode.

Figure 1 shows a typical connection diagram for an LC resonant circuit. The configuration shown uses the comparator in a single-ended manner. It is possible to use the IN0 and IN1 inputs as the negative input to the comparator for differential topologies, such as magneto-resistive Wheatstone bridges.

In this circuit, the external resonant circuit is pulsed with an LC pulse signal (LCPUL) signal, and counters detect the number of peaks from a dampened sine wave at the LCIN input. A discriminator circuit compares the number of counts against a digital threshold to decide if the circuit is in the dampened or undampened region of a rotating wheel.

Note: The ESD protection in the input pads will clip voltages above 5.25 V and below -0.3 V. The LC comparator input can be externally ac coupled to the resonant circuit and pre-biased at VIO/2 to limit clipping.

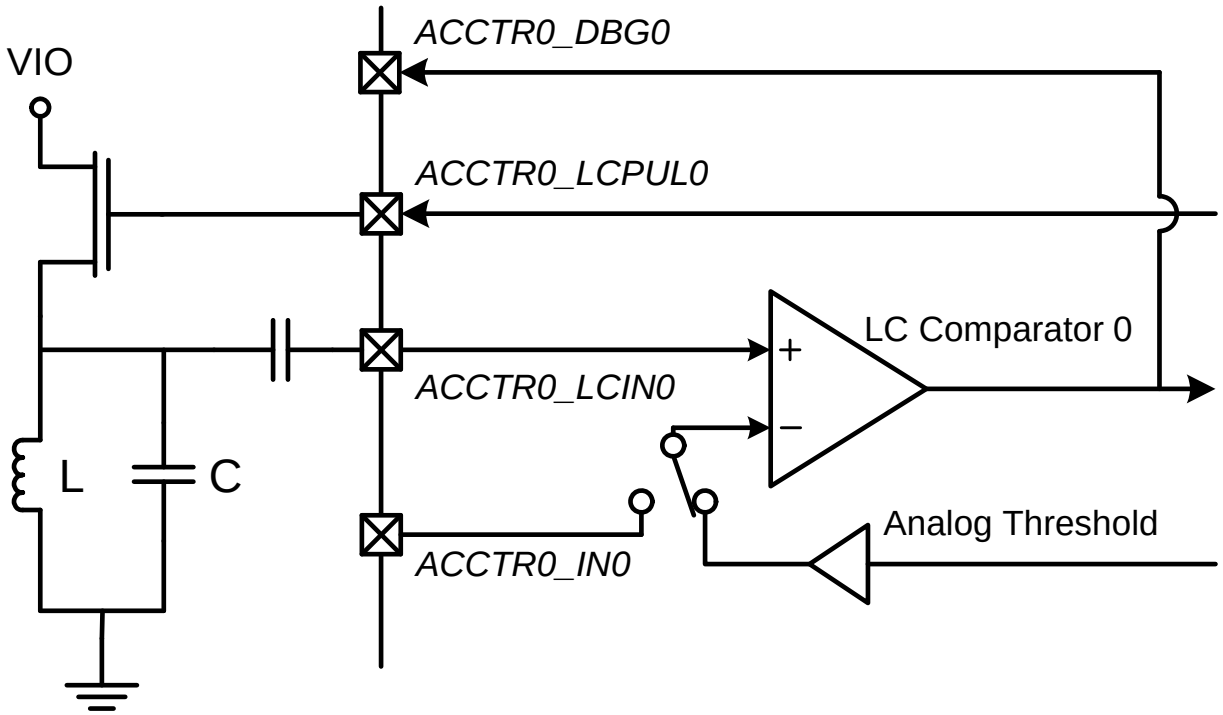


Figure 1. LC Resonant Configuration

3.0.3. Choosing Components

Impeller composition and distance from the inductor matter, so it is recommended to perform final tuning of the component values with the meter used in the application.

The power losses in the capacitor are proportional to the capacitor and sampling frequency.

$$E_C = \frac{1}{2}CV^2$$

$$P_C = F_{sampling}\frac{1}{2}CV^2$$

Equation 1. Power Consumed by the ACCTR0 Capacitor

Therefore, a small capacitor and slow sampling rate will yield the lowest power.

The power losses in the inductor depend on the current, which is determined by the pulse time.

$$E_L = \frac{1}{2}LI^2$$

$$V = L\frac{\Delta i}{\Delta t}$$

$$P_L = \frac{1}{2}F_{sampling}LI^2 = \frac{1}{2}F_{sampling}L\left(\frac{V^2t^2}{L^2}\right) = \frac{1}{2}F_{sampling}\left(\frac{V^2t^2}{L}\right)$$

Equation 2. Power Dissipated by the ACCTR0 Inductor

A large inductor minimizes the losses, and the pulse width should be as short as possible while charging the capacitor completely.

The resonant frequency, ignoring secondary effects, is determined by the simple tank circuit equation shown in Equation 3.

$$f = \frac{1}{2\pi\sqrt{LC}}$$

Equation 3. LC Circuit Resonant Frequency

After finding a suitable inductor, estimate the Q of the circuit using Equation 4. The Q value is the total energy stored in the circuit divided by the amount of energy lost on each resonance.

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}}$$

Equation 4. Resonance of the LC Circuit

The ringing frequency of the circuit including the inductor's resistance is given by Equation 5.

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}$$

Equation 5. Ringing Frequency of the ACCTR0 LC Circuit

The lower the resistance of the inductor, the more the circuit is able to maintain energy and save power. With an inductor that has a large resistance, the circuit is only able to oscillate one or two times before the inductor resistance has dissipated the energy. In addition to the inductor resistance, the rotating wheel absorbing magnetic flux from the inductor dampens the oscillation of the tank circuit.

Combined, these equations imply that the ACCTR0 output circuit has a higher count and lower power consumption with larger inductors (greater than 100 µH), smaller capacitors (smaller than 1000 pF), slower sampling rates, short widths for the A, B, C zones, and short widths for the excitation pulses. In the case of quadrature mode, the inductors needs to be small enough or oriented such that the inductors are not tightly coupled. Once the inductor size has been selected, the capacitor size can be used to optimize for power or performance, depending on the application needs.

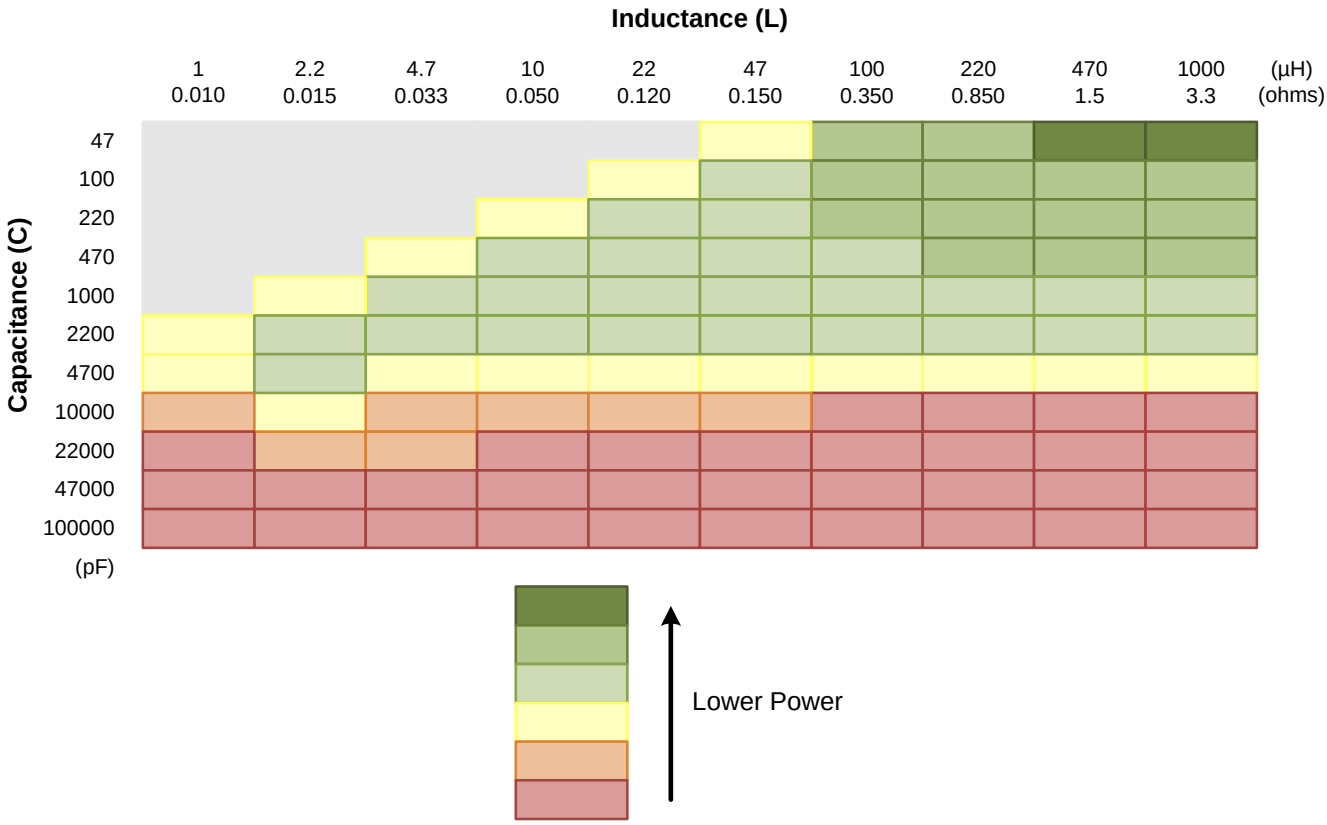


Figure 2. Power Consumption with Varying Components Values

Figure 2 shows the relative power consumption of the ACCTR0 module in LC mode. The green areas are the lowest power in Power Mode 9, including the LC tank circuit, the comparators, the excitation pulse generation, VBAT-divided-by-2 biasing, control circuitry, and the RTC. The gray area indicates a tank circuit frequency too high for the comparators, while the yellow, orange, and red indicate areas with component values that require more power. The sample rate in this scenario is 1.95 ms. Slowing down the resonant frequency allows the comparators to be set to a lower speed, which then uses less power; however, a resonant frequency that is too slow requires the ACCTR0 module to use more power while acquiring slow counts.

3.4. Analog Comparator Functions

Four analog comparators are included in the ACCTR0 module, which should not be confused with the digital comparators in the ACCTR0 module nor with any other dedicated comparator peripherals on the device. Two of these (PC comparator 0 and PC comparator 1) are used in switch topology mode, while the other two (LC comparator 0 and LC comparator 1) are used in LC resonant mode. The difference in the two circuits lies primarily in their intended function. The switch topology comparators are designed with slower, high voltage signals in mind. They are much like a digital input with programmable VIH and VIL levels. The LC comparators are higher-precision circuits designed to quickly detect low-amplitude peaks of an oscillating signal. They can be operated as single-ended with a programmable internal threshold level, or differentially with two inputs.

When the ACCTR0 is configured in LC resonant mode, the positive input of the LC comparator connects to the corresponding ACCTR0_LCIN0 or ACCTR0_LCIN1 pin. If the LC resonant circuitry is configured for differential inputs (see Table 2), the negative input of the comparator will connect to the corresponding ACCTR0_IN0 or ACCTR0_IN1 pin. When configured for single-ended inputs, the negative terminal is connected to an internal adjustable threshold circuit. The threshold for the comparator is set by the CMPnTHR, CMPnCTH and CMPnFTH fields in the LCCONFIG register. By default, the LC comparators are only turned on when they are needed by the circuit, to save power. It is possible to force the comparators to an always on state using the FCMPnEN bits.

Additionally, the comparators support programmable hysteresis and speed. These features are controlled by the CMPHHYS, CMPLHYS and CMPMD fields in LCCONFIG. The hysteresis and speed settings are common to both comparators.

The output of the LC comparator feeds into the discriminator circuit in this mode. The output can also be routed to the ACCTR0's debug output pins, or read from the CMP0OUT and CMP1OUT bits in the STATUS register.

3.5. LC Counting / Conditioning

In LC resonant mode the ACCTR0 can generate pulsed stimulus to excite external circuitry, and measure the resulting response characteristics. For an LC resonant circuit this takes the form of a dampened sinusoid. The comparator front end circuit detects the peaks of the sinusoid which occur over a short period of time, and a peak counter is used to accumulate the pulses. A discriminator circuit is used to compare the number of counts against a programmable threshold to determine whether the sinusoid is dampened or undampened.

In LC mode the ACCTR0 works by perturbing an LC tank and counting the number of peaks seen before the oscillation is damped to the point where the IC can no longer distinguish peaks.

The peaks are detected by an analog comparator. The first step in the process is to precharge the observed signal to the reference level of the comparator. This results in the tank oscillating around the reference level.

A peak is detected when the observed voltage crosses the comparator threshold. The threshold can be adjusted by software. This can be thought of as imposing a line a set number of millivolts above the reference voltage. The hardware detects a peak whenever that line is crossed by the signal.

The comparator also has configurable hysteresis. This controls how far from the threshold the signal must deviate before another peak can be detected. This is useful for eliminating the effects of high frequency noise.

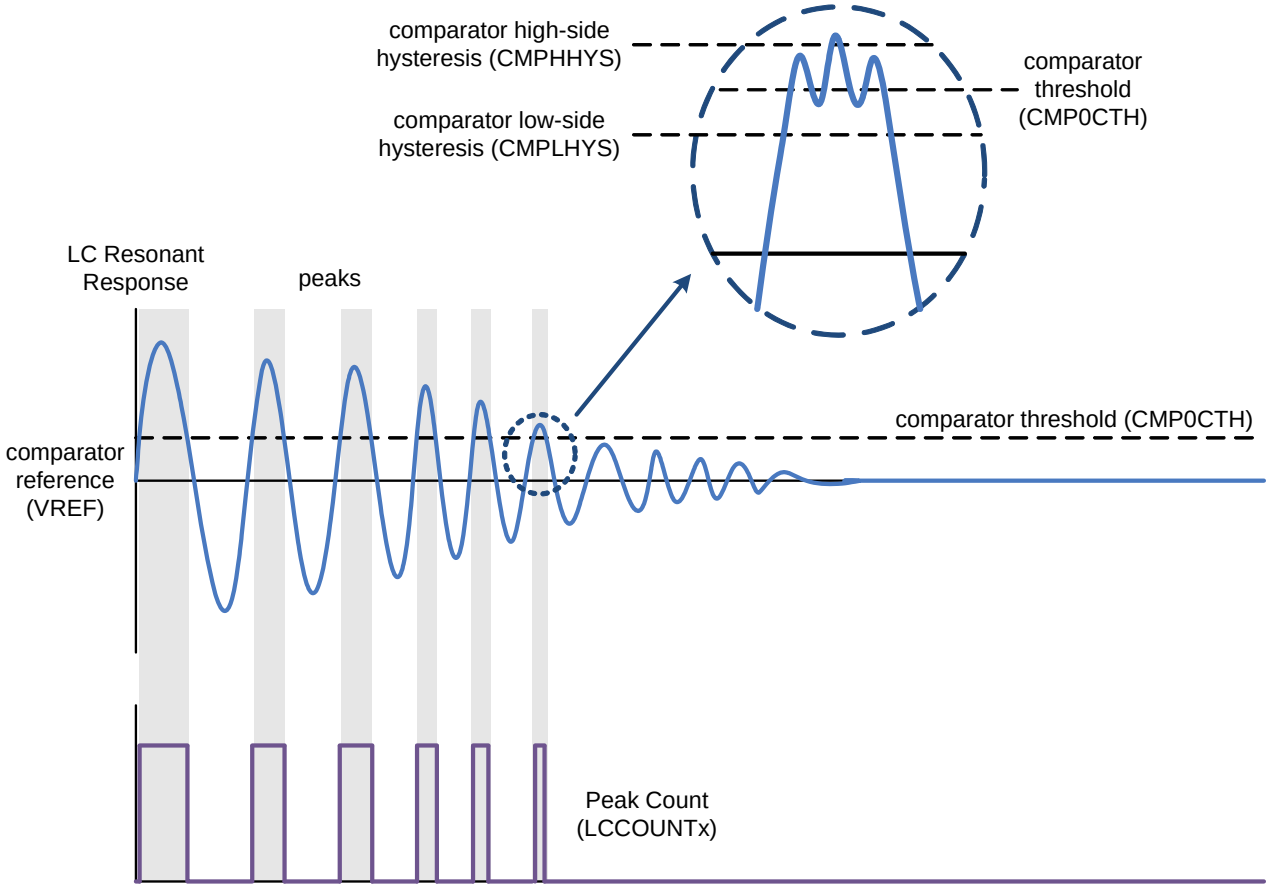


Figure 3. Counting Peaks in LC Resonant Topologies

Finally, the speed of the comparator can be configured to balance power consumption with the need to resolve high frequency signals. This setting effectively applies a filter to the signal that attenuates the voltage. As the comparator slows, the low amplitude peaks will not be seen. If the comparator slows beyond the frequency of the tank, the hardware will not detect any peaks.

The hardware applies the precharge, sends out a pulse to the tank to start oscillation, and then counts the resulting

peaks for a configurable amount of time every time it measures the LC resonant circuit. This generates a peak count for that sample. The peak count will change as the impeller turns. In one full revolution, the peak count will transition from an maximum count to a minimum count and back to the maximum count. The digital logic marks a 'count' every time the number of peaks crosses a configurable threshold in the negative (decreasing) direction.

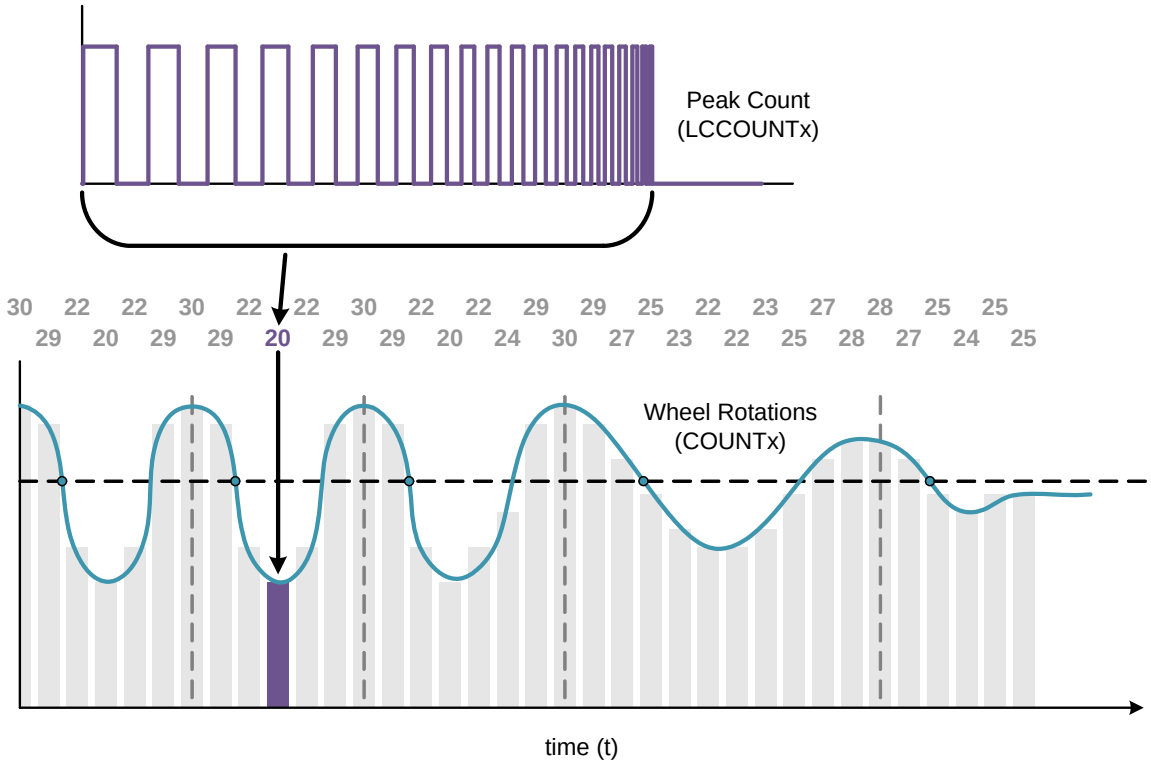


Figure 4. Measuring Counts in LC Resonant Topologies

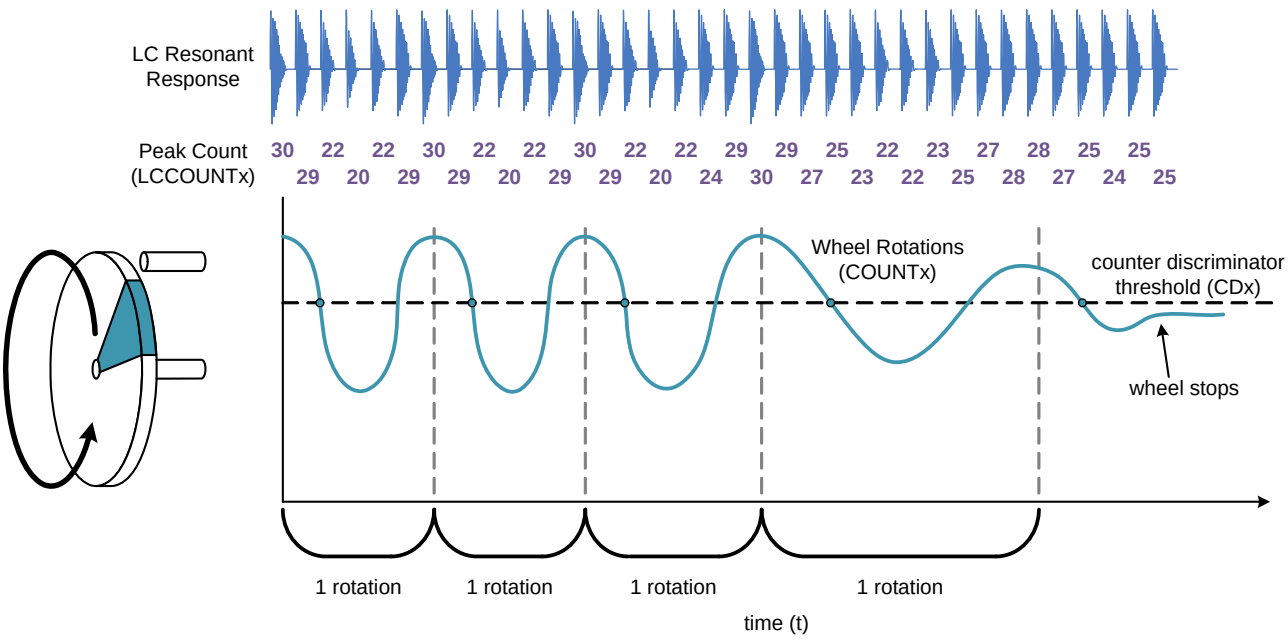


Figure 5. Counting Wheel Rotations in LC Resonant Topologies

When in automatic tracking mode, the delta between the minimum and maximum is fixed, and the hardware will slide the maximum-minimum window as it sees new minimum or maximum peak counts. The hardware also keeps the digital peak threshold half way between the minimum and maximum, providing as much digital comparator margin as possible.

Since the peak count may fluctuate a little at steady state, the digital comparator also has a hysteresis setting. This can be set to prevent seeing false counts when the meter is stalled with the peak count near the threshold.

3.5.1. LC Peak Counters

The LC peak counters count pulse outputs from the LC comparators. The LCCOUNT0 and LCCOUNT1 fields in the LCCOUNT register will contain the most recent LC counter value for each of the two channels.

3.5.2. LC Oscillator Calibration

The LC Oscillator is used to time several operations of the circuit in LC resonant mode. This oscillator nominally runs at 40 MHz and is only turned on to generate pulses as needed, to save power. Calibration of this oscillator can be performed in order to determine the actual oscillator frequency and adjust the timing parameters for the rest of the LC circuitry. An oscillator calibration does not change the frequency of the oscillator itself. Instead, the frequency is measured using the RTC0TCLK as a frequency reference. Setting the CLKCAL bit in the LCCLKCONTROL register to 1 initiates a calibration sequence. This bit will remain 1 during calibration, and hardware will clear this bit to 0 when the calibration completes. During that time, a special counter counts the number of LC Oscillator clock cycles which occur during one RTC0TCLK period. The result is presented in the CLKCYCLES field of LCCLKCONTROL.

3.5.3. Discriminators

The purpose of the discriminator is to make a distinction between how many counts of the LC peak counter constitute a logic 1 and logic 0. The discriminator consists of a digital threshold level with programmable hysteresis, and logic to enable automatic tracking and adjustment of the discriminator threshold. The current discriminator values for each channel are stored in the CD0 and CD1 field of the LCCOUNT register. The discriminator is enabled when bit 1 of the LCMD field is cleared to 0 (see Table 2). To operate without the discriminator (in sample-and-hold mode) bit 1 of the LCMD field can be set to 1.

3.5.3.1. Discriminator Digital Hysteresis

At the basic level, the discriminator can be set to a fixed value, acting as a threshold detector for 1's and 0's. Any value of the LC peak counter that is greater than or equal to the discriminator will result in a 0-to-1 transition at the discriminator output. Up to 3 counts of negative digital hysteresis can be applied to the high-to-low transition for each discriminator. The hysteresis is set by the LCD0HYS and LCD1HYS values in the LCMODE register.

3.5.3.2. Discriminator Tracking

The LCMODE register also contains two bits to enable automatic centering and signal tracking of the discriminator values. The ACDEN bit enables the automatic centering function. When centering is enabled, the discriminator value will be automatically updated to be centered between the MIN and MAX fields in the LCLIMITS register.

The MIN and MAX fields are updated after each count cycle has completed. By default, any value larger than the current MAX will replace MAX, and any value smaller than the current MIN will replace MIN. This behavior can be changed by enabling Automatic Tracking Mode using the ATRKEN bit. When ATRKEN is enabled, it forces the MIN and MAX values to remain the same distance apart, and only allows a change of one count per cycle. For example, if the current cycle completes and the count result is 5 codes higher than the current MAX value, MAX and MIN will both be incremented by 1 count. If the new count value is less than the current MIN value, both MIN and MAX are decremented by 1 count.

3.5.4. LC Pulse Stimulus

In LC resonant mode, the ACCTR0 has the ability to provide timed pulse stimuli to the external circuitry. A sampling event is divided into five distinct timing zones. The timing of the zones, the polarity of the pulses, and the region where comparisons are made are all programmable in firmware to achieve reliable, low-power operation for a variety of different circuit configurations.

3.5.4.1. Zones and Timing

The LC resonant stimulus circuitry divides the sampling event into a preconditioning zone (P) and four timing zones (A, B, C, D). Timing of each zone can be configured between 1 and 8 RTC0TCLK cycles using the ZONE fields in the TIMING register. The ACCTR0_LCPUL and ACCTR0_LCBIAS pins can be pulsed during selected zones to condition and excite external circuitry. The LC peak counters can then be activated during a selected zone to capture the resulting waveform. Figure 6 illustrates the timing zones with some example stimulus.

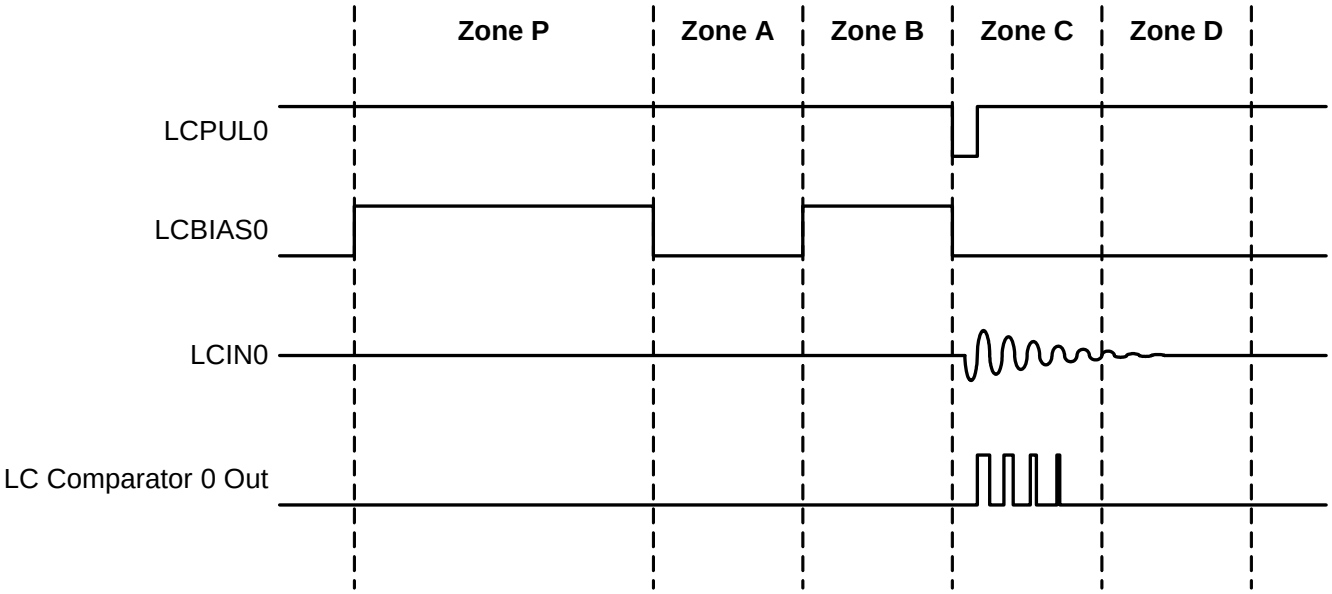


Figure 6. LC Resonant Timing

In this example, the bias signal LCBIAS0 is configured to pulse high during zones P and B. The LCPUL0 stimulus pulse is configured to pulse high during zone C and reset on an internal timer. The counter and comparator are enabled during zone C to capture the resulting waveform.

The bias pulsing options are straightforward. Bias pulses are generated at the LCBIAS pins with the polarity selected by the B0POL and B1POL bits. The user also has the option to generate bias on the external signals, internal signals, or both using the BMD field. Bias pulses are configured to occur in zones P, A, B or C using the corresponding bias zone enable bits in LCMODE. By default, bias pulses last the entire duration of the selected field. The bias pulses can be delayed from the beginning and end of the zone by 1/2 RTC0TCLK cycle each using the B0OEN and B1OEN bits in the TIMING register.

The pulse configuration options for the LCPUL pins are more extensive, and also more directly related to the operation of the rest of the circuit. A variety of different pulsing and measurement options are controlled by the LCMD field in the LCMODE register. These options are summarized in Table 2.

Table 2. LC Mode Options

LCMD Setting	Pulse Mode	Counter Behavior	Comparator Mode
0000	Full Zone	Discriminator	Single-Ended
0001	Full Zone	Discriminator	Differential
0010	Full Zone	Sample / Hold	Single-Ended
0011	Full Zone	Sample / Hold	Differential
0100	Stop on LC Timer	Discriminator	Single-Ended
0101	Stop on LC Timer	Discriminator	Differential
0110	Stop on LC Timer	Sample / Hold	Single-Ended
0111	Stop on LC Timer	Sample / Hold	Differential
1000	Stop on External Pin Rising Edge	Discriminator	Single-Ended
1001	Stop on External Pin Falling Edge	Discriminator	Single-Ended
1010	Stop on External Pin Rising Edge	Sample / Hold	Single-Ended
1011	Stop on External Pin Falling Edge	Sample / Hold	Single-Ended
1100	No Pulse Generated	Discriminator	Single-Ended
1101	No Pulse Generated	Discriminator	Differential
1110	No Pulse Generated	Sample / Hold	Single-Ended
1111	No Pulse Generated	Sample / Hold	Differential

The zone in which LCPUL pin pulses occur is selected between zones A, C, or A and C using the P0ZONE and P1ZONE fields, and the pulse type is selected between low, high and toggle operation using the PMD field.

LCMD[3:2] configures the type of pulse that will be generated on the LCPUL pin. Except when set to “No Pulse Generated”, the LCPUL pulse will begin at the start of the specified zone or zones. When set to “Full Zone”, the LCPUL pulse ends at the end of the zone. When set to “Stop on LC Timer”, the pulse will last for the number of 40 MHz LC Oscillator cycles specified in the RELOAD field of LCCLKCONTROL. If set to “Stop on External Pin”, the pulse will last until the external STOP input meets the rising/falling edge condition.

The CnZONE fields in the LCTIMING register specify which zone the counter will operate in (A, B, C or D).

3.6. Counting Modes

The Advanced Capture Counter supports three different counting modes: single counter mode, dual counter mode, and quadrature counter mode. Figure 7 illustrates the three counter modes.

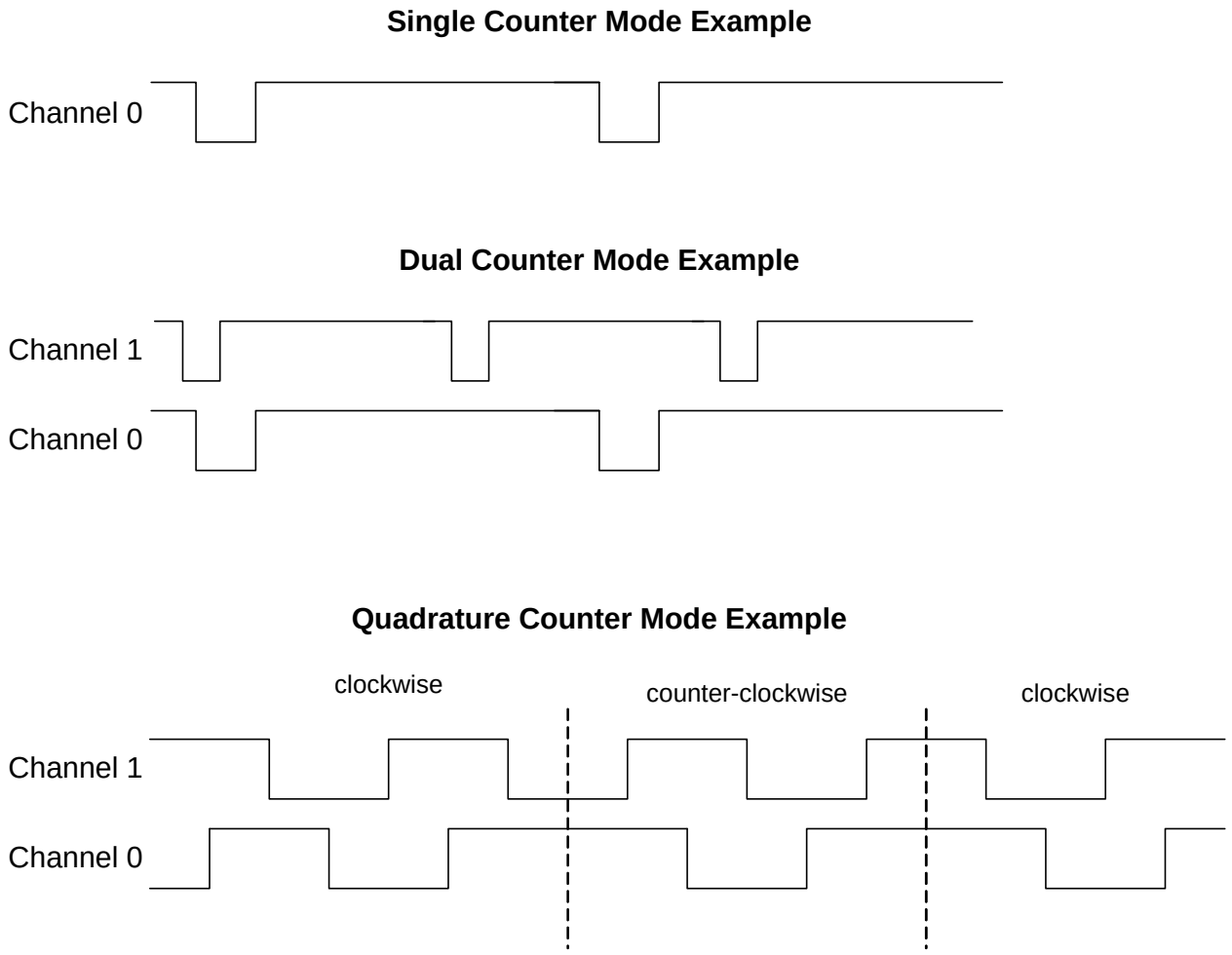


Figure 7. Counter Mode Examples

The single counter mode counts pulses from a single input channel. This mode uses only counter 0 and digital comparator 0 (counter 1 and digital comparator 1 are not used.) The single counter mode supports only one meter-encoder with a single-channel output. A single-channel encoder is an effective solution when the metered fluid flows only in one direction. A single-channel encoder does not provide any direction information and does not support bidirectional fluid metering.

The dual counter mode supports two independent single-channel meters. Each meter has its own independent counter and digital comparator. Some of the global configuration settings apply to both channels, such as pull-up current, sampling rate, and debounce time. The dual mode may also be used for a redundant count using a two-channel non-quadrature encoder.

Quadrature counter mode supports a single two-channel quadrature meter encoder. The quadrature counter mode supports bidirectional encoders and applications with bidirectional fluid flow. In quadrature counter mode, clockwise counts will increment counter 0, while counterclockwise counts will increment counter 1. Subtracting counter 1 from counter 0 will yield the net position. If the normal fluid flow is clockwise, then the counterclockwise counter 1 value represents the cumulative back-flow. Firmware may use the back-flow counter with the corresponding comparator to implement a back-flow alarm. The clockwise sequence is (LL-HL-HH-LH), and the counter clockwise sequence is (LL-LH-HH-HL). (For this sequence LH means Channel 1 = Low and Channel 0 = High.)

Firmware cannot write to the counters. The counters are reset when the CONFIG register is written and have their counting enabled when the PCMD field is set to either single, dual, or quadrature modes. The counters only increment and will roll over to 0x000000 after reaching 0xFFFFFF.

For single mode, the channel 0 input connects to counter 0. In dual mode, the channel 0 input connects to counter 0 while the channel 1 input connects to counter 1. In Quadrature mode, clockwise counts are sent to counter 0 while counterclockwise counts are sent to counter 1.

3.6.1. Quadrature Error

The quadrature encoder must only send valid quadrature codes. A valid quadrature sequence consists of four valid states. The quadrature codes are only permitted to transition to one of the adjacent states, and an invalid transition will result in a quadrature error.

Note: A quadrature error is likely to occur when first enabling the quadrature counter mode, since the Advanced Capture Counter state machine starts at the LL state and the initial state of the quadrature is arbitrary. It is safe to ignore the first quadrature error immediately after initialization.

3.6.2. Flutter Detection

The flutter detection logic can be used with either quadrature counter mode or dual counter mode when the two channels are expected to be in step. Flutter refers to the case where one input continues toggling while the other input stops toggling. This may indicate a broken switch or a pressure oscillation when the wheel magnet stops at just the right location. If a pressure oscillation causes a slight rotational oscillation in the wheel, it could cause a number of pulses on one of the inputs, but not on the other. All four edges are checked by the flutter detection feature (Channel 1 positive, Channel 1 negative, Channel 0 positive, and Channel 0 negative). When enabled, Flutter detection may be used as an interrupt or wake-up source.

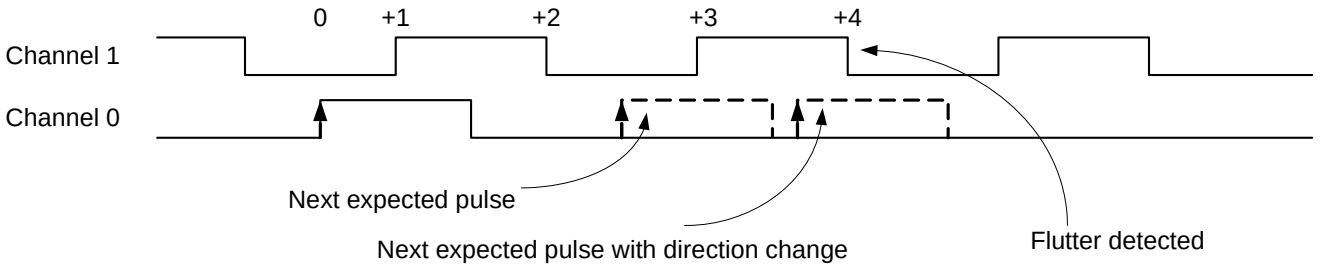


Figure 8. Flutter Example

For example, flutter detected on the channel 0 positive edge means that 4 edges (positive or negative) were detected on channel 1 since the last channel 0 positive edge. Each channel 0 positive edge resets the flutter detection counter while either channel 1 edge increments the counter. There are similar counters for all four edges.

The flutter detection circuit provides interrupts or wake-up sources, but firmware must also read the Advanced Capture Counter registers to determine what corrective action, if any, must be taken.

On the start of flutter event, the firmware should save both counter values and the DIRHIST field in the STATUS register. Once the end of flutter event occurs the firmware should also save both counter values and the DIRHIST field. The flutter stop enable bit (FLSTPEN in CONFIG) may be set to stop the counters when flutter is occurring (quadrature mode only). For quadrature mode, the opposite counter should be decremented by one. In other words, if the direction was clockwise, the counterclockwise counter (counter 1) should be decremented by one to correct for one increment before flutter was detected. For dual mode, two switches can be used to get a redundant count. If flutter starts during dual mode, both counters should be saved by firmware. After flutter stops, both counters should be read again. The counter that incremented the most was the one that picked up the flutter. There is also a mode to switch from quadrature to dual when flutter occurs, using the FLQDEN bit in CONFIG. This changes the counter style from quadrature (count on any edge of channel 1 or channel 0) to dual to allow all counts to be recorded. Once flutter ends, this mode switches the counters back to quadrature mode. Flutter stop enable does not function when the FLQDEN bit is set.

3.7. Sample Rate

The Advanced Capture Counter has a programmable sampling rate. The Advanced Capture Counter initiates samples at discrete time intervals based RTC0TCLK cycles. The PERIOD field sets the sampling rate. The system designer should carefully consider the maximum pulse rate for the particular application when setting the sampling rate and debounce time. Sample rates from 4 to 4096 RTC0TCLK cycles can be selected to either further reduce power consumption or work with shorter pulse widths. The slowest sampling rate will provide the lowest possible power consumption.

3.8. Debounce

Many types of mechanical switches exhibit switch bouncing that could potentially result in false counts or quadrature errors. The Advanced Capture Counter includes digital debounce logic using a digital integrator that can eliminate false counts due to switch bounce. In LC resonant mode, the input of the integrator is fed by the output of the discriminator logic. The output of the integrator connects to the counters.

The debounce integrator has two independent programmable thresholds: one for the rising edge and one for the falling edge. The HDBTH field in the DBCONFIG register sets the threshold for the rising edge (high debounce). This field sets the number of cumulative high samples required to output a logic high to the counter. The LDBTH field in DBCONFIG sets the threshold for the falling edge (low debounce). This field sets the number of cumulative low samples required to output a logic low to the counter.

Note that the debounce integrator does not count consecutive samples. Requiring consecutive samples would be susceptible to noise. The digital integrator inherently filters out noise.

The system designer should carefully consider the maximum anticipated counter frequency and duty-cycle when setting the debounce time. If the debounce configuration is set too large, the Advanced Capture Counter will not count short pulses. The debounce-high configuration should be set to less than one-half the minimum input pulse high-time. Similarly, the debounce-low configuration should be set to less than one-half the minimum input pulse low-time.

Figure 9 illustrates the operation of the debounce integrator when used in conjunction with a switch topology circuit. The top waveform is the representation of the reed switch (high: open, low: closed) which shows some random switch bounce. The bottom waveform is the final signal that goes into the counter which has the switch bounce removed. Based on the actual reed switch used and sample rate, the switch bounce time may appear shorter in duration than the example shown here. The second waveform is the pull-up resistor enable signal. The enable signal enables the pull-up resistor when high and disables when low. ACCTR0_IN0 is the line to the reed switch. On the right side of ACCTR0_IN0 waveform, the line voltage is decreasing towards ground when the pull-up resistors are disabled. Beneath the charging waveform, the arrows represent the sample points. The Advanced Capture Counter samples the ACCTR0_IN0 voltage once the charging completes. The sensed ones and zeros are the sampled data. Finally the integrator waveform illustrates the output of the digital integrator. The integrator is set to 4 initially and counts to down to 0 before toggling the output low. Once the integrator reaches the low state, it needs to count up to 4 before toggling its output to the high state. The debounce logic filters out switch bounce or noise that appears for a short duration.

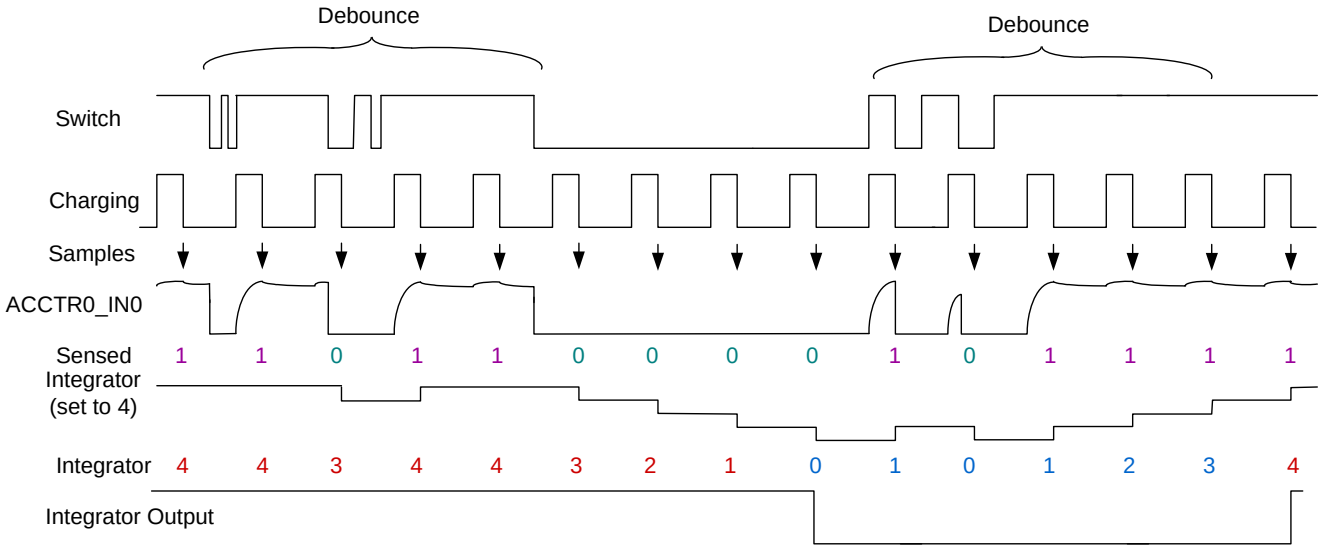


Figure 9. Debounce Timing

3.9. Reset Behavior

Unlike most SiM3L1xx peripherals, a device reset does not completely reset the Advanced Capture Counter. This includes a power on reset and all other reset sources. A device reset does not clear the counter values, and the Advanced Capture Counter registers do not reset to a default value except upon a power-on reset. The 24-bit counter values are persistent unless cleared manually by writing to the CONFIG register. Note that if the VBAT voltage ever drops below the minimum operating voltage, this may compromise contents of the counters.

The CONFIG register should normally be written only once after reset. This register sets the counter mode and resets the counter values when written.

Firmware should read the reset sources registers to determine the source of the last reset and initialize the Advanced Capture Counter accordingly.

When the Advanced Capture Counter resets, it takes some time (typically two RTC clock cycles) to synchronize between internal clock domains. The counters do not increment during this synchronization time.

3.10. Wake-up and Interrupt Sources

The Advanced Capture Counter has multiple interrupt and wake-up source conditions. To enable an interrupt, enable the source using the STATUS register and enable the Advanced Capture Counter interrupt in the NVIC. The Advanced Capture Counter interrupt service routine should read the interrupt flags in STATUS to determine the source of the interrupt and clear the interrupt flags.

To enable the Advanced Capture Counter as a wake-up source, enable the source in the STATUS and enable the Advanced Capture Counter as a wake-up source in the PMU module. Upon waking, firmware should read the PMU registers to determine the wake-up source. If the Advanced Capture Counter has woken the MCU, firmware should read the flag bits in STATUS to determine the Advanced Capture Counter wake-up source and clear the flag bits before going back to sleep. STATUS includes all interrupt and wake-up sources for the module.

3.11. Register Write Access

Writing to the ACCTR0 registers is synchronized to the RTC0TCLK domain. For this reason, some register writes may take many cycles before the actual register is updated. If a new write to a register is initiated before the previous write has completed, only the latest write may take. For this reason, the UPDTSTSF flag in the CONFIG register should be polled between consecutive writes, to ensure proper register updates.

3.12. Debug Signals

The Advanced Capture Counter module supports two output pins for hardware debug purposes (ACCTR0_DBG0 and ACCTR0_DBG1). The debug pins can be connected to the outputs of the comparators or integrators in either the LC or switch modes. To use the debug pins, the desired outputs should be selected with the DBGSEL field in the CONFIG register, and enabled using the DBGOEN in the DEBUGEN register.

4. Simple LC Resonant Example

This section details the basic steps to configure the Advanced Capture Counter in SiM3L1xx devices in LC resonant mode for an ac coupled circuit. There are a variety of topologies which can be used, but a simple tank circuit will be described here. The system counts pulses using the ACCTR0 in single channel mode. The LC tank circuit consists of a 470 µH inductor and a 39 pF capacitor. One side is grounded while the other side connects to a PMOS transistor and also to a 0.01 uF capacitor for ac coupling to the ACCTR0_LCIN0 pin. See Figure 10. This circuit is implemented on a small LC tank daughtercard that connects to the PB0 and PB1 headers on the SiM3L1xx MCU Card. Sections “LC Daughtercard Schematic” and “LC Daughtercard Bill of Materials” provide the full board schematic and BOM.

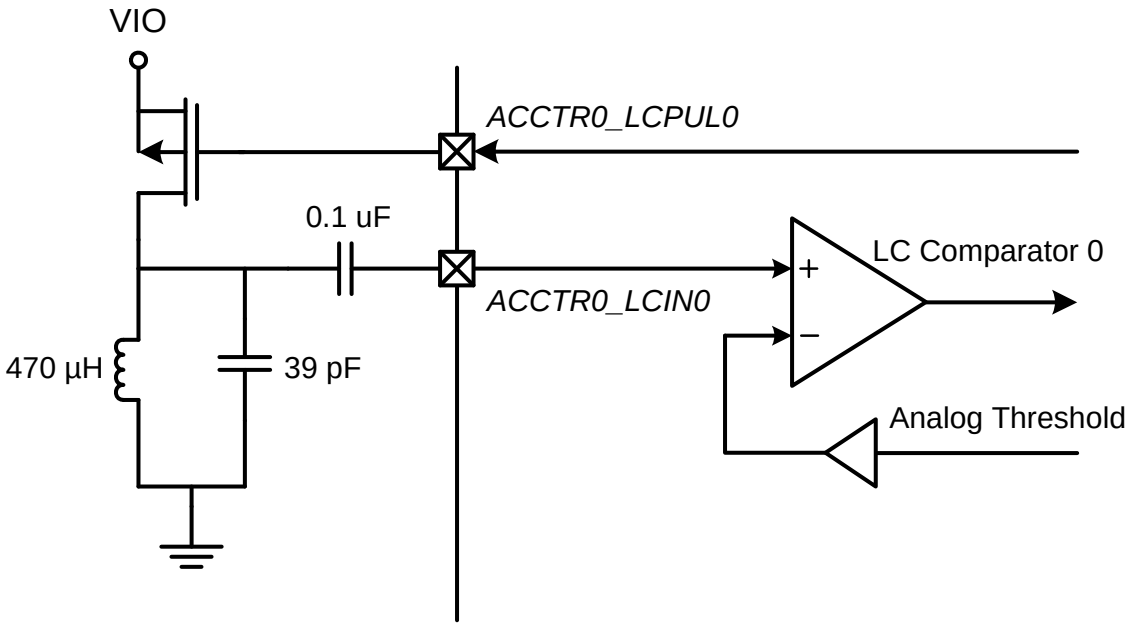


Figure 10. LC Resonant Example Schematic

The inductor must have a very low resistance in the tens of milliohms range. An inductor with even hundreds of milliohms will cause the dampening rate of the sine wave to be too fast for a useful circuit.

This example uses phases P and A. Phase P is a preconditioning phase that takes 2 cycles. In Phase A, the ACCTR0 module counts pulses and lasts 2 cycles.

The example uses digital hysteresis to prevent false counts when the impeller stalls near the decision point.

The shortest possible pulse is used to excite the tank. This is both to reduce power consumption and to prevent clipping of the measured signal.

The analog comparator hysteresis and threshold settings are used to make the peak count as stable as possible while retaining the largest minimum to maximum delta as possible. The comparator is also set to the 400 ns setting to ensure a large enough minimum to maximum delta for robust operation.

4.1. Hardware Setup

To run the ACCTR0 examples on the SiM3L1xx MCU Card with a fixed 3.3 V VBAT:

1. Connect a USB Debug Adapter to the 10-pin CoreSight connector (J14).
2. (Optional) Remove the three shorting blocks from J7 for power measurement.
3. (Optional) Remove the JP2 **Imeasure** shorting block and put a multimeter across (positive side on the bottom pin) for power measurement.
4. Move the **VBAT Sel** switch (SW2) to the middle +3.3V_VREG position.
5. Move the **VIO Sel** (SW8) and **VIORF Sel** (SW9) switches to the bottom VBAT position.
6. Connect the LC Resonant circuit to the ACCTR0 inputs (J20) or connect the ACCTR0 LC daughtercard to the PB0 and PB1 headers. The board should hang out over the edge of the MCU card and not cover the MCU.
7. Connect the 9 V power adapter to POWER (J6).
8. Download the code to the board.

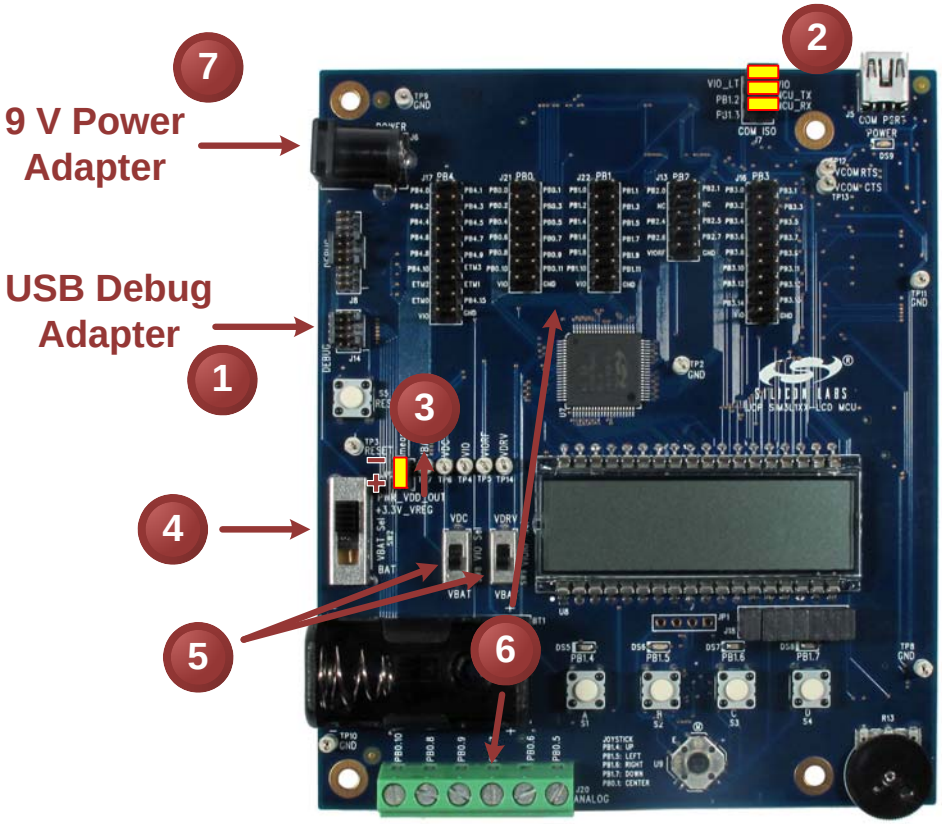


Figure 11. SiM3L1xx MCU Card ACCTR0 Example Configuration

See 5.6. "Downloading and Running the Example," on page 22 for instructions on using the example code.

5. Firmware ACCTR0 Module Configuration

The following steps outline the firmware setup to implement the LC resonant topology described in this section. The sequence is not unique to channel 0, and may be used to calibrate both channels at once in quadrature or dual mode.

1. Set the LCMD field to 0x4 to get a single ended, timed excitation pulse mode of operation.
2. Set the excitation pulse to be pulse low (PMD = 0x2) and set the bias pulses for internal use.
3. Set the bias timing offset to ½ cycle if needed. This gives ½ cycle of spacing between the bias pulse and the excitation pulse.
4. Set zone P to be 2 or 3 cycles long (3 cycles if using ½ cycle bias timing offset).
5. If using consecutive mode, set zone D to be the same number of cycles as zone P.
6. Set the PERIOD to 32 cycles or more which allows for non activity between samples and saves power.
7. Set the comparator threshold to full range (CMP0THR = 1) and a low coarse threshold (about 0x04 in CMP0CTH) for the initial calibration measurement.
8. Set the comparator low side hysteresis (CMPLHYS) to 0V and the high side hysteresis (COMHHYS) to 10 mV.
9. Select the fastest comparator speed setting (CMPMD = 0x3) if the LC resonant frequency is in the 500 kHz to 1 MHz range. For slower resonant frequencies the comparator speed setting can be lowered to save power.
10. Set the DBGOEN to 1 and write 0x2 to DBGSEL, and monitor both the ACCTR0_LCIN0 pin (comparator input) and the ACCTR0_DEBUG0 pin (comparator output) with an oscilloscope.
11. Perform an LC oscillator calibration by setting CLKCAL to 1. This will capture the number of LC oscillator cycles during a single RTC0TCLK period to the CLKCYCLES field. This number can then be divided to get a starting excitation pulse width for tuning the circuit. For example if the LC resonant frequency is 1 MHz, using a excitation pulse wider than 1us would actually leave the external excitation transistor on for too long and begin lowering the final energy going into the LC resonant circuit as well as wasting power. As the LC resonant circuit swings back the opposite direction it will be fighting against additional power coming through the external excitation transistor. As an example, for an oscillator that is calibrated and reports 0x52B cycles per RTC0TCLK, the desired excitation pulse width of 1us can be obtained by dividing 0x52B by 30.5 µs per RTC0TCLK period which gives 0x2B for the timer RELOAD value. This number still does not guarantee that the ringing seen at the ACCTR0_LCIN0 pin will not be too great and cause the ESD protection to turn on and clip the incoming signal. The ac coupling capacitor should be chosen to get a reasonable size input voltage swing.
12. For the example LC resonant circuit the voltage will be swinging above and below 0V while the ACCTR0_LCIN0 pin on the opposite side of the ac coupling capacitor will be swinging around VBAT/2. If the voltage swing at ACCTR0_LCIN0 goes much below 0 V or above 5 V, the ESD protection circuitry will turn on momentarily and inject or remove charge resulting in an unwanted dc offset. To prevent this dc offset, use the excitation calibration circuit.
13. Power VBAT at 3.6 V.
14. Set calibration to run until pass, calibration on, and set the START bit to start the sequencer.
15. The result of the calibration should find an excitation pulse width that is wide enough to produce a good waveform but not so wide that it would cause ESD clipping. This calibration only generates the 5 LSBs of the 12-bit RELOAD field. It is assumed that the user has provided the 7 MSBs to the RELOAD field from the oscillator calibration step described in Step 11.
16. The calibration result is presented in the PUVAL field. These 5 bits should be written into RELOAD[4:0], leaving the 7 MSBs intact.
17. Monitor the waveform on an oscilloscope at ACCTR0_LCIN0 to double-check that there is no dc offset added by clipping.
18. Set the coarse threshold (CMP0CTH) to a mid level such as 0x20 for normal operation.

19. The integrator/debouncer settings can be used to filter some noise out of the system but integration also increases latency. More samples are needed before the integrator recognizes a new high or low value. To begin with, set the integrator debounce high and low settings to a low value such as 0x02. This can be increased if needed in a noisy environment.
20. There is also digital hysteresis for the discriminator that can be used to when the wheel stops at a location that produces readings close to the discriminator value. However, there needs to be enough headroom to use the digital hysteresis at low supply. In other words having a maximum LCCOUNT0 value of 0x09 and a minimum LCCOUNT0 value of 0x06 at 1.8 V would not allow enough headroom to set the digital hysteresis to a value of 0x03. Initially leave the digital hysteresis at a value of 0x00 or 0x01 unless the system is very noisy.
21. Disable the automatic tracking mode and the center discriminator mode (ACDEN and ATRKEN = 0).
22. Power VBAT at 1.8 V.
23. Next, read the LCLIMITS register to reset the MAX0 to 0x00 and the MIN0 to 0xFF.
24. Run the wheel several times to capture the MAX and MIN values at 1.8 V.
25. Enable automatic tracking mode (ATRKEN = 1) and automatic center discriminator mode (ACDEN = 1). This will lock in a small window size for 1.8 V where the delta between MAX0 and MIN0 is the smallest due to the low supply. Had this window been locked in at 3.6 V, the tracking window would be too large to work well when the voltage dropped to 1.8 V.
26. As the VBAT voltage varies between 1.8 and 3.6 V the tracking window will move up and down to follow the maximum and minimum LCCOUNT values. These LCCOUNT values can vary quite a bit with voltage, and the tracking mechanism allows the pulse counter to keep the discriminator centered as the supply voltage changes. In quadrature mode, this maintains a good duty cycle with overlap between the two inputs. Without the overlap, the quadrature method used for directional counting would only see 3 states instead of 4 states.

5.1. Calibration Mode

When the firmware first starts running, it enters the **calibration** phase. To calibrate the system, spin the meter several times and press the center joystick button on the MCU card. After calibration, the firmware enters **active** mode.

While in **calibration** mode, the hardware keeps track of the minimum and maximum peaks seen. When calibration ends, the delta between the minimum and maximum fixes at the current value, and the hardware will automatically slide the minimum to maximum delta window as it sees new minimum and maximum values. See the ATRKEN bit description in the device reference manual for more details on how this automatic tracking works.

After calibration, the hardware also automatically sets the decision point to the average of the minimum to maximum delta (ACDEN). With both ACDEN and ATRKEN set, the ACCTR0 module automatically adjusts to changes in the peak count caused by outside influences like voltage or temperature changes.

It is recommended that calibration be performed at the lowest expected voltage of the system operating range.

5.2. Active Mode

Active mode allows the IDE to interact with the ACCTR0 module. During **active** mode, the firmware displays the current ACCTR0 count on the LCD and updates the count every 100 ms.

The ACCTR0 debug signals are also routed out to the pins in this mode.

The ringing of the circuit can be observed on the ACCTR0_LCIN0 pin (TP3 on the LC daughtercard), which is the input to the LC comparator. The number of peaks counted can be observed on the comparator output, or ACCTR0_DBG0 (TP1). The signal controlling the excitation pulses, ACCTR0_LCPUL0 (TP5), can be used to trigger the oscilloscope.

5.3. Sleep Mode

When SW4 is pressed while in **active** mode, the system enters **sleep** mode, which is the lowest power mode using Power Mode 8 (PM8). The system continues counting pulses but does not use the LCD to conserve power.

The system remains asleep until the center joystick button is pressed. The system then enters **active** mode and updates the LCD to show the total count (including sleep counts). The expected current of the MCU card in this mode with no scope probes attached is 2.5 µA.

Transitions between **sleep** and **monitor** modes are not supported, and the system must enter **active** mode first before transitioning to the next low power mode.

5.4. Monitor Mode

When SW3 is pressed while in **active** mode, the system enters **monitor** mode. In this mode, the part enters Power Mode 8 (PM8) with the LCD displaying the last value. The part remains in PM8 counting pulses until a configurable number of pulses are seen. At this time, the core wakes up, updates the display, and then goes back to sleep. The number of pulses between wake-up events is configured using the ACCTR_ALARM_COUNT constant found in myACCTR0.h.

Pressing the center joystick button will exit **monitor** mode and return the system to **active** mode. Transitions between **sleep** and **monitor** modes are not supported, and the system must enter **active** mode first before transitioning to the next low power mode.

5.5. Connecting the Example to a Meter

There are several relevant ACCTR0 settings that will vary from meter to meter. These settings should be determined by a process of educated trial and error.

5.5.1. CMP0CTH Full Range Threshold

The CMP0CTH setting controls the analog comparator threshold. The larger the value in this field, the larger the peaks need to be in order to be counted by the hardware. Increasing this value can reduce the amount of noise seen by the peak counter.

5.5.2. CMPLHY and CMPHHY Hysteresis

These fields control the hysteresis of the analog comparator. The setting can be used to reduce noise and help filter out common mode drift of the tank oscillation.

5.5.3. CMPMD Response Time

The CMPMD field controls the response time of the analog comparator. Slower response time reduces power but can also filter the LC signal. Typically, pulses a the end of the LC response decay and are no longer counted when response time is reduced.

5.5.4. ZONEA, ZONEB, ZONEC, ZONED, ZONEP

These fields controls the length of each phase. The longer the module is active during a phase, the more current the system draws. The time of the P phase must be at least 2 cycles (value of 1) to ensure that the LC oscillations have the correct DC bias.

The width of the zone during which peaks are counted must be wide enough to encompass both the minimum and maximum counts. Any peaks outside this phase will not be seen and will not contribute to the minimum to maximum delta.

An idle zone may be used to save power in situations where the tank rings for a long time. For example, for a tank that rings with 10 peaks every RTC0 cycle, let us set the measured minimum to 35 peaks and the maximum peaks to 47. In order to convert the maximum number of peaks, the module must be set to measure for 5 RTC0 cycles, or 50 peaks, which will consume more power than needed. Since peaks 1 through 35 are always present, these don't need to be counted by the hardware in order to differentiate between the minimum and maximum. Instead, the hardware can be configured to sit in an idle A zone before the counting B zone. If zone A is 3 RTC0 cycles and zone B is 2 RTC0 cycles, the hardware will ignore peaks 0-30 and count peaks 30-50. The hardware will measure the full 12 peak delta but only have to count for 2 RTC0 cycles, saving power.

Finally, note that the zone width is in units of RTC0 clock cycles. Running from a 32 kHz crystal will provide higher

resolution than running from the 16 kHz internal Low Frequency Oscillator since the clock cycles will be faster. In many cases, switching to the Low Power Oscillator will increase power consumption since the gain of using the LPOSC is offset by the fact that the active phase of the ACCTR0 must be longer due to the lack of timing resolution.

5.5.5. PERIOD

The PERIOD field determines how often the ACCTR0 module samples the sensor. It is based on the RTC0 clock period.

5.5.6. LCD0HYS Discriminator 0 Hysteresis

The LCD0HYS field controls the digital (peak count) hysteresis. This field should be set high enough to avoid false counts due to peak count noise, but low enough to allow adequate threshold minimum to maximum delta margin.

5.5.7. RELOAD

The RELOAD field controls the width of the excitation pulse. This field should be as small as possible while enabling sufficient ringing of the LC tank.

Care should be taken that the ringing does not exceed 5 V or drop below ground. Signals greater than 5 V or less than ground will be clipped internally by hardware's ESD protection circuitry.

5.5.8. HDBTH, LDBTH, and INTEGDCEN Debounce

The debounce options can be used to require N high or low counts before a low or high is recognized in the digital comparator. This can be used to extend the effectiveness of LCD0HYS in some cases.

This debouncing is not implemented in the simple example.

5.6. Downloading and Running the Example

To download the AN741_ACCTR_Simple_LC_Example code to an SiM3L1xx MCU Card:

1. Configure the SiM3L1xx MCU Card according to the instructions in 4.1. "Hardware Setup," on page 18.
2. Open the AN741_ACCTR_Simple_LC_Example project in either Keil µVision or the Precision32 IDE.
3. Compile and download the code to the device.
4. (Optional) Disconnect the USB Debug Adapter and any attached scope probes for power measurement.
5. Reset the device.
6. The board will enter **calibration** mode. Spin the meter several times, and then press the center button of the joystick (U9) to finish calibration.
7. The meter is now in **active** mode. The current count can be observed on the LCD, and a scope can be used to observe signals on the ACCTR0 module inputs.
8. Press SW3 to enter **monitor** mode. This mode places the device in a lower power state where the count on the LCD updates every 0x10 counts.
9. (Optional) Measure the power consumption of the device.
10. Press the center button of the joystick (U9) to return to **active** mode.
11. Press SW4 to enter **sleep** mode, the lowest power mode. The LCD will no longer display the current ACCTR0 module count.
12. (Optional) Measure the power consumption of the device.
13. Press the center button of the joystick (U9) to return to **active** mode and see pulses counted while in the lowest power state.

Note: The USB Debug Adapter and any connected scope probes must be disconnected from the board when taking power measurements. The state of the ACCTR0 module can be observed in the IDE when in **active** mode with the debug adapter connected. This is a good way to observe the effects of the various ACCTR0 settings.

6. LC Daughtercard Schematic

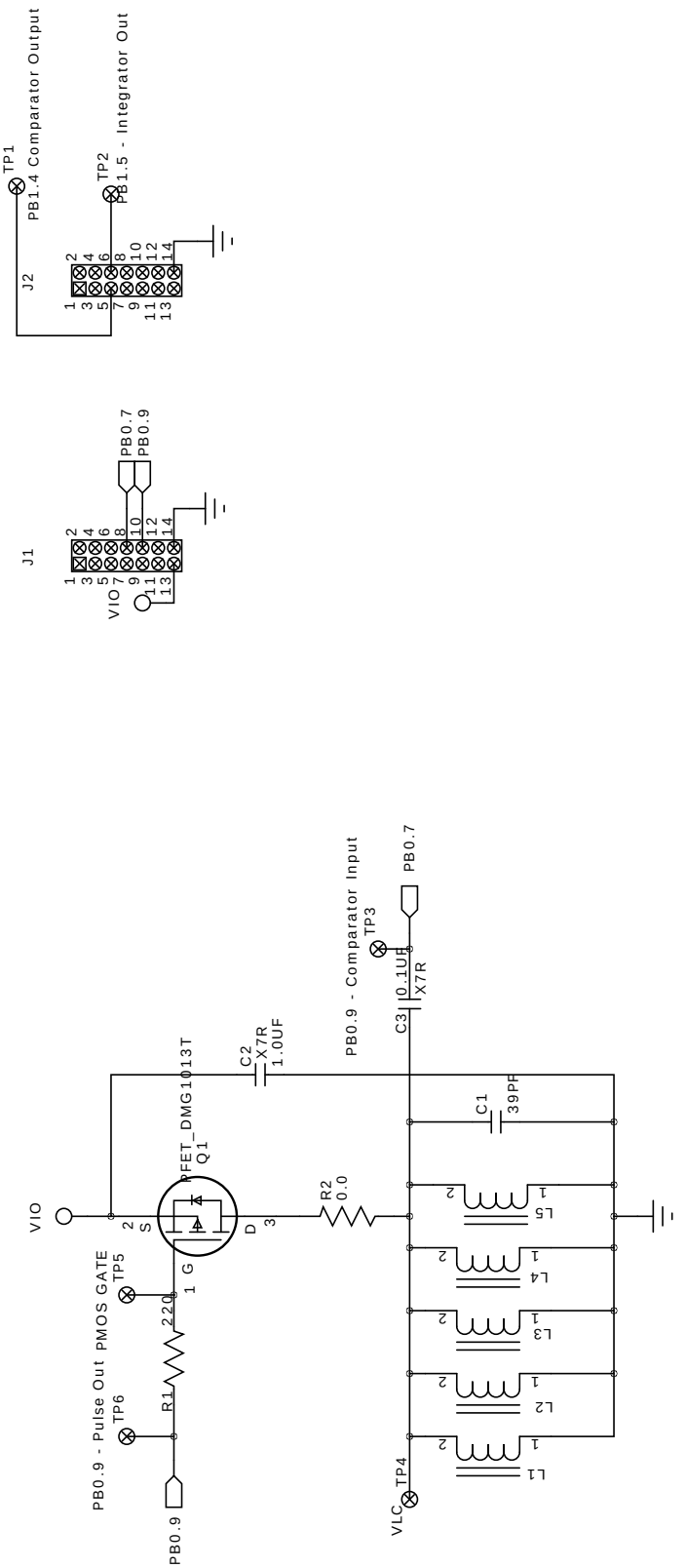
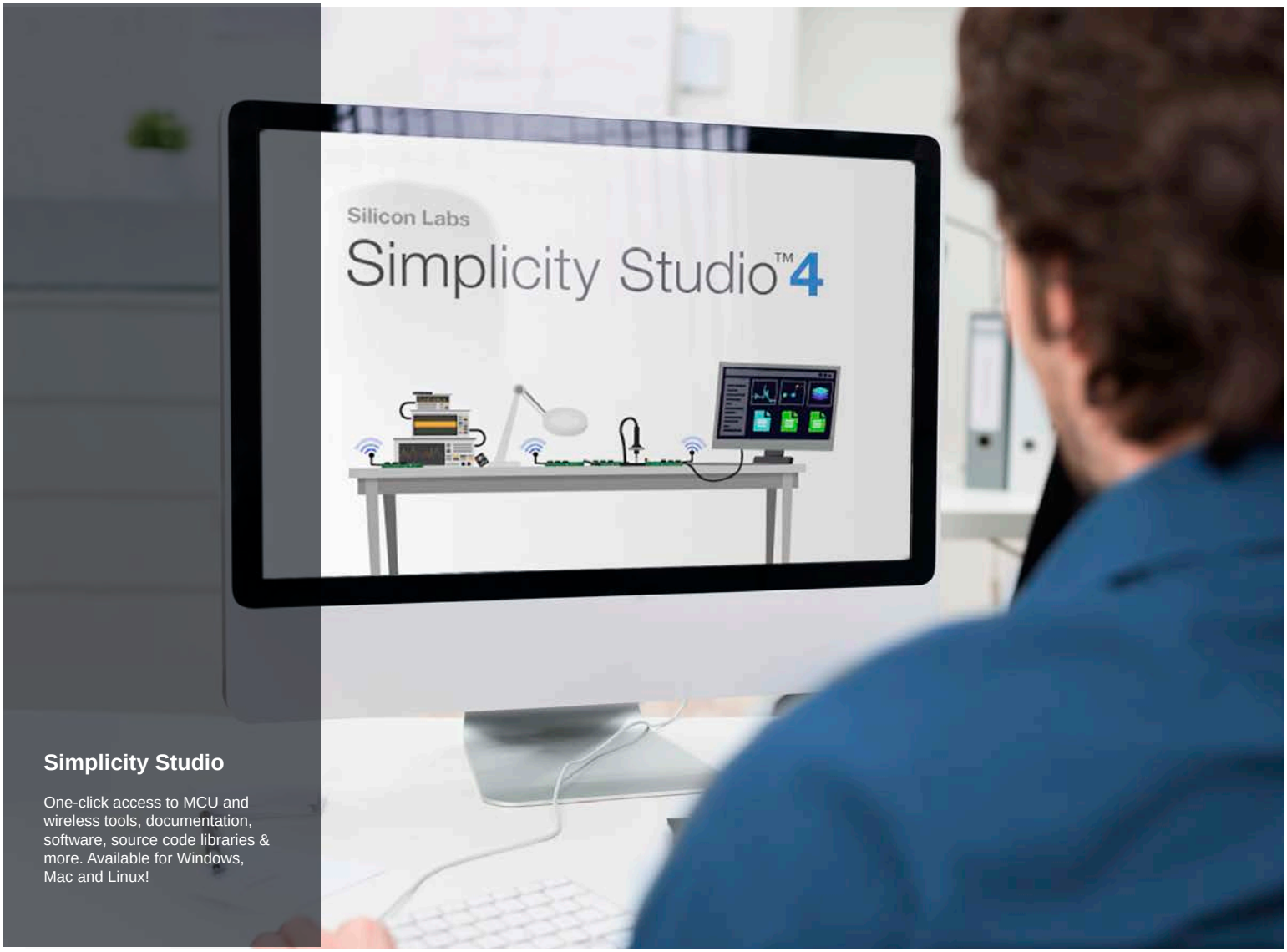


Figure 12. ACCTR0 LC Daughtercard Schematic (1 of 1)

7. LC Daughtercard Bill of Materials

Table 3. ACCTR0 LC Daughtercard Bill of Materials

Reference	Part Number	Source	Description
C3	C0603C104J3RACTU	Kemet	CAP, 0.1 UF, X7R, CERAMIC, 0603, 25 V, ±5%, OR EQ, RoHS
C2	C1608X7R1C105K	TDK Corporation	CAP CERAMIC, 1.0 UF, X7R, 0603, 16 V, ±10%, OR EQ, RoHS
C1	ECJ-2VC1H390J	Panasonic Electronic Components	CAP, 39PF, NPO, CERM, 0805, 50 V, ±5%, OR EQ, RoHS
J1-2	PPTC072LFBN-RC	Sullins Connector Solutions	STAKE HEADER FEMALE, 2X7, 0.1" CTR, GOLD, OR EQ, RoHS
L4	18R474C	Murata Power Solutions Inc	Inductor, 13.7 mm Drum Core, 470 uH, 465 mOhm, No subs
Q1	DMG1013T-7	Diodes Inc	MOSFET, P-CH, 20 V, LL, Low input C, SOT-523, RoHS
R2	ERJ-3GEY0R00V	Panasonic Electronic Components	RES, 0.0, SMT, 0603, 1/10W, ±5%, OR EQ, RoHS
R1	ERJ-3EKF2200V	Panasonic Electronic Components	RES, 220 OHM, SMT, 0603, 1/16W, ±1%, OR EQ, RoHS
Components Not Installed			
L1	AIRD-03-471K	Abracon Corporation	Inductor, 16.5 mm Drum Core, 470 uH, 187 mOhm, No subs Not Installed (NI)
L2	AIRD-02-471K	Abracon Corporation	Inductor, 21 mm Drum Core, 470 uH, 355 mOhm, No subs Not Installed (NI)
L3	AIRD-01-471K	Abracon Corporation	Inductor, 28 mm Drum Core, 470 uH, 636 mOhm, No subs Not Installed (NI)
L5	P0752.474NLT	Pulse Electronics Corporation	Inductor, 9 mm Drum Core, 470 uH, 1.46 Ohm, No subs Not Installed (NI)



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