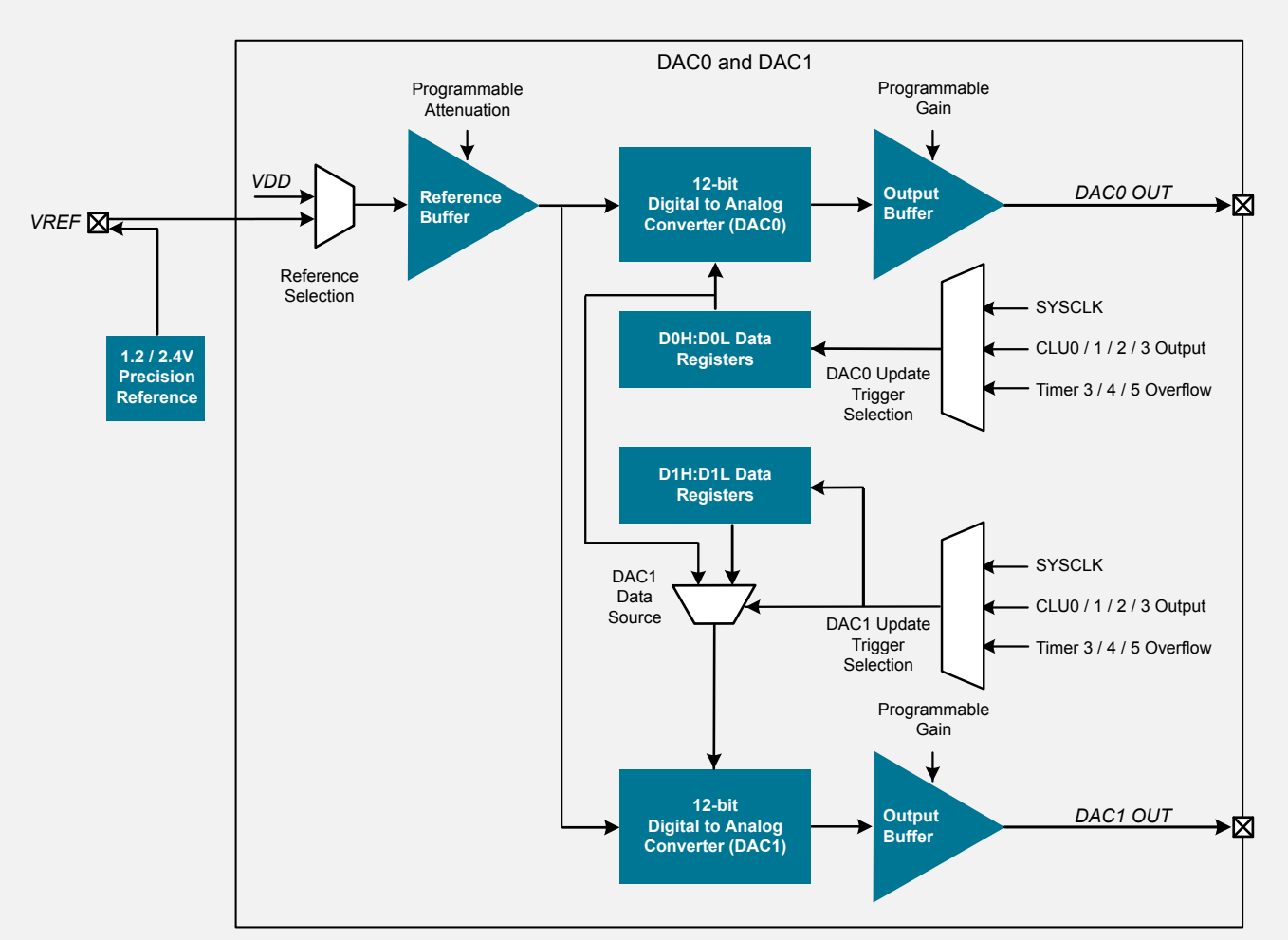
AN920: Using the EFM8LB1/BB3 DAC

This application note describes how to use the EFM8LB1 and EFM8BB3 12-bit, voltage-output Digital to Analog Converter (DAC), which can produce rail-to-rail output voltages when driving high load resistances.

The DACs can accommodate load resistances as low as 1 kΩ across a narrower output voltage range. The general operation of the peripheral is explained, and firmware examples are provided.

KEY POINTS

- 12-bit resolution
- Up to 4 DACs with output synchronization
- Output update via external I/O, timer or firmware



1. DAC Overview

The EFM8LB1 and EFM8BB3 DAC can output a configurable constant voltage between 0 V up to 3.6 V when using the maximum 3.6 V VDD as the reference. The DACs do not require any clocks to maintain the output voltage. Up to four DACs (DAC0, DAC1, DAC2, DAC3) are included, organized in pairs: DAC0 and DAC1 form a pair, and DAC2 and DAC form a pair. A block diagram of one DAC pair is shown below. Each DAC has 12-bit resolution.

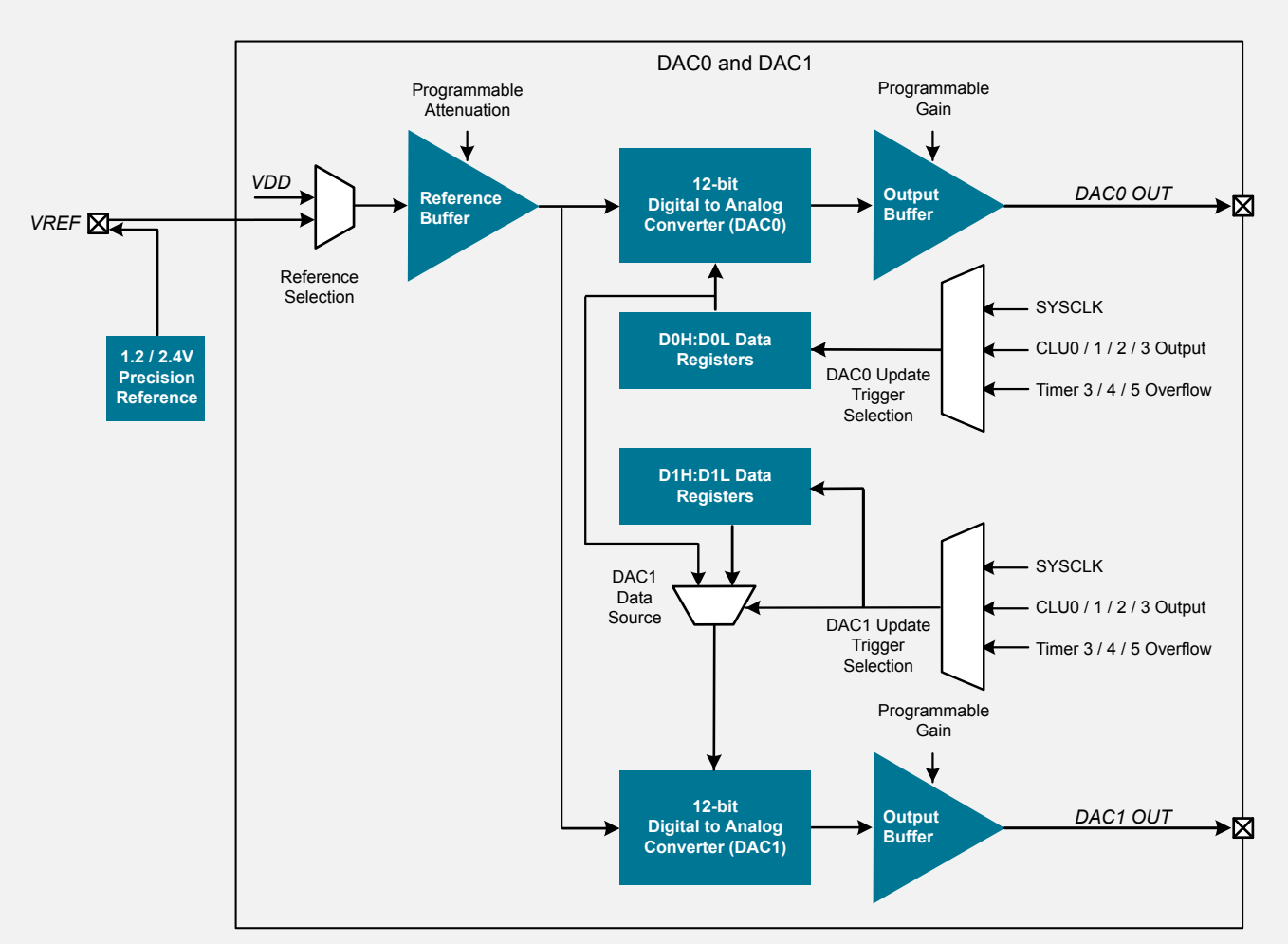


Figure 1.1. DAC0 and DAC1 Pair Block Diagram

2. General Operation

2.1 Output Voltage

The output voltage depends on the 12-bit data input, the reference voltage, the reference buffer attenuation setting, and the output buffer gain according the following formula:

$$\text{DAC Output (V)} = \left(\frac{\text{12-bit Data Input}}{2^{12}}\right) \text{x (Reference Voltage) x (Reference Attenuation) x (Output Buffer Gain Attenuation)}$$

For example, if:

- 12-bit data input = 0xFFF
- Reference voltage = 2.4V
- Reference Attenuation = 1/2.4
- Output Gain = 2.4

Then,

$$\text{DAC Output (V)} = \left(\frac{0xFFF}{2^{12}}\right) \text{x (2.4V) x} \left(\frac{1}{2.4}\right) \text{x (2.4) = (2.4V - 1LSB)}$$

The 12-bit data input, reference voltage, reference buffer attenuation, and output buffer gain are discussed in further detail in the following sections.

2.2 Data Word

The 12-bit data input to the DAC is the combination of the data high (DACnH) and data low (DACnL) registers. When writing to the data registers, always write to the DACnL register first, then write to the DACnH register. By default, the data should be right justified (LJST bit in the DACnCF0 register is 0). When right justified, the lower 8 data bits should be written to DACnL, and the upper 4 data bits should be written to the DACnH. When left justified (LJST is 1), the lower 4 data bits should be written the upper four bits of DACnL, and the upper 8 data bits should be written to DACnH.

2.2.1 DAC1 and DAC3 Features

The second DAC in each pair has multiple data input options. Using DAC1 in the DAC0/DAC1 pair as an example, the D1SRC field in the DACGCF0 register allows four different data sources for DAC1:

- The data in DAC1H:DAC1L (default setting)
- The one's complement of the value in DAC1H:DAC1L
- The data in DAC0H:DAC0L
- The one's complement of the value in DAC0H:DAC0L

This allows firmware to program DAC0H:DAC0L and see the value reflected on the DAC0 and DAC1 outputs, with DAC1 producing either the same voltage as DAC0 or its complement. Furthermore, the DAC1 Alternating Mode Enable bit (D1AMEN) provides additional options for generating DAC1 input data.

- When D1AMEN is cleared, DAC1 always updates from the data source selected by the D1SRC field (default setting)
- When D1AMEN is set, the data source is determined by the logic state of the DAC1 trigger source
  - When the DAC1 trigger is logic low, DAC1 uses the data in DAC1H:DAC1L
  - When the DAC1 trigger is logic high, DAC1 uses the data source specified by D1SRC

When using the Alternating Mode feature, the trigger source must be one of the Configurable Logic Units, and the minimum high and low times for this trigger must be at least two system clock cycles.

2.3 Reference Voltage

The minimum reference voltage is 1.15 V and the maximum is 3.6 V (maximum VDD). The reference for each DAC pair can be indepentely selected using the DxxREFSL bit in the DACGCF0 register. The reference voltage options are:

- VDD pin (default setting)
- VREF pin

The minimum VDD is 2.2 V, and the maximum VDD is 3.6 V. However, using VDD as the DAC reference is not recommended because supply pins are typically unstable.

The internal precision 1.2/2.4 V voltage reference can be routed to the VREF pin. By default, the 1.2/2.4 V voltage reference is not routed to the VREF pin. Write 0x1 to the VREFSEL field in the REF0CN register to route 1.2 V to the VREF pin, or write 0x2 to VREFSEL to route 2.4 V to VREF pin. Alternatively, an external supply can be connected the VREF pin. When using the VREF pin with the internal reference or an external reference, the pin should should be configured to analog mode using the PnMDIN register.

2.3.1 Reference Buffer Attenuation and Output Buffer Gain

The reference buffer is connected to an attenuation stage. The reference voltage scaled by 1/2, 1/2.4 or 1/3 using the DxxREFGN field in the DACGCF2 register. The DAC output is connected to a gain stage. The DAC output can be scaled by 2, 2.4, or 3 using the DRVGAIN field in the DACnCF1 register. The table below provides a summary of the reference voltage ranges, reference buffer attenuation settings, output buffer gain settings, and the resulting overall gain.

Table 2.1. DAC Reference and Gain Settings

Reference Range	DxxREFGN setting	Reference Buffer Attenuation	DRVGAIN setting	Output Buffer Gain	Overall Gain
1.15V to 1.8V	0x0	Low (Gain = 1/2)	0x0	Low (Gain = 2)	1
			0x1 (default setting)	Medium (Gain = 2.4)	1.2
			0x2	High (Gain = 3)	1.5
1.6V to 2.55V	0x1 (default setting)	Medium (Gain = 1/2.4)	0x0	Low (Gain = 2)	0.8
			0x1 (default setting)	Medium (Gain = 2.4)	1
			0x2	High (Gain = 3)	1.2
2.2V to 3.6V	0x2	High (Gain = 1/3)	0x0	Low (Gain = 2)	0.667
			0x1 (default setting)	Medium (Gain = 2.4)	0.833
			0x2	High (Gain = 3)	1

2.4 Turning the DAC On/Off

Each of the DACs has an enable bit (EN bit in the DACnCF0 register) that turns on the DAC and allows its output buffer to drive its respective pin. By default, all DACs are disabled. The enable bit only affects the analog circuitry and pin interface associated with the DAC; the registers may be accessed by firmware even if the associated DAC is disabled.

By default, any system reset will disable the DACs and reset all associated registers. By setting the Reset Mode bit (RSTMD) in register DACnCF0, the output of the DAC will persist through any system reset except for a power-on reset.

2.5 Output Pin

Each DAC has a single output pin at a fixed location indicated in the table below.

Table 2.2. DAC Output Pin Assignments

DAC Output	32-Pin Packages	24-Pin Packages
DAC0 Output	P3.0	P2.0
DAC1 Output	P3.1	P2.1
DAC2 Output	P3.2	P2.2
DAC3 Output	P3.3	P2.3

When using the DAC output, the pin should be configured to analog mode using the PnMDIN register.

2.6 Update Trigger

By default, the DAC output is updated by hardware by a trigger. The trigger for each DAC is independently selectable using the UPDATE field in DACnCF0 register, and the options are shown below:

- SYSCLK (default setting)
- Timer 3 high byte overflow
- Timer 4 high byte overflow
- Timer 5 high byte overflow
- Configurable Logic output 0 rising edge
- Configurable Logic output 1 rising edge
- Configurable Logic output 2 rising edge
- Configurable Logic output 3 rising edge

When using SYSCLK as the update trigger, the DAC output is updated one system clock after writing to DACnH. Using the Configurable Logic output allows I/O pins to trigger the update.

The DnUDIS bit is useful for synchronizing the update of multiple DACs that share the same update trigger. See the procedure below:

1. Write 1 to DnUDIS for the desired DACs. Trigger events will not update the DAC outputs.
2. Write the data input registers for multiple DACs.
3. Write 0 to DnUDIS for the desired DACs, allowing the DACs to update simultaneously on the next trigger event.

3. Firmware Examples

3.1 DAC Example

This is the simplest example that demonstrates DAC functionality. This example uses the internal 2.4 V reference and outputs a 1 kHz sine wave on all four DACs. One period of a sine wave is stored in flash. The DAC update trigger is Timer 3, configured to overflow at 200 kHz. When Timer 3 overflows, the DAC output will update, and the Timer 3 ISR will fire. In the Timer 3 ISR, the next DAC output is loaded in the data registers, but will not be reflected in the DAC output until the next trigger event.

This example is available in Simplicity Studio under [**Software Examples**]>[**Kit: EFM8LB1/EFM8BB3 Starter Kit**]>[**DAC**].

3.2 Function Generator

This example builds upon the simple DAC example. It uses Timer 4 as the update trigger. The available functions are sine, square, triangle, sawtooth, and windowed sine, selectable using the joystick on the STK. The frequency can also be selected using the joystick. The options are 10 Hz, 20 Hz, 50 Hz, 100 Hz, 200 Hz, 500 Hz, 1 kHz, 2 kHz, and 5 kHz. The function and frequency are displayed on the screen.

This example is available in Simplicity Studio under [**Software Examples**]>[**Kit: EFM8LB1/EFM8BB3 Starter Kit**]>[**Demos**].

Simplicity Studio

One-click access to MCU tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!

www.silabs.com/simplicity

MCU Portfolio
www.silabs.com/mcu

SW/HW
www.silabs.com/simplicity

Quality
www.silabs.com/quality

Support and Community
community.silabs.com

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com