

EFM32 Leopard Gecko STK	
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Revision History	
Rev.	Description
A00	Initial version for series production
A01	Updated EFM32 to Leopard Gecko Rev.D
A02	Added test points for EFM USB. Fixed small error on PCB.



STK		Schematic Title	
		EFM32 Leopard Gecko Starter Kit	
Designed: DDB Approved: JNO		Page Title	
		Title Page	
Size A3	BOM Doc No:	Document number	Revision
		BRD2201A	A02
Design Created Date: Wednesday, December 03, 2008		Sheet Created Date Saturday, March 21, 2009	Sheet Modified Date Thursday, June 14, 2012
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Breakout Connections

MCU_PA[15:0] >>

- MCU_PA12
- MCU_PA13
- MCU_PA14

TPJ100
TPJ101
TPJ102

MCU_PB[15:0] >>

- MCU_PB9
- MCU_PB10
- MCU_PB11
- MCU_PB12

TPJ145
TPJ146
TPJ103
TPJ104

MCU_PC[11:0] >>

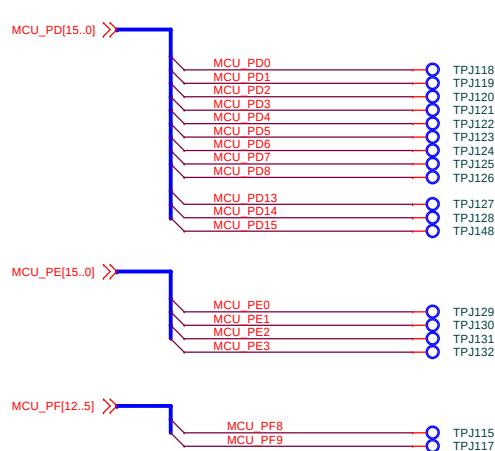
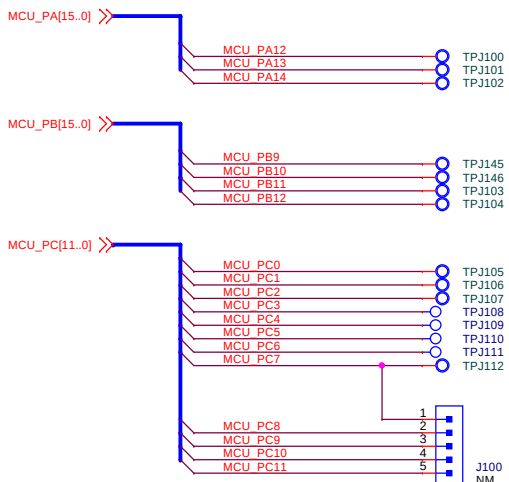
- MCU_PC0
- MCU_PC1
- MCU_PC2
- MCU_PC3
- MCU_PC4
- MCU_PC5
- MCU_PC6
- MCU_PC7

TPJ105
TPJ106
TPJ107
TPJ108
TPJ109
TPJ110
TPJ111
TPJ112

MCU_PC8
MCU_PC9
MCU_PC10
MCU_PC11

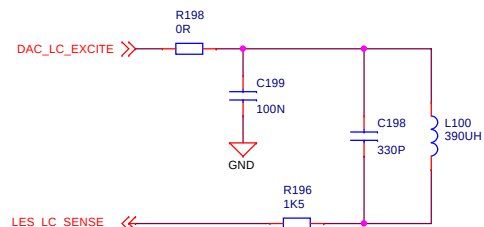
1
2
3
4
5

J100
NM



LESENSE LC-Sensor

The diagram illustrates the LC-Sensor circuit for the LESENSE module. It features a DAC output (DAC_LC_EXCITE) connected to a resistor R198 (0R). This is followed by a series combination of a capacitor C199 (100N) and an inductor L100 (390UH). A parallel combination of a capacitor C198 (330P) and the inductor L100 is connected to ground. The output is taken from the junction between the inductor and the parallel capacitor, passing through a resistor R196 (1K5) to the LES_LC_SENSE input.



Power

VMCU

3V3

5V

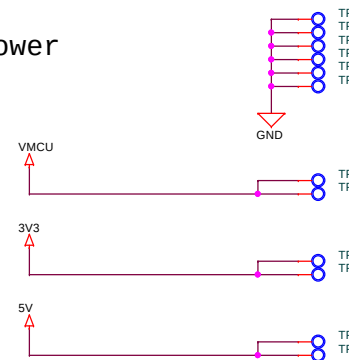
TPJ139
TPJ140

TPJ141
TPJ142

TPJ143
TPJ144

TPJ133
TPJ134
TPJ135
TPJ136
TPJ137
TPJ138

GND



32MB NAND Flash

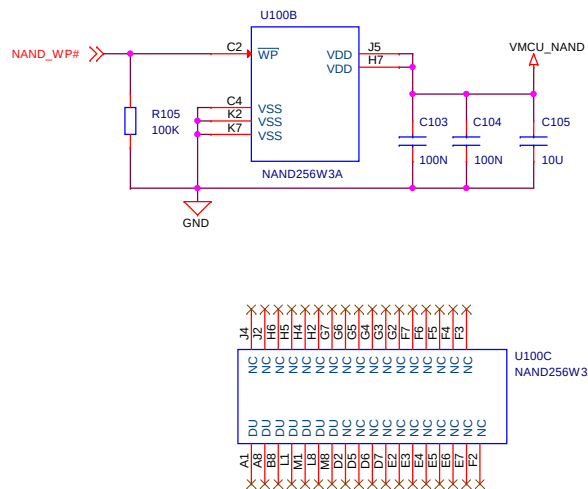
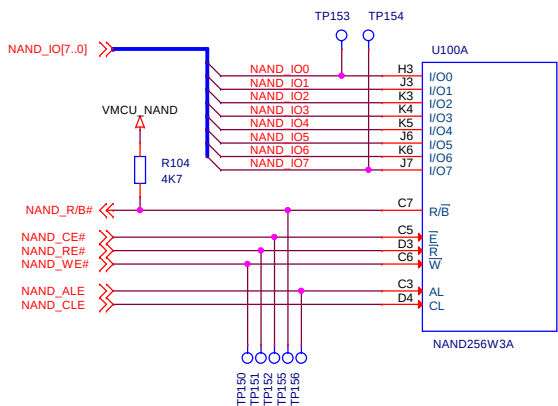
The diagram illustrates the connection of a 32MB NAND Flash to a U100A microcontroller. The U100A chip is shown with various pins connected to the NAND flash and other components.

U100A Pin Connections:

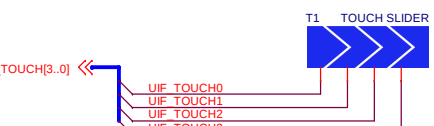
- I/O Pins:** I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7 are connected to the NAND flash data lines.
- NAND Flash Pins:** NAND_I0, NAND_I1, NAND_I2, NAND_I3, NAND_I4, NAND_I5, NAND_I6, NAND_I7 are connected to the NAND flash data lines.
- Control Pins:** NAND_CE#, NAND_RE#, NAND_WE#, NAND_ALE, NAND_CLE are connected to the NAND flash control lines.
- Other Pins:** NAND_RB#, NAND_CE#, NAND_RE#, NAND_WE#, NAND_ALE, NAND_CLE are connected to the NAND flash control lines.

Resistor and VMCU NAND: A 4K7 resistor (R104) is connected between the NAND flash and the VMCU NAND block. The VMCU NAND block is connected to the NAND flash.

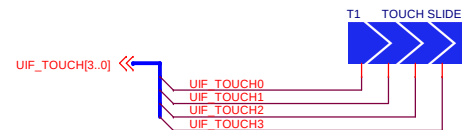
TP Pins: TP150, TP151, TP152, TP153, TP154, TP155, TP156 are connected to the NAND flash data lines.



Touch Slider



The diagram illustrates the hardware connection for a Touch Slider. On the left, a red label `UIF_TOUCH[3:0]` is connected to a blue bus structure. This bus branches into four individual lines, each labeled `UIF_TOUCH0`, `UIF_TOUCH1`, `UIF_TOUCH2`, and `UIF_TOUCH3`. These four lines are connected to the inputs of a blue block labeled `T1 TOUCH SLIDER`. The block has four output lines extending to the right.



User pushbuttons

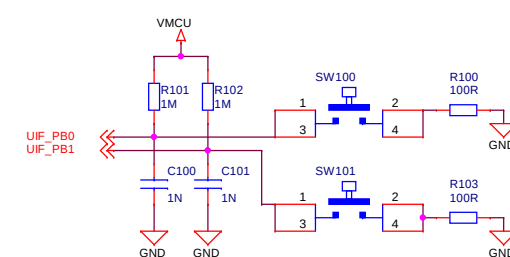
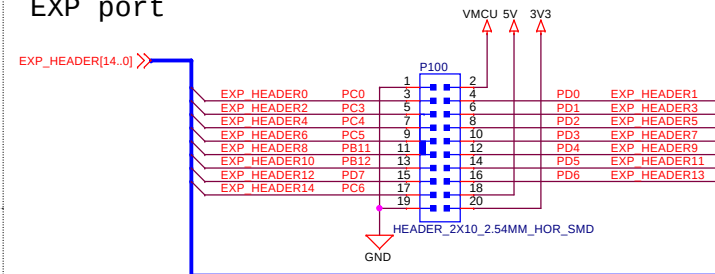


Diagram illustrating the EXP port connections for the P100 connector. The connections are as follows:

- EXP_HEADER0 (PC0) to Pin 1
- EXP_HEADER2 (PC3) to Pin 3
- EXP_HEADER4 (PC4) to Pin 5
- EXP_HEADER6 (PC5) to Pin 7
- EXP_HEADER8 (PB11) to Pin 9
- EXP_HEADER10 (PB13) to Pin 11
- EXP_HEADER12 (PB7) to Pin 13
- EXP_HEADER14 (PC6) to Pin 15
- GND to Pin 19
- VMCU 5V to Pins 2, 4, 6, 8, 10, 12, 14, 16, 18, 20
- 3V3 to Pins 3, 5, 7, 9, 11, 13, 15, 17, 19
- PD0 to EXP_HEADER1
- PD1 to EXP_HEADER3
- PD2 to EXP_HEADERS
- PD3 to EXP_HEADER7
- PD4 to EXP_HEADER9
- PD5 to EXP_HEADER11
- PD6 to EXP_HEADER13



SPI	MOSI - PD0 MISO - PD1 CLK - PD2 CS - PD3
I2C1	SDA - PC4 SCL - PC5
UART	TX - PD0 RX - PD1
LEUART	TX - PD4 RX - PD5

SPI	MOSI-PD0 MISO-PD1 CLK-PD2 CS-PD3
I2C1	SDA-PC4 SCL-PC5
UART	TX-PD0 RX-PD1
LEUART	TX-PD4 RX-PD5

Q100
2N235A
TEMPT6200FX01

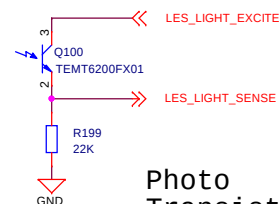
R199
22K

GND

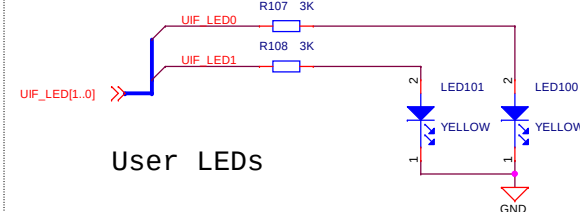
LES_LIGHT_EXCITE

LES_LIGHT_SENSE

Photo Transistor

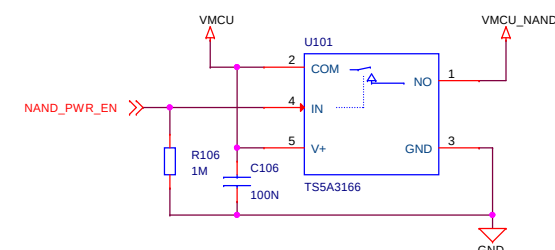


User LEDs



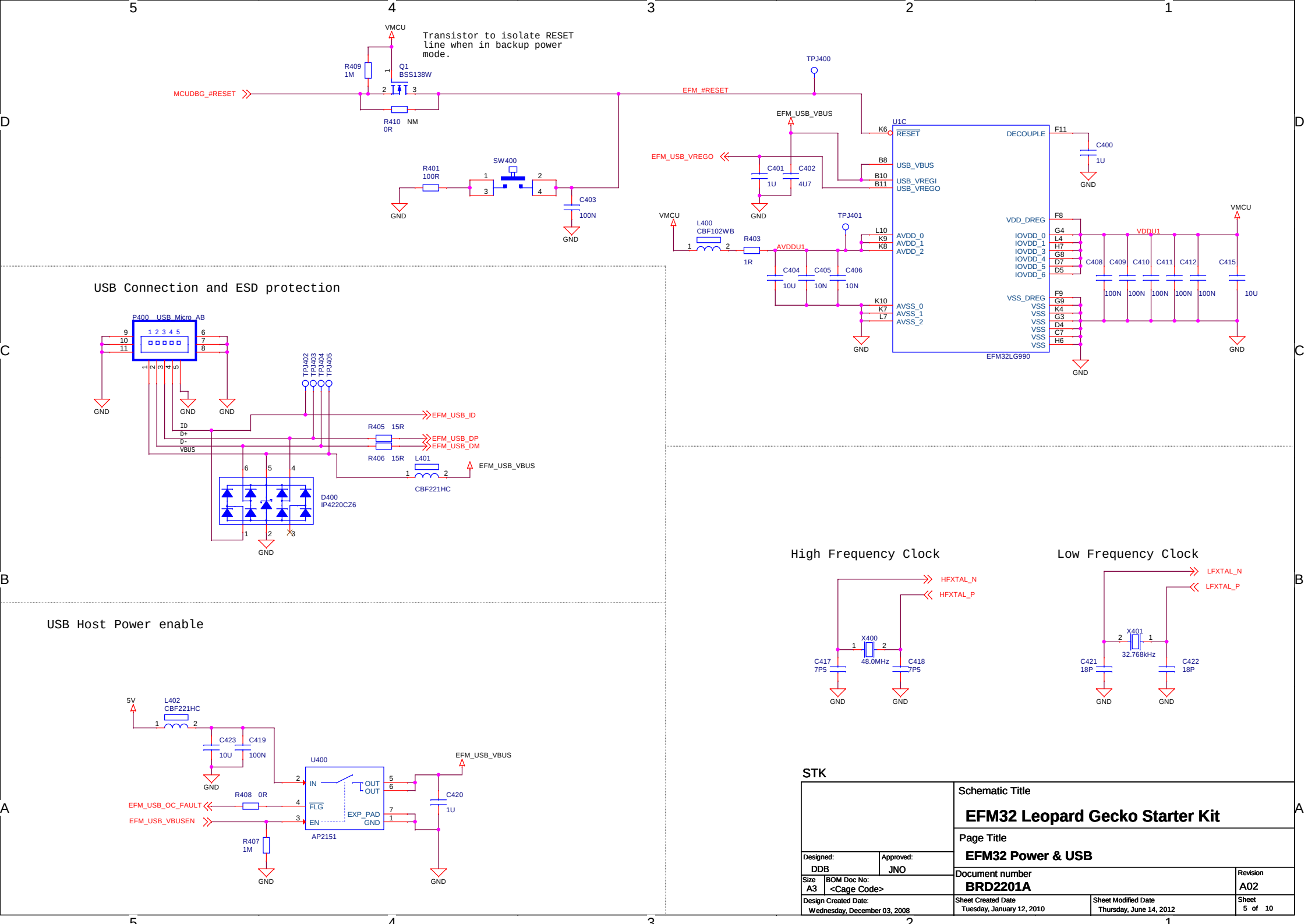
NAND Power

The diagram illustrates the power supply for a NAND gate (U101, TSSA3166). The gate's COM pin (2) is connected to VMCU. The IN pin (4) is connected to NAND_PWR_EN. The V+ pin (5) is connected to a 1MΩ resistor (R106) and a 100nF capacitor (C106), which are both connected to VMCU. The NO pin (1) is connected to VMCU_NAND. The GND pin (3) is connected to the common ground. The output of the gate is shown as a pulse.

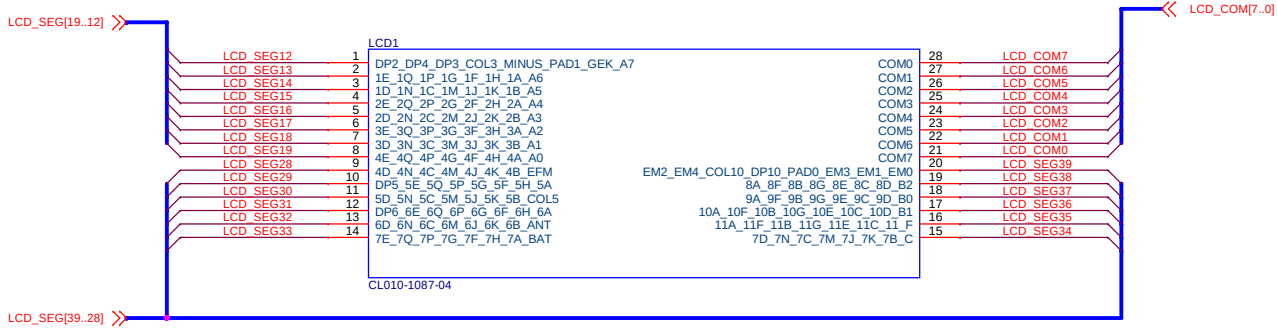


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		Page Title User Interfaces	
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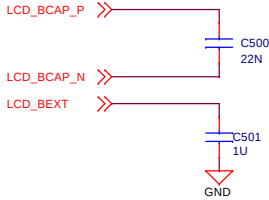
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Size A3	BOM Doc No:	Revision	
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LCD signal connections



LCD Boost

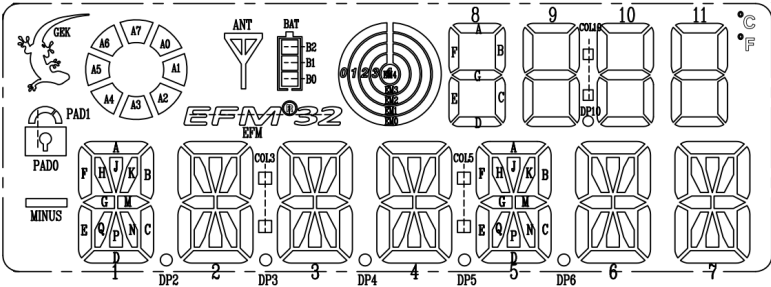


Segment names

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14
---	S0	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13
COM0	DP2	1 E	1 D	2 E	2 D	3 E	3 D	4 E	4 D	DP5	5 D	DP6	6 D	7 E
COM1	DP4	1 Q	1 N	2 Q	2 N	3 Q	3 N	4 Q	4 N	5 E	5 N	6 E	6 N	7 Q
COM2	DP3	1 P	1 C	2 P	2 C	3 P	3 C	4 P	4 C	5 Q	5 C	6 Q	6 C	7 P
COM3	COL3	1 G	1 M	2 G	2 M	3 G	3 M	4 G	4 M	5 P	5 M	6 P	6 M	7 G
COM4	MINUS	1 F	1 J	2 F	2 J	3 F	3 J	4 F	4 J	5 G	5 J	6 G	6 J	7 F
COM5	PAD1	1 H	1 K	2 H	2 K	3 H	3 K	4 H	4 K	5 F	5 K	6 F	6 K	7 H
COM6	GEK	1 A	1 B	2 A	2 B	3 A	3 B	4 A	4 B	5 H	5 B	6 H	6 B	7 A
COM7	A7	A6	A5	A4	A3	A2	A1	A0	EFM	5 A	COL5	6 A	ANT	BAT

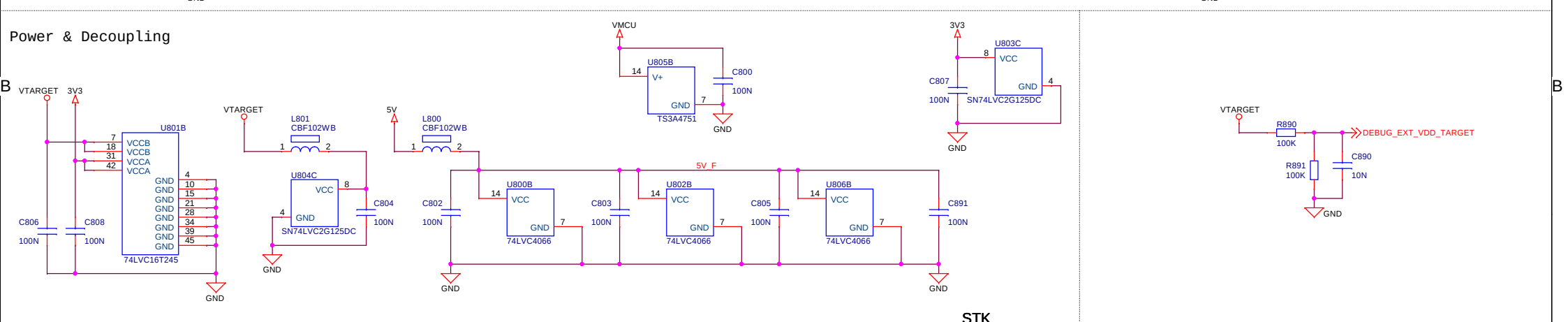
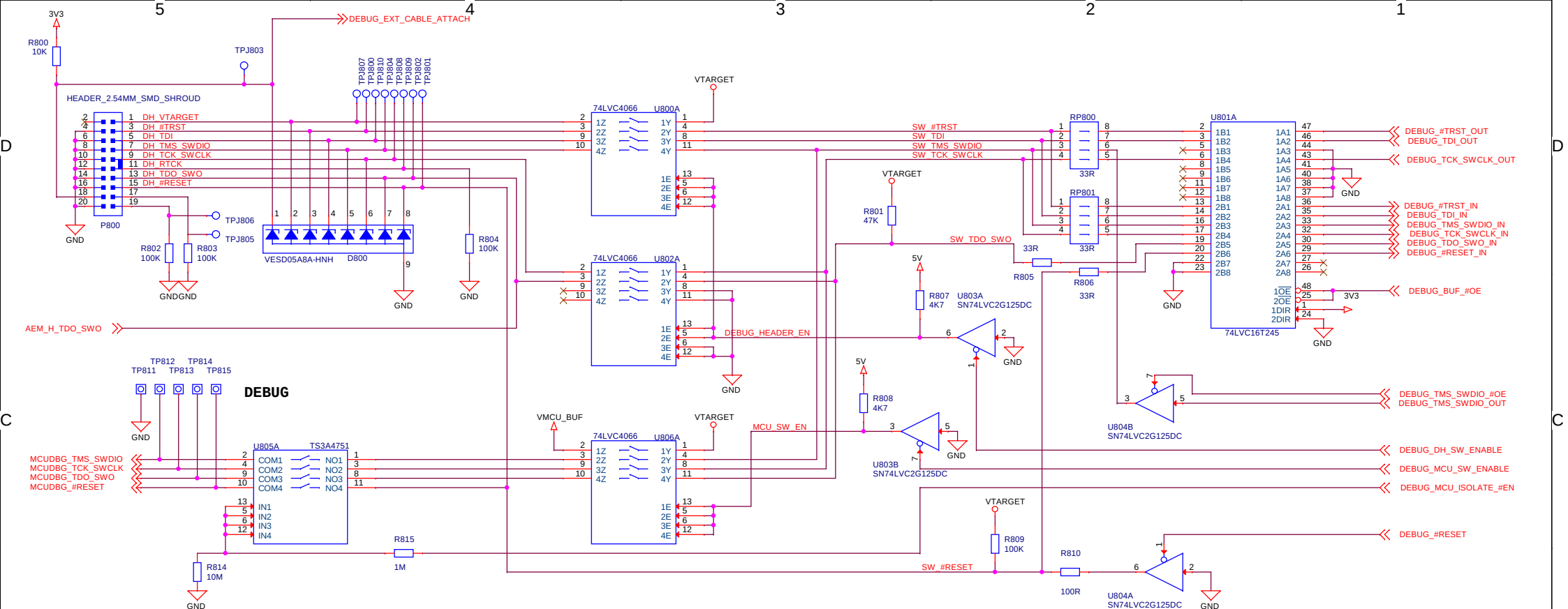
PIN	15	16	17	18	19	20	21	22	23	24	25	26	27	28
---	S14	S15	S16	S17	S18	S19	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
COM0	7 D	11 A	10 A	9 A	8 A	EM2								COM0
COM1	7 N	11 F	10 F	9 F	8 F	EM4							COM1	
COM2	7 C	11 B	10 B	9 B	8 B	COL10						COM2		
COM3	7 M	11 G	10 G	9 G	8 G	DP10					COM3			
COM4	7 J	11 E	10 E	9 E	8 E	PAD0				COM4				
COM5	7 K	11 C	10 C	9 C	8 C	EM3		COM5						
COM6	7 B	11 D	10 D	9 D	8 D	EM1		COM6						
COM7	°C	°F	B1	B0	B2	EM0	COM7							

Segment placement



STK

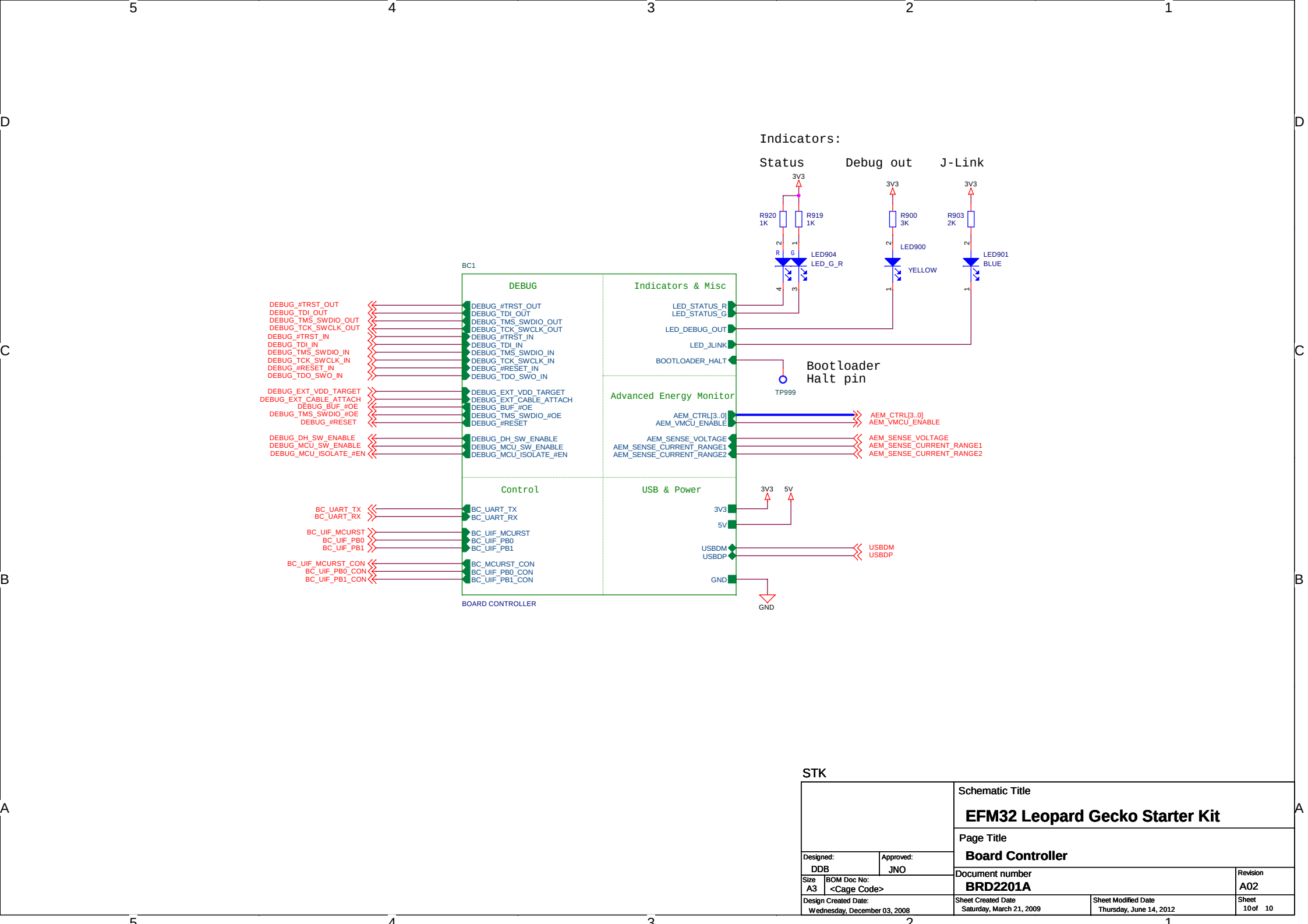
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		Revision	
		A02	
Designed: DDB		Approved: JNO	
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Design Created Date: Wednesday, December 03, 2008		Sheet Created Date: Tuesday, January 12, 2010	
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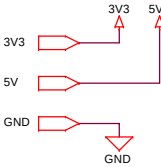
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							Page Title		
							Debug Interface		
							Document number		
							BRD2201A		
							Revision		
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Mode	DEBUG_MCU_SW_ENABLE	DEBUG_DH_SW_ENABLE	DEBUG_BUF_#OE	ISOLATE_#EN	DH_VTARGET	VTARGET
Debug Out	0	1	0	0	External voltage	External voltage
MCU Debug	1	0	0	1	Disconnected	VCPU
Debug In	1	1	1	1	VCPU	VCPU
Debug Off	1	1	1	0	-	-

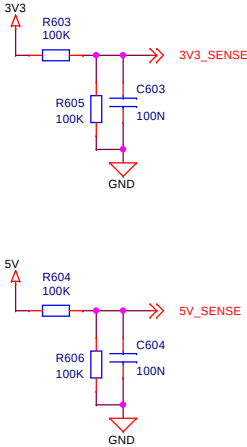
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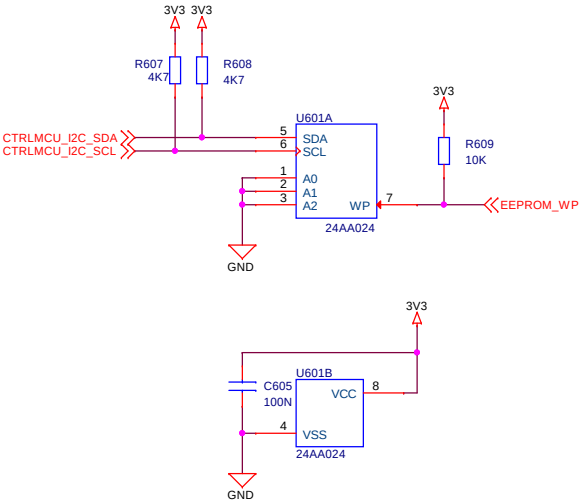
POWER INPUTS



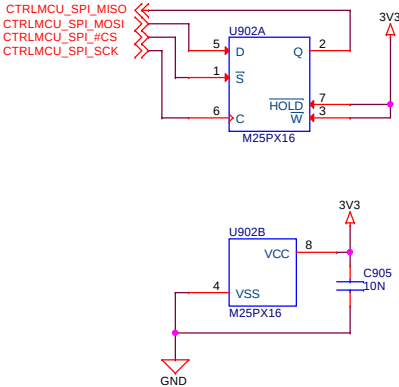
POWER SENSE



CTRLMCU EEPROM



CTRLMCU SERIAL FLASH



<Schematic Path>
BOARD CONTROLLER

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		EFM32 Starter Kit Board Controller	
		Page Title	
		Board Controller Misc	
Designed: DDB	Approved: JNO	Document number	
Size A3	BOM Doc No: <Cage Code>	BRD2200A	
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		Sheet 12 of 12	Revision A03