Si3050 Global Voice DAA

Frequently Asked Questions

Si3050 FAQ

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Other FAQs

Layout

Q: How can Silabs help generate a schematic and layout for my design?

A: We recommend copying the EVB schematic and layout. Figures 10-13, 18-20 of the Si3050 EVB datasheet show an example schematic and layout and AN67 lists layout recommendations and layout checklist on pages 13 and 14. A Silicon Labs FAE can provide schematic and layout files in .pdf, gerber, etc., format.

Silicon Labs will review customer schematic and layout files before boards are built.

Q: Are there any special layout/component considerations for a relay used in front of the Si3050?

A: A relay in front of the Si3050 should be rated for 1500 V minimum. 2500 V is preferable.

Distance between FXO tip/ring traces and any signal referenced to GND must be as wide or wider than the relay pin spacing . Also, spacing between FXO tip/ring traces and traces from the RJ-11 side of the relay needs to be as wide or wider than the relay pin spacing.

Bill of Materials

Q: How can I locate 2nd source vendors for devices in the Si3050 BOM?

A: Ask your sales representative or FAE for a copy of the "Si3050 BOM with supplier part numbers" file.

Q: What are Y-class capacitors?

A: Y-class capacitors are high voltage capacitors, regulated by EN132400. A Y3-class capacitor can withstand a 3KV lightning surge, a Y2-class capacitor 5KV, and a Y1-class capacitor 8KV. Y-class capacitors provide EMI filtering and an AC path to ground in the Si3050 circuit. Y-class capacitors are necessary because telephone lines are exposed to high voltage transients.

Y2 capacitors (and associated 5 kV isolation layout per AN67) are recommended for Si3050 designs.

See: https://www.mysilabs.com/public/documents/tpub_doc/wpaper/Wireline/Silicon_DAA/en/Si305x_Surge.pdf

Q: Why do you recommend Y2-class capacitors if EN55022 and UL1950 specs only require testing to 1500V?

A: Silicon Labs' field experience has shown that Y2-class capacitors (5kV isolation) provide more effective protection from lightning surge and a lower incidence of field returns than capacitors with lower voltage ratings, such as Y3. Utilization of surge protection below 5 kV may reduce equipment costs, but at the expense of a potentially higher field return rate.

Q: Can a ceramic capacitor be used for C4?

A: A ceramic capacitor can be used for C4. An exectrolytic/tantalum capacitor is specified in the Si3050 BOM because the BOM also applies to modem products (Si24xx, Si3052, Si3056), where an on-board speaker can cause vibrational damage to the capacitor.

Circuit Protection

Q: Why doesn't the Si3019 require sidactors limiting Tip/GND and Ring/GND voltage, but the Si32xx ProSLIC lineside devices do?

A: The Si32xx ProSLIC lineside devices are ground referenced. They have a positive breakdown relative to ground that is different than the negative (since the negative voltages are where a SLIC is designed to operate). Sidactors/thyristors are necessary to keep peak positive surges from damaging the Si32xx lineside devices. The Si3019 doesn't have a ground reference. It is isolated from ground through the isolation barrier.

Q: Do I need a fuse on Tip or Ring as shown in the Si3050 datasheet appendix?

A: If the Si3050 circuit is in a fire enclosure (metal enclosure), the fuse may not be required to pass UL1950. Consult with your testing agency to determine if the fuse is required.

Q: Why does the Si32xx use 2 fuses/current limiters, but the Si3050 only uses one?

A: A single fuse is used for metallic protection with the Si3050. When the sidactor clamps, excess current flows tip to ring. The isolation caps provide longitudinal protection, so no DC current will flow to ground. The only current that flows to ground is the instantaneous current through the caps, which is limited by the size of the caps.

On the Si32xx, there are metallic and longitudinal sidactors/thyristors. Two fuses are required because surge current can flow from tip to ground without passing through the ring lead, and from ring to ground without passing through the tip lead.

Software

Q: How do I program the Si3050 for different countries?

A: Table 13 on pages 21–23 of the Si3050 Data Sheet lists register settings for different countries.

Q: What is the recommended Si3050 SW initialization for a voice application?

A: The "Initialization" section on page 24 of the Si3050 datasheet lists initialization commands.

Q: How do I clear an Si3050 interrupt?

A: Writing a zero to any bit in Reg. 4 clears the corresponding interrupt, while writing a one to any bit in Reg. 4 has no effect on the bit.

For example, writing 0x7F = 01111111 to Reg. 4 will clear the Ring Detect Interrupt RDTI, but will not affect other bits in the register.

Troubleshooting

Q: How do I trouble-shoot my Si3050 design?

A: Appendix B of AN93, "Prototype Bring-Up Guide (Si3018/Si3010)" provides trouble-shooting techniques. Diagrams are provided showing how the Si3050 board can be cross-wired with the Si3050 EVB. Also, tables list typical Si3019/18 pin voltages and impedances to GND, as well as resistance across components and voltage across components.

Q: Why can't I read/write SPI commands to the Si3050?

A: In addition checking SPI signal levels and timing, PCLK and FSYNC should be checked. PCLK and FSYNC are used to generate internal Si3050 clocking. The SPI interface will operate only if PCLK and FSYNC meet timing, signal level, and jitter specifications in the Si30050 data sheet. Also, PCLK and FSYNC must be valid upon the rising edge of /RESET.

Q: Why can I communicate with the Si3050, but not the Si3019?

A: Before communicating with the Si3019, the PDL bit in register 6 must be cleared. Run initialization sequence on page 24 of Si3050 datasheet (shown in AN77) before reading/writing Si3019 registers.

If Si3019 registers cannot be accessed after running the initialization sequence, check the ISOcap link between the Si3050 and the Si3019. Appendix B of AN93, "Prototype Bring-Up Guide (Si3018/Si3010)" provides trouble-shooting techniques.

Q: How do I remove dc offset in Si3050 PCM data transmission?

A: Write a '1' to bit 1 of register 31 to enable the 200 Hz filter.

Q: Can you provide suggestions to help my Si3050 circuit pass EMI emissions tests?

A: See AN81.

Q: Why does the Si3050 provide a 1.8 dB loss in the Tip/Ring to PCM direction, when gain registers are set to 0 dB?

A: The Si3050+Si3019 A/D has an intentionally designed loss of approximately 1.8 dB. Gain settings can be adjusted using registers 38–41. If a net loss of 0dB is required, the 1.8 dB loss in the A/D direction can be cancelled out by setting the programmable gain to +1.8 dB using registers 39 and 41.

Q: How do I adjust the digital hybrid to improve 4-wire return loss?

A: For most applications, the default hybrid settings do not need to be modified. Because the impedance presented to the Si3050 will differ on alternate lines, it is generally best to use the default hybrid setting.

In cases where the impedance synthesized by the Si3050 differs from the impedance presented to the SLIC by the line, the digital hybrid can be used to balance the hybrid. The Digital Hybrid Calculator (available at www.silabs.com) determines the optimal hybrid coefficients for a given line model.

Since it is not practical to create the ideal hybrid coefficient for every line, a coefficient look-up table can be created using the Digital Hybrid Calculator. The system software should cycle through each set of coefficients to determine which provide the best return loss. In most applications, the default hybrid settings can be used as-is, and this process does not need to be performed.

Other FAQs

Q: How can I determine the device revision of the Si3050/Si3019?

A: The device revision is the 5th character on the 2nd line of device marking on the package. Also, registers 11 and 13 contain the device revision.

Q: How fast can I run the SPI bus with daisy-chained devices?

A: The minimum low time of SCLK is given by,

Tlomin = td4*(N-1) + tsu2

and the minimum clock high time is given by,

Thimin = th2

However, the clock frequency upper limit is dictated by the low time since it is longer. Assuming a 50% duty cycle clock, the maximum clock frequency is:

fSCLK = 0.5/(tlomin) = 0.5/(10nS*7 + 25nS) = 5.26 MHz for 8 devices

Assuming a 40/60 duty cyle, the equation is:

fSCLK = 0.4/(tlomin) = 4.21 MHz for 8 devices

If the application can control the clock high time and provide a longer clock high %, the upper limit can be increased to,

fSCLK = 1/(tlomin + thimin) = 8.69 MHz for 8 devices

Q: Can I dither 2 clocks (e.g., 2.056MHz and 2.040MHz) to produce PCLK for the Si3050?

A: No, 2 clocks cannot be dithered to produce PCLK. Dithering 2 clocks may cause issues passing data across the ISOcap interface.

Q: Should I use the IIR or FIR filter?

A: For voice applications, IIRE, bit 4 of register 16, should be set to 1 to enable the IIR filter. When the IIR filter is used, the group delay is shortened. If the FIR filter is used, there is more group delay, but the delay is more centered, which is preferred for modem/data applications.

Q: Is there a case where the DC impedance should be set to 800 ohms?

A: No. The DC termination (DCR bit in reg. 26) should be set to 0 (50 ohms). The 800 ohm termination should be used only in an overload condition when automatically modified as described in the "Overload Detection" section of the Si3050 data sheet.

Q: Are the Si3050 pins high impedance when held in reset?

A: The Si3050 pins are high impedance when held in reset.

Q: Where can I get information about Si3050 compliance?

A: Ask your sales representative or Silabs FAE for Si3018 country compliance reports.

Q: What is a recommended Si3050 test circuit when connecting to a PCM-4 or other tester?

A: See AN187.

NOTES:

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