



SILICON LABS

Si321x SINGLE-CHANNEL PROSLIC
FREQUENTLY ASKED QUESTIONS



Si321x SINGLE-CHANNEL PROSLIC—FREQUENTLY ASKED QUESTIONS

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Design and Layout

Q: How can you help me with generating a schematic and layout for my design?

A: The Si321x EVB data sheet includes example schematics and layout and AN34 includes layout recommendations (localize ground trace connections for C25, C14, C9, and L1 with a single connection point to the main ground plane is important—L1 and C9 GND connection should be short and low impedance). In addition, the Silicon Labs FAE can provide individual files in .pdf, gerber, etc., format. We recommend copying the EVB schematic and layout if possible.

Some dc-dc converter register component values are listed on pages 23, 24 of the rev. 1.43 Si3210 data sheet (page 22 of the rev. 0.92 Si3215 data sheet). If these are not appropriate, the dc-dc converter spreadsheet (posted under Si321x documentation at www.silabs.com) can be used to calculate register and component values.

Silicon Labs will review your schematic and layout files before you build boards.

Q: What can Silicon Labs provide to help with SW?

A: "Demo and Development Source Code" is posted under Si321x documentation at www.silabs.com. Customers should use/copy this code.

Q: Are there any layout considerations for the Si3201?

A: Orientation of the Si3201 should be identical to the Si321x EVB. Also, capacitors C5, C6 should be placed close to the Si3201. If not, Idle Channel Noise may be increased due to coupling into the Si321x.

Q: How do I connect to the large GND pads on the bottom of the Si321x QFN and Si3201 packages?

A: The Si3201 and Si321x QFN pads should be connected to the GND plane. This is done directly if the GND plane is on the top of the board, as shown in the layout in the Si321x EVB user's guide, or through several vias if the GND plane is on another layer.

SPI Interface

Q: What do I do if I can't read/write SPI commands to the Si321x?

A: PCLK, FSYNC are used to generate internal Si321x clocking. PCLK and FSYNC must meet timing in the Si321x data sheet. Also, excessive jitter should not be present on PCLK, FSYNC.

PCLK and FSYNC should be valid upon the rising edge of /RESET

Q: Does the SPIDC bit only need to be set in the first Si321x or all Si321x devices in an SPI daisy-chain?

A: The SPIDC bit only needs to be set in the first Si321x. At power-up, the Si321x is in 2-byte SPI mode (see the data sheet SPI description). In 2-byte mode, there is no Channel ID byte (it exists only in 3-byte SPI mode). Any writes done while in 2-byte SPI mode will be carried out on all members of the SPI chain. The SPI 2-byte write serial data will go into the first Si321x' SDI pin, then come out on the SDITHRU pin to the SDI pin of the next Si321x, etc. All daisy-chain members will be written with the same data to the same register. This sets all Si321x devices in daisy-chain mode. After the 2-byte write to make SPIDC = 1, all subsequent transactions must be 3-byte transactions, because all devices are in daisy chain mode and expect 3-byte SPI transactions, which contain the Channel ID extra byte, indicating for which device the read or write transaction is intended.

While in 2-byte mode, if a read is performed using a 2-byte transaction to a daisy-chain, all daisy-chain members will respond colliding with each other on the SDO bus. Therefore, in an SPI daisy-chain with the Si321x, the host must first write SPIDC = 1 before doing any read operations. The subsequent reads must be 3-byte SPI transactions.

Incorrect Voltage on Tip/Ring

Q: What do I do if when I place the Si321x in the active (direct reg 64 = 0x11) or ringing (direct reg 64 = 0x44) state, I read no voltage on tip and ring? Direct register 64 doesn't switch to 0x00 (remains in the active (direct reg 64 = 0x11) or ringing (direct reg 64 = 0x44) state).

A: Check whether fuse F1 is blown. If it is, check whether current flowing through F1 is too high.

Q: What do I do if when I place the Si321x in the active (direct reg 64 = 0x11) or ringing (direct reg 64 = 0x44) state, I read no voltage on tip and ring and it immediately switches to the Open state (direct reg 64 = 0x0X)?

A: Check direct registers 19 for Q1-Q6 power alarm interrupts pending. If a power alarm interrupt is pending, the power alarm placed the Si321x in the Open state.

The power alarm may be caused by the following:

1. Not running manual calibration routine (see page 3 of AN35) on a design which uses the Si3201 (discrete front-end will not cause a power alarm when manual cal is not run).
2. Improper dc-dc converter component/register settings.

To correct:

- a. Run Silicon Labs "demo2_2.zip" (or latest version) SW on the design,
- b. Adjust dc-dc converter register settings to match dc-dc converter spreadsheet or data sheet/EVB values, and
- c. Check that dc-dc converter components match the values in the dc-dc converter spreadsheet or data sheet/EVB and match the orientation of the schematic.

Q: What do I do if the dc-dc converter won't generate expected voltages on my Si321x design (not Si321x EVB).

To correct:

- a. Run Silicon Labs "demo2_2.zip" (or latest version) SW on the design,
- b. Adjust dc-dc converter register settings to match dc-dc converter spreadsheet or data sheet/EVB values, and
- c. Check that dc-dc converter components match the values in the dc-dc converter spreadsheet or data sheet/EVB and match the orientation of the schematic.

Manual Calibration

Q: Do I always need to run manual calibration after resetting the Si321x?

A: For designs using the Si3201, manual calibration must be run every time the Si321x is reset. For designs with a discrete front-end (no Si3201), manual calibration is recommended but not required.

Q: How can I shorten the time required for manual calibration?

A: To minimize the time required for manual calibration, you only need to determine the direct register 98 and 99 values the first time the Si321x is reset. You can load the same calculated values on subsequent resets.

Circuit Protection

Q: What protection circuit(s) should I use with the Si321x?

A: Example protection is shown on page 5 of the rev. 1.1 Si321x EVB data sheet. Please work with a protection component vendor to determine appropriate protection for a given application.

Q: Why does the Si321x require sidactors limiting Tip/GND and Ring/GND voltage, but the Si3050 doesn't?

A: The SLIC circuits have a ground reference. They have a positive breakdown relative to ground that is different than the negative (since the negative voltages is where a SLIC is designed to operate). The protection is necessary to keep peak positive going surges from damaging the Si321x.

The Si3050 is isolated from ground through the isolation barrier.

Si321x EVB

Q: What do I do if I read no voltage on tip and ring when I place the Si321x EVB in the active (direct reg 64 = 0x11) or ringing (direct reg 64 = 0x44) state? Direct register 64 doesn't switch to 0x00 (remains in the active (direct reg 64 = 0x11) or ringing (direct reg 64 = 0x44) state).

A: Check whether fuse F1 is blown. If it is, check whether current flowing through F1 is too high.

Q: What do I do if the Si321x EVB is outputting incorrect voltages in the active (direct reg 64 = 0x11) and ringing (direct reg 64 = 0x44) states?

A: Check to make sure +5 V is applied to the V_{DC} input of the Si321XM EVB and +12 V is applied to the V_{DC} input of the Si321x EVB.

Q: How do I determine which Si321x EVB to use and which devices to use in my design?

A: The EVB options are listed on page 123 of the Si3210 data sheet. The decisions to be made are: 1) Si3210 or Si3215 2) Si321x or Si321XM and 3) discrete or Si3201 front-end solution.

1. The Si3215 QFN is significantly lower cost than the Si3210 but does not perform DTMF detection. DTMF detection needs to be performed behind the Si3215 in a DSP/ASIC/FPGA. If DTMF detection can be performed behind the Si321x, the Si3215 QFN should be used; If not, the Si3210 should be used. A QFN package is a good choice for either the Si3210 or Si3215 because it is smaller; therefore, the example layout provides lower idle channel noise, and Si3210 the QFN is footprint compatible with the Si3215 for future cost reductions.
2. The Si321x BOM cost is lower that of the Si321XM. Determination of requirement to use the Si321XM is dictated by V_{DC} voltage and # of REN required. V_{DC} options are shown on pages 18, 19 of rev. 1.43 of the Si3210 data sheet. If 12 V or higher V_{DC} is provided, the Si321x should be used with BJT/inductor dc-dc converter. If 5 V V_{DC} is provided and requirement is to ring 3 REN or less, the Si321x should also be used with BJT/inductor dc-dc converter. If 5 V is used for V_{DC} and 5 REN is required, the Si321XM with XFMR/MOSFET dc-dc converter should be used. Likewise, if V_{DC} is 3.3 V, the Si321XM with XFMR/MOSFET dc-dc converter should be used. In addition to pages 18,19 of the Si3210 data sheet, the dc-dc converter spreadsheet can be used to determine whether M or non-M Si321x should be used.
3. The discrete front-end shown on page 21 of the data sheet is the lowest cost front-end solution. The Si3201 solution, shown on page 17 of the data sheet is higher cost but uses less board space.

Si321x FAQ

Other FAQs

Q: What do I do if the DTMF tone register settings generated from equations on page 35 of the rev. 1.43 Si3210 (page 33 of rev. 0.92 Si3215) data sheet are not producing correct DTMF tones?

A: Use radians and not degrees with the equations.

A simple method of determining DTMF tone register settings is to select the "tone generator" tab in the ProSLIC GUI. Simply enter frequency and amplitude, and it will provide register settings.

Q: How do I lower current dissipation of the Si321x?

1. Reduce the overhead voltage. Setting the VMIND (IR 41 to 0x0200h or 0x0400h) to 1 or 2 instead of 6 will reduce the required V_{BAT} and drop the current from the V_{IN} supply from ~50 mA on hook (with 5 V V_{IN}) to ~40 mA onhook. The offhook current drops to ~105 mA.
2. Reduce the bias current for the transistors. Our typical recommendation is to go with 8 mA. Reduction to 4 mA (setting ETBA = 00), the current overhead drops another ~15 mA.
3. The loop current can be lowered to 20 mA if you set ILIM to 0 and which will drop the current overhead to ~80 mA.
4. If using the Si3201, you should have good thermal relief (i.e., via connections to the GND pad) under the Si3201.
5. Run off non-regulated voltage (e.g., 12 V instead of regulated 5 V).

Q: How do I lower Idle Channel Noise of the Si321x?

1. Capacitors C15, C16, C17, C30, C31 and inductor L2 should be included in the design and placed close to the VDDA1, VDDA2, VDDD pins as in the Si321x EVB layout.
2. High-speed digital traces should not be routed near/parallel to Si321x analog traces, in particular traces connected to pins 15, 16, 20, 21.
3. If using the Si3201, place capacitors C5, C6 close to Si3201 pins 1, 3.

Q: What do I do if I hear a clicking noise when a caller is talking loudly into the Si321x?

A: Set bit 4 of DR67 to 0, which disables "speed-up". If the noise goes away, speed-up (increasing the speed of dc voltage transitions on tip/ring) is the cause of the clicking.

Speed-up is necessary to meet the transition time of Japanese pulse dialing. If turning off speed-up eliminates the clicking, but Japanese pulse dialing needs to be supported, contact a Silicon Labs FAE.

Q: What do I do if digital loopback (Reg 8 DLM is set) doesn't generate the same bit pattern as is sent to the Si321x?

A: The digital loopback path goes through the interpolation and decimation filters, which slightly attenuate the signal amplitude. When digital loopback is performed, we recommend feeding a digital sine wave bitstream and capture the returning bit stream. Look at the frequency and amplitude. The frequency will be identical, with a slight phase shift. The amplitude will be slightly attenuated.

Q: What do I do if, when converting a design from the Si3210 to the Si3215, I see issues with the Si3215 that I didn't see with the Si3210?

A: Use "demoV2.2" code posted under Si3210 documentation at www.silabs.com. This code supports the Si3210 and Si3215.

AN229 describes register differences between the Si3210 and Si3215. Bit 7 of register 1 can be used to differentiate the Si3210 and Si3215 - it contains a '1' in the Si3215 and a '0' in the Si3210.

Indirect Register Mapping translation from Si3210 to Si3215:

<u>Si3210</u>	<u>Si3215</u>	<u>Offset</u>	
0–12	—	—	(see Note 1)
13–40	0–27	–13	(see Note 2)
41–43	64–66	+23	
88–98	75–85	–13	
99–104	69–74	–30	
193–195	208–210	+15	
197	211	+14	

Notes:

1. Locations 0–12 in the Si3210 have to do with the DTMF decoder, which does not exist in the Si3215. Therefore, these locations are not defined anywhere in the Si3215 indirect register map.
2. Locations 23–25 in the Si3210 have to do with pulse metering, which is also not available in the Si3215, and therefore, these locations do not exist in the Si3215, but are part of the Si3210:13–40 → Si3215:0–27 mapping to simplify the mapping. It is assumed that the product software will not be reading/writing locations Si3210:23–25 → Si3215:10–12.
3. Indirect register addresses not included in the above translation table should never be read or written by software. Some of these excluded addresses could have undesirable and unpredictable side effects if unintentionally written. For these reasons, these addresses have been intentionally excluded from the product documentation and from the translation table provided above.
4. The above translation table includes all of the addresses referenced in AN35 Rev. 0.6, page 3, step 20 of the "ProSLIC Initialization" procedure.

Q: Does the Si321x support GR-909 testing?

A: Yes, contact your local Silicon Labs FAE for example GR-909 code.

Q: How do I determine the current rating of the F1 fuse?

A: The fuse current rating should be 125 to 140% of the Si3210 average current (the average current is listed as "Idc Avr" in the dc-dc converter spreadsheet). The fuse should be fast acting.

Q: What is the V_{DC} power required to drive the dc-dc converter?

A: V_{DC} should be capable of providing 5–10% more power than "Pout" listed in the dc-dc converter spreadsheet.

Q: How can I determine the device revision of the Si321x?

A: The device revision is the 5th character on the 2nd line of device marking on the package. Also, it is contained in the bottom 4 bits of register 0.

Si321x FAQ

Q: My design requires low power consumption and heat dissipation. What can I do to reduce Si321x power dissipation?

1. Reduce the overhead voltage. Setting the VMIND (IR 41) to 1 or 2 instead of 6 will reduce the required V_{BAT} .
2. Set IR41 to 0x400h. That drops the current from the 5 V supply from ~50 mA on hook to ~40 mA onhook. The offhook current drops to ~105 mA.
3. Reduce the bias current for the transistors. Our typical recommendation is to go with 8 mA. Reducing it to 4 mA (setting ETBA = 00), the current overhead drops another ~15 mA.
4. Lower the loop current to 20 mA by setting ILIM to 0.
5. If Si3201 is used, good thermal relief should be provided via connections to the GND pad under the Si3201.

Q: How do I locate vendors for devices in the Si321x BOM?

A: Ask your sales representative or FAE for a copy of the Si321x Recommended Suppliers file.

Q: The Si3215 is being used to provide a phone connection to a home security system. How do I program the Si3215 to always provide voltage to the security system?

A: Bit 3 of register 14 should be set to one, "PLL Free Run enabled". This ensures that the Si3215 will provide voltage even if PCLK is not being supplied to the Si3215. Note that PCLK cannot float when in this mode. It must be held high, low, or toggled at an arbitrary frequency. The default state for bit 3 of register 14 is zero, which implies normal operation (non PLL free-run).

Notes:

Si321x FAQ

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