



Timing Solutions for Altera

Overview

Silicon Labs timing portfolio includes a wide selection of frequency flexible, low jitter XO/VCXOs, clock generators, jitter attenuating clocks, and clock buffers targeting communications, computing, embedded, broadcast video, and consumer electronics applications.

The following are Silicon Labs' recommended timing products for Altera product families. Turnkey reference designs are also summarized below.

Si5xx XO/VCXOs

- Any frequency from 100 kHz to 1.4 GHz
- Single, dual, quad, I2C programmable frequency
- Ultra-low jitter: 0.3 ps rms
- 2 week lead time for production samples
- +/-20, 50, 100 ppm stability
- Industry-standard 3.2x5mm and 5x7mm pinouts
- LVPECL, LVDS, CMOS, CML, HCSL
- 1.8, 2.5, 3.3 V
- Request custom oscillator:
www.silabs.com/VCXOpartnumber

Si533x/5x Clock Generators

- Generates any combination of up to 8 frequencies (0 ppm error)
- Wide output frequency range: 8 kHz to 710 MHz
- Low jitter: <1 ps rms
- Selectable format per output (LVPECL, LVDS, CMOS, HCSL, CML, SSTL, HSTL)
- Independent VDDO per output (1.8, 2.5, 3.3 V)
- PCI Express Gen 1/2/3, PON, GbE jitter compliant
- Request custom clock:
www.silabs.com/ClockBuilder

Si531x/2x/6x/7x Jitter Attenuating Clocks

- Generate any frequency from 2kHz to 1.4GHz from 2kHz to 710MHz input
- Low jitter: 0.3 ps rms phase jitter
- Jitter cleaning w/integrated adjustable loop filter (>4 Hz), internal VCXO
- Ideal for Carrier Ethernet, OTN, wireless backhaul, PON, 1/10/40/100G Ethernet, broadcast video

Recommended Solutions

Altera Product Family	Silicon Labs Products	Applications
Stratix V Stratix IV	<ul style="list-style-type: none"> • Si510/Si530 XO • Si515/Si550 VCXO • Si570 I2C programmable XO • Si571 I2C programmable VCXO • Si5338 differential clock generator • Si5326 any-rate jitter attenuating clock • SL28PCIe25 PCIe clock 	<ul style="list-style-type: none"> • 1/10/40/100G Ethernet • Fibre Channel • GPON • OTN • PCI Express Gen 1/2/3 • Serial Rapid IO • CPRI • 3G SDI, HD SDI
Cyclone IV	<ul style="list-style-type: none"> • Si510 XO • Si5338 differential clock generator • Si5351 CMOS clock generator 	<ul style="list-style-type: none"> • DisplayPort • Serial Rapid IO • Gigabit Ethernet • 3G SDI, HD SDI • General-purpose

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Featured Reference Design

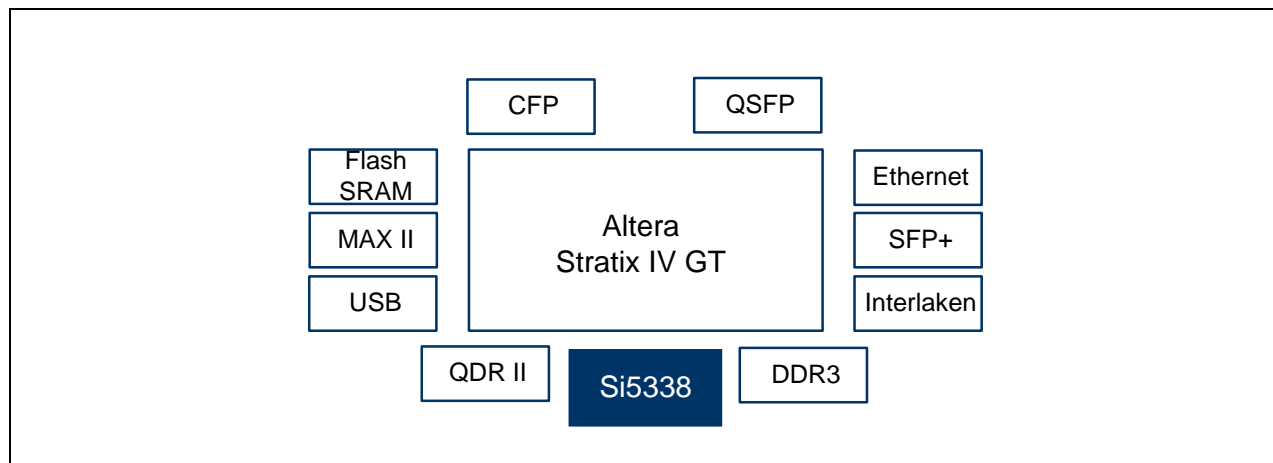


Figure 1. Altera Stratix IV GT 100G FPGA Development Kit

Altera Reference Designs with Silicon Labs Timing Solutions

Silicon Labs Part Number	Altera Reference Design	Details
Si570	Stratix IV GX Dev Kit	http://www.altera.com/literature/ug/ug_sivgx_fpga_dev_kit.pdf
Si570	Stratix IV E Development Kit	http://www.altera.com/literature/ug/ug_sive_fpga_dev_kit.pdf
Si570	Stratix IV GT Signal Integrity Dev Kit	http://www.altera.com/literature/manual/rm_sivgt_si_dev_board.pdf
Si5338	Stratix IV GT 100G Dev Kit	http://www.altera.com/products/devkits/altera/kit-stratix-iv-gt-si.html

Resources

- Product data sheets, applications notes, whitepapers: www.silabs.com/Timing
- Timing product selector guide: www.silabs.com/Marcom_Documents/Resources/Timing_Selector_Guide.pdf
- Generate a custom clock: www.silabs.com/ClockBuilder
- Generate a custom XO/VCXO part number: www.silabs.com/VCXOPartnumber
- Generate a custom silicon oscillator part number: www.silabs.com/SiXOPartnumber

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