Proven 8051 Microcontroller Technology, Brilliantly Updated

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Introduction

The proven 8051 core received a welcome second wind when its architecture lost patent protection in 1998. A plethora of new 8051 MCUs entered the market at that time, some subscribing to the original architecture and others modifying it to varying degrees.

The Silicon Labs 8051 architecture is of the second variety. It maintains code compatibility with the original core while modernizing and "RISC-ifying" the architecture, resulting in a massive performance boost. This is a tradition that's never been more obvious than in the Silicon Labs EFM8™ 8-bit MCU family.

Speeding Execution with a Pipelined Architecture and MAC

The original Intel 8051 core took 12 cycles to execute 1 instruction; thus, at 12 MHz, it ran at 1million instructions per second (1 MIP). In contrast, a 100 MHz Silicon Labs 8051 core will run at 100 MIPS or 100 times faster than the classic 8051 at a frequency that is only about 8x the classic 8051's frequency.

Silicon Labs implemented its version of the 8051 core as a 3-stage pipe Von-Neuman machine. The simplicity of this 3-stage pipe combined with the straightforward instruction decode logic of an 8-bit machine enables this device to run at 100 MHz in a 0.35-micron process. The 32 Byte register file with four regions for ease of context switching was preserved since code compatibility with the classic 8051 was of utmost importance. **Figure 1** shows a classical three-stage pipeline structure as implemented on the Silicon Labs 8051 core.

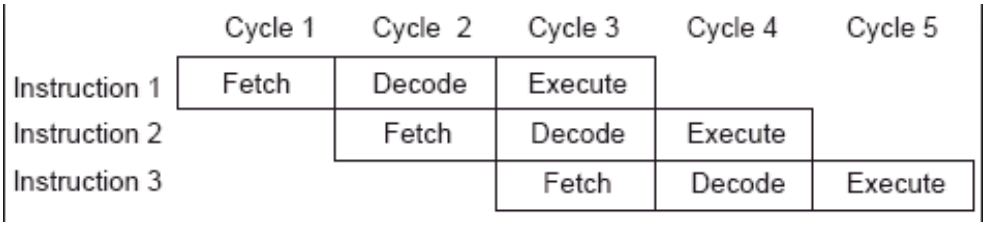

Figure 1. Example of a Typical Pipeline

An 8051 MCU may never be the right device if your design calls for high-speed, higher-order arithmetic. However, some of Silicon Labs' high-speed 8051 MCUs also implement a 16-bit MAC with a 40-bit accumulator. This technique enables single-cycle 16-bit MAC operations or multiplications to be performed. Certainly, it still takes a few cycles to load and unload the data.

Since the MAC is pipelined, the data can be moved into the input registers while the MAC is operating on the previous data. **Figure 2** shows a diagram of the MAC as implemented on the C8051F120 MCU.

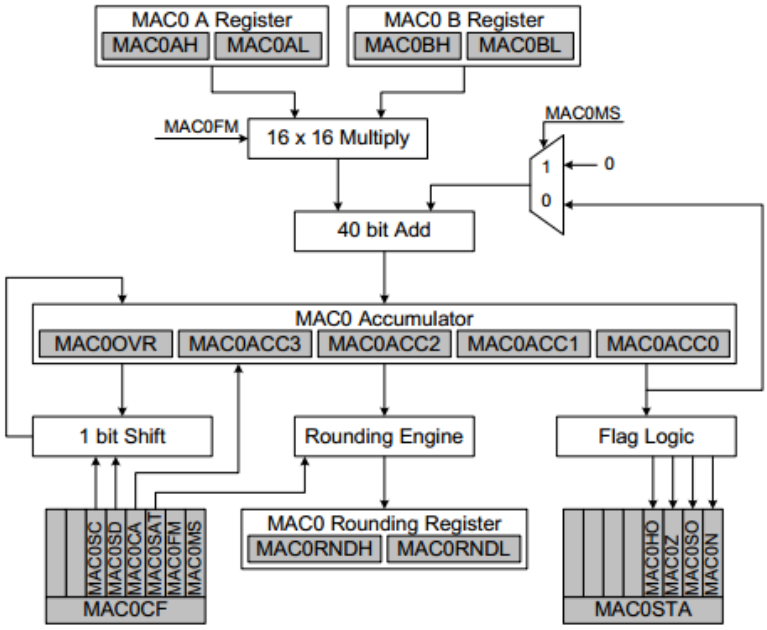

Figure 2. MAC Implementation

Meeting System Responsiveness Requirements

The 8051 core implements the ability to perform logic operations directly on some registers and memory locations. This is a very useful feature in almost any control application, be it industrial or otherwise. Given the frequencies of operation of the Silicon Labs devices, these operations can be performed in a single cycle. This allows for superior control response time, which means that a bit-banged bus definition can run at a fairly reasonable rate when compared to a hardware implementation of the same configuration. For example, a bit-banged full-duplex SPI can be implemented in 12 system clocks per bit, which supports a greater than 8 MHz bit rate for a 100 MHz system clock.

The other innovation was to implement this controller in a flash memory process with an embedded flash, which gave it the ability to start up and execute code quickly. Naturally, the instruction fetch path also had to keep up with the speed requirements, so advanced features, such as pre-fetch buffers and caches and branch-target-buffers, were implemented.

Silicon Labs' latest 8-bit devices, such as EFM8 Universal Bee (EFM8UBx) family of devices, carry on the tradition of implementing a 16-bit wide pre-fetch buffer to support 50MHz operation.

To take advantage of the higher performance characteristic of Silicon Labs 8051 based architecture a novel I/O architecture had to be implemented to support the vast number of peripherals that could be run simultaneously (or time shared). To this end, a priority crossbar architecture was developed to allow any peripheral to access almost any port in a deterministic manner. Thus, it became possible to implement a multitude of high-speed peripherals in the same system with a large I/O count that could all be controlled by the high-performance CPU.

Another advantage that 8051 cores have is that their I/Os are accessed at bus speed. Thus, if a pin needed to be sensed, and, based on the value of that pin, a decision has to be made to turn that pin around, a Silicon Labs 8051 MCU running at 100 MHz could do it in 50 ns. The same is not true of MCUs that have GPIOs on the APB bus where it will be running at some frequency slower than bus speed. If a 100 MHz MCU can only access its GPIOs at 50 a read of a port pin, a comparison, a port mode change instruction, and a write drive value instruction will take about 140 ns to execute compared to about 50 ns on an 8051 running at 100 MHz. Again, because the bus hierarchy is simpler on an 8051, branches can be taken faster than on architectures with a bus hierarchy.

Due to the nature of the 12-cycle execution latency of the 8051 core, interrupt latency could run into the hundreds of cycles, which made for slow control capabilities. The higher-performance devices obviously have far better interrupt latency, thus improving overall system response times to control/sensor interrupts.

Some of the newer Silicon Labs 8051 MCUs also implement four priority states in their interrupt hierarchy. This allows for finer granularity in interrupt handling, which is essential in a system with a large number of peripherals.

Adding Peripherals, USB and Wireless Connectivity

Silicon Labs high-performance 8051 based devices have enabled the integration of many useful peripherals including low- and full-speed USB. Running at 50 MHz, a Silicon Labs EFM8 Universal Bee 8051 has enough horsepower to run a USB stack while supporting additional peripherals such as two 800 kilosamples ADCs and a mix of UARTs, SPIs and DACs. **Figure 3** illustrates the 8051 core and peripherals of Silicon Labs EFM8 devices.

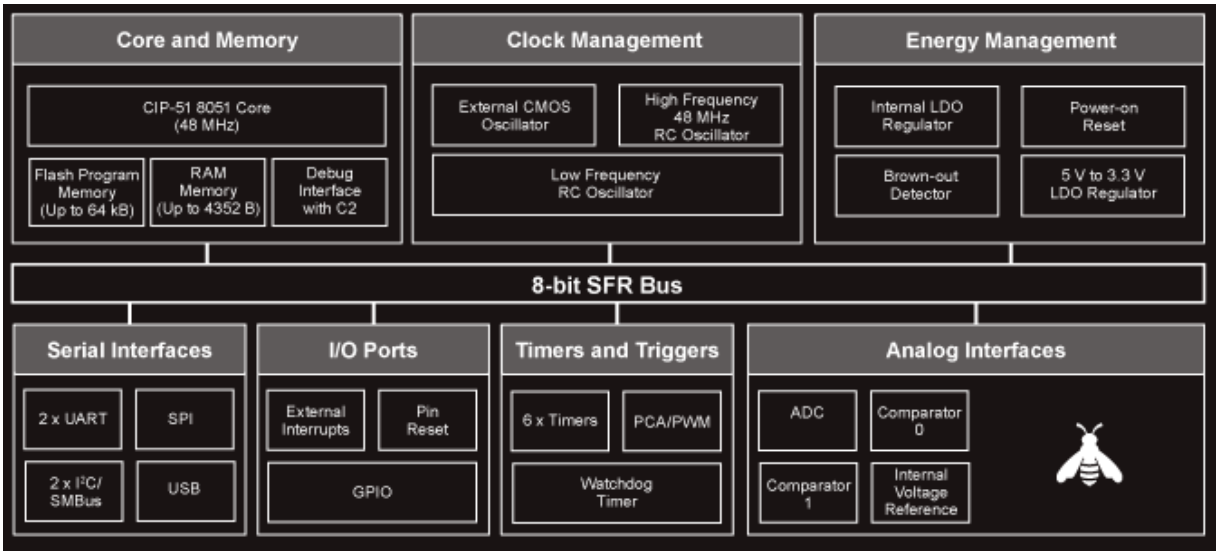

Figure 3. EFM8 Architectural Block Diagram

High-pin-count 8051 devices support an External Memory Interface (EMIF). This interface is capable of talking to any memory-mapped device (i.e., RAMs or other controllers). A typical app, such as an Ethernet controller, can be fully fed and controlled from a 50 MHz Silicon Labs 8051 based MCU with sufficient headroom to also run other peripherals.

Another class of low-power devices within the Silicon Labs portfolio also contain a sub-Gigahertz radio as in the Si1000. In these applications, the CPU is sufficiently powerful to run an entire radio stack, with some MIPS left over for data processing before wireless transmission.

These devices also happen to be low-power, and, since they are small, they do not consume much power when placed in snooze mode where all states are preserved.

A Case for Selecting 8051 based 8-bit MCUs

The 8051 core has a large installed base with literally millions of lines of code written for it. As has been shown in this discussion, the proven 8051 core has been significantly upgraded and modernized by Silicon Labs with the new EFM8 family of devices. The EFM8 8051 based families of devices are ideal for newer applications, such as connected end node devices for the Internet of Things (IoT) with require computational performance, system responsiveness, sensor integration and also have tight budgetary constraints.

Learn more about Silicon Labs' EFM8 MCU solutions and buy starter kits at www.silabs.com/efm8

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