

## CALCULATING TOTAL OUTPUT JITTER FOR PLLS

### 1. Introduction

Phase-locked loops (PLLs) within SONET/SDH systems are required to meet stringent jitter specifications. To ensure that the system, including the several PLLs in series, meets the output jitter requirements, it is useful to calculate the total output jitter from each PLL. A method for calculating the total output jitter is discussed in the following sections.

#### 1.1. Background

PLLs are control systems whose variable under control is the phase difference between the input and output signals. The input and output of a PLL is typically a sinusoidal carrier or a clock signal, but the phase control can be considered as independent of the actual carrier/clock frequencies. This independence is due to the fact that the phase detector discards the frequency information. Therefore, the input and output frequencies are only used for normalizing the phase noise to the output frequency.

The PLL effectively filters the incoming phase in a manner similar to that of a single-time-constant low-pass filter (the corner frequency of the filter set equal to the PLL loop-bandwidth). A single-time-constant filter is exact for type-I PLLs and is a close approximation for type-II PLLs. The approximation is valid if the jitter peaking is negligible (SONET/SDH requires jitter peaking to be less than 0.1 dB).

The remaining contributor to output phase noise is the PLL's own internal noise sources. For SONET/SDH related devices, internal noise is specified as the device's jitter generation. Jitter generation is specified as a root-mean-squared (RMS) and a peak-to-peak value.

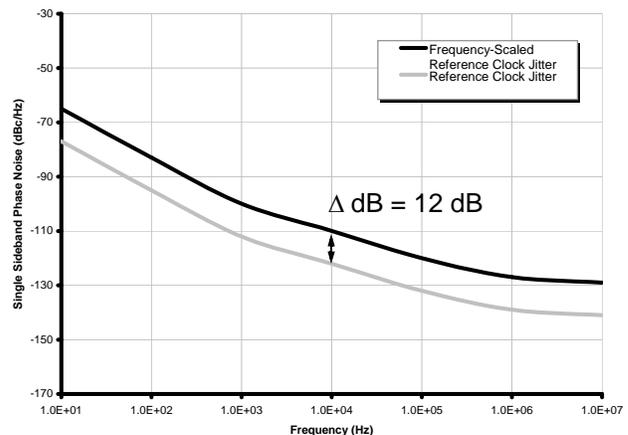
### 1.2. Procedure

To calculate the total output jitter from a PLL/clock multiplier, the following information is required: single-sideband (SSB) phase noise of the incoming reference signal, generated jitter (RMS) of the PLL, and the PLL's loop-bandwidth. The following procedure can be used to estimate the total output jitter:

1. Scale the reference signal SSB phase noise to the output frequency by adding

$$\Delta \text{dB} = 20 \log_{10} \left( \frac{f_{\text{out}}}{f_{\text{in}}} \right)$$

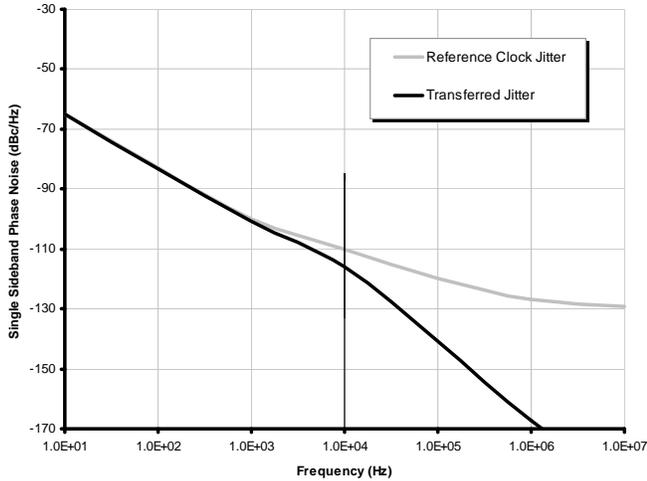
across the entire measured frequency band (see Figure 1). This scaling is required to account for the difference in period between the input and output signals.



**Figure 1. Frequency-Scaled Reference Clock Phase Noise Plot**

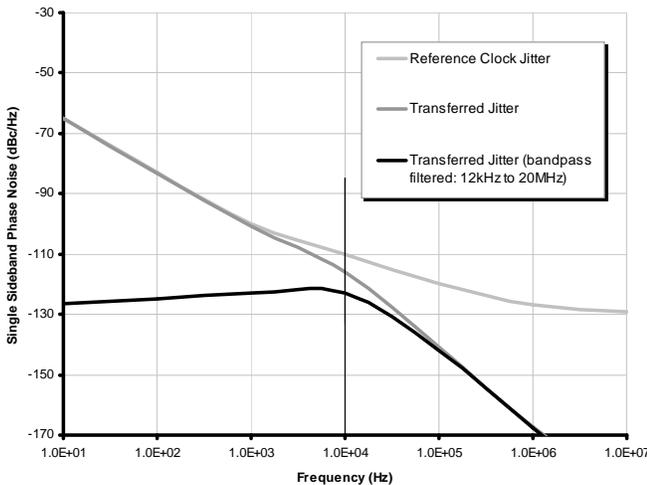
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- Apply a single-time-constant low-pass filter with a corner frequency equal to the PLL loop-bandwidth to the scaled reference signal SSB phase noise (See Figure 2). This filtering models the effect of the PLL on the incoming phase noise/jitter.



**Figure 2. PLL Filtered Reference Clock Phase Noise (Transferred Jitter)**

- Apply the appropriate SONET/SDH band-pass filter (e.g., 12 kHz to 20 MHz for OC-48) to the scaled and PLL filtered SSB phase noise (see Figure 3). SONET/SDH specifies that jitter generation be determined for a certain band of frequencies.



**Figure 3. SONET/SDH Filter Applied to the PLL Transferred Jitter**

- Integrate the scaled and filtered SSB phase noise to obtain an RMS value for the jitter. Integration must be made on the linear power scale and not on the traditional dBc/Hz scale. Multiply by 2 for double-sideband and divide by  $2 \times \pi$  to convert radians to unit-intervals (UI).
- Because the internal noise sources (generated jitter sources) are independent of the reference signal phase noise (i.e., uncorrelated), simply add the squares of the variances:

$$J_{\text{total}}^2 = J_{\text{filtered reference}}^2 + J_{\text{internal}}^2$$

This is the RMS of the total output random jitter on the PLL output signal. Typically, peak-to-peak jitter is between 8 and 10 times the RMS random jitter.

Lastly, calculate the total output jitter on the data. The jitter on the data is comprised of two sources and is typically reported as a peak-to-peak value. The two sources of jitter on the data are random jitter and deterministic jitter. The random jitter is nearly completely dominated by the PLL's random jitter. Deterministic jitter (i.e., ISI) is dependent on transmission effects and driver limitations. The device specifications provide a deterministic jitter number as measured at the output of the device package.

Additional deterministic jitter can arise from mis-termination on the PCB or other discontinuities (e.g., reflections or PCB non-idealities). To calculate the total jitter present on the data output, simply take the peak-to-peak random jitter and add it to the deterministic jitter:

$$J_{\text{total data}} = J_{\text{peak-to-peak random}} + J_{\text{deterministic}}$$

For example, to determine what input the reference signal jitter is allowed to have, a 7 mUIrms total output jitter simply use the first equation:

$$(7\text{mUI})^2 = J_{\text{filtered reference}}^2 + (2.5\text{mUI})^2$$

therefore:

$$J_{\text{filtered reference}}^2 = (6.5\text{mUI})^2$$

where 2.5 mUI is specified in the device data sheet

Remember, the reference signal is low-pass filtered by the PLL with a corner frequency equal to the loop-bandwidth. For the example so far, nothing unique to Silicon Labs has been assumed. However, once the low-pass loop-filter is taken into account, the REFCLK requirements are much reduced for the DSPLL™-based devices relative to competitor's devices.

## 1.3. Conclusion

Silicon Labs offers much lower loop-bandwidths than the competition because of the unique patented oscillator technology within the DSPLL-based devices. In addition, because of the DSPLL technology, the end user can make the trade-off between output jitter performance and reference jitter requirements by choosing different loop-bandwidths via external digital pins.

## DOCUMENT CHANGE LIST

### Revision 0.1 to Revision 0.2

- Removed references to Si5600.
- Added Figures 1, 2, and 3 to illustrate procedure.

### Revision 0.2 to Revision 0.3

- Updated title on page 1.

**NOTES:**



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