

# EFR32xG13 Wireless Gecko Reference Manual

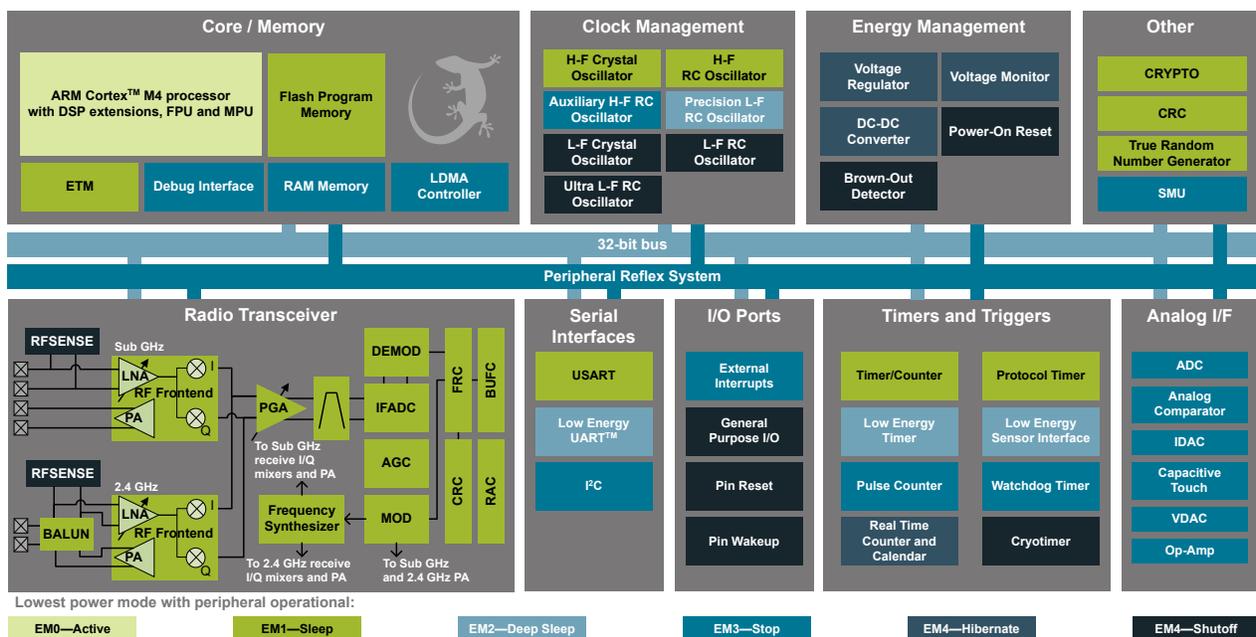


The Wireless Gecko portfolio of SoCs (EFR32) include Mighty Gecko (EFR32MG13), Blue Gecko (EFR32BG13), and Flex Gecko (EFR32FG13) families. With support for Zigbee®, Thread, Bluetooth Low Energy (BLE) and proprietary protocols, the Wireless Gecko portfolio is ideal for enabling energy-friendly wireless networking for IoT devices.

The single-die solution provides industry-leading energy efficiency, ultra-fast wakeup times, a scalable high-power amplifier, an integrated balun and no-compromise MCU features.

## KEY FEATURES

- 32-bit ARM® Cortex-M4 core with 40 MHz maximum operating frequency
- Scalable Memory and Radio configuration options available in several footprint compatible QFN packages
- 12-channel Peripheral Reflex System enabling autonomous interaction of MCU peripherals
- Autonomous Hardware Crypto Accelerator and True Random Number Generator
- Integrated balun for 2.4 GHz and integrated PA with up to 19 dBm transmit power for 2.4 GHz and 20 dBm transmit power for Sub-GHz radios
- Integrated DC-DC with RF noise mitigation
- Integrated PLFRCO eliminates external 32 kHz crystal for BLE applications



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## 1. About This Document

### 1.1 Introduction

This document contains reference material for the EFR32xG13 Wireless Gecko devices. All modules and peripherals in the EFR32xG13 Wireless Gecko devices are described in general terms. Not all modules are present in all devices and the feature set for each device might vary. Such differences, including pinout, are covered in the device data sheets and applicable errata documents.

### 1.2 Conventions

#### Register Names

Register names are given with a module name prefix followed by the short register name:

TIMERn\_CTRL - Control Register

The "n" denotes the module number for modules which can exist in more than one instance.

Some registers are grouped which leads to a group name following the module prefix:

GPIO\_Px\_DOUT - Port Data Out Register

The "x" denotes the different ports.

#### Bit Fields

Registers contain one or more bit fields which can be 1 to 32 bits wide. Bit fields wider than 1 bit are given with start (x) and stop (y) bit [y:x].

Bit fields containing more than one bit are unsigned integers unless otherwise is specified.

Unspecified bit field settings must not be used, as this may lead to unpredictable behaviour.

#### Address

The address for each register can be found by adding the base address of the module found in the Memory Map (see [Figure 4.2 System Address Space With Core and Code Space Listing on page 46](#)), and the offset address for the register (found in module Register Map).

#### Access Type

The register access types used in the register descriptions are explained in [Table 1.1 Register Access Types on page 28](#).

**Table 1.1. Register Access Types**

| Access Type           | Description   |
|-----------------------|---|
| R                     | Read only. Writes are ignored   |
| RW                    | Readable and writable   |
| RW1                   | Readable and writable. Only writes to 1 have effect   |
| (R)W1                 | Sometimes readable. Only writes to 1 have effect. Currently only used for IFC registers (see <a href="#">3.3.1.2 IFC Read-clear Operation</a> )         |
| W1                    | Read value undefined. Only writes to 1 have effect  |
| W                     | Write only. Read value undefined.   |
| RWH                   | Readable, writable, and updated by hardware   |
| RW(nB), RWH(nB), etc. | "(nB)" suffix indicates that register explicitly does not support peripheral bit set or clear (see <a href="#">4.2.3 Peripheral Bit Set and Clear</a> ) |

| Access Type       | Description   |
|-------------------|---|
| RW(a), R(a), etc. | "(a)" suffix indicates that register has actionable reads (see <a href="#">7.3.7 Debugger Reads of Actionable Registers</a> ) |

### Number format

**0x** prefix is used for hexadecimal numbers

**0b** prefix is used for binary numbers

Numbers without prefix are in decimal representation.

### Reserved

Registers and bit fields marked with **reserved** are reserved for future use. These should be written to 0 unless otherwise stated in the Register Description. Reserved bits might be read as 1 in future devices.

### Reset Value

The reset value denotes the value after reset.

Registers denoted with X have unknown value out of reset and need to be initialized before use. Note that read-modify-write operations on these registers before they are initialized results in undefined register values.

### Pin Connections

Pin connections are given with a module prefix followed by a short pin name:

CMU\_CLKOUT1 (Clock management unit, clock output pin number 1)

The location for the pin names given in the module documentation can be found in the device-specific data sheet.

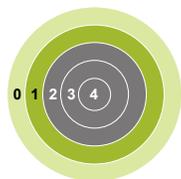
### 1.3 Related Documentation

Further documentation on the EFR32xG13 Wireless Gecko devices and the ARM Cortex-M4 can be found at the Silicon Labs and ARM web pages:

[www.silabs.com](http://www.silabs.com)

[www.arm.com](http://www.arm.com)

## 2. System Overview



### 2.1 Introduction

The high level features of EFR32xG13 Wireless Gecko include:

- High performance radio transceiver
  - Dual-band operation
  - Low power consumption in transmit, receive, and standby modes
  - Excellent receiver performance, including sensitivity, selectivity and blocking
  - Excellent transmitter performance, including programmable output power, low phase noise and PA ramping
  - Ultra Low Energy RF Detection for wake-up from any Energy Mode, through RFSense
- Configurable protocol support, including standards and customer developed protocols
  - Preamble and frame synchronization insertion in transmit and recovery in receive
  - Flexible CRC support, including configurable polynomial and multiple CRCs for single data frames
  - Basic address filtering performed in hardware
- High performance, low power MCU system
  - High Performance 32-bit ARM Cortex-M4 CPU
  - Flexible and efficient energy management
  - Complete set of digital peripherals
  - Peripheral Reflex System (PRS)
  - Precision analog interfaces
- Low external component count
  - Fully integrated 2.4 GHz BALUN
  - Integrated tunable crystal loading capacitors

A further introduction to the MCU and radio system is included in the following sections.

**Note:**

Detailed performance numbers, current consumption, pinout etc. is available in the device data sheet.

**Quick Facts****What?**

The EFR32 Wireless Gecko is a highly integrated, configurable and low power wireless System-on-Chip (SoC) with a robust set of MCU and radio peripherals.

**Why?**

The radio enables support for zigbee, Thread, Bluetooth Low Energy (BLE) and proprietary protocols in 2.4 GHz and sub-GHz frequency bands while the MCU system allows customized protocols and applications to run efficiently.

**How?**

Dynamic or fixed packet lengths, optional address recognition, and flexible CRC and crypto schemes makes the EFR32xG13 Wireless Gecko ideal for many low power wireless IoT applications. High performance analog and digital peripherals allows complete applications to run on the EFR32xG13 Wireless Gecko SoC.

## 2.2 Block Diagrams

The block diagram for the EFR32xG13 Wireless Gecko System-On-Chip series is shown in (Figure 2.1 EFR32xG13 Wireless Gecko System-On-Chip Block Diagram on page 31).

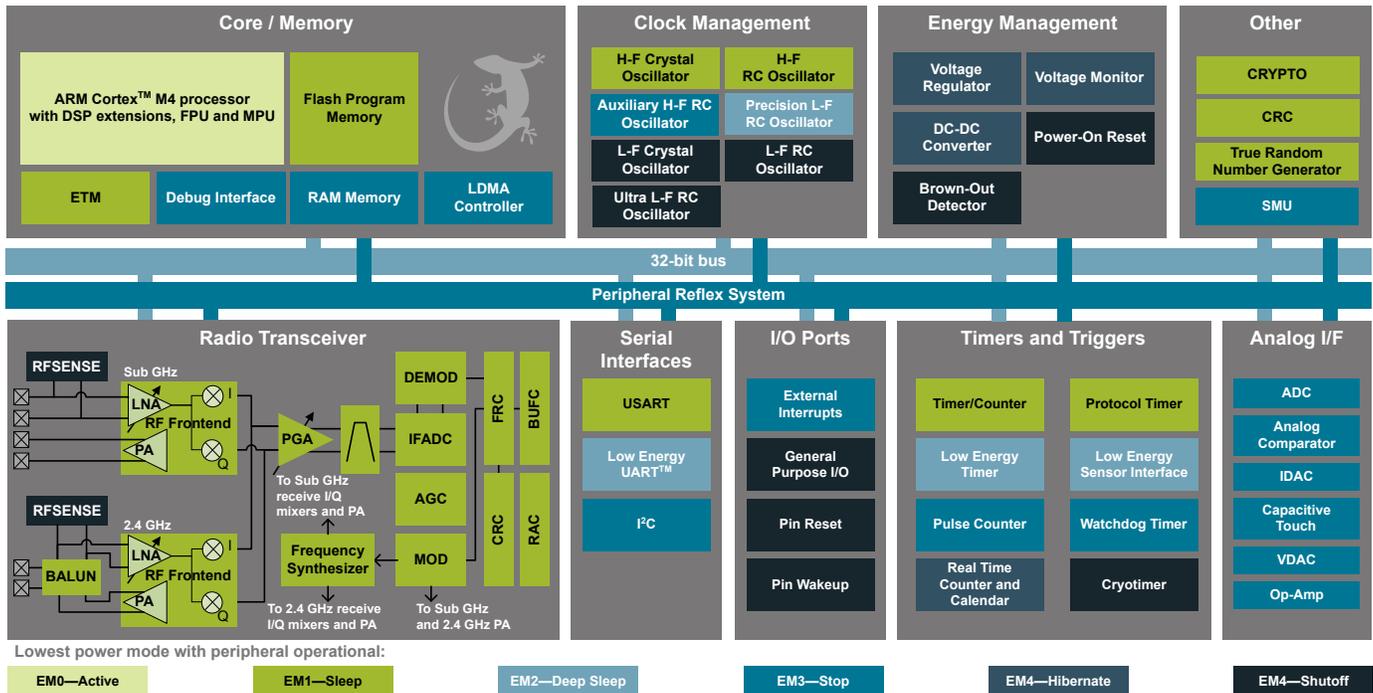


Figure 2.1. EFR32xG13 Wireless Gecko System-On-Chip Block Diagram

## 2.3 MCU Features Overview

- **ARMCortex-M4 CPU platform**
  - High Performance 32-bit processor @ up to 40 MHz
  - Memory Protection Unit
  - Wake-up Interrupt Controller
- **Flexible Energy Management System**
  - 5 Energy Modes from EM0 to EM4 provide flexibility between higher performance and low power
  - Power routing configurations including DCDC control
  - Voltage Monitoring and Brown Out Detection
  - State Retention
- **Up to 512 KB Flash**
- **Up to 64 KB RAM**
- **Up to 31 General Purpose I/O pins**
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 16 asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- **8 Channel DMA Controller**
  - Alternate/primary descriptors with scatter-gather/ping-pong operation
- **12 Channel Peripheral Reflex System**
  - Autonomous inter-peripheral signaling enables smart operation in low energy modes
- **CRYPTO Advanced Encryption Standard Accelerator**
  - AES encryption / decryption, with 128 or 256 bit keys
  - Multiple AES modes of operation, including Counter (CTR), Galois/Counter Mode (GCM), Cipher Block Chaining (CBC), Cipher Feedback (CFB) and Output Feedback (OFB).
  - Accelerated SHA-1 and SHA-2 (SHA-224 / SHA-256)
  - Accelerated Elliptic Curve Cryptography (ECC), with binary or prime fields
  - Flexible 256-bit ALU and sequencer
- **True Random Number Generator (TRNG)**
- **General Purpose Cyclic Redundancy Check**
  - Programmable 16-bit polynomial, fixed 32-bit polynomial
  - The General Purpose Cyclic Redundancy Check (GPCRC) module comes in addition to the radio CRC
- **Communication interfaces**
  - 3 Universal Synchronous/Asynchronous Receiver/Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S
    - Triple buffered full/half-duplex operation
    - Hardware flow control
    - 4-16 data bits
  - 1 Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - 2I<sup>2</sup>C Interface with SMBus support
    - Address recognition in Stop Mode
- **Timers/Counters**
  - 2 16-bit Timer/Counter
    - 3 or 4 Compare/Capture/PWM channels
    - Dead-Time Insertion on TIMER0
  - 1 32-bit Timer/Counter
    - 3 or 4 Compare/Capture/PWM channels
    - Dead-Time Insertion on WTIMER0
  - 16-bit Low Energy Timer
  - 32-bit Ultra Low Energy Timer/Counter (CRYOTIMER) for periodic wake-up from any Energy Mode
  - 32-bit Real-Time Counter and Calendar

- 16+16+32 bit Protocol Timer
- 16-bit Pulse Counter
  - Asynchronous pulse counting/quadrature decoding
- 2 Watchdog Timers with dedicated RC oscillator
- **Ultra low power precision analog peripherals**
  - 12-bit 1 Msamples/s Analog to Digital Converter
    - All APORT input channels available
    - On-chip temperature sensor
    - Single ended or differential operation
    - Conversion tailgating for predictable latency
  - 12-bit 500 ksps Digital to Analog Converter
    - 2 single ended channels/1 differential channel
  - Up to 3 Operational Amplifiers
    - Supports rail-to-rail inputs and outputs
    - Programmable gain
  - Current Digital to Analog Converter
    - Source or sink a configurable constant current
  - 2 Analog Comparator
    - Programmable speed/current
  - Capacitive Sense Module
    - Supports multi-channel scan and multi-channel gang conversions
    - Low power, fast response times
  - Analog Port
- **Low-energy sensor interface**
  - Autonomous sensor monitoring in deep sleep mode
  - Wide range of supported sensors, including LC sensors and capacitive touch switches
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **Debug Interface**
  - 4-pin Joint Test Action Group (JTAG) interface
  - 2-pin serial-wire debug (SWD) interface
  - Embedded Trace Macrocell (ETM)

## 2.4 Oscillators and Clocks

EFR32xG13 Wireless Gecko has six different oscillators integrated, as shown in [Table 2.1 EFR32xG13 Wireless Gecko Oscillators on page 34](#).

**Table 2.1. EFR32xG13 Wireless Gecko Oscillators**

| Oscillator | Frequency       | Optional? | External components | Description  |
|------------|-----------------|-----------|---------------------|--|
| HFXO       | 38 MHz - 40 MHz | No        | Crystal             | High accuracy, low jitter high frequency crystal oscillator. Tunable crystal loading capacitors are fully integrated. The HFXO is required for all types of RF communication to be active. |
| HFRCO      | 1 MHz - 38 MHz  | No        | -                   | Medium accuracy RC oscillator, typically used for timing during startup of the HFXO and as a clock source as long as no RF communication is active.  |
| AUXHFRCO   | 1 MHz - 38 MHz  | No        | -                   | Medium accuracy RC oscillator, typically used as alternative clock source for Analog to Digital Converter or Debug Trace.  |
| PLFRCO     | 32.768 kHz      | No        | -                   | Self-Calibrating RC oscillator, typically used for RTCC and BLE sleep timing.  |
| LFRCO      | 32768 Hz        | No        | -                   | Medium accuracy frequency reference typically used for medium accuracy RTCC timing.  |
| LFXO       | 32768 Hz        | Yes       | Crystal             | High accuracy frequency reference typically used for high accuracy RTCC timing. Tunable crystal loading capacitors are fully integrated.   |
| ULFRCO     | 1000 Hz         | No        | -                   | Ultra low frequency oscillator typically used for the watchdog timer.  |

The RC oscillators can be calibrated against either of the crystal oscillators in order to compensate for temperature and voltage supply variations. Hardware support is included to measure the frequency of various oscillators against each other. The PLFRCO oscillator automatically recalibrates itself against an available HFXO clock for highest precision.

Oscillator and clock management is available through the Clock Management Unit (CMU), see section [12. CMU - Clock Management Unit](#) for details.

## 2.5 RF Frequency Synthesizer

The Fractional-N RF Frequency Synthesizer (SYNTH) provides a low phase noise LO signal to be used in both receive and transmit modes.

The capabilities of the SYNTH include:

- High performance, low phase noise
- Fast frequency settling
- Fast and fully automated calibration
- Sub 100 Hz frequency resolution across the supported frequency bands

## 2.6 Modulation Modes

EFR32xG13 Wireless Gecko supports a wide range of modulation modes in transmit and receive:

- 2-FSK, 2-GFSK, 4-FSK, 4-GFSK, MSK, GMSK, O-QPSK with half-sine shaping, ASK / OOK, DBPSK TX
- NRZ or Manchester support
- UART mode over air for legacy protocols
- Data rates ranging from 600 bps up to 2 Mbps
- Configurable frequency deviation
- Configurable Direct Sequence Spread Spectrum (DSSS), with spread sequences up to 32 chips encoding up to 4 information bits
- Configurable 4-FSK symbol encoding

## 2.7 Transmit Mode

In transmit mode EFR32xG13 Wireless Gecko performs the following functionality:

- Automatic PA power ramping during the start and end of a frame transmit
- Programmable output power
- Optional preamble and synchronization word insertion
- Accurate transmit frame timing to support time synchronized radio protocols
- Optional Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) or Listen Before Talk (LBT) hardware support
- Integrated transmit test modes, as described in [2.17 RF Test Modes](#)

## 2.8 Receive Mode

In receive mode EFR32xG13 Wireless Gecko performs the following functionality:

- A single-ended (2.4 GHz) or differential (Sub-GHz) LNA amplifies the input RF signal. The amplified signal is then mixed to a low-IF signal through the quadrature down-conversion mixer. Further signal filtering is performed before conversion to a digital signal through the I/Q ADC.
- Digitally configurable receiver bandwidth from 100 Hz to 2.5 MHz
- Timing recovery on received data, including simultaneous support for two different frame synchronization words
- Automatic frequency offset compensation, to compensate for carrier frequency offset between the transmitter and receiver
- Support for a wide range of modulation formats as described in section [2.6 Modulation Modes](#)

## 2.9 Data Buffering

EFR32xG13 Wireless Gecko supports buffered transmit and receive modes through its buffer controller (BUFC), with four individually configurable buffers. The BUFC uses the system RAM as storage, and each buffer can be individually configured with parameters such as:

- Buffer size
- Buffer interrupt thresholds
- Buffer RAM location
- Overflow and underflow detection

In receive mode, data following frame synchronization is moved directly from the demodulator to the buffer storage.

In transmit mode, data following the inserted preamble and synchronization word is moved directly from the buffer storage to the modulator.

## 2.10 Unbuffered Data Transfer

For most system designs it is recommended to use the data buffering within EFR32xG13 Wireless Gecko to provide a convenient user interface.

In cases where data buffering within EFR32xG13 Wireless Gecko is not desired, it is possible to set up direct unbuffered data transfers using a single-pin or two-pin interface on EFR32xG13 Wireless Gecko. A bit clock output is provided on the Serial Clock (SC) output pin, and a serial bitstream is provided to EFR32xG13 Wireless Gecko in a transmit mode and from EFR32xG13 Wireless Gecko in a receive mode.

In unbuffered data transfer modes the hardware support provided by EFR32xG13 Wireless Gecko to perform preamble and frame synchronization insertion in transmit mode and detection in receive mode can still optionally be used.

## 2.11 Frame Format Support

EFR32xG13 Wireless Gecko has an extensive support for frame handling in transmit and receive modes, which allows effective handling of even advanced protocols. The support includes:

- Preamble and frame synchronization inserted into transmitted frames
- Full frame synchronization of received frames
- Simple address matching of received frames in hardware, further configurable address and frame filtering supported through sequencer
- Support for variable length frames
- Automated CRC calculation and verification
- Configurable bit ordering, with the most or least significant bit transmitted and received first

The frame format support is controlled by the Frame Controller (FRC).

## 2.12 Hardware CRC Support

EFR32xG13 Wireless Gecko supports a configurable CRC generation in transmit and verification in receive mode:

- 8, 16, 24 or 32 bit CRC value
- Configurable polynomial and initialization value
- Optional inversion of CRC value over air
- Configurable CRC byte ordering
- Support for multiple CRC values calculated and verified per transmitted or received frame
- The CRC module is typically controlled by the Frame Controller (FRC) for in-line operations in transmit and receive modes. Alternatively, the CRC module may be accessed directly from software to calculate and verify CRC data.

## 2.13 Convolutional Encoding / Decoding

EFR32xG13 Wireless Gecko includes hardware support for convolutional encoding and decoding, for forward error correction (FEC). This feature is performed by the Frame Controller (FRC) module:

- Constraint length configurable up to 7, for the highest robustness
- Configurable puncturing, to achieve rates between 1/2 rate and full rate
- Configurable soft decision or hard decision decoding
- Convolutional coding may be used together with the symbol interleaver to improve robustness against burst errors

## 2.14 Binary Block Encoding / Decoding

EFR32xG13 Wireless Gecko includes hardware support for binary block encoding and decoding, both performed real-time in the transmit and receive path. This is performed in the Frame Controller (FRC) module:

The block coding works on blocks of up to 16 bits of data and adds parity bits to be capable of single or multiple bit corrections by the receiver.

- One or more parity bits can be added and verified
- Bit error correction
- Lookup-codes can be used to implement virtually any block coding scheme

## 2.15 Data Encryption and Authentication

EFR32xG13 Wireless Gecko has hardware support for AES encryption, decryption and authentication modes. These security operations can be performed on data in RAM or any data buffer, without further CPU intervention. The key size is 128 bits.

AES modes of operations directly supported by the EFR32xG13 Wireless Gecko hardware are listed in [Table 2.2 AES Modes of Operation With Hardware Support on page 37](#). In addition to these modes, other modes can also be implemented by using combinations of modes. For example, the CCM mode can be implemented using the CTR and CBC-MAC modes in combination.

**Table 2.2. AES Modes of Operation With Hardware Support**

| AES Mode | Encryption / Decryption | Authentication | Comment  |
|----------|-------------------------|----------------|--|
| ECB      | Yes                     | -              | Electronic Code Book                                     |
| CTR      | Yes                     | -              | Counter mode   |
| CCM      | Yes                     | Yes            | Counter with CBC-MAC                                     |
| CCM*     | Yes                     | Yes            | CCM with encryption-only and integrity-only capabilities |
| GCM      | Yes                     | Yes            | Galois Counter Mode                                      |
| CBC      | Yes                     | -              | Cipher Block Chaining                                    |
| CBC-MAC  | -                       | Yes            | Cipher Block Chaining, Message Authentication Code       |
| CMAC     | -                       | Yes            | Cipher-based MAC   |
| CFB      | Yes                     | -              | Cipher Feedback  |
| OFB      | Yes                     | -              | Output Feedback  |

The CRYPTO module can operate directly on data buffers provided by the BUFC module. It is also possible to provide data directly from the embedded Cortex-M4 or via DMA.

A True Random Number Generator (TRNG) module is also included for additional security. The TRNG is a non-deterministic random number generator based on a full hardware solution, and is suitable for cryptographic key generation.

## 2.16 Timers

EFR32xG13 Wireless Gecko includes multiple timers, as can be seen from [Table 2.3 EFR32xG13 Wireless Gecko Timers Overview on page 38](#).

**Table 2.3. EFR32xG13 Wireless Gecko Timers Overview**

| Timer         | Number of instances | Typical clock source  | Overview   |
|---------------|---------------------|---|--|
| RTCC          | 1 (2)               | Low frequency (LFXO or LFRCO)   | 32 bit Real Time Counter and Calendar, typically used to enable wakeup on compare match. A second RTC module is used by the radio software drivers for accurately timing inactive periods in the radio communication protocol. |
| PROTIMER      | 1                   | High frequency (HFXO or HFRCO)  | 16+16+32 bit Protocol Timer, typically used to accurately control detailed RF protocol timing in transmit and receive modes.   |
| TIMER         | 2                   | High frequency (HFXO or HFRCO)  | 16 bit general purpose timer.  |
| WTIMER        | 1                   | High frequency (HFXO or HFRCO)  | 32 bit general purpose timer.  |
| SysTick timer | 1                   | High frequency (HFXO or HFRCO) or low frequency (LFXO, LFRCO or ULFRCO) | 32 bit SysTick timer integrated in the Cortex-M4. Typically used as an Operating System timer.   |
| WDOG          | 1                   | Low frequency (LFXO, LFRCO or ULFRCO)                                   | Watch dog timer. Once enabled, this module must be periodically accessed. If not, this is considered an error and the EFR32xG13 Wireless Gecko is reset in order to recover the system.  |
| LETIMER       | 1                   | Low frequency (LFXO, LFRCO or ULFRCO)                                   | Low energy general purpose timer.  |

Advanced interconnect features allows synchronization between timers. This includes:

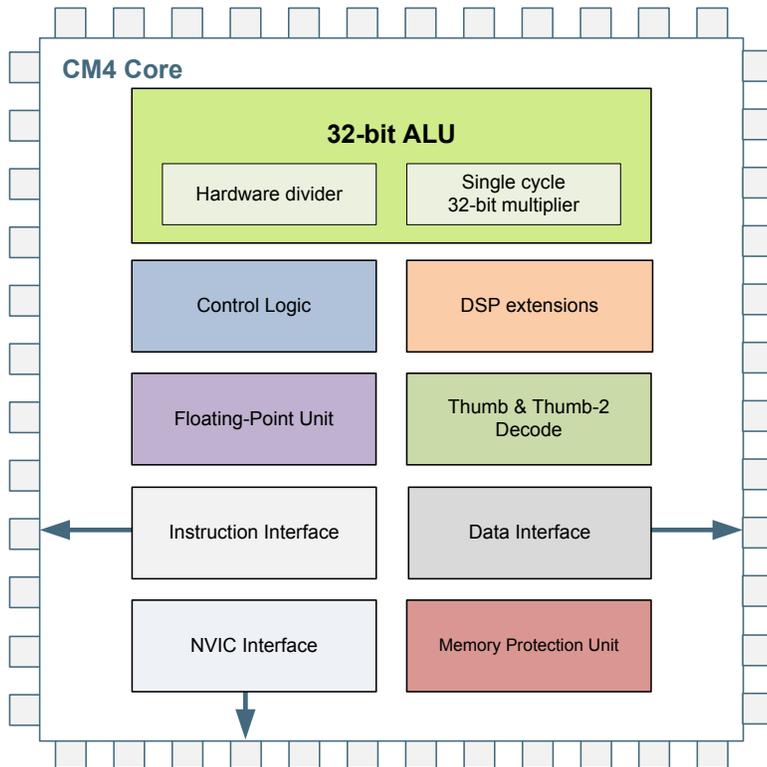
- Start / stop any high frequency timer synchronized with the RTCC
- Trigger RSM state transitions based on compare timer compare match, for instance to provide clock cycle accuracy on frame transmit timing

## 2.17 RF Test Modes

EFR32xG13 Wireless Gecko supports a wide range of RF test modes typically used for characterization and regulation compliance testing, including:

- Unmodulated carrier transmit
- Modulated carrier transmit, with internal configurable pseudo random data generator
- Continuous data reception for Bit Error Rate (BER) measurements
- Storing of raw receiver data to RAM
- Transmit of raw frequency data from RAM

### 3. System Processor



#### Quick Facts

##### What?

The industry leading Cortex-M4 processor from ARM is the CPU in the EFR32xG13 Wireless Gecko devices.

##### Why?

The ARM Cortex-M4 is designed for exceptionally short response time, high code density, and high 32-bit throughput while maintaining a strict cost and power consumption budget.

##### How?

Combined with the ultra low energy peripherals available in EFR32xG13 Wireless Gecko devices, the Cortex-M4 processor's Harvard architecture, 3 stage pipeline, single cycle instructions, Thumb-2 instruction set support, and fast interrupt handling make it perfect for 8-bit, 16-bit, and 32-bit applications.

#### 3.1 Introduction

The ARM Cortex-M4 32-bit RISC processor provides outstanding computational performance and exceptional system response to interrupts while meeting low cost requirements and low power consumption.

The ARM Cortex-M4 implemented is revision r0p1.

### 3.2 Features

- Harvard architecture
  - Separate data and program memory buses (No memory bottleneck as in a single bus system)
- 3-stage pipeline
- Thumb-2 instruction set
  - Enhanced levels of performance, energy efficiency, and code density
- Single cycle multiply and hardware divide instructions
  - 32-bit multiplication in a single cycle
  - Signed and unsigned divide operations between 2 and 12 cycles
- Atomic bit manipulation with bit banding
  - Direct access to single bits of data
  - Two 1MB bit banding regions for memory and peripherals mapping to 32MB alias regions
  - Atomic operation, cannot be interrupted by other bus activities
- 1.25 DMIPS/MHz
- Memory Protection Unit
  - Up to 8 protected memory regions
- 24 bits System Tick Timer for Real Time OS
- Excellent 32-bit migration choice for 8/16 bit architecture based designs
  - Simplified stack-based programmer's model is compatible with traditional ARM architecture and retains the programming simplicity of legacy 8-bit and 16-bit architectures
- Aligned or unaligned data storage and access
  - Contiguous storage of data requiring different byte lengths
  - Data access in a single core access cycle
- Integrated power modes
  - Sleep Now mode for immediate transfer to low power state
  - Sleep on Exit mode for entry into low power state after the servicing of an interrupt
  - Ability to extend power savings to other system components
- Optimized for low latency, nested interrupts

### 3.3 Functional Description

For a full functional description of the ARM Cortex-M4 implementation in the EFR32xG13 Wireless Gecko family, the reader is referred to the ARM Cortex-M4 documentation provided by ARM.

### 3.3.1 Interrupt Operation

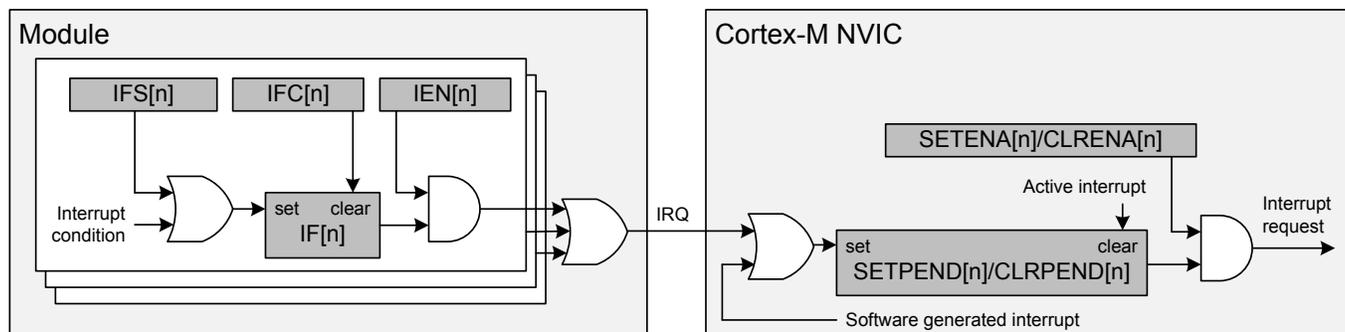


Figure 3.1. Interrupt Operation

The interrupt request (IRQ) lines are connected to the Cortex-M4. Each of these lines (shown in [Table 3.1 Interrupt Request Lines \(IRQ\) on page 42](#)) is connected to one or more interrupt flags in one or more modules. The interrupt flags are set by hardware on an interrupt condition. It is also possible to set/clear the interrupt flags through the IFS/IFC registers. Each interrupt flag is then qualified with its own interrupt enable bit (IEN register), before being OR'ed with the other interrupt flags to generate the IRQ. A high IRQ line will set the corresponding pending bit (can also be set/cleared with the SETPEND/CLRPEND bits in ISPR0/ICPR0) in the Cortex-M4 NVIC. The pending bit is then qualified with an enable bit (set/cleared with SETENA/CLRENA bits in ISER0/ICER0) before generating an interrupt request to the core. [Figure 3.1 Interrupt Operation on page 41](#) illustrates the interrupt system. For more information on how the interrupts are handled inside the Cortex-M4, the reader is referred to the **ARM Cortex-M4 Technical Reference Manual**.

#### 3.3.1.1 Avoiding Extraneous Interrupts

There can be latencies in the system such that clearing an interrupt flag could take longer than leaving an Interrupt Service Routine (ISR). This can lead to the ISR being re-entered as the interrupt flag has yet to clear immediately after leaving the ISR. To avoid this, when clearing an interrupt flag at the end of an ISR, the user should execute ARM's Data Synchronization Barrier (DSB) instruction. Another approach is to clear the interrupt flag immediately after identifying the interrupt source and then service the interrupt as shown in the pseudo-code below. The ISR typically is sufficiently long to more than cover the few cycles it may take to clear the interrupt status, and also allows the status to be checked for further interrupts before exiting the ISR.

```
irqXServiceRoutine() {
    do {
        clearIrqXStatus();
        serviceIrqX();
    } while(irqXStatusIsActive());
}
```

#### 3.3.1.2 IFC Read-clear Operation

In addition to the normal interrupt setting and clearing operations via the IFS/IFC registers, there is an additional atomic Read-clear operation that can be enabled by setting IFCREADCLEAR=1 in the MSC\_CTRL register. When enabled, reads of peripheral IFC registers will return the interrupt vector (mirroring the IF register), while at the same time clearing whichever interrupt flags are set. This operation is functionally equivalent to reading the IF register and then writing the result immediately back to the IFC register.

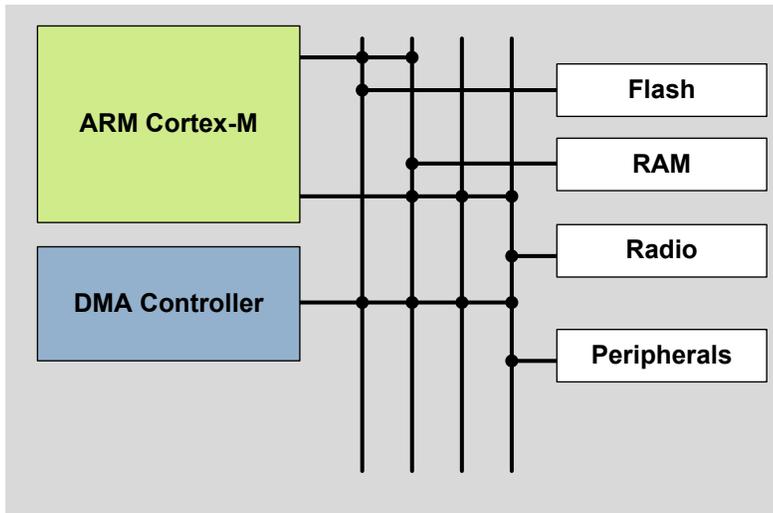
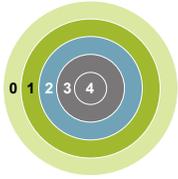
## 3.3.2 Interrupt Request Lines (IRQ)

Table 3.1. Interrupt Request Lines (IRQ)

| IRQ # | Source(s)      |
|-------|----------------|
| 0     | EMU            |
| 2     | WDOG0          |
| 3     | WDOG1          |
| 9     | LDMA           |
| 10    | GPIO_EVEN      |
| 11    | TIMER0         |
| 12    | USART0_RX      |
| 13    | USART0_TX      |
| 14    | ACMP0<br>ACMP1 |
| 15    | ADC0           |
| 16    | IDAC0          |
| 17    | I2C0           |
| 18    | GPIO_ODD       |
| 19    | TIMER1         |
| 20    | USART1_RX      |
| 21    | USART1_TX      |
| 22    | LEUART0        |
| 23    | PCNT0          |
| 24    | CMU            |
| 25    | MSC            |
| 26    | CRYPTO0        |
| 27    | LETIMER0       |
| 31    | RTCC           |
| 33    | CRYOTIMER      |
| 35    | FPUEH          |
| 36    | SMU            |
| 37    | WTIMER0        |
| 38    | USART2_RX      |
| 39    | USART2_TX      |
| 40    | I2C1           |
| 41    | VDAC0          |
| 42    | CSEN           |
| 43    | LESENSE        |

| IRQ # | Source(s) |
|-------|-----------|
| 44    | CRYPTO1   |
| 45    | TRNG0     |

## 4. Memory and Bus System



### Quick Facts

#### What?

A low latency memory system including low energy Flash and RAM with data retention which makes the energy modes attractive.

#### Why?

RAM retention reduces the need for storing data in Flash and enables frequent use of the ultra low energy modes EM2 Deep Sleep and EM3 Stop.

#### How?

Low energy and non-volatile Flash memory stores program and application data in all energy modes and can easily be reprogrammed in system. Low leakage RAM with data retention in EM0 Active to EM3 Stop removes the data restore time penalty, and the DMA ensures fast autonomous transfers with predictable response time.

## 4.1 Introduction

The EFR32xG13 Wireless Gecko contains an AMBA AHB Bus system to allow bus masters to access the memory mapped address space. A multilayer AHB bus matrix connects the 5 master bus interfaces to the AHB slaves (Figure 4.1 EFR32xG13 Wireless Gecko Bus System on page 45). The bus matrix allows several AHB slaves to be accessed simultaneously. An AMBA APB interface is used for the peripherals, which are accessed through an AHB-to-APB bridge connected to the AHB bus matrix. The 5 AHB bus masters are:

- **Cortex-M4 ICode:** Used for instruction fetches from Code memory (valid address range: 0x00000000 - 0x1FFFFFFF)
- **Cortex-M4 DCode:** Used for debug and data access to Code memory (valid address range: 0x00000000 - 0x1FFFFFFF)
- **Cortex-M4 System:** Used for data and debug access to system space. It can access entire memory space except Code memory (valid address range: 0x20000000 - 0xFFFFFFFF)
- **DMA:** Can access the entire memory space except the internal core memory region and the DMEM code region
- **Sequencer Code:** Used for instruction fetches and data accesses. Instruction fetches still come from data memory. (valid address range: 0x00000000 - 0x0FFFFFFF, 0x20000000 - 0x3FFFFFFF)
- **Sequencer System:** Can access entire memory space except internal core memory region and RAM code space (valid address range: 0x00000000 - 0x0FFFFFFF, 0x20000000 - 0xDFFFFFFF)
- **BUFC:** Can access general purpose SRAM (valid address range: 0x20000000 - 0x20FFFFFF)
- **FRC:** Can access general purpose SRAM (valid address range: 0x20000000 - 0x20FFFFFF)

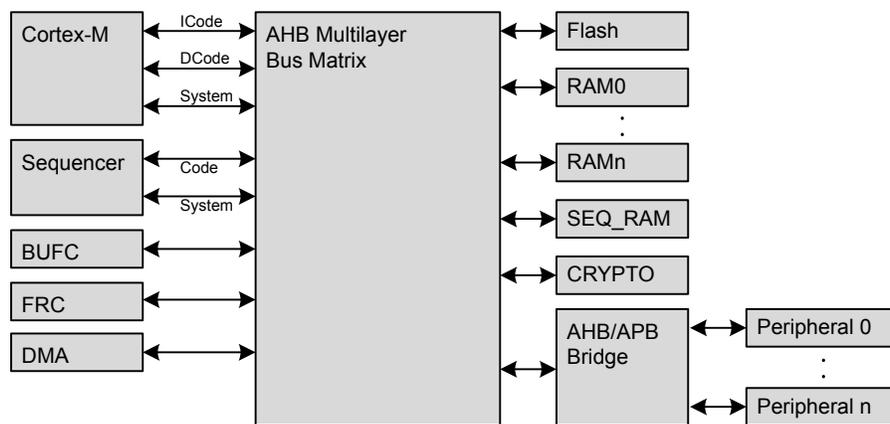
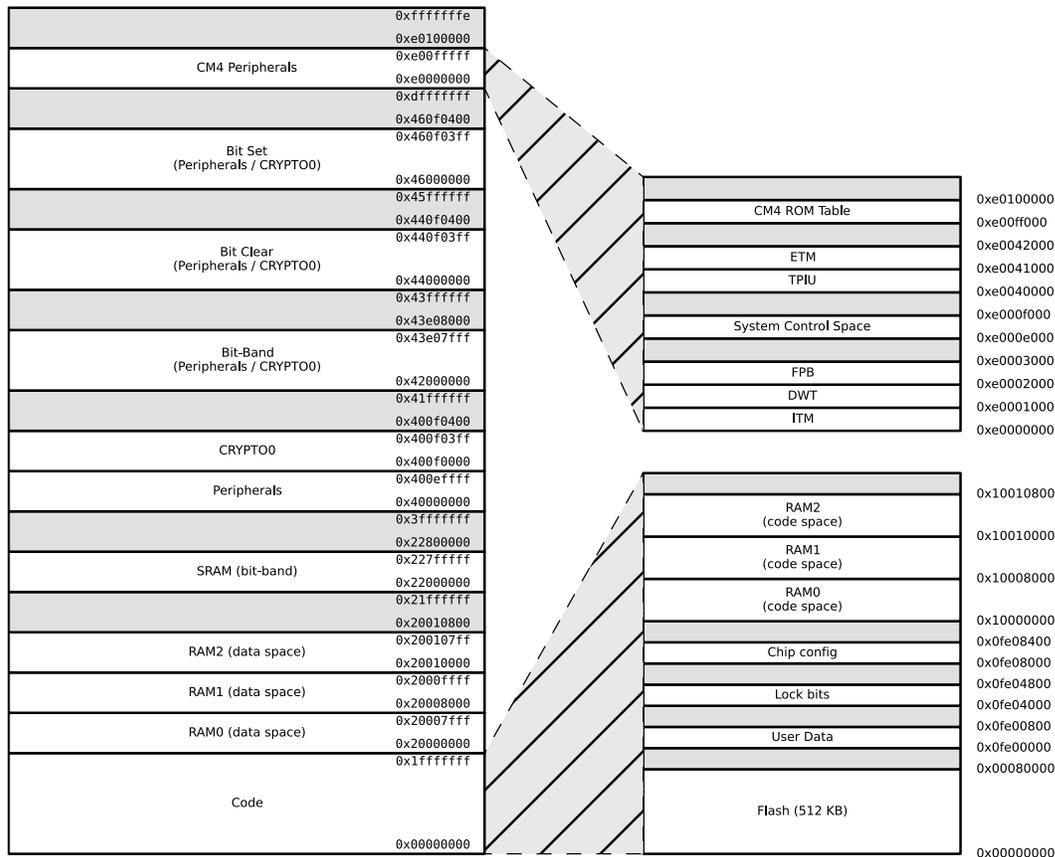


Figure 4.1. EFR32xG13 Wireless Gecko Bus System

## 4.2 Functional Description

The memory segments are mapped together with the internal segments of the Cortex-M4 into the system memory map shown by [Figure 4.2 System Address Space With Core and Code Space Listing on page 46](#).



**Figure 4.2. System Address Space With Core and Code Space Listing**

Additionally, the peripheral address map is detailed by [Figure 4.3 System Address Space With Peripheral Listing on page 47](#).

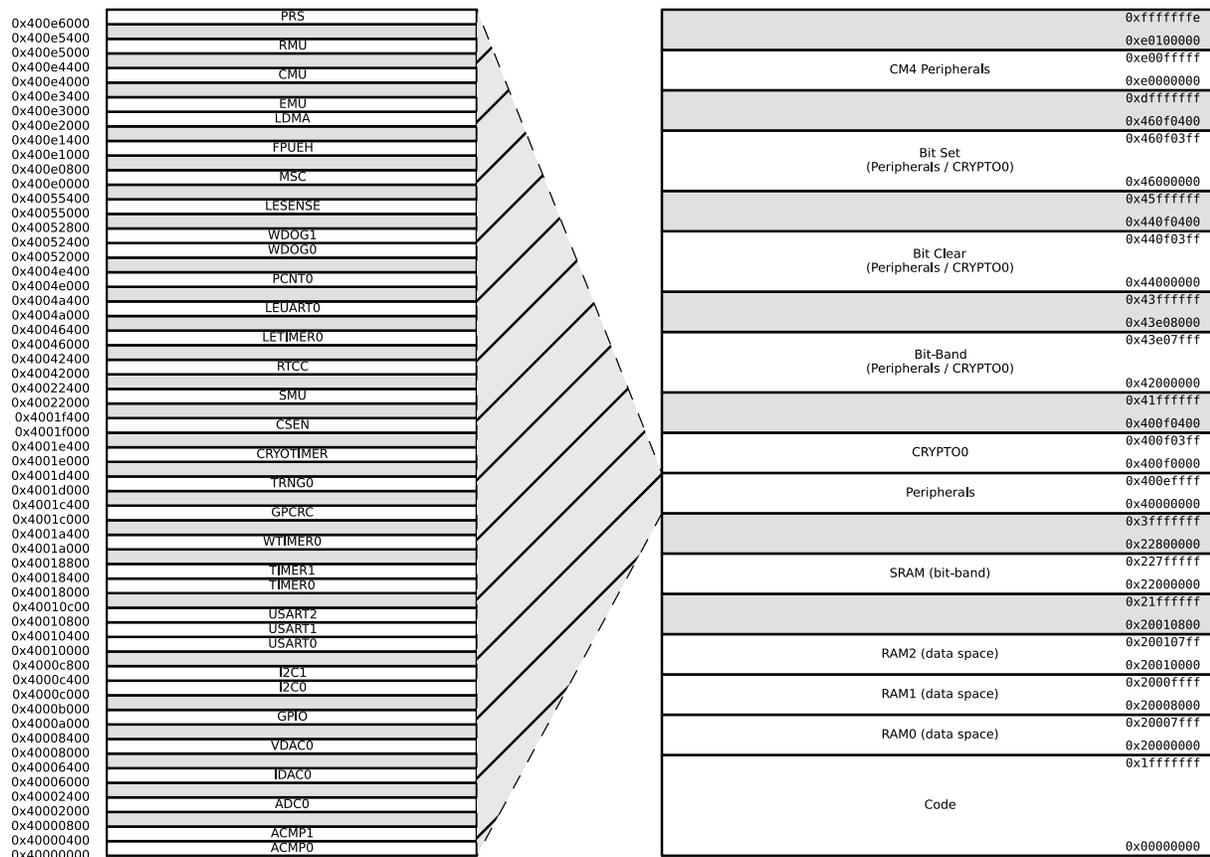


Figure 4.3. System Address Space With Peripheral Listing

The embedded SRAM is located at address 0x20000000 in the memory map of the EFR32xG13 Wireless Gecko. When running code located in SRAM starting at this address, the Cortex-M4 uses the System bus interface to fetch instructions. This results in reduced performance as the Cortex-M4 accesses stack, other data in SRAM and peripherals using the System bus interface. To be able to run code from SRAM efficiently, the SRAM is also mapped in the code space at address 0x10000000.

When running code from this space, the Cortex-M4 fetches instructions through the I/D-Code bus interface, leaving the System bus interface for data access.

The SRAM mapped into the code space can however only be accessed by the CPU and not any other bus masters, e.g. DMA. See [4.5 SRAM](#) for more detailed info on the system SRAM.

The Sequencer RAM is used by the Sequencer for both instructions and data. This RAM is also available for general use by most AHB masters.

### 4.2.1 Peripheral Non-Word Access Behavior

When writing to peripheral registers, all accesses are treated as 32-bit accesses. This means that writes to a register need to be large enough to cover all bits of register, otherwise, any uncovered bits may become corrupted from the partial-word transfer. Thus, the safest practice is to always do 32-bit writes to peripheral registers.

When reading, there is generally no issue with partial word accesses, however, note that any read action (e.g. FIFO popping) will be triggered regardless of whether the actual FIFO bit-field was included in the transfer size.

**Note:** The implementation of bit-banding in the core is such that bit-band accesses forward the transfer size info into the actual bus transfer size, so the same restrictions apply to bit-band accesses as apply to normal read/write accesses.

### 4.2.2 Bit-banding

The SRAM bit-band alias and peripheral bit-band alias regions are located at 0x22000000 and 0x42000000 respectively. Read and write operations to these regions are converted into masked single-bit reads and atomic single-bit writes to the embedded SRAM and peripherals of the EFR32xG13 Wireless Gecko.

**Note:** Bit-banding is only available through the CPU. No other AHB masters (e.g. DMA) can perform Bit-banding operations.

Using a standard approach to modify a single register or SRAM bit in the aliased regions, would require software to read the value of the byte, half-word or word containing the bit, modify the bit, and then write the byte, half-word or word back to the register or SRAM address. Using bit-banding, this can be done in a single operation, consuming only two bus cycles. As read-writeback, bit-masking and bit-shift operations are not necessary in software, code size is reduced and execution speed improved.

The bit-band regions allow each bit in the SRAM and Peripheral areas of the memory map to be addressed. To set or clear a bit in the embedded SRAM, write a 1 or a 0 to the following address:

$$\text{bit\_address} = 0x22000000 + (\text{address} - 0x20000000) \cdot 32 + \text{bit} \cdot 4$$

where address is the address of the 32-bit word containing the bit to modify, and bit is the index of the bit in the 32-bit word.

To modify a bit in the Peripheral area, use the following address:

$$\text{bit\_address} = 0x42000000 + (\text{address} - 0x40000000) \cdot 32 + \text{bit} \cdot 4$$

### 4.2.3 Peripheral Bit Set and Clear

The EFR32xG13 Wireless Gecko supports bit set and bit clear access to all peripherals except those listed in [Table 4.1 Peripherals that Do Not Support Bit Set and Bit Clear on page 49](#). The bit set and bit clear functionality (also called Bit Access) enables modification of bit fields (single bit or multiple bit wide) without the need to perform a read-modify-write (though it is functionally equivalent). Also, the operation is contained within a single bus access (for HF peripherals), unlike the Bit-banding operation described in section [4.2.2 Bit-banding](#) which consumes two bus accesses per operation. All AHB masters can utilize this feature.

The bit clear aliasing region starts at 0x44000000 and the bit set aliasing region starts at 0x46000000. Thus, to apply a bit set or clear operation, write the bit set or clear mask to the following addresses:

$$\text{bit\_clear\_address} = \text{address} + 0x04000000$$
$$\text{bit\_set\_address} = \text{address} + 0x06000000$$

For bit set operations, bit locations that are 1 in the bit mask will be set in the destination register:

$$\text{register} = (\text{register OR mask})$$

For bit clear operations, bit locations that are 1 in the bit mask will be cleared in the destination register:

$$\text{register} = (\text{register AND (NOT mask)})$$

**Note:** It is possible to combine bit clear and bit set operations in order to arbitrarily modify multi-bit register fields, without affecting other fields in the same register. In this case, care should be taken to ensure that the field does not have intermediate values that can lead to erroneous behavior. For example, if bit clear and bit set operations are used to change an analog tuning register field from 25 to 26, the field would initially take on a value of zero. If the analog module is active at the time, this could lead to undesired behavior.

The peripherals listed in [Table 4.1 Peripherals that Do Not Support Bit Set and Bit Clear on page 49](#) do not support Bit Access for any registers. All other peripherals do support Bit Access, however, there may be cases of certain registers that do not support it. Such registers have a note regarding this lack of support.

**Table 4.1. Peripherals that Do Not Support Bit Set and Bit Clear**

| Module    |
|-----------|
| EMU       |
| RMU       |
| CRYOTIMER |
| TRNG0     |

#### 4.2.4 Peripherals

The peripherals are mapped into the peripheral memory segment, each with a fixed size address range according to [Table 4.2 Peripherals on page 50](#), [Table 4.3 Low Energy Peripherals on page 50](#), and [Table 4.4 Core Peripherals on page 51](#).

**Table 4.2. Peripherals**

| Address Range           | Module Name |
|-------------------------|-------------|
| 0x400E6000 - 0x400E6400 | PRS         |
| 0x40022000 - 0x40022400 | SMU         |
| 0x4001F000 - 0x4001F400 | CSEN        |
| 0x4001E000 - 0x4001E400 | CRYOTIMER   |
| 0x4001D000 - 0x4001D400 | TRNG0       |
| 0x4001C000 - 0x4001C400 | GPCRC       |
| 0x4001A000 - 0x4001A400 | WTIMER0     |
| 0x40018400 - 0x40018800 | TIMER1      |
| 0x40018000 - 0x40018400 | TIMER0      |
| 0x40010800 - 0x40010C00 | USART2      |
| 0x40010400 - 0x40010800 | USART1      |
| 0x40010000 - 0x40010400 | USART0      |
| 0x4000C400 - 0x4000C800 | I2C1        |
| 0x4000C000 - 0x4000C400 | I2C0        |
| 0x4000A000 - 0x4000B000 | GPIO        |
| 0x40008000 - 0x40008400 | VDAC0       |
| 0x40006000 - 0x40006400 | IDAC0       |
| 0x40002000 - 0x40002400 | ADC0        |
| 0x40000400 - 0x40000800 | ACMP1       |
| 0x40000000 - 0x40000400 | ACMP0       |

**Table 4.3. Low Energy Peripherals**

| Address Range           | Module Name |
|-------------------------|-------------|
| 0x40055000 - 0x40055400 | LESENSE     |
| 0x40052400 - 0x40052800 | WDOG1       |
| 0x40052000 - 0x40052400 | WDOG0       |
| 0x4004E000 - 0x4004E400 | PCNT0       |
| 0x4004A000 - 0x4004A400 | LEUART0     |
| 0x40046000 - 0x40046400 | LETIMER0    |
| 0x40042000 - 0x40042400 | RTCC        |

Table 4.4. Core Peripherals

| Address Range           | Module Name |
|-------------------------|-------------|
| 0xE0041000 - 0xE0081000 | ETM         |
| 0xE0000000 - 0xE0040000 | CM4         |
| 0x400F0400 - 0x400F0800 | CRYPTO1     |
| 0x400F0000 - 0x400F0400 | CRYPTO0     |
| 0x400E2000 - 0x400E3000 | LDMA        |
| 0x400E1000 - 0x400E1400 | FPUEH       |
| 0x400E0000 - 0x400E0800 | MSC         |

#### 4.2.5 Bus Matrix

The Bus Matrix connects the memory segments to the bus masters as detailed in [4.1 Introduction](#).

##### 4.2.5.1 Arbitration

The Bus Matrix uses a round-robin arbitration algorithm which enables high throughput and low latency, while starvation of simultaneous accesses to the same bus slave are eliminated. Round-robin does not assign a fixed priority to each bus master. The arbiter does not insert any bus wait-states during peak interaction. However, one wait state is inserted for master accesses occurring after a prolonged inactive time. This wait state allows for increased power efficiency during master idle time.

##### 4.2.5.2 Peripheral Access Performance

The Bus Matrix is a multi-layer energy optimized AMBA AHB compliant bus with an internal bandwidth of 5x a single AHB interface.

The Cortex-M4, DMA Controller, and peripherals (not peripherals in the low frequency clock domain) run on clocks which can be pre-scaled separately. Clocks and prescaling are described in more detail in [12. CMU - Clock Management Unit](#). This section describes the expected bus wait states for a peripheral based on its frequency relative to the HFCLK frequency. For this discussion, PERCLK refers to a selected peripheral's clock frequency, which is some integer division of the HFCLK frequency.

#### 4.2.5.2.1 WS0 Mode

In general, when accessing a peripheral, the latency in number of HFCLK cycles, not including master arbitration, is given by:

$$N_{\text{bus cycles}} = N_{\text{slave cycles}} \cdot f_{\text{HFCLK}}/f_{\text{PERCLK}}, \text{ best-case write accesses}$$

$$N_{\text{bus cycles}} = N_{\text{slave cycles}} \cdot f_{\text{HFCLK}}/f_{\text{PERCLK}} + 1, \text{ best-case read accesses}$$

$$N_{\text{bus cycles}} = (N_{\text{slave cycles}} + 1) \cdot f_{\text{HFCLK}}/f_{\text{PERCLK}} - 1, \text{ worst-case write accesses}$$

$$N_{\text{bus cycles}} = (N_{\text{slave cycles}} + 1) \cdot f_{\text{HFCLK}}/f_{\text{PERCLK}}, \text{ worst-case read accesses}$$

where  $N_{\text{slave cycles}}$  is the throughput of the slave's bus interface in number of PERCLK cycles per transfer, including any wait cycles introduced by the slave.

**Figure 4.4. Bus Access Latency (General Case)**

Note that a latency of **1** cycle corresponds to **0** wait states.

Additionally, for back-to-back accesses to the same peripheral, the throughput in number of cycles per transfer is given by:

$$N_{\text{bus cycles}} = N_{\text{slave cycles}} \cdot f_{\text{HFCLK}}/f_{\text{PERCLK}}, \text{ write accesses}$$

$$N_{\text{bus cycles}} = (N_{\text{slave cycles}} + 1) \cdot f_{\text{HFCLK}}/f_{\text{PERCLK}}, \text{ read accesses}$$

**Figure 4.5. Bus Access Throughput (Back-to-Back Transfers)**

Lastly, in the highest performing case, where PERCLK equals HFCLK and the slave does not introduce any additional wait states, the access latency in number of cycles is given by:

$$N_{\text{bus cycles}} = 1, \text{ write accesses}$$

$$N_{\text{bus cycles}} = 2, \text{ read accesses}$$

**Figure 4.6. Bus Access Latency (Max Performance)**

#### 4.2.5.2.2 WS1 Mode

In general, when accessing a peripheral, the latency in number of HFCLK cycles, not including master arbitration, is given by:

$$N_{\text{bus cycles}} = N_{\text{slave cycles}} \cdot f_{\text{HFCLK}}/f_{\text{PERCLK}} + 2, \text{ best-case write accesses}$$

$$N_{\text{bus cycles}} = N_{\text{slave cycles}} \cdot f_{\text{HFCLK}}/f_{\text{PERCLK}} + 1, \text{ best-case read accesses}$$

$$N_{\text{bus cycles}} = (N_{\text{slave cycles}} + 1) \cdot f_{\text{HFCLK}}/f_{\text{PERCLK}} + 1, \text{ worst-case write accesses}$$

$$N_{\text{bus cycles}} = (N_{\text{slave cycles}} + 1) \cdot f_{\text{HFCLK}}/f_{\text{PERCLK}}, \text{ worst-case read accesses}$$

where  $N_{\text{slave cycles}}$  is the throughput of the slave's bus interface in number of PERCLK cycles per transfer, including any wait cycles introduced by the slave.

**Figure 4.7. Bus Access Latency (General Case)**

Note that a latency of 1 cycle corresponds to 0 wait states.

Additionally, for back-to-back accesses to the same peripheral, the throughput in number of cycles per transfer is given by:

$$N_{\text{bus cycles}} = \max\{f_{\text{HFCLK}}/f_{\text{PERCLK}}, 2\} + N_{\text{slave cycles}} \cdot f_{\text{HFCLK}}/f_{\text{PERCLK}}, \text{ write accesses}$$

$$N_{\text{bus cycles}} = (N_{\text{slave cycles}} + 1) \cdot f_{\text{HFCLK}}/f_{\text{PERCLK}}, \text{ read accesses}$$

**Figure 4.8. Bus Access Throughput (Back-to-Back Transfers)**

Lastly, in the highest performing case, where PERCLK equals HFCLK and the slave does not introduce any additional wait states, the access latency in number of cycles is given by:

$$N_{\text{bus cycles}} = 3, \text{ write accesses}$$

$$N_{\text{bus cycles}} = 2, \text{ read accesses}$$

**Figure 4.9. Bus Access Latency (Max Performance)**

#### 4.2.5.2.3 Core Access Latency

Note that the cycle counts in the equations above is in terms of the HFCLK. When the core is prescaled from the bus clock, the core will see a reduced number of latency cycles given by:

$$N_{\text{core cycles}} = \text{ceiling}( N_{\text{bus cycles}} \cdot f_{\text{HFCORECLK}}/f_{\text{HFCLK}} )$$

where master arbitration is not included.

**Figure 4.10. Core Access Latency**

### 4.2.5.3 Bus Faults

System accesses from the core can receive a bus fault in the following condition(s):

- The core attempts to access an address that is not assigned to any peripheral or other system device. These faults can be enabled or disabled by setting the ADDRFAULTEN bit appropriately in MSC\_CTRL.
- The core attempts to access a peripheral or system device that has its clock disabled. These faults can be enabled or disabled by setting the CLKDISFAULTEN bit appropriately in MSC\_CTRL.
- The bus times out during an access. For example, this could happen while trying to synchronize volatile read data during an LE peripheral access. See [12.3.1.1 HFCLK - High Frequency Clock](#). These faults can be enabled or disabled by setting the TIMEOUT-FAULTEN bit appropriately in MSC\_CTRL.

In addition to any condition-specific bus fault control bits, the bus fault interrupt itself can be enabled or disabled in the same way as all other internal core interrupts.

**Note:** The icache flush is not triggered at the event of a bus fault. As a result, when an instruction fetch results in a bus fault, invalid data may be cached. This means that the next time the instruction that caused the bus fault is fetched, the processor core will get the invalid cached data without any bus fault. In order to avoid invalid cached data propagation to the processor core, software should manually invalidate cache by writing 1 to MSC\_CMD\_INVCACHE bitfield at the event of a bus fault.

## 4.3 Access to Low Energy Peripherals (Asynchronous Registers)

The Low Energy Peripherals are capable of running when the high frequency oscillator and core system is powered off, i.e. in energy mode EM2 Deep Sleep and in some cases also EM3 Stop. This enables the peripherals to perform tasks while the system energy consumption is minimal.

The Low Energy Peripherals are listed in [Table 4.3 Low Energy Peripherals on page 50](#).

All Low Energy Peripherals are memory mapped, with automatic data synchronization. Because the Low Energy Peripherals are running on clocks asynchronous to the high frequency system clock, there are some constraints on how register accesses are performed, as described in the following sections.

### 4.3.1 Writing

Every Low Energy Peripheral has one or more registers with data that needs to be synchronized into the Low Energy clock domain to maintain data consistency and predictable operation. There are two different synchronization mechanisms on the EFR32, immediate synchronization, and delayed synchronization. Immediate synchronization is available for the RTCC, LESENSE and LETIMER, and results in an immediate update of the target registers. Delayed synchronization is used for the remaining Low Energy Peripherals, and for these peripherals, a write operation requires 3 positive edges of the clock on the Low Energy Peripheral being accessed. Registers requiring synchronization are marked "Async Reg" in their description header.

**Note:** On the Gecko series of devices, all LE peripherals are subject to delayed synchronization.

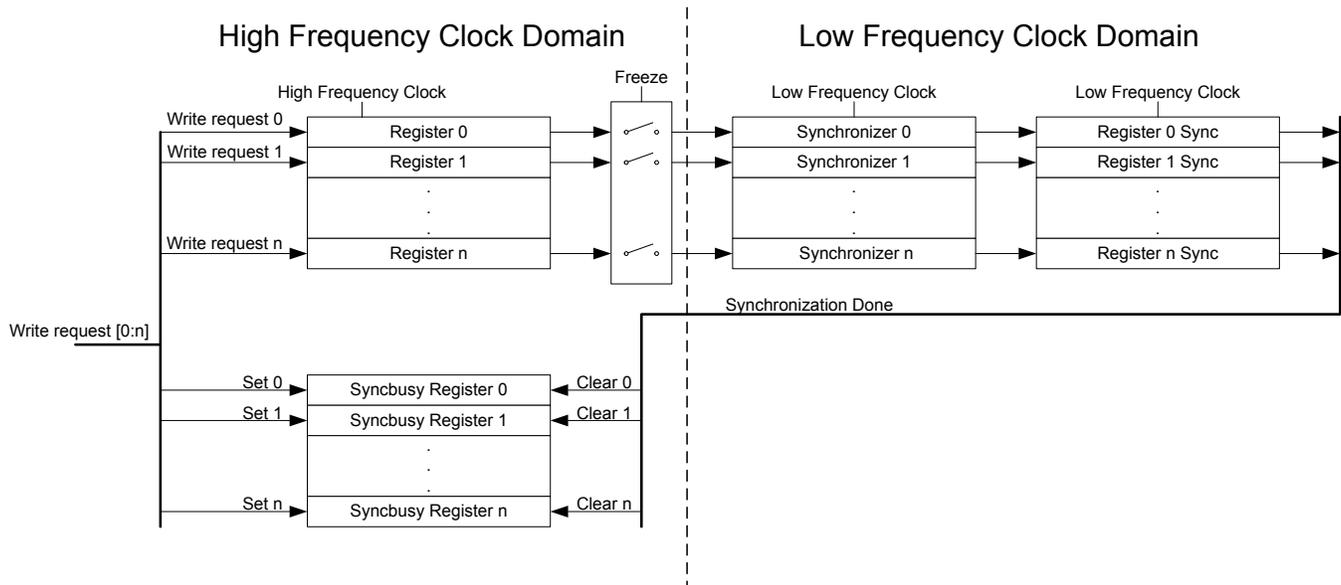


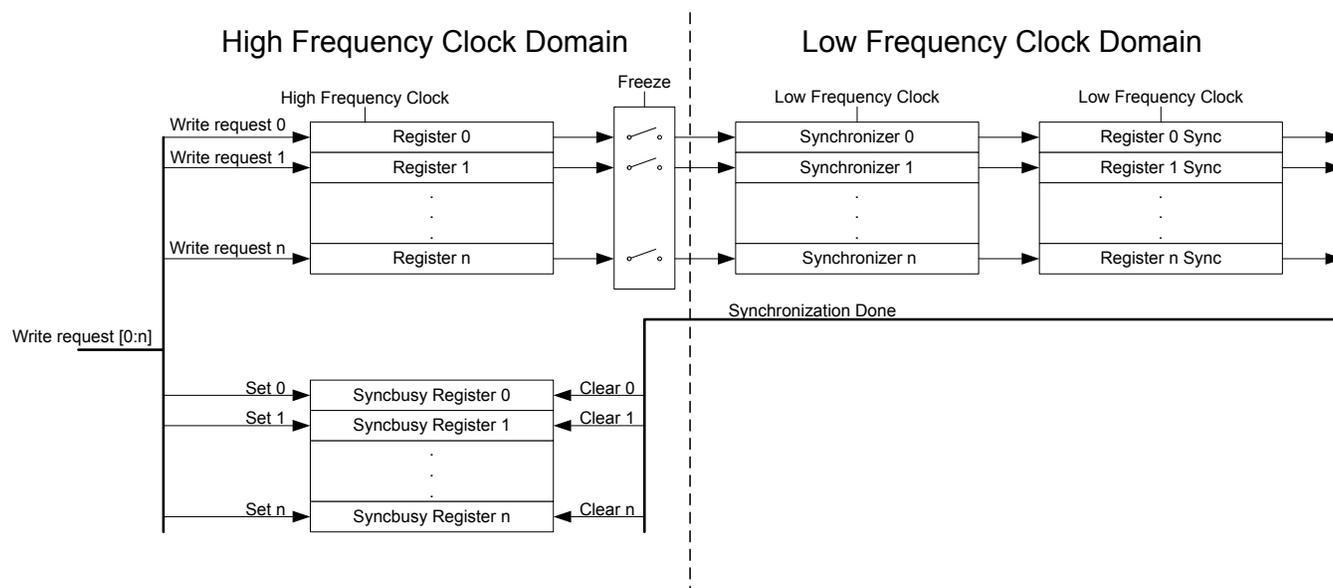
Figure 4.11. Write Operation to Low Energy Peripherals

### 4.3.1.1 Delayed Synchronization

After writing data to a register which value is to be synchronized into the Low Energy Peripheral using delayed synchronization, a corresponding busy flag in the <module\_name>\_SYNCBUSY register (e.g. LETIMER\_SYNCBUSY) is set. This flag is set as long as synchronization is in progress and is cleared upon completion.

**Note:** Subsequent writes to the same register before the corresponding busy flag is cleared is not supported. Write before the busy flag is cleared may result in undefined behavior. In general the SYNCBUSY register only needs to be observed if there is a risk of multiple write access to a register (which must be prevented). It is not required to wait until the relevant flag in the SYNCBUSY register is cleared after writing a register. E.g., EM2 Deep Sleep can be entered directly after writing a register.

See [Figure 4.12 Write Operation to Low Energy Peripherals](#) on page 56 for an overview of the writing mechanism operation.



**Figure 4.12. Write Operation to Low Energy Peripherals**

### 4.3.1.2 Immediate Synchronization

In contrast to the peripherals with delayed synchronization, peripherals with immediate synchronization do not experience a delay from a value is written to it takes effect in the peripheral. They are updated immediately on the peripheral write access. If such a write is done close to an edge on the clock of the peripheral, the write is delayed to after the clock edge. This will introduce wait-states on the peripheral access.

Peripherals with immediate synchronization each have a SYNCBUSY register. Commands written to a peripheral with immediate synchronization are not executed before the first peripheral clock after the write. In this period, the SYNCBUSY flag for the command register is set, indicating that the command has not yet been performed. Secondly, to maintain compatibility with the Gecko series, the rest of the SYNCBUSY registers are also present, but these are always 0, indicating that register writes are always safe.

**Note:** If compatibility with the Gecko series is a requirement for a given application, the rules that apply to delayed synchronization with respect to SYNCBUSY should also be followed for the peripherals that support immediate synchronization.

### 4.3.2 Reading

When reading from a Low Energy Peripheral, the data read is synchronized regardless if it originates in the Low Energy clock domain or High Frequency clock domain. See [Figure 4.13 Read Operation From Low Energy Peripherals on page 57](#) for an overview of the reading operation.

**Note:** Writing a register and then immediately reading the new value of the register may give the impression that the write operation is complete. This may not be the case. Refer to the SYNCBUSY register for correct status of the write operation to the Low Energy Peripheral.

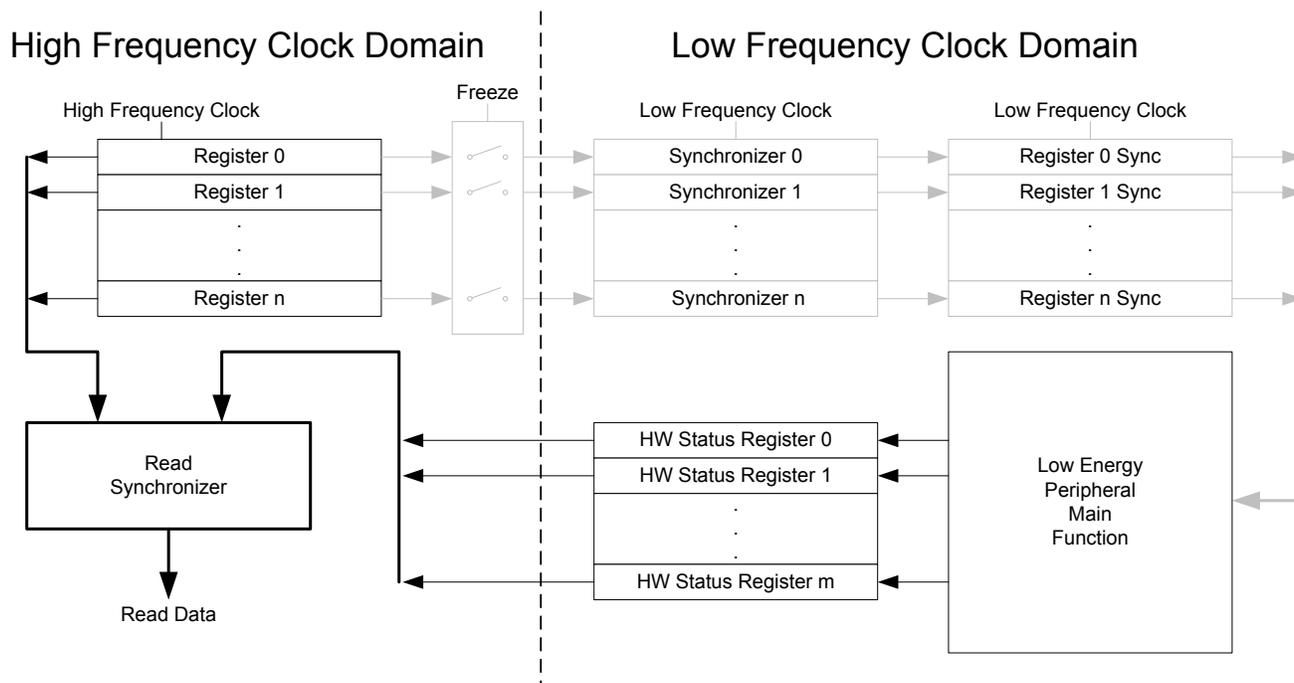


Figure 4.13. Read Operation From Low Energy Peripherals

### 4.3.3 FREEZE Register

In all Low Energy Peripheral with delayed synchronization there is a `<module_name>_FREEZE` register (e.g. `RTCC_FREEZE`). The register contains a bit named `REGFREEZE`. If precise control of the synchronization process is required, this bit may be utilized. When `REGFREEZE` is set, the synchronization process is halted allowing the software to write multiple Low Energy registers before starting the synchronization process, thus providing precise control of the module update process. The synchronization process is started by clearing the `REGFREEZE` bit.

**Note:** The FREEZE register is also present on peripherals with immediate synchronization, but there it has no effect

## 4.4 Flash

The Flash retains data in any state and typically stores the application code, special user data and security information. The Flash memory is typically programmed through the debug interface, but can also be erased and written to from software.

- Up to 512 KB of memory
- Page size of 2 KB (minimum erase unit)
- Minimum 10K erase cycles endurance
- Greater than 10 years data retention at 85 °C
- Lock-bits for memory protection
- Data retention in any state

## 4.5 SRAM

The primary task of the SRAM memory is to store application data. Additionally, it is possible to execute instructions from SRAM, and the DMA may be set up to transfer data between the SRAM, flash and peripherals.

- Up to 64 KB of memory
- Bit-band access support
- Set of RAM blocks may be powered down when not in use
- Data retention of the entire memory in EM0 Active to EM3 Stop

**Note:** The individual RAM sections may be smaller on some parts, however, the RAM AHB slaves maintain a contiguous address map. For example, if RAM0 is half-size on a part, then RAM1 is relocated to begin immediately after RAM0's last address. Using the provided software header files and linker scripts allows handling of this remapping in an autonomous manner.

## 4.6 DI Page Entry Map

The DI page contains production calibration data as well as device identification information. See the peripheral chapters for how each calibration value is to be used with the associated peripheral.

The offset address is relative to the start address of the DI page (see 8.3 Functional Description).

| Offset | Name          | Type | Description                                |
|--------|---------------|------|--|
| 0x000  | CAL           | RO   | CRC of DI-page and calibration temperature |
| 0x004  | MODULEINFO    | RO   | Module trace information                   |
| 0x008  | MODXOCAL      | RO   | Module Crystal Oscillator Calibration      |
| 0x020  | EXTINFO       | RO   | External Component description             |
| 0x028  | EUI48L        | RO   | EUI48 OUI and Unique identifier            |
| 0x02C  | EUI48H        | RO   | OUI  |
| 0x030  | CUSTOMINFO    | RO   | Custom information                         |
| 0x034  | MEMINFO       | RO   | Flash page size and misc. chip information |
| 0x040  | UNIQUEL       | RO   | Low 32 bits of device unique number        |
| 0x044  | UNIQUEH       | RO   | High 32 bits of device unique number       |
| 0x048  | MSIZE         | RO   | Flash and SRAM Memory size in kB           |
| 0x04C  | PART          | RO   | Part description                           |
| 0x050  | DEVINFOREV    | RO   | Device information page revision           |
| 0x054  | EMUTEMP       | RO   | EMU Temperature Calibration Information    |
| 0x060  | ADC0CAL0      | RO   | ADC0 calibration register 0                |
| 0x064  | ADC0CAL1      | RO   | ADC0 calibration register 1                |
| 0x068  | ADC0CAL2      | RO   | ADC0 calibration register 2                |
| 0x06C  | ADC0CAL3      | RO   | ADC0 calibration register 3                |
| 0x080  | HFRCOCAL0     | RO   | HFRCO Calibration Register (4 MHz)         |
| 0x08C  | HFRCOCAL3     | RO   | HFRCO Calibration Register (7 MHz)         |
| 0x098  | HFRCOCAL6     | RO   | HFRCO Calibration Register (13 MHz)        |
| 0x09C  | HFRCOCAL7     | RO   | HFRCO Calibration Register (16 MHz)        |
| 0x0A0  | HFRCOCAL8     | RO   | HFRCO Calibration Register (19 MHz)        |
| 0x0A8  | HFRCOCAL10    | RO   | HFRCO Calibration Register (26 MHz)        |
| 0x0AC  | HFRCOCAL11    | RO   | HFRCO Calibration Register (32 MHz)        |
| 0x0B0  | HFRCOCAL12    | RO   | HFRCO Calibration Register (38 MHz)        |
| 0x0E0  | AUXHFRCOCAL0  | RO   | AUXHFRCO Calibration Register (4 MHz)      |
| 0x0EC  | AUXHFRCOCAL3  | RO   | AUXHFRCO Calibration Register (7 MHz)      |
| 0x0F8  | AUXHFRCOCAL6  | RO   | AUXHFRCO Calibration Register (13 MHz)     |
| 0x0FC  | AUXHFRCOCAL7  | RO   | AUXHFRCO Calibration Register (16 MHz)     |
| 0x100  | AUXHFRCOCAL8  | RO   | AUXHFRCO Calibration Register (19 MHz)     |
| 0x108  | AUXHFRCOCAL10 | RO   | AUXHFRCO Calibration Register (26 MHz)     |
| 0x10C  | AUXHFRCOCAL11 | RO   | AUXHFRCO Calibration Register (32 MHz)     |

| Offset | Name            | Type | Description  |
|--------|-----------------|------|--|
| 0x110  | AUXHFRCOCAL12   | RO   | AUXHFRCO Calibration Register (38 MHz)                 |
| 0x140  | VMONCAL0        | RO   | VMON Calibration Register 0                            |
| 0x144  | VMONCAL1        | RO   | VMON Calibration Register 1                            |
| 0x148  | VMONCAL2        | RO   | VMON Calibration Register 2                            |
| 0x158  | IDAC0CAL0       | RO   | IDAC0 Calibration Register 0                           |
| 0x15C  | IDAC0CAL1       | RO   | IDAC0 Calibration Register 1                           |
| 0x168  | DCDCLNVCTRL0    | RO   | DCDC Low-noise VREF Trim Register 0                    |
| 0x16C  | DCDCLPVCTRL0    | RO   | DCDC Low-power VREF Trim Register 0                    |
| 0x170  | DCDCLPVCTRL1    | RO   | DCDC Low-power VREF Trim Register 1                    |
| 0x174  | DCDCLPVCTRL2    | RO   | DCDC Low-power VREF Trim Register 2                    |
| 0x178  | DCDCLPVCTRL3    | RO   | DCDC Low-power VREF Trim Register 3                    |
| 0x17C  | DCDCLPCMPHYSEL0 | RO   | DCDC LPCMPHYSEL Trim Register 0                        |
| 0x180  | DCDCLPCMPHYSEL1 | RO   | DCDC LPCMPHYSEL Trim Register 1                        |
| 0x184  | VDAC0MAINCAL    | RO   | VDAC0 Cals for Main Path                               |
| 0x188  | VDAC0ALTCAL     | RO   | VDAC0 Cals for Alternate Path                          |
| 0x18C  | VDAC0CH1CAL     | RO   | VDAC0 CH1 Error Cal                                    |
| 0x190  | OPA0CAL0        | RO   | OPA0 Calibration Register for DRIVESTRENGTH 0, INCBW=1 |
| 0x194  | OPA0CAL1        | RO   | OPA0 Calibration Register for DRIVESTRENGTH 1, INCBW=1 |
| 0x198  | OPA0CAL2        | RO   | OPA0 Calibration Register for DRIVESTRENGTH 2, INCBW=1 |
| 0x19C  | OPA0CAL3        | RO   | OPA0 Calibration Register for DRIVESTRENGTH 3, INCBW=1 |
| 0x1A0  | OPA1CAL0        | RO   | OPA1 Calibration Register for DRIVESTRENGTH 0, INCBW=1 |
| 0x1A4  | OPA1CAL1        | RO   | OPA1 Calibration Register for DRIVESTRENGTH 1, INCBW=1 |
| 0x1A8  | OPA1CAL2        | RO   | OPA1 Calibration Register for DRIVESTRENGTH 2, INCBW=1 |
| 0x1AC  | OPA1CAL3        | RO   | OPA1 Calibration Register for DRIVESTRENGTH 3, INCBW=1 |
| 0x1B0  | OPA2CAL0        | RO   | OPA2 Calibration Register for DRIVESTRENGTH 0, INCBW=1 |
| 0x1B4  | OPA2CAL1        | RO   | OPA2 Calibration Register for DRIVESTRENGTH 1, INCBW=1 |
| 0x1B8  | OPA2CAL2        | RO   | OPA2 Calibration Register for DRIVESTRENGTH 2, INCBW=1 |
| 0x1BC  | OPA2CAL3        | RO   | OPA2 Calibration Register for DRIVESTRENGTH 3, INCBW=1 |
| 0x1C0  | CSENGAINCAL     | RO   | Cap Sense Gain Adjustment                              |
| 0x1D0  | OPA0CAL4        | RO   | OPA0 Calibration Register for DRIVESTRENGTH 0, INCBW=0 |
| 0x1D4  | OPA0CAL5        | RO   | OPA0 Calibration Register for DRIVESTRENGTH 1, INCBW=0 |
| 0x1D8  | OPA0CAL6        | RO   | OPA0 Calibration Register for DRIVESTRENGTH 2, INCBW=0 |
| 0x1DC  | OPA0CAL7        | RO   | OPA0 Calibration Register for DRIVESTRENGTH 3, INCBW=0 |
| 0x1E0  | OPA1CAL4        | RO   | OPA1 Calibration Register for DRIVESTRENGTH 0, INCBW=0 |
| 0x1E4  | OPA1CAL5        | RO   | OPA1 Calibration Register for DRIVESTRENGTH 1, INCBW=0 |
| 0x1E8  | OPA1CAL6        | RO   | OPA1 Calibration Register for DRIVESTRENGTH 2, INCBW=0 |
| 0x1EC  | OPA1CAL7        | RO   | OPA1 Calibration Register for DRIVESTRENGTH 3, INCBW=0 |

| Offset | Name     | Type | Description  |
|--------|----------|------|--|
| 0x1F0  | OPA2CAL4 | RO   | OPA2 Calibration Register for DRIVESTRENGTH 0, INCBW=0 |
| 0x1F4  | OPA2CAL5 | RO   | OPA2 Calibration Register for DRIVESTRENGTH 1, INCBW=0 |
| 0x1F8  | OPA2CAL6 | RO   | OPA2 Calibration Register for DRIVESTRENGTH 2, INCBW=0 |
| 0x1FC  | OPA2CAL7 | RO   | OPA2 Calibration Register for DRIVESTRENGTH 3, INCBW=0 |

## 4.7 DI Page Entry Description

### 4.7.1 CAL - CRC of DI-page and calibration temperature

| Offset        | Bit Position |    |    |    |    |    |    |    |      |    |    |    |    |    |    |    |     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|------|----|----|----|----|----|----|----|-----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x000         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15  | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Access</b> |              |    |    |    |    |    |    |    | RO   |    |    |    |    |    |    |    | RO  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    | TEMP |    |    |    |    |    |    |    | CRC |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name            | Access                         | Description  |
|-------|-----------------|--------------------------------|--|
| 31:24 | <i>Reserved</i> | <i>Reserved for future use</i> |  |
| 23:16 | TEMP            | RO                             | Calibration temperature as an unsigned int in DegC (25 = 25DegC) |
| 15:0  | CRC             | RO                             | CRC of DI-page (CRC-16-CCITT)                                    |

## 4.7.2 MODULEINFO - Module trace information

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |            |            |         |      |      |           |    |    |    |    |   |         |       |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|------------|------------|---------|------|------|-----------|----|----|----|----|---|---------|-------|---|---|---|---|---|---|---|
| 0x004  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19         | 18         | 17      | 16   | 15   | 14        | 13 | 12 | 11 | 10 | 9 | 8       | 7     | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO           |    |    |    |    |    |    |    |    |    |    |    | RO         | RO         | RO      | RO   | RO   | RO        |    |    |    |    |   | RO      | RO    |   |   |   |   |   |   |   |
| Name   | RESERVED1    |    |    |    |    |    |    |    |    |    |    |    | HFXOCALVAL | LFXOCALVAL | EXPRESS | LFXO | TYPE | MODNUMBER |    |    |    |    |   | ANTENNA | HWREV |   |   |   |   |   |   |   |

| Bit   | Name       | Access    | Description                         |
|-------|------------|-----------|-------------------------------------|
| 31:20 | RESERVED1  | RO        | Reserved for future use             |
| 19    | HFXOCALVAL | RO        | HFXO Calibration Valid              |
|       | Value      | Mode      | Description                         |
|       | 0          | VALID     | XOCAL_HFXOCTUNE is valid            |
|       | 1          | NOTVALID  | XOCAL_HFXOCTUNE is not valid        |
| 18    | LFXOCALVAL | RO        | LFXO Calibration Valid              |
|       | Value      | Mode      | Description                         |
|       | 0          | VALID     | XOCAL_LFXOTUNING is valid           |
|       | 1          | NOTVALID  | XOCAL_LFXOTUNING is not valid       |
| 17    | EXPRESS    | RO        | Blue Gecko Express                  |
|       | Value      | Mode      | Description                         |
|       | 0          | SUPPORTED | Blue Gecko Express is supported     |
|       | 1          | NONE      | Blue Gecko Express is not supported |
| 16    | LFXO       | RO        | Module has LFXO                     |
|       | Value      | Mode      | Description                         |
|       | 0          | NONE      | LFXO is not installed               |
|       | 1          | PRESENT   | LFXO is installed                   |
| 15    | TYPE       | RO        | Module Type                         |
|       | Value      | Mode      | Description                         |
|       | 0          | PCB       | PCB                                 |
|       | 1          | SIP       | SIP                                 |

| Bit  | Name      | Access    | Description   |
|------|-----------|-----------|---|
| 14:8 | MODNUMBER | RO        | Module Numbers, indicates radio performance and frequency band. |
| 7:5  | ANTENNA   | RO        | Module Antenna Type   |
|      | Value     | Mode      | Description   |
|      | 0         | BUILTIN   | Built-in Antenna  |
|      | 1         | CONNECTOR | RF Connector  |
|      | 2         | RFPAD     | RF Pad  |
| 4:0  | HWREV     | RO        | Module Hardware Revision. Starting from 0.                      |

#### 4.7.3 MODXOCAL - Module Crystal Oscillator Calibration

| Offset | Bit Position |    |    |    |    |    |    |    |           |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x008  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO           |    |    |    |    |    |    |    | RO        |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Name   | LFXOTUNING   |    |    |    |    |    |    |    | HFXOCTUNE |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name       | Access | Description                 |
|------|------------|--------|-----------------------------|
| 15:9 | LFXOTUNING | RO     | Calibration for LFXO TUNING |
| 8:0  | HFXOCTUNE  | RO     | Calibration for HFXO CTUNE  |

## 4.7.4 EXTINFO - External Component description

| Offset | Bit Position |    |    |    |    |    |    |    |     |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |      |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|-----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|------|---|---|---|---|---|---|---|
| 0x020  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access |              |    |    |    |    |    |    |    | RO  |    |    |    |    |    |    |    | RO         |    |    |    |    |    |   |   | RO   |   |   |   |   |   |   |   |
| Name   |              |    |    |    |    |    |    |    | REV |    |    |    |    |    |    |    | CONNECTION |    |    |    |    |    |   |   | TYPE |   |   |   |   |   |   |   |

| Bit   | Name            | Access     | Description   |
|-------|-----------------|------------|---|
| 31:24 | <i>Reserved</i> |            | <i>Reserved for future use</i>                          |
| 23:16 | REV             | RO         | MCM Revision. Refer to MODULEINFO instead, if available |
|       | Value           | Mode       | Description   |
|       | 1               | REV1       | Revision 1  |
|       | 255             | NONE       | No external component present                           |
| 15:8  | CONNECTION      | RO         | Connection protocol to external component               |
|       | Value           | Mode       | Description   |
|       | 1               | SPI        | SPI control interface                                   |
|       | 2               | SDIO       | SDIO interface  |
|       | 255             | NONE       | None  |
| 7:0   | TYPE            | RO         | External Component. Additional IC installed in module   |
|       | Value           | Mode       | Description   |
|       | 1               | IS25LQ040B | IS25LQ040B-JWLE1 512kB Serial Flash                     |
|       | 2               | AT25S041   | AT25S041-DWFHT 512kB Serial Flash                       |
|       | 3               | WF200      | WF200 802.11bgn WiFi NCP                                |
|       | 255             | NONE       | None  |

## 4.7.5 EUI48L - EUI48 OUI and Unique identifier

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x028         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Access</b> | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RO       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | OUI48L       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | UNIQUEID |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Access | Description   |
|-------|----------|--------|---|
| 31:24 | OUI48L   | RO     | Lower Octet of EUI48 Organizationally Unique Identifier |
| 23:0  | UNIQUEID | RO     | Unique identifier                                       |

## 4.7.6 EUI48H - OUI

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x02C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RO     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | OUI48H |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name            | Access | Description  |
|-------|-----------------|--------|--|
| 31:16 | <i>Reserved</i> |        | <i>Reserved for future use</i>                               |
| 15:0  | OUI48H          | RO     | Upper two Octets of EUI48 Organizationally Unique Identifier |

## 4.7.7 CUSTOMINFO - Custom information

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x030         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Access</b> | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | PARTNO       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name            | Access | Description  |
|-------|-----------------|--------|--|
| 31:16 | PARTNO          | RO     | Custom part identifier as unsigned integer (e.g. 903) 65535 for standard product |
| 15:0  | <i>Reserved</i> |        | <i>Reserved for future use</i>   |

## 4.7.8 MEMINFO - Flash page size and misc. chip information

| Offset | Bit Position    |    |    |    |    |    |    |    |          |    |    |    |    |    |    |    |         |    |    |    |    |    |   |   |           |   |   |   |   |   |   |   |
|--------|-----------------|----|----|----|----|----|----|----|----------|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|-----------|---|---|---|---|---|---|---|
| 0x034  | 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO              |    |    |    |    |    |    |    | RO       |    |    |    |    |    |    |    | RO      |    |    |    |    |    |   |   | RO        |   |   |   |   |   |   |   |
| Name   | FLASH_PAGE_SIZE |    |    |    |    |    |    |    | PINCOUNT |    |    |    |    |    |    |    | PKGTYPE |    |    |    |    |    |   |   | TEMPGRADE |   |   |   |   |   |   |   |

| Bit   | Name            | Access   | Description  |
|-------|-----------------|----------|--|
| 31:24 | FLASH_PAGE_SIZE | RO       | Flash page size in bytes coded as $2^{\text{((MEM\_INFO\_PAGE\_SIZE + 10) \& 0xFF)}}$ . I.e. the value 0xFF = 512 bytes. |
| 23:16 | PINCOUNT        | RO       | Device pin count as unsigned integer (eg. 48)  |
| 15:8  | PKGTYPE         | RO       | Package Identifier as character  |
|       | Value           | Mode     | Description  |
|       | 74              | WLCSP    | WLCSP package  |
|       | 76              | BGA      | BGA package  |
|       | 77              | QFN      | QFN package  |
|       | 81              | QFP      | QFP package  |
| 7:0   | TEMPGRADE       | RO       | Temperature Grade of product as unsigned integer enumeration   |
|       | Value           | Mode     | Description  |
|       | 0               | N40TO85  | -40 to 85degC  |
|       | 1               | N40TO125 | -40 to 125degC   |
|       | 2               | N40TO105 | -40 to 105degC   |
|       | 3               | N0TO70   | 0 to 70degC  |

## 4.7.9 UNIQUEL - Low 32 bits of device unique number

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x040  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Name   | UNIQUEL      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name    | Access | Description                         |
|------|---------|--------|-------------------------------------|
| 31:0 | UNIQUEL | RO     | Low 32 bits of device unique number |

## 4.7.10 UNIQUEH - High 32 bits of device unique number

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x044  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Name   | UNIQUEH      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name    | Access | Description                          |
|------|---------|--------|--------------------------------------|
| 31:0 | UNIQUEH | RO     | High 32 bits of device unique number |

## 4.7.11 MSIZE - Flash and SRAM Memory size in kB

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x048  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15    | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RO    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Name   | SRAM         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | FLASH |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name  | Access | Description   |
|-------|-------|--------|---|
| 31:16 | SRAM  | RO     | Ram size, kbyte count as unsigned integer (eg. 16)    |
| 15:0  | FLASH | RO     | Flash size, kbyte count as unsigned integer (eg. 128) |

## 4.7.12 PART - Part description

| Offset | Bit Position |    |    |    |    |    |    |    |               |    |    |    |    |    |    |    |               |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x04C  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO           |    |    |    |    |    |    |    | RO            |    |    |    |    |    |    |    | RO            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Name   | PROD_REV     |    |    |    |    |    |    |    | DEVICE_FAMILY |    |    |    |    |    |    |    | DEVICE_NUMBER |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name          | Access     | Description  |
|-------|---------------|------------|--|
| 31:24 | PROD_REV      | RO         | Production revision as unsigned integer            |
| 23:16 | DEVICE_FAMILY | RO         | Device Family                                      |
|       | Value         | Mode       | Description  |
|       | 16            | EFR32MG1P  | EFR32 Mighty Gecko Family Series 1 Device Config 1 |
|       | 17            | EFR32MG1B  | EFR32 Mighty Gecko Family Series 1 Device Config 1 |
|       | 18            | EFR32MG1V  | EFR32 Mighty Gecko Family Series 1 Device Config 1 |
|       | 19            | EFR32BG1P  | EFR32 Blue Gecko Family Series 1 Device Config 1   |
|       | 20            | EFR32BG1B  | EFR32 Blue Gecko Family Series 1 Device Config 1   |
|       | 21            | EFR32BG1V  | EFR32 Blue Gecko Family Series 1 Device Config 1   |
|       | 25            | EFR32FG1P  | EFR32 Flex Gecko Family Series 1 Device Config 1   |
|       | 26            | EFR32FG1B  | EFR32 Flex Gecko Family Series 1 Device Config 1   |
|       | 27            | EFR32FG1V  | EFR32 Flex Gecko Family Series 1 Device Config 1   |
|       | 28            | EFR32MG12P | EFR32 Mighty Gecko Family Series 1 Device Config 2 |
|       | 29            | EFR32MG12B | EFR32 Mighty Gecko Family Series 1 Device Config 2 |
|       | 30            | EFR32MG12V | EFR32 Mighty Gecko Family Series 1 Device Config 2 |
|       | 31            | EFR32BG12P | EFR32 Blue Gecko Family Series 1 Device Config 2   |
|       | 32            | EFR32BG12B | EFR32 Blue Gecko Family Series 1 Device Config 2   |
|       | 33            | EFR32BG12V | EFR32 Blue Gecko Family Series 1 Device Config 2   |
|       | 37            | EFR32FG12P | EFR32 Flex Gecko Family Series 1 Device Config 2   |
|       | 38            | EFR32FG12B | EFR32 Flex Gecko Family Series 1 Device Config 2   |
|       | 39            | EFR32FG12V | EFR32 Flex Gecko Family Series 1 Device Config 2   |
|       | 40            | EFR32MG13P | EFR32 Mighty Gecko Family Series 1 Device Config 3 |
|       | 41            | EFR32MG13B | EFR32 Mighty Gecko Family Series 1 Device Config 3 |
|       | 42            | EFR32MG13V | EFR32 Mighty Gecko Family Series 1 Device Config 3 |
|       | 43            | EFR32BG13P | EFR32 Blue Gecko Family Series 1 Device Config 3   |
|       | 44            | EFR32BG13B | EFR32 Blue Gecko Family Series 1 Device Config 3   |

| Bit | Name | Access     | Description  |
|-----|------|------------|--|
| 45  |      | EFR32BG13V | EFR32 Blue Gecko Family Series 1 Device Config 3   |
| 46  |      | EFR32ZG13P | EFR32 Zen Gecko Family Series 1 Device Config 3    |
| 49  |      | EFR32FG13P | EFR32 Flex Gecko Family Series 1 Device Config 3   |
| 50  |      | EFR32FG13B | EFR32 Flex Gecko Family Series 1 Device Config 3   |
| 51  |      | EFR32FG13V | EFR32 Flex Gecko Family Series 1 Device Config 3   |
| 52  |      | EFR32MG14P | EFR32 Mighty Gecko Family Series 1 Device Config 4 |
| 53  |      | EFR32MG14B | EFR32 Mighty Gecko Family Series 1 Device Config 4 |
| 54  |      | EFR32MG14V | EFR32 Mighty Gecko Family Series 1 Device Config 4 |
| 55  |      | EFR32BG14P | EFR32 Blue Gecko Family Series 1 Device Config 4   |
| 56  |      | EFR32BG14B | EFR32 Blue Gecko Family Series 1 Device Config 4   |
| 57  |      | EFR32BG14V | EFR32 Blue Gecko Family Series 1 Device Config 4   |
| 58  |      | EFR32ZG14P | EFR32 Zen Gecko Family Series 1 Device Config 4    |
| 61  |      | EFR32FG14P | EFR32 Flex Gecko Family Series 1 Device Config 4   |
| 62  |      | EFR32FG14B | EFR32 Flex Gecko Family Series 1 Device Config 4   |
| 63  |      | EFR32FG14V | EFR32 Flex Gecko Family Series 1 Device Config 4   |
| 71  |      | EFM32G     | EFM32 Gecko Device Family                          |
| 71  |      | G          | EFM32 Gecko Device Family                          |
| 72  |      | EFM32GG    | EFM32 Giant Gecko Device Family                    |
| 72  |      | GG         | EFM32 Giant Gecko Device Family                    |
| 73  |      | TG         | EFM32 Tiny Gecko Device Family                     |
| 73  |      | EFM32TG    | EFM32 Tiny Gecko Device Family                     |
| 74  |      | EFM32LG    | EFM32 Leopard Gecko Device Family                  |
| 74  |      | LG         | EFM32 Leopard Gecko Device Family                  |
| 75  |      | EFM32WG    | EFM32 Wonder Gecko Device Family                   |
| 75  |      | WG         | EFM32 Wonder Gecko Device Family                   |
| 76  |      | ZG         | EFM32 Zero Gecko Device Family                     |
| 76  |      | EFM32ZG    | EFM32 Zero Gecko Device Family                     |
| 77  |      | HG         | EFM32 Happy Gecko Device Family                    |
| 77  |      | EFM32HG    | EFM32 Happy Gecko Device Family                    |
| 81  |      | EFM32PG1B  | EFM32 Pearl Gecko Family Series 1 Device Config 1  |
| 83  |      | EFM32JG1B  | EFM32 Jade Gecko Family Series 1 Device Config 1   |
| 85  |      | EFM32PG12B | EFM32 Pearl Gecko Family Series 1 Device Config 2  |
| 87  |      | EFM32JG12B | EFM32 Jade Gecko Family Series 1 Device Config 2   |
| 100 |      | EFM32GG11B | EFM32 Giant Gecko Family Series 1 Device Config 1  |
| 103 |      | EFM32TG11B | EFM32 Tiny Gecko Family Series 1 Device Config 1   |
| 106 |      | EFM32GG12B | EFM32 Giant Gecko Family Series 1 Device Config 2  |
| 120 |      | EZR32LG    | EZR32 Leopard Gecko Device Family                  |

| Bit  | Name          | Access  | Description  |
|------|---------------|---------|--|
|      | 121           | EZR32WG | EZR32 Wonder Gecko Device Family                                       |
|      | 122           | EZR32HG | EZR32 Happy Gecko Device Family  |
| 15:0 | DEVICE_NUMBER | RO      | Part number as unsigned integer (e.g. 233 for EFR32BG1P233F256GM48-B0) |

#### 4.7.13 DEVINFOREV - Device information page revision

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |            |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|------------|---|---|---|---|---|---|---|
| 0x050  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RO         |   |   |   |   |   |   |   |
| Name   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | DEVINFOREV |   |   |   |   |   |   |   |

| Bit  | Name            | Access                         | Description   |
|------|-----------------|--------------------------------|---|
| 31:8 | <i>Reserved</i> | <i>Reserved for future use</i> |   |
| 7:0  | DEVINFOREV      | RO                             | DEVINFO layout revision as unsigned integer (initially 1) |

#### 4.7.14 EMUTEMP - EMU Temperature Calibration Information

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |             |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|-------------|---|---|---|---|---|---|---|
| 0x054  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RO          |   |   |   |   |   |   |   |
| Name   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | EMUTEMPROOM |   |   |   |   |   |   |   |

| Bit  | Name            | Access                         | Description                          |
|------|-----------------|--------------------------------|--------------------------------------|
| 31:8 | <i>Reserved</i> | <i>Reserved for future use</i> |                                      |
| 7:0  | EMUTEMPROOM     | RO                             | EMU_TEMP temperature reading at room |

## 4.7.15 ADC0CAL0 - ADC0 calibration register 0

| Offset | Bit Position |    |    |    |         |    |    |    |    |                |    |    |    |           |    |    |    |    |    |    |          |    |   |   |   |   |                 |   |   |   |   |   |            |
|--------|--------------|----|----|----|---------|----|----|----|----|----------------|----|----|----|-----------|----|----|----|----|----|----|----------|----|---|---|---|---|-----------------|---|---|---|---|---|------------|
| 0x060  | 31           | 30 | 29 | 28 | 27      | 26 | 25 | 24 | 23 | 22             | 21 | 20 | 19 | 18        | 17 | 16 | 15 | 14 | 13 | 12 | 11       | 10 | 9 | 8 | 7 | 6 | 5               | 4 | 3 | 2 | 1 | 0 |            |
| Access |              |    |    |    | RO      |    |    |    |    | RO             |    |    |    | RO        |    |    |    |    |    |    | RO       |    |   |   |   |   | RO              |   |   |   |   |   |            |
| Name   |              |    |    |    | GAIN2V5 |    |    |    |    | NEGSEOFFSET2V5 |    |    |    | OFFSET2V5 |    |    |    |    |    |    | GAIN1V25 |    |   |   |   |   | NEGSEOFFSET1V25 |   |   |   |   |   | OFFSET1V25 |

| Bit   | Name            | Access                         | Description                                      |
|-------|-----------------|--------------------------------|--|
| 31    | <i>Reserved</i> | <i>Reserved for future use</i> |  |
| 30:24 | GAIN2V5         | RO                             | Gain for 2.5V reference                          |
| 23:20 | NEGSEOFFSET2V5  | RO                             | Negative single ended offset for 2.5V reference  |
| 19:16 | OFFSET2V5       | RO                             | Offset for 2.5V reference                        |
| 15    | <i>Reserved</i> | <i>Reserved for future use</i> |  |
| 14:8  | GAIN1V25        | RO                             | Gain for 1.25V reference                         |
| 7:4   | NEGSEOFFSET1V25 | RO                             | Negative single ended offset for 1.25V reference |
| 3:0   | OFFSET1V25      | RO                             | Offset for 1.25V reference                       |

## 4.7.16 ADC0CAL1 - ADC0 calibration register 1

| Offset | Bit Position |    |    |    |            |    |    |    |    |                   |    |    |    |              |    |    |    |    |    |    |         |    |   |   |   |   |                |   |   |   |   |           |    |
|--------|--------------|----|----|----|------------|----|----|----|----|-------------------|----|----|----|--------------|----|----|----|----|----|----|---------|----|---|---|---|---|----------------|---|---|---|---|-----------|----|
| 0x064  | 31           | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22                | 21 | 20 | 19 | 18           | 17 | 16 | 15 | 14 | 13 | 12 | 11      | 10 | 9 | 8 | 7 | 6 | 5              | 4 | 3 | 2 | 1 | 0         |    |
| Access |              |    |    |    | RO         |    |    |    |    | RO                |    |    |    | RO           |    |    |    |    |    |    | RO      |    |   |   |   |   | RO             |   |   |   |   |           | RO |
| Name   |              |    |    |    | GAIN5VDIFF |    |    |    |    | NEGSEOFFSET5VDIFF |    |    |    | OFFSET5VDIFF |    |    |    |    |    |    | GAINVDD |    |   |   |   |   | NEGSEOFFSETVDD |   |   |   |   | OFFSETVDD |    |

| Bit   | Name              | Access                         | Description   |
|-------|-------------------|--------------------------------|---|
| 31    | <i>Reserved</i>   | <i>Reserved for future use</i> |   |
| 30:24 | GAIN5VDIFF        | RO                             | Gain for for 5V differential reference                          |
| 23:20 | NEGSEOFFSET5VDIFF | RO                             | Negative single ended offset with for 5V differential reference |
| 19:16 | OFFSET5VDIFF      | RO                             | Offset for 5V differential reference                            |
| 15    | <i>Reserved</i>   | <i>Reserved for future use</i> |   |
| 14:8  | GAINVDD           | RO                             | Gain for VDD reference  |
| 7:4   | NEGSEOFFSETVDD    | RO                             | Negative single ended offset for VDD reference                  |
| 3:0   | OFFSETVDD         | RO                             | Offset for VDD reference  |

## 4.7.17 ADC0CAL2 - ADC0 calibration register 2

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                  |    |    |    |    |    |   |   |   |   |             |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------|----|----|----|----|----|---|---|---|---|-------------|---|---|---|---|---|
| 0x068  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15               | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5           | 4 | 3 | 2 | 1 | 0 |
| Access |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RO               |    |    |    |    |    |   |   |   |   | RO          |   |   |   |   |   |
| Name   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | NEGSEOFFSET2XVDD |    |    |    |    |    |   |   |   |   | OFFSET2XVDD |   |   |   |   |   |

| Bit   | Name             | Access | Description                                      |
|-------|------------------|--------|--|
| 31    | Reserved         |        | Reserved for future use                          |
| 30:24 | Reserved         |        | Reserved for future use                          |
| 23:20 | Reserved         |        | Reserved for future use                          |
| 19:16 | Reserved         |        | Reserved for future use                          |
| 15:8  | Reserved         |        | Reserved for future use                          |
| 7:4   | NEGSEOFFSET2XVDD | RO     | Negative single ended offset for 2XVDD reference |
| 3:0   | OFFSET2XVDD      | RO     | Offset for 2XVDD reference                       |

## 4.7.18 ADC0CAL3 - ADC0 calibration register 3

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |              |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x06C  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15           | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RO           |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Name   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | TEMPREAD1V25 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name         | Access | Description                           |
|-------|--------------|--------|---------------------------------------|
| 31:16 | Reserved     |        | Reserved for future use               |
| 15:4  | TEMPREAD1V25 | RO     | Temperature reading at 1V25 reference |
| 3:0   | Reserved     |        | Reserved for future use               |

## 4.7.19 HFRCOAL0 - HFRCO Calibration Register (4 MHz)

| Offset | Bit Position |    |    |    |              |        |    |       |         |    |    |           |    |    |    |    |    |            |    |    |    |    |   |        |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|--------------|--------|----|-------|---------|----|----|-----------|----|----|----|----|----|------------|----|----|----|----|---|--------|---|---|---|---|---|---|---|---|
| 0x080  | 31           | 30 | 29 | 28 | 27           | 26     | 25 | 24    | 23      | 22 | 21 | 20        | 19 | 18 | 17 | 16 | 15 | 14         | 13 | 12 | 11 | 10 | 9 | 8      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO           |    |    |    | RO           | RO     |    | RO    | RO      |    |    | RO        |    |    |    |    |    | RO         |    |    |    |    |   | RO     |   |   |   |   |   |   |   |   |
| Name   | VREFTC       |    |    |    | FINETUNINGEN | CLKDIV |    | LDOHP | CMPBIAS |    |    | FREQRANGE |    |    |    |    |    | FINETUNING |    |    |    |    |   | TUNING |   |   |   |   |   |   |   |   |

| Bit   | Name            | Access | Description  |
|-------|-----------------|--------|--|
| 31:28 | VREFTC          | RO     | HFRCO Temperature Coefficient Trim on Comparator Reference |
| 27    | FINETUNINGEN    | RO     | HFRCO enable reference for fine tuning                     |
| 26:25 | CLKDIV          | RO     | HFRCO Clock Output Divide                                  |
| 24    | LDOHP           | RO     | HFRCO LDO High Power Mode                                  |
| 23:21 | CMPBIAS         | RO     | HFRCO Comparator Bias Current                              |
| 20:16 | FREQRANGE       | RO     | HFRCO Frequency Range                                      |
| 15:14 | <i>Reserved</i> |        | <i>Reserved for future use</i>                             |
| 13:8  | FINETUNING      | RO     | HFRCO Fine Tuning Value                                    |
| 7     | <i>Reserved</i> |        | <i>Reserved for future use</i>                             |
| 6:0   | TUNING          | RO     | HFRCO Tuning Value   |

## 4.7.20 HFRCOAL3 - HFRCO Calibration Register (7 MHz)

| Offset | Bit Position |    |    |              |        |       |         |           |    |    |          |    |    |            |    |    |          |    |    |        |    |    |          |   |    |          |   |    |          |   |    |          |  |  |
|--------|--------------|----|----|--------------|--------|-------|---------|-----------|----|----|----------|----|----|------------|----|----|----------|----|----|--------|----|----|----------|---|----|----------|---|----|----------|---|----|----------|--|--|
| 0x08C  | 31           | 30 | 29 | 28           | 27     | 26    | 25      | 24        | 23 | 22 | 21       | 20 | 19 | 18         | 17 | 16 | 15       | 14 | 13 | 12     | 11 | 10 | 9        | 8 | 7  | 6        | 5 | 4  | 3        | 2 | 1  | 0        |  |  |
| Access | RO           |    |    | RO           | RO     | RO    | RO      | RO        | RO |    |          | RO |    |            | RO |    |          | RO | RO |        |    | RO |          |   | RO |          |   | RO |          |   | RO |          |  |  |
| Name   | VREFTC       |    |    | FINETUNINGEN | CLKDIV | LDOHP | CMPBIAS | FREQRANGE |    |    | Reserved |    |    | FINETUNING |    |    | Reserved |    |    | TUNING |    |    | Reserved |   |    | Reserved |   |    | Reserved |   |    | Reserved |  |  |

| Bit   | Name            | Access | Description  |
|-------|-----------------|--------|--|
| 31:28 | VREFTC          | RO     | HFRCO Temperature Coefficient Trim on Comparator Reference |
| 27    | FINETUNINGEN    | RO     | HFRCO enable reference for fine tuning                     |
| 26:25 | CLKDIV          | RO     | HFRCO Clock Output Divide                                  |
| 24    | LDOHP           | RO     | HFRCO LDO High Power Mode                                  |
| 23:21 | CMPBIAS         | RO     | HFRCO Comparator Bias Current                              |
| 20:16 | FREQRANGE       | RO     | HFRCO Frequency Range                                      |
| 15:14 | <i>Reserved</i> |        | <i>Reserved for future use</i>                             |
| 13:8  | FINETUNING      | RO     | HFRCO Fine Tuning Value                                    |
| 7     | <i>Reserved</i> |        | <i>Reserved for future use</i>                             |
| 6:0   | TUNING          | RO     | HFRCO Tuning Value   |

## 4.7.21 HFRCOAL6 - HFRCO Calibration Register (13 MHz)

| Offset | Bit Position |    |    |    |              |        |    |       |         |    |    |           |    |    |    |    |    |    |            |    |    |    |   |   |   |        |   |   |   |   |   |   |
|--------|--------------|----|----|----|--------------|--------|----|-------|---------|----|----|-----------|----|----|----|----|----|----|------------|----|----|----|---|---|---|--------|---|---|---|---|---|---|
| 0x098  | 31           | 30 | 29 | 28 | 27           | 26     | 25 | 24    | 23      | 22 | 21 | 20        | 19 | 18 | 17 | 16 | 15 | 14 | 13         | 12 | 11 | 10 | 9 | 8 | 7 | 6      | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO           |    |    |    | RO           | RO     |    | RO    | RO      |    |    | RO        |    |    |    |    |    |    | RO         |    |    |    |   |   |   |        |   |   |   |   |   |   |
| Name   | VREFTC       |    |    |    | FINETUNINGEN | CLKDIV |    | LDOHP | CMPBIAS |    |    | FREQRANGE |    |    |    |    |    |    | FINETUNING |    |    |    |   |   |   | TUNING |   |   |   |   |   |   |

| Bit   | Name            | Access | Description  |
|-------|-----------------|--------|--|
| 31:28 | VREFTC          | RO     | HFRCO Temperature Coefficient Trim on Comparator Reference |
| 27    | FINETUNINGEN    | RO     | HFRCO enable reference for fine tuning                     |
| 26:25 | CLKDIV          | RO     | HFRCO Clock Output Divide                                  |
| 24    | LDOHP           | RO     | HFRCO LDO High Power Mode                                  |
| 23:21 | CMPBIAS         | RO     | HFRCO Comparator Bias Current                              |
| 20:16 | FREQRANGE       | RO     | HFRCO Frequency Range                                      |
| 15:14 | <i>Reserved</i> |        | <i>Reserved for future use</i>                             |
| 13:8  | FINETUNING      | RO     | HFRCO Fine Tuning Value                                    |
| 7     | <i>Reserved</i> |        | <i>Reserved for future use</i>                             |
| 6:0   | TUNING          | RO     | HFRCO Tuning Value   |

## 4.7.22 HFRCOAL7 - HFRCO Calibration Register (16 MHz)

| Offset | Bit Position |    |    |              |        |       |         |           |    |    |          |    |    |            |    |    |          |    |    |        |    |    |          |   |    |          |   |    |          |   |    |          |  |  |
|--------|--------------|----|----|--------------|--------|-------|---------|-----------|----|----|----------|----|----|------------|----|----|----------|----|----|--------|----|----|----------|---|----|----------|---|----|----------|---|----|----------|--|--|
| 0x09C  | 31           | 30 | 29 | 28           | 27     | 26    | 25      | 24        | 23 | 22 | 21       | 20 | 19 | 18         | 17 | 16 | 15       | 14 | 13 | 12     | 11 | 10 | 9        | 8 | 7  | 6        | 5 | 4  | 3        | 2 | 1  | 0        |  |  |
| Access | RO           |    |    | RO           | RO     | RO    | RO      | RO        | RO |    |          | RO |    |            | RO |    |          | RO | RO |        |    | RO |          |   | RO |          |   | RO |          |   | RO |          |  |  |
| Name   | VREFTC       |    |    | FINETUNINGEN | CLKDIV | LDOHP | CMPBIAS | FREQRANGE |    |    | Reserved |    |    | FINETUNING |    |    | Reserved |    |    | TUNING |    |    | Reserved |   |    | Reserved |   |    | Reserved |   |    | Reserved |  |  |

| Bit   | Name            | Access | Description  |
|-------|-----------------|--------|--|
| 31:28 | VREFTC          | RO     | HFRCO Temperature Coefficient Trim on Comparator Reference |
| 27    | FINETUNINGEN    | RO     | HFRCO enable reference for fine tuning                     |
| 26:25 | CLKDIV          | RO     | HFRCO Clock Output Divide                                  |
| 24    | LDOHP           | RO     | HFRCO LDO High Power Mode                                  |
| 23:21 | CMPBIAS         | RO     | HFRCO Comparator Bias Current                              |
| 20:16 | FREQRANGE       | RO     | HFRCO Frequency Range                                      |
| 15:14 | <i>Reserved</i> |        | <i>Reserved for future use</i>                             |
| 13:8  | FINETUNING      | RO     | HFRCO Fine Tuning Value                                    |
| 7     | <i>Reserved</i> |        | <i>Reserved for future use</i>                             |
| 6:0   | TUNING          | RO     | HFRCO Tuning Value   |

## 4.7.23 HFRCOAL8 - HFRCO Calibration Register (19 MHz)

| Offset | Bit Position |    |    |              |        |       |         |           |    |    |          |    |    |            |    |    |          |    |    |        |    |    |          |   |    |          |   |    |          |   |    |          |  |  |
|--------|--------------|----|----|--------------|--------|-------|---------|-----------|----|----|----------|----|----|------------|----|----|----------|----|----|--------|----|----|----------|---|----|----------|---|----|----------|---|----|----------|--|--|
| 0x0A0  | 31           | 30 | 29 | 28           | 27     | 26    | 25      | 24        | 23 | 22 | 21       | 20 | 19 | 18         | 17 | 16 | 15       | 14 | 13 | 12     | 11 | 10 | 9        | 8 | 7  | 6        | 5 | 4  | 3        | 2 | 1  | 0        |  |  |
| Access | RO           |    |    | RO           | RO     | RO    | RO      | RO        | RO |    |          | RO |    |            | RO |    |          | RO | RO |        |    | RO |          |   | RO |          |   | RO |          |   | RO |          |  |  |
| Name   | VREFTC       |    |    | FINETUNINGEN | CLKDIV | LDOHP | CMPBIAS | FREQRANGE |    |    | Reserved |    |    | FINETUNING |    |    | Reserved |    |    | TUNING |    |    | Reserved |   |    | Reserved |   |    | Reserved |   |    | Reserved |  |  |

| Bit   | Name            | Access | Description  |
|-------|-----------------|--------|--|
| 31:28 | VREFTC          | RO     | HFRCO Temperature Coefficient Trim on Comparator Reference |
| 27    | FINETUNINGEN    | RO     | HFRCO enable reference for fine tuning                     |
| 26:25 | CLKDIV          | RO     | HFRCO Clock Output Divide                                  |
| 24    | LDOHP           | RO     | HFRCO LDO High Power Mode                                  |
| 23:21 | CMPBIAS         | RO     | HFRCO Comparator Bias Current                              |
| 20:16 | FREQRANGE       | RO     | HFRCO Frequency Range                                      |
| 15:14 | <i>Reserved</i> |        | <i>Reserved for future use</i>                             |
| 13:8  | FINETUNING      | RO     | HFRCO Fine Tuning Value                                    |
| 7     | <i>Reserved</i> |        | <i>Reserved for future use</i>                             |
| 6:0   | TUNING          | RO     | HFRCO Tuning Value   |

## 4.7.24 HFRCOAL10 - HFRCO Calibration Register (26 MHz)

| Offset | Bit Position |    |    |    |              |        |    |       |         |    |    |           |    |    |    |    |    |    |            |    |    |    |   |   |   |        |   |   |   |   |   |   |
|--------|--------------|----|----|----|--------------|--------|----|-------|---------|----|----|-----------|----|----|----|----|----|----|------------|----|----|----|---|---|---|--------|---|---|---|---|---|---|
| 0x0A8  | 31           | 30 | 29 | 28 | 27           | 26     | 25 | 24    | 23      | 22 | 21 | 20        | 19 | 18 | 17 | 16 | 15 | 14 | 13         | 12 | 11 | 10 | 9 | 8 | 7 | 6      | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO           |    |    |    | RO           | RO     |    | RO    | RO      |    |    | RO        |    |    |    |    |    |    | RO         |    |    |    |   |   |   |        |   |   |   |   |   |   |
| Name   | VREFTC       |    |    |    | FINETUNINGEN | CLKDIV |    | LDOHP | CMPBIAS |    |    | FREQRANGE |    |    |    |    |    |    | FINETUNING |    |    |    |   |   |   | TUNING |   |   |   |   |   |   |

| Bit   | Name            | Access | Description  |
|-------|-----------------|--------|--|
| 31:28 | VREFTC          | RO     | HFRCO Temperature Coefficient Trim on Comparator Reference |
| 27    | FINETUNINGEN    | RO     | HFRCO enable reference for fine tuning                     |
| 26:25 | CLKDIV          | RO     | HFRCO Clock Output Divide                                  |
| 24    | LDOHP           | RO     | HFRCO LDO High Power Mode                                  |
| 23:21 | CMPBIAS         | RO     | HFRCO Comparator Bias Current                              |
| 20:16 | FREQRANGE       | RO     | HFRCO Frequency Range                                      |
| 15:14 | <i>Reserved</i> |        | <i>Reserved for future use</i>                             |
| 13:8  | FINETUNING      | RO     | HFRCO Fine Tuning Value                                    |
| 7     | <i>Reserved</i> |        | <i>Reserved for future use</i>                             |
| 6:0   | TUNING          | RO     | HFRCO Tuning Value   |

## 4.7.25 HFRCOAL11 - HFRCO Calibration Register (32 MHz)

| Offset | Bit Position |    |    |    |              |        |    |       |         |    |    |           |    |    |    |    |    |    |    |            |    |    |   |   |   |        |   |   |   |   |   |   |
|--------|--------------|----|----|----|--------------|--------|----|-------|---------|----|----|-----------|----|----|----|----|----|----|----|------------|----|----|---|---|---|--------|---|---|---|---|---|---|
| 0x0AC  | 31           | 30 | 29 | 28 | 27           | 26     | 25 | 24    | 23      | 22 | 21 | 20        | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12         | 11 | 10 | 9 | 8 | 7 | 6      | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO           |    |    |    | RO           | RO     |    | RO    | RO      |    |    | RO        |    |    |    |    |    |    |    | RO         |    |    |   |   |   |        |   |   |   |   |   |   |
| Name   | VREFTC       |    |    |    | FINETUNINGEN | CLKDIV |    | LDOHP | CMPBIAS |    |    | FREQRANGE |    |    |    |    |    |    |    | FINETUNING |    |    |   |   |   | TUNING |   |   |   |   |   |   |

| Bit   | Name            | Access | Description  |
|-------|-----------------|--------|--|
| 31:28 | VREFTC          | RO     | HFRCO Temperature Coefficient Trim on Comparator Reference |
| 27    | FINETUNINGEN    | RO     | HFRCO enable reference for fine tuning                     |
| 26:25 | CLKDIV          | RO     | HFRCO Clock Output Divide                                  |
| 24    | LDOHP           | RO     | HFRCO LDO High Power Mode                                  |
| 23:21 | CMPBIAS         | RO     | HFRCO Comparator Bias Current                              |
| 20:16 | FREQRANGE       | RO     | HFRCO Frequency Range                                      |
| 15:14 | <i>Reserved</i> |        | <i>Reserved for future use</i>                             |
| 13:8  | FINETUNING      | RO     | HFRCO Fine Tuning Value                                    |
| 7     | <i>Reserved</i> |        | <i>Reserved for future use</i>                             |
| 6:0   | TUNING          | RO     | HFRCO Tuning Value   |

## 4.7.26 HFRCOAL12 - HFRCO Calibration Register (38 MHz)

| Offset | Bit Position |    |    |    |              |        |    |       |         |    |    |           |    |    |    |    |    |            |    |    |    |    |   |        |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|--------------|--------|----|-------|---------|----|----|-----------|----|----|----|----|----|------------|----|----|----|----|---|--------|---|---|---|---|---|---|---|---|
| 0x0B0  | 31           | 30 | 29 | 28 | 27           | 26     | 25 | 24    | 23      | 22 | 21 | 20        | 19 | 18 | 17 | 16 | 15 | 14         | 13 | 12 | 11 | 10 | 9 | 8      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO           |    |    |    | RO           | RO     |    | RO    | RO      |    |    | RO        |    |    |    |    |    | RO         |    |    |    |    |   | RO     |   |   |   |   |   |   |   |   |
| Name   | VREFTC       |    |    |    | FINETUNINGEN | CLKDIV |    | LDOHP | CMPBIAS |    |    | FREQRANGE |    |    |    |    |    | FINETUNING |    |    |    |    |   | TUNING |   |   |   |   |   |   |   |   |

| Bit   | Name            | Access | Description  |
|-------|-----------------|--------|--|
| 31:28 | VREFTC          | RO     | HFRCO Temperature Coefficient Trim on Comparator Reference |
| 27    | FINETUNINGEN    | RO     | HFRCO enable reference for fine tuning                     |
| 26:25 | CLKDIV          | RO     | HFRCO Clock Output Divide                                  |
| 24    | LDOHP           | RO     | HFRCO LDO High Power Mode                                  |
| 23:21 | CMPBIAS         | RO     | HFRCO Comparator Bias Current                              |
| 20:16 | FREQRANGE       | RO     | HFRCO Frequency Range                                      |
| 15:14 | <i>Reserved</i> |        | <i>Reserved for future use</i>                             |
| 13:8  | FINETUNING      | RO     | HFRCO Fine Tuning Value                                    |
| 7     | <i>Reserved</i> |        | <i>Reserved for future use</i>                             |
| 6:0   | TUNING          | RO     | HFRCO Tuning Value   |

## 4.7.27 AUXHFRCOCAL0 - AUXHFRCO Calibration Register (4 MHz)

| Offset | Bit Position |    |    |    |              |        |    |       |         |    |    |           |    |    |    |    |    |            |    |    |    |    |   |        |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|--------------|--------|----|-------|---------|----|----|-----------|----|----|----|----|----|------------|----|----|----|----|---|--------|---|---|---|---|---|---|---|---|
| 0x0E0  | 31           | 30 | 29 | 28 | 27           | 26     | 25 | 24    | 23      | 22 | 21 | 20        | 19 | 18 | 17 | 16 | 15 | 14         | 13 | 12 | 11 | 10 | 9 | 8      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO           |    |    |    | RO           | RO     |    | RO    | RO      |    |    | RO        |    |    |    |    |    | RO         |    |    |    |    |   | RO     |   |   |   |   |   |   |   |   |
| Name   | VREFTC       |    |    |    | FINETUNINGEN | CLKDIV |    | LDOHP | CMPBIAS |    |    | FREQRANGE |    |    |    |    |    | FINETUNING |    |    |    |    |   | TUNING |   |   |   |   |   |   |   |   |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31:28 | VREFTC          | RO     | AUXHFRCO Temperature Coefficient Trim on Comparator Reference |
| 27    | FINETUNINGEN    | RO     | AUXHFRCO enable reference for fine tuning                     |
| 26:25 | CLKDIV          | RO     | AUXHFRCO Clock Output Divide                                  |
| 24    | LDOHP           | RO     | AUXHFRCO LDO High Power Mode                                  |
| 23:21 | CMPBIAS         | RO     | AUXHFRCO Comparator Bias Current                              |
| 20:16 | FREQRANGE       | RO     | AUXHFRCO Frequency Range                                      |
| 15:14 | <i>Reserved</i> |        | <i>Reserved for future use</i>                                |
| 13:8  | FINETUNING      | RO     | AUXHFRCO Fine Tuning Value                                    |
| 7     | <i>Reserved</i> |        | <i>Reserved for future use</i>                                |
| 6:0   | TUNING          | RO     | AUXHFRCO Tuning Value   |

## 4.7.28 AUXHFRCOCAL3 - AUXHFRCO Calibration Register (7 MHz)

| Offset | Bit Position |    |    |    |              |        |    |       |         |    |    |           |    |    |    |    |    |            |    |    |    |    |   |        |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|--------------|--------|----|-------|---------|----|----|-----------|----|----|----|----|----|------------|----|----|----|----|---|--------|---|---|---|---|---|---|---|---|
| 0x0EC  | 31           | 30 | 29 | 28 | 27           | 26     | 25 | 24    | 23      | 22 | 21 | 20        | 19 | 18 | 17 | 16 | 15 | 14         | 13 | 12 | 11 | 10 | 9 | 8      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO           |    |    |    | RO           | RO     |    | RO    | RO      |    |    | RO        |    |    |    |    |    | RO         |    |    |    |    |   | RO     |   |   |   |   |   |   |   |   |
| Name   | VREFTC       |    |    |    | FINETUNINGEN | CLKDIV |    | LDOHP | CMPBIAS |    |    | FREQRANGE |    |    |    |    |    | FINETUNING |    |    |    |    |   | TUNING |   |   |   |   |   |   |   |   |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31:28 | VREFTC          | RO     | AUXHFRCO Temperature Coefficient Trim on Comparator Reference |
| 27    | FINETUNINGEN    | RO     | AUXHFRCO enable reference for fine tuning                     |
| 26:25 | CLKDIV          | RO     | AUXHFRCO Clock Output Divide                                  |
| 24    | LDOHP           | RO     | AUXHFRCO LDO High Power Mode                                  |
| 23:21 | CMPBIAS         | RO     | AUXHFRCO Comparator Bias Current                              |
| 20:16 | FREQRANGE       | RO     | AUXHFRCO Frequency Range                                      |
| 15:14 | <i>Reserved</i> |        | <i>Reserved for future use</i>                                |
| 13:8  | FINETUNING      | RO     | AUXHFRCO Fine Tuning Value                                    |
| 7     | <i>Reserved</i> |        | <i>Reserved for future use</i>                                |
| 6:0   | TUNING          | RO     | AUXHFRCO Tuning Value   |

## 4.7.29 AUXHFRCOCAL6 - AUXHFRCO Calibration Register (13 MHz)

| Offset | Bit Position |    |    |    |              |        |    |       |         |    |    |           |    |    |    |    |    |            |    |    |    |    |   |        |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|--------------|--------|----|-------|---------|----|----|-----------|----|----|----|----|----|------------|----|----|----|----|---|--------|---|---|---|---|---|---|---|---|
| 0x0F8  | 31           | 30 | 29 | 28 | 27           | 26     | 25 | 24    | 23      | 22 | 21 | 20        | 19 | 18 | 17 | 16 | 15 | 14         | 13 | 12 | 11 | 10 | 9 | 8      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO           |    |    |    | RO           | RO     |    | RO    | RO      |    |    | RO        |    |    |    |    |    | RO         |    |    |    |    |   | RO     |   |   |   |   |   |   |   |   |
| Name   | VREFTC       |    |    |    | FINETUNINGEN | CLKDIV |    | LDOHP | CMPBIAS |    |    | FREQRANGE |    |    |    |    |    | FINETUNING |    |    |    |    |   | TUNING |   |   |   |   |   |   |   |   |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31:28 | VREFTC          | RO     | AUXHFRCO Temperature Coefficient Trim on Comparator Reference |
| 27    | FINETUNINGEN    | RO     | AUXHFRCO enable reference for fine tuning                     |
| 26:25 | CLKDIV          | RO     | AUXHFRCO Clock Output Divide                                  |
| 24    | LDOHP           | RO     | AUXHFRCO LDO High Power Mode                                  |
| 23:21 | CMPBIAS         | RO     | AUXHFRCO Comparator Bias Current                              |
| 20:16 | FREQRANGE       | RO     | AUXHFRCO Frequency Range                                      |
| 15:14 | <i>Reserved</i> |        | <i>Reserved for future use</i>                                |
| 13:8  | FINETUNING      | RO     | AUXHFRCO Fine Tuning Value                                    |
| 7     | <i>Reserved</i> |        | <i>Reserved for future use</i>                                |
| 6:0   | TUNING          | RO     | AUXHFRCO Tuning Value   |

## 4.7.30 AUXHFRCOCAL7 - AUXHFRCO Calibration Register (16 MHz)

| Offset | Bit Position |    |    |    |              |        |    |       |         |    |    |           |    |    |    |    |    |    |            |    |    |    |   |   |        |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|--------------|--------|----|-------|---------|----|----|-----------|----|----|----|----|----|----|------------|----|----|----|---|---|--------|---|---|---|---|---|---|---|
| 0x0FC  | 31           | 30 | 29 | 28 | 27           | 26     | 25 | 24    | 23      | 22 | 21 | 20        | 19 | 18 | 17 | 16 | 15 | 14 | 13         | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO           |    |    |    | RO           | RO     |    | RO    | RO      |    |    | RO        |    |    |    |    |    |    | RO         |    |    |    |   |   |        |   |   |   |   |   |   |   |
| Name   | VREFTC       |    |    |    | FINETUNINGEN | CLKDIV |    | LDOHP | CMPBIAS |    |    | FREQRANGE |    |    |    |    |    |    | FINETUNING |    |    |    |   |   | TUNING |   |   |   |   |   |   |   |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31:28 | VREFTC          | RO     | AUXHFRCO Temperature Coefficient Trim on Comparator Reference |
| 27    | FINETUNINGEN    | RO     | AUXHFRCO enable reference for fine tuning                     |
| 26:25 | CLKDIV          | RO     | AUXHFRCO Clock Output Divide                                  |
| 24    | LDOHP           | RO     | AUXHFRCO LDO High Power Mode                                  |
| 23:21 | CMPBIAS         | RO     | AUXHFRCO Comparator Bias Current                              |
| 20:16 | FREQRANGE       | RO     | AUXHFRCO Frequency Range                                      |
| 15:14 | <i>Reserved</i> |        | <i>Reserved for future use</i>                                |
| 13:8  | FINETUNING      | RO     | AUXHFRCO Fine Tuning Value                                    |
| 7     | <i>Reserved</i> |        | <i>Reserved for future use</i>                                |
| 6:0   | TUNING          | RO     | AUXHFRCO Tuning Value   |

## 4.7.31 AUXHFRCOCAL8 - AUXHFRCO Calibration Register (19 MHz)

| Offset | Bit Position |    |    |    |              |        |    |       |         |    |    |           |    |    |    |    |    |    |            |    |    |    |   |   |        |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|--------------|--------|----|-------|---------|----|----|-----------|----|----|----|----|----|----|------------|----|----|----|---|---|--------|---|---|---|---|---|---|---|
| 0x100  | 31           | 30 | 29 | 28 | 27           | 26     | 25 | 24    | 23      | 22 | 21 | 20        | 19 | 18 | 17 | 16 | 15 | 14 | 13         | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO           |    |    |    | RO           | RO     |    | RO    | RO      |    |    | RO        |    |    |    |    |    |    | RO         |    |    |    |   |   |        |   |   |   |   |   |   |   |
| Name   | VREFTC       |    |    |    | FINETUNINGEN | CLKDIV |    | LDOHP | CMPBIAS |    |    | FREQRANGE |    |    |    |    |    |    | FINETUNING |    |    |    |   |   | TUNING |   |   |   |   |   |   |   |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31:28 | VREFTC          | RO     | AUXHFRCO Temperature Coefficient Trim on Comparator Reference |
| 27    | FINETUNINGEN    | RO     | AUXHFRCO enable reference for fine tuning                     |
| 26:25 | CLKDIV          | RO     | AUXHFRCO Clock Output Divide                                  |
| 24    | LDOHP           | RO     | AUXHFRCO LDO High Power Mode                                  |
| 23:21 | CMPBIAS         | RO     | AUXHFRCO Comparator Bias Current                              |
| 20:16 | FREQRANGE       | RO     | AUXHFRCO Frequency Range                                      |
| 15:14 | <i>Reserved</i> |        | <i>Reserved for future use</i>                                |
| 13:8  | FINETUNING      | RO     | AUXHFRCO Fine Tuning Value                                    |
| 7     | <i>Reserved</i> |        | <i>Reserved for future use</i>                                |
| 6:0   | TUNING          | RO     | AUXHFRCO Tuning Value   |

## 4.7.32 AUXHFRCOCAL10 - AUXHFRCO Calibration Register (26 MHz)

| Offset | Bit Position |    |    |    |              |        |    |       |         |    |    |           |    |    |    |    |    |            |    |    |    |    |   |        |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|--------------|--------|----|-------|---------|----|----|-----------|----|----|----|----|----|------------|----|----|----|----|---|--------|---|---|---|---|---|---|---|---|
| 0x108  | 31           | 30 | 29 | 28 | 27           | 26     | 25 | 24    | 23      | 22 | 21 | 20        | 19 | 18 | 17 | 16 | 15 | 14         | 13 | 12 | 11 | 10 | 9 | 8      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO           |    |    |    | RO           | RO     |    | RO    | RO      |    |    | RO        |    |    |    |    |    | RO         |    |    |    |    |   | RO     |   |   |   |   |   |   |   |   |
| Name   | VREFTC       |    |    |    | FINETUNINGEN | CLKDIV |    | LDOHP | CMPBIAS |    |    | FREQRANGE |    |    |    |    |    | FINETUNING |    |    |    |    |   | TUNING |   |   |   |   |   |   |   |   |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31:28 | VREFTC          | RO     | AUXHFRCO Temperature Coefficient Trim on Comparator Reference |
| 27    | FINETUNINGEN    | RO     | AUXHFRCO enable reference for fine tuning                     |
| 26:25 | CLKDIV          | RO     | AUXHFRCO Clock Output Divide                                  |
| 24    | LDOHP           | RO     | AUXHFRCO LDO High Power Mode                                  |
| 23:21 | CMPBIAS         | RO     | AUXHFRCO Comparator Bias Current                              |
| 20:16 | FREQRANGE       | RO     | AUXHFRCO Frequency Range                                      |
| 15:14 | <i>Reserved</i> |        | <i>Reserved for future use</i>                                |
| 13:8  | FINETUNING      | RO     | AUXHFRCO Fine Tuning Value                                    |
| 7     | <i>Reserved</i> |        | <i>Reserved for future use</i>                                |
| 6:0   | TUNING          | RO     | AUXHFRCO Tuning Value   |

## 4.7.33 AUXHFRCOCAL11 - AUXHFRCO Calibration Register (32 MHz)

| Offset | Bit Position |    |    |    |              |        |    |       |         |    |    |           |    |    |    |    |    |    |            |    |    |    |   |   |        |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|--------------|--------|----|-------|---------|----|----|-----------|----|----|----|----|----|----|------------|----|----|----|---|---|--------|---|---|---|---|---|---|---|
| 0x10C  | 31           | 30 | 29 | 28 | 27           | 26     | 25 | 24    | 23      | 22 | 21 | 20        | 19 | 18 | 17 | 16 | 15 | 14 | 13         | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO           |    |    |    | RO           | RO     |    | RO    | RO      |    |    | RO        |    |    |    |    |    |    | RO         |    |    |    |   |   |        |   |   |   |   |   |   |   |
| Name   | VREFTC       |    |    |    | FINETUNINGEN | CLKDIV |    | LDOHP | CMPBIAS |    |    | FREQRANGE |    |    |    |    |    |    | FINETUNING |    |    |    |   |   | TUNING |   |   |   |   |   |   |   |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31:28 | VREFTC          | RO     | AUXHFRCO Temperature Coefficient Trim on Comparator Reference |
| 27    | FINETUNINGEN    | RO     | AUXHFRCO enable reference for fine tuning                     |
| 26:25 | CLKDIV          | RO     | AUXHFRCO Clock Output Divide                                  |
| 24    | LDOHP           | RO     | AUXHFRCO LDO High Power Mode                                  |
| 23:21 | CMPBIAS         | RO     | AUXHFRCO Comparator Bias Current                              |
| 20:16 | FREQRANGE       | RO     | AUXHFRCO Frequency Range                                      |
| 15:14 | <i>Reserved</i> |        | <i>Reserved for future use</i>                                |
| 13:8  | FINETUNING      | RO     | AUXHFRCO Fine Tuning Value                                    |
| 7     | <i>Reserved</i> |        | <i>Reserved for future use</i>                                |
| 6:0   | TUNING          | RO     | AUXHFRCO Tuning Value   |

## 4.7.34 AUXHFRCOCAL12 - AUXHFRCO Calibration Register (38 MHz)

| Offset | Bit Position |    |    |    |              |        |    |       |         |    |    |           |    |    |    |    |    |    |            |    |    |    |   |   |        |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|--------------|--------|----|-------|---------|----|----|-----------|----|----|----|----|----|----|------------|----|----|----|---|---|--------|---|---|---|---|---|---|---|
| 0x110  | 31           | 30 | 29 | 28 | 27           | 26     | 25 | 24    | 23      | 22 | 21 | 20        | 19 | 18 | 17 | 16 | 15 | 14 | 13         | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO           |    |    |    | RO           | RO     |    | RO    | RO      |    |    | RO        |    |    |    |    |    |    | RO         |    |    |    |   |   |        |   |   |   |   |   |   |   |
| Name   | VREFTC       |    |    |    | FINETUNINGEN | CLKDIV |    | LDOHP | CMPBIAS |    |    | FREQRANGE |    |    |    |    |    |    | FINETUNING |    |    |    |   |   | TUNING |   |   |   |   |   |   |   |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31:28 | VREFTC          | RO     | AUXHFRCO Temperature Coefficient Trim on Comparator Reference |
| 27    | FINETUNINGEN    | RO     | AUXHFRCO enable reference for fine tuning                     |
| 26:25 | CLKDIV          | RO     | AUXHFRCO Clock Output Divide                                  |
| 24    | LDOHP           | RO     | AUXHFRCO LDO High Power Mode                                  |
| 23:21 | CMPBIAS         | RO     | AUXHFRCO Comparator Bias Current                              |
| 20:16 | FREQRANGE       | RO     | AUXHFRCO Frequency Range                                      |
| 15:14 | <i>Reserved</i> |        | <i>Reserved for future use</i>                                |
| 13:8  | FINETUNING      | RO     | AUXHFRCO Fine Tuning Value                                    |
| 7     | <i>Reserved</i> |        | <i>Reserved for future use</i>                                |
| 6:0   | TUNING          | RO     | AUXHFRCO Tuning Value   |

## 4.7.35 VMONCAL0 - VMON Calibration Register 0

| Offset | Bit Position           |    |    |    |                      |    |    |    |                        |    |    |    |                      |    |    |    |                     |    |    |    |                   |    |   |   |                     |   |   |   |                   |   |   |   |
|--------|------------------------|----|----|----|----------------------|----|----|----|------------------------|----|----|----|----------------------|----|----|----|---------------------|----|----|----|-------------------|----|---|---|---------------------|---|---|---|-------------------|---|---|---|
| 0x140  | 31                     | 30 | 29 | 28 | 27                   | 26 | 25 | 24 | 23                     | 22 | 21 | 20 | 19                   | 18 | 17 | 16 | 15                  | 14 | 13 | 12 | 11                | 10 | 9 | 8 | 7                   | 6 | 5 | 4 | 3                 | 2 | 1 | 0 |
| Access | RO                     |    |    |    | RO                   |    |    |    | RO                     |    |    |    | RO                   |    |    |    | RO                  |    |    |    | RO                |    |   |   | RO                  |   |   |   |                   |   |   |   |
| Name   | ALTAVDD2V98THRESCOARSE |    |    |    | ALTAVDD2V98THRESFINE |    |    |    | ALTAVDD1V86THRESCOARSE |    |    |    | ALTAVDD1V86THRESFINE |    |    |    | AVDD2V98THRESCOARSE |    |    |    | AVDD2V98THRESFINE |    |   |   | AVDD1V86THRESCOARSE |   |   |   | AVDD1V86THRESFINE |   |   |   |

| Bit   | Name                   | Access | Description                            |
|-------|------------------------|--------|--|
| 31:28 | ALTAVDD2V98THRESCOARSE | RO     | ALTAVDD 2.98 V Coarse Threshold Adjust |
| 27:24 | ALTAVDD2V98THRESFINE   | RO     | ALTAVDD 2.98 V Fine Threshold Adjust   |
| 23:20 | ALTAVDD1V86THRESCOARSE | RO     | ALTAVDD 1.86 V Coarse Threshold Adjust |
| 19:16 | ALTAVDD1V86THRESFINE   | RO     | ALTAVDD 1.86 V Fine Threshold Adjust   |
| 15:12 | AVDD2V98THRESCOARSE    | RO     | AVDD 2.98 V Coarse Threshold Adjust    |
| 11:8  | AVDD2V98THRESFINE      | RO     | AVDD 2.98 V Fine Threshold Adjust      |
| 7:4   | AVDD1V86THRESCOARSE    | RO     | AVDD 1.86 V Coarse Threshold Adjust    |
| 3:0   | AVDD1V86THRESFINE      | RO     | AVDD 1.86 V Fine Threshold Adjust      |

## 4.7.36 VMONCAL1 - VMON Calibration Register 1

| Offset | Bit Position       |    |    |    |                  |    |    |    |                    |    |    |    |                  |    |    |    |                     |    |    |    |                   |    |   |   |                     |   |   |   |                   |   |   |   |
|--------|--------------------|----|----|----|------------------|----|----|----|--------------------|----|----|----|------------------|----|----|----|---------------------|----|----|----|-------------------|----|---|---|---------------------|---|---|---|-------------------|---|---|---|
| 0x144  | 31                 | 30 | 29 | 28 | 27               | 26 | 25 | 24 | 23                 | 22 | 21 | 20 | 19               | 18 | 17 | 16 | 15                  | 14 | 13 | 12 | 11                | 10 | 9 | 8 | 7                   | 6 | 5 | 4 | 3                 | 2 | 1 | 0 |
| Access | RO                 |    |    |    | RO               |    |    |    | RO                 |    |    |    | RO               |    |    |    | RO                  |    |    |    | RO                |    |   |   | RO                  |   |   |   |                   |   |   |   |
| Name   | IO02V98THRESCOARSE |    |    |    | IO02V98THRESFINE |    |    |    | IO01V86THRESCOARSE |    |    |    | IO01V86THRESFINE |    |    |    | DVDD2V98THRESCOARSE |    |    |    | DVDD2V98THRESFINE |    |   |   | DVDD1V86THRESCOARSE |   |   |   | DVDD1V86THRESFINE |   |   |   |

| Bit   | Name                | Access | Description                         |
|-------|---------------------|--------|-------------------------------------|
| 31:28 | IO02V98THRESCOARSE  | RO     | IO0 2.98 V Coarse Threshold Adjust  |
| 27:24 | IO02V98THRESFINE    | RO     | IO0 2.98 V Fine Threshold Adjust    |
| 23:20 | IO01V86THRESCOARSE  | RO     | IO0 1.86 V Coarse Threshold Adjust  |
| 19:16 | IO01V86THRESFINE    | RO     | IO0 1.86 V Fine Threshold Adjust    |
| 15:12 | DVDD2V98THRESCOARSE | RO     | DVDD 2.98 V Coarse Threshold Adjust |
| 11:8  | DVDD2V98THRESFINE   | RO     | DVDD 2.98 V Fine Threshold Adjust   |
| 7:4   | DVDD1V86THRESCOARSE | RO     | DVDD 1.86 V Coarse Threshold Adjust |
| 3:0   | DVDD1V86THRESFINE   | RO     | DVDD 1.86 V Fine Threshold Adjust   |

## 4.7.37 VMONCAL2 - VMON Calibration Register 2

| Offset | Bit Position        |    |    |    |                   |    |    |    |                     |    |    |    |                   |    |    |    |                      |    |    |    |                    |    |   |   |                      |   |   |   |                    |   |   |   |
|--------|---------------------|----|----|----|-------------------|----|----|----|---------------------|----|----|----|-------------------|----|----|----|----------------------|----|----|----|--------------------|----|---|---|----------------------|---|---|---|--------------------|---|---|---|
| 0x148  | 31                  | 30 | 29 | 28 | 27                | 26 | 25 | 24 | 23                  | 22 | 21 | 20 | 19                | 18 | 17 | 16 | 15                   | 14 | 13 | 12 | 11                 | 10 | 9 | 8 | 7                    | 6 | 5 | 4 | 3                  | 2 | 1 | 0 |
| Access | RO                  |    |    |    | RO                |    |    |    | RO                  |    |    |    | RO                |    |    |    | RO                   |    |    |    | RO                 |    |   |   | RO                   |   |   |   |                    |   |   |   |
| Name   | FVDD2V98THRESCOARSE |    |    |    | FVDD2V98THRESFINE |    |    |    | FVDD1V86THRESCOARSE |    |    |    | FVDD1V86THRESFINE |    |    |    | PAVDD2V98THRESCOARSE |    |    |    | PAVDD2V98THRESFINE |    |   |   | PAVDD1V86THRESCOARSE |   |   |   | PAVDD1V86THRESFINE |   |   |   |

| Bit   | Name                 | Access | Description                          |
|-------|----------------------|--------|--------------------------------------|
| 31:28 | FVDD2V98THRESCOARSE  | RO     | FVDD 2.98 V Coarse Threshold Adjust  |
| 27:24 | FVDD2V98THRESFINE    | RO     | FVDD 2.98 V Fine Threshold Adjust    |
| 23:20 | FVDD1V86THRESCOARSE  | RO     | FVDD 1.86 V Coarse Threshold Adjust  |
| 19:16 | FVDD1V86THRESFINE    | RO     | FVDD 1.86 V Fine Threshold Adjust    |
| 15:12 | PAVDD2V98THRESCOARSE | RO     | PAVDD 2.98 V Coarse Threshold Adjust |
| 11:8  | PAVDD2V98THRESFINE   | RO     | PAVDD 2.98 V Fine Threshold Adjust   |
| 7:4   | PAVDD1V86THRESCOARSE | RO     | PAVDD 1.86 V Coarse Threshold Adjust |
| 3:0   | PAVDD1V86THRESFINE   | RO     | PAVDD 1.86 V Fine Threshold Adjust   |

## 4.7.38 IDAC0CAL0 - IDAC0 Calibration Register 0

| Offset | Bit Position       |    |    |    |    |    |    |    |                    |    |    |    |    |    |    |    |                    |    |    |    |    |    |   |   |                    |   |   |   |   |   |   |   |
|--------|--------------------|----|----|----|----|----|----|----|--------------------|----|----|----|----|----|----|----|--------------------|----|----|----|----|----|---|---|--------------------|---|---|---|---|---|---|---|
| 0x158  | 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15                 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO                 |    |    |    |    |    |    |    | RO                 |    |    |    |    |    |    |    | RO                 |    |    |    |    |    |   |   | RO                 |   |   |   |   |   |   |   |
| Name   | SOURCERANGE3TUNING |    |    |    |    |    |    |    | SOURCERANGE2TUNING |    |    |    |    |    |    |    | SOURCERANGE1TUNING |    |    |    |    |    |   |   | SOURCERANGE0TUNING |   |   |   |   |   |   |   |

| Bit   | Name               | Access | Description  |
|-------|--------------------|--------|--|
| 31:24 | SOURCERANGE3TUNING | RO     | Calibrated middle step (16) of current source mode range 3 |
| 23:16 | SOURCERANGE2TUNING | RO     | Calibrated middle step (16) of current source mode range 2 |
| 15:8  | SOURCERANGE1TUNING | RO     | Calibrated middle step (16) of current source mode range 1 |
| 7:0   | SOURCERANGE0TUNING | RO     | Calibrated middle step (16) of current source mode range 0 |

## 4.7.39 IDAC0CAL1 - IDAC0 Calibration Register 1

| Offset | Bit Position     |    |    |    |    |    |    |    |                  |    |    |    |    |    |    |    |                  |    |    |    |    |    |   |   |                  |   |   |   |   |   |   |   |
|--------|------------------|----|----|----|----|----|----|----|------------------|----|----|----|----|----|----|----|------------------|----|----|----|----|----|---|---|------------------|---|---|---|---|---|---|---|
| 0x15C  | 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15               | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO               |    |    |    |    |    |    |    | RO               |    |    |    |    |    |    |    | RO               |    |    |    |    |    |   |   | RO               |   |   |   |   |   |   |   |
| Name   | SINKRANGE3TUNING |    |    |    |    |    |    |    | SINKRANGE2TUNING |    |    |    |    |    |    |    | SINKRANGE1TUNING |    |    |    |    |    |   |   | SINKRANGE0TUNING |   |   |   |   |   |   |   |

| Bit   | Name             | Access | Description  |
|-------|------------------|--------|--|
| 31:24 | SINKRANGE3TUNING | RO     | Calibrated middle step (16) of current sink mode range 3 |
| 23:16 | SINKRANGE2TUNING | RO     | Calibrated middle step (16) of current sink mode range 2 |
| 15:8  | SINKRANGE1TUNING | RO     | Calibrated middle step (16) of current sink mode range 1 |
| 7:0   | SINKRANGE0TUNING | RO     | Calibrated middle step (16) of current sink mode range 0 |

## 4.7.40 DCDCCLNCTRL0 - DCDC Low-noise VREF Trim Register 0

| Offset | Bit Position |    |    |    |    |    |    |    |           |    |    |    |    |    |    |    |           |    |    |    |    |    |   |   |           |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|-----------|----|----|----|----|----|----|----|-----------|----|----|----|----|----|---|---|-----------|---|---|---|---|---|---|---|
| 0x168  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO           |    |    |    |    |    |    |    | RO        |    |    |    |    |    |    |    | RO        |    |    |    |    |    |   |   | RO        |   |   |   |   |   |   |   |
| Name   | 3VOLNATT1    |    |    |    |    |    |    |    | 1V8LNATT1 |    |    |    |    |    |    |    | 1V8LNATT0 |    |    |    |    |    |   |   | 1V2LNATT0 |   |   |   |   |   |   |   |

| Bit   | Name      | Access | Description                               |
|-------|-----------|--------|---|
| 31:24 | 3VOLNATT1 | RO     | DCDC LNVREF Trim for 3.0V output, LNATT=1 |
| 23:16 | 1V8LNATT1 | RO     | DCDC LNVREF Trim for 1.8V output, LNATT=1 |
| 15:8  | 1V8LNATT0 | RO     | DCDC LNVREF Trim for 1.8V output, LNATT=0 |
| 7:0   | 1V2LNATT0 | RO     | DCDC LNVREF Trim for 1.2V output, LNATT=0 |

## 4.7.41 DCDCLPCTRL0 - DCDC Low-power VREF Trim Register 0

| Offset | Bit Position        |    |    |    |    |    |    |    |                     |    |    |    |    |    |    |    |                     |    |    |    |    |    |   |   |                     |   |   |   |   |   |   |   |
|--------|---------------------|----|----|----|----|----|----|----|---------------------|----|----|----|----|----|----|----|---------------------|----|----|----|----|----|---|---|---------------------|---|---|---|---|---|---|---|
| 0x16C  | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15                  | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO                  |    |    |    |    |    |    |    | RO                  |    |    |    |    |    |    |    | RO                  |    |    |    |    |    |   |   | RO                  |   |   |   |   |   |   |   |
| Name   | 1V8LPATT0LPCMPBIAS1 |    |    |    |    |    |    |    | 1V2LPATT0LPCMPBIAS1 |    |    |    |    |    |    |    | 1V8LPATT0LPCMPBIAS0 |    |    |    |    |    |   |   | 1V2LPATT0LPCMPBIAS0 |   |   |   |   |   |   |   |

| Bit   | Name                | Access | Description  |
|-------|---------------------|--------|--|
| 31:24 | 1V8LPATT0LPCMPBIAS1 | RO     | DCDC LPVREF Trim for 1.8V output, LPATT=0, LPCMPBIAS=1 |
| 23:16 | 1V2LPATT0LPCMPBIAS1 | RO     | DCDC LPVREF Trim for 1.2V output, LPATT=0, LPCMPBIAS=1 |
| 15:8  | 1V8LPATT0LPCMPBIAS0 | RO     | DCDC LPVREF Trim for 1.8V output, LPATT=0, LPCMPBIAS=0 |
| 7:0   | 1V2LPATT0LPCMPBIAS0 | RO     | DCDC LPVREF Trim for 1.2V output, LPATT=0, LPCMPBIAS=0 |

## 4.7.42 DCDCLPCTRL1 - DCDC Low-power VREF Trim Register 1

| Offset | Bit Position        |    |    |    |    |    |    |    |                     |    |    |    |    |    |    |    |                     |    |    |    |    |    |   |   |                     |   |   |   |   |   |   |   |
|--------|---------------------|----|----|----|----|----|----|----|---------------------|----|----|----|----|----|----|----|---------------------|----|----|----|----|----|---|---|---------------------|---|---|---|---|---|---|---|
| 0x170  | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15                  | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO                  |    |    |    |    |    |    |    | RO                  |    |    |    |    |    |    |    | RO                  |    |    |    |    |    |   |   | RO                  |   |   |   |   |   |   |   |
| Name   | 1V8LPATT0LPCMPBIAS3 |    |    |    |    |    |    |    | 1V2LPATT0LPCMPBIAS3 |    |    |    |    |    |    |    | 1V8LPATT0LPCMPBIAS2 |    |    |    |    |    |   |   | 1V2LPATT0LPCMPBIAS2 |   |   |   |   |   |   |   |

| Bit   | Name                | Access | Description  |
|-------|---------------------|--------|--|
| 31:24 | 1V8LPATT0LPCMPBIAS3 | RO     | DCDC LPVREF Trim for 1.8V output, LPATT=0, LPCMPBIAS=3 |
| 23:16 | 1V2LPATT0LPCMPBIAS3 | RO     | DCDC LPVREF Trim for 1.2V output, LPATT=0, LPCMPBIAS=3 |
| 15:8  | 1V8LPATT0LPCMPBIAS2 | RO     | DCDC LPVREF Trim for 1.8V output, LPATT=0, LPCMPBIAS=2 |
| 7:0   | 1V2LPATT0LPCMPBIAS2 | RO     | DCDC LPVREF Trim for 1.2V output, LPATT=0, LPCMPBIAS=2 |

## 4.7.43 DCDCLPCTRL2 - DCDC Low-power VREF Trim Register 2

| Offset | Bit Position        |    |    |    |    |    |    |    |                     |    |    |    |    |    |    |    |                     |    |    |    |    |    |   |   |                     |   |   |   |   |   |   |   |
|--------|---------------------|----|----|----|----|----|----|----|---------------------|----|----|----|----|----|----|----|---------------------|----|----|----|----|----|---|---|---------------------|---|---|---|---|---|---|---|
| 0x174  | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15                  | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO                  |    |    |    |    |    |    |    | RO                  |    |    |    |    |    |    |    | RO                  |    |    |    |    |    |   |   | RO                  |   |   |   |   |   |   |   |
| Name   | 3V0LPATT1LPCMPBIAS1 |    |    |    |    |    |    |    | 1V8LPATT1LPCMPBIAS1 |    |    |    |    |    |    |    | 3V0LPATT1LPCMPBIAS0 |    |    |    |    |    |   |   | 1V8LPATT1LPCMPBIAS0 |   |   |   |   |   |   |   |

| Bit   | Name                | Access | Description  |
|-------|---------------------|--------|--|
| 31:24 | 3V0LPATT1LPCMPBIAS1 | RO     | DCDC LPVREF Trim for 3.0V output, LPATT=1, LPCMPBIAS=1 |
| 23:16 | 1V8LPATT1LPCMPBIAS1 | RO     | DCDC LPVREF Trim for 1.8V output, LPATT=1, LPCMPBIAS=1 |
| 15:8  | 3V0LPATT1LPCMPBIAS0 | RO     | DCDC LPVREF Trim for 3.0V output, LPATT=1, LPCMPBIAS=0 |
| 7:0   | 1V8LPATT1LPCMPBIAS0 | RO     | DCDC LPVREF Trim for 1.8V output, LPATT=1, LPCMPBIAS=0 |

## 4.7.44 DCDCLPCTRL3 - DCDC Low-power VREF Trim Register 3

| Offset        | Bit Position        |    |    |    |    |    |    |    |                     |    |    |    |    |    |    |    |                     |    |    |    |    |    |   |   |                     |   |   |   |   |   |   |   |
|---------------|---------------------|----|----|----|----|----|----|----|---------------------|----|----|----|----|----|----|----|---------------------|----|----|----|----|----|---|---|---------------------|---|---|---|---|---|---|---|
| 0x178         | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15                  | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Access</b> | RO                  |    |    |    |    |    |    |    | RO                  |    |    |    |    |    |    |    | RO                  |    |    |    |    |    |   |   | RO                  |   |   |   |   |   |   |   |
| <b>Name</b>   | 3V0LPATT1LPCMPBIAS3 |    |    |    |    |    |    |    | 1V8LPATT1LPCMPBIAS3 |    |    |    |    |    |    |    | 3V0LPATT1LPCMPBIAS2 |    |    |    |    |    |   |   | 1V8LPATT1LPCMPBIAS2 |   |   |   |   |   |   |   |

| Bit   | Name                | Access | Description  |
|-------|---------------------|--------|--|
| 31:24 | 3V0LPATT1LPCMPBIAS3 | RO     | DCDC LPVREF Trim for 3.0V output, LPATT=1, LPCMPBIAS=3 |
| 23:16 | 1V8LPATT1LPCMPBIAS3 | RO     | DCDC LPVREF Trim for 1.8V output, LPATT=1, LPCMPBIAS=3 |
| 15:8  | 3V0LPATT1LPCMPBIAS2 | RO     | DCDC LPVREF Trim for 3.0V output, LPATT=1, LPCMPBIAS=3 |
| 7:0   | 1V8LPATT1LPCMPBIAS2 | RO     | DCDC LPVREF Trim for 1.8V output, LPATT=1, LPCMPBIAS=2 |

## 4.7.45 DCDCLPCMPHYSEL0 - DCDC LPCMPHYSEL Trim Register 0

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                  |    |    |    |    |    |   |   |                  |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------|----|----|----|----|----|---|---|------------------|---|---|---|---|---|---|---|
| 0x17C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15               | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RO               |    |    |    |    |    |   |   | RO               |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LPCMPHYSELTPATT1 |    |    |    |    |    |   |   | LPCMPHYSELTPATT0 |   |   |   |   |   |   |   |

| Bit   | Name             | Access | Description                    |
|-------|------------------|--------|--------------------------------|
| 31:16 | <i>Reserved</i>  |        | <i>Reserved for future use</i> |
| 15:8  | LPCMPHYSELTPATT1 | RO     | DCDC LPCMPHYSEL Trim, LPATT=1  |
| 7:0   | LPCMPHYSELTPATT0 | RO     | DCDC LPCMPHYSEL Trim, LPATT=0  |

## 4.7.46 DCDCLPCMPHYSEL1 - DCDC LPCMPHYSEL Trim Register 1

| Offset | Bit Position        |    |    |    |    |    |    |    |                     |    |    |    |    |    |    |    |                     |    |    |    |    |    |   |   |                     |   |   |   |   |   |   |   |
|--------|---------------------|----|----|----|----|----|----|----|---------------------|----|----|----|----|----|----|----|---------------------|----|----|----|----|----|---|---|---------------------|---|---|---|---|---|---|---|
| 0x180  | 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15                  | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | RO                  |    |    |    |    |    |    |    | RO                  |    |    |    |    |    |    |    | RO                  |    |    |    |    |    |   |   | RO                  |   |   |   |   |   |   |   |
| Name   | LPCMPHYSELPCMPBIAS3 |    |    |    |    |    |    |    | LPCMPHYSELPCMPBIAS2 |    |    |    |    |    |    |    | LPCMPHYSELPCMPBIAS1 |    |    |    |    |    |   |   | LPCMPHYSELPCMPBIAS0 |   |   |   |   |   |   |   |

| Bit   | Name                | Access | Description                       |
|-------|---------------------|--------|-----------------------------------|
| 31:24 | LPCMPHYSELPCMPBIAS3 | RO     | DCDC LPCMPHYSEL Trim, LPCMPBIAS=3 |
| 23:16 | LPCMPHYSELPCMPBIAS2 | RO     | DCDC LPCMPHYSEL Trim, LPCMPBIAS=2 |
| 15:8  | LPCMPHYSELPCMPBIAS1 | RO     | DCDC LPCMPHYSEL Trim, LPCMPBIAS=1 |
| 7:0   | LPCMPHYSELPCMPBIAS0 | RO     | DCDC LPCMPHYSEL Trim, LPCMPBIAS=0 |

## 4.7.47 VDACC0MAINCAL - VDACC0 Cals for Main Path

| Offset | Bit Position |    |    |    |                         |    |    |    |    |                |    |    |    |    |    |                 |    |    |    |    |    |                  |   |   |   |   |   |   |                   |   |   |   |
|--------|--------------|----|----|----|-------------------------|----|----|----|----|----------------|----|----|----|----|----|-----------------|----|----|----|----|----|------------------|---|---|---|---|---|---|-------------------|---|---|---|
| 0x184  | 31           | 30 | 29 | 28 | 27                      | 26 | 25 | 24 | 23 | 22             | 21 | 20 | 19 | 18 | 17 | 16              | 15 | 14 | 13 | 12 | 11 | 10               | 9 | 8 | 7 | 6 | 5 | 4 | 3                 | 2 | 1 | 0 |
| Access |              |    |    |    | RO                      |    |    |    |    | RO             |    |    |    |    |    | RO              |    |    |    |    |    | RO               |   |   |   |   |   |   | RO                |   |   |   |
| Name   |              |    |    |    | GAINERRTRIMVDDANAEXTPIN |    |    |    |    | GAINERRTRIM2V5 |    |    |    |    |    | GAINERRTRIM1V25 |    |    |    |    |    | GAINERRTRIM2V5LN |   |   |   |   |   |   | GAINERRTRIM1V25LN |   |   |   |

| Bit   | Name                    | Access | Description  |
|-------|-------------------------|--------|--|
| 31:30 | <i>Reserved</i>         |        | <i>Reserved for future use</i>   |
| 29:24 | GAINERRTRIMVDDANAEXTPIN | RO     | Gain Error Trim Value for DAC main output using references VDDANA and EXTPIN |
| 23:18 | GAINERRTRIM2V5          | RO     | Gain Error Trim Value for DAC main output using reference 2V5                |
| 17:12 | GAINERRTRIM1V25         | RO     | Gain Error Trim Value for DAC main output using reference 1V25               |
| 11:6  | GAINERRTRIM2V5LN        | RO     | Gain Error Trim Value for DAC main output using reference 2V5LN              |
| 5:0   | GAINERRTRIM1V25LN       | RO     | Gain Error Trim Value for DAC main output using reference 1V25LN             |

## 4.7.48 VDACC0ALTCAL - VDACC0 Cals for Alternate Path

| Offset | Bit Position |    |    |    |                            |    |    |    |    |                   |    |    |    |    |                    |    |    |    |    |    |                     |    |   |   |   |   |   |                      |    |   |   |   |
|--------|--------------|----|----|----|----------------------------|----|----|----|----|-------------------|----|----|----|----|--------------------|----|----|----|----|----|---------------------|----|---|---|---|---|---|----------------------|----|---|---|---|
| 0x188  | 31           | 30 | 29 | 28 | 27                         | 26 | 25 | 24 | 23 | 22                | 21 | 20 | 19 | 18 | 17                 | 16 | 15 | 14 | 13 | 12 | 11                  | 10 | 9 | 8 | 7 | 6 | 5 | 4                    | 3  | 2 | 1 | 0 |
| Access |              |    |    |    | RO                         |    |    |    |    | RO                |    |    |    |    |                    | RO |    |    |    |    |                     | RO |   |   |   |   |   |                      | RO |   |   |   |
| Name   |              |    |    |    | GAINERRTRIMVDDANAEXTPINALT |    |    |    |    | GAINERRTRIM2V5ALT |    |    |    |    | GAINERRTRIM1V25ALT |    |    |    |    |    | GAINERRTRIM2V5LNALT |    |   |   |   |   |   | GAINERRTRIM1V25LNALT |    |   |   |   |

| Bit   | Name                       | Access                         | Description   |
|-------|----------------------------|--------------------------------|---|
| 31:30 | <i>Reserved</i>            | <i>Reserved for future use</i> |   |
| 29:24 | GAINERRTRIMVDDANAEXTPINALT | RO                             | Gain Error Trim Value for DAC alternative output using references VDDANA and EXTPIN |
| 23:18 | GAINERRTRIM2V5ALT          | RO                             | Gain Error Trim Value for DAC alternative output using reference 2V5                |
| 17:12 | GAINERRTRIM1V25ALT         | RO                             | Gain Error Trim Value for DAC alternative output using reference 1V25               |
| 11:6  | GAINERRTRIM2V5LNALT        | RO                             | Gain Error Trim Value for DAC alternative output using reference 2V5LN              |
| 5:0   | GAINERRTRIM1V25LNALT       | RO                             | Gain Error Trim Value for DAC alternative output using reference 1V25LN             |

## 4.7.49 VDACC0CH1CAL - VDACC0 CH1 Error Cal

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |                 |    |    |    |                 |    |    |    |    |            |    |   |   |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|-----------------|----|----|----|-----------------|----|----|----|----|------------|----|---|---|---|---|---|---|---|---|---|---|
| 0x18C  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20              | 19 | 18 | 17 | 16              | 15 | 14 | 13 | 12 | 11         | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access |              |    |    |    |    |    |    |    |    |    |    | RO              |    |    |    | RO              |    |    |    |    | RO         |    |   |   |   |   |   |   |   |   |   |   |
| Name   |              |    |    |    |    |    |    |    |    |    |    | GAINERRTRIMCH1B |    |    |    | GAINERRTRIMCH1A |    |    |    |    | OFFSETTRIM |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name            | Access                         | Description   |
|-------|-----------------|--------------------------------|---|
| 31:12 | <i>Reserved</i> | <i>Reserved for future use</i> |   |
| 11:8  | GAINERRTRIMCH1B | RO                             | Gain Error Trim Value for Channel 1 for references 2V5LN, 2V5                   |
| 7:4   | GAINERRTRIMCH1A | RO                             | Gain Error Trim Value for Channel 1 for references 1V25LN, 1V25, VDDANA, EXTPIN |
| 3     | <i>Reserved</i> | <i>Reserved for future use</i> |   |
| 2:0   | OFFSETTRIM      | RO                             | Input Buffer Offset Calibration Value for all DAC references                    |

## 4.7.50 OPA0CAL0 - OPA0 Calibration Register for DRIVESTRENGTH 0, INCBW=1

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x190  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

## 4.7.51 OPA0CAL1 - OPA0 Calibration Register for DRIVESTRENGTH 1, INCBW=1

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |     |   |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|-----|---|
| 0x194  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1   | 0 |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   | RO  |   |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   | CM1 |   |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

## 4.7.52 OPA0CAL2 - OPA0 Calibration Register for DRIVESTRENGTH 2, INCBW=1

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x198  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

## 4.7.53 OPA0CAL3 - OPA0 Calibration Register for DRIVESTRENGTH 3, INCBW=1

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x19C  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

## 4.7.54 OPA1CAL0 - OPA1 Calibration Register for DRIVESTRENGTH 0, INCBW=1

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x1A0  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

## 4.7.55 OPA1CAL1 - OPA1 Calibration Register for DRIVESTRENGTH 1, INCBW=1

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |     |   |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|-----|---|
| 0x1A4  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1   | 0 |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   | RO  |   |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   | CM1 |   |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

## 4.7.56 OPA1CAL2 - OPA1 Calibration Register for DRIVESTRENGTH 2, INCBW=1

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x1A8  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

## 4.7.57 OPA1CAL3 - OPA1 Calibration Register for DRIVESTRENGTH 3, INCBW=1

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x1AC  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name     | Access | Description   |
|-------|----------|--------|---|
| 31    | Reserved |        | Reserved for future use                             |
| 30:26 | OFFSETN  | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | Reserved |        | Reserved for future use                             |
| 24:20 | OFFSETP  | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | Reserved |        | Reserved for future use                             |
| 18:17 | GM3      | RO     | Gm3 Trim Value                                      |
| 16    | Reserved |        | Reserved for future use                             |
| 15:13 | GM       | RO     | Gm Trim Value                                       |
| 12    | Reserved |        | Reserved for future use                             |
| 11:10 | CM3      | RO     | Compensation cap Cm3 trim value                     |
| 9     | Reserved |        | Reserved for future use                             |
| 8:5   | CM2      | RO     | Compensation cap Cm2 trim value                     |
| 4     | Reserved |        | Reserved for future use                             |
| 3:0   | CM1      | RO     | Compensation cap Cm1 trim value                     |

## 4.7.58 OPA2CAL0 - OPA2 Calibration Register for DRIVESTRENGTH 0, INCBW=1

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x1B0  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

## 4.7.59 OPA2CAL1 - OPA2 Calibration Register for DRIVESTRENGTH 1, INCBW=1

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x1B4  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

## 4.7.60 OPA2CAL2 - OPA2 Calibration Register for DRIVESTRENGTH 2, INCBW=1

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x1B8  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

## 4.7.61 OPA2CAL3 - OPA2 Calibration Register for DRIVESTRENGTH 3, INCBW=1

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x1BC  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

4.7.62 CSENGAINCAL - Cap Sense Gain Adjustment

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |         |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---------|---|---|---|---|---|---|---|
| 0x1C0  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RO      |   |   |   |   |   |   |   |
| Name   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | GAINCAL |   |   |   |   |   |   |   |

| Bit  | Name     | Access | Description   |
|------|----------|--------|---|
| 31:8 | Reserved |        | Reserved for future use   |
| 7:0  | GAINCAL  | RO     | Gain Adjustment for Cap Sense. Gain should be scaled by GAINCAL/128 |

## 4.7.63 OPA0CAL4 - OPA0 Calibration Register for DRIVESTRENGTH 0, INCBW=0

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x1D0  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

## 4.7.64 OPA0CAL5 - OPA0 Calibration Register for DRIVESTRENGTH 1, INCBW=0

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x1D4  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

## 4.7.65 OPA0CAL6 - OPA0 Calibration Register for DRIVESTRENGTH 2, INCBW=0

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x1D8  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

## 4.7.66 OPA0CAL7 - OPA0 Calibration Register for DRIVESTRENGTH 3, INCBW=0

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x1DC  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

## 4.7.67 OPA1CAL4 - OPA1 Calibration Register for DRIVESTRENGTH 0, INCBW=0

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x1E0  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

## 4.7.68 OPA1CAL5 - OPA1 Calibration Register for DRIVESTRENGTH 1, INCBW=0

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x1E4  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

## 4.7.69 OPA1CAL6 - OPA1 Calibration Register for DRIVESTRENGTH 2, INCBW=0

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x1E8  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

## 4.7.70 OPA1CAL7 - OPA1 Calibration Register for DRIVESTRENGTH 3, INCBW=0

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x1EC  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

## 4.7.71 OPA2CAL4 - OPA2 Calibration Register for DRIVESTRENGTH 0, INCBW=0

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x1F0  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

## 4.7.72 OPA2CAL5 - OPA2 Calibration Register for DRIVESTRENGTH 1, INCBW=0

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x1F4  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name            | Access                         | Description   |
|-------|-----------------|--------------------------------|---|
| 31    | <i>Reserved</i> | <i>Reserved for future use</i> |   |
| 30:26 | OFFSETN         | RO                             | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> | <i>Reserved for future use</i> |   |
| 24:20 | OFFSETP         | RO                             | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> | <i>Reserved for future use</i> |   |
| 18:17 | GM3             | RO                             | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> | <i>Reserved for future use</i> |   |
| 15:13 | GM              | RO                             | Gm Trim Value                                       |
| 12    | <i>Reserved</i> | <i>Reserved for future use</i> |   |
| 11:10 | CM3             | RO                             | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> | <i>Reserved for future use</i> |   |
| 8:5   | CM2             | RO                             | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> | <i>Reserved for future use</i> |   |
| 3:0   | CM1             | RO                             | Compensation cap Cm1 trim value                     |

## 4.7.73 OPA2CAL6 - OPA2 Calibration Register for DRIVESTRENGTH 2, INCBW=0

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x1F8  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

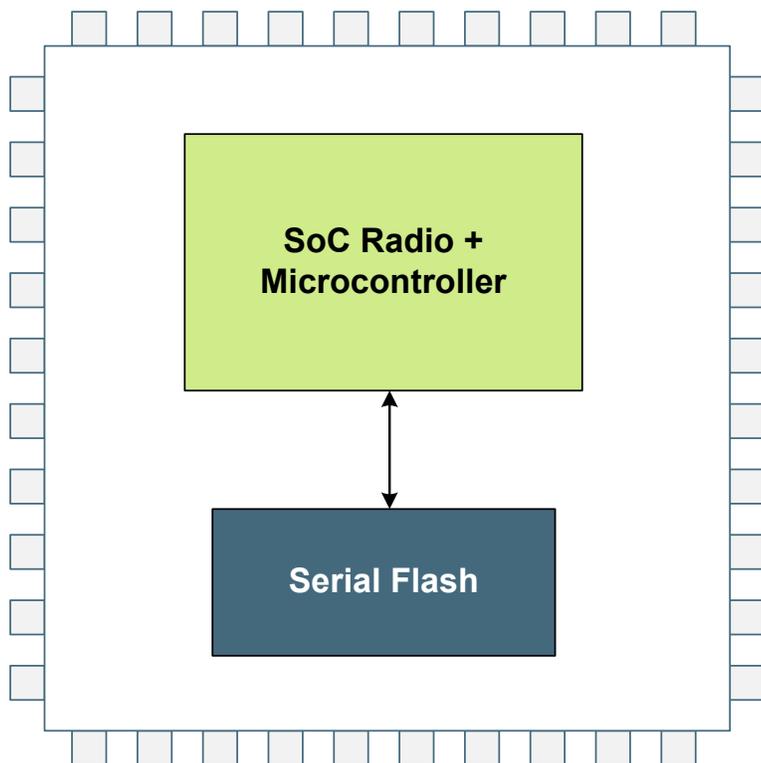
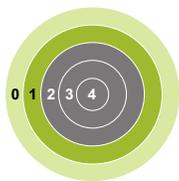
| Bit   | Name            | Access | Description   |
|-------|-----------------|--------|---|
| 31    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 30:26 | OFFSETN         | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 24:20 | OFFSETP         | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 18:17 | GM3             | RO     | Gm3 Trim Value                                      |
| 16    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 15:13 | GM              | RO     | Gm Trim Value                                       |
| 12    | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 11:10 | CM3             | RO     | Compensation cap Cm3 trim value                     |
| 9     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 8:5   | CM2             | RO     | Compensation cap Cm2 trim value                     |
| 4     | <i>Reserved</i> |        | <i>Reserved for future use</i>                      |
| 3:0   | CM1             | RO     | Compensation cap Cm1 trim value                     |

## 4.7.74 OPA2CAL7 - OPA2 Calibration Register for DRIVESTRENGTH 3, INCBW=0

| Offset | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |    |    |    |    |     |   |   |   |     |   |   |   |   |   |     |  |
|--------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|----|----|----|----|-----|---|---|---|-----|---|---|---|---|---|-----|--|
| 0x1FC  | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6   | 5 | 4 | 3 | 2 | 1 | 0   |  |
| Access |              |    |    | RO      |    |    |    |    |    | RO      |    |    |    | RO  |    |    |    | RO |    |    |    | RO  |   |   |   | RO  |   |   |   |   |   | RO  |  |
| Name   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM |    |    |    | CM3 |   |   |   | CM2 |   |   |   |   |   | CM1 |  |

| Bit   | Name     | Access | Description   |
|-------|----------|--------|---|
| 31    | Reserved |        | Reserved for future use                             |
| 30:26 | OFFSETN  | RO     | OPA Inverting Input Offset Configuration Value.     |
| 25    | Reserved |        | Reserved for future use                             |
| 24:20 | OFFSETP  | RO     | OPA Non-Inverting Input Offset Configuration Value. |
| 19    | Reserved |        | Reserved for future use                             |
| 18:17 | GM3      | RO     | Gm3 Trim Value                                      |
| 16    | Reserved |        | Reserved for future use                             |
| 15:13 | GM       | RO     | Gm Trim Value                                       |
| 12    | Reserved |        | Reserved for future use                             |
| 11:10 | CM3      | RO     | Compensation cap Cm3 trim value                     |
| 9     | Reserved |        | Reserved for future use                             |
| 8:5   | CM2      | RO     | Compensation cap Cm2 trim value                     |
| 4     | Reserved |        | Reserved for future use                             |
| 3:0   | CM1      | RO     | Compensation cap Cm1 trim value                     |

## 5. Serial Flash



### Quick Facts

#### What?

A 512 kB serial flash memory is included in the package for certain part numbers.

#### Why?

The serial flash memory extends the non-volatile storage capabilities of the device while maintaining a small PCB footprint.

#### How?

The serial flash may be read and written in EM0 or EM1, and placed in a low power state when not used.

### 5.1 Introduction

The serial flash memory adds 512 kB of non-volatile storage space for applications with larger memory requirements. It is fully internal to the package, and requires no additional board space or GPIO resources. Software drivers provided by Silicon Labs offer a simple API interface to the serial flash. Low-level access is also possible, via the USART1 peripheral.

### 5.2 Features

- 512 kB of memory
- 4 kB sectors, can be erased individually or in 32 kB or 64 kB blocks
- 1 - 256 byte page write
- 100,000 write/erase cycle endurance
- 20 year data retention
- SPI interface
- Write protection
- 4 x 256 byte dedicated security area with user-lockable bits, one-time programmable

### 5.3 Functional Description

The serial flash is powered from IOVDD and bonded to internal GPIO which are not available externally. USART1 is connected to the associated GPIO pins and functions as a SPI interface to the flash. It is recommended to use the software libraries supplied by Silicon Laboratories for interfacing to the serial flash. The information in this section is reference for users who choose to write their own low-level software drivers.

**Note:** The [EXTINFO](#) entry in the DI page identifies the specific serial flash part number included in the package. Software should verify this field before initiating any serial flash operations.

### 5.3.1 Memory Organization

The memory array of the serial flash is divided into uniform 4 kB sectors or uniform 32/64 kB blocks consisting of eight or sixteen adjacent sectors, respectively. [Table 5.1 Block and Sector Addresses on page 130](#) diagrams the organization of this memory space.

**Table 5.1. Block and Sector Addresses**

| 64 kB Block Number | 32 kB Block Number | 4 kB Sector Number  | Address Range       |
|--------------------|--------------------|---------------------|---------------------|
| 0                  | 0                  | 0                   | 0x000000 - 0x000FFF |
|                    |                    | :                   | :                   |
|                    | 1                  | :                   | :                   |
| 1                  | 2                  | 15                  | 0x00F000 - 0x00FFFF |
|                    |                    | :                   | :                   |
|                    | 3                  | :                   | :                   |
| 2                  | 4                  | 16                  | 0x010000 - 0x010FFF |
|                    |                    | :                   | :                   |
|                    | 31                 | 0x01F000 - 0x01FFFF |                     |
| 3                  | 6                  | 32                  | 0x020000 - 0x020FFF |
|                    |                    | :                   | :                   |
|                    | 47                 | 0x02F000 - 0x02FFFF |                     |
| 4                  | 8                  | 48                  | 0x030000 - 0x030FFF |
|                    |                    | :                   | :                   |
|                    | 63                 | 0x03F000 - 0x03FFFF |                     |
| 5                  | 10                 | 64                  | 0x040000 - 0x040FFF |
|                    |                    | :                   | :                   |
|                    | 79                 | 0x04F000 - 0x04FFFF |                     |
| 6                  | 12                 | 80                  | 0x050000 - 0x050FFF |
|                    |                    | :                   | :                   |
|                    | 95                 | 0x05F000 - 0x05FFFF |                     |
| 7                  | 14                 | 96                  | 0x060000 - 0x060FFF |
|                    |                    | :                   | :                   |
|                    | 111                | 0x06F000 - 0x06FFFF |                     |
| 8                  | 16                 | 112                 | 0x070000 - 0x070FFF |
|                    |                    | :                   | :                   |
|                    | 127                | 0x07F000 - 0x07FFFF |                     |

### 5.3.2 Serial Interface

Serial flash operations are controlled through a SPI interface on the flash. Internal to the package, the flash interface I/O are connected to GPIO on the MCU. USART1 may be routed to the serial interface for hardware-controlled bus writes and reads.

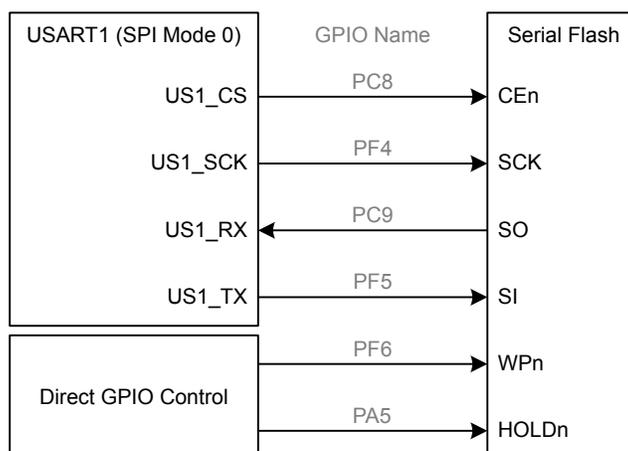


Figure 5.1. Serial Flash Connections

#### 5.3.2.1 USART1 Configuration

All of the serial flash I/O connections are bonded to standard port pins internal to the packaging. The USART1 peripheral may be directly routed to the SPI interface signals (SI, SO, SCK, and CEn), while the remaining signals (WPn and HOLDn) can be controlled as GPIO. [Table 5.2 Serial Flash I/O Connections on page 131](#) shows the GPIO connections for each signal, as well as the recommended GPIO configurations and USART1 routing locations.

Table 5.2. Serial Flash I/O Connections

| Serial Flash Signal            | GPIO | Recommended Configuration and initial state | USART1_ROUTELOC0 Settings |
|--------------------------------|------|---|---------------------------|
| SI (Serial Data Input)         | PF5  | Output, High                                | TXLOC = LOC29             |
| WPn (Active-Low Write Protect) | PF6  | Output, Low                                 | n/a                       |
| SCK (Serial Clock Input)       | PF4  | Output, Low                                 | CLKLOC = LOC26            |
| HOLDn (Active-Low Hold)        | PA5  | Output, High                                | n/a                       |
| SO (Serial Data Output)        | PC9  | Input                                       | RXLOC = LOC13             |
| CEn (Active-Low Chip Enable)   | PC8  | Output, High                                | CSLOC = LOC10             |

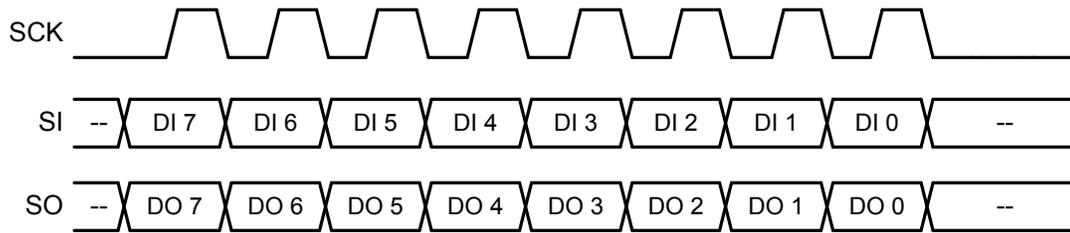
To function properly with the serial flash, USART1 should be configured for synchronous master operation in SPI mode 0, with a maximum baud rate of 8 MHz. The CEn pin may be controlled manually by software, or automatically by the US1\_CS pin. If using the US1\_CS option, the CS output signal should be configured for active-low operation.

If CEn is controlled manually as a GPIO pin, it should be cleared to a logic low state by software before any data transfer is initiated, and set back to logic high after the final byte of data has been transferred. If US1\_CS is configured to automatically drive the CEn pin, software or DMA must continue to keep the USART1 buffer full for the duration of each transfer so that CEn remains low during the operation and returns high only when data transfer is complete.

Refer to [19. USART - Universal Synchronous Asynchronous Receiver/Transmitter](#) for more detailed information about USART operation and configuration.

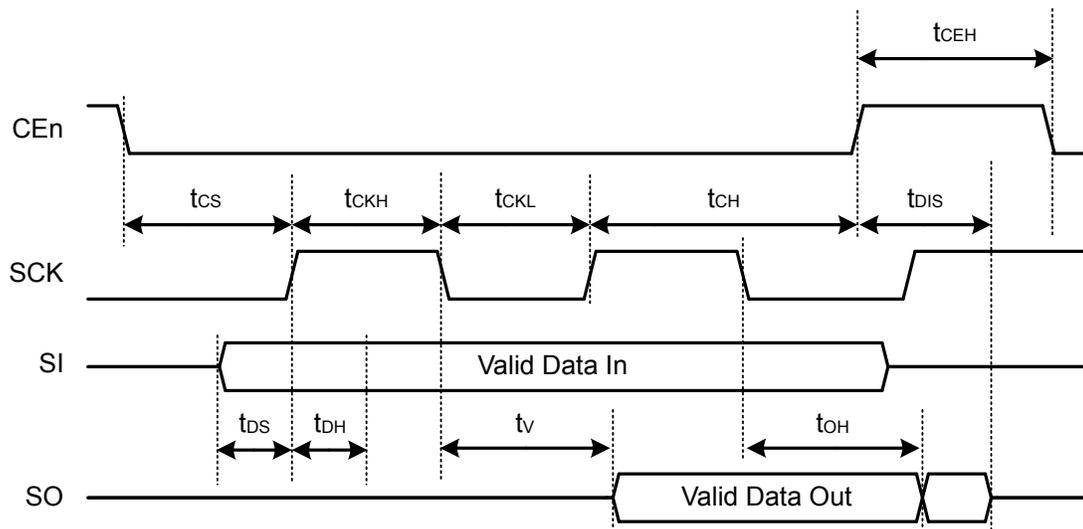
### 5.3.2.2 Timing

All data is shifted into and out of the serial flash MSB-first. Data is shifted on the falling edge of SCK and latched on the rising edge of SCK. Transfer format for a single byte is shown in [Figure 5.2 Serial Interface Data Format on page 132](#).



**Figure 5.2. Serial Interface Data Format**

When USART1 is configured as described in [5.3.2.1 USART1 Configuration](#), at no greater than an 8 MHz serial clock rate and automatic US1\_CS control, all serial flash timing parameters for CEn, SCK, SI, and SO will be met across the temperature and supply range. This is the recommended configuration for communicating with the serial flash memory. For other configurations, it is important to ensure that the serial flash timing is not violated. Refer to [Figure 5.3 Serial Flash IO Timing on page 132](#).



**Figure 5.3. Serial Flash IO Timing**

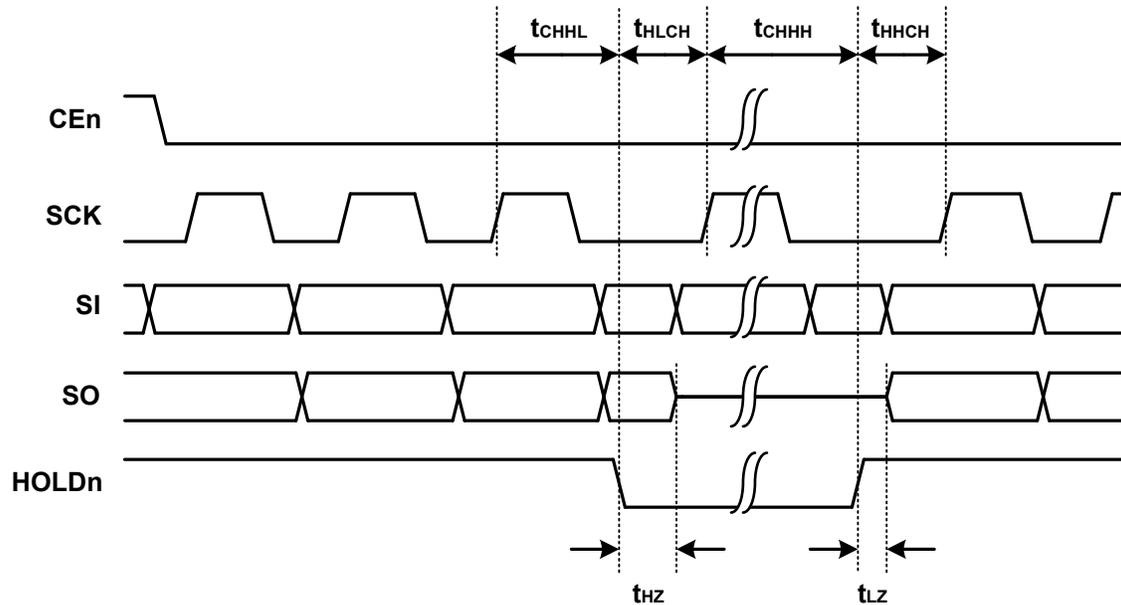
| Parameter          | Symbol    | Min | Max | Units |
|--------------------|-----------|-----|-----|-------|
| SCK High Time      | $t_{CKH}$ | 4   |     | ns    |
| SCK Low Time       | $t_{CKL}$ | 4   |     | ns    |
| CEn High Time      | $t_{CEH}$ | 7   |     | ns    |
| CEn Setup Time     | $t_{CS}$  | 10  |     | ns    |
| CEn Hold Time      | $t_{CH}$  | 5   |     | ns    |
| Data In Setup Time | $t_{DS}$  | 2   |     | ns    |
| Data In Hold Time  | $t_{DH}$  | 2   |     | ns    |
| Output Valid       | $t_v$     |     | 8   | ns    |
| Output Hold Time   | $t_{OH}$  | 2   |     | ns    |

| Parameter           | Symbol    | Min | Max | Units |
|---------------------|-----------|-----|-----|-------|
| Output Disable Time | $t_{DIS}$ |     | 8   | ns    |

### 5.3.2.3 Hold Operation

When the device is selected with  $CEN$  and a serial sequence is underway,  $HOLDn$  can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, bring the  $HOLDn$  signal low while the  $SCK$  signal is low. When  $HOLDn$  is asserted, inputs to  $SI$  will be ignored, and  $SO$  will be high impedance. To resume serial communication, bring  $HOLDn$  high while the  $SCK$  signal is low. Communication with the serial flash will resume at the clock where it was halted.

Figure 5.4. Serial Flash  $HOLDn$  Timing

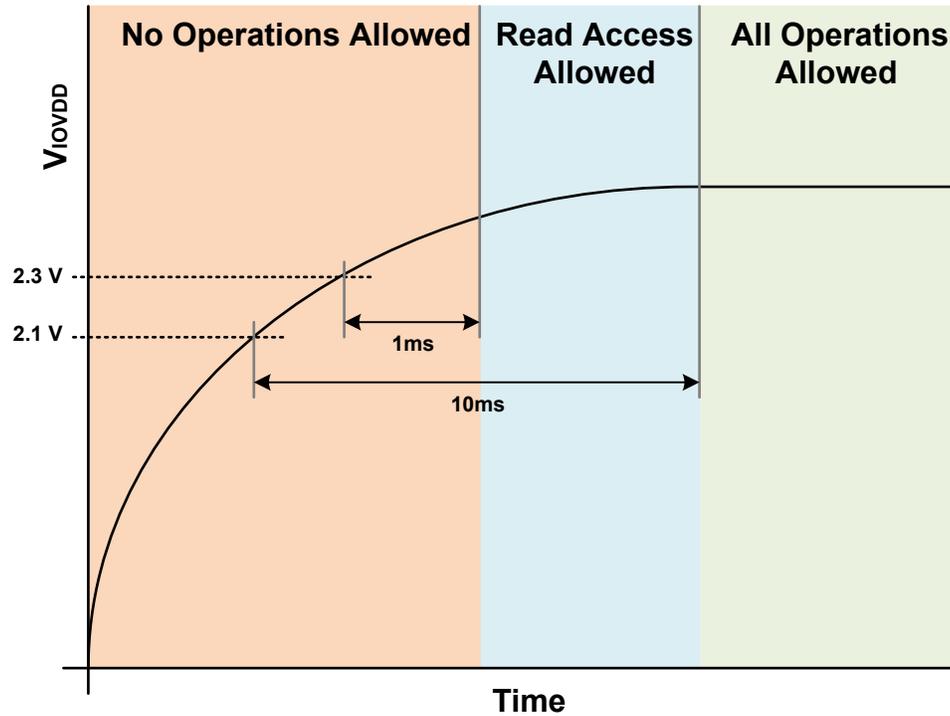


| Parameter                     | Symbol     | Min | Max | Units |
|-------------------------------|------------|-----|-----|-------|
| $HOLDn$ Low to SCK            | $t_{HLCH}$ | 5   |     | ns    |
| SCK to $HOLDn$ High           | $t_{CHHH}$ | 5   |     | ns    |
| $HOLDn$ High to SCK           | $t_{HHCH}$ | 5   |     | ns    |
| SCK to $HOLDn$ Low            | $t_{CHHL}$ | 5   |     | ns    |
| $HOLDn$ Low to Output High-Z  | $t_{HZ}$   |     | 12  | ns    |
| $HOLDn$ High to Output Driven | $t_{LZ}$   |     | 12  | ns    |

### 5.3.2.4 Power Up and Power Down

The serial flash is powered by the IOVDD supply pin, and will inhibit certain operations while it is powering on. Software should not attempt to access the serial flash for at least 1 ms after IOVDD reaches 2.3 V. Additionally, program and erase operations will be rejected for up to 10 ms from the time IOVDD reaches 2.1 V. All program and erase operations are inhibited if the IOVDD supply voltage drops below 2.1 V.

Figure 5.5. Serial Flash Power Up



### 5.3.3 Instruction Set

The serial flash utilizes an 8-bit instruction register. See [Table 5.3 Instruction Set Summary on page 135](#) for details on instructions and instruction codes. All instructions, addresses, and data are shifted in with the most significant bit (MSB) first on the Serial Data Input (SI). The input data on SI is latched on the rising edge of Serial Clock (SCK) after Chip Enable (CEn) is driven low. Every instruction sequence starts with a one-byte instruction code and is followed by address bytes, data bytes, or both address bytes and data bytes, depending on the type of instruction. CEn must be driven high after the last bit of the instruction sequence has been shifted in to end the operation.

**Table 5.3. Instruction Set Summary**

| Name      | Instruction Code | Operation               | Available During Suspend |
|-----------|------------------|-------------------------|--------------------------|
| RD        | 0x03             | Read Data               | Yes                      |
| FR        | 0x0B             | Fast Read Data          | Yes                      |
| PP        | 0x02             | Page Program            | No                       |
| SER       | 0xD7 / 0x20      | Sector Erase            | No                       |
| BER32     | 0x52             | Block Erase 32 kB       | No                       |
| BER64     | 0xD8             | Block Erase 64 kB       | No                       |
| CER       | 0xC7 / 0x60      | Chip Erase              | No                       |
| WREN      | 0x06             | Write Enable            | No                       |
| WRDI      | 0x04             | Write Disable           | No                       |
| RDSR      | 0x05             | Read Status Register    | Yes                      |
| WRSR      | 0x01             | Write Status Register   | No                       |
| RDFR      | 0x48             | Read Function Register  | Yes                      |
| WRFR      | 0x42             | Write Function Register | No                       |
| PERSUS    | 0x75 / 0xB0      | Program/Erase Suspend   | No                       |
| PERRSM    | 0x7A / 0x30      | Program/Erase Resume    | Yes                      |
| DP        | 0xB9             | Deep Power Down         | No                       |
| RDUID     | 0x4B             | Read Unique ID          | Yes                      |
| RSTEN     | 0x66             | Reset Enable            | Yes                      |
| RST       | 0x99             | Reset                   | Yes                      |
| IRP       | 0x62             | Program Information Row | No                       |
| IRRD      | 0x68             | Read Information Row    | Yes                      |
| SECUNLOCK | 0x26             | Sector Unlock           | No                       |
| SECLOCK   | 0x24             | Sector Lock             | No                       |

### 5.3.4 Registers

The serial flash has two 8-bit registers to communicate status and apply write protection to different regions of the memory array, the STATUS register and the FUNCTION register.

The STATUS register is read with the RDSR command and written with the WRSR command. The FUNCTION register is read with the RDFR command and written with the WRFR command.

**STATUS - Serial Flash Status Register**

| Bit     | 7                   | 6                   | 5                   | 4 | 3 | 2 | 1             | 0             |
|---------|---------------------|---------------------|---------------------|---|---|---|---------------|---------------|
| Default | 0                   | 0                   | 0x0                 |   |   |   | 0             | 0             |
| Access  | R/W<br>Non-Volatile | R/W<br>Non-Volatile | R/W<br>Non-Volatile |   |   |   | R<br>Volatile | R<br>Volatile |
| Name    | SRWD                | Reserved            | BP                  |   |   |   | WEL           | WIP           |

| Bit | Name            | Default                                      | Access              | Description  |
|-----|-----------------|--|---------------------|--|
| 7   | SRWD            | 0  | R/W<br>Non-Volatile | <p><b>Status Register Write Disable.</b></p> <p>The SRWD bit operates in conjunction with the Write Protection (WPn) signal to provide a hardware protection mode. When SRWD is cleared to 0, the STATUS register is not write-protected. When SRWD is set to 1 and WPn is pulled low, the STATUS register becomes read-only, and any WRSR instruction will be ignored. If SRWD is set to 1 and WPn is pulled high, the STATUS register can be changed by a WRSR instruction.</p>  |
| 6   | <i>Reserved</i> | <i>This bit must always be written to 0.</i> |                     |  |
| 5:2 | BP              | 0x0  | R/W<br>Non-Volatile | <p><b>Block Protection.</b></p> <p>The Block Protection field is used to define the portion of the memory area to be protected. Refer to <a href="#">Table 5.4 64 kB Block Write Protection on page 145</a> for the Block Protection (BP) settings. When a defined value of BP is set, the corresponding area of serial flash memory is protected. Any program or erase operation to that area will be inhibited. A Chip Erase (<a href="#">CER</a>) instruction will be ignored unless BP is 0x0.</p>   |
| 1   | WEL             | 0  | R<br>Volatile       | <p><b>Write Enable Latch.</b></p> <p>WEL indicates the status of the internal write enable latch. When WEL is 0, the write enable latch is disabled and all write or erase operations are inhibited. When WEL is 1, write operations are allowed. The WEL bit is set by a Write Enable (<a href="#">WREN</a>) instruction. Each STATUS or FUNCTION register write, program, or erase instruction must be preceded by a WREN instruction. The WEL bit can be reset by software a Write Disable (<a href="#">WRDI</a>) instruction. It will automatically be reset after the completion of any write or erase operation.</p> |
| 0   | WIP             | 0  | R<br>Volatile       | <p><b>Write In Progress.</b></p> <p>WIP indicates the progress or completion of a program or erase operation. When the WIP bit is 0, the serial flash will accept any new register write, program, or erase operation. When WIP is 1, the serial flash is busy, and new register write, program, and erase instructions will be ignored.</p>   |

**FUNCTION - Serial Flash Function Register**

| Bit     | 7          | 6          | 5          | 4          | 3             | 2             | 1        | 0 |
|---------|------------|------------|------------|------------|---------------|---------------|----------|---|
| Default | 0          | 0          | 0          | 0          | 0             | 0             | 0x0      |   |
| Access  | R/W<br>OTP | R/W<br>OTP | R/W<br>OTP | R/W<br>OTP | R<br>Volatile | R<br>Volatile | R        |   |
| Name    | IRL3       | IRL2       | IRL1       | IRL0       | ESUS          | PSUS          | Reserved |   |

| Bit | Name     | Default                     | Access        | Description  |
|-----|----------|-----------------------------|---------------|--|
| 7   | IRL3     | 0                           | R/W<br>OTP    | <b>Information Row 3 Lock.</b><br><br>This bit is used to lock information row 3. When set to 1, information row 3 cannot be programmed. This bit is one-time programmable (OTP). Once it is set to 1, it cannot be modified.                          |
| 6   | IRL2     | 0                           | R/W<br>OTP    | <b>Information Row 2 Lock.</b><br><br>This bit is used to lock information row 2. When set to 1, information row 2 cannot be programmed. This bit is one-time programmable (OTP). Once it is set to 1, it cannot be modified.                          |
| 5   | IRL1     | 0                           | R/W<br>OTP    | <b>Information Row 1 Lock.</b><br><br>This bit is used to lock information row 1. When set to 1, information row 1 cannot be programmed. This bit is one-time programmable (OTP). Once it is set to 1, it cannot be modified.                          |
| 4   | IRL0     | 0                           | R/W<br>OTP    | <b>Information Row 0 Lock.</b><br><br>This bit is used to lock information row 0. When set to 1, information row 0 cannot be programmed. This bit is one-time programmable (OTP). Once it is set to 1, it cannot be modified.                          |
| 3   | ESUS     | 0                           | R<br>Volatile | <b>Erase Suspend.</b><br><br>ESUS indicates when an erase operation has been suspended. The ESUS bit is 1 after a suspend command is issued during any erase operation. Once the suspended erase operation resumes, the ESUS bit is reset to 0.        |
| 2   | PSUS     | 0                           | R<br>Volatile | <b>Program Suspend.</b><br><br>PSUS indicates when a program operation has been suspended. The PSUS bit is 1 after a suspend command is issued during any program operation. Once the suspended program operation resumes, the PSUS bit is reset to 0. |
| 1:0 | Reserved | These bits always read 0x0. |               |  |

#### 5.3.4.1 Read Status Register (RDSR, 0x05)

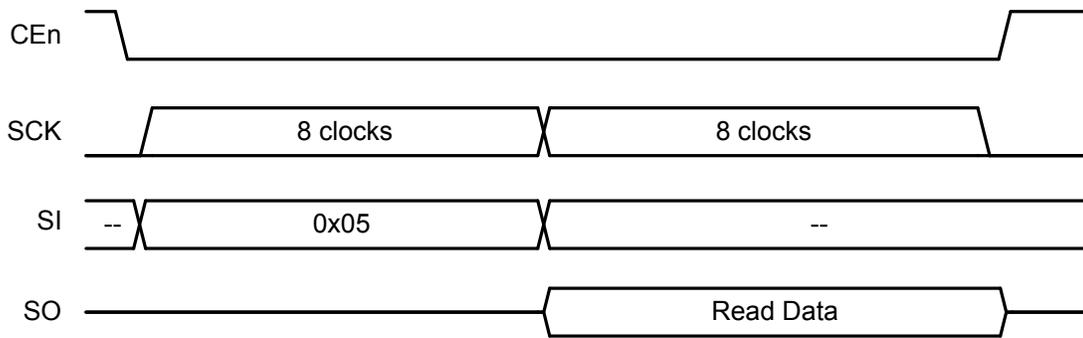


Figure 5.6. RDSR Instruction Format

#### 5.3.4.2 Write Status Register (WRSR, 0x01)

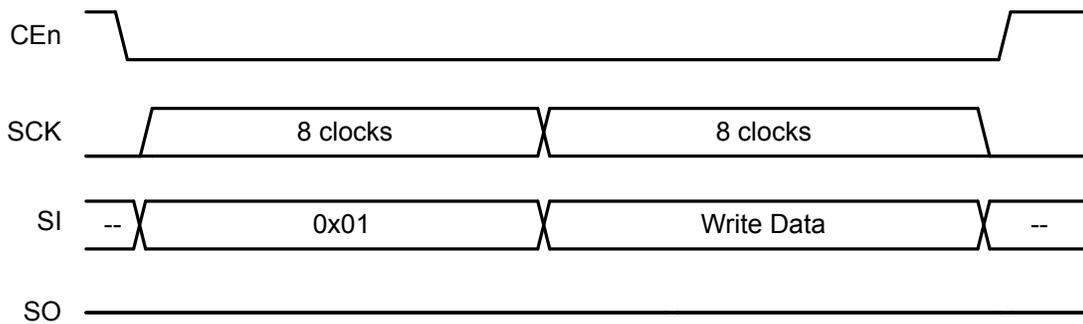


Figure 5.7. WRSR Instruction Format

#### 5.3.4.3 Read Function Register (RDFR, 0x48)

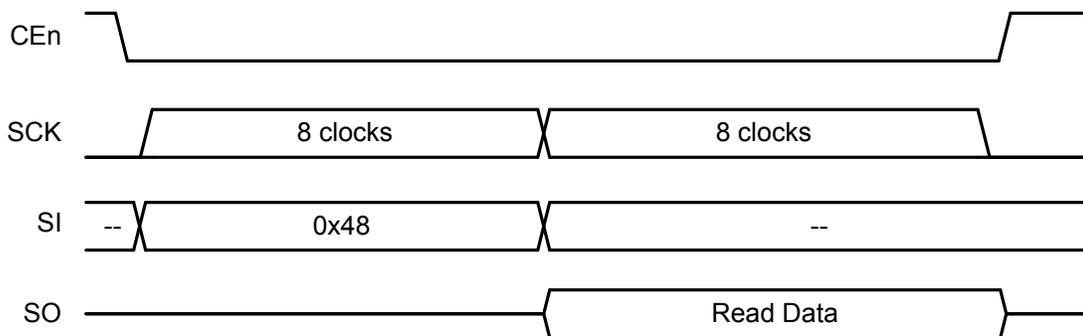


Figure 5.8. RDFR Instruction Format

### 5.3.4.4 Write Function Register (WRFR, 0x42)

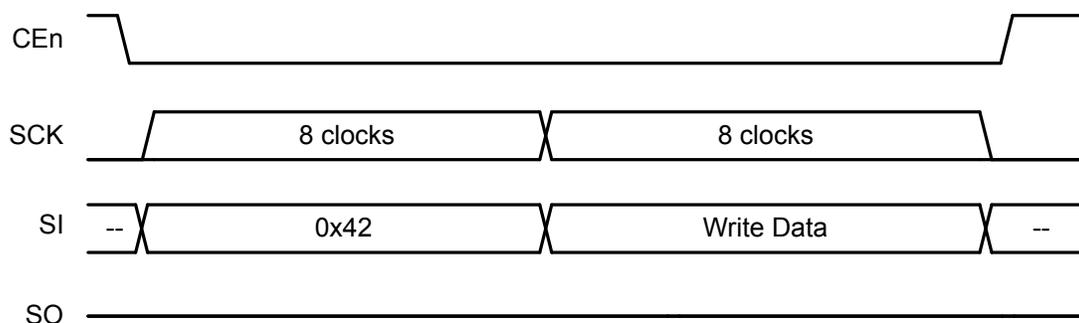


Figure 5.9. WRFR Instruction Format

### 5.3.5 Reading Memory

Reads of the serial flash memory space are performed with either the Read Data (RD) or Fast Read (FR) instruction. The Fast Read command is intended to allow for higher serial clock frequencies to be used for reading the serial flash data. In this co-packaged configuration however, both commands are limited to the overall maximum SCK rate of 8 MHz, and either may be used to read flash contents.

To initiate a memory read using the RD instruction, software should send the RD instruction code (one byte), followed by the first memory location to be read (three bytes, MSB-first). Data will be shifted out of the serial flash beginning with the next serial clock.

To initiate a memory read using the FR instruction, software should send the FR instruction code (one byte), followed by the first memory location to be read (three bytes, MSB-first), followed by a dummy byte (one byte). Data will be shifted out of the serial flash beginning with the next serial clock.

Data is shifted out on the SO line, MSB first. Any number of bytes can be read out in one RD or FR instruction. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to 0x000000, allowing the entire memory to be read in one continuous instruction. The operation is terminated when CEn is driven high.

If an RD or FR instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effect on the current operation.

#### 5.3.5.1 Read Data (RD, 0x03)

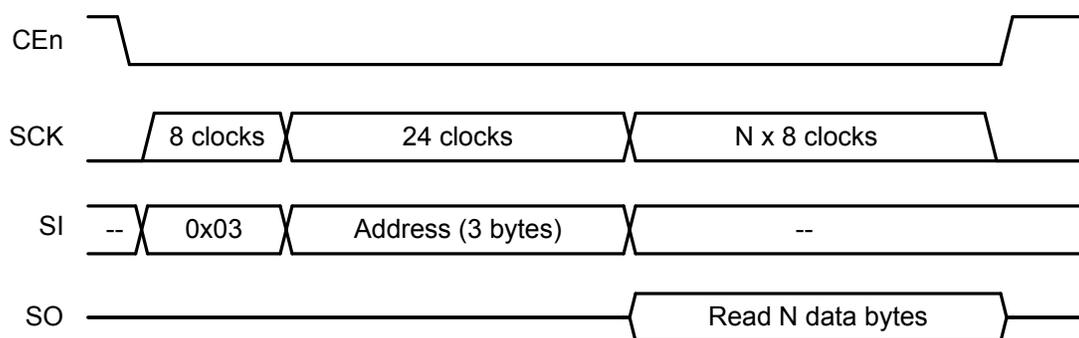


Figure 5.10. RD Instruction Format

### 5.3.5.2 Fast Read Data (FR, 0x0B)

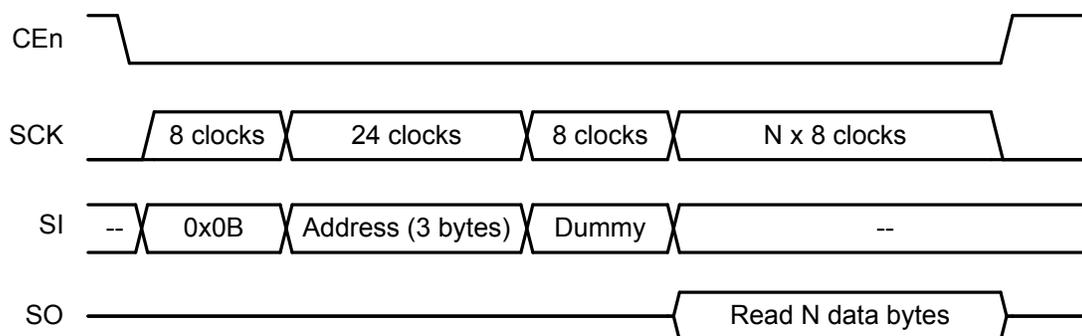


Figure 5.11. FR Instruction Format

### 5.3.6 Programming and Erasing Memory

The serial flash memory can be programmed (clearing bits to 0) in 1 to 256-byte pages. The entire 512 kB memory array may be erased (setting bits to 1) with a single command, or memory may be erased in defined 4 kB, 32 kB, or 64 kB blocks. Program or erase operations (other than full chip erase) may be suspended and resumed as needed in order to allow time-critical read operations.

**Note:** A program operation changes 1's to 0's in the flash memory array. An erase operation is required to change 0's to 1's. A byte cannot be reprogrammed with new information without first erasing the whole sector or block.

#### Programming Sequence

The Page Program instruction allows up to 256 bytes data to be programmed into memory in a single operation. The procedure to program data bytes is as follows:

1. Set the Write Enable Latch (WEL) by sending a Write Enable ([WREN](#)) instruction.
2. Send the Page Program ([PP](#)) instruction code (one byte), followed by the first memory location to be programmed (three bytes, MSB-first), and then shift the data to be programmed (1 to 256 bytes) into the flash.
3. Send Read Status Register ([RDSR](#)) instructions to the device to poll the STATUS register until the WIP bit is 0.

The write operation will start immediately after CEn is brought high in step 2. The PP instruction will not be executed until CEn goes high. The internal control logic automatically handles programming voltages and timing. During a program operation, the WIP bit in STATUS will be set to 1 and all instructions will be ignored except the RDSR instruction and the PERSUS instruction. Upon completion of the program operation, the Write Enable Latch (WEL) will also be cleared.

The starting byte can be anywhere within the page. When the end of the page is reached during a PP instruction (address ends in 0xFF), the address counter rolls over to the beginning of the page. If more than 256 bytes are received during a PP instruction, only the last 256 bytes received are programmed into the page. If the data to be programmed are less than a full page, the data of all other bytes on the same page will remain unchanged.

**Note:** The destination of the memory to be programmed must be outside the protected memory area set by the BP field in the STATUS register. Any PP instruction which attempts to program into a page that is write-protected will be ignored, unless the sector containing that page has been unlocked with a SECUNLOCK instruction.

## Erase Sequence

The memory array of the serial flash is organized into uniform 4Kbyte sectors or 32/64Kbyte uniform blocks (a block consists of eight/sixteen adjacent sectors respectively). Before a byte is reprogrammed, the sector or block that contains the byte must be erased (erasing sets bits to 1). In order to erase the serial flash, there are four erase instructions available: Sector Erase (**SER**), 32 kB Block Erase (**BER32**), 64 kB Block Erase (**BER64**) and Chip Erase (**CER**). A sector erase operation allows any individual sector to be erased without affecting the data in other sectors. A block erase operation erases any individual block. A chip erase operation erases the whole memory array of the serial flash.

To perform a sector or block erase:

1. Set the Write Enable Latch (WEL) by sending a Write Enable (**WREN**) instruction.
2. Send the SER, BER32 or BER64 instruction code (one byte), followed by the first address of the sector or block to be erased (three bytes, MSB-first).
3. Send Read Status Register (**RDSR**) instructions to the device to poll the STATUS register until the WIP bit is 0.

To perform a chip erase:

1. Set the Write Enable Latch (WEL) by sending a Write Enable (**WREN**) instruction.
2. Send the CER instruction code.
3. Send Read Status Register (**RDSR**) instructions to the device to poll the STATUS register until the WIP bit is 0.

The erase operation will start immediately after CEn is brought high for the erase instruction. The internal control logic automatically handles erase voltages and timing. During an erase operation, the WIP bit in STATUS will be set to 1 and all instructions will be ignored except the RDSR instruction and the PERSUS instruction. Upon completion of the erase operation, the Write Enable Latch (WEL) will also be cleared.

**Note:** The destination of the memory to be erased must be outside the protected memory area set by the BP field in the STATUS register. Any erase instruction which attempts to program into an area that is write-protected will be ignored, unless the sectors to be erased have been unlocked with a SECUNLOCK instruction. For a chip erase operation to execute, the entire memory array must be unlocked according to the BP field.

### 5.3.6.1 Program/Erase Suspend and Resume

The device allows the interruption of SER, BER32, BER64, and PP operations to conduct other operations. To suspend a program or erase operation, the Program/Erase Suspend (**PERSUS**) instruction is used. When the PERSUS instruction is issued, the serial flash will suspend the program or erase operation within a maximum of 100  $\mu$ s after CEn is driven high. The WIP bit in the STATUS register may also be polled by software to determine when the flash is ready to accept new commands. When a program or erase operation is suspended, the flash will respond to a limited set of other operations. Details on which instructions are allowed during suspend are found in [Table 5.3 Instruction Set Summary on page 135](#).

When a program operation has been suspended, the PSUS bit in the FUNCTION register will read back 1. If an erase operation has been suspended, the ESUS bit in the FUNCTION register will read back 1.

To resume the suspended program or erase operation, the Program/Erase Resume (**PERRSM**) operation is used. When the PERRSM instruction is issued, the serial flash will resume the program or erase operation after CEn is driven high. The WIP bit in the STATUS register may be polled by software to determine when the program or erase operation is complete.

**Note:** If multiple suspend/resume operations are used, software must wait for a minimum of 400  $\mu$ s after sending a resume command before initiating a new suspend operation.

### 5.3.6.2 Write Enable (WREN, 0x06)

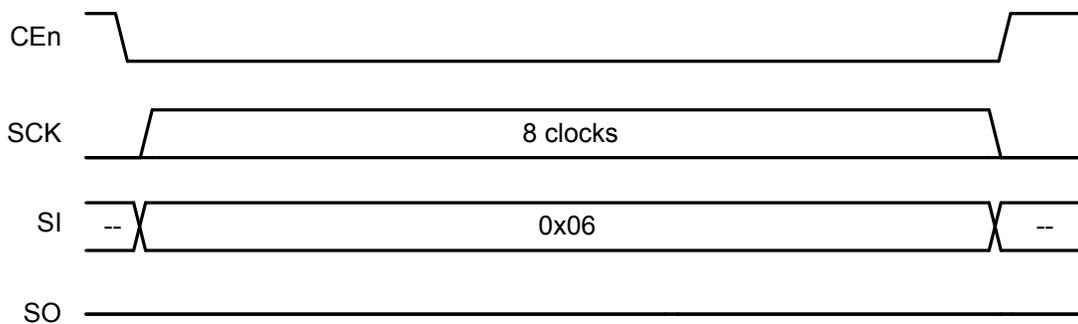


Figure 5.12. WREN Instruction Format

### 5.3.6.3 Write Disable (WRDI, 0x04)

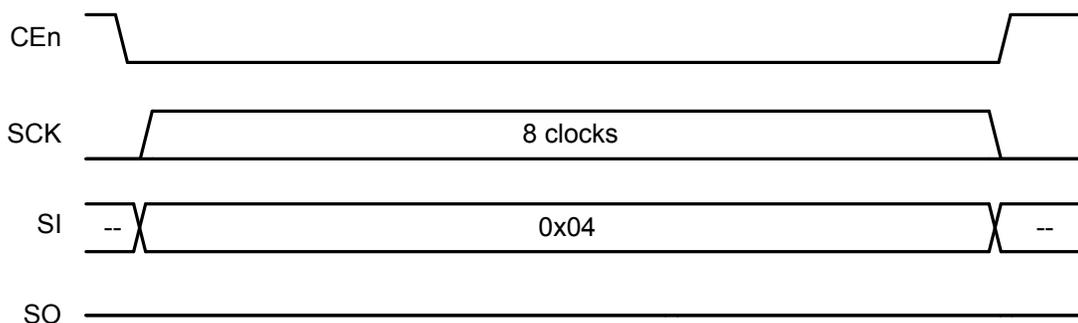


Figure 5.13. WRDI Instruction Format

### 5.3.6.4 Page Program (PP, 0x02)

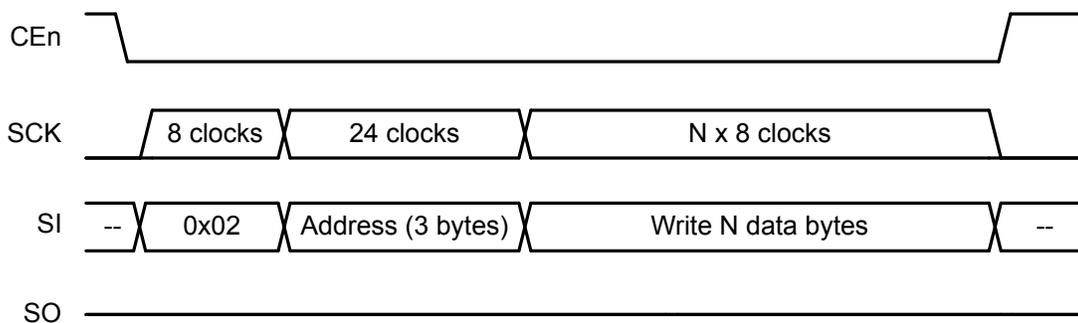


Figure 5.14. PP Instruction Format

### 5.3.6.5 Sector Erase (SER, 0xD7 / 0x20)

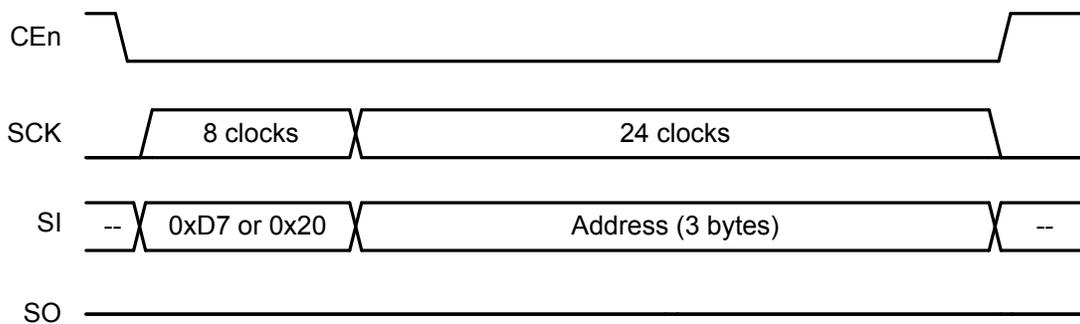


Figure 5.15. SER Instruction Format

### 5.3.6.6 Block Erase 32k (BER32, 0x52)

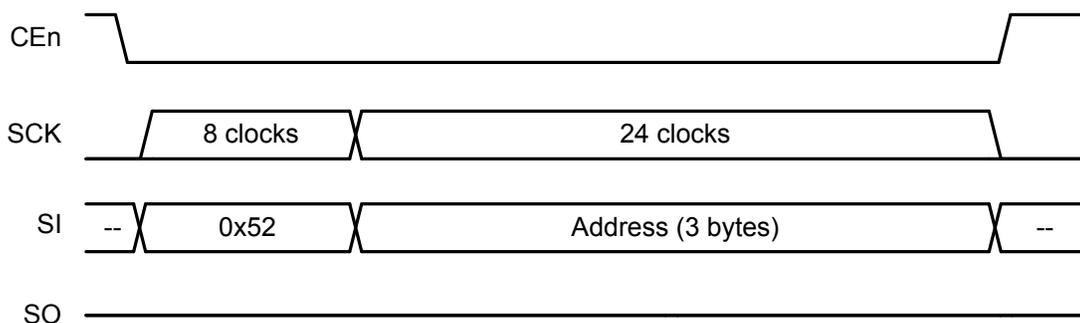


Figure 5.16. BER32 Instruction Format

### 5.3.6.7 Block Erase 64k (BER64, 0xD8)

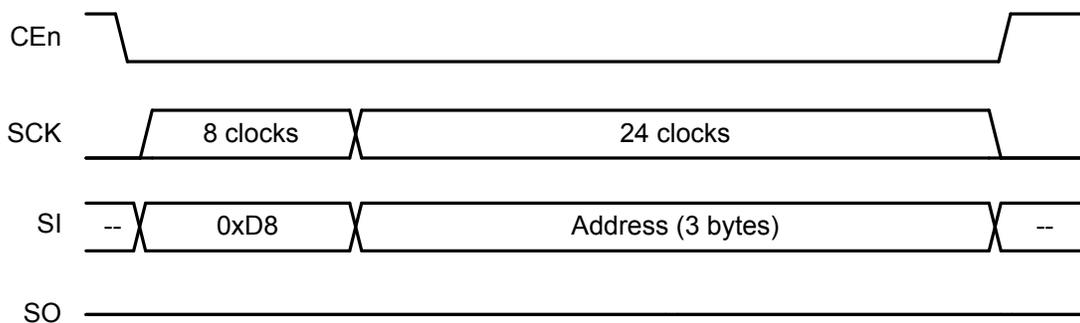


Figure 5.17. BER64 Instruction Format

### 5.3.6.8 Chip Erase (CER, 0xC7 / 0x60)

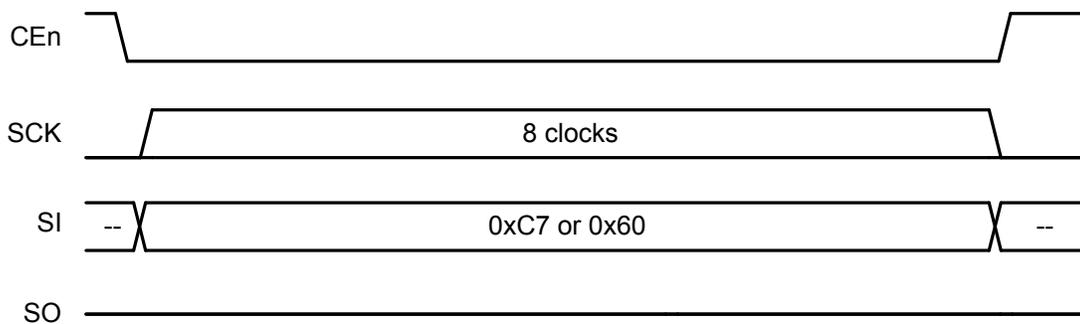


Figure 5.18. CER Instruction Format

### 5.3.6.9 Program/Erase Suspend (PERSUS, 0x75 / 0xB0)

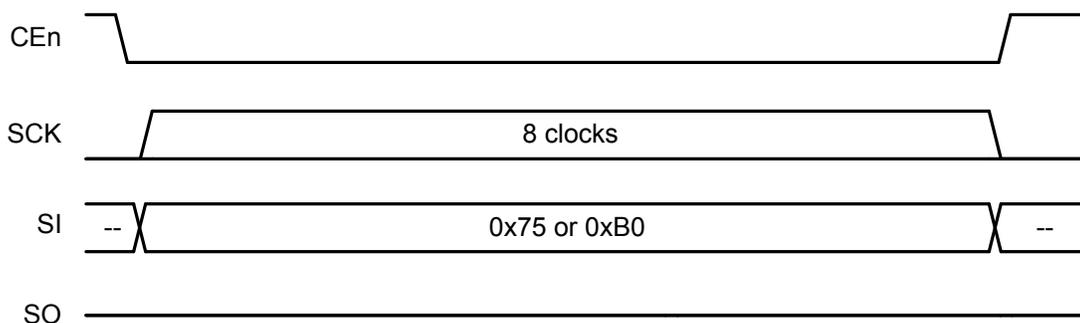


Figure 5.19. PERSUS Instruction Format

### 5.3.6.10 Program/Erase Resume (PERRSM, 0x7A / 0x30)

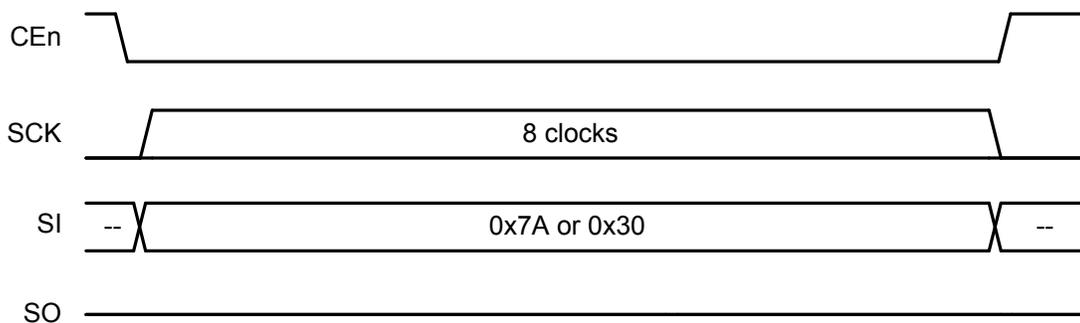


Figure 5.20. PERRSM Instruction Format

### 5.3.7 Write Protection

The serial flash supports both hardware and software write protection mechanisms to prevent accidental program or erasure. The block protect (BP) field in the STATUS register allows part or all of the memory area to be designated as write-protected. If a block is write-protected, no program or erase operations will affect the memory contents, unless a SECUNLOCK command is issued to first unlock the target sector. [Table 5.4 64 kB Block Write Protection on page 145](#) details the areas protected by each BP setting.

**Table 5.4. 64 kB Block Write Protection**

| BP field in STATUS Register (binary) | Write-Protected 64 kB Blocks |
|--------------------------------------|------------------------------|
| 0000                                 | None                         |
| 0001                                 | Block 7                      |
| 0010                                 | Blocks 6 and 7               |
| 0011                                 | Blocks 4, 5, 6, and 7        |
| 0100 - 1011                          | All Blocks                   |
| 1100                                 | Blocks 0, 1, 2 and 3         |
| 1101                                 | Blocks 0 and 1               |
| 1110                                 | Block 1                      |
| 1111                                 | None                         |

The Sector Unlock ([SECUNLOCK](#)) and Sector Lock ([SECLOCK](#)) commands are used to unlock and re-lock individual protected sectors as-needed when erasing and writing the memory. Only one sector may be unlocked with the SECUNLOCK command at a time, protecting the rest of the memory array from corruption. To unlock a sector, software should write the SECUNLOCK command (one byte), followed by the starting address of the target sector (3 bytes). The sector is locked again when a SECLOCK command is issued, or when a subsequent SECUNLOCK command unlocks a different sector. Because only one sector may be locked at a time, the SECLOCK command only requires the command byte to be sent, and does not accept an address.

Additionally, the WPn signal, in conjunction with the SRWD bit in the STATUS register, provides a means of preventing writes to the STATUS register where the software block protect (BP) field is located. [Table 5.5 Hardware STATUS Register Write Protection on page 145](#) shows how the STATUS register may be protected.

**Table 5.5. Hardware STATUS Register Write Protection**

| SRWD bit in STATUS Register | WPn Signal | Status Register |
|-----------------------------|------------|-----------------|
| 0                           | Low        | Writeable       |
| 1                           | Low        | Protected       |
| 0                           | High       | Writeable       |
| 1                           | High       | Writeable       |

### 5.3.7.1 Sector Unlock (SECUNLOCK, 0x26)

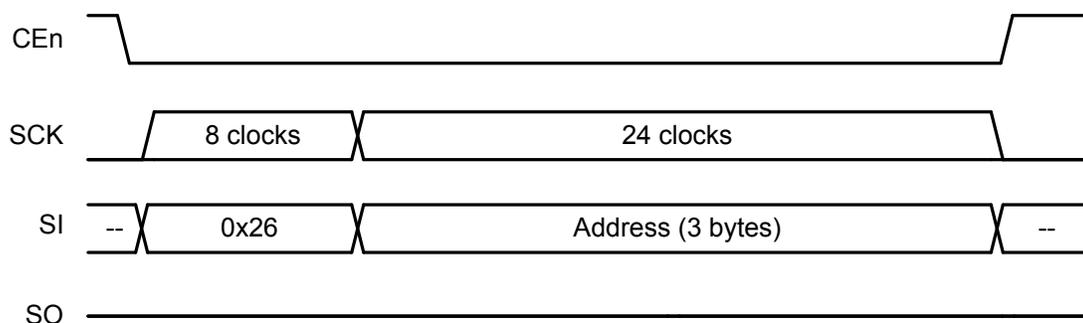


Figure 5.21. SECUNLOCK Instruction Format

### 5.3.7.2 Sector Lock (SECLOCK, 0x24)

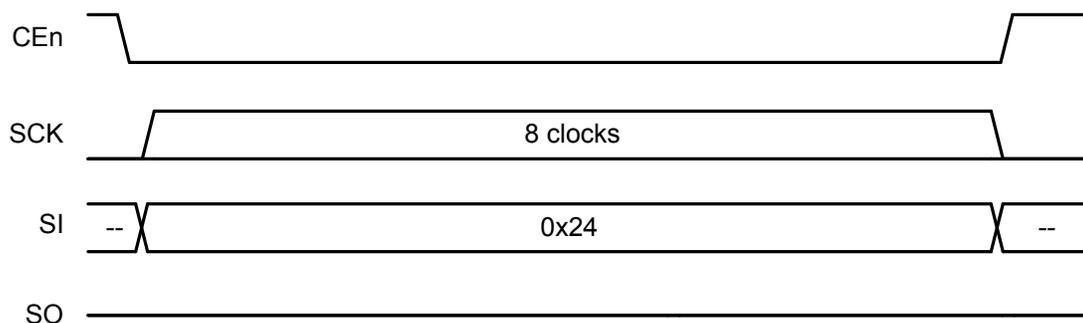


Figure 5.22. SECLOCK Instruction Format

### 5.3.8 Security Information Row and Unique ID

The serial flash has some additional storage outside of the general memory array: one 16-byte pre-programmed, read-only Unique ID space, and a Security Information Row space comprised of an additional 4 x 256 bytes of one-time programmable information.

The bits in the security information row can be written by the user, but not erased. Any program security instruction issued while program cycle is in progress is rejected without having any effect on the cycle that is in progress. The IRL0, IRL1, IRL2, and IRL3 bits in the FUNCTION register may be used to permanently lock the security information row data in 256-byte sections. When the corresponding IRL bit is set to 1, the 256 bytes in that section become read-only.

Table 5.6. Information Row Addressing

| Information Row Lock | A[23:16] | A[15:8] | A[7:0]       |
|----------------------|----------|---------|--------------|
| IRL0                 | 0x00     | 0x00    | Byte Address |
| IRL1                 | 0x00     | 0x10    | Byte Address |
| IRL2                 | 0x00     | 0x20    | Byte Address |
| IRL3                 | 0x00     | 0x30    | Byte Address |

## Reading the Information Rows

The Information Row Read (IRRD) instruction is used to read data stored in the security information rows. The IRRD instruction operates like the FR instruction, but targets the information row space.

, with each bit latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on the SO line, with each bit shifted out at a maximum frequency  $f_{CT}$ , during the falling edge of SCK. The address is automatically incremented by one after each byte of data is shifted out. Once the address reaches the last address of each 256 byte Information Row, the next address will not be valid and the data of the address will be garbage data. It is recommended to repeat four times IRRD operation that reads 256 byte with a valid starting address of each Information Row in order to read all data in the 4 x 256 byte Information Row array. The IRRD instruction is terminated by driving CE# high (VIH). If a IRRD instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle. The sequence of IRRD instruction is same as FAST READ except for the instruction code

To initiate a memory read using the IRRD instruction, software should send the IRRD instruction code (one byte), followed by the first memory location to be read (three bytes, MSB-first), followed by a dummy byte (one byte). Data will be shifted out of the serial flash beginning with the next serial clock.

Data is shifted out on the SO line, MSB first. Any number of bytes can be read out in one IRRD instruction. The address is automatically incremented after each byte of data is shifted out. Once the address reaches the last address of the information row, the next address will not be valid and the data read will be garbage data. If the entire information space is to be read, it is recommended to repeat the IRRD operation four times, with the starting address of each information row. The operation is terminated when CEn is driven high.

If an IRRD instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effect on the current operation.

## Programming the Information Rows

The Information Row Program (IRP) instruction allows up to 256 bytes data to be programmed into the information row memory in a single operation. An IRP instruction operates exactly like the Page Program instruction, but targets the information row space.

The procedure to program data bytes in an information row is as follows:

1. Set the Write Enable Latch (WEL) by sending a Write Enable (WREN) instruction.
2. Send the Information Row Program (IRP) instruction code (one byte), followed by the first information row location to be programmed (three bytes, MSB-first), and then shift the data to be programmed (1 to 256 bytes) into the flash.
3. Send Read Status Register (RDSR) instructions to the device to poll the STATUS register until the WIP bit is 0.

The write operation will start immediately after CEn is brought high. The IRP instruction will not be executed until CEn goes high. The internal control logic automatically handles programming voltages and timing. During a program operation, the WIP bit in STATUS will be set to 1 and all instructions will be ignored except the RDSR instruction and the PERSUS instruction. Upon completion of the program operation, the Write Enable Latch (WEL) will also be cleared.

The starting byte can be anywhere within the page. When the end of the row is reached during a IRP instruction (address ends in 0xFF), the address counter rolls over to the beginning of the row. If more than 256 bytes are receive during an IRP instruction, only the last 256 bytes received are programmed into the row. If the data to be programmed are less than a full row, the data of all other bytes on the same row will remain unchanged.

**Note:** The data in the security information rows is non-programmable. Once an information row is programmed, the bits cannot be erased. The information row lock bit associated with the row may be used to prevent subsequent IRP instructions from programming additional bits to 0.

## Reading the Unique ID

The Read Unique ID Number (RDUID) instruction accesses a factory-set read-only 16-byte number that is unique to the device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The RDUID instruction operates similar to the FR instruction. To read the Unique ID, issue the RDUID command (one byte), followed by an address (3 bytes), followed by a dummy byte, and then read 16 bytes of data. Because the Unique ID is 16 bytes in length, only the four LSBs of the address are used. If more than 16 bytes of data are read during the operation, the Unique ID will repeat.

## 5.3.8.1 Information Row Program (IRP, 0x62)

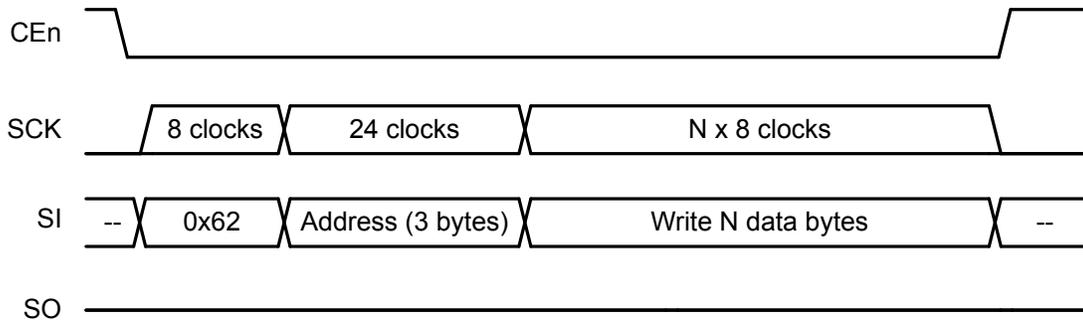


Figure 5.23. IRP Instruction Format

## 5.3.8.2 Information Row Read (IRRD, 0x68)

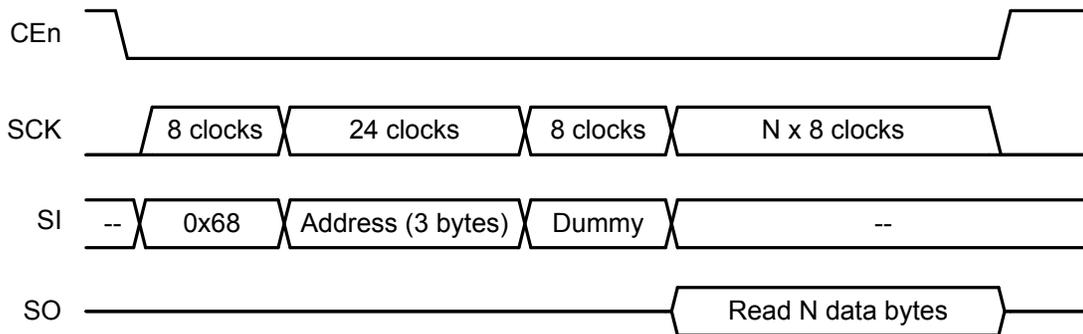


Figure 5.24. IRRD Instruction Format

## 5.3.8.3 Read Unique ID Number (RDUID, 0x4B)

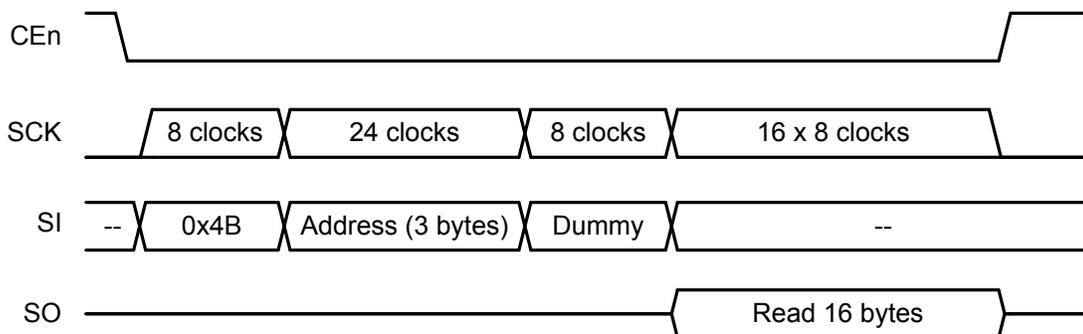


Figure 5.25. RDUID Instruction Format

### 5.3.9 Power Down

The serial flash may be put into a low-power state using the Deep Power-down (**DP**) instruction. When a DP instruction is issued, the power-down state will be entered within a maximum of 3  $\mu$ s after CEn is driven high.

To wake the serial flash and ready it for new instructions, the Release Deep Power Down (**RDPD**) is used. When an RDPD instruction is issued, the serial flash will resume normal operation within a maximum of 3  $\mu$ s after CEn is driven high. CEn must remain high during this time.

During the power-down mode, the device is not active and all instructions other than RDPD instruction are ignored.

#### 5.3.9.1 Deep Power Down (DP, 0xB9)

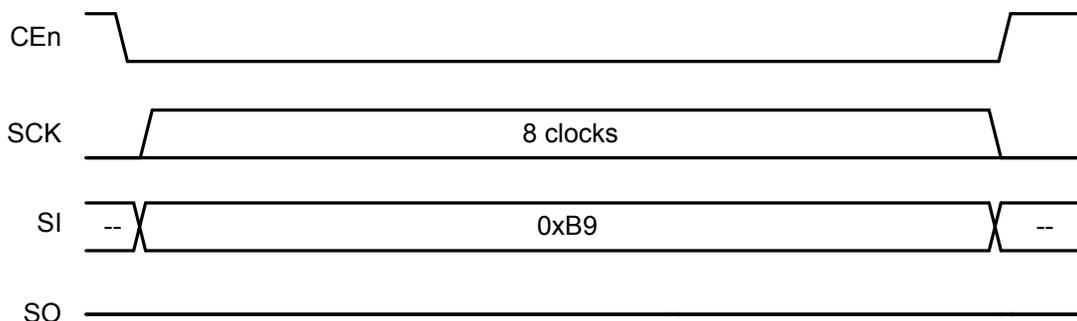


Figure 5.26. DP Instruction Format

#### 5.3.9.2 Release Deep Power Down (RDPD, 0xAB)

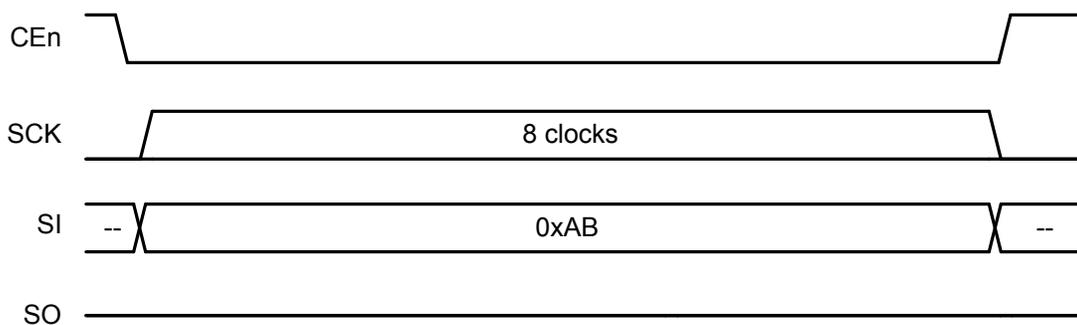


Figure 5.27. RDPD Instruction Format

### 5.3.10 Software Reset

The Reset operation is used as a system (software) reset that puts the device in normal operating mode. This operation consists of two commands: Reset-Enable (**RSTEN**) and Reset (**RST**). To initiate a reset operation, software must send the Reset-Enable command followed by the Reset command. Any command other than the Reset command after the Reset-Enable command will disable the reset.

Issuing a software reset during an active program or erase operation aborts the operation, which can result in corrupting or losing the data of the targeted address range. Depending on the prior operation, the reset timing may vary. Recovery from a write operation requires more latency time than recovery from other operations.

#### Note:

The Status and Function Registers remain unaffected.

5.3.10.1 Reset Enable (RSTEN, 0x66)

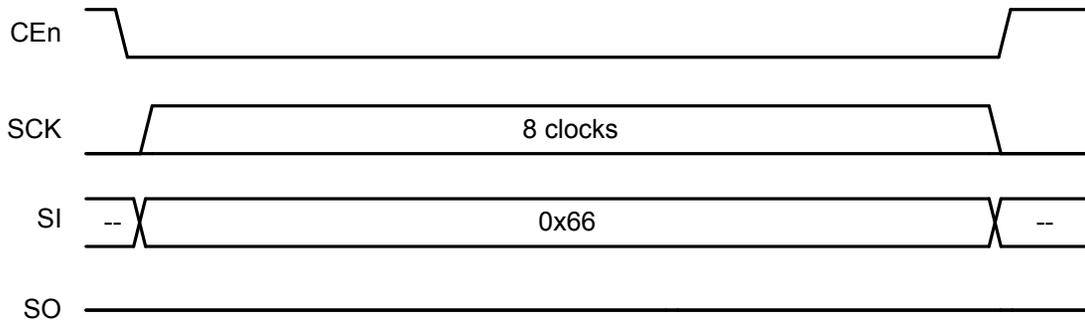


Figure 5.28. RSTEN Instruction Format

5.3.10.2 Reset (RST, 0x99)

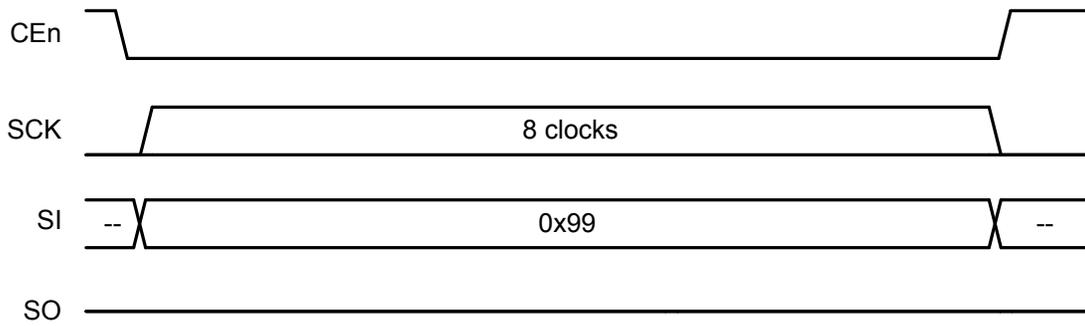
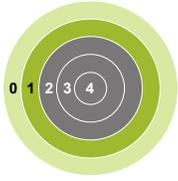


Figure 5.29. RST Instruction Format

## 6. Radio Transceiver



### Quick Facts

#### What?

The Radio Transceiver provides access to transmit and receive data, radio settings and control interface.

#### Why?

The Radio Transceiver enables the user to communicate using a wide range of data rates, modulation and frame formats.

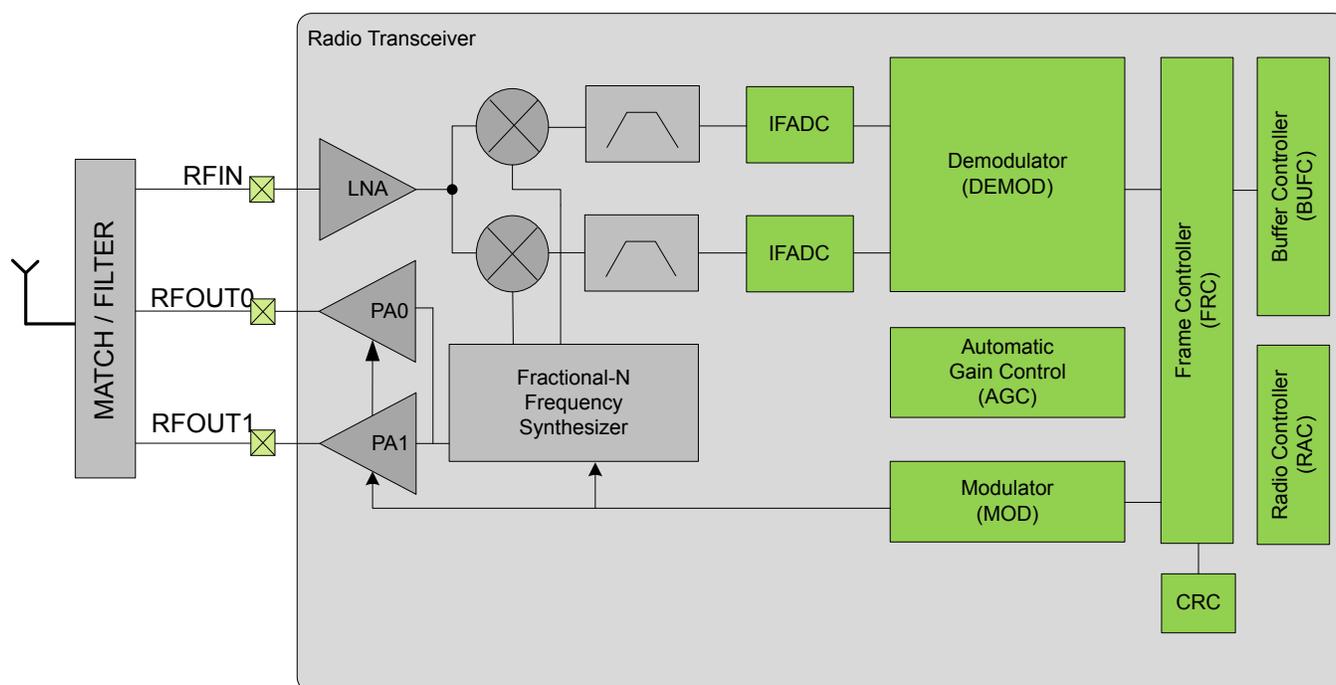
#### How?

Dynamic or fixed frame lengths, optional address recognition, flexible CRC and crypto schemes makes the EFR32 perfectly suit any application using low or medium data rate radio communication.

## 6.1 Introduction

The Radio Transceiver of the EFR32 enables the user to control a wide range of settings and options for tailoring radio operation precisely to the users need. It provides access to the transmit and receive data buffers and supports both dynamic and static frame lengths, as well as automatic address filtering and CRC insertion/verification.

As seen in the Radio Overview illustration (Figure 6.1 Radio Overview on page 152), the radio consists of several modules all responsible for specific tasks. Please refer to the abbreviations section (Appendix 1. Abbreviations) for a comprehensive description of acronyms.



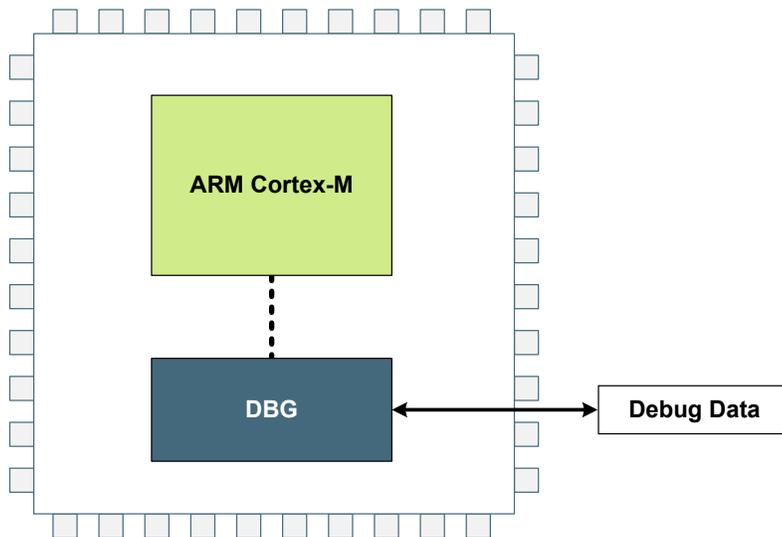
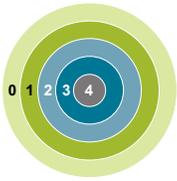
**Figure 6.1. Radio Overview**

During transmission (TX), the Radio Controller enables the SYNTH, Modulator and PA. The Modulator requests data from the Frame Controller, which reads data from a buffer. Based upon modulation format and data to send, the Modulator manipulates the SYNTH to output the correct frequency and phase. When the whole frame has been transmitted, the radio can automatically switch to receive mode.

In receive mode (RX), the radio controller enables the LNA, SYNTH, Mixer, ADC and Demodulator. The Demodulator searches for valid frames according to modulation format and data rate. If a frame is detected, the demodulated data is handed to the Frame Controller, which stores the data in the Buffer. When the complete frame has been received (determined by the Frame Controller), it is possible to either go to TX or stay in RX to search for a new frame.

The Radio Transceiver interface is accessible through software drivers provided by Silicon Labs.

## 7. DBG - Debug Interface



### Quick Facts

#### What?

The Debug Interface is used to program and debug EFR32xG13 Wireless Gecko devices.

#### Why?

The Debug Interface makes it easy to re-program and update the system in the field, and allows debugging with minimal I/O pin usage.

#### How?

The Cortex-M4 supports advanced debugging features. EFR32xG13 Wireless Gecko devices can use a minimum of two port pins for debugging or programming. The internal and external state of the system can be examined with debug extensions supporting instruction or data access break and watch points.

### 7.1 Introduction

The EFR32xG13 Wireless Gecko devices include hardware debug support through a 2-pin serial-wire debug (SWD) interface or a 4-pin Joint Test Action Group (JTAG) interface, as well as an Embedded Trace Module (ETM) for data/instruction tracing.

For more technical information about the debug interface the reader is referred to:

- ARM Cortex-M4 Technical Reference Manual
- ARM CoreSight Components Technical Reference Manual
- ARM Debug Interface v5 Architecture Specification
- IEEE Standard for Test Access Port and Boundary-Scan Architecture, IEEE 1149.1-2013

### 7.2 Features

- Debug Access Port Serial Wire JTAG (DAP SWJ-DP)
  - Implements the ADIV5 debug interface
- Authentication Access Point (AAP)
  - Implements various user commands
- Flash Patch and Breakpoint (FPB) unit
  - Implement breakpoints and code patches
- Data Watch point and Trace (DWT) unit
  - Implement watch points, trigger resources and system profiling
- Instrumentation Trace Macrocell (ITM)
  - Application-driven trace source that supports printf style debugging
- Embedded Trace Macrocell v3.5 (ETM)
  - Real time instruction and data trace information of the processor

### 7.3 Functional Description

Operation of the available debug interface is described in the following sections.

### 7.3.1 Debug Pins

The following pins are the debug connections for the device:

- Serial Wire Clock Input and Test Clock Input (SWCLKTCK) : This pin is enabled after power-up and has a built-in pull down.
- Serial Wire Data Input/Output and Test Mode Select Input (SWDIOTMS) : This pin is enabled after power-up and has a built-in pull-up.
- Test Data Output (TDO): This pin is assigned to JTAG functionality after power-up. However, it remains in high-Z state until the first valid JTAG command is received.
- Test Data Input (TDI): This pin is assigned to JTAG functionality after power-up. However, it remains in high-Z state until the first valid JTAG command is received. Once enabled, the pin has a built-in pull-up.

The debug pins have pull-down and pull-up enabled by default, so leaving them enabled may increase the current consumption if left connected to supply or ground. The debug pins can be enabled and disabled through GPIO\_ROUTEEN, see [33.3.4.2.3 Disabling Debug Connections](#). Remember that upon disabling the debug pins, debug contact with the device is lost once the DAP SWJ-DP power request bits are deasserted. By default after power cycle the part's debug pins are in JTAG mode. If during debugging session the pins are switched to SWD mode, a power cycle is required to bring restore the pins to JTAG mode.

### 7.3.2 Embedded Trace Macrocell V3.5 (ETM)

The ETM makes it possible to trace both instruction and data from the processor in real time. The trace can be controlled through a set of triggering and filtering resources. The resources include 4 address comparators, 2 data value comparators, 2 counters, a context ID comparator and a sequencer. The ETM circuit does not automatically enable an auxiliary clock. If AUXCLK is elected as the ETM clock source, the AUXHFRCO oscillator must be enabled by setting AUXHFRCOEN in CMU\_OSCENCMD before enabling the ETM. Likewise, if switching from AUXCLK to a different source for ETM, the AUXHFRCO must remain enabled until the clock switch has completed.

The trace can be exported through a set of trace pins, which include:

- Trace Clock (TCLK): Functions as a sample clock for the trace. This pin is disabled after reset.
- Trace Data 0 - Trace Data 3 (TD0-TD3): The data pins provide the compressed trace stream. These pins are disabled after reset.

For information on how to configure the ETM, see the ARM Embedded Trace Macrocell Architecture Specification. The Trace Clock and Trace Data pins can be enabled through the GPIO. For more information on how to enable the ETM Trace pins, the reader is referred to [33.3.4.2.4 ETM Trace Connections](#).

### 7.3.3 Debug and EM2 Deep Sleep/EM3 Stop

Leaving the debugger connected when issuing a WFI or WFE to enter EM2 Deep Sleep or EM3 Stop will make the system enter a special EM2 Deep Sleep. This mode differs from regular EM2 Deep Sleep and EM3 Stop in that the high frequency clocks are still enabled, and certain core functionality is still powered in order to maintain debug-functionality. Because of this, the current consumption in this mode is closer to EM1 Sleep and it is therefore important to deassert the power requests in the DAP SWJ-DP and disconnect the debugger before doing current consumption measurements.

### 7.3.4 Authentication Access Point

The Authentication Access Point (AAP) is a set of registers that provide a minimal amount of debugging and system level commands. The AAP registers contain commands to issue a FLASH erase, a system reset, a CRC of user code pages, and stalling the system bus. The user must program the APSEL bit field to 255 inside of the ARM DAP SWJ Debug Port SELECT register to access the AAP. The AAP is only accessible from a debugger and not from the core.

#### 7.3.4.1 System Bus Stall

The system bus can be stalled at any time using the SYSBUSSTALL register bit. Once the SYSBUSSTALL is set, the system bus will remain stalled until SYSBUSSTALL is cleared. While the system bus is stalled, only the registers inside the Cortex-M4, AAP and the debugger can be accessed. The SYSBUSSTALL register is available at all times through the AAP.

#### 7.3.4.2 Command Key

The AAP uses a command key to enable the DEVICEERASE and SYSRESETREQ AAP commands. The command key must be written with the correct key in order for the commands to execute.

### 7.3.4.3 Device Erase

The device can be erased by stalling the system bus, writing AAP\_CMDKEY, and then writing the DEVICEERASE register bit. Upon writing the command bit, the ERASEBUSY bit is asserted. The ERASEBUSY bit will be de-asserted once the erase is complete. The SYSRESETREQ bit must then be set to resume a normal debugger session. The DEVICEERASE register is available at all times through the AAP once the CMDKEY is entered.

### 7.3.4.4 System Reset

The system can be reset by writing AAP\_CMDKEY followed by writing the SYSRESTREQ register bit. This must be done after asserting DEVICEERASE or CRCREQ. Depending on the reset level setting for system reset, asserting SYSRESETREQ will either reset the entire AAP register space or just the SYSRESETREQ bit. See [10.3.1 Reset Levels](#) for more details on reset levels. The SYSRESETREQ register is available at all times through the AAP once the CMDKEY is entered.

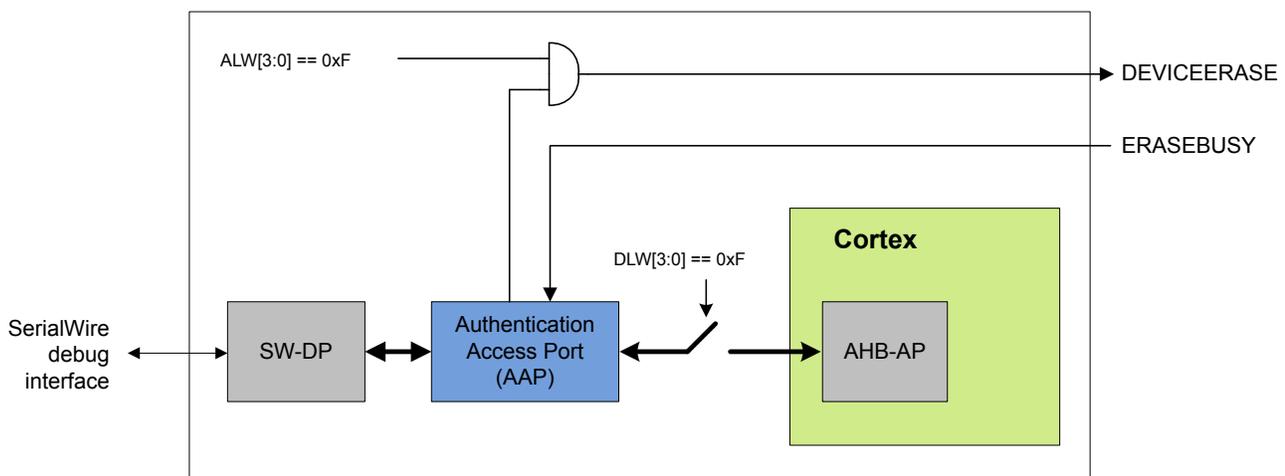
### 7.3.4.5 User Flash Page CRC

The CRCREQ command initiates a CRC calculation on a given Flash Page. The CRC is only available on the Main, User Data, and Lock Bit pages. It is highly recommended that the system bus is stalled before any CRCREQ commands are issued. The CRC calculation uses the on chip CRC block configured in 32 bit CRC mode. The Flash Page address for the CRCREQ command is written to the CRCADDR register. After issuing the CRCREQ, the CRCBUSY flag is asserted. Once the CRCBUSY flag is de-asserted, the resulting page CRC can be found in the CRCRESULT register. Once issuing a CRC command, the CPU is stalled and remains stalled until a system reset occurs. Multiple CRC requests can occur before resetting the system. However, a CRC request that occurs while the CRCBUSY flag is asserted will be ignored. The CRC registers are available at all times through the AAP.

## 7.3.5 Debug Lock

The debug access to the Cortex-M4 is locked by clearing the Debug Lock Word (DLW) and resetting the device, see [8.3.2 Lock Bits \(LB\) Page Description](#).

When debug access is locked, the debugger can access the DAP SWJ-DP and AAP registers. However, the connection to the Cortex-M4 core and the whole bus-system is blocked. This mechanism is controlled by the Authentication Access Port (AAP) as illustrated by [Figure 7.1 AAP - Authentication Access Port](#) on page 155.



**Figure 7.1. AAP - Authentication Access Port**

If the DLW is cleared, the device is locked. If the device is locked and the the AAP Lock Word (ALW) has not been cleared, it can be unlocked by writing a valid key to the AAP\_CMDKEY register and then setting the DEVICEERASE bit of the AAP\_CMD register via the debug interface. This operation erases the main block of flash, clears all lock bits, and debug access to the Cortex-M4 and bus-system is enabled. The operation takes tens of milli seconds to complete. Note that the SRAM contents will also be deleted during a device erase, while the UD-page is not erased.

The debugger may read the status of the device erase from the AAP\_STATUS register. When the ERASEBUSY bit is set low after DEVICEERASE of the AAP\_CMD register is set, the debugger may set the SYSRESETREQ bit in the AAP\_CMD register. After reset, the debugger may resume a normal debug session through the AHB-AP.

### 7.3.6 AAP Lock

Take extreme caution when using this feature. Once the AAP has been locked, the state of the FLASH can not be changed via the debugger.

### 7.3.7 Debugger Reads of Actionable Registers

Some peripheral registers cause particular actions when read, e.g FIFOs which pop and IFC registers which clear the IF flags when read. This can cause problems when debugging and the user wants to read the value without triggering the read action. For this reason, by default, the peripherals will not execute these triggered actions when an attached debugger is performing the read accesses through the AAP. To override this behavior, the debugger can configure the MASTERTYPE bitfield of the Cortex-M4 AHB Access Port CSW register in order to emulate a core access when performing system bus transfers.

**Note:**

- Registers with actionable reads are noted in their register descriptions. Refer to [Table 1.1 Register Access Types on page 28](#).

### 7.3.8 Debug Recovery

Debug recovery is the ability to stall the system bus before the Cortex-M4 executes code. For example, the first few instructions may disconnect the debugger pins. When this occurs it is difficult to connect the debugger and halt the Cortex-M4 before the Cortex-M4 starts to execute. By holding down pin reset, issuing the System Bus Stall AAP instruction, then releasing pin reset, the debugger can stall the system bus before the Cortex-M4 has a chance to execute. Because the system is under reset during this procedure the Debugger can not look for ACK's from the part. Once the system bus is stalled, the FLASH can be erased by issuing the AAP\_CMDKEY and then the writing the DEVICEERASE in the AAP\_CMD register.

## 7.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name           | Type | Description                 |
|--------|----------------|------|-----------------------------|
| 0x000  | AAP_CMD        | W1   | Command Register            |
| 0x004  | AAP_CMDKEY     | W1   | Command Key Register        |
| 0x008  | AAP_STATUS     | R    | Status Register             |
| 0x00C  | AAP_CTRL       | RW   | Control Register            |
| 0x010  | AAP_CRC_CMD    | W1   | CRC Command Register        |
| 0x014  | AAP_CRC_STATUS | R    | CRC Status Register         |
| 0x018  | AAP_CRC_ADDR   | RW   | CRC Address Register        |
| 0x01C  | AAP_CRC_RESULT | R    | CRC Result Register         |
| 0x0FC  | AAP_IDR        | R    | AAP Identification Register |

## 7.5 Register Description

### 7.5.1 AAP\_CMD - Command Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |             |              |              |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-------------|--------------|--------------|
| 0x000         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1           | 0            |              |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | 0           | 1            | 0            |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | W1          | W1           | W1           |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | SYSRESETREQ | DEVICESERASE | DEVICESERASE |

| Bit  | Name        | Reset   | Access | Description   |
|------|-------------|---|--------|---|
| 31:2 | Reserved    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 1    | SYSRESETREQ | 0   | W1     | <b>System Reset Request</b><br>A system reset request is generated when set to 1. This register is write enabled from the AAP_CMDKEY register.  |
| 0    | DEVICEERASE | 0   | W1     | <b>Erase the Flash Main Block, SRAM and Lock Bits</b><br>When set, all data and program code in the main block is erased, the SRAM is cleared and then the Lock Bit (LB) page is erased. This also includes the Debug Lock Word (DLW), causing debug access to be enabled after the next reset. The information block User Data page (UD) is left unchanged, but the User data page Lock Word (ULW) is erased. This register is write enabled from the AAP_CMDKEY register. |

### 7.5.2 AAP\_CMDKEY - Command Key Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |            |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|------------|---|--|
| 0x004         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1          | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | 0x00000000 |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | W1         |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | WRITEKEY   |   |  |

| Bit  | Name       | Reset      | Access                  | Description   |
|------|------------|------------|-------------------------|---|
| 31:0 | WRITEKEY   | 0x00000000 | W1                      | <b>CMD Key Register</b><br>The key value must be written to this register to write enable the AAP_CMD register. |
|      | Value      | Mode       | Description             |   |
|      | 0xCFACC118 | WRITEEN    | Enable write to AAP_CMD |   |

## 7.5.3 AAP\_STATUS - Status Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |        |           |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|--------|-----------|
| 0x008         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1      | 0         |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | 0      | 0         |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | R      | R         |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | LOCKED | ERASEBUSY |

| Bit  | Name      | Reset   | Access | Description  |
|------|-----------|---|--------|--|
| 31:2 | Reserved  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 1    | LOCKED    | 0   | R      | <b>AAP Locked</b><br>Set when the AAP is locked, .e.g the AAP Lock Word AAP lsb bits are not 0xF |
| 0    | ERASEBUSY | 0   | R      | <b>Device Erase Command Status</b><br>This bit is set when a device erase is executing.          |

## 7.5.4 AAP\_CTRL - Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |             |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-------------|----|
| 0x00C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1           | 0  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | 0           | 0  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | RW          | RW |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | SYSBUSSTALL |    |

| Bit  | Name        | Reset   | Access | Description  |
|------|-------------|---|--------|--|
| 31:1 | Reserved    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 0    | SYSBUSSTALL | 0   | RW     | <b>Stall the System Bus</b><br>When this bit is set, the system bus is stalled. Only the Cortex registers are accessible |

## 7.5.5 AAP\_CRC CMD - CRC Command Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |        |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|--------|
| 0x010         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0      |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0      |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | W1     |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | CRCREQ |

| Bit  | Name     | Reset  | Access | Description   |
|------|----------|--|--------|---|
| 31:1 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 0    | CRCREQ   | 0  | W1     | <b>CRC Request</b><br>A CRC request is generated when set to 1. This command is not available if debug access or AAP is locked. |

## 7.5.6 AAP\_CRC STATUS - CRC Status Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |         |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---------|
| 0x014         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0       |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0       |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | R       |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | CRCBUSY |

| Bit  | Name     | Reset  | Access | Description   |
|------|----------|--|--------|---|
| 31:1 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 0    | CRCBUSY  | 0  | R      | <b>CRC Calculation is Busy</b><br>Set when the CRC calculation is executing. Will transition from 1 to 0 on valid data. |

### 7.5.7 AAP\_CRCADDR - CRC Address Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x018         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CRCADDR    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name    | Reset      | Access | Description  |
|------|---------|------------|--------|--|
| 31:0 | CRCADDR | 0x00000000 | RW     | <b>Starting Page Address for CRC Execution</b><br>Set this to the address the CRC executes on. |

### 7.5.8 AAP\_CRCRESULT - CRC Result Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x01C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CRCRESULT  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

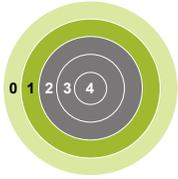
| Bit  | Name      | Reset      | Access | Description  |
|------|-----------|------------|--------|--|
| 31:0 | CRCRESULT | 0x00000000 | R      | <b>CRC Result of the CRCADDRESS</b><br>Result of the CRC calculation using the CRCADDRESS. |

### 7.5.9 AAP\_IDR - AAP Identification Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x0FC         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x26E60011 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | ID         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name | Reset      | Access | Description   |
|------|------|------------|--------|---|
| 31:0 | ID   | 0x26E60011 | R      | <b>AAP Identification Register</b><br>Access port identification register in compliance with the ARM ADI v5 specification (JEDEC Manufacturer ID) . |

## 8. MSC - Memory System Controller



```

01000101011011100110010101110010
01100111011110010010000001001101
01101001011000110111001001101111
00100000011100100111010101101100
01100101011100110010000001110100
01101000011001010010000001110111
01101111011100100110110001100100
00100000011011110110011000100000
01101100011011110111011100101101
01100101011011100110010101110010
01100111011110010010000001101101
01101001011000110111001001101111
01100011011011110110111001110100
01110010011011110110110001101100
01100101011100100010000001100100
01100101011100110110100101100111
01101110001000010100010101101110

```

### Quick Facts

#### What?

The user can perform flash memory read, read configuration and write operations through the Memory System Controller (MSC).

#### Why?

The MSC allows the application code, user data and flash lock bits to be stored in non-volatile flash memory. Certain memory system functions, such as program memory wait-states and bus faults are also configured from the MSC peripheral register interface, giving the developer the ability to dynamically customize the memory system performance, security level, energy consumption and error handling capabilities to the requirements at hand.

#### How?

The MSC integrates a low-energy flash IP with a charge pump, enabling minimum energy consumption while eliminating the need for external programming voltage to erase the memory. An easy to use write and erase interface is supported by an internal, fixed-frequency oscillator and autonomous flash timing and control reduces software complexity while not using other timer resources.

Application code may dynamically scale between high energy optimization and high code execution performance through advanced read modes.

A highly efficient low energy instruction cache reduces the number of flash reads significantly, thus saving energy. Performance is also improved when wait-states are used, since many of the wait-states are eliminated. Built-in performance counters can be used to measure the efficiency of the instruction cache.

### 8.1 Introduction

The Memory System Controller (MSC) is the program memory unit of the EFR32xG13 Wireless Gecko microcontroller. The flash memory is readable and writable from both the Cortex-M4 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 Active and EM1 Sleep.

## 8.2 Features

- AHB read interface
  - Scalable access performance to optimize the Cortex-M4 code interface
    - Zero wait-state access up to 25 MHz
    - Advanced energy optimization functionality
      - Conditional branch target prefetch suppression
      - Cortex-M4 disfolding of if-then (IT) blocks
      - Instruction Cache
  - DMA read support in EM0 Active and EM1 Sleep
- Command and status interface
  - Flash write and erase
    - Accessible from Cortex-M4 in EM0 Active
    - DMA write support in EM0 Active and EM1 Sleep
  - Core clock independent flash timing
    - Internal oscillator and internal timers for precise and autonomous flash timing
      - General purpose timers are not occupied during flash erase and write operations
  - Configurable interrupt erase abort
    - Improved interrupt predictability
  - Memory and bus fault control
- Security features
  - Lockable debug access
  - Page lock bits
  - SW mass erase lock bits
  - Authentication Access Port (AAP) lock bits
- End-of-write and end-of-erase interrupts

### 8.3 Functional Description

The size of the main block is device dependent. The largest size available is 512 KB (256 pages). The information block has 2 KB available for user data. The information block also contains chip configuration data located in a reserved area. The main block is mapped to address 0x00000000 and the information block is mapped to address 0xFE0000. [Table 8.1 MSC Flash Memory Mapping on page 164](#) outlines how the flash is mapped in the memory space. All flash memory is organized into 2 KB pages.

**Table 8.1. MSC Flash Memory Mapping**

| Block             | Page      | Base address | Write/Erase by...                           | Software Readable?           | Purpose/Name                 | Size           |
|-------------------|-----------|--------------|---|------------------------------|------------------------------|----------------|
| Main <sup>1</sup> | 0         | 0x00000000   | Software, debug                             | Yes                          | User code and data           | 32 KB - 512 KB |
|                   | ...       |              | Software, debug                             | Yes                          |                              |                |
|                   | 255       | 0x0007F800   | Software, debug                             | Yes                          |                              |                |
| Reserved          | -         | 0x00080000   | -   | -                            | Reserved for flash expansion | ~24 MB         |
| Information       | 0         | 0xFE00000    | Software, debug                             | Yes                          | User Data (UD)               | 2 kB           |
|                   | -         | 0xFE00800    | -   | -                            | Reserved                     | -              |
|                   | 1         | 0xFE04000    | Write: Software, debug<br>Erase: Debug only | Yes                          | Lock Bits (LB)               | 2 kB           |
|                   | -         | 0xFE04800    | -   | -                            | Reserved                     | -              |
|                   | 2         | 0xFE081B0    | -   | Yes                          | Device Information (DI)      | 1 kB           |
|                   | -         | 0xFE08400    | -   | -                            | Reserved                     | -              |
|                   | 2         | 0xFE0C000    | -   | -                            |                              | 1 kB           |
|                   | -         | 0xFE0C400    | -   | -                            | Reserved                     | -              |
|                   | 3 3       | 0xFE10000    | Software, debug                             | Yes                          | Bootloader (BL)              | 16 kB          |
|                   | ...       |              | -   | -                            |                              |                |
| 10                | 0xFE13800 | -            | -   |                              |                              |                |
| Reserved          | -         | 0xFE14000    | -   | Reserved for flash expansion | Rest of code space           | -              |

**Note:**

1. Block/page erased by a device erase.

#### 8.3.1 User Data (UD) Page Description

This is the user data page in the information block. The page can be erased and written by software. The page is erased by the ERASEPAGE command of the MSC\_WRITECMD register. Note that the page is not erased by a device erase operation. The device erase operation is described in [7.3.4 Authentication Access Point](#).

### 8.3.2 Lock Bits (LB) Page Description

This page contains the following information:

- Main block Page Lock Words (PLWs)
- User data page Lock Word (ULWs)
- Debug Lock Word (DLW)
- Mass erase Lock Word (MLW)
- Authentication Access Port (AAP) lock word (ALW)
- Bootloader enable (CLW0)
- Pin reset soft (CLW0)

The words in this page are organized as shown in [Table 8.2 Lock Bits Page Structure](#) on page 165:

**Table 8.2. Lock Bits Page Structure**

|     |        |
|-----|--------|
| 127 | DLW    |
| 126 | ULW    |
| 125 | MLW    |
| 124 | ALW    |
| 122 | CLW0   |
| N   | PLW[N] |
| ... | ...    |
| 1   | PLW[1] |
| 0   | PLW[0] |

There are 32 page lock bits per page lock word (PLW). Bit 0 refers to the first page and bit 31 refers to the last page within a PLW. Thus, PLW[0] contains lock bits for page 0-31 in the main block, PLW[1] contains lock bits for page 32-63 etc. A page is locked when the bit is 0. A locked page cannot be erased or written.

Word 127 is the debug lock word (DLW). The four LSBs of this word are the debug lock bits. If these bits are 0xF, then debug access is enabled. Debug access to the core is disabled from power-on reset until the DLW is evaluated immediately before the Cortex-M4 starts execution of the user application code. If the bits are not 0xF, then debug access to the core remains blocked.

Word 126 is the user page lock word (ULW). Bit 0 of this word is the User Data Page lock bit. Bit 1 in this word locks the Lock Bits Page. The lock bits can be reset by a device erase operation initiated from the Authentication Access Port (AAP) registers. The AAP is described in more detail in [7.3.4 Authentication Access Point](#). Note that the AAP is only accessible from the debug interface, and cannot be accessed from the Cortex-M4 core.

Word 125 is the mass erase lock word (MLW). Bit 0 locks the entire flash. The mass erase lock bits will not have any effect on device erases initiated from the Authentication Access Port (AAP) registers. The AAP is described in more detail in [7.3.4 Authentication Access Point](#).

Word 124 is the Authentication Access Port (AAP) lock word (ALW) and the four LSBs of this word are the lock bits. If these bits are 0xF, then AAP access is enabled. If the bits are not 0xF, AAP is disabled and it is impossible to access the device through the AAP. Bit 31 of the ALW may be used to allow AAP access under controlled conditions. If bit 31 is set to 1, software running on the device can unlock AAP access using the MSC\_AAPUNLOCKCMD register. If bit 31 is cleared to 0, software will not be able to use MSC\_AAPUNLOCKCMD to unlock AAP access. **NOTE - locking the AAP completely (including the LSBs and bit 31) is irreversible. Once the AAP is locked, it will be impossible to perform an external mass erase and the AAP lock cannot be reset.** The only way to program the device when the AAP is locked is through a boot loader or by SW already loaded into the FLASH.

Word 122 is Configuration Lock Word 0 (CLW0). Bit 2 is the Pin Reset Soft bit. By default, a pin reset is handled as a soft reset (See [10.3.5 RESETn Pin Reset](#)). Bit 1 is the bootloader enable bit. Because the state of erased flash bits is 1, the bootloader is enabled by default.

### 8.3.3 Device Information (DI) Page

This read-only page holds calibration data from the production test as well as a unique device ID. The page is further described in [4. Memory and Bus System](#).

### 8.3.4 Bootloader

The memory space includes an area for custom-programmed bootloaders. The available bootloader area is 16 kB for this device family. By default, the system is configured to boot directly into user software after system reset, and there is not a pre-programmed bootloader in the device. If a custom bootloader which follows Silicon Labs' bootloader recommendations outlined in *AN0003: UART Bootloader* ([www.silabs.com/32bit-appnotes](http://www.silabs.com/32bit-appnotes)) is programmed into the bootloader area, the system can be redirected to boot from this area by setting bit 1 in config lock word 0 (CLW0) at word 122 of the lockbit (LB) page.

After any device reset, the bootloader area is accessible to both software reads and writes. Reading and writing of this area may be disabled with the MSC\_BOOTLOADERCTRL register. Note that this register is write-once, so after writing the register, a reset of the system is required in order to change permissions again.

**Note:** Software should never erase "Reserved" pages when bootloader write/erase is enabled. Doing so may cause the device to become non-functional and irrevocably locked.

### 8.3.5 Post-reset Behavior

Calibration values are automatically written to registers by the MSC before application code startup. The values are also available to read from the DI page for later reference by software. Other information such as the device ID and production date is also stored in the DI page and is readable from software.

If the bootloader is not bypassed, the system will boot up from the bootloader at address 0x0FE10000.

### 8.3.6 Flash Startup

On transitions from EM2/3 to EM0, the flash must be powered up. The time this takes depends on the current operating conditions. To have a deterministic startup-time, set STDLY0 in MSC\_STARTUP to 0x64 and clear STDLY1, ASTWAIT, STWSEN and STWS. This will result in a 10 us delay before the flash is ready. The system will wake up before this, but the Cortex will stall on the first access to the flash until it is ready. Execute code from RAM or cache to get a quicker startup.

To get the fastest possible startup when waking, i.e. a startup that depends on the current operating conditions, set STDLY0 to 0x28 and set ASTWAIT in MSC\_STARTUP. When configured this way, the system will poll the flash to determine when it is ready, and then start execution.

For even quicker startup, run code in beginning with a set of wait-states. Set STDLY0 to 0x32, STDLY1 to 0x32, and set ASTWAIT and STWSEN. Then configure STWS in MSC\_STARTUP to the number of waitstates to run with. With this setup, sampling will begin with the given number of waitstates after 5 us, and the system will run with this number of waitstates for the remaining 5 us before returning to normal operation

A recommended setting for MSC\_STARTUP register is to leave STDLY0 at its reset value and set ASTWAIT to one for active sampling. Set STWSEN to zero to bypass the second delay period.

Flash wakeup on demand is supported when wakeup from EM2/3 to EM0. Set bit PWRUPONDEMAND of register MSC\_CTRL to one to enable the power up on demand. When enabled during powerup, flash will enter sleep mode and waiting for either pending flash read transaction or software command to MSC\_CMD.PWRUP bit. If software command wakeup, and interrupt of MSC\_IF.PWRUPF will be flagged if the MSC\_IEN.PWRUPF is set

### 8.3.7 Wait-states

**Table 8.3. Flash Wait-States**

| Wait-States | Frequency                            |
|-------------|--------------------------------------|
| WS0         | no more than 25 MHz                  |
| WS1         | above 25 MHz and no more than 40 MHz |

### 8.3.7.1 One Wait-state Access

After reset, the HFCORECLK is normally 19 MHz from the HFRCO and the MODE field of the MSC\_READCTRL register is set to WS1 (one wait-state). Software must not select a zero wait-state mode unless the clock is guaranteed to be 25 MHz or below, otherwise the resulting behavior is undefined. If a HFCORECLK frequency above 25 MHz is to be set by software, the MODE field of the MSC\_READCTRL register must be set to WS1 or WS1SCBTP before the core clock is switched to the higher frequency clock source.

When changing to a lower frequency, the MODE field of the MSC\_READCTRL register must be set to WS0 or WS0SCBTP only after the frequency transition has completed. If the HFRCO is used, wait until the oscillator is stable on the new frequency. Otherwise, the behavior is unpredictable.

To run at a frequency higher than 40 MHz, WS2 or WS2SCBTP must be selected to insert two wait-states for every flash access.

### 8.3.7.2 Zero Wait-state Access

At 25 MHz and below, read operations from flash may be performed without any wait-states. Zero wait-state access greatly improves code execution performance at frequencies from 25 MHz and below. By default, the Cortex-M4 uses speculative prefetching and If-Then block folding to maximize code execution performance at the cost of additional flash accesses and energy consumption.

### 8.3.7.3 Operation Above

To run at frequencies higher than 25 MHz, MODE in MSC\_READCTRL must be set to WS1 or WS1SCBTP.

### 8.3.8 Suppressed Conditional Branch Target Prefetch (SCBTP)

MSC offers a special instruction fetch mode which optimizes energy consumption by cancelling Cortex-M4 conditional branch target prefetches. Normally, the Cortex-M4 core prefetches both the next sequential instruction and the instruction at the branch target address when a conditional branch instruction reaches the pipeline decode stage. This prefetch scheme improves performance while one extra instruction is fetched from memory at each conditional branch, regardless of whether the branch is taken or not. To optimize for low energy, the MSC can be configured to cancel these speculative branch target prefetches. With this configuration, energy consumption is more optimal, as the branch target instruction fetch is delayed until the branch condition is evaluated.

The performance penalty with this mode enabled is source code dependent, but is normally less than 1% for core frequencies from 25 MHz and below. To enable the mode at frequencies from 25 MHz and below write WS0SCBTP to the MODE field of the MSC\_READCTRL register. For frequencies above 25 MHz, use the WS1SCBTP mode, and for frequencies above 40 MHz, use the WS2SCBTP mode. An increased performance penalty per clock cycle must be expected compared to WS0SCBTP mode. The performance penalty in WS1SCBTP/WS2SCBTP mode depends greatly on the density and organization of conditional branch instructions in the code.

### 8.3.9 Cortex-M4 If-Then Block Folding

The Cortex-M4 offers a mechanism known as if-then block folding. This is a form of speculative prefetching where small if-then blocks are collapsed in the prefetch buffer if the condition evaluates to false. The instructions in the block then appear to execute in zero cycles. With this scheme, performance is optimized at the cost of higher energy consumption as the processor fetches more instructions from memory than it actually executes. To disable the mode, write a 1 to the DISFOLD bit in the NVIC Auxiliary Control Register; see the Cortex-M4 Technical Reference Manual for details. Normally, it is expected that this feature is most efficient at core frequencies above 25 MHz. Folding is enabled by default.

### 8.3.10 Instruction Cache

The MSC includes an instruction cache. The instruction cache for the internal flash memory is enabled by default, but can be disabled by setting `IFCDIS` in `MSC_READCTRL`. When enabled, the instruction cache typically reduces the number of flash reads significantly, thus saving energy. In most cases a cache hit-rate of more than 70 % is achievable. When a 32-bit instruction fetch hits in the cache the data is returned to the processor in one clock cycle. Thus, performance is also improved when wait-states are used (i.e. running at frequencies above 25 MHz).

The instruction cache is connected directly to the `ICODE` bus on the ARM core and functions as a memory access filter between the processor and the memory system, as illustrated in [Figure 8.1 Instruction Cache on page 168](#). The cache consists of an access filter, lookup logic, SRAM, and two performance counters. The access filter checks that the address for the access is to on-chip flash memory (instructions in RAM are not cached). If the address matches, the cache lookup logic and SRAM is enabled. Otherwise, the cache is bypassed and the access is forwarded to the memory system. The cache is then updated when the memory access completes. The access filter also disables cache updates for interrupt context accesses if caching in interrupt context is disabled. The performance counters, when enabled, keep track of the number of cache hits and misses. The cachelines are filled up continuously one word at a time as the individual words are requested by the processor. Thus, not all words of a cacheline might be valid at a given time.

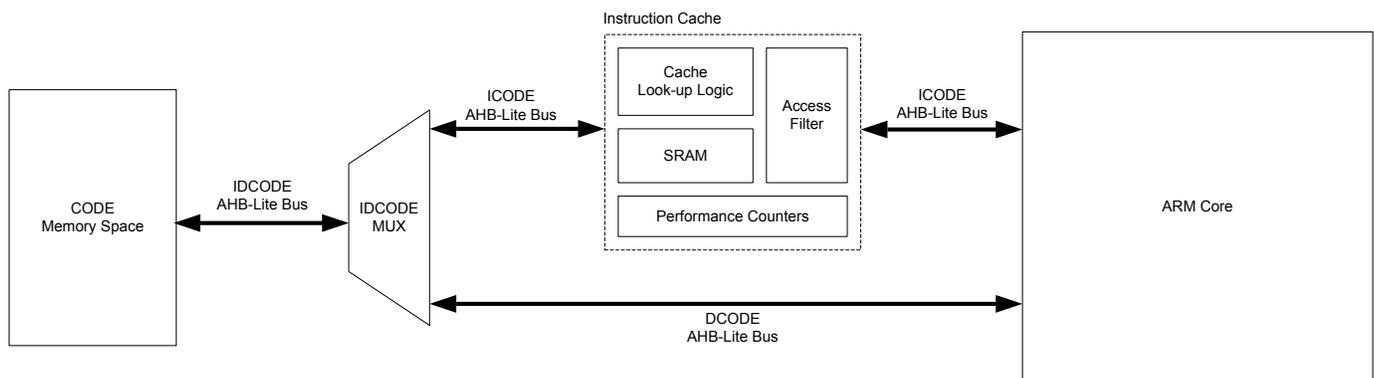


Figure 8.1. Instruction Cache

By default, the instruction cache is automatically invalidated when the contents of the flash is changed (i.e. written or erased). In many cases, however, the application only makes changes to data in the flash, not code. In this case, the automatic invalidate feature can be disabled by setting `AIDIS` in `MSC_READCTRL`. The cache can (independent of the `AIDIS` setting) be manually invalidated by writing 1 to `INVCACHE` in `MSC_CMD`.

**Note:** The instruction cache flush is not triggered at the event of a bus fault. As a result, when an instruction fetch results in a bus fault, invalid data may be cached. This means that the next time the instruction that caused the bus fault is fetched, the processor core will get the invalid cached data without any bus fault. In order to avoid invalid cached data propagation to the processor core, software should manually invalidate the instruction cache by writing 1 to `INVCACHE` in `MSC_CMD` at the event of a bus fault.

In general it is highly recommended to keep the cache enabled all the time. However, for some sections of code with very low cache hit-rate more energy-efficient execution can be achieved by disabling the cache temporarily. To measure the hit-rate of a code-section, the built-in performance counters can be used. Before the section, start the performance counters by writing 1 to `STARTPC` in `MSC_CMD`. This starts the performance counters, counting from 0. At the end of the section, stop the performance counters by writing 1 to `STOPPC` in `MSC_CMD`. The number of cache hits and cache misses for that section can then be read from `MSC_CACHEHITS` and `MSC_CACHEMISSES` respectively. The total number of 32-bit instruction fetches will be `MSC_CACHEHITS + MSC_CACHEMISSES`. Thus, the cache hit-ratio can be calculated as  $\text{MSC\_CACHEHITS} / (\text{MSC\_CACHEHITS} + \text{MSC\_CACHEMISSES})$ . When `MSC_CACHEHITS` overflows the `CHOF` interrupt flag is set. When `MSC_CACHEMISSES` overflows the `CMOF` interrupt flag is set. These flags must be cleared explicitly by software. The range of the performance counters can thus be extended by increasing a counter in the MSC interrupt routine. The performance counters only count when a cache lookup is performed. If the lookup fails, `MSC_CACHEMISSES` is increased. If the lookup is successful, `MSC_CACHEHITS` is increased. For example, a cache lookup is not performed if the cache is disabled or the code is executed from RAM.

**Note:** When caching of vector fetches and instructions in interrupt routines is disabled (`ICCDIS` in `MSC_READCTRL` is set), the performance counters do not count when these types of fetches occur (i.e. while in interrupt context).

By default, interrupt vector fetches and instructions in interrupt routines are also cached. Some applications may get better cache utilization by not caching instructions in interrupt context. This is done by setting `ICCDIS` in `MSC_READCTRL`. You should only set this bit based on the results from a cache hit ratio measurement. In general, it is recommended to keep the `ICCDIS` bit cleared. Note that look-ups in the cache are still performed, regardless of the `ICCDIS` setting - but instructions are not cached when cache misses occur inside

the interrupt routine. So, for example, if a cached function is called from the interrupt routine, the instructions for that function will be taken from the cache.

The cache content is not retained in EM2, EM3 and EM4. The cache is therefore invalidated regardless of the setting of AIDIS in MSC\_READCTRL when entering these energy modes. Applications that switch frequently between EM0 and EM2/3 and executes the very same non-looping code almost every time will most likely benefit from putting this code in RAM. The interrupt vectors can also be put in RAM to reduce current consumption even further.

### 8.3.11 Low Voltage Flash Read

The devices support low voltage flash reads. Because it takes more time to read from flash with a lower voltage supply MSC\_READCTRL.MODE should be programmed accordingly. It is recommended that software should follow certain sequences for supply voltage scaling up and down. See the EMU chapter for details.

Flash write/erase is not supported in low voltage mode. Any write/erase command will be ignored if flash is operated in a low voltage mode and the interrupt flag MSC\_IF.LVEWRITE will be set.

### 8.3.12 Erase and Write Operations

Both page erase and write operations require that the address is written into the MSC\_ADDRB register. For erase operations, the address may be any within the page to be erased. Load the address by writing 1 to the LADDRIM bit in the MSC\_WRITECMD register. The LADDRIM bit only has to be written once when loading the first address. After each word is written the internal address register ADDR will be incremented automatically by 4. The INVADDR bit of the MSC\_STATUS register is set if the loaded address is outside the flash and the LOCKED bit of the MSC\_STATUS register is set if the page addressed is locked. Any attempts to command erase of or write to the page are ignored if INVADDR or the LOCKED bits of the MSC\_STATUS register are set. To abort an ongoing erase, set the ERASEABORT bit in the MSC\_WRITECMD register.

When a word is written to the MSC\_WDATA register, the WDATAREADY bit of the MSC\_STATUS register is cleared. When this status bit is set, software or DMA may write the next word.

A single word write is commanded by setting the WRITEONCE bit of the MSC\_WRITECMD register. The operation is complete when the BUSY bit of the MSC\_STATUS register is cleared and control of the flash is handed back to the AHB interface, allowing application code to resume execution.

For a DMA write the software must write the first word to the MSC\_WDATA register and then set the WRITETRIG bit of the MSC\_WRITECMD register. DMA triggers when the WDATAREADY bit of the MSC\_STATUS register is set.

It is possible to write words twice between each erase by keeping at 1 the bits that are not to be changed. Let us take as an example writing two 16 bit values, 0xAAAA and 0x5555. To safely write them in the same flash word this method can be used:

- Write 0xFFFFAAAA (word in flash becomes 0xFFFFAAAA)
- Write 0x5555FFFF (word in flash becomes 0x5555AAAA)

#### Note:

- There is a maximum of two writes to the same word between each erase due to a physical limitation of the flash.
- Flash write/erase is not supported in low voltage mode. Any write/erase command will be ignored if flash is operated in a low voltage mode and the interrupt flag MSC\_IF.LVEWRITE will be set.
- During a write or erase, flash read accesses will be stalled, effectively halting code execution from flash. Code execution continues upon write/erase completion. Code residing in RAM may be executed during a write/erase operation.

#### 8.3.12.1 Mass Erase

A mass erase can be initiated from software using ERASEMAIN0 MSC\_WRITECMD. This command will start a mass erase of the entire flash. Prior to initiating a mass erase, MSC\_MASSLOCK must be unlocked by writing 0x631A to it. After a mass erase has been started, this register can be locked again to prevent runaway code from accidentally triggering a mass erase.

The regular flash page lock bits will not prevent a mass erase. To prevent software from initiating mass erases, use the mass erase lock bits in the mass erase lock word (MLW).

## 8.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name               | Type  | Description   |
|--------|--------------------|-------|---|
| 0x000  | MSC_CTRL           | RWH   | Memory System Control Register                        |
| 0x004  | MSC_READCTRL       | RWH   | Read Control Register                                 |
| 0x008  | MSC_WRITECTRL      | RW    | Write Control Register                                |
| 0x00C  | MSC_WRITECMD       | W1    | Write Command Register                                |
| 0x010  | MSC_ADDRB          | RW    | Page Erase/Write Address Buffer                       |
| 0x018  | MSC_WDATA          | RW    | Write Data Register                                   |
| 0x01C  | MSC_STATUS         | R     | Status Register                                       |
| 0x030  | MSC_IF             | R     | Interrupt Flag Register                               |
| 0x034  | MSC_IFS            | W1    | Interrupt Flag Set Register                           |
| 0x038  | MSC_IFC            | (R)W1 | Interrupt Flag Clear Register                         |
| 0x03C  | MSC_IEN            | RW    | Interrupt Enable Register                             |
| 0x040  | MSC_LOCK           | RWH   | Configuration Lock Register                           |
| 0x044  | MSC_CACHECMD       | W1    | Flash Cache Command Register                          |
| 0x048  | MSC_CACHEHITS      | R     | Cache Hits Performance Counter                        |
| 0x04C  | MSC_CACHEMISSES    | R     | Cache Misses Performance Counter                      |
| 0x054  | MSC_MASSLOCK       | RWH   | Mass Erase Lock Register                              |
| 0x05C  | MSC_STARTUP        | RW    | Startup Control                                       |
| 0x074  | MSC_CMD            | W1    | Command Register                                      |
| 0x090  | MSC_BOOTLOADERCTRL | RW    | Bootloader Read and Write Enable, Write Once Register |
| 0x094  | MSC_AAPUNLOCKCMD   | W1    | Software Unlock AAP Command Register                  |
| 0x098  | MSC_CACHECONFIG0   | RW    | Cache Configuration Register 0                        |



### 8.5.2 MSC\_READCTRL - Read Control Register

| Offset        | Bit Position |    |    |       |    |    |    |      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |          |          |   |   |   |        |       |        |   |  |  |
|---------------|--------------|----|----|-------|----|----|----|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|----------|----------|---|---|---|--------|-------|--------|---|--|--|
| 0x004         | 31           | 30 | 29 | 28    | 27 | 26 | 25 | 24   | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8        | 7        | 6 | 5 | 4 | 3      | 2     | 1      | 0 |  |  |
| <b>Reset</b>  |              |    |    | 0     |    |    |    | 0x1  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | 0        | 1        |   |   |   | 0      | 0     | 0      |   |  |  |
| <b>Access</b> |              |    |    | RW    |    |    |    | RWH  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | RW       | RW       |   |   |   | RW     | RW    | RW     |   |  |  |
| <b>Name</b>   |              |    |    | SCBTP |    |    |    | MODE |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | USEHPROT | PREFETCH |   |   |   | ICCDIS | AIDIS | IFCDIS |   |  |  |

| Bit   | Name     | Reset   | Access  | Description   |
|-------|----------|---|---|---|
| 31:29 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |
| 28    | SCBTP    | 0   | RW  | <b>Suppress Conditional Branch Target Prefetch</b><br><br>Enable suppressed Conditional Branch Target Prefetch (SCBTP) function. SCBTP saves energy by delaying Cortex-M conditional branch target prefetches until the conditional branch instruction is in the execute stage. When the instruction reaches this stage, the evaluation of the branch condition is completed and the core does not perform a speculative prefetch of both the branch target address and the next sequential address. With the SCBTP function enabled, one instruction fetch is saved for each branch not taken, with a negligible performance penalty.  |
| 27:26 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |
| 25:24 | MODE     | 0x1   | RWH   | <b>Read Mode</b><br><br>After reset, the core clock is 19 MHz from the HFRCO and the MODE field of MSC_READCTRL register is set to WS1. The reset value is WS1 because the HFRCO may produce a frequency above 19 MHz before it is calibrated. A large wait states is associated with high frequency. When changing to a higher frequency, this register must be set to a large wait states first before the core clock is switched to the higher frequency. When changing to a lower frequency, this register should be set to lower wait states after the frequency transition has been completed. If the HFRCO is used as clock source, wait until the oscillator is stable on the new frequency to avoid unpredictable behavior. See Flash Wait-States table for the corresponding threshold for different wait-states. |
|       | Value    | Mode  | Description   |   |
|       | 0        | WS0   | Zero wait-states inserted in fetch or read transfers  |   |
|       | 1        | WS1   | One wait-state inserted for each fetch or read transfer. See Flash Wait-States table for details    |   |
|       | 2        | WS2   | Two wait-states inserted for each fetch or read transfer. See Flash Wait-States table for details   |   |
|       | 3        | WS3   | Three wait-states inserted for each fetch or read transfer. See Flash Wait-States table for details |   |
| 23:10 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |
| 9     | USEHPROT | 0   | RW  | <b>AHB_HPROT Mode</b><br><br>Use ahb_hrpot to determine if the instruction is cacheable or not  |
| 8     | PREFETCH | 1   | RW  | <b>Prefetch Mode</b><br><br>Set to configure level of prefetching.  |
| 7:6   | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |

| Bit | Name     | Reset  | Access | Description   |
|-----|----------|--|--------|---|
| 5   | ICCDIS   | 0  | RW     | <b>Interrupt Context Cache Disable</b><br><br>Set this bit to automatically disable caching of vector fetches and instruction fetches in interrupt context. Cache lookup will still be performed in interrupt context. When set, the performance counters will not count when these types of fetches occur. |
| 4   | AIDIS    | 0  | RW     | <b>Automatic Invalidate Disable</b><br><br>When this bit is set the cache is not automatically invalidated when a write or page erase is performed.   |
| 3   | IFCDIS   | 0  | RW     | <b>Internal Flash Cache Disable</b><br><br>Disable instruction cache for internal flash memory.   |
| 2:0 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |

### 8.5.3 MSC\_WRITECTRL - Write Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |               |      |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---------------|------|---|---|
| 0x008         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3             | 2    | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0             | 0    |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | RW            | RW   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | IRQERASEABORT | WREN |   |   |

| Bit  | Name          | Reset  | Access | Description  |
|------|---------------|--|--------|--|
| 31:2 | Reserved      | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 1    | IRQERASEABORT | 0  | RW     | <b>Abort Page Erase on Interrupt</b><br><br>When this bit is set to 1, any Cortex-M interrupt aborts any current page erase operation. Executing that interrupt vector from Flash will halt the CPU. |
| 0    | WREN          | 0  | RW     | <b>Enable Write/Erase Controller</b><br><br>When this bit is set, the MSC write and erase functionality is enabled   |



### 8.5.5 MSC\_ADDRB - Page Erase/Write Address Buffer

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x010         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | ADDRB      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
|-----|------|-------|--------|-------------|

|   |       |            |    |   |
|---|-------|------------|----|---|
| 31:0  | ADDRB | 0x00000000 | RW | <b>Page Erase or Write Address Buffer</b> |
| This register holds the page address for the erase or write operation. This register is loaded into the internal MSC_ADDR register when the LADDRIM field in MSC_WRITECMD is set. |       |            |    |   |

### 8.5.6 MSC\_WDATA - Write Data Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x018         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | WDATA      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
|-----|------|-------|--------|-------------|

|  |       |            |    |                   |
|--|-------|------------|----|-------------------|
| 31:0   | WDATA | 0x00000000 | RW | <b>Write Data</b> |
| The data to be written to the address in MSC_ADDR. This register must be written when the WDATAREADY bit of MSC_STATUS is set. |       |            |    |                   |

### 8.5.7 MSC\_STATUS - Status Register

| Offset        | Bit Position       |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |           |              |             |            |         |        |      |   |
|---------------|--------------------|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|-----------|--------------|-------------|------------|---------|--------|------|---|
| 0x01C         | 31                 | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7         | 6            | 5           | 4          | 3       | 2      | 1    | 0 |
| <b>Reset</b>  | 0x0                |    |    |    | 0x0        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0         | 0            | 0           | 1          | 0       | 0      | 0    |   |
| <b>Access</b> | R                  |    |    |    | R          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | R         | R            | R           | R          | R       | R      | R    |   |
| <b>Name</b>   | PWRUPCKBDFAILCOUNT |    |    |    | WDATAVALID |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | PCRUNNING | ERASEABORTED | WORDTIMEOUT | WDATAREADY | INVADDR | LOCKED | BUSY |   |

| Bit   | Name                | Reset   | Access | Description   |
|-------|---------------------|---|--------|---|
| 31:28 | PWRUPCKBDFAIL-COUNT | 0x0   | R      | <b>Flash Power Up Checkerboard Pattern Check Fail Count</b><br><br>This field tells how many times checkboard pattern check fail occurred after a reset sequence.   |
| 27:24 | WDATAVALID          | 0x0   | R      | <b>Write Data Buffer Valid Flag</b><br><br>This field tells how many valid data in the write buffer, each bit indicates one buffer entry  |
| 23:7  | <i>Reserved</i>     | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 6     | PCRUNNING           | 0   | R      | <b>Performance Counters Running</b><br><br>This bit is set while the performance counters are running. When one performance counter reaches the maximum value, this bit is cleared.   |
| 5     | ERASEABORTED        | 0   | R      | <b>The Current Flash Erase Operation Aborted</b><br><br>When set, the current erase operation was aborted by interrupt.   |
| 4     | WORDTIMEOUT         | 0   | R      | <b>Flash Write Word Timeout</b><br><br>When this bit is set, MSC_WDATA was not written within the timeout. The flash write operation timed out and access to the flash is returned to the AHB interface. This bit is cleared when the ERASEPAGE, WRITETRIG or WRITEONCE commands in MSC_WRITECMD are triggered. |
| 3     | WDATAREADY          | 1   | R      | <b>WDATA Write Ready</b><br><br>When this bit is set, the content of MSC_WDATA is read by MSC Flash Write Controller and the register may be updated with the next 32-bit word to be written to flash. This bit is cleared when writing to MSC_WDATA.   |
| 2     | INVADDR             | 0   | R      | <b>Invalid Write Address or Erase Page</b><br><br>Set when software attempts to load an invalid (unmapped) address into ADDR  |
| 1     | LOCKED              | 0   | R      | <b>Access Locked</b><br><br>When set, the last erase or write is aborted due to erase/write access constraints  |
| 0     | BUSY                | 0   | R      | <b>Erase/Write Busy</b><br><br>When set, an erase or write operation is in progress and new commands are ignored  |

### 8.5.8 MSC\_IF - Interrupt Flag Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |          |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |          |        |      |      |       |       |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|----------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------|----------|--------|------|------|-------|-------|---|
| 0x030         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8        | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |         |          |        |      |      |       |       |   |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | 0        |   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0       | 0        | 0      | 0    | 0    | 0     | 0     |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | R        |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | R |   | R       | R        | R      | R    | R    | R     | R     | R |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | LVEWRITE |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | WDATAOV | ICACHERR | PWRUPF | CMOF | CHOF | WRITE | ERASE |   |

| Bit  | Name            | Reset   | Access | Description  |
|------|-----------------|---|--------|--|
| 31:9 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 8    | LVEWRITE        | 0   | R      | <b>Flash LVE Write Error Flag</b><br>If one, flash controller write command received while in LVE mode                               |
| 7    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 6    | WDATAOV         | 0   | R      | <b>Flash Controller Write Buffer Overflow</b><br>If one, flash controller write buffer overflow detected                             |
| 5    | ICACHERR        | 0   | R      | <b>iCache RAM Parity Error Flag</b><br>If one, iCache RAM parity Error detected  |
| 4    | PWRUPF          | 0   | R      | <b>Flash Power Up Sequence Complete Flag</b><br>Set after MSC_CMD.PWRUP received, flash powered up complete and ready for read/write |
| 3    | CMOF            | 0   | R      | <b>Cache Misses Overflow Interrupt Flag</b><br>Set when MSC_CACHEMISSES overflows  |
| 2    | CHOF            | 0   | R      | <b>Cache Hits Overflow Interrupt Flag</b><br>Set when MSC_CACHEHITS overflows  |
| 1    | WRITE           | 0   | R      | <b>Write Done Interrupt Read Flag</b><br>Set when a write is done  |
| 0    | ERASE           | 0   | R      | <b>Erase Done Interrupt Read Flag</b><br>Set when erase is done  |

## 8.5.9 MSC\_IFS - Interrupt Flag Set Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |          |   |   |   |   |   |   |   |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |         |          |        |      |      |       |       |  |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|----------|---|---|---|---|---|---|---|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---------|----------|--------|------|------|-------|-------|--|----|
| 0x034         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8        | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |         |          |        |      |      |       |       |  |    |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | 0        |   | 0 |   | 0 |   | 0 |   | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0       |          | 0      |      | 0    |       | 0     |  |    |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | W1       |   |   |   |   |   |   |   |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  | W1      |          | W1     |      | W1   |       | W1    |  | W1 |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | LVEWRITE |   |   |   |   |   |   |   |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  | WDATAOV | ICACHERR | PWRUPF | CMOF | CHOF | WRITE | ERASE |  |    |

| Bit  | Name     | Reset   | Access | Description  |
|------|----------|---|--------|--|
| 31:9 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 8    | LVEWRITE | 0   | W1     | <b>Set LVEWRITE Interrupt Flag</b><br>Write 1 to set the LVEWRITE interrupt flag |
| 7    | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 6    | WDATAOV  | 0   | W1     | <b>Set WDATAOV Interrupt Flag</b><br>Write 1 to set the WDATAOV interrupt flag   |
| 5    | ICACHERR | 0   | W1     | <b>Set ICACHERR Interrupt Flag</b><br>Write 1 to set the ICACHERR interrupt flag |
| 4    | PWRUPF   | 0   | W1     | <b>Set PWRUPF Interrupt Flag</b><br>Write 1 to set the PWRUPF interrupt flag     |
| 3    | CMOF     | 0   | W1     | <b>Set CMOF Interrupt Flag</b><br>Write 1 to set the CMOF interrupt flag         |
| 2    | CHOF     | 0   | W1     | <b>Set CHOF Interrupt Flag</b><br>Write 1 to set the CHOF interrupt flag         |
| 1    | WRITE    | 0   | W1     | <b>Set WRITE Interrupt Flag</b><br>Write 1 to set the WRITE interrupt flag       |
| 0    | ERASE    | 0   | W1     | <b>Set ERASE Interrupt Flag</b><br>Write 1 to set the ERASE interrupt flag       |

### 8.5.10 MSC\_IFC - Interrupt Flag Clear Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |          |   |         |          |        |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|----------|---|---------|----------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0x038         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8        | 7 | 6       | 5        | 4      | 3     | 2     | 1     | 0     |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | 0        |   | 0       | 0        | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | (R)W1    |   | (R)W1   | (R)W1    | (R)W1  | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | LVEWRITE |   | WDATAOV | ICACHERR | PWRUPF | CMOF  | CHOF  | WRITE | ERASE |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |

| Bit  | Name     | Reset   | Access | Description   |
|------|----------|---|--------|---|
| 31:9 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 8    | LVEWRITE | 0   | (R)W1  | <b>Clear LVEWRITE Interrupt Flag</b><br><br>Write 1 to clear the LVEWRITE interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 7    | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 6    | WDATAOV  | 0   | (R)W1  | <b>Clear WDATAOV Interrupt Flag</b><br><br>Write 1 to clear the WDATAOV interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |
| 5    | ICACHERR | 0   | (R)W1  | <b>Clear ICACHERR Interrupt Flag</b><br><br>Write 1 to clear the ICACHERR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 4    | PWRUPF   | 0   | (R)W1  | <b>Clear PWRUPF Interrupt Flag</b><br><br>Write 1 to clear the PWRUPF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 3    | CMOF     | 0   | (R)W1  | <b>Clear CMOF Interrupt Flag</b><br><br>Write 1 to clear the CMOF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).         |
| 2    | CHOF     | 0   | (R)W1  | <b>Clear CHOF Interrupt Flag</b><br><br>Write 1 to clear the CHOF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).         |
| 1    | WRITE    | 0   | (R)W1  | <b>Clear WRITE Interrupt Flag</b><br><br>Write 1 to clear the WRITE interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).       |
| 0    | ERASE    | 0   | (R)W1  | <b>Clear ERASE Interrupt Flag</b><br><br>Write 1 to clear the ERASE interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).       |

### 8.5.11 MSC\_IEN - Interrupt Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |          |   |         |          |        |      |      |       |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |  |  |  |  |  |  |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|----------|---|---------|----------|--------|------|------|-------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--|--|--|--|--|--|--|--|
| 0x03C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8        | 7 | 6       | 5        | 4      | 3    | 2    | 1     | 0     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |  |  |  |  |  |  |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | 0        |   | 0       | 0        | 0      | 0    | 0    | 0     | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |  |  |  |  |  |  |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | RW       |   | RW      | RW       | RW     | RW   | RW   | RW    | RW    | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |  |  |  |  |  |  |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | LVEWRITE |   | WDATAOV | ICACHERR | PWRUPF | CMOF | CHOF | WRITE | ERASE |    |    |    |    |    |    |    |    |    |    |    |    |    |    |  |  |  |  |  |  |  |  |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 31:9 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 8    | LVEWRITE        | 0   | RW     | <b>LVEWRITE Interrupt Enable</b><br>Enable/disable the LVEWRITE interrupt |
| 7    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 6    | WDATAOV         | 0   | RW     | <b>WDATAOV Interrupt Enable</b><br>Enable/disable the WDATAOV interrupt   |
| 5    | ICACHERR        | 0   | RW     | <b>ICACHERR Interrupt Enable</b><br>Enable/disable the ICACHERR interrupt |
| 4    | PWRUPF          | 0   | RW     | <b>PWRUPF Interrupt Enable</b><br>Enable/disable the PWRUPF interrupt     |
| 3    | CMOF            | 0   | RW     | <b>CMOF Interrupt Enable</b><br>Enable/disable the CMOF interrupt         |
| 2    | CHOF            | 0   | RW     | <b>CHOF Interrupt Enable</b><br>Enable/disable the CHOF interrupt         |
| 1    | WRITE           | 0   | RW     | <b>WRITE Interrupt Enable</b><br>Enable/disable the WRITE interrupt       |
| 0    | ERASE           | 0   | RW     | <b>ERASE Interrupt Enable</b><br>Enable/disable the ERASE interrupt       |

### 8.5.12 MSC\_LOCK - Configuration Lock Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |         |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---------|
| 0x040         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |         |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0x0000  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | RWH     |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | LOCKKEY |

| Bit   | Name            | Reset  | Access                     | Description   |
|-------|-----------------|--|----------------------------|---|
| 31:16 | Reserved        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |                            |   |
| 15:0  | LOCKKEY         | 0x0000   | RWH                        | <b>Configuration Lock</b><br><br>Write any other value than the unlock code to lock access to MSC_CTRL, MSC_READCTRL, MSC_WRITECMD, MSC_STARTUP and MSC_AAPUNLOCKCMD. Write the unlock code to enable access. When reading the register, bit 0 is set when the lock is enabled. |
|       | Mode            | Value  | Description                |   |
|       | Read Operation  |  |                            |   |
|       | UNLOCKED        | 0  | MSC registers are unlocked |   |
|       | LOCKED          | 1  | MSC registers are locked   |   |
|       | Write Operation |  |                            |   |
|       | LOCK            | 0  | Lock MSC registers         |   |
|       | UNLOCK          | 0x1B71   | Unlock MSC registers       |   |

### 8.5.13 MSC\_CACHECMD - Flash Cache Command Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |         |          |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|---------|----------|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x044         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14      | 13       | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0      | 0       | 0        | 0  |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W1     | W1      | W1       | W1 |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | STOPPC | STARTPC | INVCACHE |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name     | Reset   | Access | Description   |
|------|----------|---|--------|---|
| 31:3 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 2    | STOPPC   | 0   | W1     | <b>Stop Performance Counters</b><br>Use this command bit to stop the performance counters.  |
| 1    | STARTPC  | 0   | W1     | <b>Start Performance Counters</b><br>Use this command bit to start the performance counters. The performance counters always start counting from 0. |
| 0    | INVCACHE | 0   | W1     | <b>Invalidate Instruction Cache</b><br>Use this register to invalidate the instruction cache.   |

### 8.5.14 MSC\_CACHEHITS - Cache Hits Performance Counter

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |           |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x048         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CACHEHITS |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name      | Reset   | Access | Description   |
|-------|-----------|---|--------|---|
| 31:20 | Reserved  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 19:0  | CACHEHITS | 0x00000   | R      | <b>Cache Hits Since Last Performance Counter Start Command</b><br>Use to measure cache performance for a particular code section. |

8.5.15 MSC\_CACHEMISSES - Cache Misses Performance Counter

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x04C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18          | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000     |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    | R           |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    | CACHEMISSES |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name        | Reset   | Access | Description   |
|-------|-------------|---|--------|---|
| 31:20 | Reserved    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 19:0  | CACHEMISSES | 0x00000   | R      | <b>Cache Misses Since Last Performance Counter Start Command</b><br>Use to measure cache performance for a particular code section. |

8.5.16 MSC\_MASSLOCK - Mass Erase Lock Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x054         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15             | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LOCKKEY 0x0001 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LOCKKEY        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description |
|-------|----------|--|--------|-------------|
| 31:16 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |             |

15:0 LOCKKEY 0x0001 RWH **Mass Erase Lock**  
 Write any other value than the unlock code to lock access the the ERASEMAINn commands. Write the unlock code 631A to enable access. When reading the register, bit 0 is set when the lock is enabled. Locked by default.

| Mode            | Value  | Description         |
|-----------------|--------|---------------------|
| Read Operation  |        |                     |
| UNLOCKED        | 0      | Mass erase unlocked |
| LOCKED          | 1      | Mass erase locked   |
| Write Operation |        |                     |
| LOCK            | 0      | Lock mass erase     |
| UNLOCK          | 0x631A | Unlock mass erase   |



### 8.5.18 MSC\_CMD - Command Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------|
| 0x074         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0     |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0     |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | W1    |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | PWRUP |

| Bit  | Name     | Reset  | Access | Description  |
|------|----------|--|--------|--|
| 31:1 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 0    | PWRUP    | 0  | W1     | <b>Flash Power Up Command</b><br>Write to this bit to power up the Flash. IRQ PWRUPF will be fired when power up sequence completed. |

### 8.5.19 MSC\_BOOTLOADERCTRL - Bootloader Read and Write Enable, Write Once Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |        |        |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|--------|--------|
| 0x090         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0      |        |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0      | 0      |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | RW     | RW     |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | BLWDIS | BLRDIS |

| Bit  | Name     | Reset  | Access | Description  |
|------|----------|--|--------|--|
| 31:2 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 1    | BLWDIS   | 0  | RW     | <b>Flash Bootloader Write/Erase Disable</b><br>Controls write/erase access of the flash bootloader pages. When cleared, write/erase is enabled. When set, write/erase is disabled. |
| 0    | BLRDIS   | 0  | RW     | <b>Flash Bootloader Read Disable</b><br>Controls read access of the flash bootloader pages. When cleared, read is enabled. When set, read is disabled.                             |

8.5.20 MSC\_AAPUNLOCKCMD - Software Unlock AAP Command Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |           |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-----------|
| 0x094         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0         |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0         |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | W1        |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | UNLOCKAAP |

| Bit  | Name      | Reset  | Access | Description   |
|------|-----------|--|--------|---|
| 31:1 | Reserved  | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 0    | UNLOCKAAP | 0  | W1     | <b>Software Unlock AAP Command</b><br><br>Write to this bit to unlock AAP. This is only possible when bit 31 of the AAP Lock Word (ALW) in flash is set to 1. If bit 31 of the ALW has been cleared to 0, this command has no effect. Register is writable only when MSC_LOCK is unlocked |

8.5.21 MSC\_CACHECONFIG0 - Cache Configuration Register 0

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |             |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-------------|----|
| 0x098         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1           | 0  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | 1           | 0  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | RW          | RW |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | CACHEPLEVEL |    |

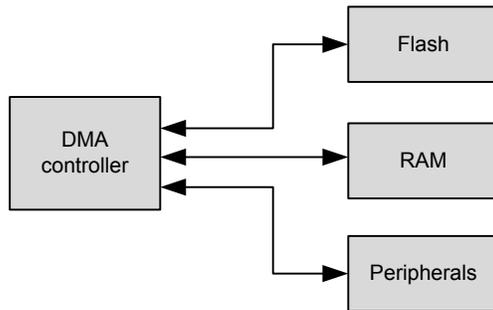
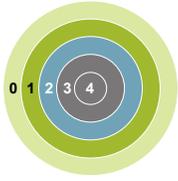
| Bit  | Name            | Reset   | Access | Description |
|------|-----------------|---|--------|-------------|
| 31:2 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in 1.2 Conventions</i> |        |             |

1:0    CACHEPLEVEL    0x3    RW    **Instruction Cache Low-Power Level**

Use this to set the low-power level of the cache. In general, the default setting is best for most applications.

| Value | Mode        | Description   |
|-------|-------------|---|
| 0     | BASE        | Base instruction cache functionality.   |
| 1     | ADVANCED    | Advanced buffering mode, where the cache uses the fetch pattern to predict highly accessed data and store it in low-energy memory.  |
| 3     | MINACTIVITY | Minimum activity mode, which allows the cache to minimize activity in logic that it predicts has a low probability being used. This mode can introduce wait-states into the instruction fetch stream when the cache exits one of its low-activity states. The number of wait-states introduced is small, but users running with 0-wait-state memory and wishing to reduce the variability that the cache might introduce with additional wait-states may wish to lower the cache low-power level. Note, this mode includes the advanced buffering mode functionality. |

## 9. LDMA - Linked DMA Controller



### Quick Facts

#### What?

The LDMA controller can move data without CPU intervention, effectively reducing the energy consumption for a data transfer.

#### Why?

The LDMA can perform data transfers more energy efficiently than the CPU and allows autonomous operation in low energy modes. For example the LEUART can provide full UART communication in EM2 Deep Sleep, consuming only a few  $\mu\text{A}$  by using the LDMA to move data between the LEUART and RAM.

#### How?

The LDMA controller has multiple highly configurable, prioritized DMA channels. A linked list of flexible descriptors makes it possible to tailor the controller to the specific needs of an application.

### 9.1 Introduction

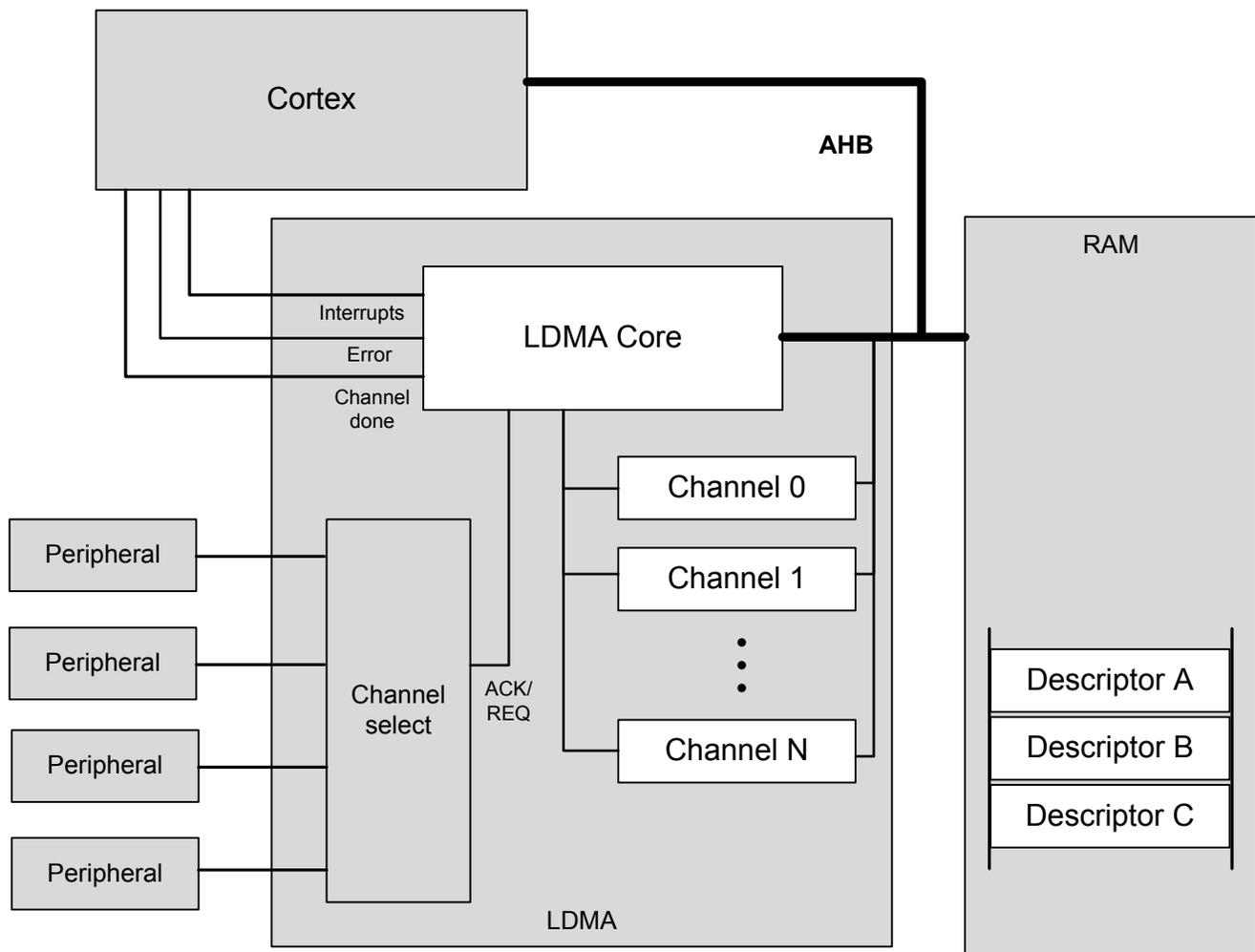
The Linked Direct Memory Access (LDMA) controller performs memory transfer operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes while still routing data to memory and peripherals. For example, moving data from the LEUART to memory or memory to LEUART. Each of the DMA channels on the EFR32 can be connected to any of the EFR32 peripherals.

### 9.1.1 Features

- Flexible Source and Destination transfers
  - Memory-to-memory
  - Memory-to-peripheral
  - Peripheral-to-memory
  - Peripheral-to-peripheral
- DMA transfers triggered by peripherals, software, or linked list
- Single or multiple data transfers for each peripheral or software request
- Inter-channel and hardware event synchronization via trigger and wait functions
- Supports single or multiple descriptors
  - Single descriptor
  - Linked list of descriptors
  - Circular and ping-pong buffers
  - Scatter-Gather
  - Looping
  - Pause and restart triggered by other channels
  - Sophisticated flow control which can function without CPU interaction
- Channel arbitration includes:
  - Fixed priority
  - Simple round robin
  - Round robin with programmable multiple interleaved entries for higher priority requesters
- Programmable data size and source and destination address strides
- Programmable interrupt generation at the end of each DMA descriptor execution
- Little-endian/big-endian conversion
- DMA write-immediate function

## 9.2 Block Diagram

An overview of the LDMA and the modules it interacts with is shown in [Figure 9.1 LDMA Block Diagram on page 191](#).



**Figure 9.1. LDMA Block Diagram**

The Linked DMA Controller consists of three main parts

- A DMA core that executes transfers and communicates status to the core
- A channel select block that routes peripheral DMA requests and acknowledge signals to the DMA
- A set of internal channel configuration registers for tracking the progress of each DMA channel

The DMA has access to all system memory through the AHB bus and the AHB->APB bridge. It can load channel descriptors from memory with no CPU intervention.

### 9.3 Functional Description

The Linked DMA Controller is highly flexible. It is capable of transferring data between peripherals and memory without involvement from the processor core. This can be used to increase system performance by off-loading the processor from copying large amounts of data or avoiding frequent interrupts to service peripherals needing more data or having available data. It can also be used to reduce the system energy consumption by making the LDMA work autonomously with some EM2/3 peripherals for data transfer without having to wake up the processor core from sleep.

The Linked DMA Controller has 8 independent channels. Each of these channels can be connected to any of the available peripheral DMA transfer request input sources by writing to the channel configuration registers, see [9.3.2 Channel Configuration](#). In addition, each channel can also be triggered directly by software, which is useful for memory-to-memory transfers.

The channel descriptors determine what the Linked DMA Controller will do when it receives DMA transfer request. The initial descriptor is written directly to the LDMA's channel registers. If desired, the initial descriptor can link to additional linked descriptors stored in memory (RAM or Flash). Alternatively, software may also load the initial descriptor by writing the descriptor address to the LDMA\_CHx\_LINK register and then setting the corresponding bit the LDMA\_LINKLOAD register.

Before enabling a channel, the software must take care to properly configure the channel registers including the link address and any linked descriptors. When a channel is triggered, the Linked DMA Controller will perform the memory transfers as specified by the descriptors. A descriptor contains the memory address to read from, the memory address to write to, link address of the next descriptor, the number of bytes to be transferred, etc. The channel descriptor is described in detail in [9.3.7 Channel Descriptor Data Structure](#).

The Linked DMA Controller supports both fixed priority and round robin arbitration. The number of fixed and round robin channels is programmable. For round robin channels, the number of arbitration slots requested for each channel is programmable. Using this scheme, it is possible to ensure that timing-critical transfers are serviced on time.

DMA transfers take place by reading a block of data at a time from the source, storing it in the LDMA's local FIFO, then writing the block out to the destination from the FIFO. Interrupts may optionally be signaled to the CPU's interrupt controller at the end of any DMA transfer or at the completion of a descriptor if the DONEIFSEN bit is set. An AHB error will always generate an interrupt.

#### 9.3.1 Channel Descriptor

Each DMA channel has descriptor registers. A transfer can be initialized by software writing to the registers or by the DMA itself copying a descriptor from RAM to memory. When using a linked list of descriptors the first descriptor should be initialized by the CPU. The DMA itself will then copy linked descriptors to its descriptor registers as required. In addition to manually initializing the first transfer, software may also cause the LDMA to load the initial descriptor by writing the descriptor address to the LDMA\_CHx\_LINK register and then setting the corresponding bit the LDMA\_LINKLOAD register.

The contents of the descriptor registers are dynamically updated during the DMA transfer. The contents of descriptors in memory are not edited by the controller.

Some descriptor field values are only used for linked descriptors. For example, the SRCMODE and DSTMODE bits of the LDMA\_CHx\_CTRL registers determine if a linked descriptor is using relative or absolute addressing. Software writes to the address registers will always use absolute addressing and never set these bits. Therefore, these bits are read only.

##### 9.3.1.1 DMA Transfer Size

A DMA transfer is the smallest unit of data that can be transferred by the LDMA. The LDMA supports byte, half-word and word sized transfers. The SIZE field in the LDMA\_CHx\_CTRL register specifies the data width of one DMA transfer.

##### 9.3.1.2 Source/Destination Increments

The SRCINC and DSTINC in the LDMA\_CHx\_CTRL register determines the increment between DMA transfers. The increment is in units of DMA transfers and using an increment size of 1 will transfer contiguous bytes, half-words, or words depending on the value of the SIZE field. Multiple unit increments are useful for transferring or packing/unpacking aligned data. For example using an increment of 4 with a size of BYTE will transfer word aligned bytes. An increment of 2 units with a size of HALFWORD is suitable for the transfer of word aligned half-word data. The LDMA can also pack or unpack data by using a different increment size for source and destination. For example - to convert from word aligned byte data (unpacked) to contiguous byte data (packed), set the SIZE to BYTE, SRCINC to 4, and DSTINC to 1.

SRCINC or DSTINC may also be set to NONE which will cause the LDMA to read or write the same location for every DMA transfer. This is useful for accessing peripheral FIFO or data registers.

### 9.3.1.3 Block Size

The block size defines the amount of data transferred in one arbitration. It consists of one or more DMA transfers. See [9.3.6.1 Arbitration Priority](#) for more details.

### 9.3.1.4 Transfer Count

The descriptor transfer count defines how many DMA transfers to perform. The number of bytes transferred by the descriptor will depend on both the transfer count XFERCNT and the SIZE field settings.  $TOTAL\_BYTES = XFERCNT * SIZE$

### 9.3.1.5 Descriptor List

A descriptor list consists of one or more descriptors which are executed in serially. This list may be a simple sequence of descriptors, a loop of descriptors, or a combination of the two.

Each descriptor in the list can be one of several types.

- Single Transfer descriptor: Transfers TOTAL\_BYTES of data and then stops.
- Linked Transfer descriptor: Transfers TOTAL\_BYTES of data and then loads the next linked descriptor.
- Loop Transfer descriptor: Transfers TOTAL\_BYTES of data and performs loop control (see [9.3.2.2 Loop Counter](#)).
- Sync descriptor: Handle synchronization of the list with other entities (see [9.3.7.2 SYNC Descriptor Structure](#)).
- WRI descriptor: Writes a value to a location in memory (see [9.3.7.3 WRI Descriptor Structure](#)).

### 9.3.1.6 Addresses

Before initiating a transfer, software should write the source address, destination address, and if applicable the link address to the descriptor registers. Alternatively, software may load a descriptor from memory by writing the descriptor address to the LDMA\_CHx\_LINK register and setting the corresponding bit in the LDMA\_LINKLOAD register.

During a DMA transfer, the DMA source and destination address registers are pointers to the next transfer address. The LDMA will update the SRC and DST addresses after each transfer. If software halts a DMA transfer by clearing the enable bit, the SRC and DST addresses will indicate the next transfer address.

When a descriptor is finished the DMA will either halt or load the next (linked) descriptor depending on the value of the LINK field in the LDMA\_Chx\_LINK register. After loading a linked descriptor, the descriptor registers will reflect the content of the loaded descriptor. Note that the linked descriptor must be word aligned in memory. The two least significant bits of the LDMA\_CHx\_LINK register are used by the LINK and LINKMODE bits. The two least significant bits of the link address are always zero.

### 9.3.1.7 Addressing Modes

The DMA descriptors support absolute addressing or relative addressing. When using relative addressing, the offset is relative to the current contents of the respective address registers. Regardless of the descriptor addressing modes, the address registers always indicate the absolute address. For example, when loading a descriptor using relative SRC addressing, the LDMA will add the descriptor source address (offset) to the contents of the SRCADDR register (base address). After loading, the SRCADDR register will indicate the absolute address of the loaded descriptor.

The initial descriptor must use absolute addressing. The LDMA will ignore the DSTMODE, SRCMODE, and LINKMODE bits for the initial descriptor and interpret the addresses as an absolute addresses.

Relative addressing is most useful for the link address. The initial descriptor will indicate the absolute address of the linked descriptors in memory. The linked descriptors might be an array of structures. In this case the offset between descriptors is constant and is always 4 words or 16 bytes (each descriptor has 4 words). The LINK address is not incremented or decremented after each transfer. Thus, a relative offset of 0x10 may be used for all linked descriptors.

The source and destination addresses also support relative addressing. When using relative addressing with the source or destination address registers, the LDMA adds the relative offset to the current contents of the respective address register. Since the source and destination addresses are normally incremented after each transfer, the final address will point to one unit past the last transfer. Thus, an offset of zero will give the next sequential data address.

See the example [9.4.6 2D Copy](#) for an common use of relative addressing.

### 9.3.1.8 Byte Swap

Enabling byte swap reverses the endianness of the incoming source data read into the LDMA's FIFO. Byte swap is only valid for transfer sizes of word and half-word. Note that linked structure reads are not byte swapped.

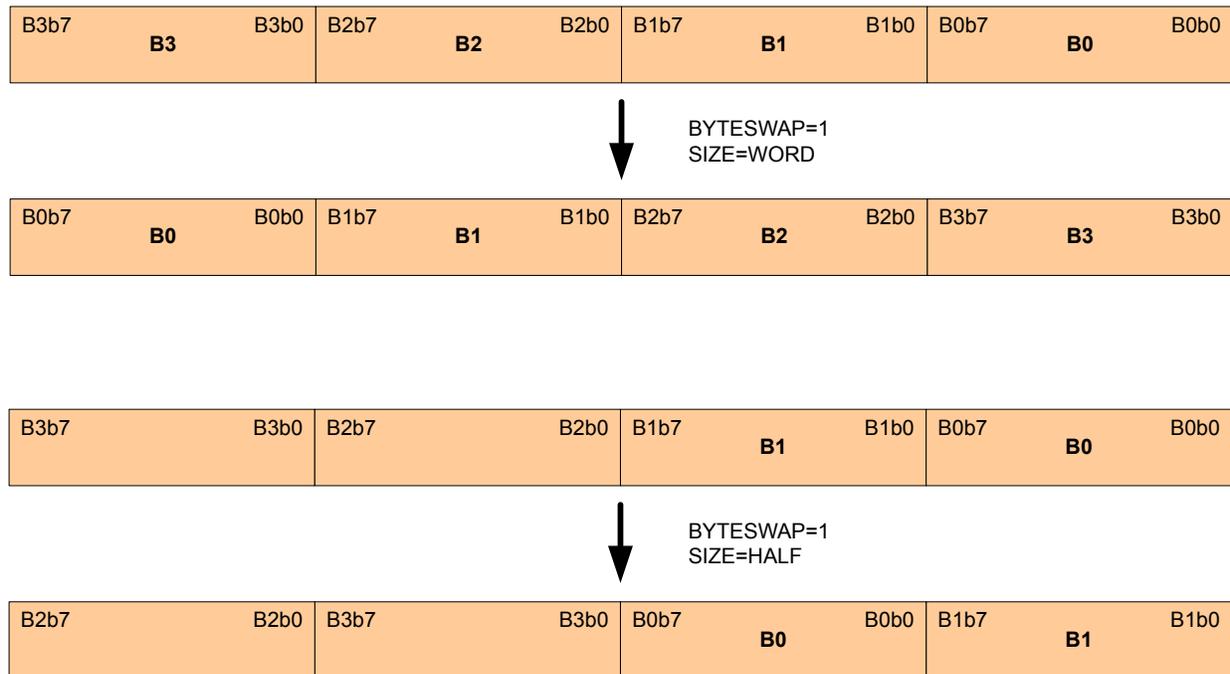


Figure 9.2. Word and Half-Word Endian Byte Swap Examples



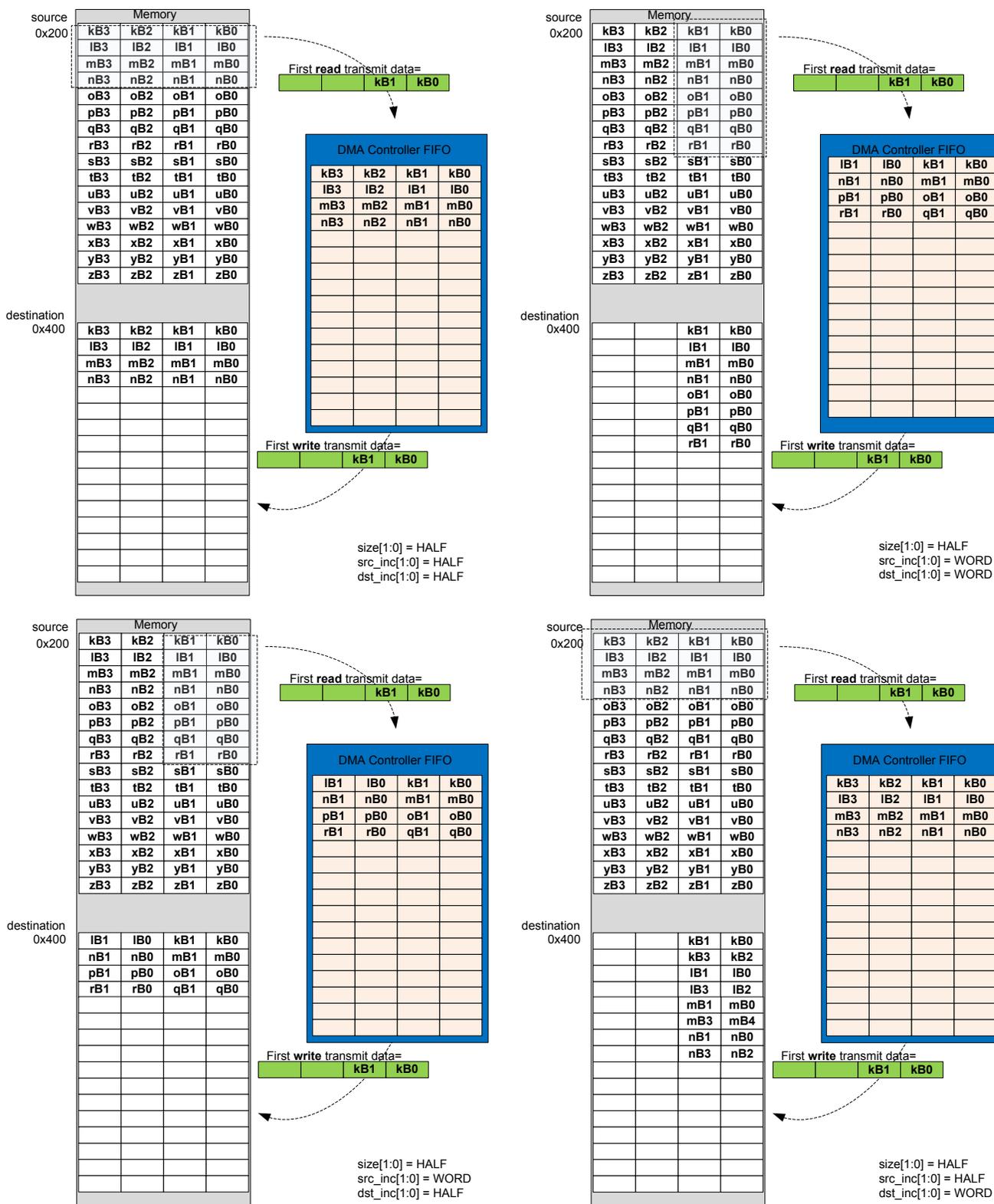


Figure 9.4. Memory-to-Memory Transfer HALF Size Examples

Fields SRCINCSIGN and DSTINCSIGN allow for address decrement. These can be used to mirror an image, for example, in the pixel copy application.

### 9.3.2 Channel Configuration

Each DMA channel has associated configuration and loop counter registers for controlling direction of address increment, arbitration slots, and descriptor looping.

#### 9.3.2.1 Address Increment/Decrement

Normally DMA transfers increment the source and destination addresses after each DMA transfer. Each channel is also capable of decrementing the source and/or destination addresses after each DMA transfer. This may be useful for flipping an array or copying data from tail to head. For example, a data packet might be prepared as an array of data with increasing addresses and then transmitted from the highest address to the lowest address, from tail to head.

After reset the SRCINCSIGN and DSTINCSIGN bits in the LDMA\_CHx\_CFG register are cleared causing the source and destination addresses to increment after each transfer. If the SRCINCSIGN bit is set, the DMA will decrement the source address after each transfer. If the DSTINCSIGN bit in the LDMA\_CHx\_CFG register is set, the DMA will decrement the destination address after each transfer. Setting only one of these bits will flip the data. Setting both bits will copy from tail to head, but will not flip the data.

The SRCINCSIGN and DSTINCSIGN bits apply to all descriptors used by that channel. Software should take care to set the starting source and/or destination address to the highest data address when decrementing.

#### 9.3.2.2 Loop Counter

Each channel has a LDMA\_CHx\_LOOP register that includes a loop counter field. To use looping, software should initialize the loop counter with the desired number of repetitions before enabling the transfer. A descriptor with the DECLOOPCNT bit set to TRUE will repeat the loop and decrement the loop counter until LOOPCNT = 0.

For a looping descriptor, with DECLOOPCNT=1, the LINK address in the LDMA\_CHx\_LINK register is used as the loop address. While LOOPCNT is greater than zero, the descriptor will execute and then the LDMA will load the next descriptor using the address specified in the LDMA\_CHx\_LINK register. This feature enables looping of multiple descriptors. To repeat a single descriptor, the LINK address of the descriptor should point to itself.

After LOOPCNT reaches zero, if the LINK bit in the descriptor LINK word is clear the transfer stops. If the LINK bit is set, the LDMA will load the next sequential descriptor located immediately following the looping descriptor. The behavior of the LINK bit is different for a looping descriptor. This is necessary because the LINK address is re-purposed as the loop address for a looping descriptor.

Note that LOOPCNT sets the number of repeats, not the number of iterations. The total number of loop iterations will be LOOPCNT plus 1. Normally, the LOOPCNT should be set to one or more repeats.

Also note that because there is only one LOOPCNT per channel, software intervention is required to update the LOOPCNT if a sequence of transfers contains multiple loops. It is also possible to use a write immediate DMA data transfer to update the LDMA\_CHx\_LOOP register.

### 9.3.3 Channel Select Configuration

The channel select block determines which peripheral request signal connects to each DMA channel.

This configuration is done by software through the SOURCESEL and SIGSEL fields of the LDMA\_CHn\_REQSEL register. SOURCESEL selects the peripheral and SIGSEL picks which DMA request signals to use from the selected peripheral.

#### 9.3.4 Starting a Transfer

A transfer may be started by software, a peripheral request, or a descriptor load.

Software may initiate a transfer by setting the bit for the desired channel in the LDMA\_SREQ register. In this case the channel should set SOURCESEL to NONE to prevent unintentional triggering of the channel by a peripheral.

A peripheral may trigger the channel by configuring the peripheral source and signal as described in [9.3.3 Channel Select Configuration](#)

The LDMA may also be configured to begin a transfer immediately after a new descriptor is loaded by setting the STRUCTREQ field of the LDMA\_CHx\_CTRL register or descriptor word.

This configuration is done by software through the SOURCESEL and SIGSEL fields of the LDMA\_CHn\_REQSEL register. SOURCESEL selects the peripheral and SIGSEL picks which DMA request signals to use from the selected peripheral.

### 9.3.4.1 Peripheral Transfer Requests

By default peripherals issue a Single Request (SREQ) when any data is present. For peripherals with a data buffer or FIFO this occurs any time the FIFO is not empty. Upon receiving an SREQ the LDMA will perform one DMA transfer and stop till another request is made.

It is generally more efficient to wait for a peripheral to accumulate data and transfer in a burst. This both reduces overhead of the DMA engine and allows EM2 peripherals to save power by using the LDMA less often. To enable this set the IGNORESREQ bit in the LDMA\_CHx\_CTRL register (or descriptor) which will cause the LDMA to ignore SREQ's and wait for a full Request (REQ) signal. When the REQ is received the entire descriptor will be executed. For most peripherals with a FIFO the REQ signal is set when the FIFO is full, or a predetermined threshold has been reached. See the individual peripheral chapters for more information.

### 9.3.5 Managing Transfer Errors

LDMA transfer errors are normally managed using interrupts. Software should clear the ERROR flag in the bit in the LDMA\_IF register and enable error interrupts by setting the ERROR bit in the LDMA\_IEN register before initiating a DMA transfer.

The LDMA interrupt handler should check the ERROR flag bit in the LDMA\_IF register. If the ERROR flag bit is set, it should then read the CHERROR field in the LDMA\_STATUS register to determine the errant channel. The interrupt handler should reset the channel and clear the ERROR flag bit in the LDMA\_IF register before returning.

### 9.3.6 Arbitration

While multiple channels are configured simultaneously the LDMA engine can only be actively copying data for one channel at a time. Arbitration determines which channel is being serviced at any point in time. The LDMA will choose a channel through arbitration, transfer BLOCK\_SIZE elements of that channel and then arbitrate again choosing another channel to service. This allows high priority channels to be serviced while lower priority channels are in the middle of a transfer.

#### 9.3.6.1 Arbitration Priority

There are two modes in determining priority when the controller arbitrates: fixed priority and round robin priority.

In fixed priority mode, channel 0 has the highest priority. As the channel number increases, the priority decreases. When the LDMA controller is idle or when a transfer completes, the highest priority channel with an active request is granted the transfer. This mode guarantees smallest latency for the highest priority requesters. It is best suited for systems where peak bandwidth is well below LDMA controller's maximum ability to serve. The drawback of this mode is the possibility of starvation for lowest priority requesters.

In the round robin priority mode, each active requesting channel is serviced in the order of priority. A late arriving request on a higher priority channel will not get serviced until the next round. This mode minimizes the risk of starving low-priority latency-tolerant requesters. The drawback of this mode is higher risk of starving low-latency requesters.

The NUMFIXED field in the LDMA\_CTRL register determines which channels are fixed priority and which are round robin. Channels lower than NUMFIXED are fixed priority while those above it are round robin. A value of 0x0 implies all channels are round robin. A value of 0x4 implies channels 0 through 3 are fixed priority and 4 through 7 are round robin. A value of 7 implies that channels 0 through 6 are fixed and channel 7 is round robin. This is functionally equivalent to having 8 fixed priority channels.

Fixed priority channels always take priority over round robin. As long as NUMFIXED is greater than 0, there is a possibility that a higher priority channel can starve the remaining channels.

To address the drawbacks of using fixed priority or round robin priority the LDMA implements the concept of arbitration slots. This allows for channels to have high bandwidth and low latency while preventing starvation of latency tolerant low priority channels.

Each channel has a two bit ARBSLOT field in its LDM\_CHx\_CFG register. This field only applies to channels marked as round robin (determined by NUMFIXED). The channels in the same arbitration slot are treated equally with round robin scheduling. Channels marked with a higher arbitration slot will get serviced more frequently. By default all channels are placed in arbitration slot 1.

Every time the channels in slot 1 get serviced the channels in slot 2 get serviced twice, those in slot 4 get serviced 4 times, and those in slot 8 get serviced 7 times. The specific arbitration allocation can be seen by the following table. The highest arbitration slot is serviced every other arbitration cycle, allowing for low latency response. If there are no requests from channels in arbitration slot then that slot is immediately skipped.

**Table 9.1. Arbitration Slot Order**

| Arbslot order | 8 | 4 | 8 | 2 | 8 | 4 | 8 | 1 | 8 | 4 | 8 | 2 | 8 | 4 |
|---------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Arbslot1      |   |   |   |   |   |   |   | 1 |   |   |   |   |   |   |
| Arbslot2      |   |   |   | 1 |   |   |   |   |   |   |   | 1 |   |   |
| Arbslot4      |   | 1 |   |   |   | 1 |   |   |   | 1 |   |   |   | 1 |
| Arbslot8      | 1 |   | 1 |   | 1 |   | 1 |   | 1 |   | 1 |   | 1 |   |

The top row shows the order at which the arbitration slots are executed. The remaining part of the table shows a more visual interpretation of the arbitration order.

For example, if we have one low latency channel (CHNL0) and two latency tolerant channels (CHNL1 and CHNL2). We could use the following settings.

LDMA\_CTRL.NUMFIXED = 0; set round robin for all channels.

CHNL0\_CFG.ARBSLOTS = TWO;

CHNL1\_CFG.ARBSLOTS = ONE;

CHNL2\_CFG.ARBSLOTS = ONE;

If all channels are constantly requesting transfers, then the arbitration order is: CHNL0, CHNL1, CHNL0, CHNL2, CHNL0, CHNL1, CHNL0, CHNL2, CHNL0, etc

Note, there are no channels assigned to arbitration slot four or eight in this example, so those slots are skipped and the final sequence is ARBSLOT2, ARBSLOT1, ARBSLOT2, ARBSLOT1, etc...

Channel 1 and Channel 2 are selected in round robin order when arbitration slot 1 is executed.

If we replace the ARBSLOTS value for channel 0 with EIGHT, then the sequence would look like the following:

CHNL0, CHNL0, CHNL0, CHNL0, CHNL1, CHNL0, CHNL0, CHNL0, CHNL0, CHNL2, CHNL0, CHNL0, CHNL0, CHNL0, CHNL1, etc.

### 9.3.6.2 DMA Transfer Arbitration

In addition to the inter channel arbitration, software can configure when the controller arbitrates during a DMA transfer. This provides reduced latency to higher priority channels when configuring low priority transfers with more arbitration cycles.

The LDMA provides four bits that configure how many DMA transfers occur before it re-arbitrates. These bits are known as the BLOCKSIZE bits and they map to the arbitration rate as shown below. For example, if BLOCKSIZE = 4 then the arbitration rate is 6, that is, the controller arbitrates every 6 DMA transfers.

Table 9.2 AHB Bus Transfer Arbitration Interval on page 200 lists the arbitration rates.

**Table 9.2. AHB Bus Transfer Arbitration Interval**

| BLOCKSIZE | Arbitrate After x DMA transfers |
|-----------|---------------------------------|
| 0         | x = 1                           |
| 1         | x = 2                           |
| 2         | x = 3                           |
| 3         | x = 4                           |
| 4         | x = 6                           |
| 5         | x = 8                           |
| 6         | x = 12                          |
| 7         | x = 16                          |
| 8         | x = 24                          |
| 9         | x = 32                          |
| 10        | x = 64                          |
| 11        | x = 128                         |
| 12        | x = 256                         |
| 13        | x = 512                         |
| 14        | x = 1024                        |
| 15        | x = lock                        |

**Note:** Software must take care not to assign a low-priority channel with a large BLOCKSIZE because this prevents the controller from servicing high-priority requests, until it re-arbitrates.

The number of DMA transfers that need to be done is specified by the user in XFERCNT. When XFERCNT > BLOCKSIZE and is not an integer multiple of BLOCKSIZE then the controller always performs sequences of BLOCKSIZE transfers until XFERCNT < BLOCKSIZE remain to be transferred. The controller performs the remaining XFERCNT transfers at the end of the DMA cycle.

Software must store the value of the BLOCKSIZE bits in the channel control data structure. See 9.3.7.1 XFER Descriptor Structure for more information about the location of the BLOCKSIZE bits in the data structure.

### 9.3.7 Channel Descriptor Data Structure

Each channel descriptor consists of four 32-bit words:

- CTRL - control word contains information like transfer count and block size.
- SRC - source address points to where to copy data from
- DST - destination address points to where to copy data to
- LINK - link address points to where to load the next linked descriptor

These words map directly to the LDMA\_CHx\_CTRL, LDMA\_CHx\_SRC, LDMA\_CHx\_DST, and LDMA\_CHx\_LINK registers. The usage of the SRC and DST fields may differ depending on the structure type

There are three different types of descriptor data structures: **XFER**, **SYNC**, and **WRI**

### 9.3.7.1 XFER Descriptor Structure

This descriptor defines a typical data transfer which may be a Normal, Link, or Loop transfer.

Only this structure type can be written directly into LDMA's registers by the CPU. All descriptors may be linked to. Refer to the register descriptions for additional information.

For specifying XFER structure type, set STRUCTTYPE to 0. See the peripheral register descriptions for information on the fields in this structure.

| Name |            | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|------|------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|
|      |            | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |
| CTRL | DSTMODE    |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|      | SRCMODE    |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|      | DSTINC     |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|      | SIZE       |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|      | SRCINC     |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|      | IGNORESREQ |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|      | DECLOOPCNT |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|      | REQMODE    |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|      | DONEIFSEN  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|      | BLOCKSIZE  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|      | BYTESWAP   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|      | XFERCNT    |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|      | STRUCTREQ  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|      | STRUCTTYPE |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| SRC  |            | SRCADDR      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| DST  |            | DSTADDR      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
| LINK |            | LINKADDR     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|      | LINK       |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |
|      | LINKMODE   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |

### 9.3.7.2 SYNC Descriptor Structure

This descriptor defines an intra-channel synchronizing structure. It allows the channel to wait for some external stimulus before continuing on to the next descriptor. This structure is also used to provide stimulus to another channel to indicate that it may continue.

For example channel 1 may be configured to transfer a header into a buffer while channel 2 is simultaneously transferring data into the same structure. When channel 1 has completed it can wait for a sync signal from channel 2 before transferring the now complete buffer to a peripheral.

Sync descriptors do nothing until a condition is met. The condition is formed by the SYNCTRIG field in the LDMA\_SYNC register and the MATCHEN and MATCHVAL fields of the descriptor. When  $(\text{SYNCTRIG} \& \text{MATCHEN}) == (\text{MATCHVAL} \& \text{MATCHEN})$  the next descriptor is loaded. In addition to waiting for the condition a Link descriptor can set or clear bits in SYNCTRIG to meet the conditions of another channel and cause it to continue. The CPU also has the ability to set and clear the SYNCTRIG bits from software.

This structure type can only be linked in from memory.

For specifying SYNC structure type, set STRUCTTYPE to 1.

| Name    | Bit Position |    |    |    |    |    |    |    |    |    |    |           |         |    |    |    |    |    |    |          |         |    |   |   |   |   |   |   |            |          |   |   |
|---------|--------------|----|----|----|----|----|----|----|----|----|----|-----------|---------|----|----|----|----|----|----|----------|---------|----|---|---|---|---|---|---|------------|----------|---|---|
|         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20        | 19      | 18 | 17 | 16 | 15 | 14 | 13 | 12       | 11      | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3          | 2        | 1 | 0 |
| CTRL    |              |    |    |    |    |    |    |    |    |    |    | DONEIFSEN |         |    |    |    |    |    |    |          |         |    |   |   |   |   |   |   | STRUCTTYPE |          |   |   |
|         |              |    |    |    |    |    |    |    |    |    |    |           | SYNCCLR |    |    |    |    |    |    |          | SYNCSET |    |   |   |   |   |   |   |            |          |   |   |
| DST SRC |              |    |    |    |    |    |    |    |    |    |    | MATCHEN   |         |    |    |    |    |    |    | MATCHVAL |         |    |   |   |   |   |   |   |            |          |   |   |
| LINK    | LINKADDR     |    |    |    |    |    |    |    |    |    |    |           |         |    |    |    |    |    |    |          |         |    |   |   |   |   |   |   | LINK       | LINKMODE |   |   |
|         |              |    |    |    |    |    |    |    |    |    |    |           |         |    |    |    |    |    |    |          |         |    |   |   |   |   |   |   |            |          |   |   |

| Bit  | Name       | Description  |
|------|------------|--|
| 1:0  | STRUCTTYPE | <b>Descriptor Type</b><br>This field indicates which type of descriptor this is. It must be 1 for a SYNC descriptor.   |
| 20   | DONEIFSEN  | <b>Done if Set indicator</b><br>If set the interrupt flag will be set when descriptor completes.   |
| 15:8 | SYNCCLR    | <b>Sync Trigger Clear</b><br>This bit-field is used to clear corresponding bits within the SYNCTRIG field of the SYNC LDMA_SYNC register. To clear a given bit, a one should be loaded to the corresponding bit. Set is given priority over clear if both corresponding bits are loaded with a one. The sync trigger clear function can only be used when loaded from a linked structure. Alternately, the user can directly write the SYNCTRIG bit-field if required. |
| 7:0  | SYNCSET    | <b>Sync Trigger Set</b><br>This bit-field is used to set corresponding bits within the SYNCTRIG bit-field. To set a given bit, a one should be loaded to the corresponding bit. Set is given priority over clear if both corresponding bits are loaded with a one. The sync trigger set function can only be used when loaded from a linked structure. Alternately, the user can directly write the SYNCTRIG bit-field if required.                                    |
| 15:8 | MATCHEN    | <b>Sync Trigger Match Enable</b><br>This bit-field serves as the SYNCTRIG match enable. A sync match triggers the load of the next linked DMA structure as specified by link_mode, when: $(\text{SYNCTRIG} \& \text{MATCHEN}) == (\text{MATCHVAL} \& \text{MATCHEN})$ .  |
| 7:0  | MATCHVAL   | <b>Sync Trigger Match Value</b>  |

| Bit | Name | Description   |
|-----|------|---|
|     |      | This bit-field serves as the SYNCTRIG match value. A sync match triggers the load of the next linked DMA structure as specified by link_mode, when: (SYNCTRIG & MATCHEN) == (MATCHVAL & MATCHEN). |

### 9.3.7.3 WRI Descriptor Structure

This descriptor defines a write-immediate structure. This allows a list of descriptors to write a value to a register or memory location. For example, if a channel wishes to perform two loops in a descriptor sequence a WRI may be used to program the loop count for the second loop.

This structure type can only be linked in from memory.

For specifying WRI structure type, set STRUCTTYPE to 2.

| Name | Bit Position |    |    |    |    |    |    |    |    |    |    |           |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |            |      |   |          |   |
|------|--------------|----|----|----|----|----|----|----|----|----|----|-----------|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|------------|------|---|----------|---|
|      | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20        | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4          | 3    | 2 | 1        | 0 |
| CTRL |              |    |    |    |    |    |    |    |    |    |    | DONEIFSEN |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | STRUCTTYPE |      |   |          |   |
| SRC  | IMMVAL       |    |    |    |    |    |    |    |    |    |    |           |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |            |      |   |          |   |
| DST  | DSTADDR      |    |    |    |    |    |    |    |    |    |    |           |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |            |      |   |          |   |
| LINK | LINKADDR     |    |    |    |    |    |    |    |    |    |    |           |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |            | LINK |   | LINKMODE |   |

| Bit  | Name       | Description   |
|------|------------|---|
| 1:0  | STRUCTTYPE | <b>Descriptor Type</b><br>This field indicates which type of descriptor this is. It must be 2 for a WRI descriptor.   |
| 20   | DONEIFSEN  | <b>Done if Set indicator</b><br>If set the interrupt flag will be set when descriptor completes.  |
| 31:0 | IMMVAL     | <b>Immediate Value for Write</b><br>This bit-field specifies the immediate data value that is to be written to the address pointed to by DSTADDR. Only one write occurs for WRI structures. |
| 31:0 | DSTADDR    | <b>Address to write</b><br>This bit-field specifies the address the immediate data should be written to.  |

### 9.3.8 Interaction With the EMU

The LDMA interacts with the Energy Management Unit (EMU) to allow transfers from a low energy peripheral while in EM2 Deep Sleep. For example, when using the LEUART in EM2 Deep Sleep the EMU can wake up the LDMA sufficiently long to allow data transfers to occur. See section "DMA Support" in the LEUART documentation.

Similarly, when using the ADC in EM2 Deep Sleep or EM3 Stop the EMU can wake up the LDMA as needed to allow data transfers to occur.

[Table 9.3 List of Peripherals Capable of Waking Up LDMA in EM2 Deep Sleep or EM3 Stop on page 204](#) shows complete list of peripherals that are capable of waking up LDMA via EMU in EM2 Deep Sleep or EM3 Stop

**Table 9.3. List of Peripherals Capable of Waking Up LDMA in EM2 Deep Sleep or EM3 Stop**

| Peripheral |
|------------|
| ADC0       |
| CSEN       |
| IDAC0      |
| LESENSE    |
| LEUART0    |

### 9.3.9 Interrupts

The LDMA\_IF Interrupt flag register contains one DONE bit for each channel and one combined ERROR bit. When enabled, these interrupts are available as interrupts to the Cortex-M4 core. They are combined into one interrupt vector, DMA\_INT. If the interrupt for the DMA is enabled in the ARM Cortex-M4 core, an interrupt will be made if one or more of the interrupt flags in LDMA\_IF and their corresponding bits in LDMA\_IEN are set.

When a descriptor finishes execution the interrupt flag for that channel will be set if the DONEIFSEN field of the LDMA\_CHx\_LOOP register is set. If LINK and DONEIFSEN are both set when the descriptor completes the interrupt and the linked descriptor will be immediately loaded. When the final descriptor in a linked list (LINK = 0) is finished the interrupt flag is always set regardless of the state of DONEIFSEN.

### 9.3.10 Debugging

For a peripheral request DMA transfer, if software sets a bit for a channel in the LDMA\_DBGHALT register then the DMA will halt during a debug halt and the SRC and DST registers in the debug window will show the transfer in progress. Otherwise, during debug halt the DMA will continue to run and complete the entire transfer causing the descriptor registers to indicate the transfer has completed.

## 9.4 Examples

This section provides examples of common LDMA usage. All examples assume the LDMA is in the reset state with the channel being configured disabled and LDMA\_CHx\_CFG, LDMA\_CHx\_LOOP, and LDMA\_CHx\_LINK cleared.

### 9.4.1 Single Direct Register DMA Transfer

This simple example uses only the Channel Descriptor registers directly and does not use linking. Software writes directly to the LDMA channel registers. This example does not use a memory based descriptor list.

This example is suitable for most simple transfers that are limited to transferring one block of data. It supports anything that can be done using a single descriptor. This includes endian conversion and packing/unpacking data. Channel 0 is used for this example.

The LDMA will be used to copy 127 contiguous half words (254 bytes) from 0x0 to 0x1000. It will allow arbitration every 4 transfers and is triggered by a CPU write to the LDMA\_SWREQ register. The CH0 interrupt flag will be set when the transfer completes since the descriptor does not link to another descriptor.

- Configure LDMA\_CH0\_CTRL
  - DSTMODE = 0 (absolute)
  - SRCMODE = 0 (absolute)
  - SIZE = HALFWORD (16 bits)
  - DSTINC = 0 (1 half-word)
  - SRCINC = 0 (1 half-word)
  - DECLOOPCNT=0 (unused)
  - REQMODE = 1 (one request transfers all data)
  - BLOCKSIZE = 3 (4 transfers)
  - BYTESWAP=0 (no byte swap)
  - XFERCNT=127 (transfer 127 half words)
  - STRUCTTYPE=0 (TRANSFER)
- Write source address to LDMA\_CH0\_SRC register
- Write destination address to LDMA\_CH0\_DST register
- Configure the LDMA\_CH0REQSEL register for the desired peripheral or select none for a memory-to-memory transfer
- Clear and enable interrupts.
  - Write a 1 to bit 0 of the LDMA\_IFC register to clear the CH0 DONE flag
  - Write a 1 to bit 0 of the LDMA\_IEN register to enable the CH0 interrupt
- Write a 1 to bit 0 of the LDMA\_CHEN register to enable CH0

The REQMODE field is normally cleared to zero for a peripheral request transfer and will transfer the specified block size for each peripheral request. The REQMODE may be set to 1 for a memory-to-memory transfer or any time it is desired for a single DMA request to initiate complete transfer.

### 9.4.2 Descriptor Linked List

This example shows how to use a Linked List of descriptors. Each descriptor has a link address which points to the next descriptor in the list. A descriptor may be removed from the Linked list by altering the Link address of the one before it to point to the one after it. Descriptor Linked lists are useful when handling an array of buffers for communication data. For example, a bad packet can be removed from a receiver queue by simply removing the descriptor from the linked list.

Software loads the first descriptor into the DMA by writing the descriptor address to LDMA\_CHx\_LINK and setting the bit for that channel in the LDMA\_LINKLOAD register. This method is preferred when using a linked list in memory since it treats the first descriptor just like all the others. However, it is also allowed for software to write the first descriptor directly to the LDMA registers.

In this example 4 descriptors are executed in series. the interrupt flag is set after the 2nd and 4th (last) descriptors have completed.

- Prepare a list of descriptors using the XFER structure type in RAM
- Initialize the CTRL, SRC, and DST members as desired
  - Setting STRUCTREQ in the CTRL word for descriptors 2-4 will cause them to begin transferring data as soon as they are loaded.
- Write 0x00000013 to the LINK member of all but the last descriptor
  - LINKMODE = 1 (relative addressing)
  - LINK = 1 (Link to the next descriptor)
  - LINKADDR = 0x00000010 (size of descriptor)
- Set the DONEIFSEN bit in the CTRL member of the 2nd structure so that the interrupt flag will be set when it completes
- Write 0x00000000 to the LINK member of the last descriptor
  - LINK = 0 (Do not link to the next descriptor)
  - LINKMODE = 0 (don't care)
  - LINKADDR = 0x00000000 (don't care)

Each descriptor now points to the start of the next descriptor as shown on the left in [Figure 9.5 Descriptor Linked List on page 206](#). To remove a descriptor from the linked list modify the LINK address of the descriptor of the one before to point to the one after. For example to remove the third descriptor, add 0x00000010 to the LINK register of the second descriptor. The second descriptor will now point to the forth descriptor and skip over the third descriptor as shown on the right in [Figure 9.5 Descriptor Linked List on page 206](#).

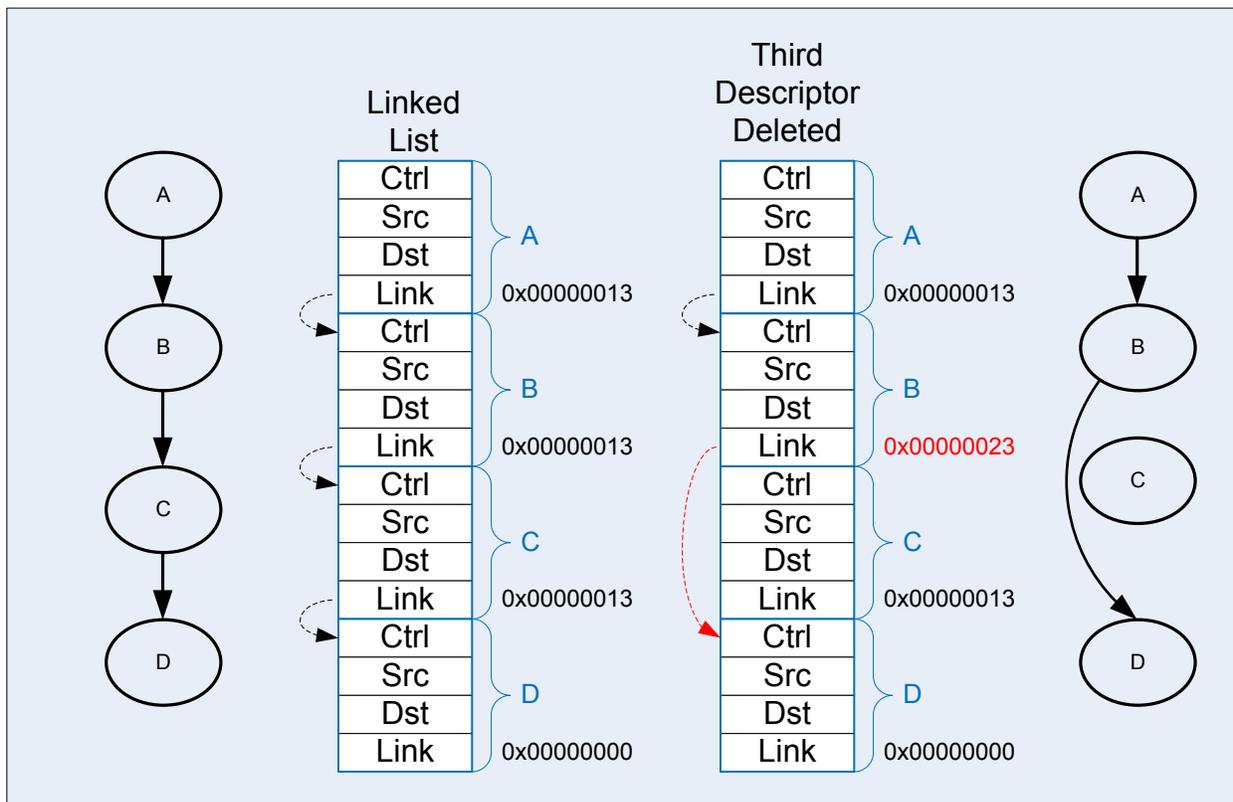


Figure 9.5. Descriptor Linked List

To start execution of the linked list of descriptors:

- Write the absolute address of the first descriptor to the LINKADR field of the LDMA\_CH0\_LINK register
- Set the LINK bit of LDMA\_CH0\_LINK register.
- Configure the LDMA\_CH0REQSEL register for the desired peripheral or select none for memory-to-memory
- Clear and enable interrupts as desired
- Set bit 0 in the LDMA\_LINKLOAD register to initiate loading and execution of the first descriptor

Alternatively, software can manually copy the first descriptor contents to the LDMA\_CH0\_CTRL, LDMA\_CH0\_SRC, LDMA\_CH0\_DST, and LDMA\_CH0\_LINK registers and then enable the channel in the LDMA\_CHEN register.

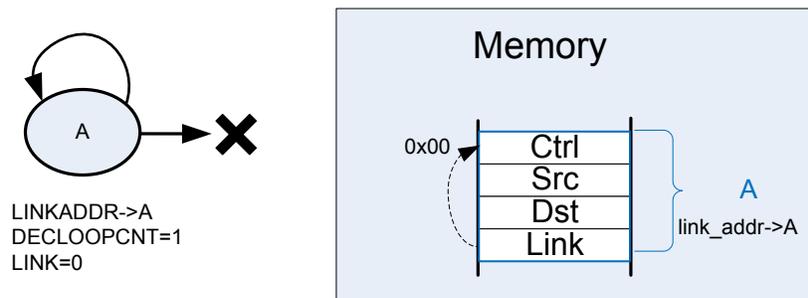
### 9.4.3 Single Descriptor Looped Transfer

This example demonstrates how to use looping using a single descriptor. This method allows a single DMA transfer to be repeated a specified number of times. The looping descriptor is stored in memory and reloaded by hardware. After a specified number of iterations, the transfer stops.

CH0 is setup to copy 4 words from the ADC FIFO into a 15 word buffer at 0x1000. It repeats 4 times to fill the entire 16 word buffer. An interrupt will fire when the entire 16 words have been transferred.

Initialize the Linked descriptor in memory as follows:

- Configure CTRL member
  - DSTMODE = 0 (absolute)
  - SRCMODE = 0 (absolute)
  - SIZE = WORD
  - DSTINC = 0 (1 WORD)
  - SRCINC = 3 (0 WORDS)
  - DECLOOPCNT=1 (decrement loop count)
  - REQMODE=1 (Use XFERCNT)
  - BLOCKSIZE = 4 (4 words)
  - BYTESWAP=0 (no swap)
  - XFERCNT= 4 (4 words)
  - STRUCTTYPE=0 (TRANSFER)
  - IGNORESREQ=1 (ignore single requests)
- Write the address ADC0\_SINGLEDATA register to the SRC member
- Write 0x1000 address to DST member
- Configure the LINK member
  - LINK = 0 (stop after loop)
  - MODE = 1 (relative link address)
  - LINKADDR = 0 (point to ourself)
- Configure the Channel
  - Write the desired number of repeats to the LDMA\_CH0\_LOOP register
  - SOURCESEL in LDMA\_CH0REQSEL = ADC0 (select the ADC)
  - SIG in LDMA\_CH0REQSEL = ADC0SCAN (select the scan conversion request)
- Clear and enable interrupts
- Load the descriptor using LINKLOAD as described in [9.4.2 Descriptor Linked List](#)



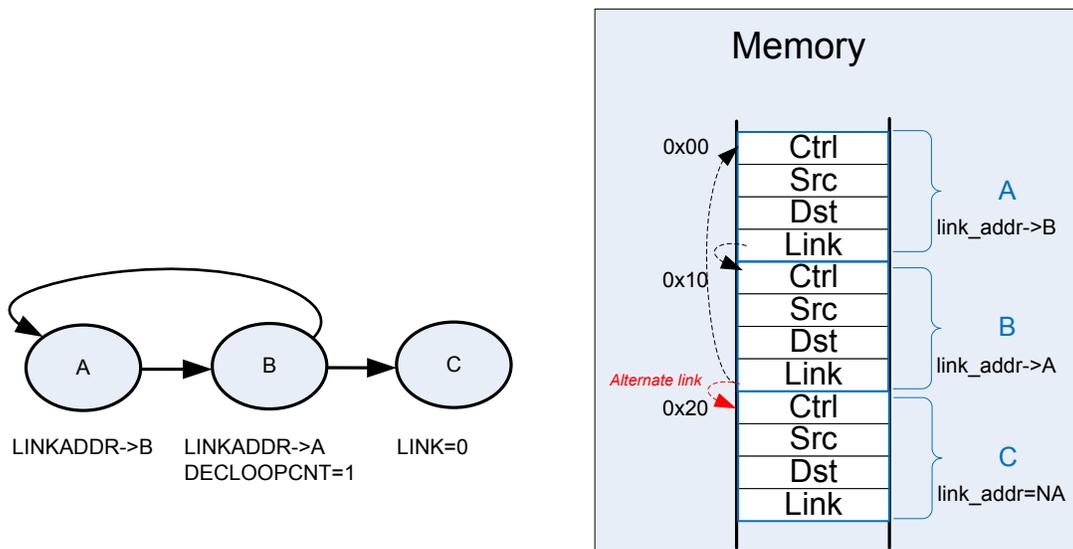
**Figure 9.6. Single Descriptor Looped Transfer**

Note that the looping descriptor must be stored in memory, because it must load itself from the link address in memory on each iteration.

### 9.4.4 Descriptor List With Looping

This example uses a descriptor list in memory with looping over multiple descriptors. This example also uses the looping feature and continues on with the next sequential descriptor after looping completes.

The descriptor list in memory is shown in figure [Figure 9.7 Descriptor List With Looping on page 209](#). Descriptor A links to descriptor B. Descriptor B has the DECLOOPCNT bit enabled and loops back to the start of descriptor A. The LINK address of descriptor B is used for the loop address. The LINK bit is set to indicate that execution will continue after completion of looping. Once the LOOPCNT reaches zero, the LDMA will load descriptor C. Descriptor C must be located immediately following descriptor B.



**Figure 9.7. Descriptor List With Looping**

Initialization is similar to the single looping descriptor with the following modifications.

- Set the LINK bit in descriptors A and B
- write the address of descriptor A into the LIKADDRESS of descriptor B
- write the address of descriptor B into the LIKADDRESS of descriptor A
- Descriptor C must be located immediately after descriptor B in memory

### 9.4.5 Simple Inter-Channel Synchronization

The LDMA controller features synchronization structures which allow differing channels and/or hardware events to pause a DMA sequence, and wait for a synchronizing event to restart it.

In this example DMA channel 0 and 1 are tasked with the transfer of different sets of data. Channel 0 has two transfer structures, and channel 1 just one, but channel 0 must wait until channel 1 has completed its transfer before it starts its second transfer structure.

Pausing channel 0 is accomplished by inserting a sync wait structure between the two transfer structures. This sync structure waits on SYNCTRIG[7] to be set by a sync set/clear structure which is controlled by channel 1. Sync structures do not transfer data, they can only set, clear, or wait to match the SYNCTRIG[7:0] bits. Note that sync structures cannot decrement loop counter.

```
LDMA_SYNC
  SYNCTRIG=0x0 (at time 0)

LDMA_CH0

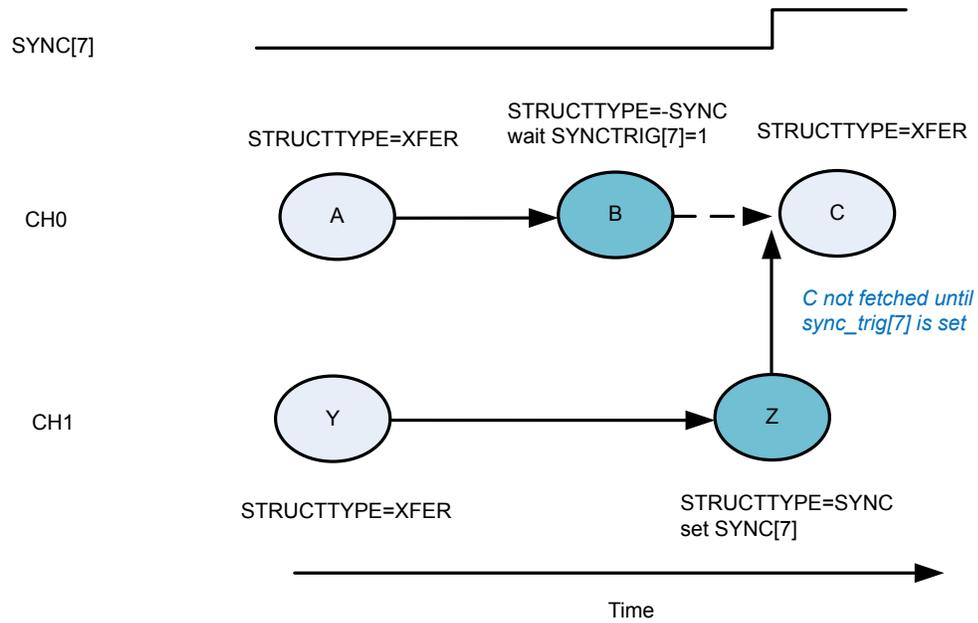
  Structure A @ 0x00          Structure B @ 0x10          Structure C @ 0x20
  CTRL                      CTRL                      CTRL
  STRUCTTYPE=XFER          STRUCTTYPE=SYNC          STRUCTTYPE=XFER
  LINK                      LINK                      LINK
  LINKADDR[29:0]=0x00000004 LINKADDR[29:0]=0x00000008 LINKADDR[29:0]=NA
  LINK=1                   LINK=1                   LINK=0

                                DST
                                MATCHEN=0x80
                                MATCHVAL=0x80 (waits for SYNCTRIG[7]=1)

LDMA_CH1

  Structure Y @ 0x30          Structure Z @ 0x40
  CTRL                      CTRL
  STRUCTTYPE=XFER          STRUCTTYPE=SYNC
  LINK                      LINK
  LINKADDR[29:0]=0x00000010 LINKADDR=NA
  LINK=1                   LINK=0

                                SRC
                                SRCCLR=0x0
                                SRCSET=0x80 (sets SYNCTRIG[7])
```



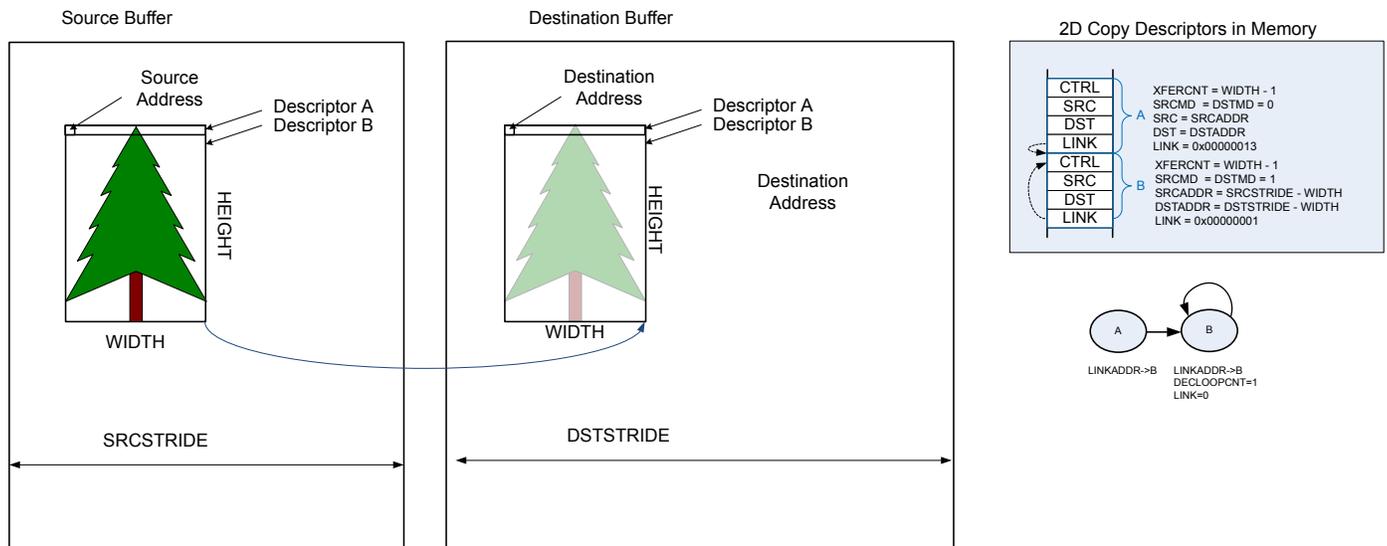
**Figure 9.8. Simple Intra-channel Synchronization Example**

Both A and Y effectively start at the same time. A finishes earlier, then it links to B, which waits for the SYNC[7] bit to be set before loading C. Y finishes after B is loaded, and it links to sync structure Z, which sets the SYNC[7] bit. Channel 0 responds to the trigger set by loading C for the final data transfer.

### 9.4.6 2D Copy

The LDMA can easily perform a 2D copy using a descriptor list with looping. This set up is visualized in [Figure 9.9 2D Copy on page 212](#).

For an application working with graphics, this would mean the ability to copy a rectangle of a given width and height from one picture to another.



**Figure 9.9. 2D Copy**

The first descriptor will use absolute addressing mode and the source and destination addresses should point to the desired target addresses. The first descriptor will copy only the first row. The XFERCNT of the first descriptor is set to the desired width minus one.

- CTRL
  - XFERCNT = WIDTH - 1
  - SRCMD = 0 (absolute)
  - DSTMD = 0 (absolute)
- SRCADDR = target source address
- DSTADDR = target destination address
- LINK = 0x00000013
  - LINK=1
  - LINKMD=1
  - LINKADDR=0x00000010 (point to next descriptor)

The second descriptor will use relative addressing and the source and destination addresses are set to the desired offset. After the completion of the first descriptor, the address registers will point to the last address transferred. Thus, the width must be subtracted from the stride to get the offset. The second descriptor uses looping and the link register has not offset.

- CTRL
  - XFERCNT = WIDTH - 1
  - SRCMD = 1 (relative)
  - DSTMD = 1 (relative)
  - DECLOOPCNT = 1
- SRCADDR = desired source offset (SRCSTRIDE-WIDTH)
- DSTADDR = desired destination offset (DSTSTRIDE-WIDTH)
- LINK = 0x00000001
  - LINK=0
  - LINKMD=1 (relative)
  - LINKADDR=0x00000000 (no offset)

---

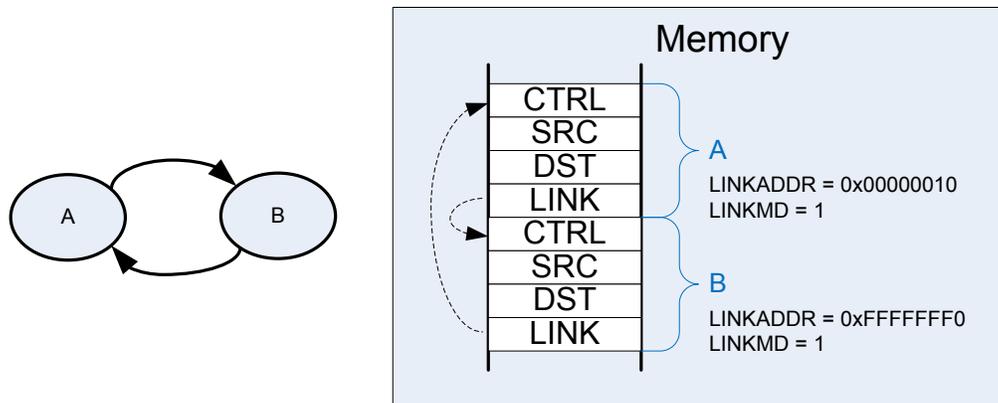
Because the first descriptor already transferred one row, the number of looping repeats should be the desired height minus two. Therefore, LOOPCNT should be set to HEIGHT minus two before initiating the transfer.

This same method is easily extended to copy multiple rectangles by linking descriptors together. To initialize the LDMA\_CHx\_LOOP register, precede each descriptor pair described above with a write immediate descriptor which writes the desired value to the LOOPCNT field of the LDMA\_CHx\_LOOP register.

### 9.4.7 Ping-Pong

Communication peripherals often use ping-pong buffers. Ping-pong buffers allow the CPU to process data in one buffer while a peripheral transmits or receives data in the other buffer.

Both transmit and receive ping-pong buffers are easily implemented using the LDMA. In either case, this requires two descriptors as shown in [Figure 9.10 Infinite Ping-Pong Example on page 214](#). The LINKADDR field of the LINK member should point to the other descriptor. Using two adjacent descriptors and relative link addressing ensures the descriptors are easily reloadable.



**Figure 9.10. Infinite Ping-Pong Example**

A **receiver** ping-pong buffer controller consists of two buffers and two descriptors stored in memory that point to the two buffers. Once initialized, as the peripheral receives data, it will fill the first buffer. Once the first buffer is full, it will link automatically to the second buffer and generate an interrupt. Software will then process the data in the first buffer while the LDMA is transferring data to the second buffer. For a receiver ping-pong buffer each descriptor should link to the other descriptor. The link bit should be set to provide infinite ping pong between the two buffers. The DONIFS bit in each descriptor should be set to generate an interrupt on the completion of each descriptor.

- Descriptor A
  - CTRL
    - DONEIFS = 1
    - other settings as desired
  - SRCADDR = peripheral source address
  - DSTADDR = memory destination address
  - LINK = 0x00000013
    - LINKADDR = 0x00000010 (next descriptor)
    - LINK = 1 (link to next descriptor)
    - LINKMD = 1 (relative addressing)
- Descriptor B
  - CTRL
    - DONEIFS = 1
    - other settings as desired
  - SRCADDR = peripheral source address
  - DSTADDR = memory destination address
  - LINK = 0xFFFFFFFF3
    - LINKADDR = 0xFFFFFFFF0 (previous descriptor)
    - LINK = 1 (link to previous descriptor)
    - LINKMD = 1 (relative addressing)

For **transmitter** ping-pong buffer, software will fill the first buffer and then initiate the DMA transfer. The LDMA will transmit the first buffer data while software is filling the second buffer. In this case, the two descriptors should point to each other, but not automatically

continue to the second buffer. The LINK bit should be cleared to zero. Once software has loaded the first buffer, it will use the LINK-LOAD bit to load the first descriptor and transmit the data. The DONEIFS need not be set in each descriptor. The DMA will stop and then generate an interrupt at the completion of each descriptor.

- Descriptor A
  - CTRL
    - DONEIFS = 0
    - other settings as desired
  - SRCADDR = memory source address
  - DSTADDR = peripheral destination address
  - LINK = 0x00000013
    - LINKADDR = 0x00000010 (next descriptor)
    - LINK = 0 (link to next descriptor)
    - LINKMD = 1 (relative addressing)
- Descriptor B
  - CTRL
    - DONEIFS = 0
    - other settings as desired
  - SRCADDR = memory source address
  - DSTADDR = peripheral destination address
  - LINK = 0xFFFFFFFF3
    - LINKADDR = 0xFFFFFFFF0 (previous descriptor)
    - LINK = 0 (link to previous descriptor)
    - LINKMD = 1 (relative addressing)

#### 9.4.8 Scatter-Gather

Scatter-Gather in general refers to a process that copies data from multiple locations scattered in memory and gathers the data to a single location in memory, or vice versa. A simple descriptor list allows data gathering. For example, data from a discontinuous list of buffers might be copied to a contiguous sequential array of buffers. The inverse is also possible when a sequential array of buffers is scattered to a discontinuous list of available buffers. See section [9.4.2 Descriptor Linked List](#).

Some DMAs which only have two descriptors implement scatter-gather by using one descriptor to modify the other descriptor. While it is possible to implement this same behavior using the LDMA, it is much more straight-forward to just use a simple descriptor list.

## 9.5 Register Map

The offset register address is relative to the registers base address.

| Offset | Name            | Type  | Description   |
|--------|-----------------|-------|---|
| 0x000  | LDMA_CTRL       | RW    | DMA Control Register                                    |
| 0x004  | LDMA_STATUS     | R     | DMA Status Register                                     |
| 0x008  | LDMA_SYNC       | RWH   | DMA Synchronization Trigger Register (Single-Cycle RMW) |
| 0x020  | LDMA_CHEN       | RWH   | DMA Channel Enable Register (Single-Cycle RMW)          |
| 0x024  | LDMA_CHBUSY     | R     | DMA Channel Busy Register                               |
| 0x028  | LDMA_CHDONE     | RWH   | DMA Channel Linking Done Register (Single-Cycle RMW)    |
| 0x02C  | LDMA_DBGHALT    | RW    | DMA Channel Debug Halt Register                         |
| 0x030  | LDMA_SWREQ      | W1    | DMA Channel Software Transfer Request Register          |
| 0x034  | LDMA_REQDIS     | RW    | DMA Channel Request Disable Register                    |
| 0x038  | LDMA_REQPEND    | R     | DMA Channel Requests Pending Register                   |
| 0x03C  | LDMA_LINKLOAD   | W1    | DMA Channel Link Load Register                          |
| 0x040  | LDMA_REQCLEAR   | W1    | DMA Channel Request Clear Register                      |
| 0x060  | LDMA_IF         | R     | Interrupt Flag Register                                 |
| 0x064  | LDMA_IFS        | W1    | Interrupt Flag Set Register                             |
| 0x068  | LDMA_IFC        | (R)W1 | Interrupt Flag Clear Register                           |
| 0x06C  | LDMA_IEN        | RW    | Interrupt Enable Register                               |
| 0x080  | LDMA_CH0_REQSEL | RW    | Channel Peripheral Request Select Register              |
| 0x084  | LDMA_CH0_CFG    | RW    | Channel Configuration Register                          |
| 0x088  | LDMA_CH0_LOOP   | RWH   | Channel Loop Counter Register                           |
| 0x08C  | LDMA_CH0_CTRL   | RWH   | Channel Descriptor Control Word Register                |
| 0x090  | LDMA_CH0_SRC    | RWH   | Channel Descriptor Source Data Address Register         |
| 0x094  | LDMA_CH0_DST    | RWH   | Channel Descriptor Destination Data Address Register    |
| 0x098  | LDMA_CH0_LINK   | RWH   | Channel Descriptor Link Structure Address Register      |
| ...    | LDMA_CHx_REQSEL | RW    | Channel Peripheral Request Select Register              |
| ...    | LDMA_CHx_CFG    | RW    | Channel Configuration Register                          |
| ...    | LDMA_CHx_LOOP   | RWH   | Channel Loop Counter Register                           |
| ...    | LDMA_CHx_CTRL   | RWH   | Channel Descriptor Control Word Register                |
| ...    | LDMA_CHx_SRC    | RWH   | Channel Descriptor Source Data Address Register         |
| ...    | LDMA_CHx_DST    | RWH   | Channel Descriptor Destination Data Address Register    |
| ...    | LDMA_CHx_LINK   | RWH   | Channel Descriptor Link Structure Address Register      |
| 0x1D0  | LDMA_CH7_REQSEL | RW    | Channel Peripheral Request Select Register              |
| 0x1D4  | LDMA_CH7_CFG    | RW    | Channel Configuration Register                          |
| 0x1D8  | LDMA_CH7_LOOP   | RWH   | Channel Loop Counter Register                           |
| 0x1DC  | LDMA_CH7_CTRL   | RWH   | Channel Descriptor Control Word Register                |
| 0x1E0  | LDMA_CH7_SRC    | RWH   | Channel Descriptor Source Data Address Register         |

| Offset | Name          | Type | Description  |
|--------|---------------|------|--|
| 0x1E4  | LDMA_CH7_DST  | RWH  | Channel Descriptor Destination Data Address Register |
| 0x1E8  | LDMA_CH7_LINK | RWH  | Channel Descriptor Link Structure Address Register   |

## 9.6 Register Description

### 9.6.1 LDMA\_CTRL - DMA Control Register

| Offset        | Bit Position |    |    |    |    |          |    |    |    |    |    |    |    |    |    |    |    |              |    |    |    |    |              |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----------|----|----|----|----|----|----|----|----|----|----|----|--------------|----|----|----|----|--------------|---|---|---|---|---|---|---|---|---|
| 0x000         | 31           | 30 | 29 | 28 | 27 | 26       | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14           | 13 | 12 | 11 | 10 | 9            | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    | 0x7      |    |    |    |    |    |    |    |    |    |    |    | 0x00         |    |    |    |    | 0x00         |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    | RW       |    |    |    |    |    |    |    |    |    |    |    | RW           |    |    |    |    | RW           |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    | NUMFIXED |    |    |    |    |    |    |    |    |    |    |    | SYNCPRSCLEEN |    |    |    |    | SYNCPRSSETEN |   |   |   |   |   |   |   |   |   |

| Bit   | Name         | Reset   | Access | Description   |
|-------|--------------|---|--------|---|
| 31:27 | Reserved     | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 26:24 | NUMFIXED     | 0x7   | RW     | <b>Number of Fixed Priority Channels</b><br><br>This field defines the number of Fixed Priority Arbitration channels. Channels CH0 through CH(n-1) are fixed, and channels CH(n) through CH7 are round robin, where n is the field value. The reset value will give all fixed channels. |
| 23:16 | Reserved     | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 15:8  | SYNCPRSCLEEN | 0x00  | RW     | <b>Synchronization PRS Clear Enable</b><br><br>Setting a bit in this field will enable the corresponding PRS input to clear the respective bit in the SYNCTRIG field of the LDMA_SYNC register. Refer to the PRS section for a list of the PRS inputs.                                  |
| 7:0   | SYNCPRSSETEN | 0x00  | RW     | <b>Synchronization PRS Set Enable</b><br><br>Setting a bit in this field will enable the corresponding PRS input to set the respective bit in the SYNCTRIG field of the LDMA_SYNC register. Refer to the PRS section for a list of the PRS inputs.                                      |

## 9.6.2 LDMA\_STATUS - DMA Status Register

| Offset        | Bit Position |    |    |    |       |    |    |    |    |    |    |    |           |    |    |    |    |    |    |    |         |    |   |   |         |   |   |   |        |   |         |   |
|---------------|--------------|----|----|----|-------|----|----|----|----|----|----|----|-----------|----|----|----|----|----|----|----|---------|----|---|---|---------|---|---|---|--------|---|---------|---|
| 0x004         | 31           | 30 | 29 | 28 | 27    | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19        | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11      | 10 | 9 | 8 | 7       | 6 | 5 | 4 | 3      | 2 | 1       | 0 |
| <b>Reset</b>  |              |    |    |    | 0x08  |    |    |    |    |    |    |    | 0x10      |    |    |    |    |    |    |    | 0x0     |    |   |   | 0x0     |   |   |   | 0      |   | 0       |   |
| <b>Access</b> |              |    |    |    | R     |    |    |    |    |    |    |    | R         |    |    |    |    |    |    |    | R       |    |   |   | R       |   |   |   | R      |   | R       |   |
| <b>Name</b>   |              |    |    |    | CHNUM |    |    |    |    |    |    |    | FIFOLEVEL |    |    |    |    |    |    |    | CHERROR |    |   |   | CHGRANT |   |   |   | ANYREQ |   | ANYBUSY |   |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 31:29 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 28:24 | CHNUM           | 0x08  | R      | <b>Number of Channels</b><br>The value of CHNUM always reads the total number of channels present for this instance of the DMA controller module.  |
| 23:21 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 20:16 | FIFOLEVEL       | 0x10  | R      | <b>FIFO Level</b><br>The value of FIFOLEVEL indicates the number of entries currently in the FIFO. (Note when all channels are disabled, this register will read the total number of entries in the FIFO.) |
| 15:11 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 10:8  | CHERROR         | 0x0   | R      | <b>Errant Channel Number</b><br>When the ERROR flag is set in the LDMA_IF register, the CHERROR field will indicate the most recent channel to have a transfer error.                                      |
| 7:6   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 5:3   | CHGRANT         | 0x0   | R      | <b>Granted Channel Number</b><br>The value of this field indicates the currently active channel or last active channel. Note that the reset value for this field is zero.                                  |
| 2     | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 1     | ANYREQ          | 0   | R      | <b>Any DMA Channel Request Pending</b><br>The value of this bit will be TRUE (1) if any requests are pending   |
| 0     | ANYBUSY         | 0   | R      | <b>Any DMA Channel Busy</b><br>The value of this bit will be TRUE (1) if one or more DMA channels are actively transferring data   |

### 9.6.3 LDMA\_SYNC - DMA Synchronization Trigger Register (Single-Cycle RMW)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |          |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|----------|---|---|---|---|---|---|---|
| 0x008         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x00     |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RWH      |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | SYNCTRIG |   |   |   |   |   |   |   |

| Bit  | Name     | Reset   | Access | Description |
|------|----------|---|--------|-------------|
| 31:8 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |             |

|   |          |      |     |                                |
|---|----------|------|-----|--------------------------------|
| 7:0   | SYNCTRIG | 0x00 | RWH | <b>Synchronization Trigger</b> |
| <p>The SYNC trigger field allows a transfer to pause until a specified trigger bit is set or cleared. The SYNC trigger bits may be set and cleared by a SYNC descriptor, PRS signal, or software. Note: software requires to use single-cycle read-modify-write, detailed in <a href="#">4.2.3 Peripheral Bit Set and Clear</a></p> |          |      |     |                                |

### 9.6.4 LDMA\_CHEN - DMA Channel Enable Register (Single-Cycle RMW)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |      |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|------|---|---|---|---|---|---|---|
| 0x020         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x00 |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RWH  |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | CHEN |   |   |   |   |   |   |   |

| Bit  | Name     | Reset   | Access | Description |
|------|----------|---|--------|-------------|
| 31:8 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |             |

|   |      |      |     |                        |
|---|------|------|-----|------------------------|
| 7:0   | CHEN | 0x00 | RWH | <b>Channel Enables</b> |
| <p>Setting one of these bits will enable the respective DMA channel. If cleared while a transfer is in progress, the current transfer block will complete. The remaining blocks will pause until resumed later by setting this bit again. Note: software requires to use single-cycle read-modify-write, detailed in <a href="#">4.2.3 Peripheral Bit Set and Clear</a></p> |      |      |     |                        |

## 9.6.5 LDMA\_CHBUSY - DMA Channel Busy Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |      |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|------|---|---|---|---|---|---|---|
| 0x024         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x00 |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | R    |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | BUSY |   |   |   |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description   |
|------|----------|--|--------|---|
| 31:8 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 7:0  | BUSY     | 0x00   | R      | <b>Channels Busy</b><br>The bits of this field read 1 when the corresponding channel is busy. |

## 9.6.6 LDMA\_CHDONE - DMA Channel Linking Done Register (Single-Cycle RMW)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |        |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|--------|---|---|---|---|---|---|---|
| 0x028         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x00   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RWH    |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | CHDONE |   |   |   |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description  |
|------|----------|--|--------|--|
| 31:8 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 7:0  | CHDONE   | 0x00   | RWH    | <b>DMA Channel Linking or Done</b><br>Each DMA channel sets the corresponding bit in this register when the entire transfer is done. The interrupt service routine should clear these bits. Enabling a DMA channel will also clear the corresponding LINKDONE bit. Note: software requires to use single-cycle read-modify-write, detailed in <a href="#">4.2.3 Peripheral Bit Set and Clear</a> |

## 9.6.7 LDMA\_DBGHALT - DMA Channel Debug Halt Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |         |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---------|---|---|---|---|---|---|---|
| 0x02C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x00    |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RW      |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | DBGHALT |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description           |
|---|----------|--|--------|-----------------------|
| 31:8  | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |                       |
| 7:0   | DBGHALT  | 0x00   | RW     | <b>DMA Debug Halt</b> |
| Setting one of these bits will mask the corresponding DMA channel's peripheral request when debugging and the CPU is halted. This may be useful for debugging DMA software. |          |  |        |                       |

## 9.6.8 LDMA\_SWREQ - DMA Channel Software Transfer Request Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |       |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|-------|---|---|---|---|---|---|---|
| 0x030         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7     | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x00  |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | W1    |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | SWREQ |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description                       |
|---|----------|--|--------|-----------------------------------|
| 31:8  | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |                                   |
| 7:0   | SWREQ    | 0x00   | W1     | <b>Software Transfer Requests</b> |
| Setting one of these bits will trigger a DMA transfer for the corresponding channel. Writing zeros has no effect. |          |  |        |                                   |

## 9.6.9 LDMA\_REQDIS - DMA Channel Request Disable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |        |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|--------|---|---|---|---|---|---|---|
| 0x034         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x00   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RW     |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | REQDIS |   |   |   |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description                 |
|--|----------|--|--------|-----------------------------|
| 31:8   | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |                             |
| 7:0  | REQDIS   | 0x00   | RW     | <b>DMA Request Disables</b> |
| Setting one of these bits will disable peripheral requests for the corresponding channel. When cleared any pending peripheral requests will be serviced. |          |  |        |                             |

## 9.6.10 LDMA\_REQPEND - DMA Channel Requests Pending Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |         |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---------|---|---|---|---|---|---|---|
| 0x038         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x00    |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | R       |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | REQPEND |   |   |   |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description                 |
|--|----------|--|--------|-----------------------------|
| 31:8   | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |                             |
| 7:0  | REQPEND  | 0x00   | R      | <b>DMA Requests Pending</b> |
| When a DMA channel has a pending peripheral request the corresponding REQPEND bit will read 1. |          |  |        |                             |

### 9.6.11 LDMA\_LINKLOAD - DMA Channel Link Load Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |          |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|----------|---|---|---|
| 0x03C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3        | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0x00     |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | W1       |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | LINKLOAD |   |   |   |

| Bit   | Name     | Reset   | Access | Description           |
|---|----------|---|--------|-----------------------|
| 31:8  | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |                       |
| 7:0   | LINKLOAD | 0x00  | W1     | <b>DMA Link Loads</b> |
| Setting one of these bits will force the corresponding DMA channel to load the next DMA structure and enable the channel. This empowers software to step through a sequence of descriptors. |          |   |        |                       |

### 9.6.12 LDMA\_REQCLEAR - DMA Channel Request Clear Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |          |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|----------|---|---|---|
| 0x040         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3        | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0x00     |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | W1       |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | REQCLEAR |   |   |   |

| Bit   | Name     | Reset   | Access | Description              |
|---|----------|---|--------|--------------------------|
| 31:8  | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |                          |
| 7:0   | REQCLEAR | 0x00  | W1     | <b>DMA Request Clear</b> |
| Setting one of these bits will clear any internally registered transfer requests for the corresponding channel. |          |   |        |                          |

## 9.6.13 LDMA\_IF - Interrupt Flag Register

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |      |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|------|
| 0x060  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |      |
| Reset  | 0            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0x00 |
| Access | R            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | R    |
| Name   | ERROR        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | DONE |

| Bit  | Name     | Reset   | Access | Description   |
|------|----------|---|--------|---|
| 31   | ERROR    | 0   | R      | <b>Transfer Error Interrupt Flag</b><br>The ERRORIF flag is set when a read or write error occurs. The CHERROR field in the LDMA_STATUS register reflects the number of the channel which had the last error. |
| 30:8 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 7:0  | DONE     | 0x00  | R      | <b>DMA Structure Operation Done Interrupt Flag</b><br>When a channel completes a transfer or sync operation, the corresponding DONE bit is set in the LDMA_IF register.                                       |

## 9.6.14 LDMA\_IFS - Interrupt Flag Set Register

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |      |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|------|
| 0x064  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |      |
| Reset  | 0            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0x00 |
| Access | W1           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | W1   |
| Name   | ERROR        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | DONE |

| Bit  | Name     | Reset   | Access | Description  |
|------|----------|---|--------|--|
| 31   | ERROR    | 0   | W1     | <b>Set ERROR Interrupt Flag</b><br>Write 1 to set the ERROR interrupt flag |
| 30:8 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 7:0  | DONE     | 0x00  | W1     | <b>Set DONE Interrupt Flag</b><br>Write 1 to set the DONE interrupt flag   |

## 9.6.15 LDMA\_IFC - Interrupt Flag Clear Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| 0x068         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| <b>Reset</b>  | 0            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0x00  |
| <b>Access</b> | (R)W1        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | (R)W1 |
| <b>Name</b>   | ERROR        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | DONE  |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 31   | ERROR           | 0   | (R)W1  | <b>Clear ERROR Interrupt Flag</b><br><br>Write 1 to clear the ERROR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 30:8 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 7:0  | DONE            | 0x00  | (R)W1  | <b>Clear DONE Interrupt Flag</b><br><br>Write 1 to clear the DONE interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |

## 9.6.16 LDMA\_IEN - Interrupt Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |      |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|------|
| 0x06C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |      |
| <b>Reset</b>  | 0            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0x00 |
| <b>Access</b> | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | RW   |
| <b>Name</b>   | ERROR        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | DONE |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 31   | ERROR           | 0   | RW     | <b>ERROR Interrupt Enable</b><br><br>Enable/disable the ERROR interrupt |
| 30:8 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 7:0  | DONE            | 0x00  | RW     | <b>DONE Interrupt Enable</b><br><br>Enable/disable the DONE interrupt   |

### 9.6.17 LDMA\_CHx\_REQSEL - Channel Peripheral Request Select Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |           |    |    |    |    |    |    |    |    |    |    |   |   |   |   |        |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|-----------|----|----|----|----|----|----|----|----|----|----|---|---|---|---|--------|---|---|---|---|---|
| 0x080         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20        | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5      | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    | 0x00      |    |    |    |    |    |    |    |    |    |    |   |   |   |   | 0x0    |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |   |   |   |   | RW     |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    | SOURCESEL |    |    |    |    |    |    |    |    |    |    |   |   |   |   | SIGSEL |   |   |   |   |   |

| Bit   | Name            | Reset   | Access  | Description   |
|-------|-----------------|---|---|---|
| 31:22 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |
| 21:16 | SOURCESEL       | 0x00  | RW  | <b>Source Select</b><br>Select input source to DMA channel. |
|       | Value           | Mode  | Description   |   |
|       | 0b000000        | NONE  | No source selected  |   |
|       | 0b000001        | PRS   | Peripheral Reflex System                                  |   |
|       | 0b001000        | ADC0  | Analog to Digital Converter 0                             |   |
|       | 0b001010        | VDAC0   | Digital to Analog Converter 0                             |   |
|       | 0b001100        | USART0  | Universal Synchronous/Asynchronous Receiver/Transmitter 0 |   |
|       | 0b001101        | USART1  | Universal Synchronous/Asynchronous Receiver/Transmitter 1 |   |
|       | 0b001110        | USART2  | Universal Synchronous/Asynchronous Receiver/Transmitter 2 |   |
|       | 0b010000        | LEUART0   | Low Energy UART 0   |   |
|       | 0b010100        | I2C0  | I2C 0   |   |
|       | 0b010101        | I2C1  | I2C 1   |   |
|       | 0b011000        | TIMER0  | Timer 0   |   |
|       | 0b011001        | TIMER1  | Timer 1   |   |
|       | 0b011010        | WTIMER0   | Wide Timer 0  |   |
|       | 0b110000        | MSC   | Memory System Controller                                  |   |
|       | 0b110001        | CRYPTO0   | Advanced Encryption Standard Accelerator 0                |   |
|       | 0b110010        | CSEN  | Capacitive touch sense module                             |   |
|       | 0b110011        | LESENSE   | Low Energy Sensor Interface                               |   |
|       | 0b110100        | CRYPTO1   | Advanced Encryption Standard Accelerator 1                |   |
| 15:4  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |
| 3:0   | SIGSEL          | 0x0   | RW  | <b>Signal Select</b><br>Select input signal to DMA channel. |

| Bit | Name               | Reset                   | Access | Description                           |
|-----|--------------------|-------------------------|--------|---------------------------------------|
|     | Value              | Mode                    |        | Description                           |
|     | <i>SOURCESEL</i> = | <i>0b000000</i>         |        | (NONE)                                |
|     | 0bxxxx             | OFF                     |        | Channel input selection is turned off |
|     | <i>SOURCESEL</i> = | <i>0b000001</i>         |        | (PRS)                                 |
|     | 0b0000             | PRSREQ0                 |        | PRSREQ0                               |
|     | 0b0001             | PRSREQ1                 |        | PRSREQ1                               |
|     | <i>SOURCESEL</i> = | <i>0b001000</i>         |        | (ADC0)                                |
|     | 0b0000             | ADC0SINGLE              |        | ADC0SINGLE REQ/SREQ                   |
|     | 0b0001             | ADC0SCAN                |        | ADC0SCAN REQ/SREQ                     |
|     | <i>SOURCESEL</i> = | <i>0b001010</i>         |        | (VDAC0)                               |
|     | 0b0000             | VDAC0CH0                |        | VDAC0CH0                              |
|     | 0b0001             | VDAC0CH1                |        | VDAC0CH1                              |
|     | <i>SOURCESEL</i> = | <i>0b001100</i>         |        | (USART0)                              |
|     | 0b0000             | USART0RXDATAV           |        | USART0RXDATAV REQ/SREQ                |
|     | 0b0001             | USART0TXBL              |        | USART0TXBL REQ/SREQ                   |
|     | 0b0010             | USART0TXEMPTY           |        | USART0TXEMPTY                         |
|     | <i>SOURCESEL</i> = | <i>0b001101</i>         |        | (USART1)                              |
|     | 0b0000             | USART1RXDATAV           |        | USART1RXDATAV REQ/SREQ                |
|     | 0b0001             | USART1TXBL              |        | USART1TXBL REQ/SREQ                   |
|     | 0b0010             | USART1TXEMPTY           |        | USART1TXEMPTY                         |
|     | 0b0011             | USART1RXDATAV-<br>RIGHT |        | USART1RXDATAVRIGHT REQ/SREQ           |
|     | 0b0100             | USART1TXBLRIGHT         |        | USART1TXBLRIGHT REQ/SREQ              |
|     | <i>SOURCESEL</i> = | <i>0b001110</i>         |        | (USART2)                              |
|     | 0b0000             | USART2RXDATAV           |        | USART2RXDATAV REQ/SREQ                |
|     | 0b0001             | USART2TXBL              |        | USART2TXBL REQ/SREQ                   |
|     | 0b0010             | USART2TXEMPTY           |        | USART2TXEMPTY                         |
|     | <i>SOURCESEL</i> = | <i>0b010000</i>         |        | (LEUART0)                             |
|     | 0b0000             | LEUART0RXDATAV          |        | LEUART0RXDATAV                        |
|     | 0b0001             | LEUART0TXBL             |        | LEUART0TXBL                           |
|     | 0b0010             | LEUART0TXEMPTY          |        | LEUART0TXEMPTY                        |
|     | <i>SOURCESEL</i> = | <i>0b010100</i>         |        | (I2C0)                                |
|     | 0b0000             | I2C0RXDATAV             |        | I2C0RXDATAV REQ/SREQ                  |
|     | 0b0001             | I2C0TXBL                |        | I2C0TXBL REQ/SREQ                     |
|     | <i>SOURCESEL</i> = | <i>0b010101</i>         |        | (I2C1)                                |
|     | 0b0000             | I2C1RXDATAV             |        | I2C1RXDATAV REQ/SREQ                  |
|     | 0b0001             | I2C1TXBL                |        | I2C1TXBL REQ/SREQ                     |

| Bit | Name               | Reset           | Access | Description              |
|-----|--------------------|-----------------|--------|--------------------------|
|     | <i>SOURCESEL =</i> | <i>0b011000</i> |        | <i>(TIMER0)</i>          |
|     | 0b0000             | TIMER0UFOF      |        | TIMER0UFOF               |
|     | 0b0001             | TIMER0CC0       |        | TIMER0CC0                |
|     | 0b0010             | TIMER0CC1       |        | TIMER0CC1                |
|     | 0b0011             | TIMER0CC2       |        | TIMER0CC2                |
|     | <i>SOURCESEL =</i> | <i>0b011001</i> |        | <i>(TIMER1)</i>          |
|     | 0b0000             | TIMER1UFOF      |        | TIMER1UFOF               |
|     | 0b0001             | TIMER1CC0       |        | TIMER1CC0                |
|     | 0b0010             | TIMER1CC1       |        | TIMER1CC1                |
|     | 0b0011             | TIMER1CC2       |        | TIMER1CC2                |
|     | 0b0100             | TIMER1CC3       |        | TIMER1CC3                |
|     | <i>SOURCESEL =</i> | <i>0b011010</i> |        | <i>(WTIMER0)</i>         |
|     | 0b0000             | WTIMER0UFOF     |        | WTIMER0UFOF              |
|     | 0b0001             | WTIMER0CC0      |        | WTIMER0CC0               |
|     | 0b0010             | WTIMER0CC1      |        | WTIMER0CC1               |
|     | 0b0011             | WTIMER0CC2      |        | WTIMER0CC2               |
|     | <i>SOURCESEL =</i> | <i>0b110000</i> |        | <i>(MSC)</i>             |
|     | 0b0000             | MSCWDATA        |        | MSCWDATA REQ/SREQ        |
|     | <i>SOURCESEL =</i> | <i>0b110001</i> |        | <i>(CRYPTO0)</i>         |
|     | 0b0000             | CRYPTO0DATA0WR  |        | CRYPTO0DATA0WR           |
|     | 0b0001             | CRYPTO0DATA0XWR |        | CRYPTO0DATA0XWR          |
|     | 0b0010             | CRYPTO0DATA0RD  |        | CRYPTO0DATA0RD           |
|     | 0b0011             | CRYPTO0DATA1WR  |        | CRYPTO0DATA1WR           |
|     | 0b0100             | CRYPTO0DATA1RD  |        | CRYPTO0DATA1RD           |
|     | <i>SOURCESEL =</i> | <i>0b110010</i> |        | <i>(CSEN)</i>            |
|     | 0b0000             | CSENDATA        |        | CSENDATA                 |
|     | 0b0001             | CSENBSLN        |        | CSENBSLN                 |
|     | <i>SOURCESEL =</i> | <i>0b110011</i> |        | <i>(LESENSE)</i>         |
|     | 0b0000             | LESENSEBUFDATAV |        | LESENSEBUFDATAV REQ/SREQ |
|     | <i>SOURCESEL =</i> | <i>0b110100</i> |        | <i>(CRYPTO1)</i>         |
|     | 0b0000             | CRYPTO1DATA0WR  |        | CRYPTO1DATA0WR           |
|     | 0b0001             | CRYPTO1DATA0XWR |        | CRYPTO1DATA0XWR          |
|     | 0b0010             | CRYPTO1DATA0RD  |        | CRYPTO1DATA0RD           |
|     | 0b0011             | CRYPTO1DATA1WR  |        | CRYPTO1DATA1WR           |
|     | 0b0100             | CRYPTO1DATA1RD  |        | CRYPTO1DATA1RD           |

## 9.6.18 LDMA\_CHx\_CFG - Channel Configuration Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |            |            |    |    |    |    |          |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|------------|------------|----|----|----|----|----------|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|
| 0x084         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20         | 19         | 18 | 17 | 16 | 15 | 14       | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    | 0          | 0          |    |    |    |    | 0x0      |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    | RW         | RW         |    |    |    |    | RW       |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    | DSTINCSIGN | SRCINCSIGN |    |    |    |    | ARBSLOTS |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |

| Bit   | Name   | Reset   | Access                           | Description                               |
|-------|--|---|----------------------------------|---|
| 31:22 | <i>Reserved</i>  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                  |   |
| 21    | DSTINCSIGN   | 0   | RW                               | <b>Destination Address Increment Sign</b> |
|       | Value  | Mode  | Description                      |   |
|       | 0  | POSITIVE  | Increment destination address    |   |
|       | 1  | NEGATIVE  | Decrement destination address    |   |
| 20    | SRCINCSIGN   | 0   | RW                               | <b>Source Address Increment Sign</b>      |
|       | Value  | Mode  | Description                      |   |
|       | 0  | POSITIVE  | Increment source address         |   |
|       | 1  | NEGATIVE  | Decrement source address         |   |
| 19:18 | <i>Reserved</i>  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                  |   |
| 17:16 | ARBSLOTS   | 0x0   | RW                               | <b>Arbitration Slot Number Select</b>     |
|       | For channels using round robin arbitration, this bit-field is used to select the number of slots in the round robin queue. |   |                                  |   |
|       | Value  | Mode  | Description                      |   |
|       | 0  | ONE   | One arbitration slot selected    |   |
|       | 1  | TWO   | Two arbitration slots selected   |   |
|       | 2  | FOUR  | Four arbitration slots selected  |   |
|       | 3  | EIGHT   | Eight arbitration slots selected |   |
| 15:0  | <i>Reserved</i>  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                  |   |

## 9.6.19 LDMA\_CHx\_LOOP - Channel Loop Counter Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |         |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---------|---|---|---|
| 0x088         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3       | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0x00    |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | RWH     |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | LOOPCNT |   |   |   |

| Bit  | Name     | Reset  | Access | Description  |
|------|----------|--|--------|--|
| 31:8 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 7:0  | LOOPCNT  | 0x00   | RWH    | <b>Linked Structure Sequence Loop Counter</b><br><br>This bit-field specifies the number of iterations when using looping descriptors. Software should write to LOOPCNT before using a looping descriptor. |

### 9.6.20 LDMA\_CHx\_CTRL - Channel Descriptor Control Word Register

| Offset        | Bit Position |         |        |    |      |    |        |    |            |           |         |           |    |           |    |    |          |    |    |    |    |    |   |   |   |         |   |   |   |   |   |   |   |           |  |     |            |
|---------------|--------------|---------|--------|----|------|----|--------|----|------------|-----------|---------|-----------|----|-----------|----|----|----------|----|----|----|----|----|---|---|---|---------|---|---|---|---|---|---|---|-----------|--|-----|------------|
| 0x08C         | 31           | 30      | 29     | 28 | 27   | 26 | 25     | 24 | 23         | 22        | 21      | 20        | 19 | 18        | 17 | 16 | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6       | 5 | 4 | 3 | 2 | 1 | 0 |   |           |  |     |            |
| <b>Reset</b>  | 0            | 0       | 0x0    |    | 0x0  |    | 0x0    |    | 0          | 0         | 0       | 0         |    | 0x0       |    |    | 0        |    |    |    |    |    |   |   |   | 0x000   |   |   |   |   |   |   | 0 |           |  | 0x0 |            |
| <b>Access</b> | R            | R       | RWH    |    | RWH  |    | RWH    |    | RWH        | RWH       | RWH     | RWH       |    | RWH       |    |    | RWH      |    |    |    |    |    |   |   |   | RWH     |   |   |   |   |   |   |   | W1        |  |     | R          |
| <b>Name</b>   | DSTMODE      | SRCMODE | DSTINC |    | SIZE |    | SRCINC |    | IGNORESREQ | DECLOPCNT | REQMODE | DONEIFSEN |    | BLOCKSIZE |    |    | BYTESWAP |    |    |    |    |    |   |   |   | XFERCNT |   |   |   |   |   |   |   | STRUCTREQ |  |     | STRUCTTYPE |

| Bit   | Name     | Reset  | Access | Description   |       |      |             |   |          |  |   |          |   |   |      |  |   |      |  |
|-------|----------|--|--------|---|-------|------|-------------|---|----------|--|---|----------|---|---|------|--|---|------|--|
| 31    | DSTMODE  | 0  | R      | <b>Destination Addressing Mode</b><br><br>This field specifies the destination addressing mode of linked descriptors. After loading a linked descriptor, reading this field will indicate the destination addressing mode of the linked descriptor. Note that the first descriptor always uses absolute addressing mode.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>ABSOLUTE</td> <td>The DSTADDR field of LDMA_CHx_DST contains the absolute address of the destination data.</td> </tr> <tr> <td>1</td> <td>RELATIVE</td> <td>The DSTADDR field of LDMA_CHx_DST contains the relative offset of the destination data.</td> </tr> </tbody> </table>   | Value | Mode | Description | 0 | ABSOLUTE | The DSTADDR field of LDMA_CHx_DST contains the absolute address of the destination data. | 1 | RELATIVE | The DSTADDR field of LDMA_CHx_DST contains the relative offset of the destination data. |   |      |  |   |      |  |
| Value | Mode     | Description  |        |   |       |      |             |   |          |  |   |          |   |   |      |  |   |      |  |
| 0     | ABSOLUTE | The DSTADDR field of LDMA_CHx_DST contains the absolute address of the destination data.                                 |        |   |       |      |             |   |          |  |   |          |   |   |      |  |   |      |  |
| 1     | RELATIVE | The DSTADDR field of LDMA_CHx_DST contains the relative offset of the destination data.                                  |        |   |       |      |             |   |          |  |   |          |   |   |      |  |   |      |  |
| 30    | SRCMODE  | 0  | R      | <b>Source Addressing Mode</b><br><br>This field specifies the source addressing mode of linked descriptors. After loading a linked descriptor, reading this field will indicate the source addressing mode of the linked descriptor. Note that the first descriptor always uses absolute addressing mode.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>ABSOLUTE</td> <td>The SRCADDR field of LDMA_CHx_SRC contains the absolute address of the source data.</td> </tr> <tr> <td>1</td> <td>RELATIVE</td> <td>The SRCADDR field of LDMA_CHx_SRC contains the relative offset of the source data.</td> </tr> </tbody> </table>  | Value | Mode | Description | 0 | ABSOLUTE | The SRCADDR field of LDMA_CHx_SRC contains the absolute address of the source data.      | 1 | RELATIVE | The SRCADDR field of LDMA_CHx_SRC contains the relative offset of the source data.      |   |      |  |   |      |  |
| Value | Mode     | Description  |        |   |       |      |             |   |          |  |   |          |   |   |      |  |   |      |  |
| 0     | ABSOLUTE | The SRCADDR field of LDMA_CHx_SRC contains the absolute address of the source data.                                      |        |   |       |      |             |   |          |  |   |          |   |   |      |  |   |      |  |
| 1     | RELATIVE | The SRCADDR field of LDMA_CHx_SRC contains the relative offset of the source data.                                       |        |   |       |      |             |   |          |  |   |          |   |   |      |  |   |      |  |
| 29:28 | DSTINC   | 0x0  | RWH    | <b>Destination Address Increment Size</b><br><br>This bit-field specifies the stride or number of unit data addresses to increment the destination address after each unit of data is transferred. The unit data width is controlled by the SIZE bit-field and can be a byte, half-word or word.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>ONE</td> <td>Increment destination address by one unit data size after each write</td> </tr> <tr> <td>1</td> <td>TWO</td> <td>Increment destination address by two unit data sizes after each write</td> </tr> <tr> <td>2</td> <td>FOUR</td> <td>Increment destination address by four unit data sizes after each write</td> </tr> <tr> <td>3</td> <td>NONE</td> <td>Do not increment the destination address. Writes are made to a fixed destination address, for example writing to a FIFO.</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | ONE      | Increment destination address by one unit data size after each write                     | 1 | TWO      | Increment destination address by two unit data sizes after each write                   | 2 | FOUR | Increment destination address by four unit data sizes after each write | 3 | NONE | Do not increment the destination address. Writes are made to a fixed destination address, for example writing to a FIFO. |
| Value | Mode     | Description  |        |   |       |      |             |   |          |  |   |          |   |   |      |  |   |      |  |
| 0     | ONE      | Increment destination address by one unit data size after each write   |        |   |       |      |             |   |          |  |   |          |   |   |      |  |   |      |  |
| 1     | TWO      | Increment destination address by two unit data sizes after each write  |        |   |       |      |             |   |          |  |   |          |   |   |      |  |   |      |  |
| 2     | FOUR     | Increment destination address by four unit data sizes after each write   |        |   |       |      |             |   |          |  |   |          |   |   |      |  |   |      |  |
| 3     | NONE     | Do not increment the destination address. Writes are made to a fixed destination address, for example writing to a FIFO. |        |   |       |      |             |   |          |  |   |          |   |   |      |  |   |      |  |

| Bit   | Name       | Reset    | Access | Description  |
|-------|------------|----------|--------|--|
| 27:26 | SIZE       | 0x0      | RWH    | <b>Unit Data Transfer Size</b><br>This field specifies the size of data transferred.   |
|       | Value      | Mode     |        | Description  |
|       | 0          | BYTE     |        | Each unit transfer is a byte   |
|       | 1          | HALFWORD |        | Each unit transfer is a half-word  |
|       | 2          | WORD     |        | Each unit transfer is a word   |
| 25:24 | SRCINC     | 0x0      | RWH    | <b>Source Address Increment Size</b><br>This bit-field specifies the stride or number of unit data addresses to increment the source address after each unit of data is transferred. The unit data width is controlled by the SIZE bit-field and can be a byte, half-word or word. |
|       | Value      | Mode     |        | Description  |
|       | 0          | ONE      |        | Increment source address by one unit data size after each read   |
|       | 1          | TWO      |        | Increment source address by two unit data sizes after each read  |
|       | 2          | FOUR     |        | Increment source address by four unit data sizes after each read   |
|       | 3          | NONE     |        | Do not increment the source address. In this mode reads are made from a fixed source address, for example reading FIFO.  |
| 23    | IGNORESREQ | 0        | RWH    | <b>Ignore Sreq</b><br>The channel arbiter will ignore single requests (SREQ) and only respond to multiple requests (REQ) when this bit is set.   |
| 22    | DECLOOPCNT | 0        | RWH    | <b>Decrement Loop Count</b><br>When using looping, setting this bit will decrement the LOOPCNT field in the LDMA_CHx_LOOP register after each descriptor execution.  |
| 21    | REQMODE    | 0        | RWH    | <b>DMA Request Transfer Mode Select</b>  |
|       | Value      | Mode     |        | Description  |
|       | 0          | BLOCK    |        | The LDMA transfers one BLOCKSIZE per transfer request.   |
|       | 1          | ALL      |        | One transfer request transfers all units as defined by the XFRCNT field.   |
| 20    | DONEIFSEN  | 0        | RWH    | <b>DMA Operation Done Interrupt Flag Set Enable</b><br>Setting this bit will set the interrupt flag when the transfer is done, or linked in the case where the LINK bit is set, or synchronized in the case of a SYNC transfer.  |
| 19:16 | BLOCKSIZE  | 0x0      | RWH    | <b>Block Transfer Size</b><br>This bit-field controls the number of unit data transfers per arbitration cycle  |
|       | Value      | Mode     |        | Description  |
|       | 0          | UNIT1    |        | One unit transfer per arbitration  |
|       | 1          | UNIT2    |        | Two unit transfers per arbitration   |
|       | 2          | UNIT3    |        | Three unit transfers per arbitration   |
|       | 3          | UNIT4    |        | Four unit transfers per arbitration  |
|       | 4          | UNIT6    |        | Six unit transfers per arbitration   |

| Bit  | Name            | Reset   | Access   | Description  |
|------|-----------------|---|--|--|
| 5    |                 | UNIT8   |  | Eight unit transfers per arbitration   |
| 7    |                 | UNIT16  |  | Sixteen unit transfers per arbitration   |
| 9    |                 | UNIT32  |  | 32 unit transfers per arbitration  |
| 10   |                 | UNIT64  |  | 64 unit transfers per arbitration  |
| 11   |                 | UNIT128   |  | 128 unit transfers per arbitration   |
| 12   |                 | UNIT256   |  | 256 unit transfers per arbitration   |
| 13   |                 | UNIT512   |  | 512 unit transfers per arbitration   |
| 14   |                 | UNIT1024  |  | 1024 unit transfers per arbitration  |
| 15   |                 | ALL   |  | Transfer all units as specified by the XFRCNT field  |
| 15   | BYTESWAP        | 0   | RWH  | <b>Endian Byte Swap</b><br>For word and half-word transfers, setting this bit will swap all bytes of each word or half-word.   |
| 14:4 | XFERCNT         | 0x000   | RWH  | <b>DMA Unit Data Transfer Count</b><br>Specifies number of unit data (words, half-words, or bytes) to transfer, as determined by the SIZE field. The value written should be one less than the desired transfer count. |
| 3    | STRUCTREQ       | 0   | W1   | <b>Structure DMA Transfer Request</b><br>When a linked descriptor is loaded with this bit set, it will immediately trigger a transfer.   |
| 2    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |  |
| 1:0  | STRUCTTYPE      | 0x0   | R  | <b>DMA Structure Type</b>  |
|      | Value           | Mode  | Description                                    |  |
|      | 0               | TRANSFER  | DMA transfer structure type selected.          |  |
|      | 1               | SYNCHRONIZE   | Synchronization structure type selected.       |  |
|      | 2               | WRITE   | Write immediate value structure type selected. |  |

## 9.6.21 LDMA\_CHx\_SRC - Channel Descriptor Source Data Address Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x090         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | SRCADDR    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name    | Reset      | Access | Description                |
|---|---------|------------|--------|----------------------------|
| 31:0  | SRCADDR | 0x00000000 | RWH    | <b>Source Data Address</b> |
| <p>Writing to this register sets the source address. Reading from this register during a DMA transfer will indicate the next source read address. The value of this register is incremented or decremented with each source read.</p> |         |            |        |                            |

## 9.6.22 LDMA\_CHx\_DST - Channel Descriptor Destination Data Address Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x094         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DSTADDR    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

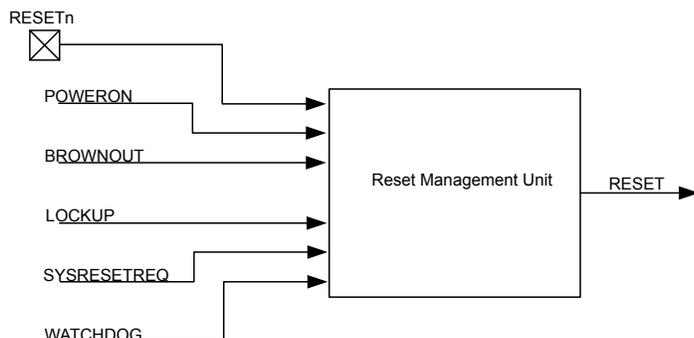
| Bit   | Name    | Reset      | Access | Description                     |
|---|---------|------------|--------|---------------------------------|
| 31:0  | DSTADDR | 0x00000000 | RWH    | <b>Destination Data Address</b> |
| <p>Writing to this register sets the destination address. Reading from this register during a DMA transfer will indicate the next destination write address. This value of this register is incremented or decremented with each destination write.</p> |         |            |        |                                 |

9.6.23 LDMA\_CHx\_LINK - Channel Descriptor Link Structure Address Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |      |          |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------|----------|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x098         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15   | 14       | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0x00000000   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0    | 0        |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> | RWH          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH  | R        |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | LINKADDR     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LINK | LINKMODE |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name     | Reset      | Access  | Description  |
|------|----------|------------|---|--|
| 31:2 | LINKADDR | 0x00000000 | RWH   | <b>Link Structure Address</b><br><br>To use linking, write the address of the the first linked descriptor to this register. When a linked descriptor is loaded, it may also be linked to another descriptor. Reading this register will reflect the address of the next linked descriptor.                 |
| 1    | LINK     | 0          | RWH   | <b>Link Next Structure</b><br><br>After completing the initial transfer, if this bit is set, the DMA will load the next linked descriptor. If the next linked descriptor also has this bit set, the DMA will load the next linked descriptor.  |
| 0    | LINKMODE | 0          | R   | <b>Link Structure Addressing Mode</b><br><br>This field specifies the addressing mode of linked descriptors. After loading a linked descriptor, reading this field will indicate the addressing mode of the loaded linked descriptor. Note that the first descriptor always uses absolute addressing mode. |
|      | Value    | Mode       | Description   |  |
|      | 0        | ABSOLUTE   | The LINKADDR field of LDMA_CHx_LINK contains the absolute address of the linked descriptor. |  |
|      | 1        | RELATIVE   | The LINKADDR field of LDMA_CHx_LINK contains the relative offset of the linked descriptor.  |  |

## 10. RMU - Reset Management Unit



### Quick Facts

#### What?

The RMU ensures correct reset operation. It is responsible for connecting the different reset sources to the reset lines of the EFR32xG13 Wireless Gecko.

#### Why?

A correct reset sequence is needed to ensure safe and synchronous startup of the EFR32xG13 Wireless Gecko. In the case of error situations such as power supply glitches or software crash, the RMU provides proper reset and startup of the EFR32xG13 Wireless Gecko.

#### How?

The Power-on Reset and Brown-out Detector of the EFR32xG13 Wireless Gecko provides power line monitoring with exceptionally low power consumption. The cause of the reset may be read from a register, thus providing software with information about the cause of the reset.

### 10.1 Introduction

The RMU is responsible for handling the reset functionality of the EFR32xG13 Wireless Gecko.

### 10.2 Features

- Reset sources
  - Power-on Reset (POR)
  - Brown-out Detection (BOD) on the following power domains:
    - Analog Unregulated Power Domain AVDD
    - Digital Unregulated Power Domain DVDD
    - Regulated Digital Domain DECOUPLE (DEC)
  - RESETEn pin reset
  - Watchdog reset
  - Software triggered reset (SYSRESETREQ)
  - Core LOCKUP condition
- EM4 Hibernate/Shutoff Detection
- EM4 Hibernate/Shutoff wakeup reset from GPIO pin
- Configurable reset levels
- A software readable register indicates the cause of the last reset

### 10.3 Functional Description

The RMU monitors each of the reset sources of the EFR32xG13 Wireless Gecko. If one or more reset sources go active, the RMU applies reset to the EFR32xG13 Wireless Gecko. When the reset sources go inactive the EFR32xG13 Wireless Gecko starts up. At startup the EFR32xG13 Wireless Gecko loads the stack pointer and program entry point from memory, and starts execution. [Figure 10.1 RMU Reset Input Sources and Connections on page 237](#) shows an overview of the reset system on EFR32xG13 Wireless Gecko.

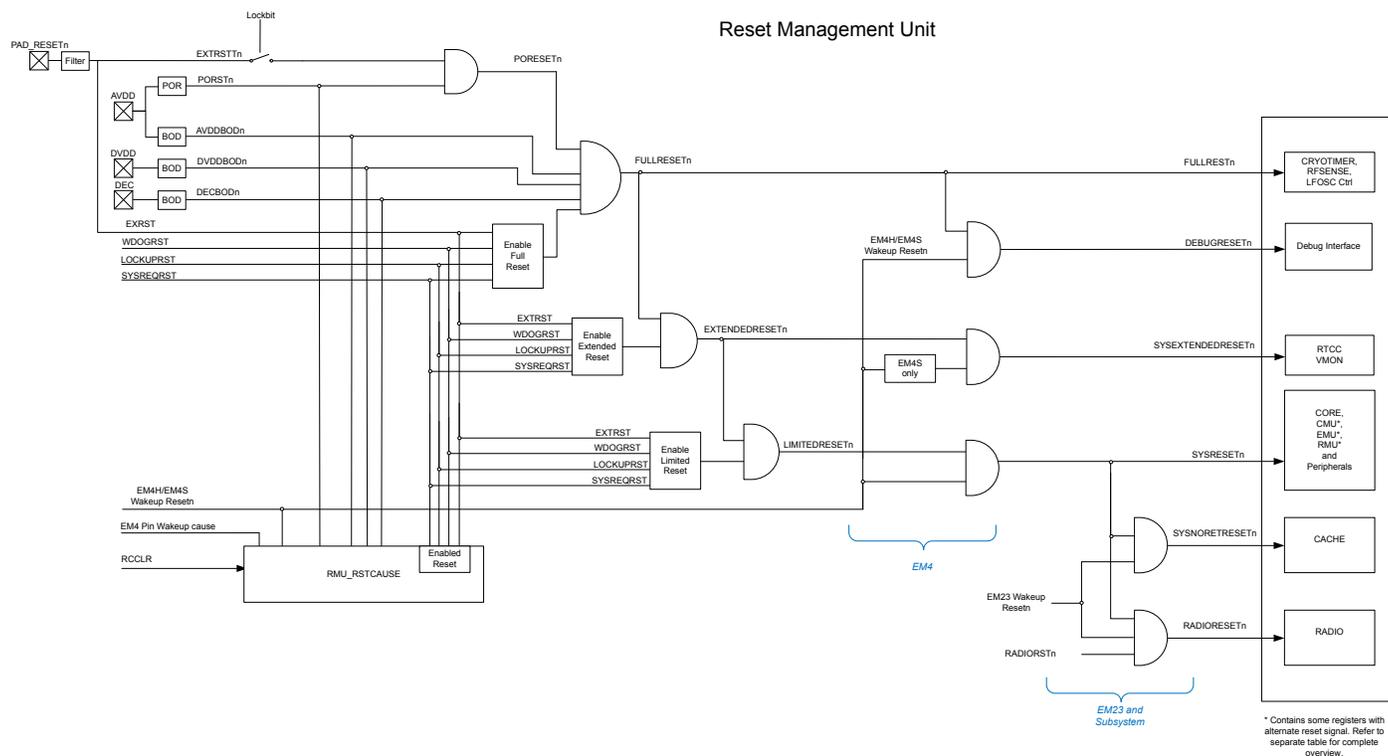


Figure 10.1. RMU Reset Input Sources and Connections

### 10.3.1 Reset Levels

The reset sources on EFR32xG13 Wireless Gecko can be divided in two main groups; Hard resets and Soft resets.

The soft resets can be configured to be either DISABLED, LIMITED, EXTENDED or FULL. The reset level for soft reset sources is configured in the xxxRMODE bitfields in RMU\_CTRL.

**Table 10.1. Reset Levels**

| RMU_CTRL_xxxRMODE | Parts of System Reset   |
|-------------------|---|
| DISABLED          | Nothing is reset, request will not be registered in RMU_RSTCAUSE  |
| LIMITED           | Everything reset, with exception of CRYOTIMER, RFSENSE, DEBUGGER, RTCC, VMON and parts of CMU, RMU and EMU. |
| EXTENDED          | Everything reset, with exception of CRYOTIMER, RFSENSE, DEBUGGER, and parts of CMU, RMU and EMU.            |
| FULL              | Everything reset, with exception of some registers in RMU and EMU.  |

The reset sources resulting in a soft reset are:

- Watchdog reset
- Lockup reset
- System reset request
- Pin reset (Pin reset can be configured to be either a soft or a hard reset, see [10.3.5 RESETn Pin Reset](#) for details.)

**Note:** LIMITED and EXTENDED resets are synchronized to HFSRCCLK. If HFSRCCLK is slow, there will be latency on reset assertion. If HFSRCCLK is not running, reset will be asserted after a timeout.

Hard resets will reset the entire chip, the reset sources resulting in a hard reset are:

- Power-on reset
- Brown-out reset
- Pin reset (Pin reset can be configured to be either a soft or a hard reset, see [10.3.5 RESETn Pin Reset](#) for details.)

### 10.3.2 RMU\_RSTCAUSE Register

Whenever a reset source is active, the corresponding bit in the RMU\_RSTCAUSE register is set. At startup the program code may investigate this register in order to determine the cause of the reset. The register is cleared upon POR and software write to RMU\_CMD\_RCCLR. The register should be cleared after the value has been read at startup, otherwise the register may indicate multiple causes for the reset at next startup.

RMU\_RSTCAUSE should be interpreted according to [Table 10.2 RMU Reset Cause Register Interpretation on page 239](#). In [Table 10.2 RMU Reset Cause Register Interpretation on page 239](#), the reset causes are ordered by severity from right to left. A reset cause bit is invalidated (i.e. can not be trusted) if one of the bits to the right of it does not match the table. X bits are don't care.

**Note:** It is possible to have multiple reset causes. For example, an external reset and a watchdog reset may happen simultaneously.

**Table 10.2. RMU Reset Cause Register Interpretation**

| RMU_RSTCAUSE |         |           |           |                  |        |         |         |       | Reset cause             |
|--------------|---------|-----------|-----------|------------------|--------|---------|---------|-------|-------------------------|
| EM4RST       | WDOGRST | SYSREQRST | LOCKUPRST | EXTRST           | DECBOD | DVDDBOD | AVDDBOD | PORST |                         |
| X            | X       | X         | X         | X                | X      | X       | X       | 1     | Power on reset          |
| X            | X       | X         | X         | X                | X      | X       | 1       | 0     | Brown-out on AVDD power |
| X            | X       | X         | X         | X                | X      | 1       | X       | 0     | Brown-out on DVDD power |
| X            | X       | X         | X         | X                | 1      | X       | X       | 0     | Brown-out on DEC power  |
| X            | X       | X         | X         | 1                | X      | X       | X       | 0     | Pin reset               |
| X            | X       | X         | 1         | 0/X <sup>1</sup> | 0      | 0       | 0       | 0     | Lockup reset            |
| X            | X       | 1         | X         | 0/X <sup>1</sup> | 0      | 0       | 0       | 0     | System reset request    |
| X            | 1       | X         | X         | 0/X <sup>1</sup> | 0      | 0       | 0       | 0     | Watchdog reset          |
| 1            | X       | X         | X         | 0/X <sup>1</sup> | 0      | 0       | 0       | 0     | System has been in EM4  |

1. Pin reset configured as hard/soft

### 10.3.3 Power-On Reset (POR)

The POR ensures that the EFR32xG13 Wireless Gecko does not start up before the AVDD supply voltage has reached the threshold voltage  $V_{PORthr}$  (roughly 1.2V). Before the POR threshold voltage is reached, the EFR32xG13 Wireless Gecko is kept in reset state. The operation of the POR is illustrated in [Figure 10.2 RMU Power-on Reset Operation on page 240](#), with the active low  $POWERONn$  reset signal. The reason for the “unknown” region is that the corresponding supply voltage is too low for any reliable operation.

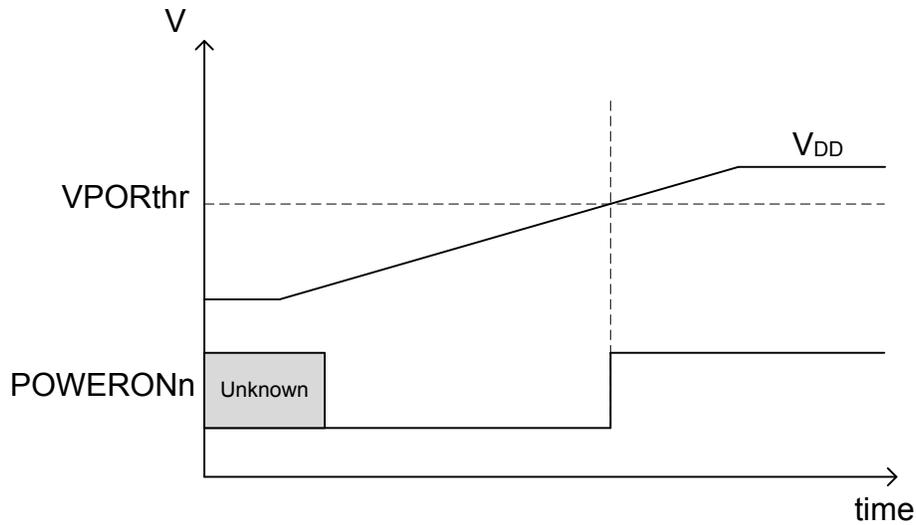


Figure 10.2. RMU Power-on Reset Operation

### 10.3.4 Brown-Out Detector (BOD)

The EFR32xG13 Wireless Gecko has 3 brownout detectors, one for the unregulated power (DVDD), one for the regulated internal power (DECOUPLE), and one for the Analog Power Domain (AVDD). The BODs are constantly monitoring these supply voltages. Whenever the unregulated or regulated power drops below the  $VBODthr$  value (see the Electrical Characteristics section of the data sheet for details), or if AVDD drops below the voltage at the DECOUPLE pin, the corresponding active low  $BROWNOUTn$  line is held low. The BODs also include hysteresis, which prevents instability in the corresponding  $BROWNOUTn$  line when the supply is crossing the  $VBODthr$  limit or the AVDD supply drops below the DECOUPLE pin. The operation of the BOD is illustrated in [Figure 10.3 RMU Brown-out Detector Operation on page 240](#). The “unknown” regions are handled by the POR module.

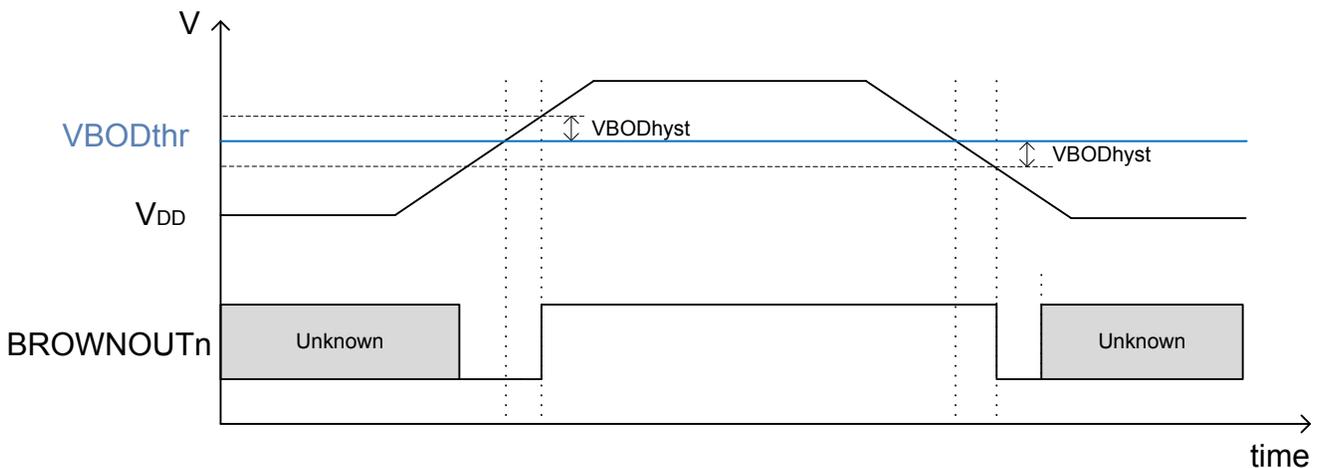


Figure 10.3. RMU Brown-out Detector Operation

### 10.3.5 RESETEn Pin Reset

The pin reset on EFR32xG13 Wireless Gecko can be configured to be either hard or soft. By default, pin reset is configured as a soft reset source. To configure it as a hard reset, clear the PINRESETSOFT bit in CLW0 in the Lock bit page, see [8.3.2 Lock Bits \(LB\) Page Description](#) for details. Forcing the RESETEn pin low generates a reset of the EFR32xG13 Wireless Gecko. The RESETEn pin includes an on-chip pull-up resistor, and can therefore be left unconnected if no external reset source is needed. Also connected to the RESETEn line is a filter which prevents glitches from resetting the EFR32xG13 Wireless Gecko.

### 10.3.6 Watchdog Reset

The Watchdog circuit is a timer which (when enabled) must be cleared by software regularly. If software does not clear it, a Watchdog reset is activated. This functionality provides recovery from a software stalemate. Refer to the Watchdog section for specifications and description. The Watchdog reset can be configured to cause different levels of reset as determined by WDOGRMODE in the RMU\_CTRL register.

### 10.3.7 Lockup Reset

A Cortex-M4 lockup is the result of the core being locked up because of an unrecoverable exception following the activation of the processor's built-in system state protection hardware.

A Cortex-M4 lockup gives immediate indication of seriously errant kernel software. This is the result of the core being locked up due to an unrecoverable exception following the activation of the processor's built in system state protection hardware. For more information about the Cortex-M4 lockup conditions see the ARMv7-M Architecture Reference Manual. The Lockup reset does not reset the Debug Interface, unless configured as a FULL reset. The Lockup reset can be configured to cause different levels of reset as determined by the LOCKUPRMODE bits in the RMU\_CTRL register. This includes disabling the reset.

### 10.3.8 System Reset Request

Software may initiate a reset (e.g. if it finds itself in a non-recoverable state). By asserting the SYSRESETREQ in the Application Interrupt and Reset Control Register, a reset is issued. The SYSRESETREQ does not reset the Debug Interface, unless configured as a FULL reset. The SYSRESETREQ reset can be configured to cause different levels of reset as determined by SYSRESETRMODE bits in the RMU\_CTRL register. This includes disabling the reset.

### 10.3.9 Reset State

The RESETSTATE bitfield in RMU\_CTRL is a read-write register intended for software use only, and can be used to keep track of state throughout a reset. This bitfield is only reset by POR and hard pin reset.

### 10.3.10 Register Reset Signals

[Figure 10.1 RMU Reset Input Sources and Connections on page 237](#) shows an overview of how the different parts of the design are affected by the different levels of reset. For RMU, EMU and CMU there are some exceptions. These are given in the following tables.

## 10.3.10.1 Registers With Alternate Reset

Table 10.3. Alternate Reset for Registers in RMU

| RMU Reset Levels       |   |
|------------------------|---|
| POR and hard pin reset | RMU_CTRL_WDOGRMODE<br>RMU_CTRL_LOCKUPRMODE<br>RMU_CTRL_SYSRMODE<br>RMU_CTRL_PINRMODE<br>RMU_CTRL_RESETSTATE |
| FULL reset             | RMU_LOCK_LOCKKEY  |

Table 10.4. Alternate Reset for Registers in CMU

| CMU Reset Levels |   |
|------------------|---|
| FULL reset       | CMU_LFRCOCTRL<br>CMU_LFXOCTRL                   |
| EXTENDED reset   | CMU_LFECLKSEL<br>CMU_LFECLKEN0<br>CMU_LFEPRESC0 |

Table 10.5. Alternate Reset for Registers in EMU

| EMU Reset Levels             |  |
|------------------------------|--|
| POR, BOD, and hard pin reset | EMU_BIASCONF_LSBIAS_SEL  |
| POR, BOD, and hard pin reset | EMU_DCDCLNVCTRL  |
| POR and hard pin reset       | EMU_CTRL_EM2BODDIS   |
| POR, BOD, and hard pin reset | EMU_PWRCTRL<br>EMU_DCDCCTRL<br>EMU_DCDCMISCCTRL<br>EMU_DCDCZDETCTRL<br>EMU_DCDCLIMCTRL<br>EMU_DCDCLNCOMPCTRL<br>EMU_DCDCLPVCTRL<br>EMU_DCDCLPCTRL<br>EMU_DCDCLNFREQCTRL<br>EMU_DCDCLPEM01CFG |

| EMU Reset Levels |  |
|------------------|--|
| EXTENDED reset   | EMU_VMONAVDDCTRL<br>EMU_VMONALTAVDDCTRL<br>EMU_VMONDVDDCTRL<br>EMU_VMONIO0CTRL |
| FULL reset       | EMU_EM4CTRL  |

#### 10.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name         | Type | Description                 |
|--------|--------------|------|-----------------------------|
| 0x000  | RMU_CTRL     | RW   | Control Register            |
| 0x004  | RMU_RSTCAUSE | R    | Reset Cause Register        |
| 0x008  | RMU_CMD      | W1   | Command Register            |
| 0x00C  | RMU_RST      | RW   | Reset Control Register      |
| 0x010  | RMU_LOCK     | RWH  | Configuration Lock Register |

## 10.5 Register Description

### 10.5.1 RMU\_CTRL - Control Register

| Offset        | Bit Position |    |    |    |    |    |    |            |    |    |    |    |    |    |    |          |    |          |    |             |    |            |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|----------|----|----------|----|-------------|----|------------|---|---|---|---|---|---|---|---|---|---|
| 0x000         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24         | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16       | 15 | 14       | 13 | 12          | 11 | 10         | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    | 0x0        |    |    |    |    |    |    |    | 0x4      |    | 0x2      |    | 0x0         |    | 0x4        |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    | RW         |    |    |    |    |    |    |    | RW       |    | RW       |    | RW          |    | RW         |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    | RESETSTATE |    |    |    |    |    |    |    | PINRMODE |    | SYSRMODE |    | LOCKUPRMODE |    | WDOGGRMODE |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name       | Reset  | Access  | Description  |
|-------|------------|--|---|--|
| 31:26 | Reserved   | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |   |  |
| 25:24 | RESETSTATE | 0x0  | RW  | <b>System Software Reset State</b><br>Bit-field for software use only. This field has no effect on the RMU and is reset by power-on reset and hard pin reset only. |
| 23:15 | Reserved   | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |   |  |
| 14:12 | PINRMODE   | 0x4  | RW  | <b>PIN Reset Mode</b><br>Controls the reset level for Pin reset request. These settings only apply when PINRESETSOFT in CLW0 in the Lock bit page is set.          |
|       | Value      | Mode   | Description   |  |
|       | 0          | DISABLED   | Reset request is blocked.                                     |  |
|       | 1          | LIMITED  | The CRYOTIMER, DEBUGGER, RTCC, are not reset.                 |  |
|       | 2          | EXTENDED   | The CRYOTIMER, DEBUGGER are not reset. RTCC is reset.         |  |
|       | 4          | FULL   | The entire device is reset except some EMU and RMU registers. |  |
| 11    | Reserved   | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |   |  |
| 10:8  | SYSRMODE   | 0x2  | RW  | <b>Core Sysreset Reset Mode</b><br>Controls the reset level for Core SYSREST reset request.  |
|       | Value      | Mode   | Description   |  |
|       | 0          | DISABLED   | Reset request is blocked.                                     |  |
|       | 1          | LIMITED  | The CRYOTIMER, DEBUGGER, RTCC, are not reset.                 |  |
|       | 2          | EXTENDED   | The CRYOTIMER, DEBUGGER are not reset. RTCC is reset.         |  |
|       | 4          | FULL   | The entire device is reset except some EMU and RMU registers. |  |
| 7     | Reserved   | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |   |  |

| Bit | Name            | Reset   | Access | Description  |
|-----|-----------------|---|--------|--|
| 6:4 | LOCKUPRMODE     | 0x0   | RW     | <b>Core LOCKUP Reset Mode</b><br>Controls the reset level for Core LOCKUP reset request. |
|     | Value           | Mode  |        | Description  |
|     | 0               | DISABLED  |        | Reset request is blocked.  |
|     | 1               | LIMITED   |        | The CRYOTIMER, DEBUGGER, RTCC, are not reset.  |
|     | 2               | EXTENDED  |        | The CRYOTIMER, DEBUGGER are not reset. RTCC is reset.                                    |
|     | 4               | FULL  |        | The entire device is reset except some EMU and RMU registers.                            |
| 3   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 2:0 | WDOGRMODE       | 0x4   | RW     | <b>WDOG Reset Mode</b><br>Controls the reset level for WDOG reset request.               |
|     | Value           | Mode  |        | Description  |
|     | 0               | DISABLED  |        | Reset request is blocked. This disable bit is redundant with enable/disable bit in WDOG  |
|     | 1               | LIMITED   |        | The CRYOTIMER, DEBUGGER, RTCC, are not reset.  |
|     | 2               | EXTENDED  |        | The CRYOTIMER, DEBUGGER are not reset. RTCC is reset.                                    |
|     | 4               | FULL  |        | The entire device is reset except some EMU and RMU registers.                            |

### 10.5.2 RMU\_RSTCAUSE - Reset Cause Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |         |           |           |        |   |   |   |   |   |        |          |          |  |   |   |       |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---------|-----------|-----------|--------|---|---|---|---|---|--------|----------|----------|--|---|---|-------|--|
| 0x004         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16     | 15 | 14 | 13 | 12 | 11 | 10      | 9         | 8         | 7      | 6 | 5 | 4 | 3 | 2 | 1      | 0        |          |  |   |   |       |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0      |    |    |    |    |    | 0       | 0         | 0         | 0      |   |   |   |   |   | 0      | 0        | 0        |  | 0 | 0 |       |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R      |    |    |    |    |    | R       | R         | R         | R      |   |   |   |   |   | R      | R        | R        |  |   |   | R     |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | EM4RST |    |    |    |    |    | WDOGRST | SYSREQRST | LOCKUPRST | EXTRST |   |   |   |   |   | DECBOD | DVDDDBOD | AVDDDBOD |  |   |   | PORST |  |

| Bit   | Name      | Reset   | Access | Description   |
|-------|-----------|---|--------|---|
| 31:17 | Reserved  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 16    | EM4RST    | 0   | R      | <b>EM4 Reset</b><br>Set if the system has been in EM4. Must be cleared by software. See <a href="#">Table 10.2 RMU Reset Cause Register Interpretation on page 239</a> for details on how to interpret this bit.  |
| 15:12 | Reserved  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 11    | WDOGRST   | 0   | R      | <b>Watchdog Reset</b><br>Set if a watchdog reset has been performed. Must be cleared by software. See <a href="#">Table 10.2 RMU Reset Cause Register Interpretation on page 239</a> for details on how to interpret this bit.  |
| 10    | SYSREQRST | 0   | R      | <b>System Request Reset</b><br>Set if a system request reset has been performed. Must be cleared by software. See <a href="#">Table 10.2 RMU Reset Cause Register Interpretation on page 239</a> for details on how to interpret this bit.  |
| 9     | LOCKUPRST | 0   | R      | <b>LOCKUP Reset</b><br>Set if a LOCKUP reset has been requested. Must be cleared by software. See <a href="#">Table 10.2 RMU Reset Cause Register Interpretation on page 239</a> for details on how to interpret this bit.  |
| 8     | EXTRST    | 0   | R      | <b>External Pin Reset</b><br>Set if an external pin reset has been performed. Must be cleared by software. See <a href="#">Table 10.2 RMU Reset Cause Register Interpretation on page 239</a> for details on how to interpret this bit.   |
| 7:5   | Reserved  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 4     | DECBOD    | 0   | R      | <b>Brown Out Detector Decouple Domain Reset</b><br>Set if a regulated domain brown out detector reset has been performed. Must be cleared by software. See <a href="#">Table 10.2 RMU Reset Cause Register Interpretation on page 239</a> for details on how to interpret this bit. |
| 3     | DVDDDBOD  | 0   | R      | <b>Brown Out Detector DVDD Reset</b><br>Set if a unregulated domain brown out detector reset has been performed. Must be cleared by software. See <a href="#">Table 10.2 RMU Reset Cause Register Interpretation on page 239</a> for details on how to interpret this bit.          |
| 2     | AVDDDBOD  | 0   | R      | <b>Brown Out Detector AVDD Reset</b><br>Set if a unregulated domain brown out detector reset has been performed. Must be cleared by software. See <a href="#">Table 10.2 RMU Reset Cause Register Interpretation on page 239</a> for details on how to interpret this bit.          |
| 1     | Reserved  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |

| Bit   | Name  | Reset | Access | Description           |
|---|-------|-------|--------|-----------------------|
| 0   | PORST | 0     | R      | <b>Power on Reset</b> |
| Set if a power on reset has been performed. Must be cleared by software. See <a href="#">Table 10.2 RMU Reset Cause Register Interpretation on page 239</a> for details on how to interpret this bit. |       |       |        |                       |

### 10.5.3 RMU\_CMD - Command Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------|
| 0x008         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0     |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |
|               |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | RCCLR |
|               |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | W1    |

| Bit  | Name            | Reset   | Access | Description              |
|--|-----------------|---|--------|--------------------------|
| 31:1   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |                          |
| 0  | RCCLR           | 0   | W1     | <b>Reset Cause Clear</b> |
| Set this bit to clear the RSTCAUSE register. |                 |   |        |                          |

### 10.5.4 RMU\_RST - Reset Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x00C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

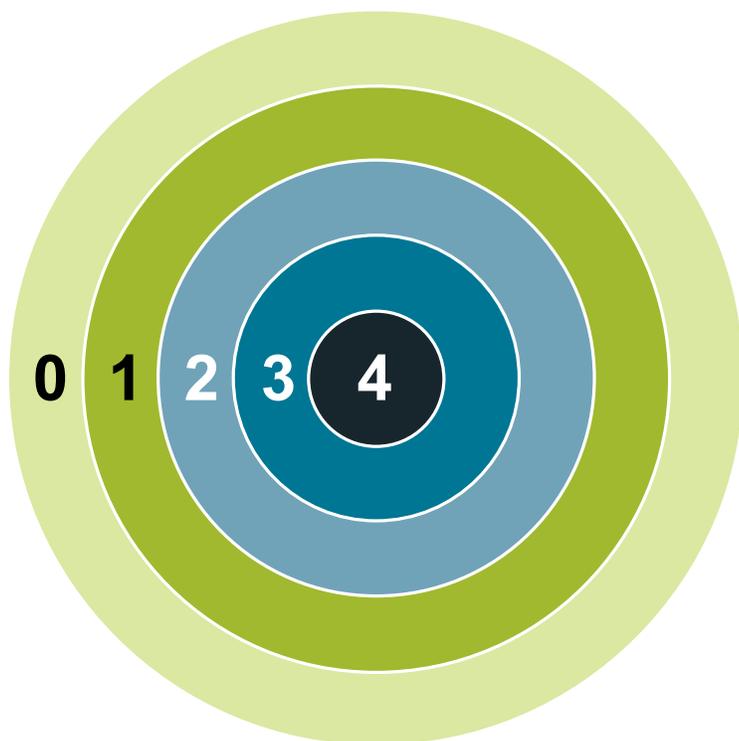
| Bit  | Name            | Reset   | Access | Description |
|------|-----------------|---|--------|-------------|
| 31:0 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |             |

10.5.5 RMU\_LOCK - Configuration Lock Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |         |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---------|
| 0x010         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |         |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0x0000  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | RWH     |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | LOCKKEY |

| Bit  | Name     | Reset  | Access                     | Description                   |
|--|----------|--|----------------------------|-------------------------------|
| 31:16  | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |                            |                               |
| 15:0   | LOCKKEY  | 0x0000   | RWH                        | <b>Configuration Lock Key</b> |
| Write any other value than the unlock code to lock RMU_CTRL and RMU_RST from editing. Write the unlock code to unlock. When reading the register, bit 0 is set when the lock is enabled. |          |  |                            |                               |
| Mode   |          | Value  | Description                |                               |
| Read Operation   |          |  |                            |                               |
| UNLOCKED   |          | 0  | RMU registers are unlocked |                               |
| LOCKED   |          | 1  | RMU registers are locked   |                               |
| Write Operation  |          |  |                            |                               |
| LOCK   |          | 0  | Lock RMU registers         |                               |
| UNLOCK   |          | 0xE084   | Unlock RMU registers       |                               |

## 11. EMU - Energy Management Unit



### Quick Facts

#### What?

The EMU (Energy Management Unit) handles the different low energy modes in EFR32xG13 Wireless Gecko

#### Why?

The need for performance and peripheral functions varies over time in most applications. By efficiently scaling the available resources in real time to match the demands of the application, the energy consumption can be kept at a minimum.

#### How?

With a broad selection of energy modes, a high number of low-energy peripherals available even in EM2 Deep Sleep, and short wake-up time (3  $\mu$ s from EM2 Deep Sleep and EM3 Stop), applications can dynamically minimize energy consumption during program execution.

### 11.1 Introduction

The Energy Management Unit (EMU) manages all the low energy modes (EM) in EFR32xG13 Wireless Gecko. Each energy mode manages whether the CPU and the various peripherals are available. The energy modes range from EM0 Active to EM4 Shutoff. EM0 Active mode provides the highest amount of features, enabling the CPU, Radio, and peripherals with the highest clock frequency. EM4 Shutoff Mode provides the lowest power state, allowing the part to return to EM0 Active on a wake-up condition. The EMU also controls the various power routing configurations, internal regulators settings, and voltage monitoring needed for optimal power configuration and protection.

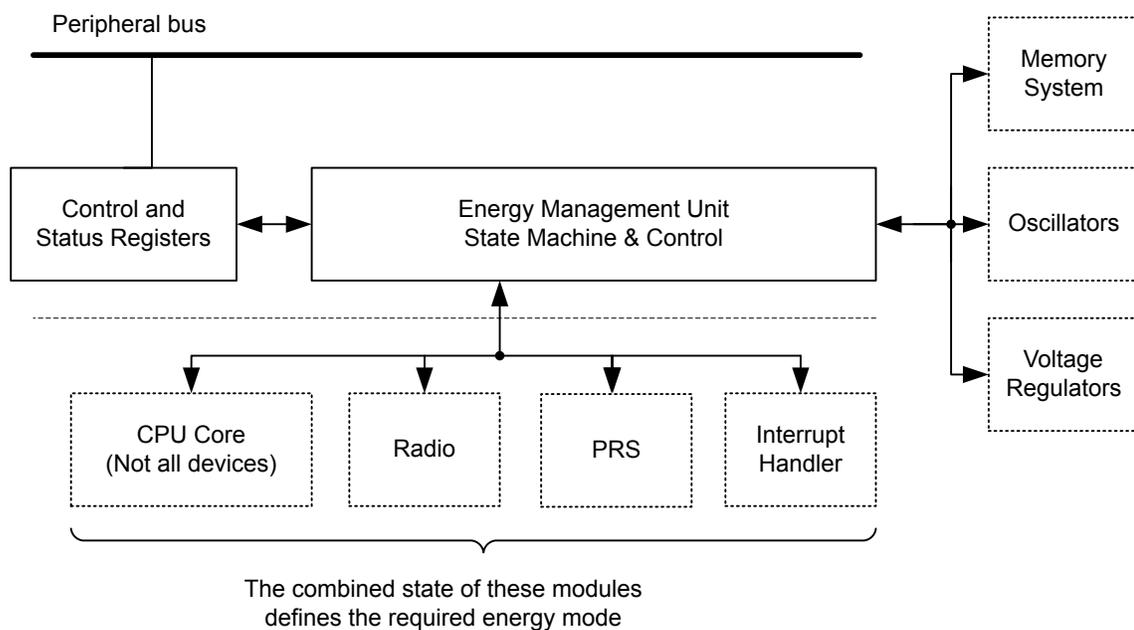
## 11.2 Features

The primary features of the EMU are listed below:

- Energy Modes control
  - Entry into EM4 Hibernate or EM4 Shutoff
  - Configuration of regulators and clocks for each Energy Mode
  - Configuration of various EM4 Hibernate/Shutoff wake-up conditions
  - Configuration of RAM power and retention settings
  - Configuration of GPIO retention settings
- Power routing configurations
  - DCDC control
  - Internal power switches allowing for extensible system power architecture
- Temperature measurement control and status
- Brown Out Detection
- Voltage Monitoring
  - Four dedicated continuous monitor channels
  - Optional monitor features include interrupt generation and low power mode wake-up
- State Retention
- Voltage Scaling
  - EM0/EM1 voltage scaling
  - EM2/EM3 voltage scaling
  - EM4H voltage scaling

### 11.3 Functional Description

The EMU is responsible for managing the wide range of energy modes available in EFR32xG13 Wireless Gecko. The block works in harmony with the entire platform to easily transition between energy modes in the most efficient manner possible. The following diagram [Figure 11.1 EMU Overview on page 251](#), shows the relative connectivity to the various blocks in the system.



**Figure 11.1. EMU Overview**

The EMU is available on the peripheral bus. The energy management state machine controls the internal voltage regulators, oscillators, memories, and interrupt system. Events, interrupts, and resets can trigger the energy management state machine to return to the active state. This is further described in the following sections.

The power architecture is highly configurable to meet system power performance needs. Several external power configurations are supported. The EMU allows flexible control of internal DCDC, Digital LDO Regulator, and internal power switching.

### 11.3.1 Energy Modes

EFR32xG13 Wireless Gecko features six main energy modes, referred to as Energy Mode 0 (EM0 Active) through Energy Mode 4 (EM4 Shutoff). The Cortex-M4 is only available for program execution in EM0 Active. In EM0 Active/EM1 Sleep any peripheral function can be enabled. EM2 Deep Sleep through EM4 Shutoff, also referred to as low energy modes, provide a significantly reduced energy consumption while still allowing a rich set of peripheral functionality. The following [Table 11.1 table on page 252](#) shows the possible transitions between different energy modes.

**Table 11.1. Energy Mode Transitions**

| Current Mode   | EM Transition Action |                                     |                                      |                                      |                     |                   |
|----------------|----------------------|-------------------------------------|--------------------------------------|--------------------------------------|---------------------|-------------------|
|                | Enter EM0 Active     | Enter EM1 Sleep                     | Enter EM2 Deep Sleep                 | Enter EM3 Stop                       | Enter EM4 Hibernate | Enter EM4 Shutoff |
| EM0 Active     |                      | Sleep (WFI, WFE)                    | Deep Sleep (WFI, WFE)                | Deep Sleep (WFI, WFE)                | EM4 Entry           | EM4 Entry         |
| EM1 Sleep      | IRQ                  |                                     | Peripheral wake up done <sup>1</sup> | Peripheral wake up done <sup>1</sup> |                     |                   |
| EM2 Deep Sleep | IRQ                  | Peripheral wake up req <sup>1</sup> |                                      |                                      |                     |                   |
| EM3 Stop       | IRQ                  | Peripheral wake up req <sup>1</sup> |                                      |                                      |                     |                   |
| EM4 Hibernate  | Wake Up              |                                     |                                      |                                      |                     |                   |
| EM4 Shutoff    | Wake Up              |                                     |                                      |                                      |                     |                   |

**Note:**  
1. Peripheral wake-up from EM2/3 to EM1 and then automatically back to EM2/3 when done.

The CSEN, LESENSE, ADC, RAC, and LEUART have the ability to temporarily wake up the part from either EM2 Deep Sleep or EM3 Stop to EM1 Sleep in order to transfer data. Once completed, the part is automatically placed back into the EM2 Deep Sleep or EM3 Stop mode.

The Core can always request to go to EM1 Sleep with the WFI or WFE command during EM0 Active. The core will be prevented from entering EM2 Deep Sleep or EM3 Stop if the RAC is transferring data or if Flash is programming or erasing.

An overview of supported energy modes and available functionality is shown in [Table 11.2 EMU Energy Mode Overview on page 252](#). For each energy mode, the system will typically default to its lowest power configuration, with non-essential clocks and peripherals disabled. Functionality may be then selectively enabled by software.

**Table 11.2. EMU Energy Mode Overview**

|                                       | EM0 Active/EM1 Sleep | EM2 Deep Sleep         | EM3 Stop               | EM4 Hibernate            | EM4 Shutoff              |
|---------------------------------------|----------------------|------------------------|------------------------|--------------------------|--------------------------|
| Wake-up time to EM0 Active/EM1 Sleep  | —                    | 3 $\mu$ s <sup>1</sup> | 3 $\mu$ s <sup>1</sup> | 160 $\mu$ s <sup>1</sup> | 160 $\mu$ s <sup>1</sup> |
| Core Active                           | Yes, in EM0 only     | —                      | —                      | —                        | —                        |
| Debug                                 | Available            | See Note <sup>2</sup>  | See Note <sup>2</sup>  | —                        | —                        |
| Digital logic and system RAM retained | Yes                  | Yes                    | Yes                    | —                        | —                        |
| Flash Memory Access                   | Available            | —                      | —                      | —                        | —                        |
| LDMA (Linked DMA Controller)          | Available            | Available <sup>3</sup> | Available <sup>3</sup> | —                        | —                        |
| RAC (Radio Controller)                | Available            | Available <sup>4</sup> | —                      | —                        | —                        |

|  | EM0 Active/EM1 Sleep | EM2 Deep Sleep            | EM3 Stop                  | EM4 Hiber-nate | EM4 Shutoff |
|--|----------------------|---------------------------|---------------------------|----------------|-------------|
| RFSENSE (Ultra Low Energy RF Detection)  | Available            | Available                 | Available                 | Available      | Available   |
| High Frequency Oscillators (HFRCO, HFXO) and Clocks (HFSRCLK, HFCLK, HFCORECLK, HFBUSCLK, HFPERCLK, HFRADIOCLK, HFCLKLE) | Available            | —                         | —                         | —              | —           |
| Auxiliary High Frequency Oscillator (AUXHFR-CO) and Clock (AUXCLK)   | Available            | Available <sup>5</sup>    | Available <sup>5</sup>    | —              | —           |
| Low Frequency Oscillators (LFRCO, LFXO)  | Available            | Available                 | —                         | Available      | Available   |
| Precision Low Frequency Oscillator (PLFRCO)  | Available            | Available                 | —                         | —              | —           |
| Low Energy Clocks A and B (LFACLK, LFBCLK)   | Available            | Available                 | Available <sup>7</sup>    | —              | —           |
| Low Energy Clock E (LFECLK)  | Available            | Available                 | Available <sup>7</sup>    | Available      | —           |
| ULFRCO (Ultra Low Frequency Oscillator)  | On                   | On                        | On                        | On             | Available   |
| CRYPTO (Crypto Accelerator)  | Available            | —                         | —                         | —              | —           |
| TRNG (True Random Number Generator)  | Available            | —                         | —                         | —              | —           |
| GPCRC (Cyclic Redundancy Check)  | Available            | —                         | —                         | —              | —           |
| RTCC (Real Time Counter and Calendar)  | Available            | Available                 | Available <sup>7</sup>    | Available      | —           |
| RTCC Memory Retained   | Yes                  | Yes                       | Yes                       | Yes            | —           |
| USART (USART/SPI)  | Available            | —                         | —                         | —              | —           |
| LEUART (Low Energy UART)   | Available            | Available <sup>3</sup>    | —                         | —              | —           |
| I <sup>2</sup> C   | Available            | Available <sup>6</sup>    | Available <sup>6</sup>    | —              | —           |
| TIMER (Timer/Counter)  | Available            | —                         | —                         | —              | —           |
| LETIMER (Low Energy Timer)   | Available            | Available                 | Available <sup>7</sup>    | —              | —           |
| CRYOTIMER (Ultra Low Energy Timer/Counter)   | Available            | Available                 | Available <sup>7</sup>    | Available      | Available   |
| WDOG (Watchdog)  | Available            | Available                 | Available <sup>7</sup>    | —              | —           |
| PCNT (Pulse Counter)   | Available            | Available                 | Available                 | —              | —           |
| CSEN (Capacitive Sense)  | Available            | Available <sup>3</sup>    | —                         | —              | —           |
| ACMP (Analog Comparator)   | Available            | Available <sup>8</sup>    | Available <sup>8</sup>    | —              | —           |
| ADC (Analog to Digital Converter)  | Available            | Available <sup>3, 5</sup> | Available <sup>3, 5</sup> | —              | —           |
| IDAC (Current Digital to Analog Converter)   | Available            | Available                 | Available                 | —              | —           |
| VDAC (Voltage Digital to Analog Converter)   | Available            | Available                 | Available                 | —              | —           |
| OPAMP (Operational Amplifier)  | Available            | Available                 | Available                 | —              | —           |
| LESENSE (Low Energy Sensor)  | Available            | Available <sup>3</sup>    | —                         | —              | —           |
| EMU Temperature Sensor   | Available            | Available                 | Available                 | Available      | —           |
| DC-DC Converter  | Available            | Available                 | Available                 | Available      | —           |
| VMON Wake-up or Reset  | Available            | Available                 | Available                 | Available      | —           |
| Brown-Out Detect/Power-on Reset  | Available            | Available                 | Available                 | Available      | Available   |
| Pin Reset  | Available            | Available                 | Available                 | Available      | Available   |

|                          | EM0 Active/EM1 Sleep | EM2 Deep Sleep | EM3 Stop  | EM4 Hiber-nate          | EM4 Shutoff             |
|--------------------------|----------------------|----------------|-----------|-------------------------|-------------------------|
| GPIO Pin Interrupts      | Available            | Available      | Available | Available <sup>9</sup>  | Available <sup>9</sup>  |
| GPIO Pin State Retention | Yes                  | Yes            | Yes       | Available <sup>10</sup> | Available <sup>10</sup> |

**Note:**

1. Approximate time. Refer to the data sheet
2. Leaving the debugger connected when in EM2 or EM3 will cause the system to enter a higher power EM2 mode in which the high frequency clocks are still enabled and certain core functionality is still powered-up in order to maintain debug-functionality.
3. The LDMA can be used with some low power peripherals (e.g., ADC, LEUART, LESENSE, CSEN) in EM2/3. Features required by the LDMA which are not supported in EM2/3 (e.g., HFCLK), will be automatically enabled prior to the LDMA transfer and then automatically disabled afterwards.
4. The RAC can be woken via a PRS interrupt to EM1 to transfer data. Once complete, the system will return to EM2.
5. While in EM2/3, an asynchronous event can be routed through PRS (e.g. GPIO IRQ or ACMP output) to wake up the ADC. Features required by the ADC which are not supported in EM2/3 (e.g., AUXHFRCO) will be automatically enabled to allow the ADC to convert a sample, and then automatically disabled afterwards.
6. I2C functionality limited to receive address recognition
7. Must be using ULFRCO
8. ACMP functionality in EM2/3 limited to edge interrupt
9. Pin wake-up in EM4 supported only on GPIO\_EM4WUx pins. Consult data sheet for complete list of pins.
10. If enabled in EMU->EM4CTRL.EM4IORETMODE.

The different energy modes are summarized in the following sections.

**11.3.1.1 EM0 Active**

EM0 Active provides all system features.

- Cortex-M4 is executing code
- Radio functionality is available
- High and low frequency clock trees are active
- All oscillators are available
- All peripheral functionality is available

**11.3.1.2 EM1 Sleep**

EM1 Sleep disables the core but leaves the remaining system fully available.

- Cortex-M4 is in sleep mode. Clocks to the core are off
- Radio functionality is available
- High and low frequency clock trees are active
- All oscillators are available
- All peripheral functionality is available

### 11.3.1.3 EM2 Deep Sleep

This is the first level into the low power energy modes. Most of the high frequency peripherals are disabled or have reduced functionality. Memory and registers retain their values.

- Cortex-M4 is in sleep mode. Clocks to the core are off.
- RFSense available. Radio inactive
- High frequency clock tree is inactive
- Low frequency clock tree is active
- The following oscillators are available
  - LFRCO, LFXO, ULFRCO, PLFRCO, AUXHFRCO (on demand, if used by the ADC)
- The following low frequency peripherals are available
  - RTCC, WDOG, LEUART, LETIMER, LESENSE, PCNT, CRYOTIMER
- The following analog peripherals are available (with potential limitations on functionality)
  - ADC, IDAC, VDAC, OPAMP, CSEN
- Wake-up to EM0 Active through
  - Peripheral interrupt, reset pin, power on reset, asynchronous pin interrupt, I2C address recognition, or ACMP edge interrupt
- Wake-up to EM1 Sleep through
  - RAC data transfer request
  - Part returns to EM2 Deep Sleep when transfers are complete
- RAM and register values are preserved
  - RAM blocks may be optionally powered down for lower power
- GPIO pin state is retained
- RTCC memory is retained
- The DC-DC converter can be configured to remain on in Low Power mode.

### 11.3.1.4 EM3 Stop

In this low energy mode, all low frequency oscillators (PLFRCO, LFXO, LFRCO) and all low frequency clocks derived from them, are stopped, as well as all high frequency clocks. Most peripherals are disabled or have reduced functionality. Memory and registers retain their values.

- Cortex-M4 is in sleep mode. Clocks to the core are off.
- RFSense available. Radio inactive
- High frequency clock tree is inactive
- All low frequency clock trees derived from the low frequency oscillators (PLFRCO, LFXO, LFRCO) are inactive
- The following oscillators are available
  - ULFRCO, AUXHFRCO (on demand, if used by the ADC)
- The following low frequency peripherals are available if clocked by the ULFRCO
  - RTCC, WDOG, CRYOTIMER
- The following analog peripherals are available (with potential limitations on functionality)
  - ADC, IDAC, VDAC, OPAMP, CSEN
- Wake-up to EM0 Active through
  - Peripheral interrupt, reset pin, power on reset, asynchronous pin interrupt, I2C address recognition, or ACMP edge interrupt
- Wake-up to EM1 Sleep through
  - RAC data transfer request
  - Part returns to EM3 Stop when transfers are complete
- RAM and register values are preserved
  - RAM blocks may be optionally powered down for lower power
- GPIO pin state is retained
- RTCC memory is retained
- The DC-DC converter can be configured to remain on in Low Power mode.

### 11.3.1.5 EM4 Hibernate

The majority of peripherals are shutoff to reduce leakage power. A few selected peripherals are available. System memory and registers do not retain values. GPIO PAD state and RTCC RAM are retained. Wake-up from EM4 Hibernate requires a reset to the system, returning it back to EM0 Active

- Cortex-M4 is off
- RFSENSE available. Radio is off.
- High frequency clock tree is off
- Some low frequency clock trees may be active
- The following oscillators are available
  - LFRCO, LFXO, ULFRCO
- The following low frequency peripherals are available
  - RTCC, CRYOTIMER
- Wake-up to EM0 Active through
  - VMON, EMU Temperature Sensor, RTCC, RFSENSE, CRYOTIMER, reset pin, power on reset, asynchronous pin interrupt (on GPIO\_EM4WUx pins only)
- GPIO pin state may be retained (depending on EMU->EM4CTRL.EM4IORETMODE configuration)
- RTCC memory is retained
- The DC-DC converter can be configured to remain on in Low Power mode.

### 11.3.1.6 EM4 Shutoff

EM4 Shutoff is the lowest energy mode of the part. There is no retention except for GPIO PAD state. Wake-up from EM4 Shutoff requires a reset to the system, returning it back to EM0 Active

- Cortex-M4 is off
- RFSENSE available. Radio is off.
- High frequency clock tree is off
- Low frequency clock tree may be active
- The following oscillators are available
  - LFRCO, LFXO, ULFRCO
- The following low frequency peripherals are available
  - CRYOTIMER
- Wake-up to EM0 Active through
  - RFSENSE, CRYOTIMER, reset pin, power on reset, asynchronous pin interrupt (on GPIO\_EM4WUx pins only)
- GPIO pin state may be retained (depending on EMU->EM4CTRL.EM4IORETMODE configuration)
- The DC-DC converter configuration is reset to its default Unconfigured configuration (DC-DC converter disabled and bypass switch is off)

## 11.3.2 Entering Low Energy Modes

The following sections describe the requirements for entering the various energy modes.

**Note:** If Voltage scaling is being used to save system energy, it is important to ensure the proper conditions for entry and exit of EM2 Deep Sleep, EM3 Stop or EM4 Hibernate be met. See [11.3.9.2.1 EM2/EM3 Voltage Scaling Guidelines](#) and [11.3.9.3.1 EM4H Voltage Scaling Guidelines](#) for details.

### 11.3.2.1 Entry Into EM1 Sleep

Energy mode EM1 Sleep is entered when the Cortex-M4 executes the Wait For Interrupt (WFI) or Wait For Event (WFE) instruction while the SLEEPDEEP bit the Cortex-M4 System Control Register is cleared. The MCU can re-enter sleep automatically out of an Interrupt Service Routine (ISR) if the SLEEPONEXIT bit in the Cortex-M4 System Control Register is set. Refer to ARM documentation on entering Sleep modes.

Alternately, EM1 Sleep can be entered from either EM2 Deep Sleep or EM3 Stop from a Peripheral Wake-up Request allowing transfers between the Peripheral and System RAM or Flash. On EFR32, ADC, CSEN, IDAC, LESENSE, and LEUART peripherals can request this wake-up event. Refer to their respective register specification to enable this option. The system will return back to EM2 Deep-Sleep or EM3 Stop once the ADC, CSEN, IDAC, LESENSE, or LEUART have completed its transfers and processing.

During Peripheral Wake-Up Request, additional system resources such as FLASH and other Peripherals can be enabled for access.

### 11.3.2.2 Entry Into EM2 Deep Sleep or EM3 Stop

Energy mode EM2 Deep Sleep or EM3 Stop may be entered when **all** of the following conditions are true:

- Radio RAC state machine is in OFF state
- IDAC is currently not updating output.
- Cortex-M4 (if present) is in DEEPSLEEP state
- Flash Program/Erase Inactive
- DMA done with all current requests
- A debugger is not currently connected.

Entry into EM2 Deep Sleep and EM3 Stop can be blocked by setting the EMU\_CTRL->EM2BLOCK bit.

**Note:** When EM2 Deep Sleep or EM3 Stop entry is blocked, the part is not able to enter a lower energy state. The core will be in a sleep state, similar to EM1, where it is waiting for a proper interrupt of other valid wake-up event. Once the blocking conditions are removed, then the part will automatically enter a lower energy state.

Energy mode EM2 Deep Sleep is entered from EM0 Active when the Cortex-M4 executes the Wait For Interrupt (WFI) or Wait For Event (WFE) instruction while the SLEEPDEEP bit in the Cortex-M4 System Control Register is set. The MCU can re-enter DeepSleep automatically out of an Interrupt Service Routine (ISR) if the SLEEPONEXIT bit in the Cortex-M4 System Control Register is set. Refer to ARM documentation on entering Sleep modes.

Alternately, EM2 Deep Sleep or EM3 Stop is entered from EM1 Sleep upon the completion of a Peripheral Wake-Up Request from the RAC if no EM0 Active wake-up happens in the meantime.

### 11.3.2.3 Entry Into EM4 Hibernate or EM4 Shutoff

Energy mode EM4 Hibernate and EM4 Shutoff is entered through register access.

Software must ensure no modules are active, such as RAC, when entering EM4 Hibernate/Shutoff. EM4CTRL->EM4STATE field must be configured to select either Hibernate (EM4H) or Shutoff (EM4S) mode prior to entering EM4.

Software may enter EM4 Hibernate/Shutoff from EM0 Active by writing the sequence 2,3,2,3,2,3,2,3,2 to EM4CTRL->EM4ENTRY bit field. If the EM4BLOCK bit in WDOGn\_CTRL is set, the CPU will be prevented from entering EM4 Hibernate/Shutoff by software request.

An active debugger connection will prevent entry into EM4 Hibernate/Shutoff.

Note that upon entry into EM4 Shutoff, the DC-DC converter configuration is reset to its default (i.e. Unconfigured) configuration. In the Unconfigured configuration, the DC-DC converter will be disabled and the bypass switch will be turned off.

### 11.3.3 Exiting a Low Energy Mode

A system in EM2 Deep Sleep and EM3 Stop can be woken up to EM0 Active through regular interrupt requests from active peripherals. Since state and RAM retention is available, the EFR32 is fully restored and can continue to operate as before it went into the Low Energy Mode.

Wake-Up from EM4 Hibernate or EM4 Shutoff is performed through reset. Wake-Up from a specific module must be enabled in that module's EM4WUEN register.

Enabled interrupts that can cause wake-up from a low energy mode are shown in [Table 11.3 EMU Wake-Up Triggers from Low Energy Modes on page 258](#). The wake-up triggers always return the EFR32 to EM0 Active/EM1 Sleep. Additionally, any reset source will return to EM0 Active. VMON-based EM4 Hibernate wake-ups also set the corresponding rise or fall interrupt flag. These flags serve as the wake-up source for EM4 Hibernate and must be cleared by software on EM4 Hibernate exit. Not doing so will result in an immediate wake-up after next EM4 Hibernate entry.

**Table 11.3. EMU Wake-Up Triggers from Low Energy Modes**

| Peripheral               | Wake-Up Trigger  | EM2 Deep Sleep | EM3 Stop         | EM4 Hibernate       | EM4 Shutoff         |
|--------------------------|--|----------------|------------------|---------------------|---------------------|
| LEUART (Low Energy UART) | Receive / transmit   | Yes            | —                | —                   | —                   |
| LETIMER                  | Any enabled interrupt  | Yes            | —                | —                   | —                   |
| WDOG                     | Any enabled interrupt  | Yes            | Yes              | —                   | —                   |
| LESENSE                  | Any enabled interrupt  | Yes            | —                | —                   | —                   |
| LFXO                     | Ready Interrupt  | Yes            | —                | —                   | —                   |
| LFRCO                    | Ready Interrupt  | Yes            | —                | —                   | —                   |
| I <sup>2</sup> C         | Receive address recognition  | Yes            | Yes              | —                   | —                   |
| ACMP                     | Any enabled edge interrupt   | Yes            | Yes              | —                   | —                   |
| ADC                      | SINGLE / SCAN FIFO events, window comparator, and VREF overvoltage | Yes            | Yes              | —                   | —                   |
| CSEN                     | Wake on threshold  | Yes            | Yes              | —                   | —                   |
| VDAC                     | Any enabled interrupt except EM23ERRIF                             | Yes            | Yes              | —                   | —                   |
| PCNT                     | Any enabled interrupt  | Yes            | Yes <sup>1</sup> | —                   | —                   |
| RTCC                     | Any enabled interrupt  | Yes            | Yes              | Yes <sup>2</sup>    |                     |
| VMON                     | Rising or falling edge on any monitored power                      | Yes            | Yes              | Yes <sup>2</sup>    | —                   |
| EMU Temperature Sensor   | Measured temperature outside the defined limits                    | Yes            | Yes              | Yes <sup>2</sup>    | —                   |
| CRYOTIMER                | Timeout  | Yes            | Yes              | Yes <sup>2</sup>    | Yes <sup>2</sup>    |
| Pin Interrupts           | Transition   | Yes            | Yes              | Yes <sup>2, 3</sup> | Yes <sup>2, 3</sup> |
| RFSENSE                  | RF signal detected   | Yes            | Yes              | Yes <sup>2</sup>    | Yes <sup>2</sup>    |
| Reset Pin                | Assertion  | Yes            | Yes              | Yes                 | Yes                 |
| Power                    | Cycle Off/On   | Yes            | Yes              | Yes                 | Yes                 |

**Note:**

1. When using an external clock
2. Corresponding bit in the module's EM4WUEN must be set.
3. Only available on a subset of the pins. Refer to the data sheet for details.

### 11.3.4 Power Configurations

The EFR32xG13 Wireless Gecko allows several power configurations with additional options giving flexible power architecture selection.

In order to provide the lowest power consuming radio solutions, the EFR32xG13 Wireless Gecko comes with a DC-DC module to power internal circuits. The DC-DC requires an external inductor and capacitor (refer to the data sheet for recommended values).

The EFR32xG13 Wireless Gecko has multiple internal power domains: IO Supply (IOVDD), Analog & Flash (AVDD), RF Analog Supply (RFVDD), RF Power Amplifier Supply (PAVDD), Input to Digital LDO (DVDD), and Low Voltage Digital Supply (DECOUPLE). Additional detail for each configuration and option is given in the following sections.

When assigning supply sources, the following requirement must be adhered to:

- VREGVDD = AVDD (Must be the highest voltage in the system)
- VREGVDD >= DVDD
- VREGVDD >= PAVDD
- VREGVDD >= RFVDD
- VREGVDD >= IOVDD

### 11.3.4.1 Power Configuration 0: Unconfigured

Upon power-on reset (POR) or entry into EM4 Shutoff, the system is configured in a safe state that supports all of the available Power Configurations. The Unconfigured Configuration is shown in the simplified diagram below.

In the Unconfigured Configuration:

- The DC-DC converter's Bypass switch is OFF.
- The internal digital LDO is powered from the AVDD pin (i.e. REGPWRSEL=0 in EMU\_PWRCTRL). Note the maximum allowable current into the LDO when REGPWRSEL=0 is 20 mA. For this reason, immediately after startup firmware should configure REGPWRSEL=1 to power the digital LDO from DVDD.
- The analog blocks are powered from the AVDD supply pin (i.e., ANASW=0 in EMU\_PWRCTRL).

After power on, firmware can configure the device based on the external hardware configuration. Note that the PWRCFG register can only be written once to a valid value and is then locked. This should be done immediately out of boot to select the proper power configuration. The DC-DC and PWRCTRL registers will be locked until the PWRCFG register is configured.

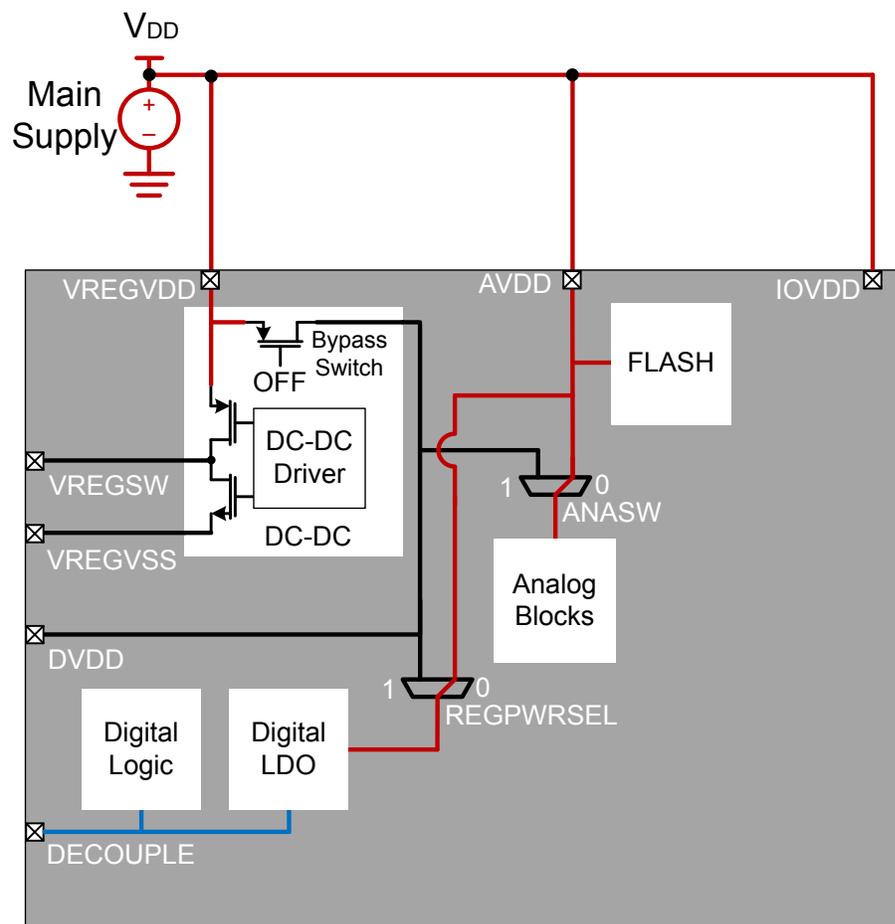


Figure 11.2. Unconfigured Power Configuration

### 11.3.4.2 Power Configuration 1: No DC-DC

In Power Configuration 1, the DC-DC converter is programmed in Off mode and the Bypass switch is Off. The DVDD pin must be powered externally - typically, DVDD is connected to the main supply. DVDD powers the internal Digital LDO (i.e., REGPWRSEL=1) which powers the digital circuits. IOVDD and AVDD are powered from the main supply as well. RFVDD and PAVDD, which power the radio, are shorted to the main supply as well.

VREGSW must be left disconnected in this configuration.

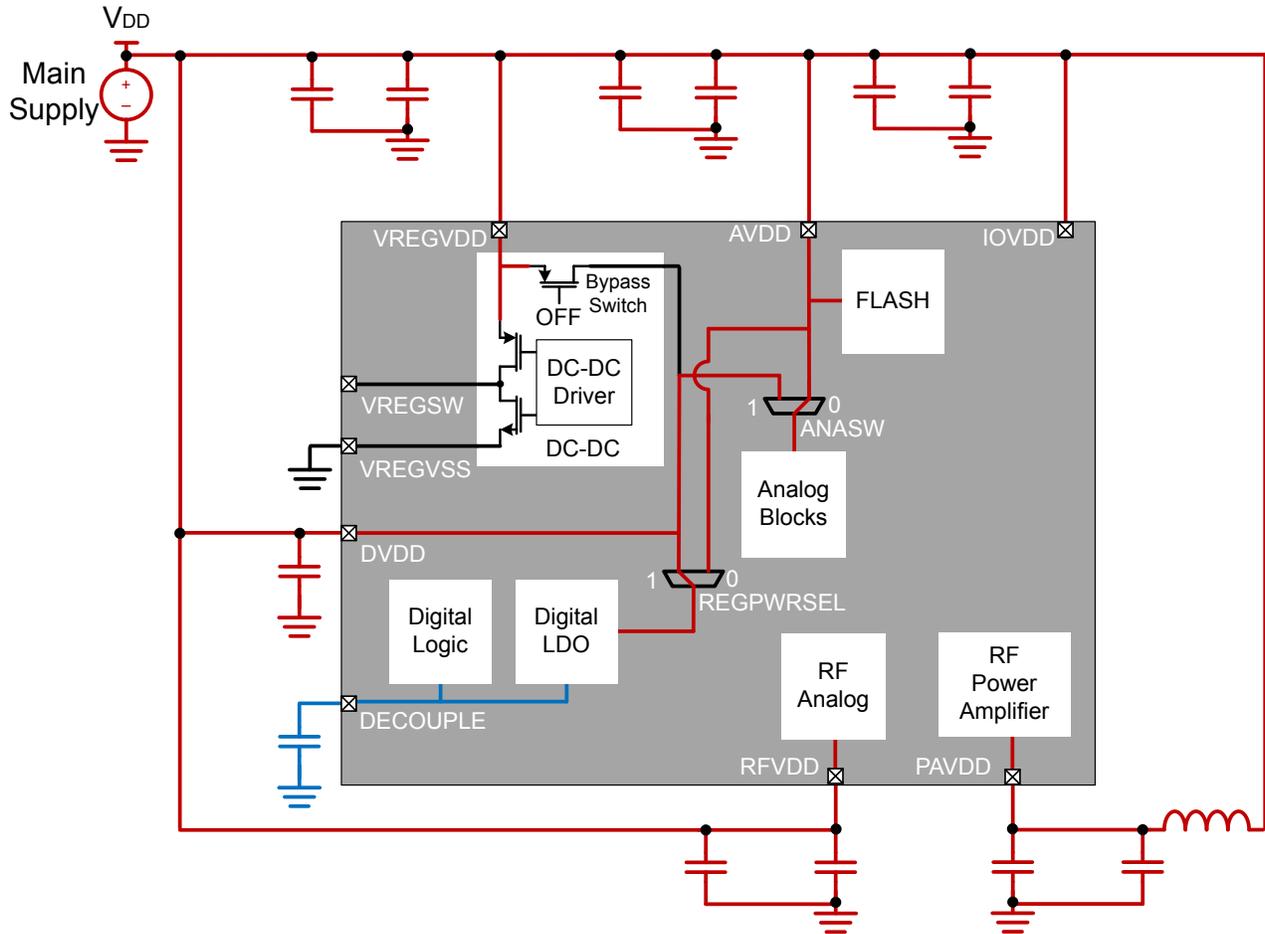


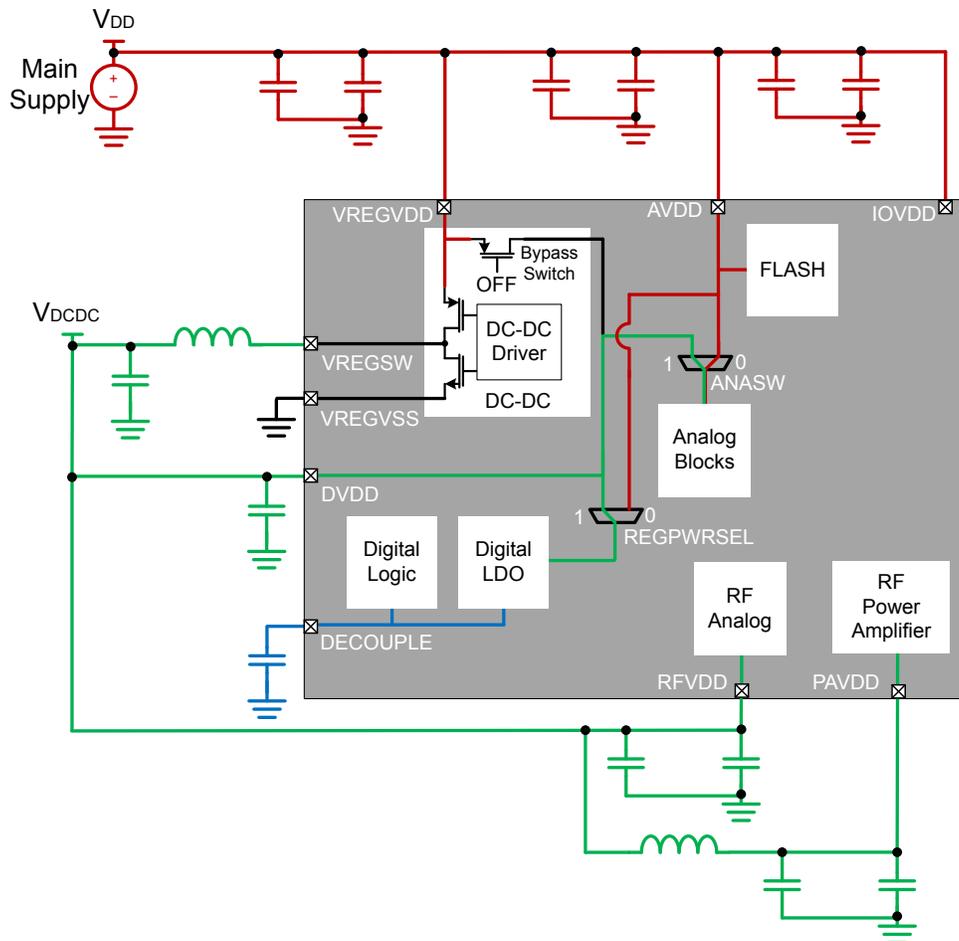
Figure 11.3. DC-DC Off Power Configuration

### 11.3.4.3 Power Configuration 2: DC-DC

For the lowest power applications, the DC-DC converter can be used to power the DVDD supply, as well as RFVDD and PAVDD.

In Power Configuration 2, the DC-DC Output ( $V_{DCDC}$ ) is connected to DVDD. DVDD powers the internal Digital LDO (i.e.,  $REGPWRSEL=1$ ) which powers the digital circuits. AVDD is connected to the main supply voltage. The internal analog blocks may be powered from AVDD or DVDD, depending on the ANASW configuration. RFVDD and PAVDD are powered from  $V_{DCDC}$  as well.

IOVDD could be connected to either the main supply (as shown below) or to  $V_{DCDC}$ , depending on the system IO requirements. Because  $V_{DCDC}$  will be unpowered (i.e., floating) at startup, if IOVDD is powered from the DC-DC converter then any circuit attached to IOVDD will not be powered until the DC-DC is configured (or the bypass switch is enabled). Refer to [11.3.8 IOVDD Connection](#) section for further details and issues that may result when connecting IOVDD to  $V_{DCDC}$ .



**Figure 11.4. DC-DC Standard Power Configuration**

As the Main Supply voltage approaches the DC-DC output voltage, it eventually reaches a point where becomes inefficient (or impossible) for the DC-DC module to regulate  $V_{DCDC}$ . At this point, firmware can enable bypass mode, which effectively disables the DC-DC and shorts the Main Supply voltage directly to the DC-DC output. If and when sufficient voltage margin on the Main Supply returns, the system can be switched back into DC-DC regulation mode.

An alternate "High RF Power" DC-DC configuration has the external Main Supply connected directly to the PAVDD. This configuration supports a higher transmit power (e.g., >13 dBm) required for some radio protocol specifications. No additional software setting is required for this mode. The following diagram shows an example of connecting PAVDD to the Main Supply while DVDD and RFVDD are connected to the filtered  $V_{DCDC}$ .



### 11.3.5.1 Bypass Mode

In Bypass mode, the VREGVDD input voltage is directly shorted to the DC-DC converter output through an internal switch. Consult the data sheet for the Bypass switch impedance specification.

The Bypass Current Limit limits the maximum current drawn from the input supply in Bypass mode. This current limit is enabled by setting the BYPLIMEN bit in the EMU\_DCDCCLIMCTRL register, and the limit value may be adjusted between 20 mA and 320 mA using the BYPLIMSEL bitfield in the EMU\_DCDCMISCCTRL register. When the difference between the DC-DC output voltage ( $V_{DCDC}$ ) and the DC-DC input voltage (VREGVDD) is large, applications should enable the Bypass Current Limit before enabling Bypass mode. For example, if Bypass mode is enabled with VREGVDD=3.8 V and  $V_{DCDC}$ =1.8 V with a 4.7  $\mu$ F capacitor, the peak current draw may be quite large as it is limited only by the bypass switch on-resistance, which could result in drooping on the input supply voltage. For smaller input / output voltage differences (e.g., VREGVDD=2.4 V and  $V_{DCDC}$ =1.8 V), it may not be necessary to enable the Bypass Current Limit at all.

Note that the device will see an additional  $\sim 10$   $\mu$ A of current draw when both the Bypass Current Limiter and Bypass Mode are enabled. Applications should therefore disable the Bypass Current Limiter (i.e., set BYPLIMEN = 0) after the DVDD voltage has reached the main supply voltage in Bypass Mode.

### 11.3.5.2 Low Power (LP) Mode

The Low Power (LP) controller operates in a hysteretic mode to keep the output voltage within a defined voltage band. Once the DC-DC output voltage drops below a programmable internal reference, the LP controller generates a pulse train to control the powertrain PFET switch, which charges up the DC-DC output capacitor. When the output voltage is at the programmed upper level, the powertrain PFET is turned off. The output ripple voltage may be quite large (>100 mV) in LP mode.

The LP controller supports load currents up to approximately 10 mA, making it suitable for light loads in EM0 and EM1, as well as EM2, EM3, or EM4 low energy modes.

### 11.3.5.3 Low Noise (LN) Mode

The Low Noise (LN) controller continuously switches the powertrain NFET and PFET switches to maintain a constant programmed voltage at the DVDD pin. The LN controller supports load current from sub-mA up to 200 mA.

The LN controller switching frequency is programmable using the RCOBAND bitfield in the EMU\_DCDCCLNFREQCTRL register. See below for recommended RCOBAND settings for each mode.

The DC-DC Low Noise controller operates in one of two modes:

1. Continuous Conduction Mode (CCM)
2. Discontinuous Conduction Mode (DCM)

#### 11.3.5.3.1 Low Noise (LN) Continuous Conduction Mode (CCM)

CCM operation is configured by setting the LNFORCECCM bit in the EMU\_DCDCMISCCTRL register. CCM can be used to improve the DC-DC converter's output transient response time to quick load current changes, which minimizes voltage transients on the DC-DC output.

Note that all references to CCM in the documentation actually refer to Forced Continuous Conduction Mode (FCCM) - that is, if the LNFORCECCM bit is set and the output load current is very low, the DC-DC will be forced to operate in CCM. In this case, the current through the inductor may be negative and current may flow back into the battery.

CCM is required for radio or Wireless Gecko systems because, unlike DCM, it allows use of the radio's interference minimization features. In CCM, the recommended DC-DC converter switching frequency is 6.4 MHz (RCOBAND = 4). Note that when the radio's interference minimization features are enabled, RCOBAND = 4 corresponds to a DC-DC converter switching frequency of 7 MHz.

### 11.3.5.3.2 Low Noise (LN) Discontinuous Conduction Mode (DCM)

To enable DCM, the LNFORCECCM bit in EMU\_DCDCMISCCTRL must be cleared before entering LN. Typically, this configuration would occur while the part was in Bypass mode. Once DCM is enabled, the DC-DC should operate in DCM at light load currents. However, as the load current increases, the DC-DC will automatically transition into CCM without software intervention.

The advantage of DCM is improved efficiency for light load currents. However, in DCM the DC-DC has poorer dynamic response to changes in load current, leading to potentially larger changes in the regulated output voltage. In addition, DCM increases the potential RF switching interference, because in DCM the DC-DC switching events are load dependent and can no longer be synchronized with radio operation. For these reasons, DCM is not recommended for radio applications or for non-radio applications that expect large instantaneous load current steps. For example, if the DC-DC is in DCM, firmware may need to increment the core clock frequency in small steps to prevent a large sudden load increase.

In DCM, the recommended DC-DC converter switching frequency is 3 MHz (RCOBAND = 0).

### 11.3.5.4 DC-to-DC Programming Guidelines

**Note:** Refer to Application Note *AN0948: EFM32 and EFR32 Series 1 Power Configurations and DC-DC* for detailed information on programming the DC-DC. Application Notes can be found on the Silicon Labs website ([www.silabs.com/32bit-appnotes](http://www.silabs.com/32bit-appnotes)) or using the [Application Notes] tile in Simplicity Studio.

### 11.3.6 Analog Peripheral Power Selection

The analog peripherals (e.g., ULFRCO, LFRCO, LFXO, HFRCO, AUXHFRCO, VMON, IDAC, ADC, CSEN) are powered from an internal analog supply domain, VDDX\_ANA. VDDX\_ANA may be supplied from either the AVDD or DVDD supply pins, depending on the configuration of the ANASW bit in the EMU\_PWRCTRL register. Changes to the ANASW setting should be made immediately out of reset (i.e., in the Unconfigured Configuration), before all clocks (with the exception of HFRCO and ULFRCO) are enabled. If the DCDC converter is used and ANASW is set to 1, the switch will not take effect until after the DCDC output voltage has reached its target level. To prevent supply transients, firmware should configure and enable the DCDC, configure ANASW, and then enable clocks. If the DCDC converter is not used, IMMEDIATEPWRSWITCH should be set prior to setting ANASW so hardware can immediately apply the switch without waiting for the DCDC to settle.

Once ANASW is configured it should not be changed. Note that the flash is always powered from the AVDD pin, regardless of the state of the ANASW bit.

**Table 11.4. Analog Peripheral Power Configuration**

| ANASW       | Analog Peripheral Power Supply Source (VDDX_ANA) | Comments  |
|-------------|--|---|
| 0 (default) | AVDD pin   | This configuration may provide a quieter supply to the analog modules, but is less efficient as AVDD is typically at a higher voltage than DVDD.  |
| 1           | DVDD pin   | This configuration may provide a noisier supply to the analog modules, but is more efficient. However, because the maximum allowable input voltage to many of the analog modules using APORT is limited to MIN(VDDX_ANA, IOVDD), this setting could artificially limit your analog input range. |

### 11.3.7 Digital LDO Power Selection

The digital LDO may be powered from one of two supply pins, depending on the configuration of the REGPWRSEL bit in the EMU\_PWRCTRL register. At startup, the digital is powered from the AVDD pin. When powered from AVDD, the LDO current is limited to 20 mA. Out of startup, firmware should configure and enable the DCDC (if desired) and then set REGPWRSEL=1 before increasing the core clock frequency.

**Table 11.5. Digital LDO Power Configuration**

| REGPWRSEL   | Digital LDO Power Source | Comments  |
|-------------|--------------------------|---|
| 0 (default) | AVDD pin                 | Maximum LDO current in this configuration is 20 mA. Firmware should configure REGPWRSEL to 1 after startup. |
| 1           | DVDD pin                 | This configuration supports all core frequencies, and should be used after startup.                         |

### 11.3.8 IOVDD Connection

The IOVDD supply(s) must be less than or equal to AVDD. IOVDD will typically be connected to either the DC-DC Output ( $V_{DCDC}$ ) or the main supply.

Because  $V_{DCDC}$  will be unpowered (i.e., floating) at startup, if IOVDD is powered from the DC-DC converter then any circuit attached to IOVDD will not be powered until the DC-DC is configured (or the bypass switch is enabled).

**Note:** This constraint can have serious and unintended side-effects. For example, if  $IOVDD=V_{DCDC}$ :

1. It isn't directly possible to program an unprogrammed device on a PCB through the serial wire interface. Programming the device requires IOVDD to be present (i.e., for SWCLK, SWDIO, etc), and IOVDD won't be present until after the part is programmed (i.e., the DC-DC is enabled in firmware to power up  $V_{DCDC}$ ). It is possible to work around this issue, however, by providing an external supply for  $V_{DCDC}$  during programming.
2. Some unprogrammed devices are preloaded with a bootloader. The bootloader is expecting to read a logic high on the SWCLK pin to determine if the bootloader should execute. With no valid IOVDD voltage present, the code may incorrectly decide to execute the bootloader, which will cause the system to wait in the bootloader until a reset occurs.

Additionally, upon entry into EM4 Shutoff, the DC-DC converter configuration is reset to its default (Unconfigured) configuration. If  $IOVDD = V_{DCDC}$ , then any circuits attached to IOVDD will remain unpowered until the system is reset to exit EM4 Shutoff, and the DC-DC is configured (or the bypass switch is enabled).

Any application with powering external loads from the DC-DC converter must take into consideration the maximum allowable DC-DC load current. Refer to the data sheet for DC-DC load current specification.

### 11.3.9 Voltage Scaling

The voltage scaling feature allows for a tradeoff between power and performance. Voltage scaling applies an adjustment to the supply voltage for the on-chip digital logic and memories. For EM0 and EM1 operation, full device performance is supported when the Voltage Scale Level is set to its highest value. The Voltage Scale Level may be set lower when operating the system at slower clock speeds to save power. Voltage scaling does not affect the input or output range for analog peripherals or digital I/O logic levels. For more information about max system frequency supported for different voltage scaling levels. Refer to the CMU chapter and the data sheet specification tables.

**Note:** Some device sub-systems and operations are only supported at Voltage Scale Level 2.

- Flash write/erase is only supported at Voltage Scale Level 2.
- TRNG operation is only supported at Voltage Scale Level 2.
- HFXO supports only 38-40 MHz crystals and is only supported at Voltage Scale Level 2.
- Radio operation and radio module register access is only supported at Voltage Scale Level 2. When using any other Voltage Scale Level access to all radio peripherals is locked out. Thus, firmware may only use Voltage Scale Level 0 during periods when radio operations or radio register accesses are not required.

Separate voltage scaling controls are available for the different energy modes. These are as follows:

- EM0/EM1 Voltage Scaling
- EM2/EM3 Voltage Scaling
- EM4H Voltage Scaling

#### 11.3.9.1 EM0/EM1 Voltage Scaling

In energy modes EM0 and EM1, the user can dynamically scale voltages between Voltage Scale Level 2 and Voltage Scale Level 0 using the EM01VSCALE2 and EM01VSCALE0 bitfields in EMU\_CMD register. A lower Voltage Scale Level can be used in conjunction with lower processor frequency to reduce power consumption. Once these commands are issued, hardware begins the process of voltage scaling and when done, the VSCALEDONE interrupt is triggered. Users can also poll VSCALEBUSY in EMU\_STATUS which indicates that hardware is busy changing the voltage scale setting when set. VSCALE in EMU\_STATUS shows the current voltage the system is in at any time.

**Note:**

- If more than one voltage scaling command is issued in EMU\_CMD simultaneously, the lower voltage scaling level has higher priority. e.g. priority order: EM01VSCALE0 > EM01VSCALE2.
- The reset value of VSCALE for EM0 and EM1 operation is Voltage Scale Level 2.

When voltage scaling up or down, the user should follow the following sequences in order to ensure proper scaling.

- Voltage Scale Down
  1. Decrease system clock frequency to the target frequency
  2. Update the wait states of Flash for the target frequency
  3. Issue voltage scaling command by setting EM01VSCALE2 or EM01VSCALE0 in EMU\_CMD
  4. Once Hardware completes voltage scaling up, VSCALEDONE interrupt is set.
- Voltage Scale Up
  1. Issue voltage scaling command by setting EM01VSCALE2 or EM01VSCALE0 in EMU\_CMD
  2. Wait for hardware to complete voltage scaling. When done, VSCALEDONE interrupt is set.
  3. Update the wait states of Flash for the target frequency
  4. Increase system clock frequency to the target frequency

Multiple voltage scaling commands are allowed to be issued even when the current voltage scaling is not yet completed. In such a case, the current scaling will be aborted and the last command will be executed. VSCALEDONE interrupt will be issued for every voltage scaling command.

**Note:** When a hard reset occurs, VSCALE will be set to the reset value (Voltage Scale Level 2). In most cases, a soft reset will not affect the current VSCALE level. However, when a soft reset is issued in the middle of the voltage scaling process, the minimum voltage scale level indicated by VSCALE or the EMU\_CMD which triggered the voltage scale operation will be applied and reflected in VSCALE.

### 11.3.9.2 EM2/EM3 Voltage Scaling

The EM23VSCALE bitfield in EMU\_CTRL allows user to independently setup the voltage scaling value for EM2/EM3 energy mode. The EM23VSCALE in EMU\_CTRL should be programmed to a level which is less than or equal to VSCALE in EMU\_STATUS. This means that EM2/EM3 voltage scaling is always a voltage scaling down process. If EM23VSCALE level in EMU\_CTRL is greater than VSCALE level in EMU\_STATUS, the VSCALE level will be implemented in EM2/EM3 instead of EM23VSCALE. Upon EM2/EM3 entry, the system will scale down the voltage to a smaller level between VSCALE or EM23VSCALE.

**Note:** The reset value of EM23VSCALE is Voltage Scale Level 2. Therefore, if user scales EM0/EM1 voltage to Voltage Scale Level 0 (reflected in VSCALE in EMU\_STATUS) and enters EM2/EM3, this VSCALE voltage of Voltage Scale Level 0 is maintained in EM2/EM3 as well since this is smaller level between VSCALE and EM23VSCALE.

#### 11.3.9.2.1 EM2/EM3 Voltage Scaling Guidelines

Note that when using EM23VSCALE in EMU\_CTRL to scale down EM2/EM3, the scaled down voltage in EM2/EM3 is maintained after waking from EM2/EM3 to EM0/EM1. For example, if VSCALE was at Voltage Scale Level 2 prior to EM2/EM3 entry, and EM23VSCALE was set to Voltage Scale Level 0, the system will scale down to Voltage Scale Level 0 on EM2/EM3 entry. When waking up to EM0/EM1, the system maintains its voltage at Voltage Scale Level 0. Therefore, user must ensure the system clock frequency and Flash wait states are programmed to correct values to support waking up to EM0/EM1 at the lower voltages prior to EM2/EM3 entry.

EM23VSCALEAUTOWSEN bitfield in EMU\_CTRL enables hardware to automatically configure the system clock frequency and Flash wait states to support low voltage operation when waking up to EM0/EM1 from EM2/EM3. Therefore, this obviates the need for user to setup the clock frequency and Flash wait states prior to EM2/EM3 entry with EM23VSCALE. When waking up to EM0/EM1, while using EM23VSCALEAUTOWSEN set to 1, the HFRCO will default to its production calibrated 19 MHz frequency.

### 11.3.9.3 EM4H Voltage Scaling

EM4HVSCALE bitfield in EMU\_CTRL allows user to independently setup the voltage scaling levels for EM4H energy mode. The EM4HVSCALE in EMU\_CTRL should be programmed to a level which is smaller than or equal to VSCALE level in EMU\_STATUS or EM23VSCALE in EMU\_CTRL. This means that EM4H voltage scaling is always a voltage scaling down process. If EM4HVSCALE level in EMU\_CTRL is greater than level of VSCALE in EMU\_STATUS or level of EM23VSCALE in EMU\_CTRL, the smaller of VSCALE, EM23VSCALE or EM4HVSCALE levels will be implemented in EM4H.

**Note:** The reset level of EM4HVSCALE is Voltage Scale Level 2. Therefore, if user scales EM0/EM1 voltage to Voltage Scale Level 0 (reflected in VSCALE in EMU\_STATUS) and enters EM4H, this VSCALE voltage of Voltage Scale Level 0 is maintained in EM2/EM3 as well since this is minimum of VSCALE and EM23VSCALE.

#### 11.3.9.3.1 EM4H Voltage Scaling Guidelines

Note that when using EM4HVSCALE in EMU\_CTRL to scale down voltage in EM4H, the scaled down voltage in EM4H is maintained after waking from EM4H to EM0/EM1. For example prior to EM4H entry, if VSCALE was at Voltage Scale Level 2 and EM4HVSCALE was set to Voltage Scale Level 0, the system will scale down to Voltage Scale Level 0 on EM4H entry. When waking up to EM0/EM1, the system maintains its voltage at Voltage Scale Level 0.

### 11.3.9.4 Voltage Scaling Recommended Use

Refer to the data sheet for the maximum supported system frequencies for different Voltage Scaling Levels. Use of the lowest voltage scaling level is recommended for maximum power savings. For any voltage scaling level, it is recommend to use the highest frequency for performance benefits.

Voltage can then be scaled to higher voltage scale levels only when higher system clock frequency is required by the application for a period of time after which user can dynamically scale the voltage back to lower voltage scale levels to continue saving power.

### 11.3.10 EM2/EM3 Peripheral Retention Disable

Peripherals that are available in EM2 Deep Sleep or EM3 Stop can optionally be powered down during EM2 Deep Sleep or EM3 Stop. This allows lower energy consumption in these energy modes. However, when powering down, these peripherals are independently reset so the registers lose their configuration values. Therefore, they will have to be reconfigured upon wake-up to EM0 Active if they were previously configured to non reset values.

EMU\_EM23PERNORETAINCTRL register can be used to setup unused peripherals for powering down prior to EM2/EM3 entry. Once setup, upon EM2/EM3 entry, all peripherals in the power-down domain will get powered down if all of them are setup to be disabled.

**Note:** User must ensure that the peripherals being powered down should have their clocks disabled in CMU prior to EM2/EM3 entry.

On waking up from EM2/EM3, EMU\_EM23PERNORETAINSTATUS register indicates if the peripherals were powered down by the system and subsequently locked out from register access. Locking out peripherals prevents users from accidentally using peripherals with configurations at their reset state. EMU\_EM23PERNORETAINCMD allows user to unlock these peripherals and hence grant access to their registers for updating their configurations.

#### 11.3.11 Brown Out Detector (BOD)

The EFR32xG13 Wireless Gecko contains multiple supply brown out detectors (BODs).

##### 11.3.11.1 AVDD BOD

The EFR32xG13 Wireless Gecko has a fast response BOD on AVDD that is always active. This BOD ensures the minimal supply is provided to the AVDD supply (typically also connected to VREGVDD). Once triggered, the BOD will cause the system to reset.

**Note:** In EM4 Hibernate/Shutoff a low power version of the AVDD BOD, called EM4BOD, is available to trigger a reset at level lower than in other energy modes. All other BODs are disabled during EM4 Hibernate/Shutoff

##### 11.3.11.2 DVDD and DECOUPLE BOD

Additional BODs will monitor DVDD and DECOUPLE during EM0 Active through EM3 Stop. This can cause a reset to the internal logic, but will not cause a power-on reset or reset the EMU or RTCC.

### 11.3.12 Voltage Monitor (VMON)

The EFR32 features an extremely low energy Voltage Monitor (VMON) capable of running down to EM4 Hibernate. Trigger points are preloaded but may be reconfigured.

- AVDD X 2
- DVDD
- IOVDD0

**Table 11.6. VMON Events**

| Feature                                      | Condition    | AVDD | DVDD | IOVDD |
|--|--------------|------|------|-------|
| Hysteresis (separate rise and fall triggers) | —            | Yes  | —    | —     |
| Interrupt                                    | Fall or Rise | Yes  | Yes  | Yes   |
| Wake-Up from EM4 Hibernate                   | Fall or Rise | Yes  | Yes  | Yes   |

The status of the VMON is reflected in the EMU\_STATUS register.

The status of the sticky interrupt can be found at EMU\_IF. These interrupt flags also serve as the wake-up source of EM4H when the associated RISEWU and FALLWU bits are set. This means that if these flags are set, EM4H entry will result in an immediate wake-up. To prevent this, these must be cleared by software before EM4H entry.

Note that the VMON has offset high hysteresis, specified in the device Data Sheet. For rising edge detection the threshold will be the threshold setting (as described below) +  $V_{VMON\_HST}$ , and for falling edge detection the threshold will simply be the threshold setting.

VMON channels are calibrated at two voltages: 1.86 V and 2.98 V. The calibration results (coarse thresholds and fine thresholds for 1.86 V and 2.98 V) are placed in the VMONCAL registers in the DI page. Using these thresholds it is possible to calculate thresholds for the entire supported VMON VDD range, i.e., 1.62 V to 3.4 V. Using the values given in VMONCAL registers, one can calculate  $T_{1.86}$ ,  $T_{2.98}$ ,  $V_a$  and  $V_b$ .

$$T_{1.86} = (10 \times VMONCALX\_XVDD1V86THRESCOARSE) + VMONCALX\_XVDD1V86THRESFINE,$$

$$T_{2.98} = (10 \times VMONCALX\_XVDD2V98THRESCOARSE) + VMONCALX\_XVDD2V98THRESFINE,$$

$$V_a = (1.12) / (T_{2.98} - T_{1.86}),$$

$$V_b = 1.86 - (V_a \times T_{1.86}),$$

**Figure 11.6. VMON Calibration Equations**

Now if it is required to find the coarse and fine thresholds for a certain voltage Y, following equation can be used:

$$Thres_Y = (Y - V_b) / V_a,$$

$$Y_{calib} = (Thres_Y \times V_a) + V_b,$$

**Figure 11.7. VMON Threshold Equations**

$Thres_Y$  should be rounded to the nearest integer. The least significant digit of the rounded  $Thres_Y$  gives the fine threshold and remaining digits give the coarse threshold for Y. These can now be programmed in the relevant EMU\_VMONXVDDCTRL register as the coarse and fine thresholds. It may not be possible to set threshold exactly for Y. In that case the closest possible voltage is used.  $Y_{calib}$  gives the value of this closest possible voltage.

Consider the example where it is required to set the AVDD rise threshold to 2.2 V (so  $Y=2.2$  V). This means that the EMU\_VMONAVDDCTRL\_RISETHRESCOARSE and EMU\_VMONAVDDCTRL\_RISETHRESFINE need to be programmed. Here are the steps that should be followed:

- Check VMONCAL0 register. It has the VMON AVDD channel calibrated thresholds for 1.86 V and 2.98 V. Lets assume that the following values are present in the associated bitfields:
  - AVDD1V86THRESCOARSE = 3
  - AVDD1V86THRESFINE = 5
  - AVDD2V98THRESCOARSE = 8
  - AVDD2V98THRESFINE = 7

- Using the above numbers and the VMON calibration equations:
  - $T_{1.86} = 35$
  - $T_{2.98} = 87$
  - $V_a = 21.53 \text{ mV}$
  - $V_b = 1.106 \text{ V}$
- Using the VMON threshold equations (with  $Y=2.2 \text{ V}$ ),  $\text{Thres}_Y = 51$  (rounded from 50.8) and  $Y_{\text{calib}} = 2.204 \text{ V}$

EMU\_VMONAVDDCTRL\_RISETHRESCOARSE should be programmed to 5 and EMU\_VMONAVDDCTRL\_RISETHRESFINE should be programmed to 1 (since  $\text{Thres}_Y = 51$ ). With these programmed values, VMON AVDD rise threshold is set for  $Y_{\text{calib}} = 2.204 \text{ V}$ , which is the closest programmable threshold.

### 11.3.13 Powering Off SRAM Blocks

SRAM blocks may be powered off using the EMU\_RAMxCTRL RAMPOWERDOWN fields. Selected blocks are powered down in order from the highest to lowest address in each bank. The lowest SRAM block in RAM0 cannot be powered off and will always remain powered on for proper system functionality. The stack must be located in retained memory. Refer to the EMU\_RAMxCTRL register descriptions for power configuration options and the associated address ranges.

### 11.3.14 Temperature Sensor

EMU provides low energy periodic temperature measurement. A temperature measurement is taken every 250 ms, with the 8-bit result stored in EMU->TEMP register.

**Note:** The EMU temperature sensor is always running (except in EM4 Shutoff) and is independent from the ADC temperature sensor.

The EMU provides the following features around temperature changes

- Wake-Up from EM4 Hibernate on Temperature Change
- Interrupt from High Level Trip
- Interrupt from Low Level Trip

During production test, the EMU temperature sensor for each device is calibrated at room temperature, with the corresponding calibration temperature and reading stored off in the DI page as follows:

- DEVINFO->CAL.TEMP : This bitfield contains the temperature in degrees C at calibration
- DEVINFO->EMUTEMP : This register contains the EMU->TEMP reading at the calibration temperature stored in DEVINFO->CAL.TEMP

The current calibrated EMU temperature sensor result from EMU->TEMP may be converted to degrees C using the following equation:

$$T_{J\_EMU} [^{\circ}\text{C}] = (\text{DEVINFO->CAL.TEMP}) + (\text{TEMPCO}_{EM_{xx}}) * [(\text{DEVINFO->EMUTEMP}) - (\text{EMU->TEMP})]$$

**Figure 11.8. Temperature Calculation**

$\text{TEMPCO}_{EM_{xx}}$  is a temperature coefficient that varies based on the energy mode at the time of the EMU temperature sensor reading:

- $\text{TEMPCO}_{EM01} = 0.278 + (\text{DEVINFO->EMUTEMP}) / 100$
- $\text{TEMPCO}_{EM234} = 0.268 + (\text{DEVINFO->EMUTEMP}) / 100$

For maximum accuracy when using the high/low level temperature interrupts, firmware should ensure that  $\text{TEMPCO}_{EM234}$  is used to set the temperature thresholds in EMU->TEMPLIMITS before entering EM2/3/4. Similarly, when exiting EM2/3/4, the temperature thresholds should be updated using  $\text{TEMPCO}_{EM01}$ .

Note that an increasing reading in EMU->TEMP corresponds to a decreasing temperature, and vice-versa. If enabled, the TEMPHIGH High Level Limit in EMU->TEMPLIMITS causes an interrupt flag on a increasing EMU->TEMP reading (i.e., decreasing temperature). Similarly, the TEMPLow Low Level Limit causes a interrupt flag on a decreasing EMU->TEMP reading (i.e., increasing temperature).

The EMU temperature sensor accuracy is approximately  $\pm 10^{\circ}\text{C}$  over most of the useable temperature range, but may be  $+15^{\circ}\text{C}$  at higher temperatures. Accordingly, any use of the EMU temperature sensor should include margin to account for that accuracy.

### 11.3.15 Registers latched in EM4

The following registers will be latched when entering EM4. After wake-up from EM4, these registers will be reset and require reprogramming prior to writing the EMU\_CMD\_EM4UNLATCH command.

- CMU\_LFRCOCTRL
- CMU\_LFXOCTRL
- CMU\_LFECLKSEL
- CMU\_LFECLKEN0
- CMU\_LFEPRESC0

### 11.3.16 Register Resets

Each EMU register requires retaining state in various energy modes and power transitions and will consequently need to be reset with a different condition. The following reset conditions will apply to the appropriate set of registers as marked in the Register Description table.

- Reset with POR or Hard Pin Reset
- Reset with POR, Hard Pin Reset, or any BOD reset
- Reset with SYSEXTENDEDRESETn
- Reset with FULLRESETn (default)

If a register field is not marked with a specific reset condition then it is assumed to be reset with FULLRESETn.

## 11.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name                      | Type  | Description   |
|--------|---------------------------|-------|---|
| 0x000  | EMU_CTRL                  | RW    | Control Register  |
| 0x004  | EMU_STATUS                | R     | Status Register   |
| 0x008  | EMU_LOCK                  | RWH   | Configuration Lock Register   |
| 0x00C  | EMU_RAM0CTRL              | RW    | Memory Control Register   |
| 0x010  | EMU_CMD                   | W1    | Command Register  |
| 0x018  | EMU_EM4CTRL               | RW    | EM4 Control Register  |
| 0x01C  | EMU_TEMPLIMITS            | RW    | Temperature Limits for Interrupt Generation   |
| 0x020  | EMU_TEMP                  | R     | Value of Last Temperature Measurement   |
| 0x024  | EMU_IF                    | R     | Interrupt Flag Register   |
| 0x028  | EMU_IFS                   | W1    | Interrupt Flag Set Register   |
| 0x02C  | EMU_IFC                   | (R)W1 | Interrupt Flag Clear Register   |
| 0x030  | EMU_IEN                   | RW    | Interrupt Enable Register   |
| 0x034  | EMU_PWRLOCK               | RW    | Regulator and Supply Lock Register  |
| 0x03C  | EMU_PWRCTRL               | RW    | Power Control Register  |
| 0x040  | EMU_DCDCCTRL              | RW    | DCDC Control  |
| 0x04C  | EMU_DCDCMISCCTRL          | RW    | DCDC Miscellaneous Control Register   |
| 0x050  | EMU_DCDCZDETCTRL          | RW    | DCDC Power Train NFET Zero Current Detector Control Register  |
| 0x054  | EMU_DCDCCLIMCTRL          | RW    | DCDC Power Train PFET Current Limiter Control Register  |
| 0x058  | EMU_DCDCLNCOMPCTRL        | RW    | DCDC Low Noise Compensator Control Register   |
| 0x05C  | EMU_DCDCLNVCTRL           | RWH   | DCDC Low Noise Voltage Register   |
| 0x064  | EMU_DCDCLPVCTRL           | RW    | DCDC Low Power Voltage Register   |
| 0x06C  | EMU_DCDCLPCTRL            | RW    | DCDC Low Power Control Register   |
| 0x070  | EMU_DCDCLNFREQCTRL        | RW    | DCDC Low Noise Controller Frequency Control   |
| 0x078  | EMU_DCDCSYNC              | R     | DCDC Read Status Register   |
| 0x090  | EMU_VMONAVDDCTRL          | RW    | VMON AVDD Channel Control   |
| 0x094  | EMU_VMONALTAVDDCTRL       | RW    | Alternate VMON AVDD Channel Control   |
| 0x098  | EMU_VMONDVDDCTRL          | RW    | VMON DVDD Channel Control   |
| 0x09C  | EMU_VMONIO0CTRL           | RW    | VMON IOVDD0 Channel Control   |
| 0x0B0  | EMU_RAM1CTRL              | RW    | Memory Control Register   |
| 0x0B4  | EMU_RAM2CTRL              | RW    | Memory Control Register   |
| 0x0E0  | EMU_DCDCLPEM01CFG         | RW    | Configuration Bits for Low Power Mode to Be Applied During EM01, This Field is Only Relevant If LP Mode is Used in EM01 |
| 0x0F4  | EMU_EM23PERNORETAINCMD    | W1    | Clears Corresponding Bits in EM23PERNORETAINSTATUS Unlocking Access to Peripheral                                       |
| 0x0F8  | EMU_EM23PERNORETAINSTATUS | R     | Status Indicating If Peripherals Were Powered Down in EM23, Subsequently Locking Access to It                           |

| Offset | Name                    | Type | Description   |
|--------|-------------------------|------|---|
| 0x0FC  | EMU_EM23PERNORETAINCTRL | RW   | When Set Corresponding Peripherals May Get Powered Down in EM23 |

## 11.5 Register Description

### 11.5.1 EMU\_CTRL - Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    |        |           |          |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------|--------|-----------|----------|
| 0x000         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    |        |           |          |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  | 0x0        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                  | 0      | 0         | 0        |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  | RW         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | RW                 | RW     | RW        | RW       |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | EM4HVSCALE |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  | EM23VSCALE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EM23VSCALEAUTOWSEN | EM01LD | EM2BODDIS | EM2BLOCK |

| Bit   | Name               | Reset   | Access                | Description   |
|-------|--------------------|---|-----------------------|---|
| 31:18 | Reserved           | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                       |   |
| 17:16 | EM4HVSCALE         | 0x0   | RW                    | <b>EM4H Voltage Scale</b><br><br>Set EM4H voltage. Entry to EM4H will trigger voltage scaling to this voltage if voltage scale level in EM4HVSCALE is less than that of VSCALE  |
|       | Value              | Mode  | Description           |   |
|       | 0                  | VSCALE2   | Voltage Scale Level 2 |   |
|       | 2                  | VSCALE0   | Voltage Scale Level 0 |   |
|       | 3                  | RESV  | RESV                  |   |
| 15:10 | Reserved           | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                       |   |
| 9:8   | EM23VSCALE         | 0x0   | RW                    | <b>EM23 Voltage Scale</b><br><br>Set EM23 voltage. Entry to EM2/3 will trigger voltage scaling to this voltage if voltage scale level in EM23VSCALE is lesser than that of VSCALE   |
|       | Value              | Mode  | Description           |   |
|       | 0                  | VSCALE2   | Voltage Scale Level 2 |   |
|       | 2                  | VSCALE0   | Voltage Scale Level 0 |   |
|       | 3                  | RESV  | RESV                  |   |
| 7:5   | Reserved           | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                       |   |
| 4     | EM23VSCALEAUTOWSEN | 0   | RW                    | <b>Automatically Configures Flash and Frequency to Wakeup From EM2 or EM3 at Low Voltage</b><br><br>With voltage scaling on EM2/3 entry, wakeup to EM0/1 will be at the same voltage as EM2. When this bit is set the Flash wait states and CMU clock frequency are automatically configured to safe value without needing software to configure it prior to EM2/3 entry. |

| Bit | Name            | Reset   | Access | Description  |
|-----|-----------------|---|--------|--|
| 3   | EM01LD          | 0   | RW     | <b>Reserved for internal use. Do not change.</b><br>Reserved for internal use. Do not change.                              |
| 2   | EM2BODDIS       | 0   | RW     | <b>Disable BOD in EM2</b><br>This bit is used to disable BODs to minimize current in EM2. Reset with POR or Hard Pin Reset |
| 1   | EM2BLOCK        | 0   | RW     | <b>Energy Mode 2 Block</b><br>This bit is used to prevent the MCU from entering Energy Mode 2 or 3.                        |
| 0   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |

## 11.5.2 EMU\_STATUS - Status Register

| Offset        | Bit Position |    |    |    |    |            |           |    |    |    |    |          |    |            |        |    |    |    |    |    |    |    |   |          |   |   |   |         |          |             |          |         |   |
|---------------|--------------|----|----|----|----|------------|-----------|----|----|----|----|----------|----|------------|--------|----|----|----|----|----|----|----|---|----------|---|---|---|---------|----------|-------------|----------|---------|---|
| 0x004         | 31           | 30 | 29 | 28 | 27 | 26         | 25        | 24 | 23 | 22 | 21 | 20       | 19 | 18         | 17     | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8        | 7 | 6 | 5 | 4       | 3        | 2           | 1        | 0       |   |
| <b>Reset</b>  |              |    |    |    |    | 0          | 0         |    |    |    |    | 0        |    | 0          | 0x0    |    |    |    |    |    |    |    |   | 0        |   |   |   |         | 0        | 0           | 0        | 0       | 0 |
| <b>Access</b> |              |    |    |    |    | R          | R         |    |    |    |    | R        |    | R          | R      |    |    |    |    |    |    |    |   | R        |   |   |   |         | R        | R           | R        | R       | R |
| <b>Name</b>   |              |    |    |    |    | TEMPACTIVE | RACACTIVE |    |    |    |    | EM4IORET |    | VSCALEBUSY | VSCALE |    |    |    |    |    |    |    |   | VMONFVDD |   |   |   | VMONIO0 | VMONDVDD | VMONALTAVDD | VMONAVDD | VMONRDY |   |

| Bit   | Name       | Reset    | Access | Description   |
|-------|------------|----------|--------|---|
| 31:27 | Reserved   |          |        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a>  |
| 26    | TEMPACTIVE | 0        | R      | <b>Temperature Measurement Active</b><br>This signal is set during EMU Temperature measurement  |
| 25    | RACACTIVE  | 0        | R      | <b>Radio Controller Active</b><br>This bit indicates the status of the RAC state machine. System can not enter EM2 or lower if set.   |
|       | Value      |          |        | Description   |
|       | 0          |          |        | RAC is in OFF state   |
|       | 1          |          |        | RAC is not in OFF state   |
| 24:21 | Reserved   |          |        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a>  |
| 20    | EM4IORET   | 0        | R      | <b>IO Retention Status</b><br>The status of IO retention. Will be set upon EM4 entry based on EM4IORETMODE in EMU_EM4CTRL. Cleared by setting EM4UNLATCH in EMU_CMD, and can also be cleared in EM4H by the VMON.                                   |
|       | Value      | Mode     |        | Description   |
|       | 0          | DISABLED |        | IO retention is disabled.   |
|       | 1          | ENABLED  |        | IO retention is enabled.  |
| 19    | Reserved   |          |        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a>  |
| 18    | VSCALEBUSY | 0        | R      | <b>System is Busy Scaling Voltage</b><br>Indicates that the system is busy scaling voltage in EM0/1. Writing EM01VSCALE0 or EM01VSCALE2 in EMU_CMD register while this is set will abort the current voltage scaling process and initiate a new one |
| 17:16 | VSCALE     | 0x0      | R      | <b>Current Voltage Scale Value</b><br>This shows the current system voltage value. This gets updated after VSCALEDONE interrupt or on EM23 exit or EM4H exit  |
|       | Value      | Mode     |        | Description   |
|       | 0          | VSCALE2  |        | Voltage Scale Level 2   |
|       | 2          | VSCALE0  |        | Voltage Scale Level 0   |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 3    |                 | RESV  |        | RESV  |
| 15:9 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 8    | VMONFVDD        | 0   | R      | <b>VMON VDDFLASH Channel</b><br>Indicates the status of the VDDFLASH channel of the VMON.   |
| 7:5  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 4    | VMONIO0         | 0   | R      | <b>VMON IOVDD0 Channel</b><br>Indicates the status of the IOVDD0 channel of the VMON.   |
| 3    | VMONDVDD        | 0   | R      | <b>VMON DVDD Channel</b><br>Indicates the status of the DVDD channel of the VMON.   |
| 2    | VMONALTAVDD     | 0   | R      | <b>Alternate VMON AVDD Channel</b><br>Indicates the status of the Alternate AVDD channel of the VMON.   |
| 1    | VMONAVDD        | 0   | R      | <b>VMON AVDD Channel</b><br>Indicates the status of the AVDD channel of the VMON.   |
| 0    | VMONRDY         | 0   | R      | <b>VMON Ready</b><br>VMON status. When high, this bit indicates that all the enabled channels are ready. When low, it indicates that one or more of the enabled channels are not ready. |

### 11.5.3 EMU\_LOCK - Configuration Lock Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x008         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LOCKKEY |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name     | Reset   | Access                     | Description                   |
|--|----------|---|----------------------------|-------------------------------|
| 31:16  | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                            |                               |
| 15:0   | LOCKKEY  | 0x0000  | RWH                        | <b>Configuration Lock Key</b> |
| Write any other value than the unlock code to lock all EMU registers, except the interrupt registers and regulator control registers, from editing. Write the unlock code to unlock. When reading the register, bit 0 is set when the lock is enabled. |          |   |                            |                               |
| Mode   |          | Value   | Description                |                               |
| Read Operation   |          |   |                            |                               |
| UNLOCKED   |          | 0   | EMU registers are unlocked |                               |
| LOCKED   |          | 1   | EMU registers are locked   |                               |
| Write Operation  |          |   |                            |                               |
| LOCK   |          | 0   | Lock EMU registers         |                               |
| UNLOCK   |          | 0xADE8  | Unlock EMU registers       |                               |

## 11.5.4 EMU\_RAM0CTRL - Memory Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |              |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|--------------|
| 0x00C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0            |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0x0          |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | RW           |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | RAMPOWERDOWN |

| Bit  | Name            | Reset   | Access                              | Description   |
|------|-----------------|---|-------------------------------------|---|
| 31:1 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                     |   |
| 0:0  | RAMPOWERDOWN    | 0x0   | RW                                  | <b>RAM0 Blockset Power-down</b><br>RAM blockset power-down in EM23 with full access in EM01. Block 0 may never be powered down. |
|      | Mode            | Value   | Description                         |   |
|      | NONE            | 0x00  | None of the RAM blocks powered down |   |
|      | BLK1            | 0x1   | Power down RAM block 1              |   |



## 11.5.6 EMU\_EM4CTRL - EM4 Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |    |    |    |    |    |    |   |   |   |   |   |              |              |            |             |          |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|----|----|----|---|---|---|---|---|--------------|--------------|------------|-------------|----------|
| 0x018         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16       | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4            | 3            | 2          | 1           | 0        |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0      |    |    |    |    |    |    |   |   |   |   |   | 0x0          | 0            | 0          | 0           | 0        |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W1       |    |    |    |    |    |    |   |   |   |   |   | RW           | RW           | RW         | RW          | RW       |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | EM4ENTRY |    |    |    |    |    |    |   |   |   |   |   | EM4IORETMODE | RETAINULFRCO | RETAINLFXO | RETAINLFRCO | EM4STATE |

| Bit   | Name         | Reset  | Access   | Description  |
|-------|--------------|--|--|--|
| 31:18 | Reserved     | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |  |  |
| 17:16 | EM4ENTRY     | 0x0  | W1   | <b>Energy Mode 4 Entry</b><br><br>This register is used to enter the Energy Mode 4 sequence. Writing the sequence 2,3,2,3,2,3,2,3,2 will enter the part into Energy Mode 4.  |
| 15:6  | Reserved     | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |  |  |
| 5:4   | EM4IORETMODE | 0x0  | RW   | <b>EM4 IO Retention Disable</b><br><br>Determine when IO retention will be applied and removed.  |
|       | Value        | Mode   | Description  |  |
|       | 0            | DISABLE  | No Retention: Pads enter reset state when entering EM4                                 |  |
|       | 1            | EM4EXIT  | Retention through EM4: Pads enter reset state when exiting EM4                         |  |
|       | 2            | SWUNLATCH  | Retention through EM4 and Wakeup: software writes UNLATCH register to remove retention |  |
| 3     | RETAINULFRCO | 0  | RW   | <b>ULFRCO Retain During EM4S</b><br><br>Retain the ULFRCO upon EM4S entry. If set to 1, an already running ULFRCO will be retained in its running state in EM4. ULFRCO will always be retained if EM4STATE is in EM4H.   |
| 2     | RETAINLFXO   | 0  | RW   | <b>LFXO Retain During EM4</b><br><br>Retain the LFXO upon EM4(SH/H) entry. If set to 1, an already running LFXO will be retained in its running state in EM4.  |
| 1     | RETAINLFRCO  | 0  | RW   | <b>LFRCO Retain During EM4</b><br><br>Retain the LFRCO upon EM4(S/H) entry. If set to 1, an already running LFRCO will be retained in its running state in EM4.  |
| 0     | EM4STATE     | 0  | RW   | <b>Energy Mode 4 State</b><br><br>When set, the system will enter Hibernate state (EM4H) when entering EM4. In EM4H, the regulator will be on in reduced mode allowing for RTCC. Otherwise, when entering in EM4, the regulator will be disabled allowing for lowest power mode, Shutoff state (EM4S). Only reset with POR or Hard Pin Reset |
|       | Value        | Mode   | Description  |  |
|       | 0            | EM4S   | EM4S Shutoff state   |  |
|       | 1            | EM4H   | EM4H Hibernate state   |  |

## 11.5.7 EMU\_TEMPLIMITS - Temperature Limits for Interrupt Generation

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |          |    |    |    |    |    |         |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----------|----|----|----|----|----|---------|---|---|---|---|---|---|---|---|---|
| 0x01C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16      | 15       | 14 | 13 | 12 | 11 | 10 | 9       | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       | 0xFF     |    |    |    |    |    | 0x00    |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      | RW       |    |    |    |    |    | RW      |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | EM4WUEN | TEMPHIGH |    |    |    |    |    | TEMPLOW |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset   | Access | Description   |
|-------|----------|---|--------|---|
| 31:17 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 16    | EM4WUEN  | 0   | RW     | <b>Enable EM4 Wakeup Due to Low/high Temperature</b><br>Enable EM4 wakeup from low or high temperature from EM4H  |
| 15:8  | TEMPHIGH | 0xFF  | RW     | <b>Temperature High Limit</b><br>The TEMPHIGH interrupt flag is set when a periodic temperature measurement is equal to or higher than this value. If the high limit is changed during a temperature measurement (TEMPACTIVE=1), the limit update will be delayed until the end of the temperature measurement. |
| 7:0   | TEMPLOW  | 0x00  | RW     | <b>Temperature Low Limit</b><br>The TEMPLOW interrupt flag is set when a periodic temperature measurement is equal to or lower than this value. If the low limit is changed during a temperature measurement (TEMPACTIVE=1), the limit update will be delayed until the end of the temperature measurement.     |

## 11.5.8 EMU\_TEMP - Value of Last Temperature Measurement

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |      |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x020         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16   | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0xXX |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | TEMP |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name     | Reset   | Access | Description   |
|------|----------|---|--------|---|
| 31:8 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 7:0  | TEMP     | 0xXX  | R      | <b>Temperature Measurement</b><br>Value of last periodic temperature measurement. Value is asynchronously updated. Value is stable for 250 ms after a temperature-based interrupt (TEMPHIGH, TEMPLOW, or TEMP) and can be read with a single read operation. If register is read not in response to a temperature-based interrupt, multiple readings should be taken until two consecutive values are the same. |

### 11.5.9 EMU\_IF - Interrupt Flag Register

| Offset        | Bit Position |         |      |    |    |    |            |            |    |    |    |              |               |               |                      |                      |              |              |    |    |    |    |   |   |             |             |              |              |                 |                 |              |              |   |
|---------------|--------------|---------|------|----|----|----|------------|------------|----|----|----|--------------|---------------|---------------|----------------------|----------------------|--------------|--------------|----|----|----|----|---|---|-------------|-------------|--------------|--------------|-----------------|-----------------|--------------|--------------|---|
| 0x024         | 31           | 30      | 29   | 28 | 27 | 26 | 25         | 24         | 23 | 22 | 21 | 20           | 19            | 18            | 17                   | 16                   | 15           | 14           | 13 | 12 | 11 | 10 | 9 | 8 | 7           | 6           | 5            | 4            | 3               | 2               | 1            | 0            |   |
| <b>Reset</b>  | 0            | 0       | 0    |    |    |    | 0          | 0          |    |    |    | 0            | 0             | 0             | 0                    | 0                    | 0            | 0            |    |    |    |    |   |   |             | 0           | 0            | 0            | 0               | 0               | 0            | 0            | 0 |
| <b>Access</b> | R            | R       | R    |    |    |    | R          | R          |    |    |    | R            | R             | R             | R                    | R                    | R            | R            |    |    |    |    |   |   |             | R           | R            | R            | R               | R               | R            | R            | R |
| <b>Name</b>   | TEMPHIGH     | TEMPLOW | TEMP |    |    |    | VSCALEDONE | EM23WAKEUP |    |    |    | DCDCINBYPASS | DCDCLNRUNNING | DCDCLPRUNNING | NFETOVERCURRENTLIMIT | PFETOVERCURRENTLIMIT | VMONFVDDRISE | VMONFVDDFALL |    |    |    |    |   |   | VMONIO0RISE | VMONIO0FALL | VMONDVDDRISE | VMONDVDDFALL | VMONALTAVDDRISE | VMONALTAVDDFALL | VMONAVDDRISE | VMONAVDDFALL |   |

| Bit   | Name                 | Reset   | Access | Description   |
|-------|----------------------|---|--------|---|
| 31    | TEMPHIGH             | 0   | R      | <b>Temperature High Limit Reached</b><br>Set when the value of a periodic temperature measurement is higher or equal than TEMPHIGH in EMU_TEMPLIMITS  |
| 30    | TEMPLOW              | 0   | R      | <b>Temperature Low Limit Reached</b><br>Set when the value of a periodic temperature measurement is lower or equal than TEMPHIGH in EMU_TEMPLIMITS  |
| 29    | TEMP                 | 0   | R      | <b>New Temperature Measurement Valid</b><br>Set when a new periodic temperature measurement is available  |
| 28:26 | <i>Reserved</i>      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 25    | VSCALEDONE           | 0   | R      | <b>Voltage Scale Steps Done IRQ</b><br>Will be set when all the steps needed for voltage scaling is done. For voltage upgrade, the software can start increasing clock frequency after this interrupt. For voltage downgrade, this will indicate that hardware has finished all the steps including updating of BOD levels and regulator controls, but voltage drop may take lot longer due to load current |
| 24    | EM23WAKEUP           | 0   | R      | <b>Wakeup IRQ From EM2 and EM3</b><br>Will be set when the system wakes up from EM2 and EM3. This interrupt can be used to run initialization code need to reconfigure the system when returning from EM2 and EM3.  |
| 23:21 | <i>Reserved</i>      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 20    | DCDCINBYPASS         | 0   | R      | <b>DCDC is in Bypass</b><br>DCDC is in bypass   |
| 19    | DCDCLNRUNNING        | 0   | R      | <b>LN Mode is Running</b><br>This flag is set once the DCDC regulator has started to run in LN mode   |
| 18    | DCDCLPRUNNING        | 0   | R      | <b>LP Mode is Running</b><br>This flag is set once the DCDC regulator has started to run in LP mode   |
| 17    | NFETOVERCURRENTLIMIT | 0   | R      | <b>NFET Current Limit Hit</b><br>Reserved for internal use.   |

| Bit  | Name                 | Reset   | Access | Description   |
|------|----------------------|---|--------|---|
| 16   | PFETOVERCURRENTLIMIT | 0   | R      | <b>PFET Current Limit Hit</b><br><br>Reserved for internal use.   |
| 15   | VMONFVDDRRISE        | 0   | R      | <b>VMON VDDFLASH Channel Rise</b><br><br>A rising edge on VMON VDDFLASH channel has been detected.              |
| 14   | VMONFVDDFALL         | 0   | R      | <b>VMON VDDFLASH Channel Fall</b><br><br>A falling edge on VMON VDDFLASH channel has been detected.             |
| 13:8 | <i>Reserved</i>      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 7    | VMONIO0RISE          | 0   | R      | <b>VMON IOVDD0 Channel Rise</b><br><br>A rising edge on VMON IOVDD0 channel has been detected.                  |
| 6    | VMONIO0FALL          | 0   | R      | <b>VMON IOVDD0 Channel Fall</b><br><br>A falling edge on VMON IOVDD0 channel has been detected.                 |
| 5    | VMONDVDDRRISE        | 0   | R      | <b>VMON DVDD Channel Rise</b><br><br>A rising edge on VMON DVDD channel has been detected.                      |
| 4    | VMONDVDDFALL         | 0   | R      | <b>VMON DVDD Channel Fall</b><br><br>A falling edge on VMON DVDD channel has been detected.                     |
| 3    | VMONALTAVDDRRISE     | 0   | R      | <b>Alternate VMON AVDD Channel Rise</b><br><br>A rising edge on Alternate VMON AVDD channel has been detected.  |
| 2    | VMONALTAVDDFALL      | 0   | R      | <b>Alternate VMON AVDD Channel Fall</b><br><br>A falling edge on Alternate VMON AVDD channel has been detected. |
| 1    | VMONAVDDRRISE        | 0   | R      | <b>VMON AVDD Channel Rise</b><br><br>A rising edge on VMON AVDD channel has been detected.                      |
| 0    | VMONAVDDFALL         | 0   | R      | <b>VMON AVDD Channel Fall</b><br><br>A falling edge on VMON AVDD channel has been detected.                     |

## 11.5.10 EMU\_IFS - Interrupt Flag Set Register

| Offset        | Bit Position |         |      |    |    |    |            |            |    |    |    |              |               |               |                      |                      |              |              |    |    |    |    |   |   |             |             |              |              |                 |                 |              |              |    |
|---------------|--------------|---------|------|----|----|----|------------|------------|----|----|----|--------------|---------------|---------------|----------------------|----------------------|--------------|--------------|----|----|----|----|---|---|-------------|-------------|--------------|--------------|-----------------|-----------------|--------------|--------------|----|
| 0x028         | 31           | 30      | 29   | 28 | 27 | 26 | 25         | 24         | 23 | 22 | 21 | 20           | 19            | 18            | 17                   | 16                   | 15           | 14           | 13 | 12 | 11 | 10 | 9 | 8 | 7           | 6           | 5            | 4            | 3               | 2               | 1            | 0            |    |
| <b>Reset</b>  | 0            | 0       | 0    |    |    |    | 0          | 0          |    |    |    | 0            | 0             | 0             | 0                    | 0                    | 0            | 0            |    |    |    |    |   |   |             | 0           | 0            | 0            | 0               | 0               | 0            | 0            | 0  |
| <b>Access</b> | W1           | W1      | W1   |    |    |    | W1         | W1         |    |    |    | W1           | W1            | W1            | W1                   | W1                   | W1           | W1           |    |    |    |    |   |   |             | W1          | W1           | W1           | W1              | W1              | W1           | W1           | W1 |
| <b>Name</b>   | TEMPHIGH     | TEMPLOW | TEMP |    |    |    | VSCALEDONE | EM23WAKEUP |    |    |    | DCDCINBYPASS | DCDCLNRUNNING | DCDCLPRUNNING | NFETOVERCURRENTLIMIT | PFETOVERCURRENTLIMIT | VMONFVDDRISE | VMONFVDDFALL |    |    |    |    |   |   | VMONIO0RISE | VMONIO0FALL | VMONDVDDRISE | VMONDVDDFALL | VMONALTAVDDRISE | VMONALTAVDDFALL | VMONAVDDRISE | VMONAVDDFALL |    |

| Bit   | Name                 | Reset   | Access | Description  |
|-------|----------------------|---|--------|--|
| 31    | TEMPHIGH             | 0   | W1     | <b>Set TEMPHIGH Interrupt Flag</b><br>Write 1 to set the TEMPHIGH interrupt flag                         |
| 30    | TEMPLOW              | 0   | W1     | <b>Set TEMPLOW Interrupt Flag</b><br>Write 1 to set the TEMPLOW interrupt flag                           |
| 29    | TEMP                 | 0   | W1     | <b>Set TEMP Interrupt Flag</b><br>Write 1 to set the TEMP interrupt flag                                 |
| 28:26 | <i>Reserved</i>      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 25    | VSCALEDONE           | 0   | W1     | <b>Set VSCALEDONE Interrupt Flag</b><br>Write 1 to set the VSCALEDONE interrupt flag                     |
| 24    | EM23WAKEUP           | 0   | W1     | <b>Set EM23WAKEUP Interrupt Flag</b><br>Write 1 to set the EM23WAKEUP interrupt flag                     |
| 23:21 | <i>Reserved</i>      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 20    | DCDCINBYPASS         | 0   | W1     | <b>Set DCDCINBYPASS Interrupt Flag</b><br>Write 1 to set the DCDCINBYPASS interrupt flag                 |
| 19    | DCDCLNRUNNING        | 0   | W1     | <b>Set DCDCLNRUNNING Interrupt Flag</b><br>Write 1 to set the DCDCLNRUNNING interrupt flag               |
| 18    | DCDCLPRUNNING        | 0   | W1     | <b>Set DCDCLPRUNNING Interrupt Flag</b><br>Write 1 to set the DCDCLPRUNNING interrupt flag               |
| 17    | NFETOVERCURRENTLIMIT | 0   | W1     | <b>Set NFETOVERCURRENTLIMIT Interrupt Flag</b><br>Write 1 to set the NFETOVERCURRENTLIMIT interrupt flag |
| 16    | PFETOVERCURRENTLIMIT | 0   | W1     | <b>Set PFETOVERCURRENTLIMIT Interrupt Flag</b><br>Write 1 to set the PFETOVERCURRENTLIMIT interrupt flag |

| Bit  | Name            | Reset   | Access | Description  |
|------|-----------------|---|--------|--|
| 15   | VMONFVDDRISE    | 0   | W1     | <b>Set VMONFVDDRISE Interrupt Flag</b><br>Write 1 to set the VMONFVDDRISE interrupt flag       |
| 14   | VMONFVDDFALL    | 0   | W1     | <b>Set VMONFVDDFALL Interrupt Flag</b><br>Write 1 to set the VMONFVDDFALL interrupt flag       |
| 13:8 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 7    | VMONIO0RISE     | 0   | W1     | <b>Set VMONIO0RISE Interrupt Flag</b><br>Write 1 to set the VMONIO0RISE interrupt flag         |
| 6    | VMONIO0FALL     | 0   | W1     | <b>Set VMONIO0FALL Interrupt Flag</b><br>Write 1 to set the VMONIO0FALL interrupt flag         |
| 5    | VMONDVDDRISE    | 0   | W1     | <b>Set VMONDVDDRISE Interrupt Flag</b><br>Write 1 to set the VMONDVDDRISE interrupt flag       |
| 4    | VMONDVDDFALL    | 0   | W1     | <b>Set VMONDVDDFALL Interrupt Flag</b><br>Write 1 to set the VMONDVDDFALL interrupt flag       |
| 3    | VMONALTAVDDRISE | 0   | W1     | <b>Set VMONALTAVDDRISE Interrupt Flag</b><br>Write 1 to set the VMONALTAVDDRISE interrupt flag |
| 2    | VMONALTAVDDFALL | 0   | W1     | <b>Set VMONALTAVDDFALL Interrupt Flag</b><br>Write 1 to set the VMONALTAVDDFALL interrupt flag |
| 1    | VMONAVDDRISE    | 0   | W1     | <b>Set VMONAVDDRISE Interrupt Flag</b><br>Write 1 to set the VMONAVDDRISE interrupt flag       |
| 0    | VMONAVDDFALL    | 0   | W1     | <b>Set VMONAVDDFALL Interrupt Flag</b><br>Write 1 to set the VMONAVDDFALL interrupt flag       |

11.5.11 EMU\_IFC - Interrupt Flag Clear Register

| Offset | Bit Position |         |       |    |    |    |            |            |    |    |    |              |               |               |                      |                      |              |              |    |    |    |    |   |   |             |             |              |              |                 |                 |              |              |   |
|--------|--------------|---------|-------|----|----|----|------------|------------|----|----|----|--------------|---------------|---------------|----------------------|----------------------|--------------|--------------|----|----|----|----|---|---|-------------|-------------|--------------|--------------|-----------------|-----------------|--------------|--------------|---|
| 0x02C  | 31           | 30      | 29    | 28 | 27 | 26 | 25         | 24         | 23 | 22 | 21 | 20           | 19            | 18            | 17                   | 16                   | 15           | 14           | 13 | 12 | 11 | 10 | 9 | 8 | 7           | 6           | 5            | 4            | 3               | 2               | 1            | 0            |   |
| Reset  | 0            | 0       | 0     |    |    |    | 0          | 0          |    |    |    | 0            | 0             | 0             | 0                    | 0                    | 0            | 0            |    |    |    |    |   |   |             | 0           | 0            | 0            | 0               | 0               | 0            | 0            | 0 |
| Access | (R)W1        | (R)W1   | (R)W1 |    |    |    | (R)W1      | (R)W1      |    |    |    | (R)W1        | (R)W1         | (R)W1         | (R)W1                | (R)W1                | (R)W1        | (R)W1        |    |    |    |    |   |   | (R)W1       | (R)W1       | (R)W1        | (R)W1        | (R)W1           | (R)W1           | (R)W1        | (R)W1        |   |
| Name   | TEMPHIGH     | TEMPLOW | TEMP  |    |    |    | VSCALEDONE | EM23WAKEUP |    |    |    | DCDCINBYPASS | DCDCLNRUNNING | DCDCLPRUNNING | NFETOVERCURRENTLIMIT | PFETOVERCURRENTLIMIT | VMONFVDDRISE | VMONFVDDFALL |    |    |    |    |   |   | VMONIO0RISE | VMONIO0FALL | VMONDVDDRISE | VMONDVDDFALL | VMONALTAVDDRISE | VMONALTAVDDFALL | VMONAVDDRISE | VMONAVDDFALL |   |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31    | TEMPHIGH        | 0   | (R)W1  | <b>Clear TEMPHIGH Interrupt Flag</b><br><br>Write 1 to clear the TEMPHIGH interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).           |
| 30    | TEMPLOW         | 0   | (R)W1  | <b>Clear TEMPLOW Interrupt Flag</b><br><br>Write 1 to clear the TEMPLOW interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).             |
| 29    | TEMP            | 0   | (R)W1  | <b>Clear TEMP Interrupt Flag</b><br><br>Write 1 to clear the TEMP interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                   |
| 28:26 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 25    | VSCALEDONE      | 0   | (R)W1  | <b>Clear VSCALEDONE Interrupt Flag</b><br><br>Write 1 to clear the VSCALEDONE interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).       |
| 24    | EM23WAKEUP      | 0   | (R)W1  | <b>Clear EM23WAKEUP Interrupt Flag</b><br><br>Write 1 to clear the EM23WAKEUP interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).       |
| 23:21 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 20    | DCDCINBYPASS    | 0   | (R)W1  | <b>Clear DCDCINBYPASS Interrupt Flag</b><br><br>Write 1 to clear the DCDCINBYPASS interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |
| 19    | DCDCLNRUNNING   | 0   | (R)W1  | <b>Clear DCDCLNRUNNING Interrupt Flag</b><br><br>Write 1 to clear the DCDCLNRUNNING interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 18    | DCDCLPRUNNING   | 0   | (R)W1  | <b>Clear DCDCLPRUNNING Interrupt Flag</b><br><br>Write 1 to clear the DCDCLPRUNNING interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |

| Bit  | Name                 | Reset   | Access | Description   |
|------|----------------------|---|--------|---|
| 17   | NFETOVERCURRENTLIMIT | 0   | (R)W1  | <b>Clear NFETOVERCURRENTLIMIT Interrupt Flag</b><br><br>Write 1 to clear the NFETOVERCURRENTLIMIT interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 16   | PFETOVERCURRENTLIMIT | 0   | (R)W1  | <b>Clear PFETOVERCURRENTLIMIT Interrupt Flag</b><br><br>Write 1 to clear the PFETOVERCURRENTLIMIT interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 15   | VMONFVDDRRISE        | 0   | (R)W1  | <b>Clear VMONFVDDRRISE Interrupt Flag</b><br><br>Write 1 to clear the VMONFVDDRRISE interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).               |
| 14   | VMONFVDDFALL         | 0   | (R)W1  | <b>Clear VMONFVDDFALL Interrupt Flag</b><br><br>Write 1 to clear the VMONFVDDFALL interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                 |
| 13:8 | <i>Reserved</i>      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 7    | VMONIOORRISE         | 0   | (R)W1  | <b>Clear VMONIOORRISE Interrupt Flag</b><br><br>Write 1 to clear the VMONIOORRISE interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                 |
| 6    | VMONIOOFALL          | 0   | (R)W1  | <b>Clear VMONIOOFALL Interrupt Flag</b><br><br>Write 1 to clear the VMONIOOFALL interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                   |
| 5    | VMONDVDDRRISE        | 0   | (R)W1  | <b>Clear VMONDVDDRRISE Interrupt Flag</b><br><br>Write 1 to clear the VMONDVDDRRISE interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).               |
| 4    | VMONDVDDFALL         | 0   | (R)W1  | <b>Clear VMONDVDDFALL Interrupt Flag</b><br><br>Write 1 to clear the VMONDVDDFALL interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                 |
| 3    | VMONALTAVDDRRISE     | 0   | (R)W1  | <b>Clear VMONALTAVDDRRISE Interrupt Flag</b><br><br>Write 1 to clear the VMONALTAVDDRRISE interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).         |
| 2    | VMONALTAVDDFALL      | 0   | (R)W1  | <b>Clear VMONALTAVDDFALL Interrupt Flag</b><br><br>Write 1 to clear the VMONALTAVDDFALL interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).           |
| 1    | VMONAVDDRRISE        | 0   | (R)W1  | <b>Clear VMONAVDDRRISE Interrupt Flag</b><br><br>Write 1 to clear the VMONAVDDRRISE interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).               |
| 0    | VMONAVDDFALL         | 0   | (R)W1  | <b>Clear VMONAVDDFALL Interrupt Flag</b><br><br>Write 1 to clear the VMONAVDDFALL interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                 |

## 11.5.12 EMU\_IEN - Interrupt Enable Register

| Offset        | Bit Position |         |      |    |    |    |            |            |    |    |    |              |               |               |                      |                      |              |              |    |    |    |    |   |   |             |             |              |              |                 |                 |              |              |    |
|---------------|--------------|---------|------|----|----|----|------------|------------|----|----|----|--------------|---------------|---------------|----------------------|----------------------|--------------|--------------|----|----|----|----|---|---|-------------|-------------|--------------|--------------|-----------------|-----------------|--------------|--------------|----|
| 0x030         | 31           | 30      | 29   | 28 | 27 | 26 | 25         | 24         | 23 | 22 | 21 | 20           | 19            | 18            | 17                   | 16                   | 15           | 14           | 13 | 12 | 11 | 10 | 9 | 8 | 7           | 6           | 5            | 4            | 3               | 2               | 1            | 0            |    |
| <b>Reset</b>  | 0            | 0       | 0    |    |    |    | 0          | 0          |    |    |    | 0            | 0             | 0             | 0                    | 0                    | 0            | 0            |    |    |    |    |   |   |             | 0           | 0            | 0            | 0               | 0               | 0            | 0            | 0  |
| <b>Access</b> | RW           | RW      | RW   |    |    |    | RW         | RW         |    |    |    | RW           | RW            | RW            | RW                   | RW                   | RW           | RW           |    |    |    |    |   |   |             | RW          | RW           | RW           | RW              | RW              | RW           | RW           | RW |
| <b>Name</b>   | TEMPHIGH     | TEMPLOW | TEMP |    |    |    | VSCALEDONE | EM23WAKEUP |    |    |    | DCDCINBYPASS | DCDCLNRUNNING | DCDCLPRUNNING | NFETOVERCURRENTLIMIT | PFETOVERCURRENTLIMIT | VMONFVDDRISE | VMONFVDDFALL |    |    |    |    |   |   | VMONIO0RISE | VMONIO0FALL | VMONDVDDRISE | VMONDVDDFALL | VMONALTAVDDRISE | VMONALTAVDDFALL | VMONAVDDRISE | VMONAVDDFALL |    |

| Bit   | Name                 | Reset   | Access | Description   |
|-------|----------------------|---|--------|---|
| 31    | TEMPHIGH             | 0   | RW     | <b>TEMPHIGH Interrupt Enable</b><br>Enable/disable the TEMPHIGH interrupt                         |
| 30    | TEMPLOW              | 0   | RW     | <b>TEMPLOW Interrupt Enable</b><br>Enable/disable the TEMPLOW interrupt                           |
| 29    | TEMP                 | 0   | RW     | <b>TEMP Interrupt Enable</b><br>Enable/disable the TEMP interrupt                                 |
| 28:26 | <i>Reserved</i>      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 25    | VSCALEDONE           | 0   | RW     | <b>VSCALEDONE Interrupt Enable</b><br>Enable/disable the VSCALEDONE interrupt                     |
| 24    | EM23WAKEUP           | 0   | RW     | <b>EM23WAKEUP Interrupt Enable</b><br>Enable/disable the EM23WAKEUP interrupt                     |
| 23:21 | <i>Reserved</i>      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 20    | DCDCINBYPASS         | 0   | RW     | <b>DCDCINBYPASS Interrupt Enable</b><br>Enable/disable the DCDCINBYPASS interrupt                 |
| 19    | DCDCLNRUNNING        | 0   | RW     | <b>DCDCLNRUNNING Interrupt Enable</b><br>Enable/disable the DCDCLNRUNNING interrupt               |
| 18    | DCDCLPRUNNING        | 0   | RW     | <b>DCDCLPRUNNING Interrupt Enable</b><br>Enable/disable the DCDCLPRUNNING interrupt               |
| 17    | NFETOVERCURRENTLIMIT | 0   | RW     | <b>NFETOVERCURRENTLIMIT Interrupt Enable</b><br>Enable/disable the NFETOVERCURRENTLIMIT interrupt |
| 16    | PFETOVERCURRENTLIMIT | 0   | RW     | <b>PFETOVERCURRENTLIMIT Interrupt Enable</b><br>Enable/disable the PFETOVERCURRENTLIMIT interrupt |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 15   | VMONFVDDRISE    | 0   | RW     | <b>VMONFVDDRISE Interrupt Enable</b><br>Enable/disable the VMONFVDDRISE interrupt       |
| 14   | VMONFVDDFALL    | 0   | RW     | <b>VMONFVDDFALL Interrupt Enable</b><br>Enable/disable the VMONFVDDFALL interrupt       |
| 13:8 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 7    | VMONIO0RISE     | 0   | RW     | <b>VMONIO0RISE Interrupt Enable</b><br>Enable/disable the VMONIO0RISE interrupt         |
| 6    | VMONIO0FALL     | 0   | RW     | <b>VMONIO0FALL Interrupt Enable</b><br>Enable/disable the VMONIO0FALL interrupt         |
| 5    | VMONDVDDRISE    | 0   | RW     | <b>VMONDVDDRISE Interrupt Enable</b><br>Enable/disable the VMONDVDDRISE interrupt       |
| 4    | VMONDVDDFALL    | 0   | RW     | <b>VMONDVDDFALL Interrupt Enable</b><br>Enable/disable the VMONDVDDFALL interrupt       |
| 3    | VMONALTAVDDRISE | 0   | RW     | <b>VMONALTAVDDRISE Interrupt Enable</b><br>Enable/disable the VMONALTAVDDRISE interrupt |
| 2    | VMONALTAVDDFALL | 0   | RW     | <b>VMONALTAVDDFALL Interrupt Enable</b><br>Enable/disable the VMONALTAVDDFALL interrupt |
| 1    | VMONAVDDRISE    | 0   | RW     | <b>VMONAVDDRISE Interrupt Enable</b><br>Enable/disable the VMONAVDDRISE interrupt       |
| 0    | VMONAVDDFALL    | 0   | RW     | <b>VMONAVDDFALL Interrupt Enable</b><br>Enable/disable the VMONAVDDFALL interrupt       |

### 11.5.13 EMU\_PWRLOCK - Regulator and Supply Lock Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x034         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LOCKKEY |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset   | Access | Description |
|-------|----------|---|--------|-------------|
| 31:16 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |             |

15:0    LOCKKEY    0x0000    RW    **Regulator and Supply Configuration Lock Key**

Write any other value than the unlock code to lock all regulator control registers, from editing. Write the unlock code to unlock. When reading the register, bit 0 is set when the lock is enabled. Registers that are locked: PWRCFG, PWRCTRL and DCDC\* registers.

| Mode            | Value  | Description                          |
|-----------------|--------|--------------------------------------|
| Read Operation  |        |                                      |
| UNLOCKED        | 0      | EMU Regulator registers are unlocked |
| LOCKED          | 1      | EMU Regulator registers are locked   |
| Write Operation |        |                                      |
| LOCK            | 0      | Lock EMU Regulator registers         |
| UNLOCK          | 0xADE8 | Unlock EMU Regulator registers       |

## 11.5.14 EMU\_PWRCTRL - Power Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                    |    |    |    |   |           |   |   |   |   |       |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------------|----|----|----|---|-----------|---|---|---|---|-------|---|---|---|--|
| 0x03C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13                 | 12 | 11 | 10 | 9 | 8         | 7 | 6 | 5 | 4 | 3     | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                  |    |    |    |   | 0         |   |   |   |   | 0     |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW                 |    |    |    |   | RW        |   |   |   |   | RW    |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | IMMEDIATEPWRSWITCH |    |    |    |   | REGPWRSEL |   |   |   |   | ANASW |   |   |   |  |

| Bit   | Name               | Reset  | Access | Description   |       |      |             |   |      |  |   |      |  |
|-------|--------------------|--|--------|---|-------|------|-------------|---|------|--|---|------|--|
| 31:14 | Reserved           | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i>            |        |   |       |      |             |   |      |  |   |      |  |
| 13    | IMMEDIATEPWRSWITCH | 0  | RW     | <p><b>Allows Immediate Switching of ANASW and REGPWRSEL Bit-fields</b></p> <p>When set, allows immediate ANASW/REGPWRSEL switching. When cleared, Hardware protects switching of ANASW/REGPWRSEL and switching is applied by hardware only when DCDC is stable</p>  |       |      |             |   |      |  |   |      |  |
| 12:11 | Reserved           | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i>            |        |   |       |      |             |   |      |  |   |      |  |
| 10    | REGPWRSEL          | 0  | RW     | <p><b>This Field Selects the Input Supply Pin for the Digital LDO</b></p> <p>Determines the power supply input used by the Digital LDO. Firmware should select DVDD as the input after startup. If DCDC is not configured to drive DVDD, IMMEDIATEPWRSWITCH needs to be set to prior to setting this bit to immediately make the switch. If DCDC is configured to drive DVDD, hardware will make the switch to DVDD only when DCDC is stable</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>AVDD</td> <td>The AVDD pin is the supply for the digital LDO. LDO current is limited to 20 mA in this configuration.</td> </tr> <tr> <td>1</td> <td>DVDD</td> <td>The DVDD pin is the supply for the digital LDO. Firmware should set REGPWRSEL=1 after startup, before increasing the core clock frequency.</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | AVDD | The AVDD pin is the supply for the digital LDO. LDO current is limited to 20 mA in this configuration. | 1 | DVDD | The DVDD pin is the supply for the digital LDO. Firmware should set REGPWRSEL=1 after startup, before increasing the core clock frequency. |
| Value | Mode               | Description  |        |   |       |      |             |   |      |  |   |      |  |
| 0     | AVDD               | The AVDD pin is the supply for the digital LDO. LDO current is limited to 20 mA in this configuration.                                     |        |   |       |      |             |   |      |  |   |      |  |
| 1     | DVDD               | The DVDD pin is the supply for the digital LDO. Firmware should set REGPWRSEL=1 after startup, before increasing the core clock frequency. |        |   |       |      |             |   |      |  |   |      |  |
| 9:6   | Reserved           | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i>            |        |   |       |      |             |   |      |  |   |      |  |
| 5     | ANASW              | 0  | RW     | <p><b>Analog Switch Selection</b></p> <p>Determines the power supply routed to the analog supply (VDDX_ANA) used by the analog peripherals (e.g., ULFRCO, LFRCO, LFXO, HFRCO, AUXHFRCO, VMON, IDAC, and ADC). Reset with POR, Hard Pin Reset, or BOD Reset. If DCDC is not configured to drive DVDD, IMMEDIATEPWRSWITCH needs to be set to prior to setting this bit to immediately make the switch. If DCDC is configured to drive DVDD, hardware will make the switch to DVDD only when DCDC is stable</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>AVDD</td> <td>Select AVDD as the analog power supply</td> </tr> <tr> <td>1</td> <td>DVDD</td> <td>Select DVDD as the analog power supply</td> </tr> </tbody> </table>   | Value | Mode | Description | 0 | AVDD | Select AVDD as the analog power supply   | 1 | DVDD | Select DVDD as the analog power supply   |
| Value | Mode               | Description  |        |   |       |      |             |   |      |  |   |      |  |
| 0     | AVDD               | Select AVDD as the analog power supply   |        |   |       |      |             |   |      |  |   |      |  |
| 1     | DVDD               | Select DVDD as the analog power supply   |        |   |       |      |             |   |      |  |   |      |  |
| 4:0   | Reserved           | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i>            |        |   |       |      |             |   |      |  |   |      |  |

### 11.5.15 EMU\_DCDCCTRL - DCDC Control

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |             |              |   |   |          |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|-------------|--------------|---|---|----------|---|
| 0x040         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5           | 4            | 3 | 2 | 1        | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | 1           | 1            |   |   | 0x3      |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | RW          | RW           |   |   | RW       |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | DCDCMODEEM4 | DCDCMODEEM23 |   |   | DCDCMODE |   |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 31:6 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 5    | DCDCMODEEM4     | 1   | RW     | <b>DCDC Mode EM4H</b><br><br>Determines the DCDC mode in EM4H. This bit is ignored if DCDCMODE=Bypass. Reset with POR, Hard Pin Reset, or BOD Reset.  |
|      | Value           | Mode  |        | Description   |
|      | 0               | EM4SW   |        | DCDC mode is according to DCDCMODE field.   |
|      | 1               | EM4LOWPOWER   |        | DCDC mode is low power.   |
| 4    | DCDCMODEEM23    | 1   | RW     | <b>DCDC Mode EM23</b><br><br>Determines the DCDC mode in EM2 and EM3. This bit is ignored if DCDCMODE=Bypass. Reset with POR, Hard Pin Reset, or BOD Reset.                                     |
|      | Value           | Mode  |        | Description   |
|      | 0               | EM23SW  |        | DCDC mode is according to DCDCMODE field.   |
|      | 1               | EM23LOWPOWER  |        | DCDC mode is low power.   |
| 3:2  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 1:0  | DCDCMODE        | 0x3   | RW     | <b>Regulator Mode</b><br><br>Determines the operating mode of the DCDC regulator. Reset with POR, Hard Pin Reset, or BOD Reset.   |
|      | Value           | Mode  |        | Description   |
|      | 0               | BYPASS  |        | DCDC regulator is operating in bypass mode. Prior to configuring DCDCMODE=BYPASS, software must set EMU_DCDCCLIMCTRL.BYPLIMEN=1 to prevent excessive current between VREGVDD and DVDD supplies. |
|      | 1               | LOWNOISE  |        | DCDC regulator is operating in low noise mode.  |
|      | 2               | LOWPOWER  |        | DCDC regulator is operating in low power mode.  |
|      | 3               | OFF   |        | DCDC regulator is off and the bypass switch is off. Note: DVDD must be supplied externally  |

## 11.5.16 EMU\_DCDCMISCCTRL - DCDC Miscellaneous Control Register

| Offset        | Bit Position |    |                 |    |    |              |    |    |    |              |    |    |    |           |    |    |    |         |    |    |    |         |   |   |   |   |               |   |   |   |   |            |             |            |
|---------------|--------------|----|-----------------|----|----|--------------|----|----|----|--------------|----|----|----|-----------|----|----|----|---------|----|----|----|---------|---|---|---|---|---------------|---|---|---|---|------------|-------------|------------|
| 0x04C         | 31           | 30 | 29              | 28 | 27 | 26           | 25 | 24 | 23 | 22           | 21 | 20 | 19 | 18        | 17 | 16 | 15 | 14      | 13 | 12 | 11 | 10      | 9 | 8 | 7 | 6 | 5             | 4 | 3 | 2 | 1 | 0          |             |            |
| <b>Reset</b>  |              |    | 0x0             |    |    | 0x3          |    |    |    | 0x1          |    |    |    | 0x0       |    |    |    | 0x7     |    |    |    | 0x7     |   |   |   |   | 0             |   |   |   |   |            | 0           |            |
| <b>Access</b> |              |    | RW              |    |    | RW           |    |    |    | RW           |    |    |    | RW        |    |    |    | RW      |    |    |    | RW      |   |   |   |   | RW            |   |   |   |   |            | RW          |            |
| <b>Name</b>   |              |    | LPCMPBIASEM234H |    |    | LNCLIMLIMSEL |    |    |    | LPCLIMLIMSEL |    |    |    | BYPLIMSEL |    |    |    | NFETCNT |    |    |    | PFETCNT |   |   |   |   | LNFORCECCMIMM |   |   |   |   | LPCMPHYSHI | LPCMPHYSDIS | LNFORCECCM |

| Bit   | Name            | Reset                                 | Access | Description  |       |      |             |   |       |                                      |   |       |                                       |   |       |                                       |   |       |                                      |
|-------|-----------------|---------------------------------------|--------|--|-------|------|-------------|---|-------|--------------------------------------|---|-------|---------------------------------------|---|-------|---------------------------------------|---|-------|--------------------------------------|
| 31:30 | Reserved        |                                       |        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a>   |       |      |             |   |       |                                      |   |       |                                       |   |       |                                       |   |       |                                      |
| 29:28 | LPCMPBIASEM234H | 0x0                                   | RW     | <b>LP Mode Comparator Bias Selection for EM23 or EM4H</b><br>LP mode comparator bias selection. Reset with POR, Hard Pin Reset, or BOD Reset.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>BIAS0</td> <td>Maximum load current less than 75uA.</td> </tr> <tr> <td>1</td> <td>BIAS1</td> <td>Maximum load current less than 500uA.</td> </tr> <tr> <td>2</td> <td>BIAS2</td> <td>Maximum load current less than 2.5mA.</td> </tr> <tr> <td>3</td> <td>BIAS3</td> <td>Maximum load current less than 10mA.</td> </tr> </tbody> </table>  | Value | Mode | Description | 0 | BIAS0 | Maximum load current less than 75uA. | 1 | BIAS1 | Maximum load current less than 500uA. | 2 | BIAS2 | Maximum load current less than 2.5mA. | 3 | BIAS3 | Maximum load current less than 10mA. |
| Value | Mode            | Description                           |        |  |       |      |             |   |       |                                      |   |       |                                       |   |       |                                       |   |       |                                      |
| 0     | BIAS0           | Maximum load current less than 75uA.  |        |  |       |      |             |   |       |                                      |   |       |                                       |   |       |                                       |   |       |                                      |
| 1     | BIAS1           | Maximum load current less than 500uA. |        |  |       |      |             |   |       |                                      |   |       |                                       |   |       |                                       |   |       |                                      |
| 2     | BIAS2           | Maximum load current less than 2.5mA. |        |  |       |      |             |   |       |                                      |   |       |                                       |   |       |                                       |   |       |                                      |
| 3     | BIAS3           | Maximum load current less than 10mA.  |        |  |       |      |             |   |       |                                      |   |       |                                       |   |       |                                       |   |       |                                      |
| 27    | Reserved        |                                       |        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a>   |       |      |             |   |       |                                      |   |       |                                       |   |       |                                       |   |       |                                      |
| 26:24 | LNCLIMLIMSEL    | 0x3                                   | RW     | <b>Current Limit Level Selection for Current Limiter in LN Mode</b><br>High-side current limiter's current limit level selection in low noise mode. The recommended setting is calculated by $LNCLIMLIMSEL = (I\_MAX + 40mA) * 1.5 / (5mA * (PFETCNT + 1)) - 1$ , where $I\_MAX$ is the maximum average current allowed to the load, and 40mA represents the current ripple with some margin, and the factor of 1.5 accounts for detecting error and other variations. For strong (i.e., low internal impedance) battery, it is recommended to have $I\_MAX = 200mA$ . $I\_MAX$ should never be set higher than 200mA to avoid reliability issues. Reset with POR, Hard Pin Reset, or BOD reset. |       |      |             |   |       |                                      |   |       |                                       |   |       |                                       |   |       |                                      |
| 23    | Reserved        |                                       |        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a>   |       |      |             |   |       |                                      |   |       |                                       |   |       |                                       |   |       |                                      |
| 22:20 | LPCLIMLIMSEL    | 0x1                                   | RW     | <b>Current Limit Level Selection for Current Limiter in LP Mode</b><br>Sets high-side current limit in low power mode, with maximum current equal to $40 mA * (1 + LPCLIMLIMSEL)$ . Recommend setting $LPCLIMLIMSEL = 1$ , corresponding to a maximum current of 80 mA for optimal efficiency and to support up to 10 mA loads when $LPCMPBIASEM234H = 0x3$ . Reset with POR, Hard Pin Reset, or BOD reset.  |       |      |             |   |       |                                      |   |       |                                       |   |       |                                       |   |       |                                      |
| 19:16 | BYPLIMSEL       | 0x0                                   | RW     | <b>Current Limit in Bypass Mode</b><br>Set current limit in bypass mode when $BYPLIMEN$ equals one. The limit is from 20mA to 320mA, with 20mA/step. Reset with POR, Hard Pin Reset, or BOD Reset.   |       |      |             |   |       |                                      |   |       |                                       |   |       |                                       |   |       |                                      |
| 15:12 | NFETCNT         | 0x7                                   | RW     | <b>NFET Switch Number Selection</b><br>Low Noise mode NFET power switch count number. The selected number of switches are $NFETCNT + 1$ . This may cause a very momentary efficiency hit. Reset with POR, Hard Pin Reset, or BOD Reset.  |       |      |             |   |       |                                      |   |       |                                       |   |       |                                       |   |       |                                      |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 11:8 | PFETCNT         | 0x7   | RW     | <b>PFET Switch Number Selection</b><br><br>Low Noise mode PFET power switch count number. The selected number of switches are PFETCNT+1. Reset with POR, Hard Pin Reset, or BOD Reset.  |
| 7:6  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 5    | LNFORCECCMIMM   | 0   | RW     | <b>Force DCDC Into CCM Mode Immediately, Based on LNFORCECCM</b><br><br>When set, this bit allows software to change LNFORCECCM bit and have the change take effect while DCDC is running. Otherwise, LNFORCECCM must be programmed prior to enabling the DCDC.   |
| 4:3  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 2    | LPCMPHYSHI      | 1   | RW     | <b>Comparator Threshold on the High Side</b><br><br>Reserved for internal use. Should always be set to 1.   |
| 1    | LPCMPHYSDIS     | 1   | RW     | <b>Disable LP Mode Hysteresis in the State Machine Control</b><br><br>Reserved for internal use. Should always be set to 1.   |
| 0    | LNFORCECCM      | 0   | RW     | <b>Force DCDC Into CCM Mode in Low Noise Operation</b><br><br>When this bit is set to 0 in low noise mode, the zero detector is configured as zero-crossing detector and the DCDC will be in forced CCM mode. The threshold set by ZDETILIMSEL will be ignored. When this bit is set to 1 in low noise mode, the zero detector is configured as reverse-current limiter and the DCDC will be in DCM mode. The reverse current limit level is set by ZDETILIMSEL. In low power mode, the zero detector is always configured as zero-crossing detector. Reset with POR, Hard Pin Reset, or BOD reset. |

11.5.17 EMU\_DCDCZDETCTRL - DCDC Power Train NFET Zero Current Detector Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |              |   |            |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|--------------|---|------------|---|---|---|---|---|---|
| 0x050         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8            | 7 | 6          | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | 0x1          |   | 0x5        |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | RW           |   | RW         |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | ZDETBLANKDLY |   | ZDETILMSEL |   |   |   |   |   |   |

| Bit   | Name         | Reset   | Access | Description  |
|-------|--------------|---|--------|--|
| 31:10 | Reserved     | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 9:8   | ZDETBLANKDLY | 0x1   | RW     | <b>Reserved for internal use. Do not change.</b><br>Reserved for internal use. Do not change.  |
| 7     | Reserved     | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 6:4   | ZDETILMSEL   | 0x5   | RW     | <b>Reverse Current Limit Level Selection for Zero Detector</b><br><br>Zero detector is reconfigured as low-side reverse current limiter when LNFORCECCM=1 in LN mode. The configuration of this register is calculated by the allowed average reverse current I_RMAX through the equation: $ZDETILMSEL = (I\_RMAX + 40mA) * 1.5 / (2.5mA * (NFETCNT + 1))$ , where 40mA represents the current ripple with some margin, and the factor of 1.5 accounts for detecting error and other variations. When the battery can tolerate large reverse current, it is recommended to have I_RMAX=160mA to maximize ZDETILMSEL to 7 with NFETCNT=15. Note that when LNFORCECCM=1 but ZDETILMSEL=0, the DCDC's behavior will be very similar to when LNFORCECCM=0 - that is, the DCDC will be in DCM mode. When LNFORCECCM=0, the zero detector will only detect zero-crossings (reverse-current limit=0 mA) and this register is ignored. Reset with POR, Hard Pin Reset, or BOD reset. |
| 3:0   | Reserved     | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |

## 11.5.18 EMU\_DCDCLIMCTRL - DCDC Power Train PFET Current Limiter Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |    |    |    |   |              |   |   |   |   |   |   |   |   |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|---|--------------|---|---|---|---|---|---|---|---|--|--|
| 0x054         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13       | 12 | 11 | 10 | 9 | 8            | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0        |    |    |    |   | 0x1          |   |   |   |   |   |   |   |   |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW       |    |    |    |   | RW           |   |   |   |   |   |   |   |   |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | BYPLIMEN |    |    |    |   | CLIMBLANKDLY |   |   |   |   |   |   |   |   |  |  |

| Bit   | Name         | Reset   | Access | Description  |
|-------|--------------|---|--------|--|
| 31:14 | Reserved     | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 13    | BYPLIMEN     | 0   | RW     | <b>Bypass Current Limit Enable</b><br><br>Bypass current limit enable. Setting this bit limits maximum current drawn from DCDC input supply while DCDC is in BYPASS mode. Note that the device will see an additional ~10 µA of current draw when BYPLIMEN=1 and Bypass Mode is enabled. To prevent this excess current, applications should disable the Bypass Current Limit (BYPLIMEN=0) once the DVDD voltage has reached the main supply voltage in Bypass Mode. Reset with POR, Hard Pin Reset, or BOD Reset. |
| 12:10 | Reserved     | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 9:8   | CLIMBLANKDLY | 0x1   | RW     | <b>Reserved for internal use. Do not change.</b><br><br>Reserved for internal use. Do not change.  |
| 7:0   | Reserved     | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |

## 11.5.19 EMU\_DCDCLNCOMPCTRL - DCDC Low Noise Compensator Control Register

| Offset | Bit Position |    |    |    |          |    |    |    |          |    |    |    |          |    |    |    |          |    |    |    |          |    |   |   |    |   |   |   |          |   |   |   |
|--------|--------------|----|----|----|----------|----|----|----|----------|----|----|----|----------|----|----|----|----------|----|----|----|----------|----|---|---|----|---|---|---|----------|---|---|---|
| 0x058  | 31           | 30 | 29 | 28 | 27       | 26 | 25 | 24 | 23       | 22 | 21 | 20 | 19       | 18 | 17 | 16 | 15       | 14 | 13 | 12 | 11       | 10 | 9 | 8 | 7  | 6 | 5 | 4 | 3        | 2 | 1 | 0 |
| Reset  | 0x5          |    |    |    | 0x7      |    |    |    | 0x2      |    |    |    | 0x4      |    |    |    | 0x07     |    |    |    | 0x7      |    |   |   |    |   |   |   | 0x7      |   |   |   |
| Access | RW           |    |    |    | RW       |    |    |    | RW       |    |    |    | RW       |    |    |    | RW       |    |    |    | RW       |    |   |   | RW |   |   |   | RW       |   |   |   |
| Name   | COMPENC3     |    |    |    | COMPENC2 |    |    |    | COMPENC1 |    |    |    | COMPENR3 |    |    |    | COMPENR2 |    |    |    | COMPENR1 |    |   |   |    |   |   |   | COMPENR1 |   |   |   |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:28 | COMPENC3        | 0x5   | RW     | <b>Low Noise Mode Compensator C3 Trim Value</b><br>LN mode compensator C3 trim, 0.5pF-8pF in 0.5pF steps. Reset with POR, Hard Pin Reset, or BOD Reset.       |
| 27    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 26:24 | COMPENC2        | 0x7   | RW     | <b>Low Noise Mode Compensator C2 Trim Value</b><br>LN mode compensator C2 trim, 1pF-8pF in 1pF steps. Reset with POR, Hard Pin Reset, or BOD Reset.           |
| 23:22 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 21:20 | COMPENC1        | 0x2   | RW     | <b>Low Noise Mode Compensator C1 Trim Value</b><br>LN mode compensator C1 trim, 0.15pF-0.60pF in 0.15pF step. Reset with POR, Hard Pin Reset, or BOD Reset.   |
| 19:16 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 15:12 | COMPENR3        | 0x4   | RW     | <b>Low Noise Mode Compensator R3 Trim Value</b><br>LN mode compensator r3 trim, 5-80KOhm in 5Khom steps. Reset with POR, Hard Pin Reset, or BOD Reset.        |
| 11:9  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 8:4   | COMPENR2        | 0x07  | RW     | <b>Low Noise Mode Compensator R2 Trim Value</b><br>LN mode compensator r2 trim, 50-1600KOhm, in 50KOhm steps. Reset with POR, Hard Pin Reset, or BOD Reset.   |
| 3     | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 2:0   | COMPENR1        | 0x7   | RW     | <b>Low Noise Mode Compensator R1 Trim Value</b><br>LN mode compensator r1 trim, 500-1200kOhm, in 100KOhm steps. Reset with POR, Hard Pin Reset, or BOD Reset. |

11.5.20 EMU\_DCDCLNVCTRL - DCDC Low Noise Voltage Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x05C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LNVREF 0x71 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LNVREF RWH  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LNVREF      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset   | Access                | Description  |
|-------|----------|---|-----------------------|--|
| 31:15 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                       |  |
| 14:8  | LNVREF   | 0x71  | RWH                   | <b>Low Noise Mode VREF Trim</b><br><br>Low noise mode Vref trim. LNATT and LNVREF set the output of the DCDC to $3*(1+LNATT)*(235.48+3.226*LNVREF)$ . Customers should use the emlib functions for configuring this field. Reset with POR, Hard Pin Reset, or BOD Reset. |
| 7:2   | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                       |  |
| 1     | LNATT    | 0   | RW                    | <b>Low Noise Mode Feedback Attenuation</b><br><br>Low noise mode feedback attenuation. Customers should use the emlib functions for configuring this field. Reset with POR, Hard Pin Reset, or BOD Reset.  |
|       | Value    | Mode  | Description           |  |
|       | 0        | DIV3  | Feedback Ratio is 1/3 |  |
|       | 1        | DIV6  | Feedback Ratio is 1/6 |  |
| 0     | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                       |  |

11.5.21 EMU\_DCDCLPVCTRL - DCDC Low Power Voltage Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |        |   |   |   |       |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|--------|---|---|---|-------|---|---|---|
| 0x064         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3     | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0xB4   |   |   |   | 0     |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RW     |   |   |   | RW    |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | LPVREF |   |   |   | LPATT |   |   |   |

| Bit   | Name     | Reset   | Access | Description  |       |      |             |   |      |                       |   |      |                       |
|-------|----------|---|--------|--|-------|------|-------------|---|------|-----------------------|---|------|-----------------------|
| 31:9  | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |      |                       |   |      |                       |
| 8:1   | LPVREF   | 0xB4  | RW     | <p><b>LP Mode Reference Selection for EM23 and EM4H</b></p> <p>Select Vref level. Maximum available code is 8'b11100111. LPATT and LPVREFSEL set the output of the DCDC to <math>4 \cdot (1 + LPATT) \cdot (30 + LPVREF) \cdot 2.2\text{mV}</math>. Customers should use the emlib functions for configuring this field. Reset with POR, Hard Pin Reset, or BOD Reset.</p>   |       |      |             |   |      |                       |   |      |                       |
| 0     | LPATT    | 0   | RW     | <p><b>Low Power Feedback Attenuation</b></p> <p>Low power feedback attenuation select. Customers should use the emlib functions for configuring this field. Reset with POR, Hard Pin Reset, or BOD Reset.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>DIV4</td> <td>Feedback Ratio is 1/4</td> </tr> <tr> <td>1</td> <td>DIV8</td> <td>Feedback Ratio is 1/8</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | DIV4 | Feedback Ratio is 1/4 | 1 | DIV8 | Feedback Ratio is 1/8 |
| Value | Mode     | Description   |        |  |       |      |             |   |      |                       |   |      |                       |
| 0     | DIV4     | Feedback Ratio is 1/4   |        |  |       |      |             |   |      |                       |   |      |                       |
| 1     | DIV8     | Feedback Ratio is 1/8   |        |  |       |      |             |   |      |                       |   |      |                       |

## 11.5.22 EMU\_DCDCLPCTRL - DCDC Low Power Control Register

| Offset        | Bit Position |    |    |    |    |         |              |    |    |    |    |    |    |    |    |    |    |                    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|---------|--------------|----|----|----|----|----|----|----|----|----|----|--------------------|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x06C         | 31           | 30 | 29 | 28 | 27 | 26      | 25           | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14                 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    | 0x1     | 1            |    |    |    |    |    |    |    |    |    |    | 0x0                |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    | RW      | RW           |    |    |    |    |    |    |    |    |    |    | RW                 |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    | LPBLANK | LPVREFDUTYEN |    |    |    |    |    |    |    |    |    |    | LPCMPHYSSSELEM234H |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name                    | Reset   | Access | Description   |
|-------|-------------------------|---|--------|---|
| 31:27 | Reserved                | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 26:25 | LPBLANK                 | 0x1   | RW     | <b>Reserved for internal use. Do not change.</b><br>Reserved for internal use. Do not change.   |
| 24    | LPVREFDUTYEN            | 1   | RW     | <b>LP Mode Duty Cycling Enable</b><br>Allow duty cycling of the bias. This is to minimize DC bias. Reset with POR, Hard Pin Reset, or BOD Reset.  |
| 23:16 | Reserved                | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 15:12 | LPCMPHYSSSE-<br>LEM234H | 0x0   | RW     | <b>LP Mode Hysteresis Selection for EM23 and EM4H</b><br><br>User-programmable hysteresis level for the low power comparator. Hysteresis voltage at the output is $4 \cdot (1 + LPATT) \cdot LPCMPHYSSSEL \cdot 3.13\text{mv}$ . Customers should use the emlib functions for configuring this field. Reset with POR, Hard Pin Reset, or BOD Reset. |
| 11:0  | Reserved                | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |

## 11.5.23 EMU\_DCDCLNFREQCTRL - DCDC Low Noise Controller Frequency Control

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x070  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21      | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset  |              |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Access |              |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Name   |              |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|        | RCOTRIM      |    |    |    |    |    |    |    |    |    | RCOBAND |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|        | 0x10         |    |    |    |    |    |    |    |    |    | 0x0     |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|        | RW           |    |    |    |    |    |    |    |    |    | RW      |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset | Access | Description   |
|-------|----------|-------|--------|---|
| 31:29 | Reserved |       |        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a>  |
| 28:24 | RCOTRIM  | 0x10  | RW     | <b>Reserved for internal use. Do not change.</b><br>Reserved for internal use. Do not change.   |
| 23:3  | Reserved |       |        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a>  |
| 2:0   | RCOBAND  | 0x0   | RW     | <b>LN Mode RCO Frequency Band Selection</b><br>Low noise mode RCO frequency selection. 0~7: 3~8.95MHz, approximately 0.85MHz/step when the radio is disabled. 3~10MHz, 1MHz/step when the radio is enabled to match the clock frequency from the radio. Reset with POR, Hard Pin Reset, or BOD Reset. |

## 11.5.24 EMU\_DCDCSYNC - DCDC Read Status Register

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x078  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Access |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Name   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|        | DCDCCTRLBUSY |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name         | Reset | Access | Description  |
|------|--------------|-------|--------|--|
| 31:1 | Reserved     |       |        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a>   |
| 0    | DCDCCTRLBUSY | 0     | R      | <b>DCDC CTRL Register Transfer Busy</b><br>Indicates the status of the DCDCCTRL transfer to the EMU OSC clock domain. Software cannot re-write the DCDCCTRL register until this signal goes low. |

## 11.5.25 EMU\_VMONAVDDCTRL - VMON AVDD Channel Control

| Offset        | Bit Position |    |    |    |    |    |    |    |                 |    |    |    |               |    |    |    |                 |    |    |    |               |    |   |   |    |    |   |    |        |        |   |    |
|---------------|--------------|----|----|----|----|----|----|----|-----------------|----|----|----|---------------|----|----|----|-----------------|----|----|----|---------------|----|---|---|----|----|---|----|--------|--------|---|----|
| 0x090         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23              | 22 | 21 | 20 | 19            | 18 | 17 | 16 | 15              | 14 | 13 | 12 | 11            | 10 | 9 | 8 | 7  | 6  | 5 | 4  | 3      | 2      | 1 | 0  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    | 0x0             |    |    |    | 0x0           |    |    |    | 0x0             |    |    |    |               |    |   |   | 0  | 0  | 0 | 0  |        |        |   |    |
| <b>Access</b> |              |    |    |    |    |    |    |    | RW              |    |    |    | RW            |    |    |    | RW              |    |    |    |               |    |   |   | RW | RW |   | RW |        |        |   |    |
| <b>Name</b>   |              |    |    |    |    |    |    |    | RISETHRESCOARSE |    |    |    | RISETHRESFINE |    |    |    | FALLTHRESCOARSE |    |    |    | FALLTHRESFINE |    |   |   |    |    |   |    | FALLWU | RISEWU |   | EN |

| Bit   | Name             | Reset   | Access | Description   |
|-------|------------------|---|--------|---|
| 31:24 | <i>Reserved</i>  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 23:20 | RISETHRES-COARSE | 0x0   | RW     | <b>Rising Threshold Coarse Adjust</b><br>Check VMON section for programming the threshold value. Reset with SYSEXTENDEDRESETn.  |
| 19:16 | RISETHRESFINE    | 0x0   | RW     | <b>Rising Threshold Fine Adjust</b><br>Check VMON section for programming the threshold value. Reset with SYSEXTENDEDRESETn.    |
| 15:12 | FALLTHRES-COARSE | 0x0   | RW     | <b>Falling Threshold Coarse Adjust</b><br>Check VMON section for programming the threshold value. Reset with SYSEXTENDEDRESETn. |
| 11:8  | FALLTHRESFINE    | 0x0   | RW     | <b>Falling Threshold Fine Adjust</b><br>Check VMON section for programming the threshold value. Reset with SYSEXTENDEDRESETn.   |
| 7:4   | <i>Reserved</i>  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 3     | FALLWU           | 0   | RW     | <b>Fall Wakeup</b><br>When set, a wakeup from EM4H will take place upon a falling edge. Reset with SYSEXTENDEDRESETn.           |
| 2     | RISEWU           | 0   | RW     | <b>Rise Wakeup</b><br>When set, a wakeup from EM4H will take place upon a rising edge. Reset with SYSEXTENDEDRESETn.            |
| 1     | <i>Reserved</i>  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 0     | EN               | 0   | RW     | <b>Enable</b><br>Set this bit to enable the AVDD VMON. Reset with SYSEXTENDEDRESETn.  |

11.5.26 EMU\_VMONALTAVDDCTRL - Alternate VMON AVDD Channel Control

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |           |    |    |    |   |   |        |        |   |    |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|-----------|----|----|----|---|---|--------|--------|---|----|---|---|---|---|
| 0x094         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15          | 14 | 13        | 12 | 11 | 10 | 9 | 8 | 7      | 6      | 5 | 4  | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0         |    | 0x0       |    |    |    |   |   | 0      | 0      |   | 0  |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW          |    | RW        |    |    |    |   |   | RW     | RW     |   | RW |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | THRESCOARSE |    | THRESFINE |    |    |    |   |   | FALLWU | RISEWU |   | EN |   |   |   |   |

| Bit   | Name        | Reset   | Access | Description   |
|-------|-------------|---|--------|---|
| 31:16 | Reserved    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 15:12 | THRESCOARSE | 0x0   | RW     | <b>Threshold Coarse Adjust</b><br>Check VMON section for programming the threshold value. Reset with SYSEXTENDEDRESETn. |
| 11:8  | THRESFINE   | 0x0   | RW     | <b>Threshold Fine Adjust</b><br>Check VMON section for programming the threshold value. Reset with SYSEXTENDEDRESETn.   |
| 7:4   | Reserved    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 3     | FALLWU      | 0   | RW     | <b>Fall Wakeup</b><br>When set, a wakeup from EM4H will take place upon a falling edge. Reset with SYSEXTENDEDRESETn.   |
| 2     | RISEWU      | 0   | RW     | <b>Rise Wakeup</b><br>When set, a wakeup from EM4H will take place upon a rising edge. Reset with SYSEXTENDEDRESETn.    |
| 1     | Reserved    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 0     | EN          | 0   | RW     | <b>Enable</b><br>Set this bit to enable the ALTAVDD VMON. Reset with SYSEXTENDEDRESETn.                                 |

## 11.5.27 EMU\_VMONDVDDCTRL - VMON DVDD Channel Control

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |           |    |    |    |        |        |   |    |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|-----------|----|----|----|--------|--------|---|----|---|---|---|---|---|---|
| 0x098         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15          | 14 | 13        | 12 | 11 | 10 | 9      | 8      | 7 | 6  | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0         |    | 0x0       |    |    |    | 0      | 0      |   | 0  |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW          |    | RW        |    |    |    | RW     | RW     |   | RW |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | THRESCOARSE |    | THRESFINE |    |    |    | FALLWU | RISEWU |   | EN |   |   |   |   |   |   |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:16 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 15:12 | THRESCOARSE     | 0x0   | RW     | <b>Threshold Coarse Adjust</b><br>Check VMON section for programming the threshold value. Reset with SYSEXTENDEDRESETn. |
| 11:8  | THRESFINE       | 0x0   | RW     | <b>Threshold Fine Adjust</b><br>Check VMON section for programming the threshold value. Reset with SYSEXTENDEDRESETn.   |
| 7:4   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 3     | FALLWU          | 0   | RW     | <b>Fall Wakeup</b><br>When set, a wakeup from EM4H will take place upon a falling edge. Reset with SYSEXTENDEDRESETn.   |
| 2     | RISEWU          | 0   | RW     | <b>Rise Wakeup</b><br>When set, a wakeup from EM4H will take place upon a rising edge. Reset with SYSEXTENDEDRESETn.    |
| 1     | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 0     | EN              | 0   | RW     | <b>Enable</b><br>Set this bit to enable the DVDD VMON. Reset with SYSEXTENDEDRESETn.                                    |

## 11.5.28 EMU\_VMONIO0CTRL - VMON IOVDD0 Channel Control

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |           |    |    |    |        |        |        |    |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|-----------|----|----|----|--------|--------|--------|----|---|---|---|---|---|---|
| 0x09C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15          | 14 | 13        | 12 | 11 | 10 | 9      | 8      | 7      | 6  | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0         |    | 0x0       |    |    |    | 0      | 0      | 0      | 0  |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW          |    | RW        |    |    |    | RW     | RW     | RW     |    |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | THRESCOARSE |    | THRESFINE |    |    |    | RETDIS | FALLWU | RISEWU | EN |   |   |   |   |   |   |

| Bit   | Name        | Reset   | Access | Description   |
|-------|-------------|---|--------|---|
| 31:16 | Reserved    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 15:12 | THRESCOARSE | 0x0   | RW     | <b>Threshold Coarse Adjust</b><br>Check VMON section for programming the threshold value. Reset with SYSEXTENDEDRESETn.   |
| 11:8  | THRESFINE   | 0x0   | RW     | <b>Threshold Fine Adjust</b><br>Check VMON section for programming the threshold value. Reset with SYSEXTENDEDRESETn.   |
| 7:5   | Reserved    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 4     | RETDIS      | 0   | RW     | <b>EM4 IO0 Retention Disable</b><br>When set, the IO0 Retention will be disabled when this IO0 voltage drops below the threshold set. Reset with SYSEXTENDEDRESETn. |
| 3     | FALLWU      | 0   | RW     | <b>Fall Wakeup</b><br>When set, a wakeup from EM4H will take place upon a falling edge. Reset with SYSEXTENDEDRESETn.   |
| 2     | RISEWU      | 0   | RW     | <b>Rise Wakeup</b><br>When set, a wakeup from EM4H will take place upon a rising edge. Reset with SYSEXTENDEDRESETn.  |
| 1     | Reserved    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 0     | EN          | 0   | RW     | <b>Enable</b><br>Set this bit to enable the IO0 VMON. Reset with SYSEXTENDEDRESETn.   |

11.5.29 EMU\_RAM1CTRL - Memory Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |              |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|--------------|----|
| 0x0B0         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1            | 0  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | 1            | 0  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | RW           | RW |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | RAMPOWERDOWN |    |

| Bit  | Name            | Reset   | Access  | Description  |
|------|-----------------|---|---|--|
| 31:2 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 1:0  | RAMPOWERDOWN    | 0x0   | RW  | <b>RAM1 Blockset Power-down</b><br>RAM blockset power-down in EM23 with full access in EM01. |
|      | Value           | Mode  | Description   |  |
|      | 0               | NONE  | None of the RAM blocks powered down                             |  |
|      | 2               | BLK1  | Power down RAM block 1 (address range 0x20030000-0x2003FFFF)    |  |
|      | 3               | BLK0TO1   | Power down RAM blocks 0-1 (address range 0x20020000-0x2003FFFF) |  |

11.5.30 EMU\_RAM2CTRL - Memory Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |              |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|--------------|
| 0x0B4         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0            |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0x0          |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | RW           |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | RAMPOWERDOWN |

| Bit  | Name         | Reset  | Access | Description  |      |       |             |      |      |                                     |     |     |   |
|------|--------------|--|--------|--|------|-------|-------------|------|------|-------------------------------------|-----|-----|---|
| 31:1 | Reserved     | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |      |       |             |      |      |                                     |     |     |   |
| 0:0  | RAMPOWERDOWN | 0x0  | RW     | <p><b>RAM2 Blockset Power-down</b></p> <p>RAM blockset power-down in EM23 with full access in EM01.</p> <table border="1"> <thead> <tr> <th>Mode</th> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>NONE</td> <td>0x00</td> <td>None of the RAM blocks powered down</td> </tr> <tr> <td>BLK</td> <td>0x1</td> <td>Power down RAM blocks 0-3 (address range 0x20040000-0x200407FF)</td> </tr> </tbody> </table> | Mode | Value | Description | NONE | 0x00 | None of the RAM blocks powered down | BLK | 0x1 | Power down RAM blocks 0-3 (address range 0x20040000-0x200407FF) |
| Mode | Value        | Description  |        |  |      |       |             |      |      |                                     |     |     |   |
| NONE | 0x00         | None of the RAM blocks powered down  |        |  |      |       |             |      |      |                                     |     |     |   |
| BLK  | 0x1          | Power down RAM blocks 0-3 (address range 0x20040000-0x200407FF)  |        |  |      |       |             |      |      |                                     |     |     |   |

### 11.5.31 EMU\_DCDCLPEM01CFG - Configuration Bits for Low Power Mode to Be Applied During EM01, This Field is Only Relevant If LP Mode is Used in EM01

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                 |    |    |    |               |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------------|----|----|----|---------------|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|--|--|
| 0x0E0         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15              | 14 | 13 | 12 | 11            | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0             |    |    |    | 0x3           |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW              |    |    |    | RW            |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LPCMPHYSSELEM01 |    |    |    | LPCMPBIASEM01 |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |

| Bit   | Name                 | Reset   | Access                                | Description  |
|-------|----------------------|---|---------------------------------------|--|
| 31:16 | Reserved             | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                       |  |
| 15:12 | LPCMPHYSSE-<br>LEM01 | 0x0   | RW                                    | <b>LP Mode Hysteresis Selection for EM01</b><br><br>LP mode hysteresis voltage in at the output is $4*(1+LPATT)*LPCMPHYSSEL*3.13mV$ . Customers should use the emlib functions for configuring this field. |
| 11:10 | Reserved             | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                       |  |
| 9:8   | LPCMPBIASEM01        | 0x3   | RW                                    | <b>LP Mode Comparator Bias Selection for EM01</b><br><br>Reserved for internal use. Do not change.   |
|       | Value                | Mode  | Description                           |  |
|       | 0                    | BIAS0   | Maximum load current less than 75uA.  |  |
|       | 1                    | BIAS1   | Maximum load current less than 500uA. |  |
|       | 2                    | BIAS2   | Maximum load current less than 2.5mA. |  |
|       | 3                    | BIAS3   | Maximum load current less than 10mA.  |  |
| 7:0   | Reserved             | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                       |  |

## 11.5.32 EMU\_EM23PERNORETAINCMD - Clears Corresponding Bits in EM23PERNORETAINSTATUS Unlocking Access to Peripheral

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |           |                |             |             |                |            |             |            |            |            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |             |             |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|-----------|----------------|-------------|-------------|----------------|------------|-------------|------------|------------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|-------------|-------------|
| 0x0F4         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15            | 14        | 13             | 12          | 11          | 10             | 9          | 8           | 7          | 6          | 5          | 4  | 3  | 2  | 1  | 0  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |             |             |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0             | 0         | 0              | 0           | 0           | 0              | 0          | 0           | 0          | 0          | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |             |             |             |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W1            | W1        | W1             | W1          | W1          | W1             | W1         | W1          | W1         | W1         | W1         | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1          | W1          |             |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LEUART0UNLOCK | CSEUNLOCK | LESENSE0UNLOCK | WDOG1UNLOCK | WDOG0UNLOCK | LETIMER0UNLOCK | ADC0UNLOCK | IDAC0UNLOCK | DAC0UNLOCK | I2C1UNLOCK | I2C0UNLOCK |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PCNT0UNLOCK | ACMP1UNLOCK | ACMP0UNLOCK |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:16 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 15    | LEUART0UNLOCK   | 0   | W1     | <b>Clears Status Bit of LEUART0 and Unlocks Access to It</b><br>clears status bit of LEUART0 and unlocks access to it   |
| 14    | CSEUNLOCK       | 0   | W1     | <b>Clears Status Bit of CSEN and Unlocks Access to It</b><br>clears status bit of CSEN and unlocks access to it         |
| 13    | LESENSE0UNLOCK  | 0   | W1     | <b>Clears Status Bit of LESENSE0 and Unlocks Access to It</b><br>clears status bit of LESENSE0 and unlocks access to it |
| 12    | WDOG1UNLOCK     | 0   | W1     | <b>Clears Status Bit of WDOG1 and Unlocks Access to It</b><br>clears status bit of WDOG1 and unlocks access to it       |
| 11    | WDOG0UNLOCK     | 0   | W1     | <b>Clears Status Bit of WDOG0 and Unlocks Access to It</b><br>clears status bit of WDOG0 and unlocks access to it       |
| 10    | LETIMER0UNLOCK  | 0   | W1     | <b>Clears Status Bit of LETIMER0 and Unlocks Access to It</b><br>clears status bit of LETIMER0 and unlocks access to it |
| 9     | ADC0UNLOCK      | 0   | W1     | <b>Clears Status Bit of ADC0 and Unlocks Access to It</b><br>clears status bit of ADC0 and unlocks access to it         |
| 8     | IDAC0UNLOCK     | 0   | W1     | <b>Clears Status Bit of IDAC0 and Unlocks Access to It</b><br>clears status bit of IDAC0 and unlocks access to it       |
| 7     | DAC0UNLOCK      | 0   | W1     | <b>Clears Status Bit of DAC0 and Unlocks Access to It</b><br>clears status bit of DAC0 and unlocks access to it         |
| 6     | I2C1UNLOCK      | 0   | W1     | <b>Clears Status Bit of I2C1 and Unlocks Access to It</b><br>clears status bit of I2C1 and unlocks access to it         |
| 5     | I2C0UNLOCK      | 0   | W1     | <b>Clears Status Bit of I2C0 and Unlocks Access to It</b><br>clears status bit of I2C0 and unlocks access to it         |
| 4:3   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |

| Bit | Name        | Reset | Access | Description   |
|-----|-------------|-------|--------|---|
| 2   | PCNT0UNLOCK | 0     | W1     | <b>Clears Status Bit of PCNT0 and Unlocks Access to It</b><br>clears status bit of PCNT0 and unlocks access to it |
| 1   | ACMP1UNLOCK | 0     | W1     | <b>Clears Status Bit of ACMP1 and Unlocks Access to It</b><br>clears status bit of ACMP1 and unlocks access to it |
| 0   | ACMP0UNLOCK | 0     | W1     | <b>Clears Status Bit of ACMP0 and Unlocks Access to It</b><br>clears status bit of ACMP0 and unlocks access to it |

**11.5.33 EMU\_EM23PERNORETAINSTATUS - Status Indicating If Peripherals Were Powered Down in EM23, Subsequently Locking Access to It**

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |            |                |             |             |                |            |             |            |            |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |             |             |             |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|------------|----------------|-------------|-------------|----------------|------------|-------------|------------|------------|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------|-------------|-------------|
| 0x0F8         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15            | 14         | 13             | 12          | 11          | 10             | 9          | 8           | 7          | 6          | 5          | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |             |             |             |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0             | 0          | 0              | 0           | 0           | 0              | 0          | 0           | 0          | 0          | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |             |             |             |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R             | R          | R              | R           | R           | R              | R          | R           | R          | R          | R          | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R           | R           |             |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LEUART0LOCKED | CSENLOCKED | LESENSE0LOCKED | WDOG1LOCKED | WDOG0LOCKED | LETIMER0LOCKED | ADC0LOCKED | IDAC0LOCKED | DAC0LOCKED | I2C1LOCKED | I2C0LOCKED |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | PCNT0LOCKED | ACMP1LOCKED | ACMP0LOCKED |

| Bit   | Name           | Reset | Access | Description   |
|-------|----------------|-------|--------|---|
| 31:16 | Reserved       |       |        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a>  |
| 15    | LEUART0LOCKED  | 0     | R      | <b>Indicates If LEUART0 Powered Down During EM23</b><br>Indicates if LEUART0 powered down during EM23. Access to this peripheral locked until this bit cleared using EM23PERNORETAINCMD   |
| 14    | CSENLOCKED     | 0     | R      | <b>Indicates If CSEN Powered Down During EM23</b><br>Indicates if CSEN powered down during EM23. Access to this peripheral locked until this bit cleared using EM23PERNORETAINCMD         |
| 13    | LESENSE0LOCKED | 0     | R      | <b>Indicates If LESENSE0 Powered Down During EM23</b><br>Indicates if LESENSE0 powered down during EM23. Access to this peripheral locked until this bit cleared using EM23PERNORETAINCMD |
| 12    | WDOG1LOCKED    | 0     | R      | <b>Indicates If WDOG1 Powered Down During EM23</b><br>Indicates if WDOG1 powered down during EM23. Access to this peripheral locked until this bit cleared using EM23PERNORETAINCMD       |
| 11    | WDOG0LOCKED    | 0     | R      | <b>Indicates If WDOG0 Powered Down During EM23</b><br>Indicates if WDOG0 powered down during EM23. Access to this peripheral locked until this bit cleared using EM23PERNORETAINCMD       |
| 10    | LETIMER0LOCKED | 0     | R      | <b>Indicates If LETIMER0 Powered Down During EM23</b><br>Indicates if LETIMER0 powered down during EM23. Access to this peripheral locked until this bit cleared using EM23PERNORETAINCMD |
| 9     | ADC0LOCKED     | 0     | R      | <b>Indicates If ADC0 Powered Down During EM23</b><br>Indicates if ADC0 powered down during EM23. Access to this peripheral locked until this bit cleared using EM23PERNORETAINCMD         |
| 8     | IDAC0LOCKED    | 0     | R      | <b>Indicates If IDAC0 Powered Down During EM23</b><br>Indicates if IDAC0 powered down during EM23. Access to this peripheral locked until this bit cleared using EM23PERNORETAINCMD       |
| 7     | DAC0LOCKED     | 0     | R      | <b>Indicates If DAC0 Powered Down During EM23</b><br>Indicates if DAC0 powered down during EM23. Access to this peripheral locked until this bit cleared using EM23PERNORETAINCMD         |

| Bit | Name            | Reset   | Access | Description   |
|-----|-----------------|---|--------|---|
| 6   | I2C1LOCKED      | 0   | R      | <b>Indicates If I2C1 Powered Down During EM23</b><br>Indicates if I2C1 powered down during EM23. Access to this peripheral locked until this bit cleared using EM23PERNORETAINCMD   |
| 5   | I2C0LOCKED      | 0   | R      | <b>Indicates If I2C0 Powered Down During EM23</b><br>Indicates if I2C0 powered down during EM23. Access to this peripheral locked until this bit cleared using EM23PERNORETAINCMD   |
| 4:3 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 2   | PCNT0LOCKED     | 0   | R      | <b>Indicates If PCNT0 Powered Down During EM23</b><br>Indicates if PCNT0 powered down during EM23. Access to this peripheral locked until this bit cleared using EM23PERNORETAINCMD |
| 1   | ACMP1LOCKED     | 0   | R      | <b>Indicates If ACMP1 Powered Down During EM23</b><br>Indicates if ACMP1 powered down during EM23. Access to this peripheral locked until this bit cleared using EM23PERNORETAINCMD |
| 0   | ACMP0LOCKED     | 0   | R      | <b>Indicates If ACMP0 Powered Down During EM23</b><br>Indicates if ACMP0 powered down during EM23. Access to this peripheral locked until this bit cleared using EM23PERNORETAINCMD |

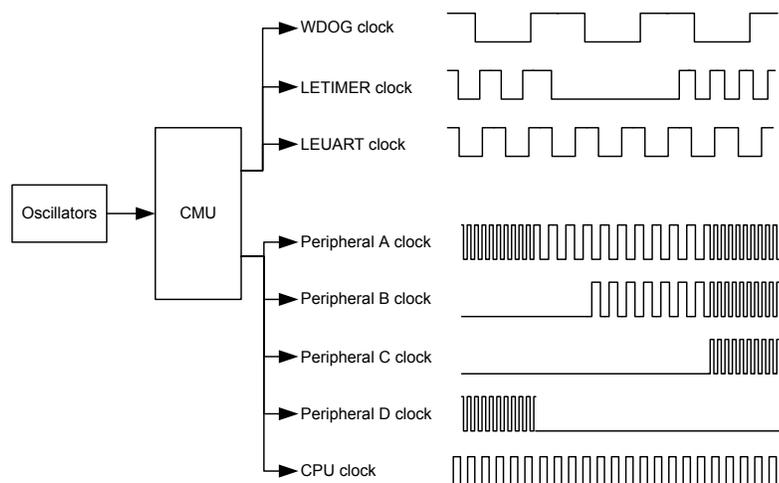
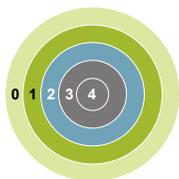
## 11.5.34 EMU\_EM23PERNORETAINCTRL - When Set Corresponding Peripherals May Get Powered Down in EM23

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |         |             |          |          |             |         |          |          |         |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |          |          |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|---------|-------------|----------|----------|-------------|---------|----------|----------|---------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|----------|----------|
| 0x0FC         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14      | 13          | 12       | 11       | 10          | 9       | 8        | 7        | 6       | 5       | 4  | 3  | 2  | 1  | 0  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |          |          |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0          | 0       | 0           | 0        | 0        | 0           | 0       | 0        | 0        | 0       | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |    |          |          |          |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW         | RW      | RW          | RW       | RW       | RW          | RW      | RW       | RW       | RW      | RW      | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW       |          |          |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LEUART0DIS | CSENDIS | LESENSE0DIS | WDOG1DIS | WDOG0DIS | LETIMER0DIS | ADC0DIS | IDAC0DIS | VDAC0DIS | I2C1DIS | I2C0DIS |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PCNT0DIS | ACMP1DIS | ACMP0DIS |

| Bit   | Name        | Reset  | Access | Description   |
|-------|-------------|--|--------|---|
| 31:16 | Reserved    | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 15    | LEUART0DIS  | 0  | RW     | <b>Allow Power Down of LEUART0 During EM23</b><br>Allow power down of LEUART0 during EM23   |
| 14    | CSENDIS     | 0  | RW     | <b>Allow Power Down of CSEN During EM23</b><br>Allow power down of CSEN during EM23         |
| 13    | LESENSE0DIS | 0  | RW     | <b>Allow Power Down of LESENSE0 During EM23</b><br>Allow power down of LESENSE0 during EM23 |
| 12    | WDOG1DIS    | 0  | RW     | <b>Allow Power Down of WDOG1 During EM23</b><br>Allow power down of WDOG1 during EM23       |
| 11    | WDOG0DIS    | 0  | RW     | <b>Allow Power Down of WDOG0 During EM23</b><br>Allow power down of WDOG0 during EM23       |
| 10    | LETIMER0DIS | 0  | RW     | <b>Allow Power Down of LETIMER0 During EM23</b><br>Allow power down of LETIMER0 during EM23 |
| 9     | ADC0DIS     | 0  | RW     | <b>Allow Power Down of ADC0 During EM23</b><br>Allow power down of ADC0 during EM23         |
| 8     | IDAC0DIS    | 0  | RW     | <b>Allow Power Down of IDAC0 During EM23</b><br>Allow power down of IDAC0 during EM23       |
| 7     | VDAC0DIS    | 0  | RW     | <b>Allow Power Down of DAC0 During EM23</b><br>Allow power down of DAC0 during EM23         |
| 6     | I2C1DIS     | 0  | RW     | <b>Allow Power Down of I2C1 During EM23</b><br>Allow power down of I2C1 during EM23         |
| 5     | I2C0DIS     | 0  | RW     | <b>Allow Power Down of I2C0 During EM23</b><br>Allow power down of I2C0 during EM23         |
| 4:3   | Reserved    | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 2     | PCNT0DIS    | 0  | RW     | <b>Allow Power Down of PCNT0 During EM23</b><br>Allow power down of PCNT0 during EM23       |

| Bit | Name     | Reset | Access | Description   |
|-----|----------|-------|--------|---|
| 1   | ACMP1DIS | 0     | RW     | <b>Allow Power Down of ACMP1 During EM23</b><br>Allow power down of ACMP1 during EM23 |
| 0   | ACMP0DIS | 0     | RW     | <b>Allow Power Down of ACMP0 During EM23</b><br>Allow power down of ACMP0 during EM23 |

## 12. CMU - Clock Management Unit



### Quick Facts

#### What?

The CMU controls oscillators and clocks. EFR32xG13 Wireless Gecko supports 6 different oscillators with minimized power consumption and short start-up time. The CMU has HW support for calibration of RC oscillators.

#### Why?

Oscillators and clocks contribute significantly to the power consumption of an MCU. Low power oscillators combined with a flexible clock control scheme make it possible to minimize the energy consumption in any given application.

#### How?

The CMU can configure different clock sources, enable/disable clocks to peripherals on an individual basis and set the prescaler for the different clocks. The short oscillator start-up times makes duty-cycling between active mode and the different low energy modes (EM2 Deep Sleep, EM3 Stop, and EM4 Hibernate/Shutoff) very efficient. The calibration feature ensures high accuracy RC oscillators. Several interrupts are available to avoid CPU polling of flags.

### 12.1 Introduction

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks in the EFR32xG13 Wireless Gecko. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that do not need to be active.

### 12.2 Features

- Multiple clock sources available:
  - 38 MHz - 40 MHz High Frequency Crystal Oscillator (HFXO)
  - 1 MHz - 38 MHz High Frequency RC Oscillator (HFRCO)
  - 1 MHz - 38 MHz Auxiliary High Frequency RC Oscillator (AUXHFRCO)
  - 32768 Hz Low Frequency Crystal Oscillator (LFXO)
  - 32768 Hz Low Frequency RC Oscillator (LFRCO)
  - 1000 Hz Ultra Low Frequency RC Oscillator (ULFRCO)
  - 32768 Hz Precision Low Frequency Oscillator (PLFRCO)
- All oscillator sources are low power.
- Fast start-up times.
- Separate prescalers for High Frequency Core Clocks (HFCORECLK), Radio Clocks (HFRADIOCLK), and Peripheral Clocks (HFPERCLK).
- Individual clock prescaler selection for each Low Energy Peripheral.
- Clock gating on an individual basis to core modules and all peripherals.
- Selectable clock output to external pins and/or PRS.
- Wakeup interrupt for LFRCO or LFXO ready allows entry into EM2 Deep Sleep while waiting for low-frequency oscillator startup. This avoids the need for software polling and saves power during oscillator startup.
- Auxiliary 1 MHz - 38 MHz RC oscillator (AUXHFRCO), which is asynchronous to the HFSRCCLK system clock, can be selected for ADC operation, LESENSE timing and debug trace.

### 12.3 Functional Description

An overview of the high frequency portion of the CMU is shown in [Figure 12.1 CMU Overview - High Frequency Portion on page 318](#). An overview of the low frequency portion is shown in [Figure 12.2 CMU Overview - Low Frequency Portion on page 319](#). These figures show the CMU for the largest device in the EFR32 family. Refer to the Configuration Summary in the device data sheet to see which core, radio, and peripheral modules, and therefore clock connections, are present in a specific device.

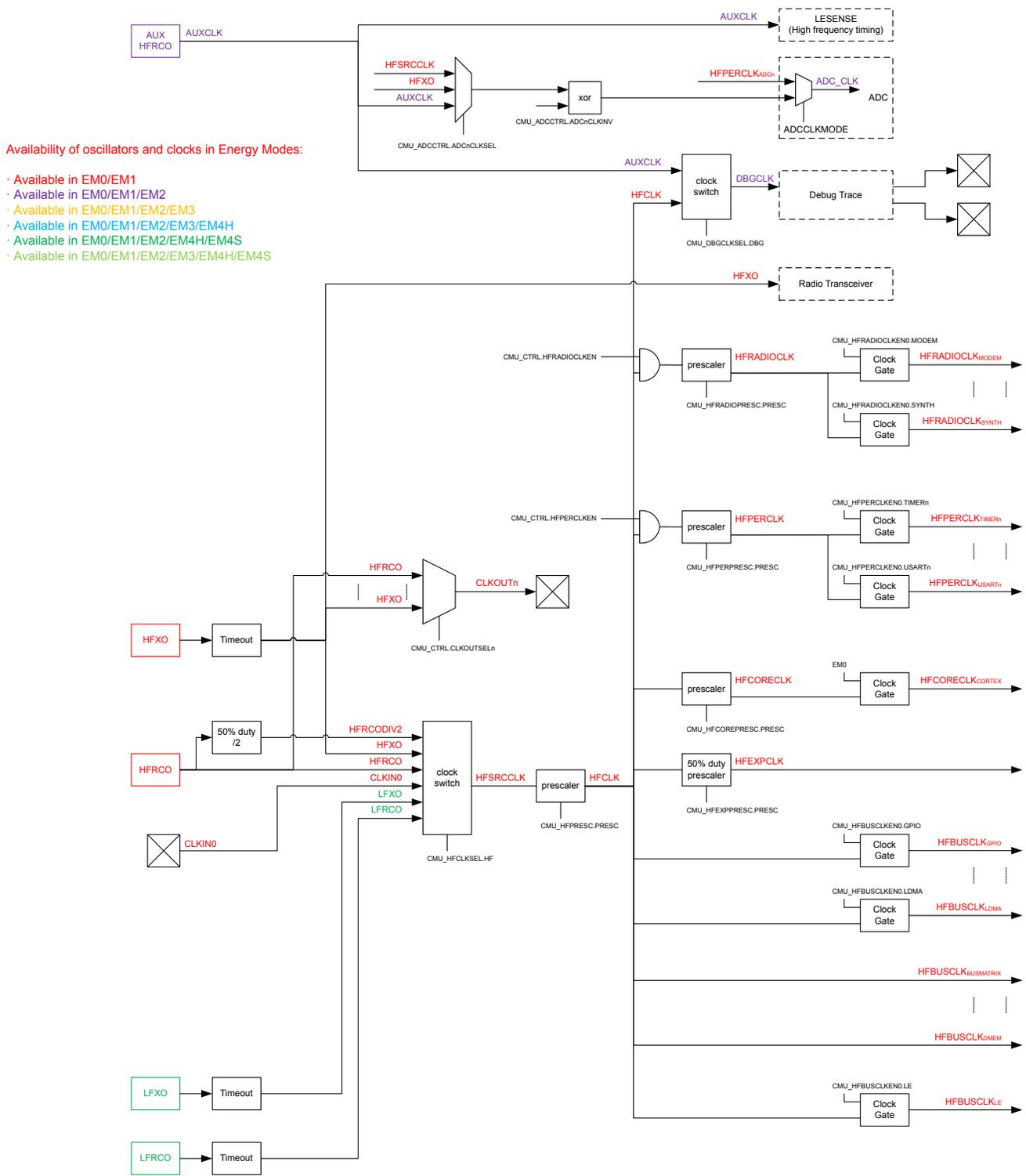
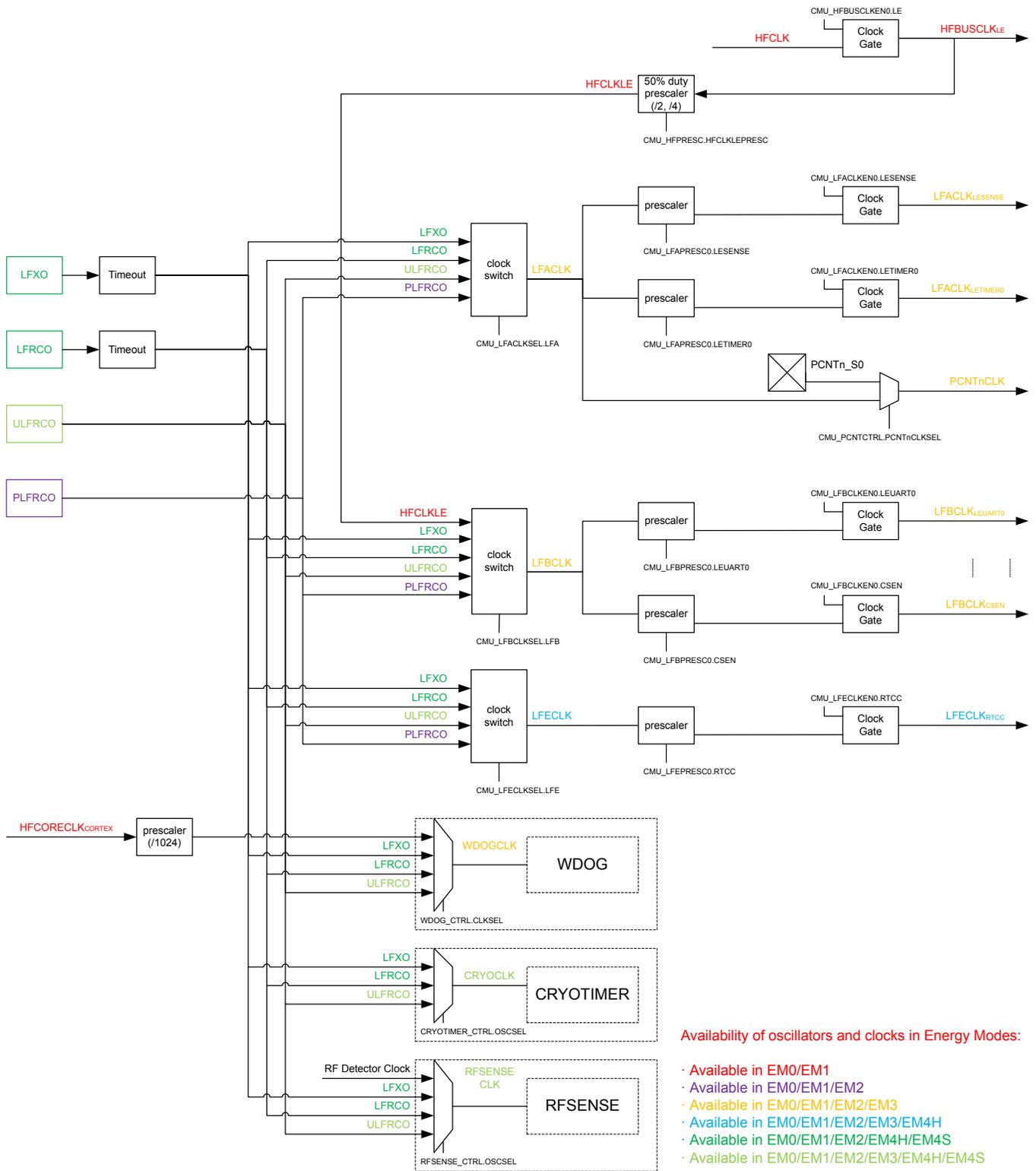


Figure 12.1. CMU Overview - High Frequency Portion



Availability of oscillators and clocks in Energy Modes:

- Available in EM0/EM1
- Available in EM0/EM1/EM2
- Available in EM0/EM1/EM2/EM3
- Available in EM0/EM1/EM2/EM3/EM4H
- Available in EM0/EM1/EM2/EM4H/EM4S
- Available in EM0/EM1/EM2/EM3/EM4H/EM4S

Figure 12.2. CMU Overview - Low Frequency Portion

### 12.3.1 System Clocks

Available system clock sources are detailed in the following sections.

### 12.3.1.1 HFCLK - High Frequency Clock

HFSRCCLK is the selected High Frequency Source Clock. HFCLK is an optionally prescaled version of HFSRCCLK. The HFSRCCLK, and therefore HFCLK, can be driven by a high-frequency oscillator, such as HFRCO or HFXO, or one of the low-frequency oscillators (LFRCO or LFXO). Additionally, HFSRCCLK can also be driven from a pin (CLKIN0) described in [12.3.6 Clock Input From a Pin](#). By default the HFRCO is selected. In most applications, one of the high frequency oscillators will be the preferred choice. To change the selected clock source, write to the HF bitfield in CMU\_HFCLKSEL. The high frequency clock source can also be changed automatically by hardware as explained in [12.3.2.4.1 Automatic HFXO Start](#). The currently selected source for HFSRCCLK and HFCLK can be read from CMU\_HFCLKSTATUS. The HFSRCCLK is running in EM0 Active and EM1 Sleep and is automatically stopped in EM2 Deep Sleep. During Voltage Scaling (see [11.3.9 Voltage Scaling](#)), if a fixed frequency oscillator source (i.e. HFXO or CLKIN0) exceeds the maximum system frequency supported, it must be disabled or not selected. Likewise, an adjustable oscillator source (i.e. HFRCO or AUXHFRCO) must be configured to not exceed the maximum system frequency supported before voltage scaling is applied.

**Note:** If a low frequency clock (i.e. LFRCO or LFXO) is selected as source clock for HFSRCCLK via the HF bitfield in CMU\_HFCLKSEL, then no register reads should be performed from Low Energy Peripherals for registers which can change value every clock cycle (e.g., a counter register). In addition to the peripherals on LFACLK, LFBCLK and LFECLK, this restriction applies in general to any low frequency peripheral, which is not directly or indirectly clocked from HFSRCCLK (e.g., WDOGn).

HFCLK can optionally be prescaled by setting PRESC in CMU\_HFPRESC to a non-zero value. This prescales HFCLK to all high frequency components and is typically used to save energy in applications where the system is not required to run at the highest frequency. The prescaler setting can be changed dynamically and the new setting takes effect immediately. HFCLK is used by the CMU and drives the prescalers that generate HFCORECLK, HFRADIOCLK and HFPERCLK allowing for flexible clock prescaling. The HFBUSCLK, used in for example the bus and memory system, is equal to HFCLK.

The HFXO clock is fed directly to the Radio Transceiver. The clock received by the Radio Transceiver is therefore not affected by the selected clock source for HFSRCCLK nor by any clock prescaler.

### 12.3.1.2 HFCORECLK - High Frequency Core Clock

HFCORECLK is a prescaled version of HFCLK. This clock drives the Core Modules, which consists of the CPU and modules that are tightly coupled to the CPU (e.g., the cache). The prescale factor for prescaling HFCLK into HFCORECLK is set using the CMU\_HFCOREPRESC register. The setting can be changed dynamically and the new setting takes effect immediately.

**Note:** If HFPERCLK or HFRADIOCLK runs faster than HFCORECLK, the number of clock cycles for each bus-access to (radio) peripheral modules will increase with the ratio between the clocks. Refer to [4.2.5 Bus Matrix](#) for more details.

### 12.3.1.3 HFBUSCLK - High Frequency Bus Clock

HFBUSCLK is equal to HFCLK. This clock drives the Bus and Memory System. HFBUSCLK is also used to drive the bus interface to the Low Energy Peripherals as described further in [12.3.1.7 LFACLK - Low Frequency a Clock](#), [12.3.1.8 LFBCLK - Low Frequency B Clock](#) and [12.3.1.9 LFECLK - Low Frequency E Clock](#). Some of the modules that are driven by this clock can be clock gated completely when not in use. This is done by clearing the clock enable bit for the specific module in CMU\_HFBUSCLKEN0. The frequency of HFBUSCLK is equal to the frequency of HFCLK and can therefore only be prescaled by using the PRESC bitfield in CMU\_HFPRESC.

### 12.3.1.4 HFPERCLK - High Frequency Peripheral Clock

Like HFCORECLK, HFPERCLK is a prescaled version of HFCLK. This clock drives the High-Frequency Peripherals. All the peripherals that are driven by this clock can be clock gated individually when not in use. This is done by clearing the clock enable bit for the specific peripheral in CMU\_HFPERCLKEN0. All high frequency peripheral clocks can be universally and simultaneously gated by clearing the HFPERCLKEN bit in the CMU\_CTRL register. The prescale factor for prescaling HFCLK into HFPERCLK is set using the CMU\_HFPERPRESC register. The setting can be changed dynamically and the new setting takes effect immediately.

**Note:** If HFPERCLK runs faster than HFCORECLK, the number of clock cycles for each bus-access to peripheral modules will increase with the ratio between the clocks. For example, if a bus-access normally takes three cycles, it will take 9 cycles of HFCORECLK if HFPERCLK runs three times as fast as HFCORECLK.

### 12.3.1.5 HFRADIOCLK - High Frequency Radio Clock

HFRADIOCLK is a prescaled version of HFCLK which drives the High-Frequency Radio Peripherals. All the radio peripherals that are driven by this clock can be clock gated completely when not in use. This is done by clearing the clock enable bit for the specific peripheral in CMU\_HFRADIOCLKEN0. The radio peripherals can also be gated simultaneously by clearing the HFRADIOCLKEN bit in the CMU\_CTRL register. The prescale factor for prescaling HFCLK into HFRADIOCLK is set using the CMU\_HFRADIOPRESC register. The setting can be changed dynamically and the new setting takes effect immediately.

**Note:** If HFRADIOCLK runs faster than HFCORECLK, the number of clock cycles for each bus-access to radio peripheral modules will increase with the ratio between the clocks. E.g. if a bus-access normally takes three cycles, it will take 9 cycles if HFRADIOCLK runs three times as fast as the HFCORECLK.

### 12.3.1.6 ADCnCLK - ADC Core Clock

ADCnCLK is a selectable core clock for ADCn. There are three selectable sources for ADCnCLK: HFSRCCLK, HFXO and AUXHFRCO. In addition, the ADCnCLK can be disabled, which is the default setting. The selection is configured using the ADCnCLKSEL field in CMU\_ADCCTRL. The ADCnCLKINV bit in CMU\_ADCCTRL can be used to invert ADCnCLK. The ADCnCLKDIV bitfield in CMU\_ADCCTRL can be used to prescale ADCnCLK. The bus interface of ADCn is clocked with HFBUSCLK.

### 12.3.1.7 LFACTLK - Low Frequency a Clock

LFACTLK is the selected clock for the Low Energy A Peripherals. There are several selectable sources for LFACTLK: LFRCO, LFXO, PLFRCO and ULFRCO. In addition, the LFACTLK can be disabled, which is the default setting. The selection is configured using the LFA field in CMU\_LFACTLKSEL.

The bus interface to the Low Energy A Peripherals is clocked by HFBUSCLK<sub>LE</sub> and this clock therefore needs to be enabled when programming a Low Energy (LE) peripheral.

Each Low Energy Peripheral that is clocked by LFACTLK has its own prescaler setting and enable bit. The prescaler settings are configured using CMU\_LFAPRESC0 and the clock enable bits can be found in CMU\_LFACTLKEN0.

When operating in oversampling mode, the pulse counters are clocked by LFACTLK. This is configured for each pulse counter (n) individually by setting PCNTnCLKSEL in CMU\_PCNTCTRL.

### 12.3.1.8 LFBCLK - Low Frequency B Clock

LFBCLK is the selected clock for the Low Energy B Peripherals. There are several selectable sources for LFBCLK: LFRCO, LFXO, HFCLKLE, PLFRCO and ULFRCO. In addition, the LFBCLK can be disabled, which is the default setting. The selection is configured using the LFB field in CMU\_LFBCLKSEL. The HFCLKLE setting allows the Low Energy B Peripherals to be used as high-frequency peripherals.

The bus interface to the Low Energy B Peripherals is clocked by HFBUSCLK<sub>LE</sub> and this clock therefore needs to be enabled when programming a LE peripheral.

**Note:** If HFCLKLE is selected as LFBCLK, the clock will stop in EM2 Deep Sleep and EM3 Stop.

Each Low Energy Peripheral that is clocked by LFBCLK has its own prescaler setting and enable bit. The prescaler settings are configured using CMU\_LFBPRESC0 and the clock enable bits can be found in CMU\_LFBCLKEN0.

### 12.3.1.9 LFECLK - Low Frequency E Clock

LFECLK is the selected clock for the Low Energy E Peripherals. There are several selectable sources for LFECLK: LFRCO, LFXO, PLFRCO and ULFRCO. In addition, the LFECLK can be disabled, which is the default setting. The selection is configured using the LFE field in CMU\_LFECLKSEL.

The bus interface to the Low Energy E Peripherals is clocked by HFBUSCLK<sub>LE</sub> and this clock therefore needs to be enabled when programming a LE peripheral.

**Note:** LFECLK is in a different power domain than LFACTLK and LFBCLK, which makes it available all the way down to EM4 Hibernate.

Each Low Energy Peripheral that is clocked by LFECLK has its own prescaler setting and enable bit. The prescaler settings are configured using CMU\_LFEPRESC0 and the clock enable bits can be found in CMU\_LFECLKEN0.

### 12.3.1.10 PCNTnCLK - Pulse Counter N Clock

Each available pulse counter is driven by its own clock, PCNTnCLK where n is the pulse counter instance number. Each pulse counter can be configured to use an external pin (PCNTn\_S0) or LFACLK as PCNTnCLK.

### 12.3.1.11 WDOGnCLK - Watchdog Timer Clock

The Watchdog Timer (WDOGn) can be configured to use one of many different clock sources. Refer to CLKSEL field in WDOGn\_CTRL for a complete list.

### 12.3.1.12 CRYOCLK - CRYOTIMER Clock

The CRYOTIMER clock can be configured to use one of many different clock sources. Refer to OSCSEL field in CRYOTIMER\_CTRL for a complete list. The CRYOTIMER can also run in EM4 Hibernate/Shutoff provided that its selected clock is kept enabled as configured in EMU\_EM4CTRL.

### 12.3.1.13 RFSENSECLK - RFSENSE Clock

The RFSENSE clock can be configured to use one of four different clock sources: LFRCO, LFXO, ULFRCO or the RF Detector Clock. The RFSENSE module can also run in EM4 Hibernate/Shutoff provided that its selected clock is kept enabled as configured in EMU\_EM4CTRL.

### 12.3.1.14 AUXCLK - Auxiliary Clock

AUXCLK is a 1 MHz - 38 MHz clock driven by a separate RC oscillator, the AUXHFRCO. This clock can be used for ADC operation LESENSE operation. When the AUXHFRCO is selected as the ADCn clock via the ADCnCLKSEL bitfield in the CMU\_ADCCTRL register, or if needed by LESENSE, this clock will become active automatically when needed. Even if the AUXHFRCO has not been enabled explicitly by software, the ADC or LESENSE can automatically start and stop it. The AUXHFRCO is explicitly enabled by writing a 1 to AUXHFRCOEN in CMU\_OSCENCMD. This explicit enabling is required when selecting the AUXCLK for SWO operation.

### 12.3.1.15 Debug Trace Clock

The CMU selects the clock used for debug trace via the DBGCLKSEL register. The user can use AUXHFRCO or the HFCLK. The selected debug trace clock will be used to run the Cortex-M4 trace logic.

**Note:** When using AUXHFRCO as the debug trace clock, it must be stopped before entering EM2 or EM3.

## 12.3.2 Oscillators

Control of the various oscillators available in the device is detailed in the following sections.

### 12.3.2.1 Enabling and Disabling

The different oscillators can typically be enabled and disabled via both hardware and software mechanisms. Enabling via software is done by setting the corresponding enable bit in the CMU\_OSCENCMD register. Disabling via software is done by setting the corresponding disable bit in CMU\_OSCENCMD. Enabling via hardware can be performed by various peripherals and varies per oscillator. Disabling via hardware is typically performed on entry of low energy modes. The enable and disable mechanisms for each of the oscillators are summarized in [Table 12.1 Software Based and Hardware Based Enabling and Disabling of Oscillators](#) on page 323 and described in more detail below.

**Table 12.1. Software Based and Hardware Based Enabling and Disabling of Oscillators**

| Oscillator | SW Enable                       | SW Disable                       | HW Enable   | HW Disable   |
|------------|---------------------------------|----------------------------------|---|--|
| ULFRCO     | -                               | -                                | Enabled when in EM0/EM1/EM2/EM3/EM4H.   | EM4S entry depending on configuration in EMU_EM4CTRL.  |
| LFRCO      | Via LFRCOEN in CMU_OSCENCMD.    | Via LFRCODIS in CMU_OSCENCMD.    | Via WDOGn if it is configured to use LFRCO as its clock source via the CLKSEL bitfield in WDOGn_CTRL while SWOSCBLOCK is set. | EM3 entry. EM4 entry depending on configuration in EMU_EM4CTRL.  |
| PLFRCO     | Via PLFRCOEN in CMU_OSCENCMD.   | Via PLFRCODIS in CMU_OSCENCMD.   | Software enable only.   | Software disable only.   |
| LF XO      | Via LFXOEN in CMU_OSCENCMD.     | Via LFXODIS in CMU_OSCENCMD.     | Via WDOGn if it is configured to use LF XO as its clock source via the CLKSEL bitfield in WDOGn_CTRL while SWOSCBLOCK is set. | EM3 entry. EM4 entry depending on configuration in EMU_EM4CTRL.  |
| HFRCO      | Via HFRCOEN in CMU_OSCENCMD.    | Via HFRCODIS in CMU_OSCENCMD.    | Reset exit. EM2/EM3 exit. Automatic control by LEUART RX/TX DMA wake-up as configured in LEUARTn_CTRL.                        | EM2/EM3/EM4 entry. Automatic control by LEUART RX/TX DMA wake-up as configured in LEUARTn_CTRL. Automatic start and selection of HF XO causes HFRCO disable. |
| AUXHFRCO   | Via AUXHFRCOEN in CMU_OSCENCMD. | Via AUXHFRCODIS in CMU_OSCENCMD. | Automatic control by ADC and LESENSE.   | EM2/EM3/EM4 entry. Automatic control by ADC and LESENSE even in EM2/EM3.   |
| HFXO       | Via HFXOEN in CMU_OSCENCMD.     | Via HFXODIS in CMU_OSCENCMD.     | Automatic start by Radio Controller (RAC) or EM0/EM1 entry as configured in CMU_HFXOCTRL.                                     | EM2/EM3/EM4 entry.   |

### 12.3.2.1.1 LFRCO and LFXO

The LFXO and LFRCO can be enabled and disabled by software via the CMU\_OSCENCMD register. WDOGn can be configured to force the LFXO or LFRCO to become (and remain) enabled when such an oscillator is selected as its clock source via the CLKSEL bitfield in the WDOGn\_CTRL register while SWOSCBLOCK is set. In that case LFXODIS and LFRCODIS commands are blocked. They are automatically disabled when entering EM3. Upon EM4 entry they are default turned off, but they can optionally be retained depending on the EMU\_EM4CTRL configuration. Retaining of the LFXO or LFRCO in EM4 is needed if such an oscillator is required by a specific peripheral in EM4. Retaining can also be used to guarantee quick oscillator availability after EM4 exit.

The oscillators should never be retained in case they are off before entering EM4. The following are the valid ways of using the LFXO/LFRCO retention mechanism:

- Turn on LFXO/LFRCO always (even in EM4):
  1. POR
  2. Enable LFXO/LFRCO
  3. Enable RETAINLFXO/RETAINLFRCO
  4. EM4 entry
  5. LFXO/LFRCO are retained and remain running in EM4
  6. EM4 wakeup
  7. Enable LFXO/LFRCO
  8. Set EM4UNLATCH in EMU\_CMD
- Turn off LFXO/LFRCO in EM4:
  1. POR
  2. Disable RETAINLFXO/RETAINLFRCO (default)
  3. Enable LFXO/LFRCO
  4. EM4 entry
  5. LFXO/LFRCO are off in EM4
  6. EM4 wakeup
  7. Enable LFXO/LFRCO
  8. Set EM4UNLATCH in EMU\_CMD
- Turn on LFXO/LFRCO after EM4 exit:
  1. POR
  2. Disable RETAINLFXO/RETAINLFRCO (default)
  3. Enable LFXO/LFRCO
  4. EM4 entry
  5. LFXO/LFRCO are off in EM4
  6. EM4 wakeup
  7. Enable LFXO/LFRCO
  8. Set EM4UNLATCH in EMU\_CMD
  9. Enable RETAINLFXO/RETAINLFRCO

In summary RETAINLFXO/RETAINLFRCO should either be changed once after POR and kept static, or they can be changed on-the-fly only after asserting EM4UNLATCH.

**Note:**

- In order to support usage of LFRCO and LFXO in EM4, their settings are automatically latched upon EM4 entry. These settings remain latched upon wake-up from EM4 to EM0 although the related registers (CMU\_LFRCOCTRL, CMU\_LFXOCTRL, CMU\_LFECLKSEL, CMU\_LFECLKEN0 and CMU\_LEEPPRESCO) will have been reset. The registers can be rewritten by software, but they will only affect the LFRCO and LFXO after unlatching their settings by setting EM4UNLATCH in the EMU\_CMD register.
- Turning off the LFRCO and LFXO upon EM4 Hibernate/Shutoff entry is most easily done by using the RETAINLFRCO and RETAINLFXO bitfields from the EMU\_EM4CTRL register, which are default such that the LFRCO and LFXO are turned off automatically upon EM4 Hibernate/Shutoff entry. Alternatively the LFRCO and LFXO can be disabled via the CMU\_OSCENCMD register, in which case software should wait for the oscillators to be properly disabled before executing the EM4 Hibernate/Shutoff entry routine.

After enabling the LFRCO (or LFXO), it should not be disabled before it has been signaled to be ready. Similarly, after disabling the LFRCO (or LFXO), it should not be re-enabled before it has been signaled to be non-ready. Before entering EM4, software should check that the LFRCO (or LFXO) is signaled to be ready before allowing or initiating the EM4 entry if that oscillator is required in EM4. Also, to guarantee latching the latest settings, no control write should be ongoing upon EM4 entry as can be checked via the CMU\_SYNCBUSY register. Typical enable and disable sequences are as follows:

```

CMU->OSCENCMD = CMU_OSCENCMD_LFRCOEN;
while ((CMU->STATUS & CMU_STATUS_LFRCORDY) != CMU_STATUS_LFRCORDY);

CMU->OSCENCMD = CMU_OSCENCMD_LFRCODIS;
while ((CMU->STATUS & CMU_STATUS_LFRCORDY) == CMU_STATUS_LFRCORDY);

```

When the LFXO is disabled, the interface to the LFXTAL\_N and LFXTAL\_P pins are set in a high-Z state. The XTAL oscillations will not stop immediately when LFXO is disabled, but typically die out gradually over some 100 ms. If the LFXO is enabled before XTAL oscillations have had time to reach zero amplitude, startup time can be significantly shorter.

**Note:** The LFRCORDY and LFXORDY interrupts can be used to wake up the system from EM2 Deep Sleep. In this way busy waiting for the LFRCO or LFXO to become ready can be avoided by going into EM2 after enabling these oscillators and sleeping until the interrupt causes a wakeup.

### 12.3.2.1.2 ULFRCO

The ULFRCO is automatically enabled in EM0, EM1, EM2, EM3, and EM4H and cannot be controlled via CMU\_OSCENCMD. It is automatically disabled upon entering EM4S unless prevented by the configuration in EMU\_EM4CTRL.

### 12.3.2.1.3 HFRCO

The HFRCO can be enabled and disabled by software via the CMU\_OSCENCMD register. The HFRCO is disabled automatically when entering EM2, EM3, or EM4. Further hardware based enabling and disabling can be performed by the LEUART when using automatic RX/TX DMA wakeup as controlled by the RXDMAWU and TXDMAWU bits in the LEUARTn\_CTRL register. An automatic start and selection of the HFXO will lead to an automatic HFRCO disabling.

The supported HFRCO frequency range is from 1 MHz to 38 MHz. The default HFRCO frequency is 19 MHz.

### 12.3.2.1.4 HFXO

The HFXO can be enabled and disabled by software via the CMU\_OSCENCMD register. The HFXO is disabled automatically when entering EM2, EM3, or EM4. Hardware based HFXO enabling can be initiated by various peripherals as configured via the AUTOSTARTRDYSELRA, AUTOSTARTEM0EM1, and AUTOSTARTSELEM0EM1 bits in the CMU\_HFXOCTRL register. The interaction between hardware based and software based control of the HFXO is further explained in [12.3.2.4.1 Automatic HFXO Start](#).

The supported HFXO frequency range is from 38 MHz to 40 MHz.

After enabling the HFXO, it should not be disabled before it has been signaled to be enabled. Similarly, after disabling the HFXO it should not be re-enabled before it has been signaled to be non-enabled. Typical enable and disable sequences are as follows:

```

CMU->OSCENCMD = CMU_OSCENCMD_HFXOEN;
while ((CMU->STATUS & CMU_STATUS_HFXOENS) != CMU_STATUS_HFXOENS);

CMU->OSCENCMD = CMU_OSCENCMD_HFXODIS;
while ((CMU->STATUS & CMU_STATUS_HFXOENS) == CMU_STATUS_HFXOENS);

```

### 12.3.2.1.5 AUXHFRCO

The AUXHFRCO can be enabled and disabled by software via the CMU\_OSCENCMD register. The AUXHFRCO is disabled automatically when entering EM2, EM3, or EM4. Hardware based AUXHFRCO enabling and disabling is however performed by the ADC module when AUXCLK is selected for its operation and by the LESENSE module making it available even when being in EM2/EM3.

The supported AUXHFRCO frequency range is from 1 MHz to 38 MHz. The default AUXHFRCO frequency is 19 MHz

After enabling the AUXHFRCO, it should not be disabled before it has been signaled to be enabled. Similarly, after disabling the AUXHFRCO, it should not be re-enabled before it has been signaled to be non-enabled. Typical enable and disable sequences are as follows:

```
CMU->OSCENCMD = CMU_OSCENCMD_AUXHFRCOEN;
while ((CMU->STATUS & CMU_STATUS_AUXHFRCOENS) != CMU_STATUS_AUXHFRCOENS);

CMU->OSCENCMD = CMU_OSCENCMD_AUXHFRCODIS;
while ((CMU->STATUS & CMU_STATUS_AUXHFRCOENS) == CMU_STATUS_AUXHFRCOENS);
```

**Note:** When using AUXHFRCO as the debug trace clock (as selected in CMU\_DBGCLKSEL), it must be stopped before entering EM2 or EM3.

### 12.3.2.2 Oscillator Start-up Time and Time-out

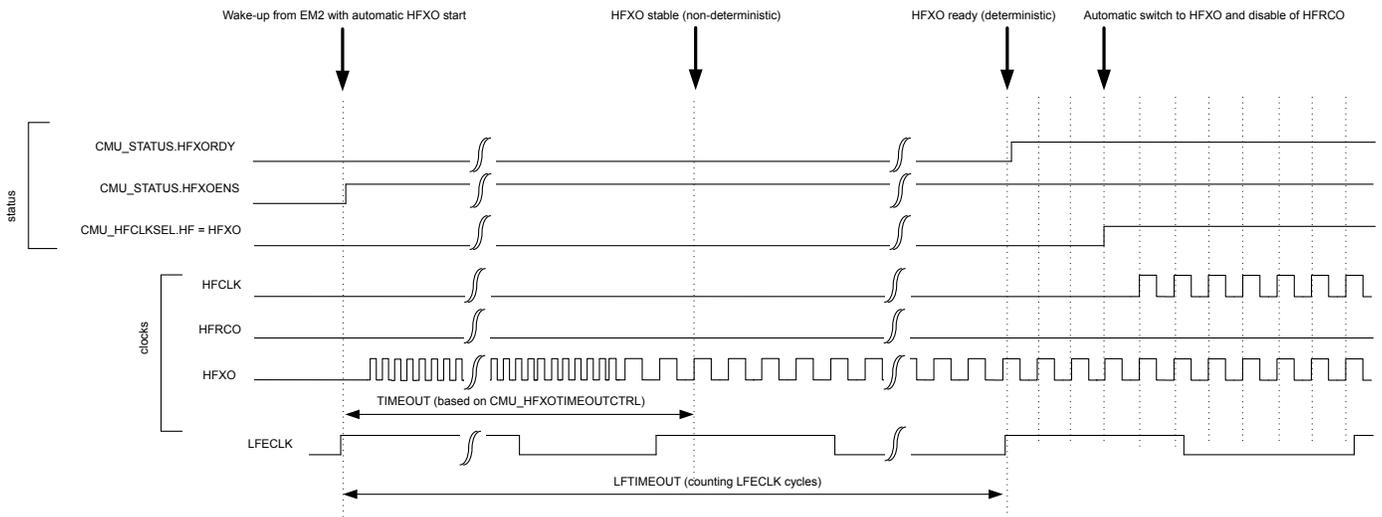
The start-up time differs per oscillator and the usage of an oscillator clock can further be delayed by a time-out. The LFRCO, LFXO and the HFXO have a configurable time-out which is set by software in the (various) TIMEOUT bitfields of the CMU\_LFRCTRL, CMU\_LFXOCTRL and CMU\_HFXOCTRL registers respectively. The time-out delays the assertion of the READY signal for LFRCO, LFXO and HFXO and should allow for enough time for the oscillator to stabilize. The time-out can be optimized for the chosen crystal (for LFXO and HFXO) used in the application. In case LFRCO and/or LFXO has been retained throughout EM4 Hibernate/Shutdown, such retained oscillators can be quickly restarted for use as LFACLK, LFBCLK or LFECLK by using the minimum TIMEOUT settings for them. For the other RC oscillators (HFRCO, AUXHFRCO, and ULFRCO), the start-up time is known and a fixed time-out is used.

There are individual bits in the CMU\_STATUS register for each oscillator indicating the status of the oscillator:

- ENABLED - Indicates that the oscillator is enabled
- READY - Start-up time including time-out is exceeded

These status bits are located in the CMU\_STATUS register.

Additionally, the HFXO has a second time-out counter which can be used to achieve deterministic start-up time based on timing from the LFXO, ULFRCO, or LFRCO. This second counter runs off LFECLK and can be programmed via the LFTIMEOUT bitfield in the CMU\_HFXOCTRL register. It can be used when waking up from EM2 when either ULFRCO, LFRCO or LFXO is already running and stable. In this case the HFXO ready assertion can be delayed with the number of LFECLK cycles as programmed in LFTIMEOUT. The HFXO ready signal is asserted when both the TIMEOUT counter (configured via the CMU\_HFXOCTRL register) and the LFTIMEOUT counter (configured via CMU\_HFXOCTRL register) have timed out as shown in [Figure 12.3 CMU Deterministic HFXO startup using LFTIMEOUT on page 327](#). The TIMEOUT should cover the actual crystal startup time. Typically the time base used for the TIMEOUT counter is not as accurate as the time base accuracy that can be achieved for the LFTIMEOUT counter, specifically if that one is based on the LFXO timing. If LFTIMEOUT is triggered before TIMEOUT is triggered, then the LFTIMEOUTERR bitfield in CMU\_IF will be set to 1. Note that use of LFTIMEOUT requires that the peripheral causing the wake-up is on the LFECLK domain. The intended use scenario is for example to wake up from EM2 by the RTCC triggering RAC wake-up via the PRS, which in turn can wake up the entire system. The RAC wake-up causes an automatic start of the HFXO in case the AUTOSTARTRDYSELRAC bit in CMU\_HFXOCTRL is set to 1. Assertion of the HFXO ready signal, and therefore the radio start timing, can then be made deterministic by using LFTIMEOUT.



**Figure 12.3. CMU Deterministic HFXO startup using LFTIMEOUT**

The startup behavior of the HFXO also depends on how and how long the HFXO is disabled. This can be controlled by configuring the XT12GND, and XTO2GND bitfields in the CMU\_HFXOCTRL register.

### 12.3.2.3 Switching Clock Source

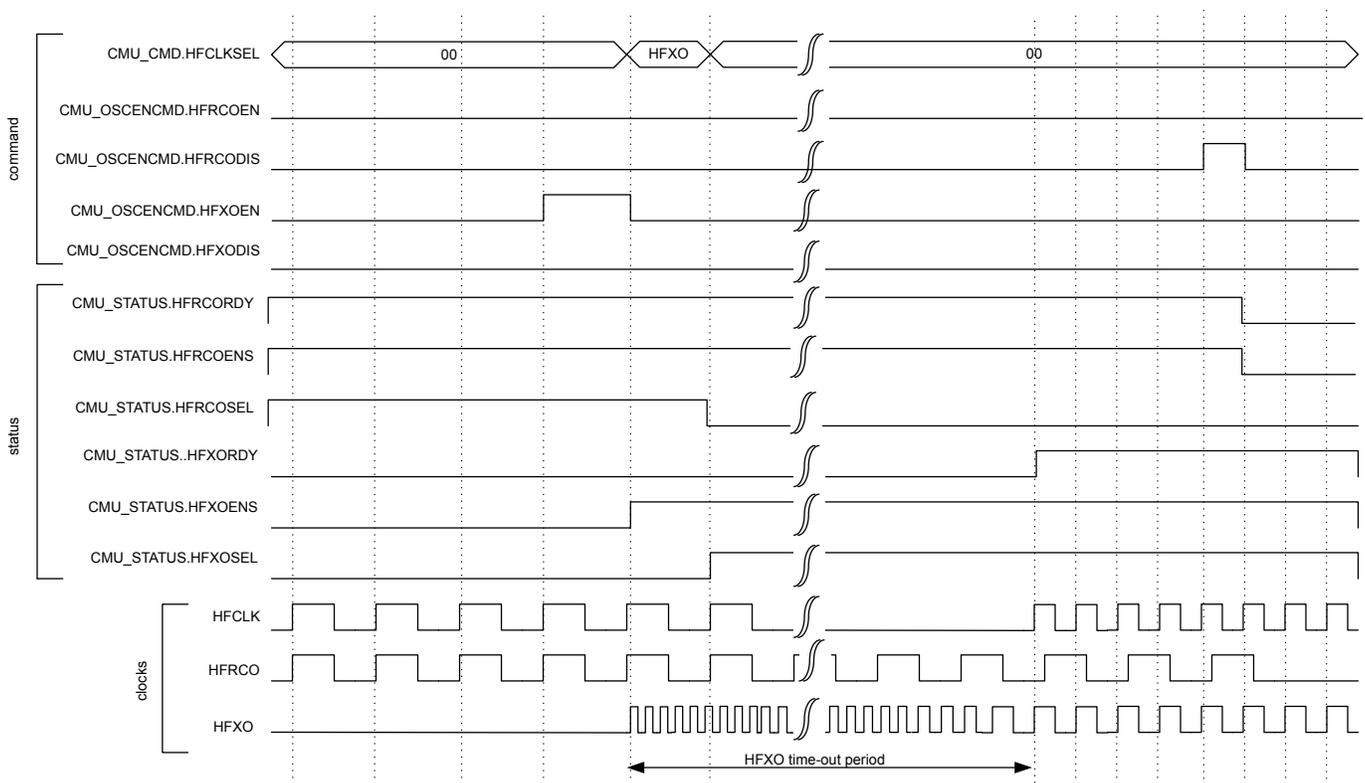
The HFRCO oscillator is a low energy oscillator with extremely short start-up time. Therefore, this oscillator is always chosen by hardware as the clock source for HFCLK when the device starts up (e.g., after reset and after waking up from EM2 Deep Sleep and EM3 Stop). After reset, the HFRCO frequency is 19 MHz.

Software can switch between the different clock sources at run-time. For example, when the HFRCO is the clock source, software can switch to HFXO by writing the field HF in the CMU\_HFCLKSEL command register. See [Figure 12.4 CMU Switching from HFRCO to HFXO before HFXO is ready on page 328](#) for a description of the sequence of events for this specific operation.

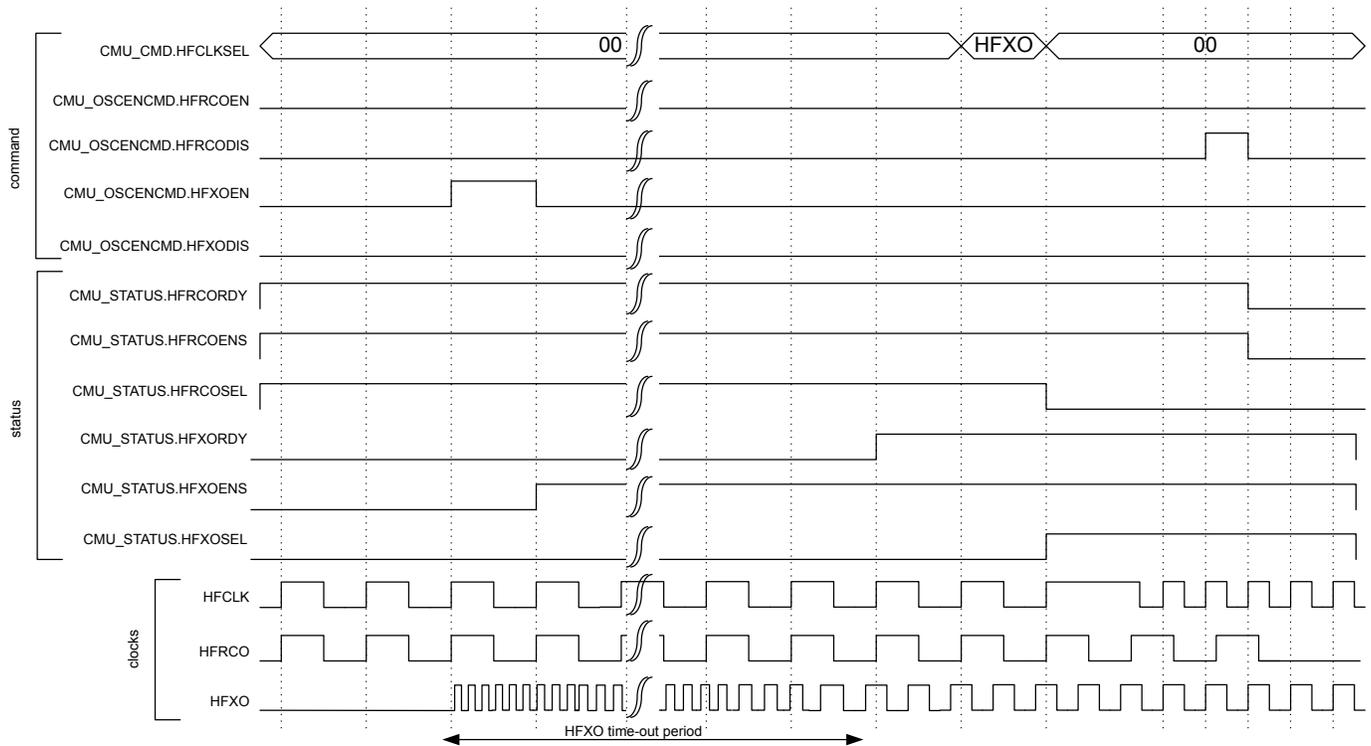
**Note:** Before switching the HFCLKSRC to HFXO via the HF bitfield in CMU\_HFCLKSEL it is important to first enable the HFXO. Switching to a disabled oscillator will effectively stop HFSRCCLK and only a reset can recover the system.

When selecting an oscillator which has been enabled, but which is not ready yet, the HFSRCCLK will stop for the duration of the oscillator start-up time since the oscillator driving it is not ready. This effectively stalls the Core Modules and the High-Frequency Peripherals. It is possible to avoid this by first enabling the target oscillator (e.g., HFXO) and then waiting for that oscillator to become ready before switching the clock source. This way, the system continues to run on the HFRCO until the target oscillator (e.g., HFXO) has timed out and provides a reliable clock. This sequence of events is shown in [Figure 12.5 CMU Switching from HFRCO to HFXO after HFXO is ready on page 329](#).

A separate flag is set when the oscillator is ready. This flag can also be configured to generate an interrupt.



**Figure 12.4. CMU Switching from HFRCO to HFXO before HFXO is ready**



**Figure 12.5. CMU Switching from HFRCO to HFXO after HFXO is ready**

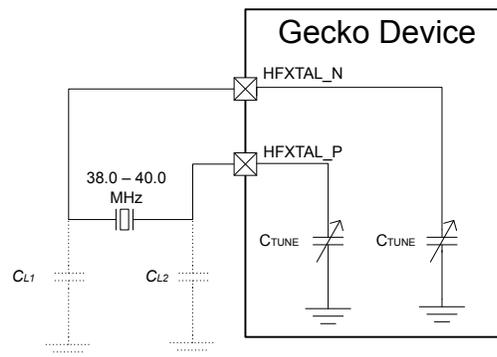
Switching clock source for LFACLK, LFBCLK, and LFECLK is done by setting the LFA, LFB and LFE bitfields in `CMU_LFACLKSEL`, `CMU_LFBCLKSEL` and `CMU_LFECLKSEL` respectively. To ensure no stalls in the Low Energy Peripherals, the clock source should be ready before switching to it.

**Note:** To save energy, remember to turn off all oscillators not in use.

### 12.3.2.4 HFXO Configuration

The High Frequency Crystal Oscillator needs to be configured to ensure safe startup for the given crystal. Refer to the device data sheet and application notes for guidelines in selecting correct components and crystals as well as for configuration trade-offs.

The HFXO crystal is connected to the HFXTAL\_N/HFXTAL\_P pins as shown in [Figure 12.6 HFXO Pin Connection on page 330](#)

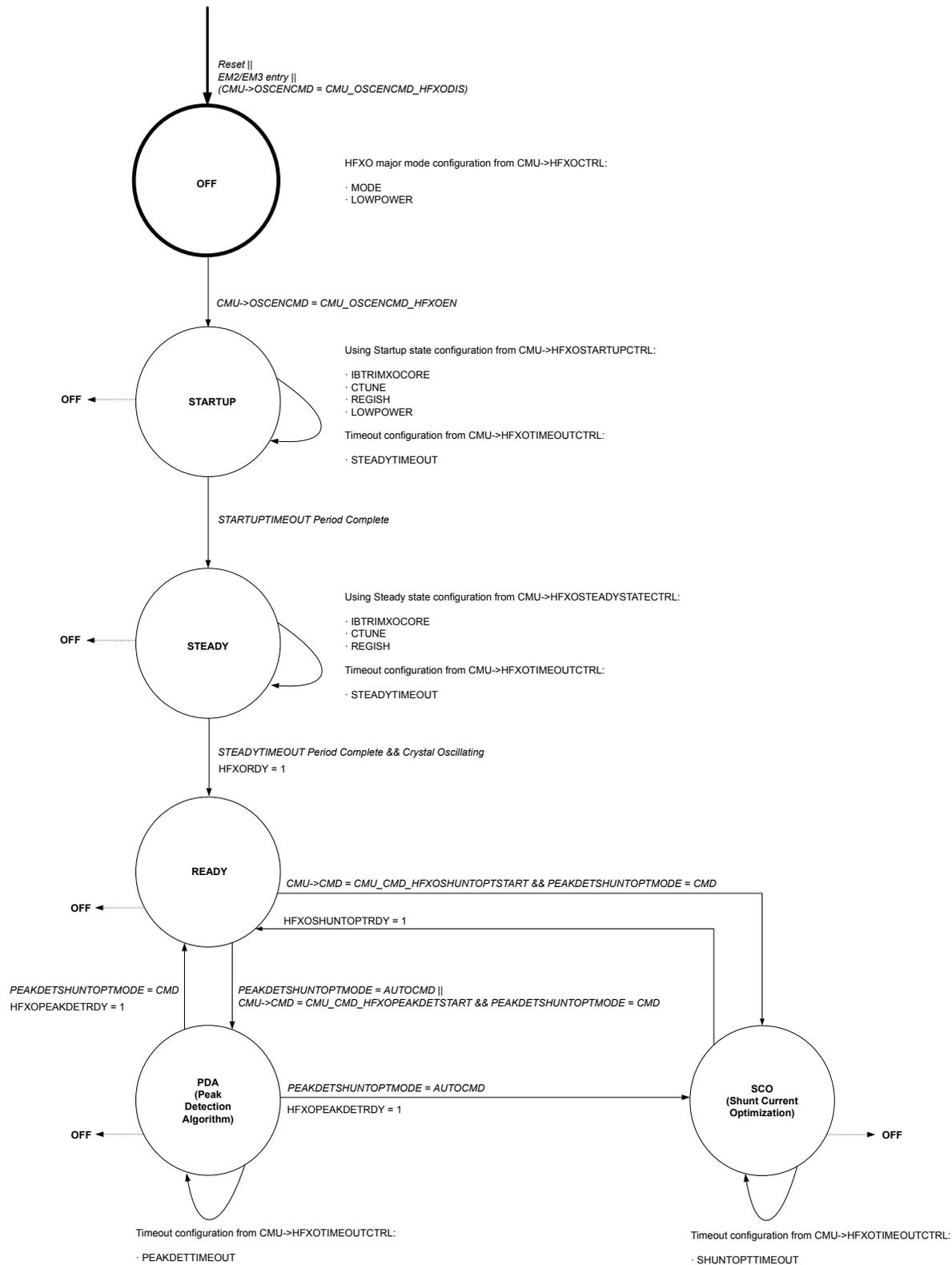


**Figure 12.6. HFXO Pin Connection**

By default the HFXO is started in crystal mode, but it is possible to connect an active external sine wave or square wave clock source to the HFXTAL\_N pin of the HFXO. By configuring the MODE field in CMU\_HFXOCTRL to EXTCLK, the HFXO can be bypassed and the source clock can be provided through the HFXTAL\_N pin.

Upon enabling the HFXO, a hardware state machine sequentially applies the configurable startup state and steady state control settings from the CMU\_HFXOSTARTUPCTRL and CMU\_HFXOSTEADYSTATECTRL registers. Configuration is required for both the startup state and the steady state of the HFXO. After reaching the steady operation state of the HFXO, further optimization can optionally be performed to optimize the HFXO for noise and current consumption. Optimization for noise can be performed by an automatic Peak Detection Algorithm (PDA). Optimization for current can be performed by an automatic Shunt Current Optimization algorithm (SCO). HFXO operation is possible without PDA and SCO at the cost of higher noise and current consumption than required. Note that the HFXO circuit supports only crystals in the frequency range from 38-40 MHz, and is therefore only supported at voltage scale level 2. See [11.3.9 Voltage Scaling](#) for more details.

Upon fully disabling the HFXO, the HFXTAL\_N and HFXTAL\_P pins can optionally be automatically pulled to ground as configured via the XT12GND and XTO2GND bits respectively from the CMU\_HFXOCTRL register. Do not set XT12GND to 1 when the HFXO is in EXTCLK mode and an external wave is connected.



**Figure 12.7. CMU HFXO control state machine**

Refer to the device data sheet to find the configuration values for a given crystal. The startup state configuration needs to be written into the IBTRIMXOCORE and CTUNE bitfields of the `CMU_HFXOSTARTUPCTRL` register. The duration of the startup phase is configured in the `STARTUPTIMEOUT` bitfield of the `CMU_HFXOTIMEOUTCTRL` register. Similarly, the device data sheet provides the steady

state configuration depending on the crystal's CL, RESR and oscillation frequency. This configuration is programmed into the IBTRIMXOCORE, REGISH and CTUNE bitfields of the CMU\_HFXOSTEADYSTATECTRL register. The minimum duration of the steady phase is configured in the STEADYTIMEOUT bitfield of the CMU\_HFXOTIMEOUTCTRL register.

All HFXO configuration needs to be performed prior to enabling the HFXO via HFXOEN in CMU\_OSCENCMD unless noted otherwise. The HFXOENS flag in CMU\_STATUS indicates if the HFXO has been successfully enabled. Once the HFXO startup time (STARTUPTIMEOUT plus STEADYTIMEOUT) has exceeded and oscillations begin, the HFXORDY flag in CMU\_STATUS. If PDA and SCO are enabled, the HFXOPEAKDETRDY and HFXOSHUNTOPTRDY flags in the CMU\_STATUS register indicate when these algorithms are ready and it is advised to also wait for these flags before using the HFXO.

The HFXO crystal bias current may be optimized and set to a value which decreases output phase noise without sacrificing PSR. This is done by programming the recommended IBTRIMXOCORE value into the CMU\_HFXOSTEADYSTATECTRL register. The built-in Peak Detector Algorithm (PDA) performs further optimization to accommodate for process variations. Once PDA is ready as indicated by the HFXOPEAKDETRDY flag, the found optimal bias current setting is available in the IBTRIMXOCORE bitfield of the CMU\_HFXOTRIMSTATUS register. This IBTRIMXOCORE setting should be saved and can be applied directly during a future HFXO startup as a low noise setting by programming it into the corresponding bitfield in CMU\_HFXOSTEADYSTATECTRL while the HFXO is off.

If low noise is not required, the same PDA algorithm can be configured to optimize the HFXO for low current consumption by enabling LOWPOWER in the CMU\_HFXOCTRL register before starting up the HFXO. The found IBTRIMXOCORE setting can be saved as a future low current setting.

Default PDA is started automatically once the HFXO has become ready. Repeated PDA can be triggered by writing HFXOPEAKDETSTART to 1 in the CMU\_CMD register. PDA can also be triggered only by the command register by configuring PEAKDETSHUNTOPTMODE to CMD in the CMU\_HFXOCTRL register before starting the HFXO. For PDA to work correctly, the REGISHUPPER bitfield of CMU\_HFXOSTEADYSTATECTRL should be programmed to the value of the steady state REGISH + 3. The PEAKDETTIMEOUT bitfield in the CMU\_HFXOTIMEOUTCTRL register is used to time the PDA steps and needs to be configured according to the device data sheet for the given crystal. The PEAKDETEN bitfield of the CMU\_HFXOSTEADYSTATECTRL register is only used during manual (i.e. fully software controlled) peak detection and is ignored during automatic or command based triggering of the PDA. Note that the manual PDA mode is not recommended for general usage and therefore it is not further described. PDA should not be used when using an external wave as clock source.

Current consumption can be (further) reduced by running Shunt Current Optimization (SCO) after PDA. Once SCO is ready as indicated by the HFXOSHUNTOPTRDY flag, the found optimal regulator output current setting is available in the REGISH bitfield of the CMU\_HFXOTRIMSTATUS register. This REGISH setting should be saved and can be applied directly during a future HFXO startup as a low current setting by programming it into the corresponding bitfield in CMU\_HFXOSTEADYSTATECTRL while the HFXO is off. Normally SCO is run only for initial HFXO start up. The amplitude of the oscillator is not strongly dependent on temperature, but further optimization may be done each time that the temperature changes significantly. In that case, run SCO again by writing HFXOSHUNTOPTSTART to 1 in the CMU\_CMD register. SCO depends on the LOWPOWER setting in the CMU\_HFXOCTRL and needs to be re-run if that value has been changed. SCO should not be run when the HFXO is in use by the Radio Transceiver.

Default SCO is started automatically once the HFXO has become ready and PDA has finished. Repeated SCO can be triggered by writing HFXOSHUNTOPTSTART to 1 in the CMU\_CMD register. SCO can also be triggered only by the command register by configuring PEAKDETSHUNTOPTMODE to CMD in the CMU\_HFXOCTRL register before starting the HFXO. For SCO to work correctly, the REGISHUPPER bitfield of CMU\_HFXOSTEADYSTATECTRL should be programmed to the value of the steady state REGISH + 3. The SHUNTOPTTIMEOUT bitfield in the CMU\_HFXOTIMEOUTCTRL register is used to time the SCO steps and needs to be configured according to the device data sheet for the given crystal. The REGSELILOW bitfield of the CMU\_HFXOSTEADYSTATECTRL register is only used during manual (i.e. fully software controlled) shunt current optimization and is ignored during automatic or command based triggering of the SCO. Note that the manual SCO mode is not recommended for general usage and therefore it is not further described.

#### 12.3.2.4.1 Automatic HFXO Start

The enabling of the HFXO and its selection as HFSRCCLK source can be performed automatically by hardware. Automatic HFXO enable and select can for example be used upon wake-up of the Radio Controller (RAC). Automatic control of the HFXO is controlled via the AUTOSTARTRDYSELRAC, AUTOSTARTSELEM0EM1 and AUTOSTARTEM0EM1 bits in the CMU\_HFXOCTRL register. It further depends on the energy mode of the EFR32 and on the status of the RAC .

The HFXO autostart functionality is typically used when the RAC is used. The RAC module always requires the HFXO for its operation. The hardware requirement from RAC for an HFXO based HFSRCCLK is indicated in the HFXOREQ bitfield of the CMU\_STATUS register. This requirement in itself does not lead to an automatic enable or select of the HFXO.

An automatic HFXO enable is performed only if any of the following conditions are met:

- EFR32 is in EM0/EM1 and AUTOSTARTEM0EM1 or AUTOSTARTSELEM0EM1 are set to 1.
- RAC is awake and AUTOSTARTRDYSELRAC is set to 1.

An automatic HFXO select is performed only if any of the following conditions is met:

- EFR32 is in EM0/EM1 and AUTOSTARTSELEM0EM1 is set to 1.
- RAC is awake, HFXO is ready, and AUTOSTARTRDYSELRAC is set to 1.

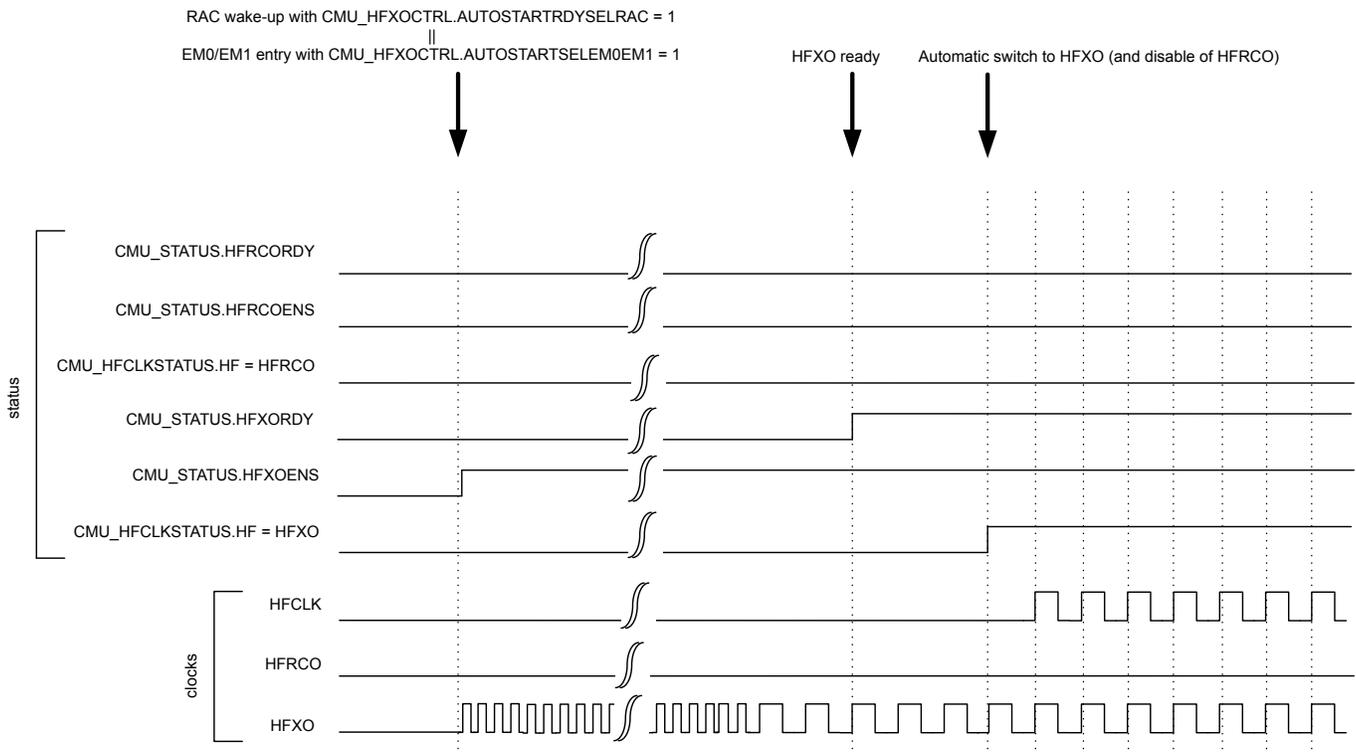
Whenever any of the conditions for automatic HFXO enable is met, software is not allowed to disable the HFXO. An attempt to do so (e.g., by writing 1 to the HFXODIS bit) is ignored and causes the HFXODISERR bit in the CMU\_IF register to be set to 1. Similarly, whenever any of the conditions for automatic HFXO selection is met, software is not allowed to deselect the HFXO as clock source for HFSRCCLK. An attempt to do so (e.g., by selecting another clock source via CMU\_HFCLKSEL) is ignored and causes the HFXODISERR bit in the CMU\_IF register to be set to 1. Note that CMUERR is not implied by HFXODISERR. CMUERR will not get set to 1 for the above scenarios in which HFXODISERR gets set.

Software can only disable or deselect the HFXO after removing all of the HFXO automatic enable or select reasons. Note that if the autostart functionality is not used, software can always disable or deselect the HFXO even if hardware requires the HFXO as indicated via HFXOREQ bitfield in CMU\_STATUS. The HFXODISERR flag will not get set in that case. The HFXO is only disabled by hardware upon EM2, EM3 or EM4 entry.

In case that AUTOSTARTSELEM0EM1 is set to 1 in EM0/EM1 (irrespective of the other autostart bits), the HFXO select will occur immediately, even if HFXO is not ready yet. Upon wake-up into EM0/EM1 this can therefore lead to a relatively long startup time as the system will not start operating from the HFRCO as it would otherwise do. In case of an automatic select triggered by the RAC (while AUTOSTARTSELEM0EM1 is set to 0), such a select will only occur upon the HFXO becoming ready and software can select and use another clock source in the mean time.

A typical use scenario of the AUTOSTARTRDYSELRAC bit is as follows. Set the AUTOSTARTRDYSELRAC bit in the CMU\_HFXOCTRL register to 1 and set up the RTCC to periodically generate a compare match. Setup a PRS channel which uses this RTCC compare match as its source and allow the PRS channel to cause a wake-up into EM1. Setup the RAC to use the PRS channel as its source for TXEN or RXEN. Now, when the EFR32 is in EM2 and the RTCC generates a compare match, a wake-up into EM1 will occur and the HFXO will automatically start and become selected after which the RAC can perform its work and trigger a transition back into EM2 when done. The system started, used, and stopped the HFXO without ever being in EM0.

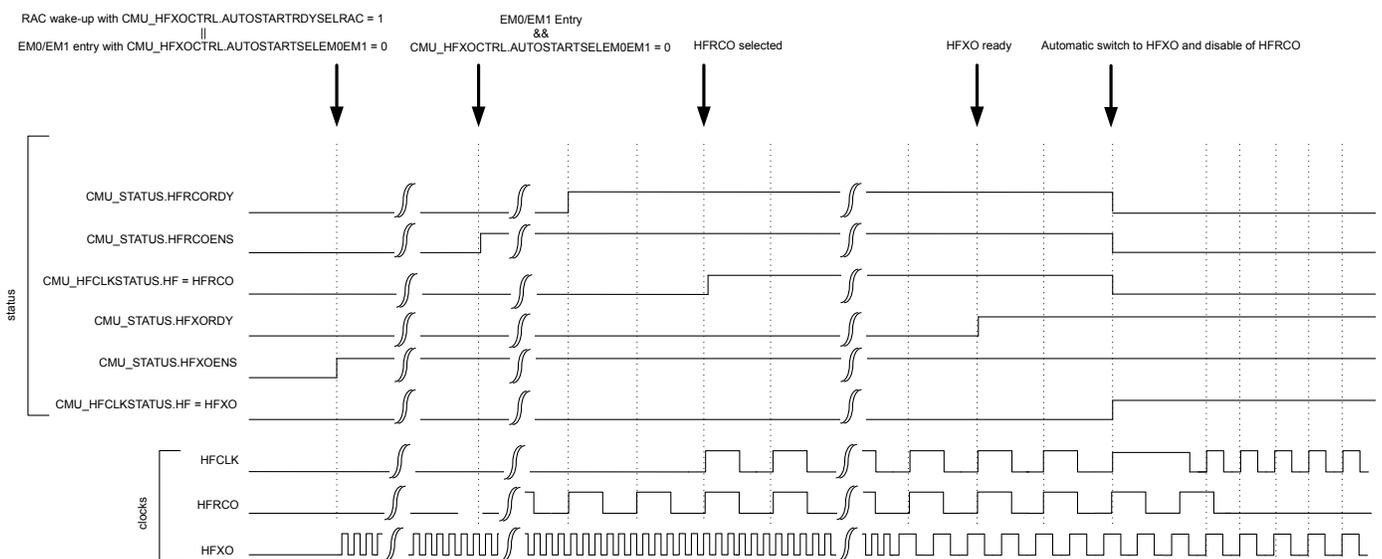
Note that the user should take care that the settings in the MSC\_READCTRL and CMU\_CTRL registers, as described in [12.3.3 Configuration for Operating Frequencies](#), are compatible with 40 MHz HFXO operation before enabling the HFXO automatic startup feature. A basic automatic HFXO start scenario is shown in [Figure 12.8 CMU Automatic Startup and Selection of HFXO on page 334](#).



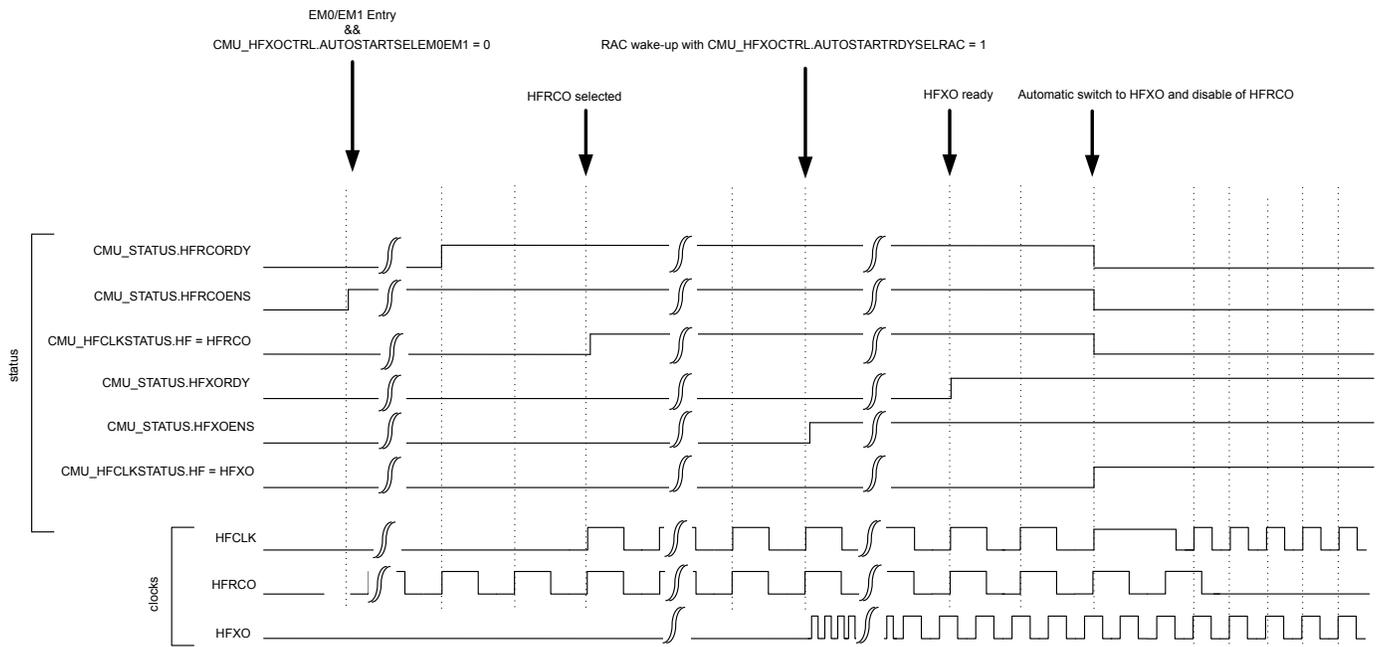
**Figure 12.8. CMU Automatic Startup and Selection of HFXO**

If an automatic selection of HFXO is performed, which switches the clock source used for HFSRCCLK, then the HFXOAUTOSW bit in CMU\_IF is set to 1. After automatic enable and selection of the HFXO, the HFRCO is automatically disabled in case it is running. The disabling of a running HFRCO is signalled via the HFRCODIS bit in CMU\_IF. This only applies to the HFRCO. If for example the LFXO was used as HFSRCCLK at the time of automatic selection of the HFXO, the LFXO remains unaffected.

The interaction between automatic HFXO startup and selection with startup and selection of HFRCO is shown in [Figure 12.9 CMU HFRCO Startup/Selection While Awaiting Automatic HFXO Startup/Selection on page 334](#) and [Figure 12.10 CMU Automatic HFXO startup/selection while HFRCO started/selected on page 335](#).



**Figure 12.9. CMU HFRCO Startup/Selection While Awaiting Automatic HFXO Startup/Selection**



**Figure 12.10. CMU Automatic HFXO startup/selection while HFRCO started/selected**

### 12.3.2.5 LFXO Configuration

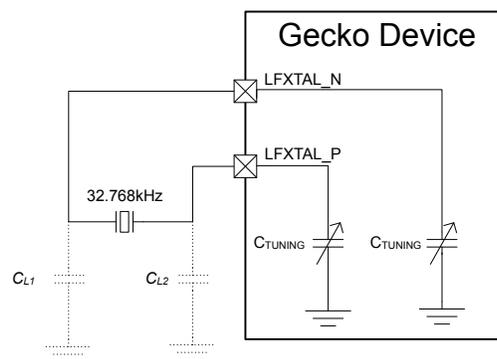
The Low Frequency Crystal Oscillator (LFXO) is default configured to ensure safe startup for all crystals. In order to optimize startup time and power consumption for a given crystal, it is possible to adjust the startup gain in the oscillator by programming the GAIN field in CMU\_LFXOCTRL. Recommendations for the GAIN setting are as follows:

1. C0 must be < 2 pF
2. For 12.5 pF < CL < 18 pF, GAIN = 3
3. For 8 pF < CL < 12.5 pF, GAIN = 2
4. For 6 pF < CL < 8 pF, GAIN = 1
5. For CL = 6 pF, GAIN = 0

Refer to the device data sheet and application notes for guidelines in selecting correct components and crystals as well as for configuration trade-offs.

The LFXO can be retained on in EM4 Hibernate/Shutoff. In that case its required configuration is latched/retained throughout EM4 even though the CMU\_LFXOCTRL register itself will be reset. Upon EM4 exit, the CMU\_LFXOCTRL register therefore needs to be reconfigured to its original settings and the LFXO needs to be restarted via CMU\_OSCENCMD, before optionally unlatching the retained LFXO configuration by writing 1 to EM4UNLATCH in the EMU\_CMD register. The LFXO startup time is configured via the TIMEOUT bitfield of the CMU\_LFXOCTRL register. If the LFXO has been retained throughout EM4 Hibernate/Shutoff, it can be quickly restarted for use as LFACLK, LFBCLK or LFECLK by using its minimum TIMEOUT setting. While retained, the LFXO can be used down to EM4 Hibernate as source for LFECLK and down to EM4 Shutoff as source for RFSENSECLK and CRYOCLK.

The LFXO crystal is connected to the LFXTAL\_N/LFXTAL\_P pins as shown in [Figure 12.11 LFXO Pin Connection on page 336](#).



**Figure 12.11. LFXO Pin Connection**

By configuring the MODE field in CMU\_LFXOCTRL, the LFXO can be bypassed, and an external clock source can be connected to the LFXTAL\_N pin of the LFXO oscillator. If MODE is set to BUFEXTCLK, an external active sine source can be used as clock source. If MODE is set to DIGEXTCLK, an external active CMOS source can be used as clock source.

The LFXO includes on-chip tunable capacitance, which can replace external load capacitors. The TUNING bitfield of the CMU\_LFXOCTRL register is used to tune the internal load capacitance connected between LFXTAL\_P and ground and LFXTAL\_N and ground symmetrically. The capacitance range and step size information is available in the device data sheets. Use the formula below to calculate the TUNING bitfield:

$$\text{TUNING} = ((\text{desiredTotalLoadCap} * 2 - \text{Min}(C_{\text{LFXO\_T}})) / C_{\text{LFXO\_TS}})$$

**Figure 12.12. CMU LFXO Tuning Capacitance Equation**

These tunable capacitors can also be used to compensate for temperature drift of the XTAL in software. Crystals normally have a temperature dependency which is given by a parabolic function. The crystal has highest frequency at its turnover temperature, normally 25C. The frequency is reduced following a parabola for higher and lower temperatures. The LFXO offers a mechanism to internally add capacitance on the LFXTAL\_N and LFXTAL\_P pins (in parallel to an optional external load capacitance). The variation in frequency as a function of temperature can therefore be compensated by adjusting the load capacitance. When the temperature compensation scheme is used, the maximum internal capacitance should be used to obtain good frequency matching at the turnover temperature. For higher and lower temperatures software then has the maximum range available to adjust the tuning. The external load capacitance

must then of course be reduced accordingly. Note that the ADC0 (27. [ADC - Analog to Digital Converter](#)) includes an embedded temperature sensor and that the EMU (11. [EMU - Energy Management Unit](#)) offers a temperature management interface, both of which can be used in combination with this LFXO temperature compensation scheme.

The XTAL oscillation amplitude can be controlled via the HIGHAMPL bitfield in CMU\_LFXOCTRL. Setting HIGHAMPL to 1 will result in higher amplitude, which in turn provides safer operation, somewhat improved duty cycle, and lower sensitivity to noise at the cost of increased current consumption.

The AGC bit of the CMU\_LFXOCTRL register is used to turn on or off the Automatic Gain Control module that adjusts the amplitude of the XTAL. When disabled, the LFXO will run at the startup current and the XTAL will oscillate rail to rail, again providing safer operation, improved duty cycle, and lower sensitivity to noise at the cost of increased current consumption.

### 12.3.2.6 HFRCO and AUXHFRCO Configuration

It is possible to calibrate the HFRCO and AUXHFRCO to achieve higher accuracy (see the device data sheets for details on accuracy). The frequency is adjusted by changing the TUNING and FINETUNING bitfields in CMU\_HFRCOCTRL and CMU\_AUXHFRCOCTRL. Changing to a higher value will result in a lower frequency. Refer to the data sheet for stepsize details.

The HFRCO can be set to one of several different frequency bands from 1 MHz to 38 MHz by setting the FREQRANGE field in CMU\_HFRCOCTRL. Similarly the AUXHFRCO can be set to one of several different frequency bands from 1 MHz to 38 MHz by setting the FREQRANGE field in CMU\_AUXHFRCOCTRL. The HFRCO and AUXHFRCO frequency bands are calibrated during production test, and the production tested calibration values can be read from the Device Information (DI) page. The DI page contains separate tuning values for various frequency bands. During reset, HFRCO and AUXHFRCO tuning values are set to the production calibrated values for the 19 MHz band, which is the default frequency band. When changing to a different HFRCO or AUXHFRCO band, make sure to also update the TUNING value and other bitfields in the CMU\_HFRCOCTRL and CMU\_AUXHFRCOCTRL registers. Typically the entire register is written with a value obtained from the Device Information (DI) page. Refer to [4.6 DI Page Entry Map](#) for information on which frequency band settings are stored in the DI page.

The frequency can be tuned more accurately via the FINETUNING bitfield if fine tuning has been enabled via the FINETUNINGEN bit. Note that there will be a slight increase in the oscillator current consumption when fine tuning is enabled. Note also that changing the value of FINETUNINGEN will result in a frequency shift, regardless of the FINETUNING field value. If the oscillator is to be used at different times with fine tuning enabled and disabled, it should be tuned separately for both settings. The HFRCO and AUXHFRCO contain a local prescaler, which can be used in combination with any FREQRANGE setting. These prescalers allow the output clocks to be divided by 1, 2, or 4 as configured in the CLKDIV bitfield.

When using [12.3.2.8 RC Oscillator Calibration](#) to tune HFRCO and AUXHFRCO to the desired frequency, linear search must be used to avoid over clocking the calibration counters. Before changing the FREQRANGE field in CMU\_HFRCOCTRL, TUNING and FINETUNING fields should initially be set to the highest value (slowest frequency). After changing the FREQRANGE, linearly step TUNING value until desired frequency is reached. Likewise, before changing the TUNING field, FINETUNING field should initially be set to the highest value (lowest frequency). After changing the TUNING field, linearly step FINETUNING until accuracy is reached.

### 12.3.2.7 LFRCO Configuration

It is possible to calibrate the LFRCO to achieve higher accuracy (see the device data sheets for details on accuracy). The frequency is adjusted by changing the TUNING bitfield in CMU\_LFRCOCTRL. Changing to a higher value will result in a lower frequency. Refer to the data sheet for stepsize details.

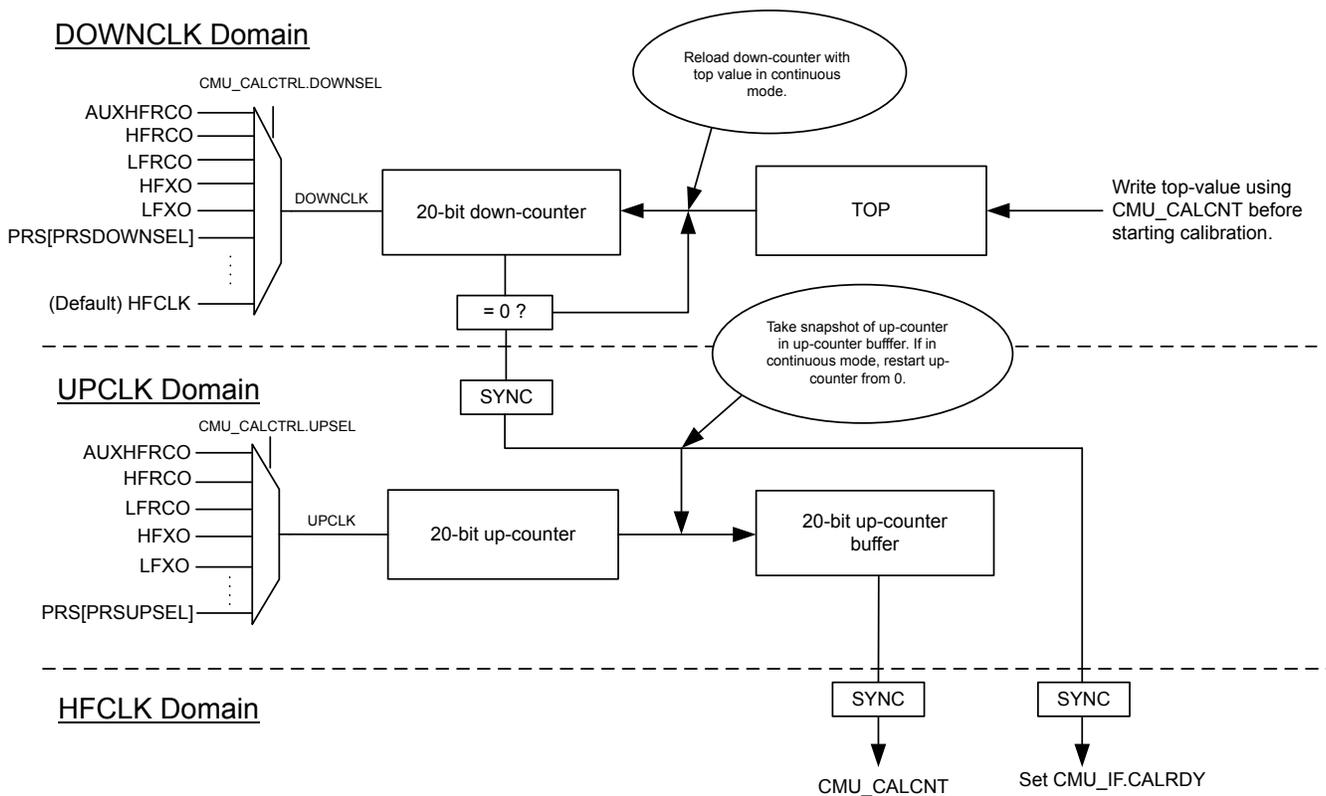
The LFRCO can be retained on in EM4 Hibernate/Shutoff. In that case its required configuration is latched/retained throughout EM4 even though the CMU\_LFRCOCTRL register itself will be reset. Upon EM4 exit the CMU\_LFRCOCTRL register therefore needs to be reconfigured to its original settings and the LFRCO needs to be restarted via CMU\_OSCENCMD, before optionally unlatching the retained LFRCO configuration by writing 1 to EM4UNLATCH in the EMU\_CMD register. The LFRCO startup time is configured via the TIMEOUT bitfield of the CMU\_LFRCOCTRL register. Default its 16 cycle startup should be used. However, in case the LFRCO has been retained throughout EM4 Hibernate/Shutoff, it can be quickly restarted for use as LFACLK or LFBCLK by using its minimum TIMEOUT setting. While retained, the LFRCO can be used down to EM4 Hibernate as source for LFECLK and down to EM4 Shutoff as source for RFSENSECLK and CRYOCLK.

The LFRCO is also calibrated in production and its TUNING values are set to the correct value during reset.

The LFRCO can be put in duty cycle mode by setting the ENVREF bit in CMU\_LFRCOCTRL to 1 before starting the LFRCO. This will reduce current consumption, but will result in slightly worse accuracy especially at high temperatures. Setting the ENCHOP and/or ENDEM bitfields to 1 in the CMU\_LFRCOCTRL register will improve the average LFRCO frequency accuracy at the cost of a worse cycle-to-cycle accuracy.

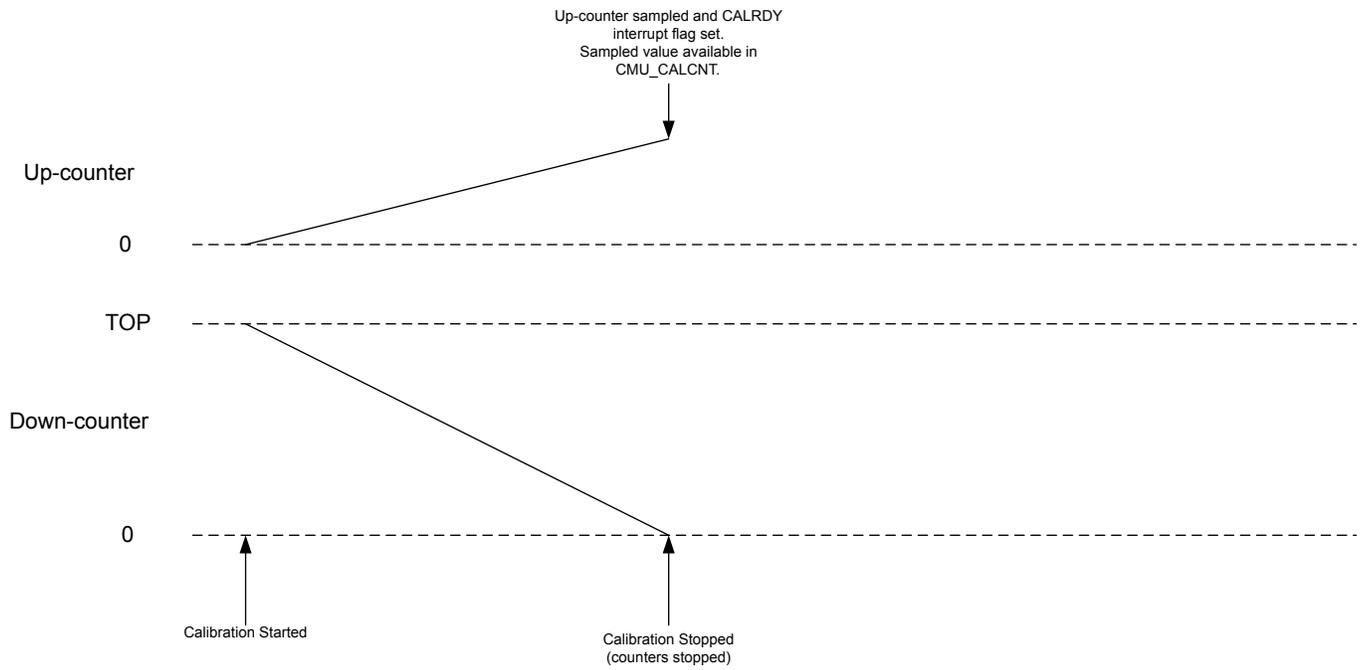
### 12.3.2.8 RC Oscillator Calibration

The CMU has built-in HW support to efficiently calibrate the RC oscillators (LFRCO, HFRCO, AUXHFRCO, etc) at run-time. For a complete list of supported oscillators, refer to DOWNSSEL and UPSEL fields in CMU\_CALCTRL. See [Figure 12.13 HW-support for RC Oscillator Calibration on page 338](#) for an illustration of this circuit. The concept is to select a reference and compare the RC frequency with the reference frequency. When the calibration circuit is started, one down-counter running on a selectable clock (DOWNSSEL in CMU\_CALCTRL) and one up-counter running on a selectable clock (UPSEL in CMU\_CALCTRL) are started simultaneously. The top value for the down-counter must be written to CMU\_CALCNT before calibration is started. The down-counter counts for CMU\_CALCNT + 1 cycles. When the down-counter has reached 0, the up-counter is sampled and the CALRDY interrupt flag is set. If CONT in CMU\_CALCTRL is cleared, the counters are stopped after finishing the ongoing calibration. If continuous mode is selected by setting CONT in CMU\_CALCTRL the down-counter reloads the top value and continues counting and the up-counter restarts from 0. Software can then read out the sampled up-counter value from CMU\_CALCNT. The up-counter has counted (the sampled value)+1 cycles. The ratio between the reference and the oscillator subject to the calibration can easily be found using top+1 and sample+1. Overflows of the up-counter will not occur. If the up-counter reaches its top value before the down-counter reaches 0, the up-counter stays at its top value. Calibration can be stopped by writing CALSTOP in CMU\_CMD. With this HW support, it is simple to write efficient calibration algorithms in software.

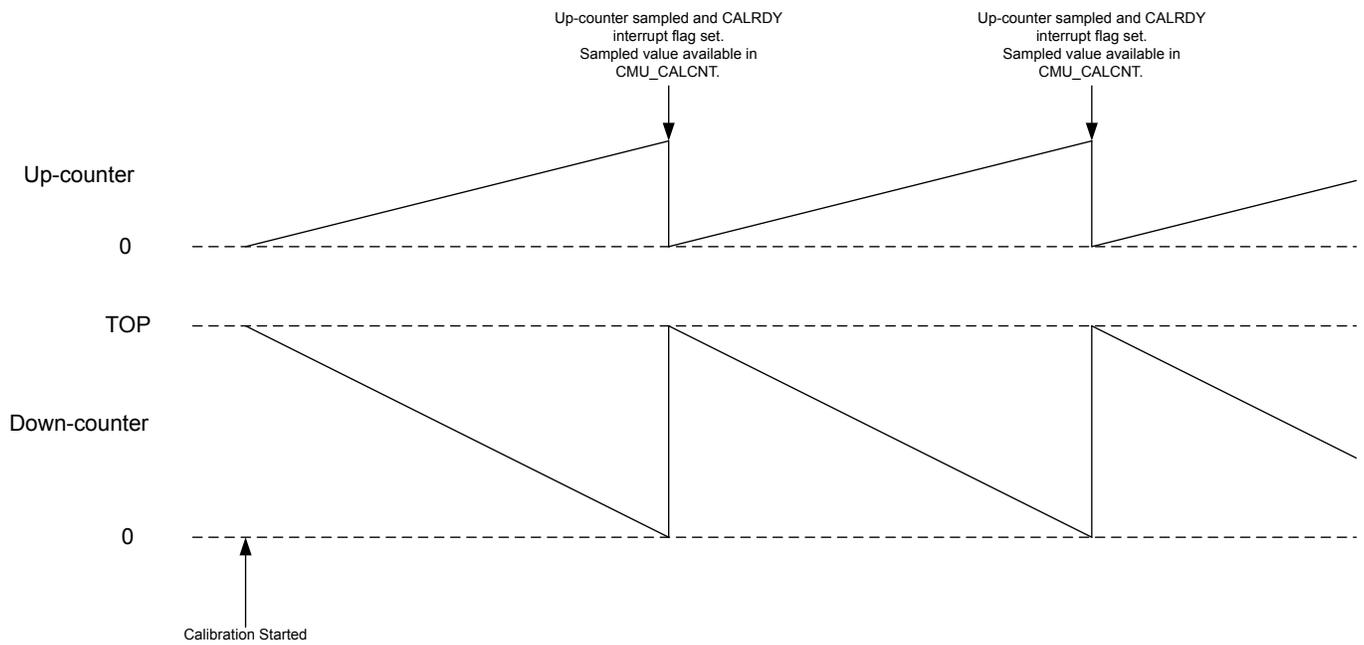


**Figure 12.13. HW-support for RC Oscillator Calibration**

The counter operation for single and continuous mode are shown in [Figure 12.14 Single Calibration \(CONT=0\) on page 339](#) and [Figure 12.15 Continuous Calibration \(CONT=1\) on page 339](#) respectively.



**Figure 12.14. Single Calibration (CONT=0)**



**Figure 12.15. Continuous Calibration (CONT=1)**

### 12.3.3 Configuration for Operating Frequencies

The HFXO is capable of frequencies up to 40 MHz, which allows the EFR32 to run at up to this frequency. However the Memory System Controller (MSC) and the Low Energy Peripheral Interface need to be configured correctly to allow operation at higher frequencies as explained below.

The MODE bitfield in MSC\_READCTRL makes sure the flash is able to operate at the given HFCLK frequency by inserting wait states for flash accesses. The required settings for controlling flash wait states are shown in [Table 12.2 MSC Configuration for Operating Frequencies, at VSCALE2: Flash Wait States on page 340](#). The WSHFLE bitfield in CMU\_CTRL is used to ensure that the Low Energy Peripheral Interface is able to operate at the given HFBUSCLK<sub>LE</sub> frequency by inserting wait states when using this interface. The required settings are shown in [Table 12.4 LE Configuration for Operating Frequencies: Low Energy Peripheral Interface on page 340](#).

Before going to a high frequency, make sure the registers in the table have the correct values. When going down in frequency, make sure to keep the registers at the values required by the higher frequency until after the switch has been done.

**Table 12.2. MSC Configuration for Operating Frequencies, at VSCALE2: Flash Wait States**

| Condition                | MODE in MSC_READCTRL |
|--------------------------|----------------------|
| HFCLK <= 25 MHz          | WS0 or above         |
| 25 MHz < HFCLK <= 40 MHz | WS1 or above         |

**Table 12.3. MSC Configuration for Operating Frequencies, at VSCALE0: Flash Wait States**

| Condition               | MODE in MSC_READCTRL |
|-------------------------|----------------------|
| HFCLK <= 7 MHz          | WS0 or above         |
| 7 MHz < HFCLK <= 14 MHz | WS1 or above         |

**Table 12.4. LE Configuration for Operating Frequencies: Low Energy Peripheral Interface**

| Condition                        | WSHFLE in CMU_CTRL |
|----------------------------------|--------------------|
| HFBUSCLK <sub>LE</sub> <= 32 MHz | 0 / 1              |
| HFBUSCLK <sub>LE</sub> > 32 MHz  | 1                  |

### 12.3.4 Energy Modes

The availability of oscillators and system clocks depends on the chosen energy mode. Default the high frequency oscillators (HFRCO, AUXHFRCO, and HFXO) and high frequency clocks (HFSRCLK, HFCLK, HFCORECLK, HFBUSCLK, HFPERCLK, HFRADIOCLK, HFCLKLE) are available down to EM1 Sleep. From EM2 Deep Sleep onwards these oscillators and clocks are normally off, although special cases exist as summarized in [Table 12.5 Oscillator and Clock Availability in Energy Modes on page 341](#) and [Table 11.2 EMU Energy Mode Overview on page 252](#). The CMU overview figure in [Figure 12.1 CMU Overview - High Frequency Portion on page 318](#) and [Figure 12.2 CMU Overview - Low Frequency Portion on page 319](#) also indicate which oscillators and clocks can be used in what energy modes.

The low frequency oscillators (LFRCO and LFXO) are available in all energy modes except in EM3 Stop when they are off by definition. Default these oscillators are also off in EM4 Hibernate and EM4 Shutoff, but they can be retained on in these states as well if needed. The ultra low frequency oscillator (ULFRCO) is default on in all energy modes, except for EM4 Shutoff, but it can be retained on in that mode as well if needed. The low frequency clocks (LFACLK, LFBCLK, LFECLK, WDOGnCLK, RFSENSECLK, and CRYOCLK) are in various power domains and therefore their availability not only depends on the chosen clock source, but also on the chosen energy mode as indicated in [Table 12.5 Oscillator and Clock Availability in Energy Modes on page 341](#).

**Table 12.5. Oscillator and Clock Availability in Energy Modes**

|  | EM0 Active/EM1 Sleep | EM2 Deep Sleep  | EM3 Stop        | EM4 Hibernate            | EM4 Shutoff              |
|--|----------------------|-----------------|-----------------|--------------------------|--------------------------|
| HFRCO  | On <sup>1</sup>      | Off             | Off             | Off                      | Off                      |
| HFXO   | On <sup>1</sup>      | Off             | Off             | Off                      | Off                      |
| AUXHFRCO   | On <sup>1</sup>      | On <sup>2</sup> | On <sup>2</sup> | Off                      | Off                      |
| LFRCO, LFXO  | On <sup>1</sup>      | On <sup>1</sup> | Off             | Retained on <sup>3</sup> | Retained on <sup>3</sup> |
| ULFRCO   | On                   | On              | On              | On                       | Retained on <sup>3</sup> |
| HFSRCLK, HFCLK, HFCORECLK, HFBUSCLK, HFPERCLK, HFRADIOCLK, HFCLKLE | On <sup>1</sup>      | Off             | Off             | Off                      | Off                      |
| AUXCLK   | On <sup>1</sup>      | On <sup>2</sup> | On <sup>2</sup> | Off                      | Off                      |
| ADCnCLK  | On <sup>1</sup>      | On <sup>4</sup> | On <sup>4</sup> | Off                      | Off                      |
| LFACLK, LFBCLK   | On <sup>1</sup>      | On <sup>1</sup> | On <sup>5</sup> | Off                      | Off                      |
| LFECLK   | On <sup>1</sup>      | On <sup>1</sup> | On <sup>5</sup> | Retained on <sup>3</sup> | Off                      |
| WDOGnCLK   | On <sup>1</sup>      | On <sup>1</sup> | On <sup>5</sup> | Off                      | Off                      |
| CRYOCLK  | On <sup>1</sup>      | On <sup>1</sup> | On <sup>5</sup> | Retained on <sup>3</sup> | Retained on <sup>3</sup> |

**Note:**

1. Under software control.
2. Default off, but kept active if used by the ADC.
3. Default off, but can be retained on.
4. Will be kept on if AUXHFRCO is selected as clock source.
5. On only if ULFRCO is used as clock source.

### 12.3.5 Clock Output on a Pin

It is possible to configure the CMU to output clocks on the CMU\_CLK0, CMU\_CLK1 and CMU\_CLK2 pins. This clock selection is done using the CLKOUTSEL0, CLKOUTSEL1 and CLKOUTSEL2 bitfields respectively in CMU\_CTRL. The required output pins must be enabled in the CMU\_ROUTEPEN register and the pin locations can be configured in the CMU\_ROUTELOC0 register. The following clocks can be output on a pin:

- HFSRCCLK and HFEXPCLK. The HFSRCCLK is the high frequency clock before any prescaling has been applied. The HFEXPCLK is a prescaled version of HFCLK as controlled by the HFEXPPRESC bitfield in the CMU\_HFPRESC register.
- The unqualified clock output from any of the oscillators (ULFRCO, LFRCO, LFXO, HFXO). Note that these unqualified clocks can exhibit glitches or skewed duty-cycle during startup and therefore these clock outputs are normally not used before observing the related ready flag being set to 1 in CMU\_STATUS.
- The qualified clock from any of the oscillators (ULFRCO, LFRCO, LFXO, HFXO, HFRCO, AUXHFRCO). A qualified clock will not have any glitches or skewed duty-cycle during startup. For LFRCO, LFXO and HFXO correct configuration of the TIMEOUT bitfield(s) in CMU\_LFRCOCTRL, CMU\_LFXOCTRL and CMU\_HFXOTIMEOUTCTRL respectively is required to guarantee a properly qualified clock.

HFCLK will not have a 50-50 duty cycle when any other division factor than 1 is used in CMU\_HFPRESC (i.e. if PRESC is not equal to 0). In such a case, the exported HFEXPCLK will therefore also not be 50-50 when its division factor is not set to an even number in CMU\_HFEXPPRESC.

### 12.3.6 Clock Input From a Pin

It is possible to configure the CMU to input a low-frequency (< 1 MHz) clock from the CMU\_CLKI0. This clock can be selected to drive HFSRCCLK reference using CMU\_HFCLKSEL. The required input pin must be enabled in the CMU\_ROUTEPEN register and the pin location can be configured in the CMU\_ROUTELOC1 register.

### 12.3.7 Clock Output on PRS

The CMU can be used as a PRS producer. It can output clocks onto PRS which can be selected by a consumer as CMUCLKOUT0, CMUCLKOUT1 and CMUCLKOUT2. The clocks which can be produced via CMUCLKOUT0, CMUCLKOUT1 and CMUCLKOUT2 are selected via the CLKOUTSEL0, CLKOUTSEL1 and CLKOUTSEL2 fields respectively in CMU\_CTRL.

Note that the CLKOUTSEL0 and CLKOUTSEL1 fields are also used for selecting which clock is output onto a pin as described in [12.3.5 Clock Output on a Pin](#). In contrast with clock output on a pin however, output of a clock onto PRS does not depend on any configuration of the CMU\_ROUTEPEN and CMU\_ROUTELOC0 registers.

### 12.3.8 Error Handling

Certain restrictions apply to how and when the CMU registers can be configured as is described for the respective registers. Not adhering to these restrictions can lead to unpredictable and non-defined behaviour. Some of these software restrictions are checked in hardware and not adhering to them will cause the CMUERR interrupt flag in CMU\_IF to be set to 1. The restrictions impacting CMUERR are as follows:

- CMU\_HFRCOCTRL should not be written while HFRCOBSY in the CMU\_SYNCBUSY register is set to 1.
- CMU\_AUXHFRCOCTRL should not be written while AUXHFRCOBSY in the CMU\_SYNCBUSY register is set to 1.
- CMU\_HFXOSTARTUPCTRL, CMU\_HFXOSTEADYSTATECTRL and CMU\_HFXOTIMEOUTCTRL should not be written while HFXOBSY in the CMU\_SYNCBUSY register is set to 1. Note that writes to CMU\_HFXOCTRL do not impact CMUERR. Although most of its bitfields need to be configured before enabling the HFXO, it is allowed to change the AUTOSTART bits (i.e. AUTOSTARTRDYSELRAC, AUTOSTARTSELEM0EM1 and AUTOSTARTEM0EM1) at any time.
- HFXO should not be enabled before it has been properly disabled (so only enable HFXO when HFXOENS=0 or HFXOBSY=0). Likewise, HFXO should not be disabled before it has been properly enabled (so only disable HFXO when HFXOENS=1 or HFXOBSY=0).
- CMU\_LFRCOCTRL should not be written while LFRCOBSY in the CMU\_SYNCBUSY register is set to 1. The GMCCURTUNE bitfield should not be written with a differing value while the LFRCOVREFBSY flag is set to 1.
- CMU\_LFXOCTRL should not be written while LFXOBSY in the CMU\_SYNCBUSY register is set to 1.

### 12.3.9 Interrupts

The interrupts generated by the CMU module are combined into one interrupt vector. If CMU interrupts are enabled, an interrupt will be made if one or more of the interrupt flags in CMU\_IF and their corresponding bits in CMU\_IEN are set.

### 12.3.10 Wake-up

The CMU can be (partially) active all the way down to EM4 Shutoff. It can wake up the CPU from EM2 upon LFRCO or LFXO becoming ready as LFRCORDY and LFXORDY can be used as wake-up interrupt.

### 12.3.11 Protection

It is possible to lock the control- and command registers to prevent unintended software writes to critical clock settings. This is controlled by the CMU\_LOCK register.

### 12.3.12 Precision Low Frequency Oscillator

The PLFRCO, Precision Low Frequency RC Oscillator, is a 500ppm RC oscillator that eliminates the need for a 32.768kHz crystal by automatically recalibrating itself against the HFXO. The PLFRCO can support energy modes EM0/1/2. Do not use the PLFRCO for any peripheral that can run in EM4H or EM4S since the PLFRCO will be powered down in EM4H and EM4S.

Several times a second the PLFRCO will check for a relative change in temperature. If the temperature change is large enough, the PLFRCO will start up the HFXO and recalibrate to maintain 500ppm. The temperature checking is also performed in EM2, and the PLFRCO can wake up from EM2, go to EM1, start the HFXO, recalibrate, and go back to EM2 automatically without any software interaction.

To enable the PLFRCO set PLFRCOEN in CMU\_OSCENCMD. After being enabled the PLFRCO will perform a one time base calibration to determine the minimum and maximum frequencies of the oscillator, perform a calibration to adjust its finetrim tuning, and take a relative temperature measurement. The temperature measurement is not correlated to a specific temperature in degrees centigrade. The temperature measurement is a part specific measurement allowing the PLFRCO to determine when the temperature has changed by a small amount. Once a large enough temperature change has occurred, the PLFRCO will recalibrate against the HFXO. The default settings assume an HFXO frequency of 38.4MHz.

Starting the HFXO uses more power, so the PLFRCO's use of a temperature change detection significantly reduces the power usage by only recalibrating when the temperature has actually changed.

Once the initial base calibration has completed, the PLFRCORDY in CMU\_STATUS will go high to indicate that the 32768 Hz clock is ready to use. Disabling the PLFRCO is done by setting PLFRCODIS in CMU\_OSCENCMD. PLFRCOENS in CMU\_STATUS shows the status of the PLFRCOEN and PLFRCODIS commands. When the PLFRCO is disabled, there will be a few more additional low frequency cycles before the PLFRCO shuts down and disables the PLFRCO clock. The PLFRCORDY can be used to determine when the PLFRCO clock is ready to use and when the PLFRCO has completed shutting down. Do not set the PLFRCOEN until after PLFRCORDY has gone low.

PLFRCOHFXODNSERR in CMU\_IF indicates some error conditions such as the HFXO has not been configured properly or stopped running, or an HFXO crystal other than 38.4MHz was used.

## 12.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name                    | Type  | Description   |
|--------|-------------------------|-------|---|
| 0x000  | CMU_CTRL                | RW    | CMU Control Register  |
| 0x010  | CMU_HFRCCOCTRL          | RWH   | HFRCCO Control Register   |
| 0x018  | CMU_AUXHFRCCOCTRL       | RW    | AUXHFRCCO Control Register  |
| 0x020  | CMU_LFRCCOCTRL          | RW    | LFRCCO Control Register   |
| 0x024  | CMU_HFXOCTRL            | RW    | HFXO Control Register   |
| 0x02C  | CMU_HFXOSTARTUPCTRL     | RW    | HFXO Startup Control  |
| 0x030  | CMU_HFXOSTEADYSTATECTRL | RW    | HFXO Steady State Control   |
| 0x034  | CMU_HFXOTIMEOUTCTRL     | RW    | HFXO Timeout Control  |
| 0x038  | CMU_LFXOCTRL            | RW    | LFXO Control Register   |
| 0x050  | CMU_CALCTRL             | RW    | Calibration Control Register                                      |
| 0x054  | CMU_CALCNT              | RWH   | Calibration Counter Register                                      |
| 0x060  | CMU_OSCENCMD            | W1    | Oscillator Enable/Disable Command Register                        |
| 0x064  | CMU_CMD                 | W1    | Command Register  |
| 0x070  | CMU_DBGCLKSEL           | RW    | Debug Trace Clock Select  |
| 0x074  | CMU_HFCLKSEL            | W1    | High Frequency Clock Select Command Register                      |
| 0x080  | CMU_LFACLKSEL           | RW    | Low Frequency A Clock Select Register                             |
| 0x084  | CMU_LFBCLKSEL           | RW    | Low Frequency B Clock Select Register                             |
| 0x088  | CMU_LFECLKSEL           | RW    | Low Frequency E Clock Select Register                             |
| 0x090  | CMU_STATUS              | R     | Status Register   |
| 0x094  | CMU_HFCLKSTATUS         | R     | HFCLK Status Register   |
| 0x09C  | CMU_HFXOTRIMSTATUS      | R     | HFXO Trim Status  |
| 0x0A0  | CMU_IF                  | R     | Interrupt Flag Register   |
| 0x0A4  | CMU_IFS                 | W1    | Interrupt Flag Set Register                                       |
| 0x0A8  | CMU_IFC                 | (R)W1 | Interrupt Flag Clear Register                                     |
| 0x0AC  | CMU_IEN                 | RW    | Interrupt Enable Register   |
| 0x0B0  | CMU_HFBUSCLKEN0         | RW    | High Frequency Bus Clock Enable Register 0                        |
| 0x0C0  | CMU_HFPERCLKEN0         | RW    | High Frequency Peripheral Clock Enable Register 0                 |
| 0x0CC  | CMU_HFRADIOALTCLKEN0    | RW    | High Frequency Alternate Radio Peripheral Clock Enable Register 0 |
| 0x0E0  | CMU_LFACLKEN0           | RW    | Low Frequency a Clock Enable Register 0 (Async Reg)               |
| 0x0E8  | CMU_LFBCLKEN0           | RW    | Low Frequency B Clock Enable Register 0 (Async Reg)               |
| 0x0F0  | CMU_LFECLKEN0           | RW    | Low Frequency E Clock Enable Register 0 (Async Reg)               |
| 0x100  | CMU_HFPRESC             | RW    | High Frequency Clock Prescaler Register                           |
| 0x108  | CMU_HFCOREPRESC         | RW    | High Frequency Core Clock Prescaler Register                      |
| 0x10C  | CMU_HFPERPRESC          | RW    | High Frequency Peripheral Clock Prescaler Register                |
| 0x110  | CMU_HFRADIOPRESC        | RW    | High Frequency Radio Peripheral Clock Prescaler Register          |

| Offset | Name                | Type | Description  |
|--------|---------------------|------|--|
| 0x114  | CMU_HFEXPPRESC      | RW   | High Frequency Export Clock Prescaler Register                     |
| 0x120  | CMU_LFAPRESC0       | RW   | Low Frequency a Prescaler Register 0 (Async Reg)                   |
| 0x128  | CMU_LFBPRESC0       | RW   | Low Frequency B Prescaler Register 0 (Async Reg)                   |
| 0x130  | CMU_LFEPRESC0       | RW   | Low Frequency E Prescaler Register 0 (Async Reg)                   |
| 0x138  | CMU_HFRADIOALTPRESC | RW   | High Frequency Alternate Radio Peripheral Clock Prescaler Register |
| 0x140  | CMU_SYNCBUSY        | R    | Synchronization Busy Register                                      |
| 0x144  | CMU_FREEZE          | RW   | Freeze Register  |
| 0x150  | CMU_PCNTCTRL        | RWH  | PCNT Control Register  |
| 0x15C  | CMU_ADCCTRL         | RWH  | ADC Control Register   |
| 0x170  | CMU_ROUTEPEN        | RW   | I/O Routing Pin Enable Register                                    |
| 0x174  | CMU_ROUTELOC0       | RW   | I/O Routing Location Register                                      |
| 0x178  | CMU_ROUTELOC1       | RW   | I/O Routing Location Register                                      |
| 0x180  | CMU_LOCK            | RWH  | Configuration Lock Register  |

## 12.5 Register Description

## 12.5.1 CMU\_CTRL - CMU Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |             |           |    |    |    |    |    |        |    |    |    |   |   |            |   |   |            |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|-------------|-----------|----|----|----|----|----|--------|----|----|----|---|---|------------|---|---|------------|---|---|---|---|
| 0x000         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20          | 19        | 18 | 17 | 16 | 15 | 14 | 13     | 12 | 11 | 10 | 9 | 8 | 7          | 6 | 5 | 4          | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    | 1           | 1         |    |    |    |    |    | 0      |    |    |    |   |   | 0x00       |   |   | 0x00       |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    | RW          | RW        |    |    |    |    |    | RW     |    |    |    |   |   | RW         |   |   | RW         |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    | HFRADIOCKEN | HFPERCKEN |    |    |    |    |    | WSHFLE |    |    |    |   |   | CLKOUTSEL1 |   |   | CLKOUTSEL0 |   |   |   |   |

| Bit   | Name            | Reset   | Access                            | Description  |
|-------|-----------------|---|-----------------------------------|--|
| 31:22 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                   |  |
| 21    | HFRADIOCKEN     | 1   | RW                                | <b>HFRADIOCLK Enable</b><br>Set to enable the HFRADIOCLK.  |
| 20    | HFPERCKEN       | 1   | RW                                | <b>HFPERCLK Enable</b><br>Set to enable the HFPERCLK.  |
| 19:17 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                   |  |
| 16    | WSHFLE          | 0   | RW                                | <b>Wait State for High-Frequency LE Interface</b><br>Set to allow access to LE peripherals when running HFBUSCLK <sub>LE</sub> at frequencies higher than 32 MHz |
| 15:10 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                   |  |
| 9:5   | CLKOUTSEL1      | 0x00  | RW                                | <b>Clock Output Select 1</b><br>Controls the clock output 1 multiplexer. To actually output on the pin, set CLKOUT1PEN in CMU_ROUTE.                             |
|       | Value           | Mode  | Description                       |  |
|       | 0               | DISABLED  | Disabled                          |  |
|       | 1               | ULFRCO  | ULFRCO (directly from oscillator) |  |
|       | 2               | LFRCO   | LFRCO (directly from oscillator)  |  |
|       | 3               | LFXO  | LFXO (directly from oscillator)   |  |
|       | 6               | HFXO  | HFXO (directly from oscillator)   |  |
|       | 7               | HFEXPCLK  | HFEXPCLK                          |  |
|       | 9               | ULFRCOQ   | ULFRCO (qualified)                |  |
|       | 10              | LFRCOQ  | LFRCO (qualified)                 |  |
|       | 11              | LFXOQ   | LFXO (qualified)                  |  |
|       | 12              | HFRCOQ  | HFRCO (qualified)                 |  |
|       | 13              | AUXHFRCOQ   | AUXHFRCO (qualified)              |  |

| Bit | Name       | Reset     | Access | Description  |
|-----|------------|-----------|--------|--|
|     | 14         | HFXOQ     |        | HFXO (qualified)   |
|     | 15         | HFSRCCLK  |        | HFSRCCLK   |
|     | 16         | PLFRCO    |        | PLFRCO (directly from oscillator)  |
|     | 17         | PLFRCOQ   |        | PLFRCO (qualified)   |
| 4:0 | CLKOUTSEL0 | 0x00      | RW     | <b>Clock Output Select 0</b><br>Controls the clock output multiplexer. To actually output on the pin, set CLKOUT0PEN in CMU_ROUTE. |
|     | Value      | Mode      |        | Description  |
|     | 0          | DISABLED  |        | Disabled   |
|     | 1          | ULFRCO    |        | ULFRCO (directly from oscillator)  |
|     | 2          | LFRCO     |        | LFRCO (directly from oscillator)   |
|     | 3          | LFXO      |        | LFXO (directly from oscillator)  |
|     | 6          | HFXO      |        | HFXO (directly from oscillator)  |
|     | 7          | HFEXPCLK  |        | HFEXPCLK   |
|     | 9          | ULFRCOQ   |        | ULFRCO (qualified)   |
|     | 10         | LFRCOQ    |        | LFRCO (qualified)  |
|     | 11         | LFXOQ     |        | LFXO (qualified)   |
|     | 12         | HFRCOQ    |        | HFRCO (qualified)  |
|     | 13         | AUXHFRCOQ |        | AUXHFRCO (qualified)   |
|     | 14         | HFXOQ     |        | HFXO (qualified)   |
|     | 15         | HFSRCCLK  |        | HFSRCCLK   |
|     | 16         | PLFRCO    |        | PLFRCO (directly from oscillator)  |
|     | 17         | PLFRCOQ   |        | PLFRCO (qualified)   |

### 12.5.2 CMU\_HFRCTRL - HFRCO Control Register

Write this register to set the frequency band in which the HFRCO is to operate. Always update all fields in this register at once by writing the value for the desired band, which has been obtained from the Device Information page entry for that band. The TUNING, FINE-TUNING, FINETUNINGEN and CLKDIV bitfields can be used to tune a specific band (FREQRANGE) of the oscillator to a non-preconfigured frequency. When changing this setting there will be no glitches on the HFRCO output, hence it is safe to change this setting

even while the system is running on the HFRCO. Only write CMU\_HFRCOCTRL when it is ready for an update as indicated by HFRCOBSY=0 in CMU\_SYNCBUSY.

| Offset        | Bit Position |    |    |              |        |    |    |       |         |    |    |           |     |    |    |            |     |    |    |        |     |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|--------------|--------|----|----|-------|---------|----|----|-----------|-----|----|----|------------|-----|----|----|--------|-----|----|---|---|---|---|---|---|---|---|---|---|
| 0x010         | 31           | 30 | 29 | 28           | 27     | 26 | 25 | 24    | 23      | 22 | 21 | 20        | 19  | 18 | 17 | 16         | 15  | 14 | 13 | 12     | 11  | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0xB          |    |    | 0            | 0x0    |    |    | 1     | 0x2     |    |    | 0x08      |     |    |    | 0x1F       |     |    |    | 0x7F   |     |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> | RWH          |    |    | RWH          | RWH    |    |    | RWH   | RWH     |    |    |           | RWH |    |    |            | RWH |    |    |        | RWH |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | VREFTC       |    |    | FINETUNINGEN | CLKDIV |    |    | LDOHP | CMPBIAS |    |    | FREQRANGE |     |    |    | FINETUNING |     |    |    | TUNING |     |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:28 | VREFTC          | 0xB   | RWH    | <b>HFRCO Temperature Coefficient Trim on Comparator Reference</b><br>Writing this field adjusts the temperature coefficient trim on comparator reference.                           |
| 27    | FINETUNINGEN    | 0   | RWH    | <b>Enable Reference for Fine Tuning</b><br>Settings this bit enables HFRCO fine tuning.   |
| 26:25 | CLKDIV          | 0x0   | RWH    | <b>Locally Divide HFRCO Clock Output</b><br>Writing this field configures the HFRCO clock output divider.   |
|       | Value           | Mode  |        | Description   |
|       | 0               | DIV1  |        | Divide by 1.  |
|       | 1               | DIV2  |        | Divide by 2.  |
|       | 2               | DIV4  |        | Divide by 4.  |
| 24    | LDOHP           | 1   | RWH    | <b>HFRCO LDO High Power Mode</b><br>Settings this bit puts the HFRCO LDO in high power mode.  |
| 23:21 | CMPBIAS         | 0x2   | RWH    | <b>HFRCO Comparator Bias Current</b><br>Writing this field adjusts the HFRCO comparator bias current.   |
| 20:16 | FREQRANGE       | 0x08  | RWH    | <b>HFRCO Frequency Range</b><br>Writing this field adjusts the HFRCO frequency range.   |
| 15:14 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 13:8  | FINETUNING      | 0x1F  | RWH    | <b>HFRCO Fine Tuning Value</b><br>Writing this field adjusts the HFRCO fine tuning value. Higher value means lower frequency. Fine tuning is only enabled when FINETUNINGEN is set. |
| 7     | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 6:0   | TUNING          | 0x7F  | RWH    | <b>HFRCO Tuning Value</b><br>Writing this field adjusts the HFRCO tuning value. Higher value means lower frequency.   |

### 12.5.3 CMU\_AUXHFRCOCTRL - AUXHFRCO Control Register

Write this register with the production calibrated values from the Device Info pages. The TUNING, FINETUNING, FINETUNINGEN and CLKDIV bitfields can be used to tune a specific band (FREQRANGE) of the oscillator to a non-preconfigured frequency. Only write CMU\_AUXHFRCOCTRL when it is ready for an update as indicated by AUXHFRCOBSY=0 in CMU\_SYNCBUSY.

| Offset        | Bit Position |    |    |              |        |    |    |       |         |    |    |           |    |    |    |    |    |            |    |    |    |    |   |        |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|--------------|--------|----|----|-------|---------|----|----|-----------|----|----|----|----|----|------------|----|----|----|----|---|--------|---|---|---|---|---|---|---|---|
| 0x018         | 31           | 30 | 29 | 28           | 27     | 26 | 25 | 24    | 23      | 22 | 21 | 20        | 19 | 18 | 17 | 16 | 15 | 14         | 13 | 12 | 11 | 10 | 9 | 8      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0xB          |    |    | 0            | 0x0    |    |    | 1     | 0x2     |    |    | 0x08      |    |    |    |    |    | 0x1F       |    |    |    |    |   | 0x7F   |   |   |   |   |   |   |   |   |
| <b>Access</b> | RW           |    |    | RW           | RW     |    |    | RW    | RW      |    |    | RW        |    |    |    |    |    | RW         |    |    |    |    |   | RW     |   |   |   |   |   |   |   |   |
| <b>Name</b>   | VREFTC       |    |    | FINETUNINGEN | CLKDIV |    |    | LDOHP | CMPBIAS |    |    | FREQRANGE |    |    |    |    |    | FINETUNING |    |    |    |    |   | TUNING |   |   |   |   |   |   |   |   |

| Bit   | Name            | Reset   | Access | Description  |       |      |             |   |      |              |   |      |              |   |      |              |
|-------|-----------------|---|--------|--|-------|------|-------------|---|------|--------------|---|------|--------------|---|------|--------------|
| 31:28 | VREFTC          | 0xB   | RW     | <b>AUXHFRCO Temperature Coefficient Trim on Comparator Reference</b><br><br>Writing this field adjusts the temperature coefficient trim on comparator reference.   |       |      |             |   |      |              |   |      |              |   |      |              |
| 27    | FINETUNINGEN    | 0   | RW     | <b>Enable Reference for Fine Tuning</b><br><br>Settings this bit enables AUXHFRCO fine tuning.   |       |      |             |   |      |              |   |      |              |   |      |              |
| 26:25 | CLKDIV          | 0x0   | RW     | <b>Locally Divide AUXHFRCO Clock Output</b><br><br>Writing this field configures the AUXHFRCO clock output divider.<br><table border="1" data-bbox="207 1094 1500 1289"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>DIV1</td> <td>Divide by 1.</td> </tr> <tr> <td>1</td> <td>DIV2</td> <td>Divide by 2.</td> </tr> <tr> <td>2</td> <td>DIV4</td> <td>Divide by 4.</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | DIV1 | Divide by 1. | 1 | DIV2 | Divide by 2. | 2 | DIV4 | Divide by 4. |
| Value | Mode            | Description   |        |  |       |      |             |   |      |              |   |      |              |   |      |              |
| 0     | DIV1            | Divide by 1.  |        |  |       |      |             |   |      |              |   |      |              |   |      |              |
| 1     | DIV2            | Divide by 2.  |        |  |       |      |             |   |      |              |   |      |              |   |      |              |
| 2     | DIV4            | Divide by 4.  |        |  |       |      |             |   |      |              |   |      |              |   |      |              |
| 24    | LDOHP           | 1   | RW     | <b>AUXHFRCO LDO High Power Mode</b><br><br>Settings this bit puts the AUXHFRCO LDO in high power mode.   |       |      |             |   |      |              |   |      |              |   |      |              |
| 23:21 | CMPBIAS         | 0x2   | RW     | <b>AUXHFRCO Comparator Bias Current</b><br><br>Writing this field adjusts the AUXHFRCO comparator bias current.  |       |      |             |   |      |              |   |      |              |   |      |              |
| 20:16 | FREQRANGE       | 0x08  | RW     | <b>AUXHFRCO Frequency Range</b><br><br>Writing this field adjusts the AUXHFRCO frequency range.  |       |      |             |   |      |              |   |      |              |   |      |              |
| 15:14 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |      |              |   |      |              |   |      |              |
| 13:8  | FINETUNING      | 0x1F  | RW     | <b>AUXHFRCO Fine Tuning Value</b><br><br>Writing this field adjusts the AUXHFRCO fine tuning value. Higher value means lower frequency. Fine tuning is only enabled when FINETUNINGEN is set.  |       |      |             |   |      |              |   |      |              |   |      |              |
| 7     | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |      |              |   |      |              |   |      |              |
| 6:0   | TUNING          | 0x7F  | RW     | <b>AUXHFRCO Tuning Value</b><br><br>Writing this field adjusts the AUXHFRCO tuning value. Higher value means lower frequency.  |       |      |             |   |      |              |   |      |              |   |      |              |

## 12.5.4 CMU\_LFRCOCTRL - LFRCO Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |         |    |    |    |            |    |    |    |    |    |    |    |       |    |   |   |        |   |   |   |        |   |   |   |  |  |  |  |        |  |  |  |
|---------------|--------------|----|----|----|----|----|----|----|---------|----|----|----|------------|----|----|----|----|----|----|----|-------|----|---|---|--------|---|---|---|--------|---|---|---|--|--|--|--|--------|--|--|--|
| 0x020         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23      | 22 | 21 | 20 | 19         | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11    | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3      | 2 | 1 | 0 |  |  |  |  |        |  |  |  |
| <b>Reset</b>  | 0x8          |    |    |    |    |    |    |    | 0x1     |    |    |    | 0x0        |    |    |    |    |    |    |    |       |    |   |   | 0x100  |   |   |   |        |   |   |   |  |  |  |  |        |  |  |  |
| <b>Access</b> | RW           |    |    |    |    |    |    |    | RW      |    |    |    |            |    |    |    | RW |    |    |    |       |    |   |   | RW     |   |   |   |        |   |   |   |  |  |  |  |        |  |  |  |
| <b>Name</b>   | GMCCURTUNE   |    |    |    |    |    |    |    | TIMEOUT |    |    |    | VREFUPDATE |    |    |    |    |    |    |    | ENDEM |    |   |   | ENCHOP |   |   |   | ENVREF |   |   |   |  |  |  |  | TUNING |  |  |  |

| Bit   | Name            | Reset   | Access | Description  |       |      |             |   |          |                            |   |          |                             |   |           |                             |   |           |             |
|-------|-----------------|---|--------|--|-------|------|-------------|---|----------|----------------------------|---|----------|-----------------------------|---|-----------|-----------------------------|---|-----------|-------------|
| 31:28 | GMCCURTUNE      | 0x8   | RW     | <b>Tuning of Gmc Current</b><br>Set to tune GMC current. This field is updated with the production calibrated value during reset, and the reset value might therefore vary between devices.  |       |      |             |   |          |                            |   |          |                             |   |           |                             |   |           |             |
| 27:26 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |          |                            |   |          |                             |   |           |                             |   |           |             |
| 25:24 | TIMEOUT         | 0x1   | RW     | <b>LFRCO Timeout</b><br>Configures the start-up delay for LFRCO. Do not change while LFRCO is enabled. When starting up the LFRCO after it has been completely turned off, use TIMEOUT=16cycles. If the LFRCO has been retained on in EM4, then the TIMEOUT=2cycles configuration is also allowed when re-enabling the LFRCO after EM4 exit (as it is still running).<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>2CYCLES</td> <td>Timeout period of 2 cycles</td> </tr> <tr> <td>1</td> <td>16CYCLES</td> <td>Timeout period of 16 cycles</td> </tr> <tr> <td>2</td> <td>32CYCLES</td> <td>Timeout period of 32 cycles</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | 2CYCLES  | Timeout period of 2 cycles | 1 | 16CYCLES | Timeout period of 16 cycles | 2 | 32CYCLES  | Timeout period of 32 cycles |   |           |             |
| Value | Mode            | Description   |        |  |       |      |             |   |          |                            |   |          |                             |   |           |                             |   |           |             |
| 0     | 2CYCLES         | Timeout period of 2 cycles  |        |  |       |      |             |   |          |                            |   |          |                             |   |           |                             |   |           |             |
| 1     | 16CYCLES        | Timeout period of 16 cycles   |        |  |       |      |             |   |          |                            |   |          |                             |   |           |                             |   |           |             |
| 2     | 32CYCLES        | Timeout period of 32 cycles   |        |  |       |      |             |   |          |                            |   |          |                             |   |           |                             |   |           |             |
| 23:22 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |          |                            |   |          |                             |   |           |                             |   |           |             |
| 21:20 | VREFUPDATE      | 0x0   | RW     | <b>Control Vref Update Rate</b><br>Specify Vref update rate. This field can be updated with the production test value during reset, and the reset value might therefore differ.<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>32CYCLES</td> <td>32 clocks.</td> </tr> <tr> <td>1</td> <td>64CYCLES</td> <td>64 clocks.</td> </tr> <tr> <td>2</td> <td>128CYCLES</td> <td>128 clocks.</td> </tr> <tr> <td>3</td> <td>256CYCLES</td> <td>256 clocks.</td> </tr> </tbody> </table>  | Value | Mode | Description | 0 | 32CYCLES | 32 clocks.                 | 1 | 64CYCLES | 64 clocks.                  | 2 | 128CYCLES | 128 clocks.                 | 3 | 256CYCLES | 256 clocks. |
| Value | Mode            | Description   |        |  |       |      |             |   |          |                            |   |          |                             |   |           |                             |   |           |             |
| 0     | 32CYCLES        | 32 clocks.  |        |  |       |      |             |   |          |                            |   |          |                             |   |           |                             |   |           |             |
| 1     | 64CYCLES        | 64 clocks.  |        |  |       |      |             |   |          |                            |   |          |                             |   |           |                             |   |           |             |
| 2     | 128CYCLES       | 128 clocks.   |        |  |       |      |             |   |          |                            |   |          |                             |   |           |                             |   |           |             |
| 3     | 256CYCLES       | 256 clocks.   |        |  |       |      |             |   |          |                            |   |          |                             |   |           |                             |   |           |             |
| 19    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |          |                            |   |          |                             |   |           |                             |   |           |             |
| 18    | ENDEM           | 1   | RW     | <b>Enable Dynamic Element Matching</b><br>Set to enable dynamic element matching. This improves average frequency accuracy at the cost of increased jitter.  |       |      |             |   |          |                            |   |          |                             |   |           |                             |   |           |             |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 17   | ENCHOP          | 1   | RW     | <b>Enable Comparator Chopping</b><br>Set to enable comparator chopping. This improves average frequency accuracy at the cost of increased jitter.   |
| 16   | ENVREF          | 0   | RW     | <b>Enable Duty Cycling of Vref</b><br>Set to enable duty cycling of vref. Clear during calibration of LFRCO. Only change when LFRCO is off.   |
| 15:9 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 8:0  | TUNING          | 0x100   | RW     | <b>LFRCO Tuning Value</b><br>Writing this field adjusts the LFRCO frequency (the higher the value, the lower the frequency). This field is updated with the production calibrated value during reset, and the reset value might therefore vary between devices. |

## 12.5.5 CMU\_HFXOCTRL - HFXO Control Register

| Offset        | Bit Position |                        |                        |                     |    |    |           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |         |          |    |   |   |                         |   |   |   |      |
|---------------|--------------|------------------------|------------------------|---------------------|----|----|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|---------|----------|----|---|---|-------------------------|---|---|---|------|
| 0x024         | 31           | 30                     | 29                     | 28                  | 27 | 26 | 25        | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10      | 9       | 8        | 7  | 6 | 5 | 4                       | 3 | 2 | 1 | 0    |
| <b>Reset</b>  |              | 0                      | 0                      | 0                   |    |    | 0x0       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         | 0       | 0        | 0  |   |   | 0x0                     |   |   |   | 0    |
| <b>Access</b> |              | RW                     | RW                     | RW                  |    |    | RW        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         | RW      | RW       | RW |   |   | RW                      |   |   |   | RW   |
| <b>Name</b>   |              | AUTOSTARTRDYSEL<br>RAC | AUTOSTARTSELE<br>M0EM1 | AUTOSTARTEM0<br>EM1 |    |    | LFTIMEOUT |    |    |    |    |    |    |    |    |    |    |    |    |    |    | XTO2GND | XTI2GND | LOWPOWER |    |   |   | PEAKDETSHUN<br>TOPTMODE |   |   |   | MODE |

| Bit   | Name                    | Reset   | Access                                | Description  |
|-------|-------------------------|---|---------------------------------------|--|
| 31    | <i>Reserved</i>         | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                       |  |
| 30    | AUTOSTARTRDY-<br>SELRAC | 0   | RW                                    | <b>Automatically Start HFXO on RAC Wake-up and Select It Upon HFXO Ready</b><br><br>This bit enables automatic HFXO start-up and HFXO selection when ready on RAC wake-up. Allowed to change at any time.  |
| 29    | AUTOSTARTSE-<br>LEM0EM1 | 0   | RW                                    | <b>Automatically Start and Select of HFXO Upon EM0/EM1 Entry From EM2/EM3</b><br><br>This bit enables automatic start-up and immediate selection of the HFXO when in EM0/EM1 (also after entry from EM2/EM3). Note that setting this bit to 1 will stall HFSRCCLK until HFXO becomes ready. Allowed to change at any time. |
| 28    | AUTOSTAR-<br>TEM0EM1    | 0   | RW                                    | <b>Automatically Start of HFXO Upon EM0/EM1 Entry From EM2/EM3</b><br><br>This bit enables automatic start-up of the HFXO when in EM0/EM1 (also after entry from EM2/EM3) without causing an automatic HFXO selection. Allowed to change at any time.  |
| 27    | <i>Reserved</i>         | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                       |  |
| 26:24 | LFTIMEOUT               | 0x0   | RW                                    | <b>HFXO Low Frequency Timeout</b><br><br>Configures the start-up delay for HFXO measured in LFECLK cycles. Only change when both HFXO and LFECLK are off.  |
|       | Value                   | Mode  | Description                           |  |
|       | 0                       | 0CYCLES   | Timeout period of 0 cycles (disabled) |  |
|       | 1                       | 2CYCLES   | Timeout period of 2 cycles            |  |
|       | 2                       | 4CYCLES   | Timeout period of 4 cycles            |  |
|       | 3                       | 16CYCLES  | Timeout period of 16 cycles           |  |
|       | 4                       | 32CYCLES  | Timeout period of 32 cycles           |  |
|       | 5                       | 64CYCLES  | Timeout period of 64 cycles           |  |
|       | 6                       | 1KCYCLES  | Timeout period of 1024 cycles         |  |
|       | 7                       | 4KCYCLES  | Timeout period of 4096 cycles         |  |

| Bit   | Name                     | Reset   | Access  | Description  |
|-------|--------------------------|---|---|--|
| 23:11 | <i>Reserved</i>          | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 10    | XTO2GND                  | 0   | RW  | <b>Clamp HFXTAL_P Pin to Ground When HFXO Oscillator is Off</b><br>Set to enable grounding of HFXTAL_P pin when HFXO oscillator is off   |
| 9     | XTI2GND                  | 0   | RW  | <b>Clamp HFXTAL_N Pin to Ground When HFXO Oscillator is Off</b><br>Set to enable grounding of HFXTAL_N pin when HFXO oscillator is off. Do not enable if MODE=EXTCLK and an external source is supplied.   |
| 8     | LOWPOWER                 | 0   | RW  | <b>Low Power Mode Control</b><br>Set LOWPOWER=0 for RF performance. Set LOWPOWER=1 for non RF performance (not compatible with Radio operation).   |
| 7:6   | <i>Reserved</i>          | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 5:4   | PEAKDETSHUN-<br>TOPTMODE | 0x0   | RW  | <b>HFXO Automatic Peak Detection and Shunt Current Optimization Mode</b><br>Set to AUTOCMD to allow automatic HFXO peak detection and shunt current optimization (MANUAL mode provides direct control of IBTRIMXOCORE, REGISH, PEAKDETEN, REGSELILOW). |
|       | Value                    | Mode  | Description   |  |
|       | 0                        | AUTOCMD   | Automatic control of HFXO peak detection and shunt optimization sequences. CMU_CMD HFXOPEAKDETSTART and HFXOSHUNTOPTSTART can also be used.               |  |
|       | 1                        | CMD   | CMU_CMD HFXOPEAKDETSTART and HFXOSHUNTOPTSTART can be used to trigger peak detection and shunt optimization sequences.                                    |  |
|       | 2                        | MANUAL  | CMU_HFXOSTEADYSTATECTRL IBTRIMXOCORE, REGISH, REGSELILOW, and PEAKDETEN are under full software control and are allowed to be changed once HFXO is ready. |  |
| 3:1   | <i>Reserved</i>          | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 0     | MODE                     | 0   | RW  | <b>HFXO Mode</b><br>Set this to configure the external source for the HFXO. The oscillator setting takes effect when 1 is written to HFXOEN in CMU_OSCENCMD.   |
|       | Value                    | Mode  | Description   |  |
|       | 0                        | XTAL  | 38 MHz - 40 MHz crystal oscillator  |  |
|       | 1                        | EXTCLK  | External clock can be supplied (square or wave) on HFXTAL_N pin.  |  |

12.5.6 CMU\_HFXOSTARTUPCTRL - HFXO Startup Control

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |       |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |              |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|-------|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|--------------|---|---|---|
| 0x02C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19    | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3            | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    | 0x0A0 |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0x20         |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    | RW    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | RW           |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    | CTUNE |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | IBTRIMXOCORE |   |   |   |

| Bit   | Name         | Reset   | Access | Description  |
|-------|--------------|---|--------|--|
| 31:20 | Reserved     | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 19:11 | CTUNE        | 0x0A0   | RW     | <p><b>Sets Oscillator Tuning Capacitance</b></p> <p>This CTUNE value is applied during the startup phase of the HFXO. Capacitance on HFXTAL_N and HFXTAL_P (pF) = Ctune = Cpar + CTUNE&lt;8:0&gt; X 40fF. Max Ctune 25pF (CLmax ~12.5pF). CL(DNLmax)=50fF ~ 0.6ppm (12.5ppm/pF).</p> |
| 10:7  | Reserved     | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 6:0   | IBTRIMXOCORE | 0x20  | RW     | <p><b>Sets the Startup Oscillator Core Bias Current</b></p> <p>This IBTRIMXOCORE value is applied during the startup phase of the HFXO. Current (uA) = IBTRIMXOCORE X 40uA. Bits 6 and 5 may only me high in the crystal oscillator startup phase.</p>                               |

## 12.5.7 CMU\_HFXOSTEADYSTATECTRL - HFXO Steady State Control

| Offset        | Bit Position |    |    |    |    |           |            |    |    |    |    |    |    |    |    |    |    |    |    |    |       |    |   |   |        |   |   |              |   |   |   |   |  |  |
|---------------|--------------|----|----|----|----|-----------|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|----|---|---|--------|---|---|--------------|---|---|---|---|--|--|
| 0x030         | 31           | 30 | 29 | 28 | 27 | 26        | 25         | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11    | 10 | 9 | 8 | 7      | 6 | 5 | 4            | 3 | 2 | 1 | 0 |  |  |
| <b>Reset</b>  | 0xA          |    |    |    |    | 0         | 0x3        |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x168 |    |   |   | 0xA    |   |   | 0x07         |   |   |   |   |  |  |
| <b>Access</b> | RW           |    |    |    |    | RW        | RW         |    |    |    |    |    |    |    |    |    |    |    |    |    | RW    |    |   |   | RW     |   |   | RW           |   |   |   |   |  |  |
| <b>Name</b>   | REGISHUPPER  |    |    |    |    | PEAKDETEN | REGSELILOW |    |    |    |    |    |    |    |    |    |    |    |    |    | CTUNE |    |   |   | REGISH |   |   | IBTRIMXOCORE |   |   |   |   |  |  |

| Bit   | Name         | Reset  | Access | Description  |
|-------|--------------|--|--------|--|
| 31:28 | REGISHUPPER  | 0xA  | RW     | <p><b>Set Regulator Output Current Level (shunt Regulator). Ish = 120uA + REGISHUPPER X 120uA</b></p> <p>Set to steady state value of REGISH + 3.</p>  |
| 27    | Reserved     | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 26    | PEAKDETEN    | 0  | RW     | <p><b>Enables Oscillator Peak Detectors</b></p> <p>Direct control allowed when PEAKDETSHUNTOPTMODE=MANUAL and HFXO is ready.</p>   |
| 25:24 | REGSELILOW   | 0x3  | RW     | <p><b>Controls Regulator Minimum Shunt Current Detection Relative to Nominal</b></p> <p>Steady state used during HFXO FSM. Direct control allowed when PEAKDETSHUNTOPTMODE=MANUAL and HFXO is ready.</p>   |
| 23:20 | Reserved     | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 19:11 | CTUNE        | 0x168  | RW     | <p><b>Sets Oscillator Tuning Capacitance</b></p> <p>This CTUNE value is applied during the steady state phase of the HFXO (as well as during the peak detection and shunt current optimization algorithms). Capacitance on HFXTAL_N and HFXTAL_P (pF) = Ctune = Cpar + CTUNE&lt;8:0&gt; X 40fF. Max Ctune 25pF (CLmax ~12.5pF). CL(DNLmax)=50fF ~ 0.6ppm (12.5ppm/pF).</p>   |
| 10:7  | REGISH       | 0xA  | RW     | <p><b>Sets the Steady State Regulator Output Current Level (shunt Regulator)</b></p> <p>This REGISH value is applied during the steady state phase of the HFXO. Direct control allowed when PEAKDETSHUNTOPTMODE=MANUAL and HFXO is ready. Ish = 120uA + REGISH X 120uA.</p>  |
| 6:0   | IBTRIMXOCORE | 0x07   | RW     | <p><b>Sets the Steady State Oscillator Core Bias Current.</b></p> <p>This IBTRIMXOCORE value is applied during the steady state phase of the HFXO. It is also used as the initial value during the peak detection algorithm. Direct control allowed when PEAKDETSHUNTOPTMODE=MANUAL and HFXO is ready. Current (uA) = IBTRIMXOCORE x 40uA. Bits 6 and 5 may only be high in the crystal oscillator startup phase..</p> |

## 12.5.8 CMU\_HFXOTIMEOUTCTRL - HFXO Timeout Control

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |                 |    |    |    |                |    |    |    |    |    |   |   |               |   |   |   |                |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|-----------------|----|----|----|----------------|----|----|----|----|----|---|---|---------------|---|---|---|----------------|---|---|---|
| 0x034         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19              | 18 | 17 | 16 | 15             | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7             | 6 | 5 | 4 | 3              | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    | 0x2             |    |    |    | 0xA            |    |    |    |    |    |   |   | 0x6           |   |   |   | 0x7            |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    | RW              |    |    |    | RW             |    |    |    |    |    |   |   | RW            |   |   |   | RW             |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    | SHUNTOPTTIMEOUT |    |    |    | PEAKDETTIMEOUT |    |    |    |    |    |   |   | STEADYTIMEOUT |   |   |   | STARTUPTIMEOUT |   |   |   |

| Bit   | Name  | Reset  | Access                         | Description  |
|-------|---|--|--------------------------------|--|
| 31:20 | Reserved  | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |                                |  |
| 19:16 | SHUNTOPTTIMEOUT   | 0x2  | RW                             | <b>Wait Duration in HFXO Shunt Current Optimization Wait State</b> |
|       | Wait duration depends on the chosen XTAL (expected value is around 1 us). Program the desired duration measured in cycles of (at least) 83 ns.              |  |                                |  |
|       | Value   | Mode   | Description                    |  |
|       | 0   | 2CYCLES  | Timeout period of 2 cycles     |  |
|       | 1   | 4CYCLES  | Timeout period of 4 cycles     |  |
|       | 2   | 16CYCLES   | Timeout period of 16 cycles    |  |
|       | 3   | 32CYCLES   | Timeout period of 32 cycles    |  |
|       | 4   | 256CYCLES  | Timeout period of 256 cycles   |  |
|       | 5   | 1KCYCLES   | Timeout period of 1024 cycles  |  |
|       | 6   | 2KCYCLES   | Timeout period of 2048 cycles  |  |
|       | 7   | 4KCYCLES   | Timeout period of 4096 cycles  |  |
|       | 8   | 8KCYCLES   | Timeout period of 8192 cycles  |  |
|       | 9   | 16KCYCLES  | Timeout period of 16384 cycles |  |
|       | 10  | 32KCYCLES  | Timeout period of 32768 cycles |  |
| 15:12 | PEAKDETTIMEOUT  | 0xA  | RW                             | <b>Wait Duration in HFXO Peak Detection Wait State</b>             |
|       | Wait duration depends on the chosen XTAL (expected value is between 25 us and 200 us). Program the desired duration measured in cycles of (at least) 83 ns. |  |                                |  |
|       | Value   | Mode   | Description                    |  |
|       | 0   | 2CYCLES  | Timeout period of 2 cycles     |  |
|       | 1   | 4CYCLES  | Timeout period of 4 cycles     |  |
|       | 2   | 16CYCLES   | Timeout period of 16 cycles    |  |
|       | 3   | 32CYCLES   | Timeout period of 32 cycles    |  |

| Bit  | Name            | Reset   | Access | Description                    |
|------|-----------------|---|--------|--------------------------------|
|      | 4               | 256CYCLES   |        | Timeout period of 256 cycles   |
|      | 5               | 1KCYCLES  |        | Timeout period of 1024 cycles  |
|      | 6               | 2KCYCLES  |        | Timeout period of 2048 cycles  |
|      | 7               | 4KCYCLES  |        | Timeout period of 4096 cycles  |
|      | 8               | 8KCYCLES  |        | Timeout period of 8192 cycles  |
|      | 9               | 16KCYCLES   |        | Timeout period of 16384 cycles |
|      | 10              | 32KCYCLES   |        | Timeout period of 32768 cycles |
| 11:8 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |                                |

7:4 STEADYTIMEOUT 0x6 RW **Wait Duration in HFXO Startup Steady Wait State**

Wait duration depends on the chosen XTAL (expected value is around 100 us). Program the desired duration measured in cycles of (at least) 83 ns.

| Value | Mode      | Description                    |
|-------|-----------|--------------------------------|
| 0     | 2CYCLES   | Timeout period of 2 cycles     |
| 1     | 4CYCLES   | Timeout period of 4 cycles     |
| 2     | 16CYCLES  | Timeout period of 16 cycles    |
| 3     | 32CYCLES  | Timeout period of 32 cycles    |
| 4     | 256CYCLES | Timeout period of 256 cycles   |
| 5     | 1KCYCLES  | Timeout period of 1024 cycles  |
| 6     | 2KCYCLES  | Timeout period of 2048 cycles  |
| 7     | 4KCYCLES  | Timeout period of 4096 cycles  |
| 8     | 8KCYCLES  | Timeout period of 8192 cycles  |
| 9     | 16KCYCLES | Timeout period of 16384 cycles |
| 10    | 32KCYCLES | Timeout period of 32768 cycles |

3:0 STARTUPTIMEOUT 0x7 RW **Wait Duration in HFXO Startup Enable Wait State**

Wait duration depends on the chosen XTAL (expected value is between 100 us and 1600 us). Program the desired duration measured in cycles of (at least) 83 ns.

| Value | Mode      | Description                   |
|-------|-----------|-------------------------------|
| 0     | 2CYCLES   | Timeout period of 2 cycles    |
| 1     | 4CYCLES   | Timeout period of 4 cycles    |
| 2     | 16CYCLES  | Timeout period of 16 cycles   |
| 3     | 32CYCLES  | Timeout period of 32 cycles   |
| 4     | 256CYCLES | Timeout period of 256 cycles  |
| 5     | 1KCYCLES  | Timeout period of 1024 cycles |
| 6     | 2KCYCLES  | Timeout period of 2048 cycles |
| 7     | 4KCYCLES  | Timeout period of 4096 cycles |
| 8     | 8KCYCLES  | Timeout period of 8192 cycles |

| Bit | Name | Reset     | Access | Description                    |
|-----|------|-----------|--------|--------------------------------|
| 9   |      | 16KCYCLES |        | Timeout period of 16384 cycles |
| 10  |      | 32KCYCLES |        | Timeout period of 32768 cycles |

## 12.5.9 CMU\_LFXOCTRL - LFXO Control Register

| Offset        | Bit Position |    |    |    |    |         |    |    |    |    |    |    |        |    |    |    |    |    |     |    |     |          |    |   |    |      |    |   |    |      |   |   |  |  |  |    |        |  |
|---------------|--------------|----|----|----|----|---------|----|----|----|----|----|----|--------|----|----|----|----|----|-----|----|-----|----------|----|---|----|------|----|---|----|------|---|---|--|--|--|----|--------|--|
| 0x038         | 31           | 30 | 29 | 28 | 27 | 26      | 25 | 24 | 23 | 22 | 21 | 20 | 19     | 18 | 17 | 16 | 15 | 14 | 13  | 12 | 11  | 10       | 9  | 8 | 7  | 6    | 5  | 4 | 3  | 2    | 1 | 0 |  |  |  |    |        |  |
| <b>Reset</b>  |              |    |    |    |    | 0x7     |    |    |    |    |    |    | 0      |    |    |    |    |    | 0x0 |    | 1   | 0        |    |   |    | 0x2  |    |   |    | 0x0  |   |   |  |  |  |    | 0x00   |  |
| <b>Access</b> |              |    |    |    |    | RW      |    |    |    |    |    |    | RW     |    |    |    |    |    | RW  | RW | RW  |          | RW |   | RW |      | RW |   | RW |      |   |   |  |  |  | RW |        |  |
| <b>Name</b>   |              |    |    |    |    | TIMEOUT |    |    |    |    |    |    | BUFCUR |    |    |    |    |    | CUR |    | AGC | HIGHAMPL |    |   |    | GAIN |    |   |    | MODE |   |   |  |  |  |    | TUNING |  |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:27 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 26:24 | TIMEOUT         | 0x7   | RW     | <b>LFXO Timeout</b><br><br>Configures the start-up delay for LFXO. Do not change while LFXO is enabled. When starting up the LFXO after it has been completely turned off, use the TIMEOUT setting required by the XTAL. If the LFXO has been retained on in EM4, then the TIMEOUT=2cycles configuration is also allowed when re-enabling the LFXO after EM4 exit (as it is still running). |
|       | Value           | Mode  |        | Description   |
|       | 0               | 2CYCLES   |        | Timeout period of 2 cycles  |
|       | 1               | 256CYCLES   |        | Timeout period of 256 cycles  |
|       | 2               | 1KCYCLES  |        | Timeout period of 1024 cycles   |
|       | 3               | 2KCYCLES  |        | Timeout period of 2048 cycles   |
|       | 4               | 4KCYCLES  |        | Timeout period of 4096 cycles   |
|       | 5               | 8KCYCLES  |        | Timeout period of 8192 cycles   |
|       | 6               | 16KCYCLES   |        | Timeout period of 16384 cycles  |
|       | 7               | 32KCYCLES   |        | Timeout period of 32768 cycles  |
| 23:21 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 20    | BUFCUR          | 0   | RW     | <b>LFXO Buffer Bias Current</b><br><br>The default value is intended to cover all use cases and reprogramming is not recommended. Do not change while LFXO is enabled.  |
| 19:18 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 17:16 | CUR             | 0x0   | RW     | <b>LFXO Current Trim</b><br><br>The default value is intended to cover all use cases and reprogramming is not recommended. Do not change while LFXO is enabled.   |
| 15    | AGC             | 1   | RW     | <b>LFXO AGC Enable</b><br><br>Set this bit to enable automatic gain control which limits XTAL oscillation amplitude. Do not change while LFXO is enabled.   |
| 14    | HIGHAMPL        | 0   | RW     | <b>LFXO High XTAL Oscillation Amplitude Enable</b><br><br>Set this bit to enable high XTAL oscillation amplitude. Do not change while LFXO is enabled.  |
| 13    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |

| Bit   | Name            | Reset   | Access   | Description  |
|-------|-----------------|---|--|--|
| 12:11 | GAIN            | 0x2   | RW   | <b>LFXO Startup Gain</b><br><br>The optimal value for maximum startup margin depends on the chosen XTAL. Refer to the device data sheet or Simplicity Studio for more information.   |
| 10    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |  |
| 9:8   | MODE            | 0x0   | RW   | <b>LFXO Mode</b><br><br>Set this to configure the external source for the LFXO. Do not change while LFXO is enabled. The oscillator setting takes effect when 1 is written to LFXOEN in CMU_OSCENCMD. The oscillator setting is reset to default when 1 is written to LFXODIS in CMU_OSCENCMD.                               |
|       | Value           | Mode  | Description  |  |
|       | 0               | XTAL  | 32768 Hz crystal oscillator  |  |
|       | 1               | BUFEXTCLK   | An AC coupled buffer is coupled in series with LFX TAL_N pin, suitable for external sinus wave (32768 Hz). |  |
|       | 2               | DIGEXTCLK   | Digital external clock on LFX TAL_N pin. Oscillator is effectively by-passed.                              |  |
| 7     | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |  |
| 6:0   | TUNING          | 0x00  | RW   | <b>LFXO Internal Capacitor Array Tuning Value</b><br><br>Writing this field adjusts the internal load capacitance connected between LFX TAL_P and ground and LFX TAL_N and ground symmetrically (the higher the value, the higher the capacitance, the lower the frequency). Only increment or decrement by 1 LSB at a time. |

### 12.5.10 CMU\_CALCTRL - Calibration Control Register

| Offset        | Bit Position |    |    |    |            |    |    |    |    |    |    |    |          |    |    |    |    |    |    |    |      |     |         |   |   |   |   |   |   |   |       |   |
|---------------|--------------|----|----|----|------------|----|----|----|----|----|----|----|----------|----|----|----|----|----|----|----|------|-----|---------|---|---|---|---|---|---|---|-------|---|
| 0x050         | 31           | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19       | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11   | 10  | 9       | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0 |
| <b>Reset</b>  |              |    |    |    | 0x0        |    |    |    |    |    |    |    | 0x0      |    |    |    |    |    |    |    | 0    | 0x0 |         |   |   |   |   |   |   |   |       |   |
| <b>Access</b> |              |    |    |    | RW         |    |    |    |    |    |    |    | RW       |    |    |    |    |    |    |    | RW   | 0   | RW      |   |   |   |   |   |   |   | RW    |   |
| <b>Name</b>   |              |    |    |    | PRSDOWNSEL |    |    |    |    |    |    |    | PRSUPSEL |    |    |    |    |    |    |    | CONT | 0   | DOWNSEL |   |   |   |   |   |   |   | UPSEL |   |

| Bit   | Name            | Reset   | Access | Description |
|-------|-----------------|---|--------|-------------|
| 31:28 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |             |

|       |            |         |                                  |  |
|-------|------------|---------|----------------------------------|--|
| 27:24 | PRSDOWNSEL | 0x0     | RW                               | <b>PRS Select for PRS Input When Selected in DOWNSEL</b><br>Select PRS input for PRS based calibration. Only change when calibration circuit is off. |
|       | Value      | Mode    | Description                      |  |
|       | 0          | PRSCH0  | PRS Channel 0 selected as input  |  |
|       | 1          | PRSCH1  | PRS Channel 1 selected as input  |  |
|       | 2          | PRSCH2  | PRS Channel 2 selected as input  |  |
|       | 3          | PRSCH3  | PRS Channel 3 selected as input  |  |
|       | 4          | PRSCH4  | PRS Channel 4 selected as input  |  |
|       | 5          | PRSCH5  | PRS Channel 5 selected as input  |  |
|       | 6          | PRSCH6  | PRS Channel 6 selected as input  |  |
|       | 7          | PRSCH7  | PRS Channel 7 selected as input  |  |
|       | 8          | PRSCH8  | PRS Channel 8 selected as input  |  |
|       | 9          | PRSCH9  | PRS Channel 9 selected as input  |  |
|       | 10         | PRSCH10 | PRS Channel 10 selected as input |  |
|       | 11         | PRSCH11 | PRS Channel 11 selected as input |  |

|       |                 |   |  |  |
|-------|-----------------|---|--|--|
| 23:20 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |  |
|-------|-----------------|---|--|--|

|       |          |        |                                 |  |
|-------|----------|--------|---------------------------------|--|
| 19:16 | PRSUPSEL | 0x0    | RW                              | <b>PRS Select for PRS Input When Selected in UPSEL</b><br>Select PRS input for PRS based calibration. Only change when calibration circuit is off. |
|       | Value    | Mode   | Description                     |  |
|       | 0        | PRSCH0 | PRS Channel 0 selected as input |  |
|       | 1        | PRSCH1 | PRS Channel 1 selected as input |  |
|       | 2        | PRSCH2 | PRS Channel 2 selected as input |  |
|       | 3        | PRSCH3 | PRS Channel 3 selected as input |  |
|       | 4        | PRSCH4 | PRS Channel 4 selected as input |  |

| Bit  | Name            | Reset   | Access  | Description   |
|------|-----------------|---|---|---|
|      | 5               | PRSCH5  |   | PRS Channel 5 selected as input   |
|      | 6               | PRSCH6  |   | PRS Channel 6 selected as input   |
|      | 7               | PRSCH7  |   | PRS Channel 7 selected as input   |
|      | 8               | PRSCH8  |   | PRS Channel 8 selected as input   |
|      | 9               | PRSCH9  |   | PRS Channel 9 selected as input   |
|      | 10              | PRSCH10   |   | PRS Channel 10 selected as input  |
|      | 11              | PRSCH11   |   | PRS Channel 11 selected as input  |
| 15:9 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |
| 8    | CONT            | 0   | RW  | <b>Continuous Calibration</b><br>Set this bit to enable continuous calibration  |
| 7:4  | DOWNSEL         | 0x0   | RW  | <b>Calibration Down-counter Select</b><br>Selects clock source for the calibration down-counter. Only change when calibration circuit is off. |
|      | Value           | Mode  | Description   |   |
|      | 0               | HFCLK   | Select HFCLK for down-counter                           |   |
|      | 1               | HFXO  | Select HFXO for down-counter                            |   |
|      | 2               | LFXO  | Select LFXO for down-counter                            |   |
|      | 3               | HFRCO   | Select HFRCO for down-counter                           |   |
|      | 4               | LFRCO   | Select LFRCO for down-counter                           |   |
|      | 5               | AUXHFRCO  | Select AUXHFRCO for down-counter                        |   |
|      | 6               | PRS   | Select PRS input selected by PRSDOWNSEL as down-counter |   |
|      | 9               | PLFRCO  | Select PLFRCO for down-counter                          |   |
| 3:0  | UPSEL           | 0x0   | RW  | <b>Calibration Up-counter Select</b><br>Selects clock source for the calibration up-counter. Only change when calibration circuit is off.     |
|      | Value           | Mode  | Description   |   |
|      | 0               | HFXO  | Select HFXO as up-counter                               |   |
|      | 1               | LFXO  | Select LFXO as up-counter                               |   |
|      | 2               | HFRCO   | Select HFRCO as up-counter                              |   |
|      | 3               | LFRCO   | Select LFRCO as up-counter                              |   |
|      | 4               | AUXHFRCO  | Select AUXHFRCO as up-counter                           |   |
|      | 5               | PRS   | Select PRS input selected by PRSUPSEL as up-counter     |   |
|      | 8               | PLFRCO  | Select PLFRCO as up-counter                             |   |

12.5.11 CMU\_CALCNT - Calibration Counter Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x054         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19      | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    | 0x00000 |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    | RWH     |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    | CALCNT  |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description                |
|-------|----------|--|--------|----------------------------|
| 31:20 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |                            |
| 19:0  | CALCNT   | 0x00000  | RWH    | <b>Calibration Counter</b> |

Write top value before calibration. Read calibration result from this register when Calibration Ready flag has been set.

## 12.5.12 CMU\_OSCENCMD - Oscillator Enable/Disable Command Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |           |          |    |    |    |    |   |   |   |   |   |   |         |        |          |         |             |            |         |        |          |         |    |    |    |    |    |    |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------|----------|----|----|----|----|---|---|---|---|---|---|---------|--------|----------|---------|-------------|------------|---------|--------|----------|---------|----|----|----|----|----|----|----|
| 0x060         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15        | 14       | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3       | 2      | 1        | 0       |             |            |         |        |          |         |    |    |    |    |    |    |    |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0         | 0        |    |    |    |    |   |   |   |   |   |   | 0       | 0      | 0        | 0       | 0           | 0          | 0       | 0      | 0        | 0       | 0  | 0  |    |    |    |    |    |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W1        | W1       |    |    |    |    |   |   |   |   |   |   | W1      | W1     | W1       | W1      | W1          | W1         | W1      | W1     | W1       | W1      | W1 | W1 | W1 | W1 | W1 | W1 | W1 |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PLFRCODIS | PLFRCOEN |    |    |    |    |   |   |   |   |   |   | LFXODIS | LFXOEN | LFRCODIS | LFRCOEN | AUXHFRCODIS | AUXHFRCOEN | HFXODIS | HFXOEN | HFRCODIS | HFRCOEN |    |    |    |    |    |    |    |

| Bit   | Name        | Reset  | Access | Description   |
|-------|-------------|--|--------|---|
| 31:16 | Reserved    | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 15    | PLFRCODIS   | 0  | W1     | <b>PLFRCO Disable</b><br>Disables the PLFRCO. PLFRCOEN has higher priority if written simultaneously.   |
| 14    | PLFRCOEN    | 0  | W1     | <b>PLFRCO Enable</b><br>Enables the PLFRCO.   |
| 13:10 | Reserved    | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 9     | LFXODIS     | 0  | W1     | <b>LFXO Disable</b><br>Disables the LFXO. LFXOEN has higher priority if written simultaneously. WARNING: Do not disable the LFXO if this oscillator is selected as the source for HFCLK. When waking up from EM4 make sure EM4UNLATCH in EMU_CMD is set for this to take effect     |
| 8     | LFXOEN      | 0  | W1     | <b>LFXO Enable</b><br>Enables the LFXO. When waking up from EM4 make sure EM4UNLATCH in EMU_CMD is set for this to take effect  |
| 7     | LFRCODIS    | 0  | W1     | <b>LFRCO Disable</b><br>Disables the LFRCO. LFRCOEN has higher priority if written simultaneously. WARNING: Do not disable the LFRCO if this oscillator is selected as the source for HFCLK. When waking up from EM4 make sure EM4UNLATCH in EMU_CMD is set for this to take effect |
| 6     | LFRCOEN     | 0  | W1     | <b>LFRCO Enable</b><br>Enables the LFRCO. When waking up from EM4 make sure EM4UNLATCH in EMU_CMD is set for this to take effect  |
| 5     | AUXHFRCODIS | 0  | W1     | <b>AUXHFRCO Disable</b><br>Disables the AUXHFRCO. AUXHFRCOEN has higher priority if written simultaneously.   |
| 4     | AUXHFRCOEN  | 0  | W1     | <b>AUXHFRCO Enable</b><br>Enables the AUXHFRCO.   |
| 3     | HFXODIS     | 0  | W1     | <b>HFXO Disable</b><br>Disables the HFXO. HFXOEN has higher priority if written simultaneously. WARNING: Do not disable the HFXO if this oscillator is selected as the source for HFCLK.  |
| 2     | HFXOEN      | 0  | W1     | <b>HFXO Enable</b><br>Enables the HFXO.   |

| Bit | Name     | Reset | Access | Description  |
|-----|----------|-------|--------|--|
| 1   | HFRCODIS | 0     | W1     | <b>HFRCO Disable</b><br><br>Disables the HFRCO. HFRCOEN has higher priority if written simultaneously. WARNING: Do not disable the HFRCO if this oscillator is selected as the source for HFCLK. |
| 0   | HFRCOEN  | 0     | W1     | <b>HFRCO Enable</b><br><br>Enables the HFRCO.  |

### 12.5.13 CMU\_CMD - Command Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |                   |                  |   |   |   |         |          |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|-------------------|------------------|---|---|---|---------|----------|---|
| 0x064         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6                | 5 | 4 | 3 | 2       | 1        | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0                 | 0                |   |   | 0 | 0       |          |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | W1                | W1               |   |   |   | W1      | W1       |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | HFXOSHUNTOPTSTART | HFXOPEAKDETSTART |   |   |   | CALSTOP | CALSTART |   |

| Bit  | Name                   | Reset   | Access | Description  |
|------|------------------------|---|--------|--|
| 31:6 | <i>Reserved</i>        | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 5    | HFXOSHUNTOPT-<br>START | 0   | W1     | <b>HFXO Shunt Current Optimization Start</b><br><br>Starts the HFXO Shunt Current Optimization and runs it one time.                     |
| 4    | HFXOPEAKDET-<br>START  | 0   | W1     | <b>HFXO Peak Detection Start</b><br><br>Starts the HFXO peak detection and runs it one time.   |
| 3:2  | <i>Reserved</i>        | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 1    | CALSTOP                | 0   | W1     | <b>Calibration Stop</b><br><br>Stops the calibration counters.   |
| 0    | CALSTART               | 0   | W1     | <b>Calibration Start</b><br><br>Starts the calibration, effectively loading the CMU_CALCNT into the down-counter and start decrementing. |

## 12.5.14 CMU\_DBGCLKSEL - Debug Trace Clock Select

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |     |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|-----|---|---|---|---|
| 0x070         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4   | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | 0x0 |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | RW  |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | DBG |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description  |
|------|----------|--|--------|--|
| 31:1 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 0:0  | DBG      | 0x0  | RW     | <b>Debug Trace Clock</b><br>Select clock used for debug trace. |
|      | Value    | Mode   |        | Description  |
|      | 0        | AUXHFRCO   |        | AUXHFRCO is the debug trace clock                              |
|      | 1        | HFCLK  |        | HFCLK is the debug trace clock                                 |

## 12.5.15 CMU\_HFCLKSEL - High Frequency Clock Select Command Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |     |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|-----|---|---|---|---|
| 0x074         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4   | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | 0x0 |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | W1  |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | HF  |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description  |
|------|----------|--|--------|--|
| 31:3 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 2:0  | HF       | 0x0  | W1     | <b>HFCLK Select</b><br>Selects the clock source for HFCLK. Note that selecting an oscillator that is disabled will cause the system clock to stop. Check the status register and confirm that oscillator is ready before switching. If the system can deal with a temporarily stopped system clock, then it is okay to switch to an oscillator as soon as the status register indicates that the oscillator has been enabled successfully. |
|      | Value    | Mode   |        | Description  |
|      | 1        | HFRCO  |        | Select HFRCO as HFCLK  |
|      | 2        | HFXO   |        | Select HFXO as HFCLK   |
|      | 3        | LFRCO  |        | Select LFRCO as HFCLK  |
|      | 4        | LFXO   |        | Select LFXO as HFCLK   |
|      | 5        | HFRCODIV2  |        | Select HFRCO divided by 2 as HFCLK   |
|      | 7        | CLKIN0   |        | Select CLKIN0 as HFCLK   |

12.5.16 CMU\_LFACLKSEL - Low Frequency A Clock Select Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |     |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|-----|---|---|---|---|
| 0x080         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4   | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | 2 | 1   | 0 |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | RW  |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | LFA |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description |
|------|----------|--|--------|-------------|
| 31:3 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |             |

|                                      |       |          |                           |                             |
|--------------------------------------|-------|----------|---------------------------|-----------------------------|
| 2:0                                  | LFA   | 0x0      | RW                        | <b>Clock Select for LFA</b> |
| Selects the clock source for LFACLK. |       |          |                           |                             |
|                                      | Value | Mode     | Description               |                             |
|                                      | 0     | DISABLED | LFACLK is disabled        |                             |
|                                      | 1     | LFRCO    | LFRCO selected as LFACLK  |                             |
|                                      | 2     | LFXO     | LFXO selected as LFACLK   |                             |
|                                      | 4     | ULFRCO   | ULFRCO selected as LFACLK |                             |
|                                      | 5     | PLFRCO   | PLFRCO selected as LFACLK |                             |

## 12.5.17 CMU\_LFBCLKSEL - Low Frequency B Clock Select Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |     |     |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|-----|-----|---|---|---|---|
| 0x084         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5   | 4   | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | LFB | 0x0 |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | RW  |     |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | LFB |     |   |   |   |   |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 31:3 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 2:0  | LFB             | 0x0   | RW     | <b>Clock Select for LFB</b><br>Selects the clock source for LFBCLK. |
|      | Value           | Mode  |        | Description   |
|      | 0               | DISABLED  |        | LFBCLK is disabled  |
|      | 1               | LFRCO   |        | LFRCO selected as LFBCLK  |
|      | 2               | LFXO  |        | LFXO selected as LFBCLK   |
|      | 3               | HFCLKLE   |        | HFCLK divided by two/four is selected as LFBCLK                     |
|      | 4               | ULFRCO  |        | ULFRCO selected as LFBCLK   |
|      | 5               | PLFRCO  |        | PLFRCO selected as LFBCLK   |

12.5.18 CMU\_LFECLKSEL - Low Frequency E Clock Select Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |     |     |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|-----|-----|---|---|---|---|
| 0x088         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5   | 4   | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | LFE | 0x0 |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | RW  |     |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | LFE |     |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description |
|------|----------|--|--------|-------------|
| 31:3 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |             |

2:0 LFE 0x0 RW **Clock Select for LFE**  
 Selects the clock source for LFECLK. When waking up from EM4 make sure EM4UNLATCH in EMU\_CMD is set for this to take effect

| Value | Mode     | Description               |
|-------|----------|---------------------------|
| 0     | DISABLED | LFECLK is disabled        |
| 1     | LFRCO    | LFRCO selected as LFECLK  |
| 2     | LFXO     | LFXO selected as LFECLK   |
| 4     | ULFRCO   | ULFRCO selected as LFECLK |
| 5     | PLFRCO   | PLFRCO selected as LFECLK |

## 12.5.19 CMU\_STATUS - Status Register

| Offset        | Bit Position |             |             |             |           |            |            |             |                 |                |         |    |    |    |    |        |           |           |    |    |    |    |         |         |         |          |            |             |         |         |         |          |
|---------------|--------------|-------------|-------------|-------------|-----------|------------|------------|-------------|-----------------|----------------|---------|----|----|----|----|--------|-----------|-----------|----|----|----|----|---------|---------|---------|----------|------------|-------------|---------|---------|---------|----------|
| 0x090         | 31           | 30          | 29          | 28          | 27        | 26         | 25         | 24          | 23              | 22             | 21      | 20 | 19 | 18 | 17 | 16     | 15        | 14        | 13 | 12 | 11 | 10 | 9       | 8       | 7       | 6        | 5          | 4           | 3       | 2       | 1       | 0        |
| <b>Reset</b>  |              | 0           | 0           | 0           | 0         | 0          | 0          | 0           | 0               | 0              | 0       |    |    |    |    | 1      | 0         | 0         |    |    |    |    | 0       | 0       | 0       | 0        | 0          | 0           | 0       | 0       | 1       | 1        |
| <b>Access</b> |              | R           | R           | R           | R         | R          | R          | R           | R               | R              | R       |    |    |    |    | R      | R         | R         |    |    |    |    | R       | R       | R       | R        | R          | R           | R       | R       | R       | R        |
| <b>Name</b>   |              | PLFRCOPHASE | ULFRCOPHASE | LFRFCOPHASE | LFXOPHASE | HFXOREGLOW | HFXOAMPLOW | HFXOAMPHIGH | HFXOSHUNTOPTRDY | HFXOPEAKDETRDY | HFXOREQ |    |    |    |    | CALRDY | PLFRCORDY | PLFRCOENS |    |    |    |    | LFXORDY | LFXOENS | LFXORDY | LFRCOENS | AUXHFCORDY | AUXHFRCOENS | HFXORDY | HFXOENS | HFXORDY | HFRCOENS |

| Bit | Name            | Reset | Access | Description  |
|-----|-----------------|-------|--------|--|
| 31  | <i>Reserved</i> |       |        | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i>  |
| 30  | PLFRCOPHASE     | 0     | R      | <b>PLFRCO Clock Phase</b><br>Used to determine if PLFRCO is in high or low phase.  |
| 29  | ULFRCOPHASE     | 0     | R      | <b>ULFRCO Clock Phase</b><br>Used to determine if ULFRCO is in high or low phase.  |
| 28  | LFRFCOPHASE     | 0     | R      | <b>LFRCO Clock Phase</b><br>Used to determine if LFRCO is in high or low phase.  |
| 27  | LFXOPHASE       | 0     | R      | <b>LFXO Clock Phase</b><br>Used to determine if LFXO is in high or low phase.  |
| 26  | HFXOREGLOW      | 0     | R      | <b>HFXO Regulator Shunt Current Too Low</b><br>HFXO regulator shunt current too low. When using PEAKDETSRUNTOPTMODE=MANUAL, the REGISH value in CMU_HFXOSTEADYSTATECTRL should be tuned up by 1 LSB.   |
| 25  | HFXOAMPLOW      | 0     | R      | <b>HFXO Amplitude Tuning Value Too Low</b><br>HFXO oscillation amplitude is too low. When using PEAKDETSRUNTOPTMODE=MANUAL, the IBTRIMXOCORE value in CMU_HFXOSTEADYSTATECTRL should be tuned up by 1 LSB.   |
| 24  | HFXOAMPHIGH     | 0     | R      | <b>HFXO Oscillation Amplitude is Too High</b><br>HFXO oscillation amplitude is too high. When using PEAKDETSRUNTOPTMODE=MANUAL, the IBTRIMXOCORE value in CMU_HFXOSTEADYSTATECTRL should be tuned down by 1 LSB.   |
| 23  | HFXOSHUNTOPTRDY | 0     | R      | <b>HFXO Shunt Current Optimization Ready</b><br>HFXO shunt current optimization is ready.  |
| 22  | HFXOPEAKDETRDY  | 0     | R      | <b>HFXO Peak Detection Ready</b><br>HFXO peak detection is ready.  |
| 21  | HFXOREQ         | 0     | R      | <b>HFXO is Required By Hardware</b><br>HFXO is required by another hardware block and HFXO should typically not be disabled or deselected. Whether disabling or deselecting of the HFXO can be performed and whether this leads to setting of HFXODISERR depends on whether the HFXO enable/select conditions are met. |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 20:17 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 16    | CALRDY          | 1   | R      | <b>Calibration Ready</b><br>Calibration is Ready (0 when calibration is ongoing).                    |
| 15    | PLFRCORDY       | 0   | R      | <b>PLFRCO Ready</b><br>PLFRCO is enabled and start-up time has exceeded.                             |
| 14    | PLFRCOENS       | 0   | R      | <b>PLFRCO Enable Status</b><br>PLFRCO is enabled (shows disabled status if EM4 repaint is required). |
| 13:10 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 9     | LFXORDY         | 0   | R      | <b>LFXO Ready</b><br>LFXO is enabled and start-up time has exceeded.                                 |
| 8     | LFXOENS         | 0   | R      | <b>LFXO Enable Status</b><br>LFXO is enabled (shows disabled status if EM4 repaint is required).     |
| 7     | LFRCORDY        | 0   | R      | <b>LFRCO Ready</b><br>LFRCO is enabled and start-up time has exceeded.                               |
| 6     | LFRCOENS        | 0   | R      | <b>LFRCO Enable Status</b><br>LFRCO is enabled (shows disabled status if EM4 repaint is required).   |
| 5     | AUXHFRCORDY     | 0   | R      | <b>AUXHFRCO Ready</b><br>AUXHFRCO is enabled and start-up time has exceeded.                         |
| 4     | AUXHFRCOENS     | 0   | R      | <b>AUXHFRCO Enable Status</b><br>AUXHFRCO is enabled.  |
| 3     | HFXORDY         | 0   | R      | <b>HFXO Ready</b><br>HFXO is enabled and start-up time has exceeded.                                 |
| 2     | HFXOENS         | 0   | R      | <b>HFXO Enable Status</b><br>HFXO is enabled.  |
| 1     | HFRCORDY        | 1   | R      | <b>HFRCO Ready</b><br>HFRCO is enabled and start-up time has exceeded.                               |
| 0     | HFRCOENS        | 1   | R      | <b>HFRCO Enable Status</b><br>HFRCO is enabled.  |

## 12.5.20 CMU\_HFCLKSTATUS - HFCLK Status Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |          |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|----------|---|---|---|---|---|
| 0x094         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5        | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | 0x1      |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | R        |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | SELECTED |   |   |   |   |   |

| Bit  | Name            | Reset   | Access | Description  |
|------|-----------------|---|--------|--|
| 31:3 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 2:0  | SELECTED        | 0x1   | R      | <b>HFCLK Selected</b><br>Clock selected as HFCLK clock source. |
|      | Value           | Mode  |        | Description  |
|      | 1               | HFRCO   |        | HFRCO is selected as HFCLK clock source                        |
|      | 2               | HFXO  |        | HFXO is selected as HFCLK clock source                         |
|      | 3               | LFRCO   |        | LFRCO is selected as HFCLK clock source                        |
|      | 4               | LFXO  |        | LFXO is selected as HFCLK clock source                         |
|      | 5               | HFRCODIV2   |        | HFRCO divided by 2 is selected as HFCLK clock source           |
|      | 7               | CLKIN0  |        | CLKIN0 is selected as HFCLK clock source                       |

12.5.21 CMU\_HFXOTRIMSTATUS - HFXO Trim Status

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |   |   |   |   |              |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|---|---|---|---|--------------|---|---|---|---|---|
| 0x09C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11     | 10 | 9 | 8 | 7 | 6 | 5            | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0xA    |    |   |   |   |   | 0x00         |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R      |    |   |   |   |   | R            |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | REGISH |    |   |   |   |   | IBTRIMXOCORE |   |   |   |   |   |

| Bit   | Name         | Reset   | Access | Description   |
|-------|--------------|---|--------|---|
| 31:11 | Reserved     | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 10:7  | REGISH       | 0xA   | R      | <p><b>Value of REGISH Found By Automatic HFXO Shunt Current Optimization Algorithm</b></p> <p>Can be used as initial value for REGISH value in the CMU_HFXOSTEADYSTATECTRL register if HFXO is to be started again.</p> |
| 6:0   | IBTRIMXOCORE | 0x00  | R      | <p><b>Value of IBTRIMXOCORE Found By Automatic HFXO Peak Detection Algorithm</b></p> <p>Can be used as initial value for IBTRIMXOCORE in the CMU_HFXOSTEADYSTATECTRL register if HFXO is to be started again.</p>       |

## 12.5.22 CMU\_IF - Interrupt Flag Register

| Offset        | Bit Position |            |            |           |          |    |    |    |    |                 |                   |                  |           |               |    |    |    |              |         |                 |                |                |            |            |   |       |        |            |         |          |         |         |   |
|---------------|--------------|------------|------------|-----------|----------|----|----|----|----|-----------------|-------------------|------------------|-----------|---------------|----|----|----|--------------|---------|-----------------|----------------|----------------|------------|------------|---|-------|--------|------------|---------|----------|---------|---------|---|
| 0x0A0         | 31           | 30         | 29         | 28        | 27       | 26 | 25 | 24 | 23 | 22              | 21                | 20               | 19        | 18            | 17 | 16 | 15 | 14           | 13      | 12              | 11             | 10             | 9          | 8          | 7 | 6     | 5      | 4          | 3       | 2        | 1       | 0       |   |
| <b>Reset</b>  | 0            | 0          | 0          | 0         | 0        |    |    |    |    | 0               | 0                 | 0                | 0         | 0             |    |    |    | 0            | 0       | 0               | 0              | 0              | 0          | 0          |   |       | 0      | 0          | 0       | 0        | 1       |         |   |
| <b>Access</b> | R            | R          | R          | R         | R        |    |    |    |    | R               | R                 | R                | R         | R             |    |    |    | R            | R       | R               | R              | R              | R          | R          |   |       | R      | R          | R       | R        | R       | R       | R |
| <b>Name</b>   | CMUERR       | PLFRCOEDGE | ULFRCOEDGE | LFRCOEDGE | LFXOEDGE |    |    |    |    | PLFRCOTIMERDONE | PLFRCOTEMPCHKDONE | PLFRCOHFXODNSERR | PLFRCORDY | PLFRCOCALDONE |    |    |    | LFTIMEOUTERR | HFCODIS | HFXOSHUNTOPTRDY | HFXOPEAKDETRDY | HFXOPEAKDETERR | HFXOAUTOSW | HFXODISERR |   | CALOF | CALRDY | AUXHFCORDY | LFXORDY | LFRCORDY | HFXORDY | HFXORDY |   |

| Bit   | Name               | Reset   | Access | Description   |
|-------|--------------------|---|--------|---|
| 31    | CMUERR             | 0   | R      | <b>CMU Error Interrupt Flag</b><br>Set upon illegal CMU write attempt (e.g. writing CMU_LFRCOCTRL while LFRCOBSY is set).   |
| 30    | PLFRCOEDGE         | 0   | R      | <b>PLFRCO Clock Edge Detected Interrupt Flag</b><br>Sets when PLFRCO clock switches phases.   |
| 29    | ULFRCOEDGE         | 0   | R      | <b>ULFRCO Clock Edge Detected Interrupt Flag</b><br>Sets when ULFRCO clock switches phases.   |
| 28    | LFRCOEDGE          | 0   | R      | <b>LFRCO Clock Edge Detected Interrupt Flag</b><br>Sets when LFRCO clock switches phases.   |
| 27    | LFXOEDGE           | 0   | R      | <b>LFXO Clock Edge Detected Interrupt Flag</b><br>Sets when LFXO clock switches phases.   |
| 26:23 | <i>Reserved</i>    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 22    | PLFRCOTIMER-DONE   | 0   | R      | <b>Timer Done Interrupt Flag</b><br>Sets when the recalibration timer has expired.  |
| 21    | PLFRCOTEMPCHK-DONE | 0   | R      | <b>Temperature Check Done Interrupt Flag</b><br>Sets when the temperature check is done.  |
| 20    | PLFRCOHFXODN-SERR  | 0   | R      | <b>Error Due to HFXO Not Starting Interrupt Flag</b><br>The HFXO did not start. AUTOCALTEMPCHG, AUTOCALTIMER, and CALSTART will attempt a second recalibration before reporting an error. |
| 19    | PLFRCORDY          | 0   | R      | <b>PLFRCO Ready Interrupt Flag</b><br>The PLFRCO is ready to use.   |
| 18    | PLFRCOCALDONE      | 0   | R      | <b>Calibration Interrupt Flag</b><br>Either the base calibration or the recalibration is done.  |
| 17:15 | <i>Reserved</i>    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |

| Bit | Name             | Reset   | Access | Description  |
|-----|------------------|---|--------|--|
| 14  | LFTIMEOUTERR     | 0   | R      | <b>Low Frequency Timeout Error Interrupt Flag</b><br>Set when LFTIMEOUT of CMU_HFXOCTRL triggers before the combined STARTUPTIMEOUT plus STEADYTIMEOUT of the CMU_HFXOTIMEOUTCTRL register triggers. |
| 13  | HFRCODIS         | 0   | R      | <b>HFRCO Disable Interrupt Flag</b><br>Set when a running HFRCO is disabled because of automatic HFXO start and selection.   |
| 12  | HFXOSHUNTOPTR-DY | 0   | R      | <b>HFXO Automatic Shunt Current Optimization Ready Interrupt Flag</b><br>Set when automatic HFXO shunt current optimization is ready.  |
| 11  | HFXOPEAKDETRDY   | 0   | R      | <b>HFXO Automatic Peak Detection Ready Interrupt Flag</b><br>Set when automatic HFXO peak detection is ready.  |
| 10  | HFXOPEAKDETERR   | 0   | R      | <b>HFXO Automatic Peak Detection Error Interrupt Flag</b><br>Set when automatic HFXO peak detection failed.  |
| 9   | HFXOAUTOSW       | 0   | R      | <b>HFXO Automatic Switch Interrupt Flag</b><br>Set when automatic selection of HFXO causes a switch of the source clock used for HFCLKSRC.   |
| 8   | HFXODISERR       | 0   | R      | <b>HFXO Disable Error Interrupt Flag</b><br>Set when software tries to disable/deselect the HFXO in case the automatic enable/select reason is met. The HFXO was not disabled/deselected.            |
| 7   | <i>Reserved</i>  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 6   | CALOF            | 0   | R      | <b>Calibration Overflow Interrupt Flag</b><br>Set when calibration overflow has occurred (i.e. if a new calibration completes before CMU_CALCNT has been read).                                      |
| 5   | CALRDY           | 0   | R      | <b>Calibration Ready Interrupt Flag</b><br>Set when calibration is completed.  |
| 4   | AUXHFRCORDY      | 0   | R      | <b>AUXHFRCO Ready Interrupt Flag</b><br>Set when AUXHFRCO is ready (start-up time exceeded).   |
| 3   | LFXORDY          | 0   | R      | <b>LFXO Ready Interrupt Flag</b><br>Set when LFXO is ready (start-up time exceeded). LFXORDY can be used as wake-up interrupt.   |
| 2   | LFRCORDY         | 0   | R      | <b>LFRCO Ready Interrupt Flag</b><br>Set when LFRCO is ready (start-up time exceeded). LFRCORDY can be used as wake-up interrupt.  |
| 1   | HFXORDY          | 0   | R      | <b>HFXO Ready Interrupt Flag</b><br>Set when HFXO is ready (start-up time exceeded).   |
| 0   | HFRCORDY         | 1   | R      | <b>HFRCO Ready Interrupt Flag</b><br>Set when HFRCO is ready (start-up time exceeded).   |

## 12.5.23 CMU\_IFS - Interrupt Flag Set Register

| Offset        | Bit Position |            |            |           |          |    |    |    |    |                 |                   |                  |           |               |    |    |    |              |          |                 |                |                 |            |            |   |       |        |            |         |          |         |         |    |
|---------------|--------------|------------|------------|-----------|----------|----|----|----|----|-----------------|-------------------|------------------|-----------|---------------|----|----|----|--------------|----------|-----------------|----------------|-----------------|------------|------------|---|-------|--------|------------|---------|----------|---------|---------|----|
| 0x0A4         | 31           | 30         | 29         | 28        | 27       | 26 | 25 | 24 | 23 | 22              | 21                | 20               | 19        | 18            | 17 | 16 | 15 | 14           | 13       | 12              | 11             | 10              | 9          | 8          | 7 | 6     | 5      | 4          | 3       | 2        | 1       | 0       |    |
| <b>Reset</b>  | 0            | 0          | 0          | 0         | 0        |    |    |    |    | 0               | 0                 | 0                | 0         | 0             |    |    |    | 0            | 0        | 0               | 0              | 0               | 0          | 0          |   |       | 0      | 0          | 0       | 0        | 0       | 0       | 0  |
| <b>Access</b> | W1           | W1         | W1         | W1        | W1       |    |    |    |    | W1              | W1                | W1               | W1        | W1            |    |    |    | W1           | W1       | W1              | W1             | W1              | W1         | W1         |   |       | W1     | W1         | W1      | W1       | W1      | W1      | W1 |
| <b>Name</b>   | CMUERR       | PLFRCOEDGE | ULFRCOEDGE | LFRCOEDGE | LFXOEDGE |    |    |    |    | PLFRCOTIMERDONE | PLFRCOTEMPCHKDONE | PLFRCOHFXODNSERR | PLFRCORDY | PLFRCOCALDONE |    |    |    | LFTIMEOUTERR | HFRCODIS | HFXOSHUNTOPTRDY | HFXOPEAKDETRDY | HFXOPEAKDETEERR | HFXOAUTOSW | HFXODISERR |   | CALOF | CALRDY | AUXHFCORDY | LFXORDY | LFRCORDY | HFXORDY | HFCORDY |    |

| Bit   | Name               | Reset   | Access | Description  |
|-------|--------------------|---|--------|--|
| 31    | CMUERR             | 0   | W1     | <b>Set CMUERR Interrupt Flag</b><br>Write 1 to set the CMUERR interrupt flag                       |
| 30    | PLFRCOEDGE         | 0   | W1     | <b>Set PLFRCOEDGE Interrupt Flag</b><br>Write 1 to set the PLFRCOEDGE interrupt flag               |
| 29    | ULFRCOEDGE         | 0   | W1     | <b>Set ULFRCOEDGE Interrupt Flag</b><br>Write 1 to set the ULFRCOEDGE interrupt flag               |
| 28    | LFRCOEDGE          | 0   | W1     | <b>Set LFRCOEDGE Interrupt Flag</b><br>Write 1 to set the LFRCOEDGE interrupt flag                 |
| 27    | LFXOEDGE           | 0   | W1     | <b>Set LFXOEDGE Interrupt Flag</b><br>Write 1 to set the LFXOEDGE interrupt flag                   |
| 26:23 | <i>Reserved</i>    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 22    | PLFRCOTIMER-DONE   | 0   | W1     | <b>Set PLFRCOTIMERDONE Interrupt Flag</b><br>Write 1 to set the PLFRCOTIMERDONE interrupt flag     |
| 21    | PLFRCOTEMPCHK-DONE | 0   | W1     | <b>Set PLFRCOTEMPCHKDONE Interrupt Flag</b><br>Write 1 to set the PLFRCOTEMPCHKDONE interrupt flag |
| 20    | PLFRCOHFXODN-SERR  | 0   | W1     | <b>Set PLFRCOHFXODNSERR Interrupt Flag</b><br>Write 1 to set the PLFRCOHFXODNSERR interrupt flag   |
| 19    | PLFRCORDY          | 0   | W1     | <b>Set PLFRCORDY Interrupt Flag</b><br>Write 1 to set the PLFRCORDY interrupt flag                 |
| 18    | PLFRCOCALDONE      | 0   | W1     | <b>Set PLFRCOCALDONE Interrupt Flag</b><br>Write 1 to set the PLFRCOCALDONE interrupt flag         |
| 17:15 | <i>Reserved</i>    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |

| Bit | Name            | Reset   | Access | Description  |
|-----|-----------------|---|--------|--|
| 14  | LFTIMEOUTERR    | 0   | W1     | <b>Set LFTIMEOUTERR Interrupt Flag</b><br>Write 1 to set the LFTIMEOUTERR interrupt flag       |
| 13  | HFRCODIS        | 0   | W1     | <b>Set HFRCODIS Interrupt Flag</b><br>Write 1 to set the HFRCODIS interrupt flag               |
| 12  | HFXOSHUNTOPTRDY | 0   | W1     | <b>Set HFXOSHUNTOPTRDY Interrupt Flag</b><br>Write 1 to set the HFXOSHUNTOPTRDY interrupt flag |
| 11  | HFXOPEAKDETRDY  | 0   | W1     | <b>Set HFXOPEAKDETRDY Interrupt Flag</b><br>Write 1 to set the HFXOPEAKDETRDY interrupt flag   |
| 10  | HFXOPEAKDETERR  | 0   | W1     | <b>Set HFXOPEAKDETERR Interrupt Flag</b><br>Write 1 to set the HFXOPEAKDETERR interrupt flag   |
| 9   | HFXOAUTOSW      | 0   | W1     | <b>Set HFXOAUTOSW Interrupt Flag</b><br>Write 1 to set the HFXOAUTOSW interrupt flag           |
| 8   | HFXODISERR      | 0   | W1     | <b>Set HFXODISERR Interrupt Flag</b><br>Write 1 to set the HFXODISERR interrupt flag           |
| 7   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 6   | CALOF           | 0   | W1     | <b>Set CALOF Interrupt Flag</b><br>Write 1 to set the CALOF interrupt flag                     |
| 5   | CALRDY          | 0   | W1     | <b>Set CALRDY Interrupt Flag</b><br>Write 1 to set the CALRDY interrupt flag                   |
| 4   | AUXHFCORDY      | 0   | W1     | <b>Set AUXHFCORDY Interrupt Flag</b><br>Write 1 to set the AUXHFCORDY interrupt flag           |
| 3   | LFXORDY         | 0   | W1     | <b>Set LFXORDY Interrupt Flag</b><br>Write 1 to set the LFXORDY interrupt flag                 |
| 2   | LFCORDY         | 0   | W1     | <b>Set LFCORDY Interrupt Flag</b><br>Write 1 to set the LFCORDY interrupt flag                 |
| 1   | HFXORDY         | 0   | W1     | <b>Set HFXORDY Interrupt Flag</b><br>Write 1 to set the HFXORDY interrupt flag                 |
| 0   | HFCORDY         | 0   | W1     | <b>Set HFCORDY Interrupt Flag</b><br>Write 1 to set the HFCORDY interrupt flag                 |

## 12.5.24 CMU\_IFC - Interrupt Flag Clear Register

| Offset | Bit Position |            |            |           |          |    |    |    |    |                 |                   |                  |           |               |    |    |    |              |          |                 |                |                 |            |            |   |       |        |             |         |          |         |          |   |
|--------|--------------|------------|------------|-----------|----------|----|----|----|----|-----------------|-------------------|------------------|-----------|---------------|----|----|----|--------------|----------|-----------------|----------------|-----------------|------------|------------|---|-------|--------|-------------|---------|----------|---------|----------|---|
| 0x0A8  | 31           | 30         | 29         | 28        | 27       | 26 | 25 | 24 | 23 | 22              | 21                | 20               | 19        | 18            | 17 | 16 | 15 | 14           | 13       | 12              | 11             | 10              | 9          | 8          | 7 | 6     | 5      | 4           | 3       | 2        | 1       | 0        |   |
| Reset  | 0            | 0          | 0          | 0         | 0        |    |    |    |    | 0               | 0                 | 0                | 0         | 0             |    |    |    | 0            | 0        | 0               | 0              | 0               | 0          | 0          |   |       | 0      | 0           | 0       | 0        | 0       | 0        | 0 |
| Access | (R)W1        | (R)W1      | (R)W1      | (R)W1     | (R)W1    |    |    |    |    | (R)W1           | (R)W1             | (R)W1            | (R)W1     | (R)W1         |    |    |    | (R)W1        | (R)W1    | (R)W1           | (R)W1          | (R)W1           | (R)W1      | (R)W1      |   |       | (R)W1  | (R)W1       | (R)W1   | (R)W1    | (R)W1   | (R)W1    |   |
| Name   | CMUERR       | PLFRCOEDGE | ULFRCOEDGE | LFRCOEDGE | LFXOEDGE |    |    |    |    | PLFRCOTIMERDONE | PLFRCOTEMPCHKDONE | PLFRCOHFXODNSERR | PLFRCORDY | PLFRCOCALDONE |    |    |    | LFTIMEOUTERR | HFRCODIS | HFXOSHUNTOPTRDY | HFXOPEAKDETRDY | HFXOPEAKDETRERR | HFXOAUTOSW | HFXODISERR |   | CALOF | CALRDY | AUXHFRCORDY | LFXORDY | LFRCORDY | HFXORDY | HFRCORDY |   |

| Bit   | Name               | Reset   | Access | Description   |
|-------|--------------------|---|--------|---|
| 31    | CMUERR             | 0   | (R)W1  | <b>Clear CMUERR Interrupt Flag</b><br><br>Write 1 to clear the CMUERR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                       |
| 30    | PLFRCOEDGE         | 0   | (R)W1  | <b>Clear PLFRCOEDGE Interrupt Flag</b><br><br>Write 1 to clear the PLFRCOEDGE interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).               |
| 29    | ULFRCOEDGE         | 0   | (R)W1  | <b>Clear ULFRCOEDGE Interrupt Flag</b><br><br>Write 1 to clear the ULFRCOEDGE interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).               |
| 28    | LFRCOEDGE          | 0   | (R)W1  | <b>Clear LFRCOEDGE Interrupt Flag</b><br><br>Write 1 to clear the LFRCOEDGE interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                 |
| 27    | LFXOEDGE           | 0   | (R)W1  | <b>Clear LFXOEDGE Interrupt Flag</b><br><br>Write 1 to clear the LFXOEDGE interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                   |
| 26:23 | <i>Reserved</i>    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 22    | PLFRCOTIMER-DONE   | 0   | (R)W1  | <b>Clear PLFRCOTIMERDONE Interrupt Flag</b><br><br>Write 1 to clear the PLFRCOTIMERDONE interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 21    | PLFRCOTEMPCHK-DONE | 0   | (R)W1  | <b>Clear PLFRCOTEMPCHKDONE Interrupt Flag</b><br><br>Write 1 to clear the PLFRCOTEMPCHKDONE interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 20    | PLFRCOHFXODN-SERR  | 0   | (R)W1  | <b>Clear PLFRCOHFXODNSERR Interrupt Flag</b><br><br>Write 1 to clear the PLFRCOHFXODNSERR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 19    | PLFRCORDY       | 0   | (R)W1  | <b>Clear PLFRCORDY Interrupt Flag</b><br><br>Write 1 to clear the PLFRCORDY interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).             |
| 18    | PLFRCOCALDONE   | 0   | (R)W1  | <b>Clear PLFRCOCALDONE Interrupt Flag</b><br><br>Write 1 to clear the PLFRCOCALDONE interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 17:15 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 14    | LFTIMEOUTERR    | 0   | (R)W1  | <b>Clear LFTIMEOUTERR Interrupt Flag</b><br><br>Write 1 to clear the LFTIMEOUTERR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).       |
| 13    | HFRCODIS        | 0   | (R)W1  | <b>Clear HFRCODIS Interrupt Flag</b><br><br>Write 1 to clear the HFRCODIS interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).               |
| 12    | HFXOSHUNTOPTRDY | 0   | (R)W1  | <b>Clear HFXOSHUNTOPTRDY Interrupt Flag</b><br><br>Write 1 to clear the HFXOSHUNTOPTRDY interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 11    | HFXOPEAKDETRDY  | 0   | (R)W1  | <b>Clear HFXOPEAKDETRDY Interrupt Flag</b><br><br>Write 1 to clear the HFXOPEAKDETRDY interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |
| 10    | HFXOPEAKDETERR  | 0   | (R)W1  | <b>Clear HFXOPEAKDETERR Interrupt Flag</b><br><br>Write 1 to clear the HFXOPEAKDETERR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |
| 9     | HFXOAUTOSW      | 0   | (R)W1  | <b>Clear HFXOAUTOSW Interrupt Flag</b><br><br>Write 1 to clear the HFXOAUTOSW interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).           |
| 8     | HFXODISERR      | 0   | (R)W1  | <b>Clear HFXODISERR Interrupt Flag</b><br><br>Write 1 to clear the HFXODISERR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).           |
| 7     | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 6     | CALOF           | 0   | (R)W1  | <b>Clear CALOF Interrupt Flag</b><br><br>Write 1 to clear the CALOF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                     |
| 5     | CALRDY          | 0   | (R)W1  | <b>Clear CALRDY Interrupt Flag</b><br><br>Write 1 to clear the CALRDY interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                   |
| 4     | AUXHFRCORDY     | 0   | (R)W1  | <b>Clear AUXHFRCORDY Interrupt Flag</b><br><br>Write 1 to clear the AUXHFRCORDY interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).         |
| 3     | LFXORDY         | 0   | (R)W1  | <b>Clear LFXORDY Interrupt Flag</b><br><br>Write 1 to clear the LFXORDY interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                 |

| Bit | Name    | Reset | Access | Description   |
|-----|---------|-------|--------|---|
| 2   | LFCORDY | 0     | (R)W1  | <b>Clear LFCORDY Interrupt Flag</b><br><br>Write 1 to clear the LFCORDY interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 1   | HFXORDY | 0     | (R)W1  | <b>Clear HFXORDY Interrupt Flag</b><br><br>Write 1 to clear the HFXORDY interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 0   | HFCORDY | 0     | (R)W1  | <b>Clear HFCORDY Interrupt Flag</b><br><br>Write 1 to clear the HFCORDY interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |

## 12.5.25 CMU\_IEN - Interrupt Enable Register

| Offset        | Bit Position |            |            |           |          |    |    |    |    |                 |                   |                  |           |               |    |    |    |              |          |                 |                |                 |            |            |   |       |        |             |         |          |         |          |    |
|---------------|--------------|------------|------------|-----------|----------|----|----|----|----|-----------------|-------------------|------------------|-----------|---------------|----|----|----|--------------|----------|-----------------|----------------|-----------------|------------|------------|---|-------|--------|-------------|---------|----------|---------|----------|----|
| 0x0AC         | 31           | 30         | 29         | 28        | 27       | 26 | 25 | 24 | 23 | 22              | 21                | 20               | 19        | 18            | 17 | 16 | 15 | 14           | 13       | 12              | 11             | 10              | 9          | 8          | 7 | 6     | 5      | 4           | 3       | 2        | 1       | 0        |    |
| <b>Reset</b>  | 0            | 0          | 0          | 0         | 0        |    |    |    |    | 0               | 0                 | 0                | 0         | 0             |    |    |    | 0            | 0        | 0               | 0              | 0               | 0          | 0          |   |       | 0      | 0           | 0       | 0        | 0       | 0        | 0  |
| <b>Access</b> | RW           | RW         | RW         | RW        | RW       |    |    |    |    | RW              | RW                | RW               | RW        | RW            |    |    |    | RW           | RW       | RW              | RW             | RW              | RW         | RW         |   |       | RW     | RW          | RW      | RW       | RW      | RW       | RW |
| <b>Name</b>   | CMUERR       | PLFRCOEDGE | ULFRCOEDGE | LFRCOEDGE | LFXOEDGE |    |    |    |    | PLFRCOTIMERDONE | PLFRCOTEMPCHKDONE | PLFRCOHFXODNSERR | PLFRCORDY | PLFRCOCALDONE |    |    |    | LFTIMEOUTERR | HFRCODIS | HFXOSHUNTOPTRDY | HFXOPEAKDETRDY | HFXOPEAKDETEERR | HFXOAUTOSW | HFXODISERR |   | CALOF | CALRDY | AUXHFRCORDY | LFXORDY | LFRCORDY | HFXORDY | HFRCORDY |    |

| Bit   | Name               | Reset   | Access | Description   |
|-------|--------------------|---|--------|---|
| 31    | CMUERR             | 0   | RW     | <b>CMUERR Interrupt Enable</b><br>Enable/disable the CMUERR interrupt                       |
| 30    | PLFRCOEDGE         | 0   | RW     | <b>PLFRCOEDGE Interrupt Enable</b><br>Enable/disable the PLFRCOEDGE interrupt               |
| 29    | ULFRCOEDGE         | 0   | RW     | <b>ULFRCOEDGE Interrupt Enable</b><br>Enable/disable the ULFRCOEDGE interrupt               |
| 28    | LFRCOEDGE          | 0   | RW     | <b>LFRCOEDGE Interrupt Enable</b><br>Enable/disable the LFRCOEDGE interrupt                 |
| 27    | LFXOEDGE           | 0   | RW     | <b>LFXOEDGE Interrupt Enable</b><br>Enable/disable the LFXOEDGE interrupt                   |
| 26:23 | <i>Reserved</i>    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 22    | PLFRCOTIMER-DONE   | 0   | RW     | <b>PLFRCOTIMERDONE Interrupt Enable</b><br>Enable/disable the PLFRCOTIMERDONE interrupt     |
| 21    | PLFRCOTEMPCHK-DONE | 0   | RW     | <b>PLFRCOTEMPCHKDONE Interrupt Enable</b><br>Enable/disable the PLFRCOTEMPCHKDONE interrupt |
| 20    | PLFRCOHFXODN-SERR  | 0   | RW     | <b>PLFRCOHFXODNSERR Interrupt Enable</b><br>Enable/disable the PLFRCOHFXODNSERR interrupt   |
| 19    | PLFRCORDY          | 0   | RW     | <b>PLFRCORDY Interrupt Enable</b><br>Enable/disable the PLFRCORDY interrupt                 |
| 18    | PLFRCOCALDONE      | 0   | RW     | <b>PLFRCOCALDONE Interrupt Enable</b><br>Enable/disable the PLFRCOCALDONE interrupt         |
| 17:15 | <i>Reserved</i>    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |

| Bit | Name            | Reset   | Access | Description   |
|-----|-----------------|---|--------|---|
| 14  | LFTIMEOUTERR    | 0   | RW     | <b>LFTIMEOUTERR Interrupt Enable</b><br>Enable/disable the LFTIMEOUTERR interrupt       |
| 13  | HFRCODIS        | 0   | RW     | <b>HFRCODIS Interrupt Enable</b><br>Enable/disable the HFRCODIS interrupt               |
| 12  | HFXOSHUNTOPTRDY | 0   | RW     | <b>HFXOSHUNTOPTRDY Interrupt Enable</b><br>Enable/disable the HFXOSHUNTOPTRDY interrupt |
| 11  | HFXOPEAKDETRDY  | 0   | RW     | <b>HFXOPEAKDETRDY Interrupt Enable</b><br>Enable/disable the HFXOPEAKDETRDY interrupt   |
| 10  | HFXOPEAKDETERR  | 0   | RW     | <b>HFXOPEAKDETERR Interrupt Enable</b><br>Enable/disable the HFXOPEAKDETERR interrupt   |
| 9   | HFXOAUTOSW      | 0   | RW     | <b>HFXOAUTOSW Interrupt Enable</b><br>Enable/disable the HFXOAUTOSW interrupt           |
| 8   | HFXODISERR      | 0   | RW     | <b>HFXODISERR Interrupt Enable</b><br>Enable/disable the HFXODISERR interrupt           |
| 7   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 6   | CALOF           | 0   | RW     | <b>CALOF Interrupt Enable</b><br>Enable/disable the CALOF interrupt                     |
| 5   | CALRDY          | 0   | RW     | <b>CALRDY Interrupt Enable</b><br>Enable/disable the CALRDY interrupt                   |
| 4   | AUXHFCORDY      | 0   | RW     | <b>AUXHFCORDY Interrupt Enable</b><br>Enable/disable the AUXHFCORDY interrupt           |
| 3   | LFXORDY         | 0   | RW     | <b>LFXORDY Interrupt Enable</b><br>Enable/disable the LFXORDY interrupt                 |
| 2   | LFCORDY         | 0   | RW     | <b>LFCORDY Interrupt Enable</b><br>Enable/disable the LFCORDY interrupt                 |
| 1   | HFXORDY         | 0   | RW     | <b>HFXORDY Interrupt Enable</b><br>Enable/disable the HFXORDY interrupt                 |
| 0   | HFCORDY         | 0   | RW     | <b>HFCORDY Interrupt Enable</b><br>Enable/disable the HFCORDY interrupt                 |

## 12.5.26 CMU\_HFBUSCLKEN0 - High Frequency Bus Clock Enable Register 0

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |       |      |     |      |    |         |         |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|-------|------|-----|------|----|---------|---------|
| 0x0B0         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5     | 4    | 3   | 2    | 1  | 0       |         |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | 0     | 0    | 0   | 0    | 0  | 0       |         |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | RW    | RW   | RW  | RW   | RW | RW      |         |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | GPCRC | LDMA | PRS | GPIO | LE | CRYPTO1 | CRYPTO0 |

| Bit  | Name     | Reset  | Access | Description   |
|------|----------|--|--------|---|
| 31:7 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 6    | GPCRC    | 0  | RW     | <b>General Purpose CRC Clock Enable</b><br>Set to enable the clock for GPCRC.   |
| 5    | LDMA     | 0  | RW     | <b>Linked Direct Memory Access Controller Clock Enable</b><br>Set to enable the clock for LDMA.   |
| 4    | PRS      | 0  | RW     | <b>Peripheral Reflex System Clock Enable</b><br>Set to enable the clock for PRS.  |
| 3    | GPIO     | 0  | RW     | <b>General purpose Input/Output Clock Enable</b><br>Set to enable the clock for GPIO.   |
| 2    | LE       | 0  | RW     | <b>Low Energy Peripheral Interface Clock Enable</b><br>Set to enable the clock for LE. Interface used for bus access to Low Energy peripherals. |
| 1    | CRYPTO1  | 0  | RW     | <b>Advanced Encryption Standard Accelerator 1 Clock Enable</b><br>Set to enable the clock for CRYPTO1.  |
| 0    | CRYPTO0  | 0  | RW     | <b>Advanced Encryption Standard Accelerator 0 Clock Enable</b><br>Set to enable the clock for CRYPTO0.  |

## 12.5.27 CMU\_HFPERCLKEN0 - High Frequency Peripheral Clock Enable Register 0

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |       |       |      |       |      |           |       |       |      |      |        |        |        |         |        |        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|-------|------|-------|------|-----------|-------|-------|------|------|--------|--------|--------|---------|--------|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--|
| 0x0C0         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15    | 14    | 13   | 12    | 11   | 10        | 9     | 8     | 7    | 6    | 5      | 4      | 3      | 2       | 1      | 0      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0     | 0     | 0    | 0     | 0    | 0         | 0     | 0     | 0    | 0    | 0      | 0      | 0      | 0       | 0      | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |    |    |    |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW    | RW    | RW   | RW    | RW   | RW        | RW    | RW    | RW   | RW   | RW     | RW     | RW     | RW      | RW     | RW     | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | TRNG0 | IDAC0 | CSEN | VDAC0 | ADC0 | CRYOTIMER | ACMP1 | ACMP0 | I2C1 | I2C0 | USART2 | USART1 | USART0 | WTIMER0 | TIMER1 | TIMER0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |  |

| Bit   | Name      | Reset  | Access | Description  |
|-------|-----------|--|--------|--|
| 31:16 | Reserved  | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 15    | TRNG0     | 0  | RW     | <b>True Random Number Generator 0 Clock Enable</b><br>Set to enable the clock for TRNG0.                             |
| 14    | IDAC0     | 0  | RW     | <b>Current Digital to Analog Converter 0 Clock Enable</b><br>Set to enable the clock for IDAC0.                      |
| 13    | CSEN      | 0  | RW     | <b>Capacitive touch sense module Clock Enable</b><br>Set to enable the clock for CSEN.                               |
| 12    | VDAC0     | 0  | RW     | <b>Digital to Analog Converter 0 Clock Enable</b><br>Set to enable the clock for VDAC0.                              |
| 11    | ADC0      | 0  | RW     | <b>Analog to Digital Converter 0 Clock Enable</b><br>Set to enable the clock for ADC0.                               |
| 10    | CRYOTIMER | 0  | RW     | <b>CRYOTIMER Clock Enable</b><br>Set to enable the clock for CRYOTIMER.  |
| 9     | ACMP1     | 0  | RW     | <b>Analog Comparator 1 Clock Enable</b><br>Set to enable the clock for ACMP1.  |
| 8     | ACMP0     | 0  | RW     | <b>Analog Comparator 0 Clock Enable</b><br>Set to enable the clock for ACMP0.  |
| 7     | I2C1      | 0  | RW     | <b>I2C 1 Clock Enable</b><br>Set to enable the clock for I2C1.   |
| 6     | I2C0      | 0  | RW     | <b>I2C 0 Clock Enable</b><br>Set to enable the clock for I2C0.   |
| 5     | USART2    | 0  | RW     | <b>Universal Synchronous/Asynchronous Receiver/Transmitter 2 Clock Enable</b><br>Set to enable the clock for USART2. |
| 4     | USART1    | 0  | RW     | <b>Universal Synchronous/Asynchronous Receiver/Transmitter 1 Clock Enable</b><br>Set to enable the clock for USART1. |

| Bit | Name    | Reset | Access | Description  |
|-----|---------|-------|--------|--|
| 3   | USART0  | 0     | RW     | <b>Universal Synchronous/Asynchronous Receiver/Transmitter 0 Clock Enable</b><br><br>Set to enable the clock for USART0. |
| 2   | WTIMER0 | 0     | RW     | <b>Wide Timer 0 Clock Enable</b><br><br>Set to enable the clock for WTIMER0.   |
| 1   | TIMER1  | 0     | RW     | <b>Timer 1 Clock Enable</b><br><br>Set to enable the clock for TIMER1.   |
| 0   | TIMER0  | 0     | RW     | <b>Timer 0 Clock Enable</b><br><br>Set to enable the clock for TIMER0.   |

**12.5.28 CMU\_HFRADIOALTCLKEN0 - High Frequency Alternate Radio Peripheral Clock Enable Register 0**

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x0CC         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name            | Reset | Access | Description   |
|------|-----------------|-------|--------|---|
| 31:0 | <i>Reserved</i> |       |        | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |

**12.5.29 CMU\_LFACLKEN0 - Low Frequency a Clock Enable Register 0 (Async Reg)**

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |         |          |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---------|----------|
| 0x0E0         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1       | 0        |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | 0       | 0        |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | RW      | RW       |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | LESENSE | LETIMER0 |

| Bit  | Name            | Reset | Access | Description   |
|------|-----------------|-------|--------|---|
| 31:2 | <i>Reserved</i> |       |        | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |
| 1    | LESENSE         | 0     | RW     | <b>Low Energy Sensor Interface Clock Enable</b><br><br>Set to enable the clock for LESENSE.                                     |
| 0    | LETIMER0        | 0     | RW     | <b>Low Energy Timer 0 Clock Enable</b><br><br>Set to enable the clock for LETIMER0.   |

## 12.5.30 CMU\_LFBCLKEN0 - Low Frequency B Clock Enable Register 0 (Async Reg)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |      |   |   |         |   |   |         |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|------|---|---|---------|---|---|---------|---|---|
| 0x0E8         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3    | 2 | 1 | 0       |   |   |         |   |   |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | CSEN | 0 | 2 | LEUART0 | 0 | 1 | SYSTICK | 0 | 0 |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | RW   |   |   | RW      |   |   | RW      |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | CSEN |   |   | LEUART0 |   |   | SYSTICK |   |   |

| Bit  | Name     | Reset   | Access | Description  |
|------|----------|---|--------|--|
| 31:3 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 2    | CSEN     | 0   | RW     | <b>Capacitive touch sense module Clock Enable</b><br>Set to enable the clock for CSEN. |
| 1    | LEUART0  | 0   | RW     | <b>Low Energy UART 0 Clock Enable</b><br>Set to enable the clock for LEUART0.          |
| 0    | SYSTICK  | 0   | RW     | <b>Clock Enable</b><br>Set to enable the clock for SYSTICK.                            |

## 12.5.31 CMU\_LFECLKEN0 - Low Frequency E Clock Enable Register 0 (Async Reg)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |      |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|------|---|---|---|
| 0x0F0         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3    | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | RTCC | 0 |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | RW   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | RTCC |   |   |   |

| Bit  | Name     | Reset   | Access | Description   |
|------|----------|---|--------|---|
| 31:1 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 0    | RTCC     | 0   | RW     | <b>Real-Time Counter and Calendar Clock Enable</b><br>Set to enable the clock for RTCC. |

12.5.32 CMU\_HFPRESC - High Frequency Clock Prescaler Register

| Offset | Bit Position |    |    |    |    |    |    |    |              |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |       |   |   |   |   |   |   |  |
|--------|--------------|----|----|----|----|----|----|----|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|-------|---|---|---|---|---|---|--|
| 0x100  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6     | 5 | 4 | 3 | 2 | 1 | 0 |  |
| Reset  |              |    |    |    |    |    |    |    | 0x0          |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   | 0x00  |   |   |   |   |   |   |  |
| Access |              |    |    |    |    |    |    |    | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   | RW    |   |   |   |   |   |   |  |
| Name   |              |    |    |    |    |    |    |    | HFCLKLEPRESC |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   | PRESC |   |   |   |   |   |   |  |

| Bit   | Name         | Reset   | Access  | Description   |
|-------|--------------|---|---|---|
| 31:25 | Reserved     | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |
| 24:24 | HFCLKLEPRESC | 0x0   | RW  | <b>HFCLKLE Prescaler</b><br>Specifies the clock divider for HFCLKLE.                    |
|       | Value        | Mode  | Description                                     |   |
|       | 0            | DIV2  | HFCLKLE is HFBUSCLK <sub>LE</sub> divided by 2. |   |
|       | 1            | DIV4  | HFCLKLE is HFBUSCLK <sub>LE</sub> divided by 4. |   |
| 23:13 | Reserved     | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |
| 12:8  | PRESC        | 0x00  | RW  | <b>HFCLK Prescaler</b><br>Specifies the clock divider for HFCLK (relative to HFSRCCLK). |
|       | Value        | Description   |   |   |
|       | PRESC        | Clock division factor of PRESC+1.   |   |   |
| 7:0   | Reserved     | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |

## 12.5.33 CMU\_HFCOREPRESC - High Frequency Core Clock Prescaler Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x108         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15    | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PRESC |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description  |
|-------|----------|--|--------|--|
| 31:17 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 16:8  | PRESC    | 0x000  | RW     | <b>HFCORECLK Prescaler</b><br>Specifies the clock divider for HFCORECLK (relative to HFCLK). |
|       | Value    | Description  |        |  |
|       | PRESC    | Clock division factor of PRESC+1.  |        |  |
| 7:0   | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |

## 12.5.34 CMU\_HFPERPRESC - High Frequency Peripheral Clock Prescaler Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x10C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15    | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PRESC |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description  |
|-------|----------|--|--------|--|
| 31:17 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 16:8  | PRESC    | 0x000  | RW     | <b>HFPERCLK Prescaler</b><br>Specifies the clock divider for the HFPERCLK (relative to HFCLK). |
|       | Value    | Description  |        |  |
|       | PRESC    | Clock division factor of PRESC+1.  |        |  |
| 7:0   | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |

### 12.5.35 CMU\_HFRADIOPRESC - High Frequency Radio Peripheral Clock Prescaler Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x110         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15    | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PRESC |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset   | Access | Description  |
|-------|----------|---|--------|--|
| 31:17 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 16:8  | PRESC    | 0x000   | RW     | <b>HFRADIOCLK Prescaler</b><br>Specifies the clock divider for the HFRADIOCLK (relative to HFCLK).<br><hr/> Value: PRESC<br>Description: Clock division factor of PRESC+1. |
| 7:0   | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |

### 12.5.36 CMU\_HFEXPPRESC - High Frequency Export Clock Prescaler Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x114         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15    | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PRESC |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset   | Access | Description  |
|-------|----------|---|--------|--|
| 31:13 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 12:8  | PRESC    | 0x00  | RW     | <b>HFEXPCLK Prescaler</b><br>Specifies the clock divider for HFEXPCLK (relative to HFCLK).<br><hr/> Value: PRESC<br>Description: Clock division factor of PRESC+1. |
| 7:0   | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |

## 12.5.37 CMU\_LFAPRESC0 - Low Frequency a Prescaler Register 0 (Async Reg)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |         |          |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---------|----------|---|---|---|---|---|---|
| 0x120         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7       | 6        | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x0     | 0x0      |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RW      | RW       |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | LESENSE | LETIMER0 |   |   |   |   |   |   |

| Bit  | Name            | Reset   | Access                                   | Description   |
|------|-----------------|---|--|---|
| 31:6 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |   |
| 5:4  | LESENSE         | 0x0   | RW                                       | <b>Low Energy Sensor Interface Prescaler</b><br>Configure Low Energy Sensor Interface prescaler |
|      | Value           | Mode  | Description                              |   |
|      | 0               | DIV1  | LFACLK <sub>LESENSE</sub> = LFACLK       |   |
|      | 1               | DIV2  | LFACLK <sub>LESENSE</sub> = LFACLK/2     |   |
|      | 2               | DIV4  | LFACLK <sub>LESENSE</sub> = LFACLK/4     |   |
|      | 3               | DIV8  | LFACLK <sub>LESENSE</sub> = LFACLK/8     |   |
| 3:0  | LETIMER0        | 0x0   | RW                                       | <b>Low Energy Timer 0 Prescaler</b><br>Configure Low Energy Timer 0 prescaler                   |
|      | Value           | Mode  | Description                              |   |
|      | 0               | DIV1  | LFACLK <sub>LETIMER0</sub> = LFACLK      |   |
|      | 1               | DIV2  | LFACLK <sub>LETIMER0</sub> = LFACLK/2    |   |
|      | 2               | DIV4  | LFACLK <sub>LETIMER0</sub> = LFACLK/4    |   |
|      | 3               | DIV8  | LFACLK <sub>LETIMER0</sub> = LFACLK/8    |   |
|      | 4               | DIV16   | LFACLK <sub>LETIMER0</sub> = LFACLK/16   |   |
|      | 5               | DIV32   | LFACLK <sub>LETIMER0</sub> = LFACLK/32   |   |
|      | 6               | DIV64   | LFACLK <sub>LETIMER0</sub> = LFACLK/64   |   |
|      | 7               | DIV128  | LFACLK <sub>LETIMER0</sub> = LFACLK/128  |   |
|      | 8               | DIV256  | LFACLK <sub>LETIMER0</sub> = LFACLK/256  |   |
|      | 9               | DIV512  | LFACLK <sub>LETIMER0</sub> = LFACLK/512  |   |
|      | 10              | DIV1024   | LFACLK <sub>LETIMER0</sub> = LFACLK/1024 |   |
|      | 11              | DIV2048   | LFACLK <sub>LETIMER0</sub> = LFACLK/2048 |   |
|      | 12              | DIV4096   | LFACLK <sub>LETIMER0</sub> = LFACLK/4096 |   |
|      | 13              | DIV8192   | LFACLK <sub>LETIMER0</sub> = LFACLK/8192 |   |

| Bit | Name | Reset    | Access | Description                        |
|-----|------|----------|--------|------------------------------------|
| 14  |      | DIV16384 |        | $LFACLK_{LETIMER0} = LFACLK/16384$ |
| 15  |      | DIV32768 |        | $LFACLK_{LETIMER0} = LFACLK/32768$ |

### 12.5.38 CMU\_LFBPRESC0 - Low Frequency B Prescaler Register 0 (Async Reg)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |     |      |   |   |     |         |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|-----|------|---|---|-----|---------|---|---|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7   | 6    | 5 | 4 | 3   | 2       | 1 | 0 |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |
| 0x128         |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 9   | 8    | 7 | 6 | 5   | 4       | 3 | 2 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x0 |      |   |   | 0x0 |         |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0     |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |     | RW   |   |   |     | RW      |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |     | CSEN |   |   |     | LEUART0 |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SYSTICK |

| Bit   | Name            | Reset   | Access                        | Description   |
|-------|-----------------|---|-------------------------------|---|
| 31:10 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                               |   |
| 9:8   | CSEN            | 0x0   | RW                            | <b>Capacitive touch sense module Prescaler</b><br>Configure Capacitive touch sense module prescaler |
|       | Value           | Mode  | Description                   |   |
|       | 0               | DIV16   | $LFBCLK_{CSEN} = LFBCLK/16$   |   |
|       | 1               | DIV32   | $LFBCLK_{CSEN} = LFBCLK/32$   |   |
|       | 2               | DIV64   | $LFBCLK_{CSEN} = LFBCLK/64$   |   |
|       | 3               | DIV128  | $LFBCLK_{CSEN} = LFBCLK/128$  |   |
| 7:6   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                               |   |
| 5:4   | LEUART0         | 0x0   | RW                            | <b>Low Energy UART 0 Prescaler</b><br>Configure Low Energy UART 0 prescaler                         |
|       | Value           | Mode  | Description                   |   |
|       | 0               | DIV1  | $LFBCLK_{LEUART0} = LFBCLK$   |   |
|       | 1               | DIV2  | $LFBCLK_{LEUART0} = LFBCLK/2$ |   |
|       | 2               | DIV4  | $LFBCLK_{LEUART0} = LFBCLK/4$ |   |
|       | 3               | DIV8  | $LFBCLK_{LEUART0} = LFBCLK/8$ |   |
| 3:0   | SYSTICK         | 0x0   |                               | <b>Prescaler</b><br>Configure prescaler   |
|       | Value           | Mode  | Description                   |   |
|       | 0               | DIV1  | $LFBCLK_{SYSTICK} = LFBCLK$   |   |

**12.5.39 CMU\_LFEPRESC0 - Low Frequency E Prescaler Register 0 (Async Reg)**

When waking up from EM4 make sure EM4UNLATCH in EMU\_CMD is set for this to take effect

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |      |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|------|---|
| 0x130         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1    | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | 0x0  |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | RW   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | RTCC |   |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 31:2 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 1:0  | RTCC            | 0x0   | RW     | <b>Real-Time Counter and Calendar Prescaler</b><br>Configure Real-Time Counter and Calendar prescaler |
|      | Value           | Mode  |        | Description   |
|      | 0               | DIV1  |        | $LFECLK_{RTCC} = LFECLK$  |
|      | 1               | DIV2  |        | $LFECLK_{RTCC} = LFECLK/2$  |
|      | 2               | DIV4  |        | $LFECLK_{RTCC} = LFECLK/4$  |

**12.5.40 CMU\_HFRADIOALTPRESC - High Frequency Alternate Radio Peripheral Clock Prescaler Register**

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x138         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15    | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PRESC |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 31:17 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 16:8  | PRESC           | 0x000   | RW     | <b>HFRADIOALTCLK Prescaler</b><br>Specifies the clock divider for the HFRADIOALTCLK (relative to HFCLK). |
|       | Value           |   |        | Description  |
|       | PRESC           |   |        | Clock division factor of PRESC+1.  |
| 7:0   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |

### 12.5.41 CMU\_SYNCBUSY - Synchronization Busy Register

| Offset        | Bit Position |    |         |         |              |          |             |          |    |    |    |    |    |          |    |           |    |    |    |    |    |    |   |   |   |           |   |   |           |   |   |           |  |           |
|---------------|--------------|----|---------|---------|--------------|----------|-------------|----------|----|----|----|----|----|----------|----|-----------|----|----|----|----|----|----|---|---|---|-----------|---|---|-----------|---|---|-----------|--|-----------|
| 0x140         | 31           | 30 | 29      | 28      | 27           | 26       | 25          | 24       | 23 | 22 | 21 | 20 | 19 | 18       | 17 | 16        | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6         | 5 | 4 | 3         | 2 | 1 | 0         |  |           |
| <b>Reset</b>  |              |    | 0       | 0       | 0            | 0        | 0           | 0        |    |    |    |    |    | 0        |    | 0         |    |    |    |    |    |    |   |   |   | 0         |   |   | 0         |   |   | 0         |  | 0         |
| <b>Access</b> |              |    | R       | R       | R            | R        | R           | R        |    |    |    |    |    | R        |    | R         |    |    |    |    |    |    |   |   |   | R         |   |   | R         |   |   | R         |  | R         |
| <b>Name</b>   |              |    | LFXOBSY | HFXOBSY | LFRCOVREFBSY | LFRCOBSY | AUXHFRCOBSY | HFRCOBSY |    |    |    |    |    | LFPRESCO |    | LFECLKEN0 |    |    |    |    |    |    |   |   |   | LFBPRESCO |   |   | LFBCLKEN0 |   |   | LFAPRESCO |  | LFACLKEN0 |

| Bit   | Name   | Reset  | Access | Description  |       |             |   |   |   |  |
|-------|--|--|--------|--|-------|-------------|---|---|---|--|
| 31:30 | Reserved   | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |       |             |   |   |   |  |
| 29    | LFXOBSY  | 0  | R      | <p><b>LFXO Busy</b></p> <p>Used to check the synchronization status of CMU_LFXOCTRL.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>CMU_LFXOCTRL is ready for update</td> </tr> <tr> <td>1</td> <td>CMU_LFXOCTRL is busy synchronizing new value</td> </tr> </tbody> </table>  | Value | Description | 0 | CMU_LFXOCTRL is ready for update  | 1 | CMU_LFXOCTRL is busy synchronizing new value   |
| Value | Description  |  |        |  |       |             |   |   |   |  |
| 0     | CMU_LFXOCTRL is ready for update   |  |        |  |       |             |   |   |   |  |
| 1     | CMU_LFXOCTRL is busy synchronizing new value   |  |        |  |       |             |   |   |   |  |
| 28    | HFXOBSY  | 0  | R      | <p><b>HFXO Busy</b></p> <p>Used to check the synchronization status of CMU_HFXOCTRL, CMU_HFXOSTARTUPCTRL, CMU_HFXOSTEADYSTATECTRL, CMU_HFXOTIMEOUTCTRL, CMU_HFXOCTRL1.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>CMU_HFXOCTRL, CMU_HFXOSTARTUPCTRL, CMU_HFXOSTEADYSTATECTRL, CMU_HFXOTIMEOUTCTRL, CMU_HFXOCTRL1 are ready for update</td> </tr> <tr> <td>1</td> <td>CMU_HFXOCTRL, CMU_HFXOSTARTUPCTRL, CMU_HFXOSTEADYSTATECTRL, CMU_HFXOTIMEOUTCTRL, CMU_HFXOCTRL1 are busy synchronizing new value. HFXO is also BUSY when these registers are actively being used (e.g. when HFXOENS=1).</td> </tr> </tbody> </table> | Value | Description | 0 | CMU_HFXOCTRL, CMU_HFXOSTARTUPCTRL, CMU_HFXOSTEADYSTATECTRL, CMU_HFXOTIMEOUTCTRL, CMU_HFXOCTRL1 are ready for update | 1 | CMU_HFXOCTRL, CMU_HFXOSTARTUPCTRL, CMU_HFXOSTEADYSTATECTRL, CMU_HFXOTIMEOUTCTRL, CMU_HFXOCTRL1 are busy synchronizing new value. HFXO is also BUSY when these registers are actively being used (e.g. when HFXOENS=1). |
| Value | Description  |  |        |  |       |             |   |   |   |  |
| 0     | CMU_HFXOCTRL, CMU_HFXOSTARTUPCTRL, CMU_HFXOSTEADYSTATECTRL, CMU_HFXOTIMEOUTCTRL, CMU_HFXOCTRL1 are ready for update  |  |        |  |       |             |   |   |   |  |
| 1     | CMU_HFXOCTRL, CMU_HFXOSTARTUPCTRL, CMU_HFXOSTEADYSTATECTRL, CMU_HFXOTIMEOUTCTRL, CMU_HFXOCTRL1 are busy synchronizing new value. HFXO is also BUSY when these registers are actively being used (e.g. when HFXOENS=1). |  |        |  |       |             |   |   |   |  |
| 27    | LFRCOVREFBSY   | 0  | R      | <p><b>LFRCO VREF Busy</b></p> <p>Used to check the synchronization status of GMCCURTUNE.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>CMU_LFRCOCTRL GMCCURTUNE bitfield is ready for update</td> </tr> <tr> <td>1</td> <td>CMU_LFRCOCTRL GMCCURTUNE bitfield is busy synchronizing new value</td> </tr> </tbody> </table>  | Value | Description | 0 | CMU_LFRCOCTRL GMCCURTUNE bitfield is ready for update   | 1 | CMU_LFRCOCTRL GMCCURTUNE bitfield is busy synchronizing new value  |
| Value | Description  |  |        |  |       |             |   |   |   |  |
| 0     | CMU_LFRCOCTRL GMCCURTUNE bitfield is ready for update  |  |        |  |       |             |   |   |   |  |
| 1     | CMU_LFRCOCTRL GMCCURTUNE bitfield is busy synchronizing new value  |  |        |  |       |             |   |   |   |  |
| 26    | LFRCOBSY   | 0  | R      | <p><b>LFRCO Busy</b></p> <p>Used to check the synchronization status of CMU_LFRCOCTRL.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>CMU_LFRCOCTRL is ready for update</td> </tr> </tbody> </table>   | Value | Description | 0 | CMU_LFRCOCTRL is ready for update   |   |  |
| Value | Description  |  |        |  |       |             |   |   |   |  |
| 0     | CMU_LFRCOCTRL is ready for update  |  |        |  |       |             |   |   |   |  |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
|       | 1               |   |        | CMU_LFRCCOCTRL is busy synchronizing new value  |
| 25    | AUXHFRCOBSY     | 0   | R      | <b>AUXHFRCO Busy</b><br>Used to check the synchronization status of CMU_AUXHFRCOCTRL.                   |
|       | Value           |   |        | Description   |
|       | 0               |   |        | CMU_AUXHFRCOCTRL is ready for update  |
|       | 1               |   |        | CMU_AUXHFRCOCTRL is busy synchronizing new value  |
| 24    | HFRCOBSY        | 0   | R      | <b>HFRCO Busy</b><br>Used to check the synchronization status of CMU_HFRCCOCTRL.                        |
|       | Value           |   |        | Description   |
|       | 0               |   |        | CMU_HFRCCOCTRL is ready for update  |
|       | 1               |   |        | CMU_HFRCCOCTRL is busy synchronizing new value  |
| 23:19 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 18    | LFEPRESC0       | 0   | R      | <b>Low Frequency E Prescaler 0 Busy</b><br>Used to check the synchronization status of CMU_LFEPRESC0.   |
|       | Value           |   |        | Description   |
|       | 0               |   |        | CMU_LFEPRESC0 is ready for update   |
|       | 1               |   |        | CMU_LFEPRESC0 is busy synchronizing new value   |
| 17    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 16    | LFECKEN0        | 0   | R      | <b>Low Frequency E Clock Enable 0 Busy</b><br>Used to check the synchronization status of CMU_LFECKEN0. |
|       | Value           |   |        | Description   |
|       | 0               |   |        | CMU_LFECKEN0 is ready for update  |
|       | 1               |   |        | CMU_LFECKEN0 is busy synchronizing new value  |
| 15:7  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 6     | LFBPRESC0       | 0   | R      | <b>Low Frequency B Prescaler 0 Busy</b><br>Used to check the synchronization status of CMU_LFBPRESC0.   |
|       | Value           |   |        | Description   |
|       | 0               |   |        | CMU_LFBPRESC0 is ready for update   |
|       | 1               |   |        | CMU_LFBPRESC0 is busy synchronizing new value   |
| 5     | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |

| Bit | Name            | Reset   | Access | Description  |
|-----|-----------------|---|--------|--|
| 4   | LFBCLKEN0       | 0   | R      | <b>Low Frequency B Clock Enable 0 Busy</b><br>Used to check the synchronization status of CMU_LFBCLKEN0. |
|     | Value           |   |        | Description  |
|     | 0               |   |        | CMU_LFBCLKEN0 is ready for update  |
|     | 1               |   |        | CMU_LFBCLKEN0 is busy synchronizing new value  |
| 3   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 2   | LFAPRESC0       | 0   | R      | <b>Low Frequency a Prescaler 0 Busy</b><br>Used to check the synchronization status of CMU_LFAPRESC0.    |
|     | Value           |   |        | Description  |
|     | 0               |   |        | CMU_LFAPRESC0 is ready for update  |
|     | 1               |   |        | CMU_LFAPRESC0 is busy synchronizing new value  |
| 1   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 0   | LFACLKEN0       | 0   | R      | <b>Low Frequency a Clock Enable 0 Busy</b><br>Used to check the synchronization status of CMU_LFACLKEN0. |
|     | Value           |   |        | Description  |
|     | 0               |   |        | CMU_LFACLKEN0 is ready for update  |
|     | 1               |   |        | CMU_LFACLKEN0 is busy synchronizing new value  |

12.5.42 CMU\_FREEZE - Freeze Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |           |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-----------|
| 0x144         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0         |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0         |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | RW        |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | REGFREEZE |

| Bit  | Name     | Reset  | Access | Description |
|------|----------|--|--------|-------------|
| 31:1 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |             |

0 REGFREEZE 0 RW **Register Update Freeze**  
 When set, the update of the Low Frequency clock control registers is postponed until this bit is cleared. Use this bit to update several registers simultaneously.

| Value | Mode   | Description   |
|-------|--------|---|
| 0     | UPDATE | Each write access to a Low Frequency clock control register is updated into the Low Frequency domain as soon as possible. |
| 1     | FREEZE | The LE Clock Control registers are not updated with the new written value.  |

## 12.5.43 CMU\_PCNTCTRL - PCNT Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |             |            |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|-------------|------------|---|---|
| 0x150         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3           | 2          | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0           | 0          |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | RWH         | RWH        |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | PCNT0CLKSEL | PCNT0CLKEN |   |   |

| Bit   | Name            | Reset   | Access | Description   |       |      |             |   |        |                          |   |         |   |
|-------|-----------------|---|--------|---|-------|------|-------------|---|--------|--------------------------|---|---------|---|
| 31:2  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |      |             |   |        |                          |   |         |   |
| 1     | PCNT0CLKSEL     | 0   | RWH    | <b>PCNT0 Clock Select</b><br>This bit controls which clock that is used for the PCNT.<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>LFACLK</td> <td>LFACLK is clocking PCNT0</td> </tr> <tr> <td>1</td> <td>PCNT0S0</td> <td>External pin PCNT0_S0 is clocking PCNT0</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | LFACLK | LFACLK is clocking PCNT0 | 1 | PCNT0S0 | External pin PCNT0_S0 is clocking PCNT0 |
| Value | Mode            | Description   |        |   |       |      |             |   |        |                          |   |         |   |
| 0     | LFACLK          | LFACLK is clocking PCNT0  |        |   |       |      |             |   |        |                          |   |         |   |
| 1     | PCNT0S0         | External pin PCNT0_S0 is clocking PCNT0   |        |   |       |      |             |   |        |                          |   |         |   |
| 0     | PCNT0CLKEN      | 0   | RWH    | <b>PCNT0 Clock Enable</b><br>This bit enables/disables the clock to the PCNT.   |       |      |             |   |        |                          |   |         |   |

## 12.5.44 CMU\_ADCCTRL - ADC Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |            |   |   |            |   |   |   |   |   |  |  |  |  |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|------------|---|---|------------|---|---|---|---|---|--|--|--|--|--|--|
| 0x15C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8          | 7 | 6 | 5          | 4 | 3 | 2 | 1 | 0 |  |  |  |  |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | 0          |   |   | 0x0        |   |   |   |   |   |  |  |  |  |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | RWH        |   |   | RWH        |   |   |   |   |   |  |  |  |  |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | ADC0CLKINV |   |   | ADC0CLKSEL |   |   |   |   |   |  |  |  |  |  |  |

| Bit  | Name            | Reset   | Access | Description  |
|------|-----------------|---|--------|--|
| 31:9 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 8    | ADC0CLKINV      | 0   | RWH    | <b>Invert Clock Selected By ADC0CLKSEL</b><br>This bit enables inverting the selected clock to ADC0.   |
| 7:6  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 5:4  | ADC0CLKSEL      | 0x0   | RWH    | <b>ADC0 Clock Select</b><br>This bit controls which clock is used for ADC0 in case ADCCLKMODE in ADCn_CTRL is set to ASYNC. It should only be changed when ADCCLKMODE in ADCn_CTRL is set to SYNC. HFXO should never be selected as clock source for ADC0 when disabling the HFXO (e.g. because of EM2 entry). |
|      | Value           | Mode  |        | Description  |
|      | 0               | DISABLED  |        | ADC0 is not clocked  |
|      | 1               | AUXHFRCO  |        | AUXHFRCO is clocking ADC0  |
|      | 2               | HFXO  |        | HFXO is clocking ADC0  |
|      | 3               | HFSRCCLK  |        | HFSRCCLK is clocking ADC0  |
| 3:0  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |

12.5.45 CMU\_ROUTE PEN - I/O Routing Pin Enable Register

| Offset        | Bit Position |    |    |           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |            |            |
|---------------|--------------|----|----|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|------------|------------|
| 0x170         | 31           | 30 | 29 | 28        | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |            |            |
| <b>Reset</b>  |              |    |    |           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |            |            |
| <b>Access</b> |              |    |    |           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |            |            |
| <b>Name</b>   |              |    |    |           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |            |            |
|               |              |    |    | CLKIN0PEN |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  | CLKOUT1PEN | CLKOUT0PEN |

| Bit   | Name       | Reset   | Access | Description  |
|-------|------------|---|--------|--|
| 31:29 | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 28    | CLKIN0PEN  | 0   | RW     | <b>CLKIN0 Pin Enable</b><br>When set, the CLKIN0 pin is enabled.   |
| 27:2  | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 1     | CLKOUT1PEN | 0   | RW     | <b>CLKOUT1 Pin Enable</b><br>When set, the CLKOUT1 pin is enabled. |
| 0     | CLKOUT0PEN | 0   | RW     | <b>CLKOUT0 Pin Enable</b><br>When set, the CLKOUT0 pin is enabled. |

### 12.5.46 CMU\_ROUTELOC0 - I/O Routing Location Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |            |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|------------|---|---|---|---|---|---|---|---|---|
| 0x174         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9          | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00       |    |    |    |    |    | 0x00       |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW         |    |    |    |    |    | RW         |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CLKOUT1LOC |    |    |    |    |    | CLKOUT0LOC |   |   |   |   |   |   |   |   |   |

| Bit   | Name            | Reset   | Access      | Description   |
|-------|-----------------|---|-------------|---|
| 31:14 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |   |
| 13:8  | CLKOUT1LOC      | 0x00  | RW          | <b>I/O Location</b><br>Decides the location of the CLKOUT1.     |
|       | Value           | Mode  | Description |   |
|       | 0               | LOC0  | Location 0  |   |
|       | 1               | LOC1  | Location 1  |   |
|       | 2               | LOC2  | Location 2  |   |
|       | 3               | LOC3  | Location 3  |   |
|       | 4               | LOC4  | Location 4  |   |
|       | 5               | LOC5  | Location 5  |   |
|       | 6               | LOC6  | Location 6  |   |
|       | 7               | LOC7  | Location 7  |   |
| 7:6   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |   |
| 5:0   | CLKOUT0LOC      | 0x00  | RW          | <b>I/O Location</b><br>Decides the location of the CMU CLKOUT0. |
|       | Value           | Mode  | Description |   |
|       | 0               | LOC0  | Location 0  |   |
|       | 1               | LOC1  | Location 1  |   |
|       | 2               | LOC2  | Location 2  |   |
|       | 3               | LOC3  | Location 3  |   |
|       | 4               | LOC4  | Location 4  |   |
|       | 5               | LOC5  | Location 5  |   |
|       | 6               | LOC6  | Location 6  |   |
|       | 7               | LOC7  | Location 7  |   |

12.5.47 CMU\_ROUTELOC1 - I/O Routing Location Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |           |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|-----------|---|---|---|---|
| 0x178         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4         | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | 0x00      |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | RW        |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | CLKIN0LOC |   |   |   |   |

| Bit  | Name      | Reset  | Access      | Description  |
|------|-----------|--|-------------|--|
| 31:6 | Reserved  | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |             |  |
| 5:0  | CLKIN0LOC | 0x00   | RW          | <b>I/O Location</b><br>Decides the location of the CLKIN0. |
|      | Value     | Mode   | Description |  |
|      | 0         | LOC0   | Location 0  |  |
|      | 1         | LOC1   | Location 1  |  |
|      | 2         | LOC2   | Location 2  |  |
|      | 3         | LOC3   | Location 3  |  |
|      | 4         | LOC4   | Location 4  |  |

12.5.48 CMU\_LOCK - Configuration Lock Register

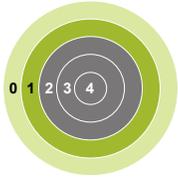
| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x180         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LOCKKEY |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description |
|-------|----------|--|--------|-------------|
| 31:16 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |             |

| Bit  | Name    | Reset  | Access | Description  |
|------|---------|--------|--------|--|
| 15:0 | LOCKKEY | 0x0000 | RWH    | <b>Configuration Lock Key</b><br><br>Write any other value than the unlock code to lock CMU_CTRL, CMU_ROUTEOPEN, CMU_ROUTELOC0, CMU_ROUTELOC1, CMU_HFRCCOCTRL, CMU_AUXHFRCCOCTRL, CMU_LFRCCOCTRL, CMU_ULFRCCOCTRL, CMU_HFXOCTRL, CMU_HFXOCTRL1, CMU_HFXOSTARTUPCTRL, CMU_HFXOSTEADYSTATECTRL, CMU_HFXOTIMEOUTCTRL, CMU_LFXOCTRL, CMU_OSCENCMD, CMU_CMD, CMU_DBGCLKSEL, CMU_HFCLKSEL, CMU_LFACLKSEL, CMU_LFBCLKSEL, CMU_LFECLKSEL, CMU_LFRCLKSEL, CMU_HFBUSCLKEN0, CMU_HFUNDIVCLKEN0, CMU_HFPERCLKEN0, CMU_HFRADIOCLKEN0, CMU_HFRADIOALTCLKEN0, CMU_HFPRESC, CMU_HFCOREPRESC, CMU_HFPERPRESC, CMU_HFRADIOPRESC, CMU_HFRADIOALTPRESC, CMU_HFEXPPRESC, CMU_LFACLKEN0, CMU_LFBCLKEN0, CMU_LFECLKEN0, CMU_LFRCLKEN0, CMU_LFAPRESC0, CMU_LFBPRESC0, CMU_LFEPRESC0, CMU_LFRPRESC0, CMU_ADCCTRL, CMU_LVDSCTRL, and CMU_PCNTCTRL from editing. Write the unlock code to unlock. When reading the register, bit 0 is set when the lock is enabled. |

| Mode            | Value  | Description                |
|-----------------|--------|----------------------------|
| Read Operation  |        |                            |
| UNLOCKED        | 0      | CMU registers are unlocked |
| LOCKED          | 1      | CMU registers are locked   |
| Write Operation |        |                            |
| LOCK            | 0      | Lock CMU registers         |
| UNLOCK          | 0x580E | Unlock CMU registers       |

## 13. SMU - Security Management Unit



### Quick Facts

#### What?

The Security Management Unit (SMU) forms the control and status/reporting component of bus-level security in the EFR32xG13 Wireless Gecko.

#### Why?

Enables a robust and low-energy security solution at the system level

#### How?

Hardware context switching and access control provided via BLS components.

### 13.1 Introduction

The Security Management Unit (SMU) peripheral adds hardware access control over all of the MCU peripherals that are managed by low level firmware integrated into a Real Time Operating System (RTOS). The SMU is used in conjunction with the Cortex-M operating modes (privileged and non-privileged) and the Memory Protection Unit (MPU). The EFR32xG13 Wireless Gecko MCUs include the ARM v7-M MPU that defines configurable access parameters to regions within the entire CPU memory map. The MPU is not covered in detail in this reference manual. For a complete description of the MPU registers etc, consult the ARM v7-M Architecture Reference Manual. The MPU can define up to 8 regions of varying sizes within the memory map, with each region also being able to be split into 8 equal sub-regions. Using these regions, firmware can define rules that enforce privileged and non-privileged accesses to different memory locations. For example, sections of flash can be marked as privileged access, whereas other areas within the flash can be marked as having non-privileged mode access. Only privileged mode regions can access other privileged mode regions. Accesses attempted by a non-privileged region to a privileged region will cause a fault. The access permissions can be extended across the entire memory map including the peripheral region.

The Cortex-M starts up in privileged mode and the MPU is disabled after reset which means all regions in the memory map are accessible to the running application code. For many applications this is sufficient and the MPU remains disabled. However, when using a RTOS the kernel requires protection from user code and will switch to privileged mode and create tasks in non-privileged or thread mode. In addition, security is also a concern, so MCU peripherals should be protected to avoid security holes. Adding peripheral security to systems requires an increased number of MPU regions to protect areas such as the peripheral registers, including bit set/clear and bit banding regions. The defined regions are also dynamic based on the task requirements and in many cases the number of regions required exceeds the number of regions that can be enabled by the MPU.

The SMU is used to extend the access controls of each peripheral beyond the number of regions available using the MPU. The SMU peripheral registers provide the configuration and status bits for the Peripheral Protection Unit (PPU) to the CPU. The PPU is the underlying hardware component that operates on the low level bus interfaces within the SoC to derive the status for each peripheral .

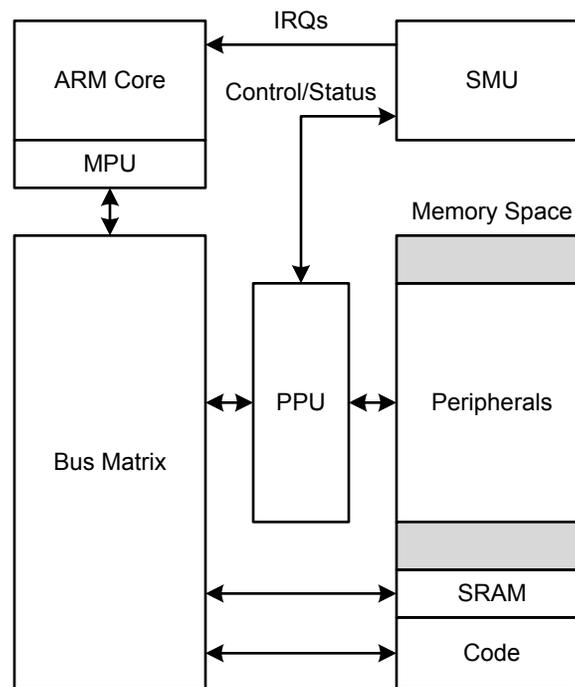
### 13.2 Features

The main features of the SMU are as follows:

- Contains control and status registers for hardware bus level component instances (e.g., the PPU)
- Simplifies RTOS context switching
  - Hardware to complement any software context switching enabled by an MPU
  - Hardware-enforced access control extends capability of the v7-M MPU regions
  - One bit control per peripheral reduces software overhead while dynamically modifying access permissions
- A configurable interrupt line that can be triggered from peripheral access fault events

### 13.3 Functional Description

An overview of the SMU module within the system is shown in [Figure 13.1 Bus-Level Security System View](#) on page 405.



**Figure 13.1. Bus-Level Security System View**

#### 13.3.1 PPU - Peripheral Protection Unit

The number of peripheral memory regions on the device exceeds the number of configurable regions available using the MPU. While it is possible to manage finer granularity of memory security through software, the PPU provides a hardware solution for fine-grained peripheral-level protection to eliminate the performance degradation associated with a partially software-managed solution.

The PPU provides a hardware access barrier to any peripheral that is configured to be protected. When an attempt is made to access a peripheral without the required privilege level, the PPU detects the fault and intercepts the access. No write or read of the peripheral register space occurs, and an all-zero value is returned if the access is a read. See [13.3.2.2 PPU Control](#) for more details on how access faults are reported to the CPU.

**Note:** The CPU is the only system bus master in the EFR32xG13 Wireless Gecko that can trigger access faults. All other masters are given full access privileges and have no configurable context switching enabled.

### 13.3.2 Programming Model

The SMU does not provide any access control out of reset and needs to be configured by software. SMU access controls should be configured along with the MPU configuration. This is typically performed in a bootloader or other low level RTOS kernel/supervisor code prior to user code or other non-privileged code execution. At least one MPU region will be allocated to the entire peripheral region as a full access region (0x4000\_0000 - 0x4006\_FFFF). An RTOS kernel/supervisor can dynamically allocate peripheral accessibility by maintaining the hardware and software contexts available to each task. In the chart below there are multiple tasks and the system switches between Task A and Task B via the RTOS handler. There are 16 peripherals shown in the example split between two regions. Task A has rights to access peripherals 0, 1, 4, 5 and 7, whereas task B has rights to access the complement of A (2, 3, and 6). After a Task B IRQ, the privileged OS handler is entered which signals the supervisor to reprogram the regions using the SMU based on an access control list. Control is then handed to Task B in non-privileged mode.

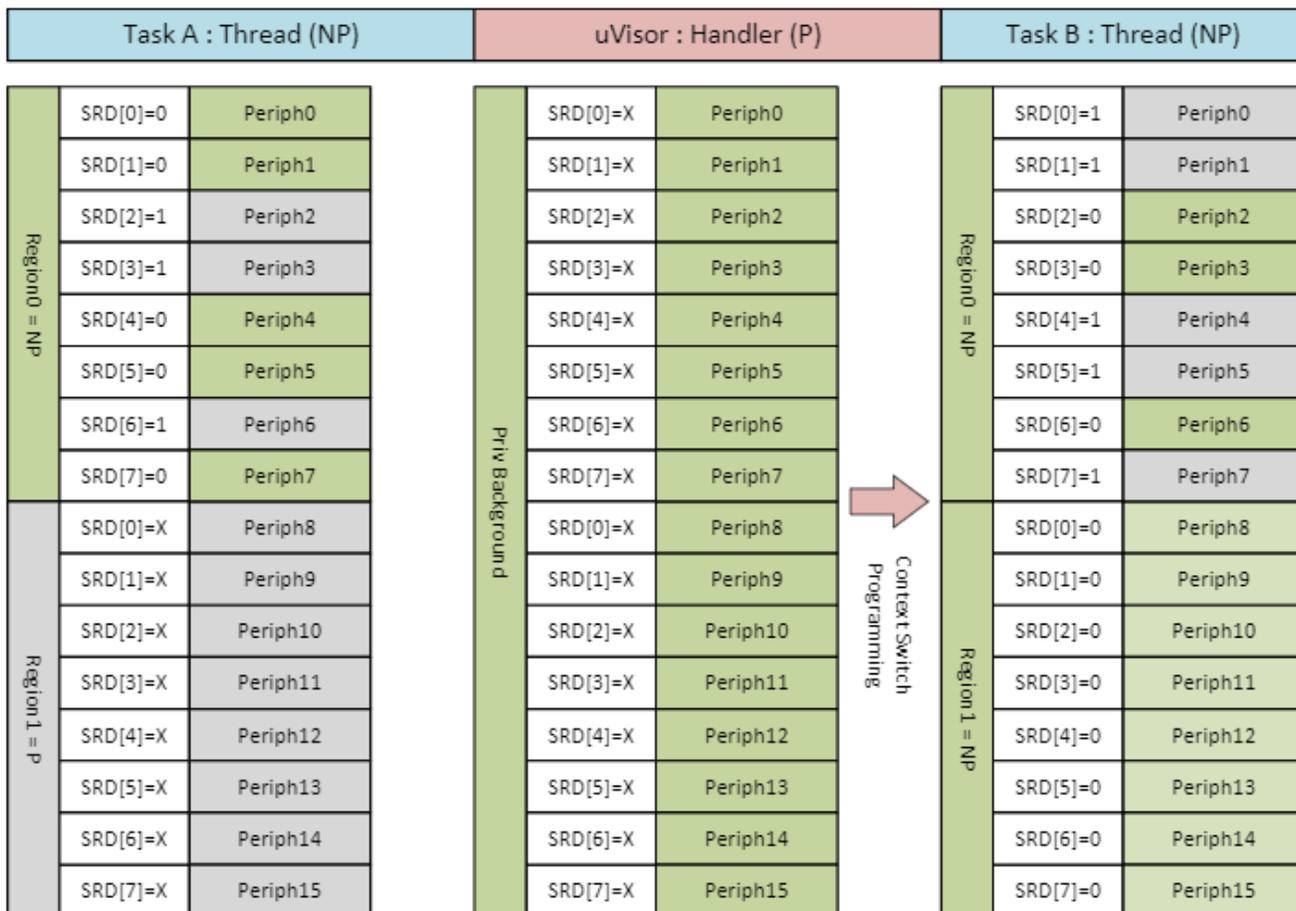


Figure 13.2. Peripheral Access Control Example

All hardware protections happen immediately in response to SMU configuration register writes without any latency cycles. However, since software instructions may be optimized or pipelined, it is important to make sure that software memory barrier instructions are used as needed after any SMU re-configuration before moving on or changing contexts. This ensures that the hardware context switch has taken full effect.

For the remainder of this section, the programming model is split into general SMU controls and component-specific controls (e.g., PPU).

#### 13.3.2.1 Interrupt Control/Status

The SMU follows the standard EFR32xG13 Wireless Gecko interrupt programming model with SMU\_IF/IFS/IFC/IEN registers.

There is one interrupt bit PUPRIV that will trigger on privilege faults detected by the PPU. Such fault mechanisms are configured as specified in [13.3.2.2 PPU Control](#).

### 13.3.2.2 PPU Control

The PPU\_CTRL register provides an ENABLE bit that allows bypassing all PPU checking when set to 0. In this case, the rest of the PPU registers have no effect, and no access faults will occur. This is the reset state of the SMU.

When the ENABLE bit of PPU\_CTRL register is asserted, access protection is configured on a peripheral-by-peripheral basis using the SMU\_PPUPATDx register(s). Setting a bit in the SMU\_PPUPATDx register to one configures the corresponding peripheral controlled by that bit to privileged access only. The single bit mode control for each peripheral provides fast hardware context switching for peripheral sharing, while still supporting fast software context switches for task-based CPU context switching.

**Note:** The SMU itself is a peripheral which has protection afforded by the PPU. A proper security/privilege context configuration requires setting of the SMU's access control bits properly at startup so that only a top-level task (e.g., a uVisor from ARM) can perform security/privilege context switches.

When a peripheral has access protection configured and the peripheral is accessed with invalid privilege credentials, then an access fault occurs. The corresponding interrupt flag in SMU\_IF is asserted and the ID of the peripheral for which an unprivileged access was attempted is captured in the PERIPID bit-field of the PPU Fault Status register (SMU\_PPUFS). This peripheral ID is held stable until all PPU interrupt flags are cleared to ensure that the first unprivileged access that caused the fault is not overwritten due to subsequent faults before being acknowledged by software.

**Note:** In the case of simultaneously occurring faults (which may be possible in some systems), only one of the faults' peripheral IDs will be captured. There is no inherent peripheral priority defined that would result in one peripheral being recognized before another.

## 13.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name         | Type  | Description                            |
|--------|--------------|-------|--|
| 0x00C  | SMU_IF       | R     | Interrupt Flag Register                |
| 0x010  | SMU_IFS      | W1    | Interrupt Flag Set Register            |
| 0x014  | SMU_IFC      | (R)W1 | Interrupt Flag Clear Register          |
| 0x018  | SMU_IEN      | RW    | Interrupt Enable Register              |
| 0x040  | SMU_PPUCTRL  | RW    | PPU Control Register                   |
| 0x050  | SMU_PPUPATD0 | RW    | PPU Privilege Access Type Descriptor 0 |
| 0x054  | SMU_PPUPATD1 | RW    | PPU Privilege Access Type Descriptor 1 |
| 0x090  | SMU_PPUFS    | R     | PPU Fault Status                       |

## 13.5 Register Description

### 13.5.1 SMU\_IF - Interrupt Flag Register

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |         |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---------|
| 0x00C  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0       |
| Reset  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0       |
| Access |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | R       |
| Name   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | PPUPRIV |

| Bit  | Name     | Reset   | Access | Description  |
|------|----------|---|--------|--|
| 31:1 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 0    | PPUPRIV  | 0   | R      | <b>PPU Privilege Interrupt Flag</b><br>Triggered when a privilege fault occurs in the Peripheral Protection Unit |

### 13.5.2 SMU\_IFS - Interrupt Flag Set Register

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |         |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---------|
| 0x010  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0       |
| Reset  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0       |
| Access |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | W1      |
| Name   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | PPUPRIV |

| Bit  | Name     | Reset   | Access | Description  |
|------|----------|---|--------|--|
| 31:1 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 0    | PPUPRIV  | 0   | W1     | <b>Set PPUPRIV Interrupt Flag</b><br>Write 1 to set the PPUPRIV interrupt flag |

### 13.5.3 SMU\_IFC - Interrupt Flag Clear Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |         |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---------|
| 0x014         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0       |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0       |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | (R)W1   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | PPUPRIV |

| Bit  | Name     | Reset   | Access | Description   |
|------|----------|---|--------|---|
| 31:1 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 0    | PPUPRIV  | 0   | (R)W1  | <b>Clear PPUPRIV Interrupt Flag</b><br><br>Write 1 to clear the PPUPRIV interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |

### 13.5.4 SMU\_IEN - Interrupt Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |         |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---------|
| 0x018         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0       |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0       |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | RW      |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | PPUPRIV |

| Bit  | Name     | Reset   | Access | Description   |
|------|----------|---|--------|---|
| 31:1 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 0    | PPUPRIV  | 0   | RW     | <b>PPUPRIV Interrupt Enable</b><br><br>Enable/disable the PPUPRIV interrupt |

### 13.5.5 SMU\_PPCTRL - PPU Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |        |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|--------|
| 0x040         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0      |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0      |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | RW     |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | ENABLE |

| Bit  | Name     | Reset  | Access | Description                                 |
|------|----------|--|--------|---|
| 31:1 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 0    | ENABLE   | 0  | RW     | Set to enable checking of peripheral access |
|      | Value    | Description  |        |   |
|      | 0        | Privilege/Security-level checking completely bypassed in the PPU   |        |   |
|      | 1        | Behavior controlled by PPU_PATD  |        |   |

**13.5.6 SMU\_PPUPATD0 - PPU Privilege Access Type Descriptor 0**

Set peripheral bits to 1 to mark as privileged access only

| Offset        | Bit Position |    |    |    |       |    |         |          |         |      |     |       |      |      |      |       |    |       |     |     |       |      |         |         |           |   |     |   |   |   |   |      |       |       |  |
|---------------|--------------|----|----|----|-------|----|---------|----------|---------|------|-----|-------|------|------|------|-------|----|-------|-----|-----|-------|------|---------|---------|-----------|---|-----|---|---|---|---|------|-------|-------|--|
|               | 31           | 30 | 29 | 28 | 27    | 26 | 25      | 24       | 23      | 22   | 21  | 20    | 19   | 18   | 17   | 16    | 15 | 14    | 13  | 12  | 11    | 10   | 9       | 8       | 7         | 6 | 5   | 4 | 3 | 2 | 1 | 0    |       |       |  |
| 0x050         |              |    |    |    |       |    |         |          |         |      |     |       |      |      |      |       |    |       |     |     |       |      |         |         |           |   |     |   |   |   |   |      |       |       |  |
| <b>Reset</b>  |              |    |    |    | 0     |    | 0       | 0        | 0       | 0    | 0   | 0     | 0    | 0    | 0    | 0     |    | 0     | 0   | 0   | 0     | 0    | 0       | 0       | 0         |   | 0   |   |   |   |   |      |       |       |  |
| <b>Access</b> |              |    |    |    | RW    |    | RW      | RW       | RW      | RW   | RW  | RW    | RW   | RW   | RW   | RW    |    | RW    | RW  | RW  | RW    | RW   | RW      | RW      | RW        |   | RW  |   |   |   |   |      |       |       |  |
| <b>Name</b>   |              |    |    |    | PCNT0 |    | LEUART0 | LETIMER0 | LESENSE | LDMA | MSC | IDAC0 | I2C1 | I2C0 | GPIO | GPCRC |    | FPUEH | EMU | PRS | VDAC0 | CSEN | CRYPTO1 | CRYPTO0 | CRYOTIMER |   | CMU |   |   |   |   | ADC0 | ACMP1 | ACMP0 |  |

| Bit   | Name     | Reset  | Access | Description  |
|-------|----------|--|--------|--|
| 31:28 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 27    | PCNT0    | 0  | RW     | <b>Pulse Counter 0 access control bit</b><br>Access control only for PCNT0                       |
| 26    | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 25    | LEUART0  | 0  | RW     | <b>Low Energy UART 0 access control bit</b><br>Access control only for LEUART0                   |
| 24    | LETIMER0 | 0  | RW     | <b>Low Energy Timer 0 access control bit</b><br>Access control only for LETIMER0                 |
| 23    | LESENSE  | 0  | RW     | <b>Low Energy Sensor Interface access control bit</b><br>Access control only for LESENSE         |
| 22    | LDMA     | 0  | RW     | <b>Linked Direct Memory Access Controller access control bit</b><br>Access control only for LDMA |
| 21    | MSC      | 0  | RW     | <b>Memory System Controller access control bit</b><br>Access control only for MSC                |
| 20    | IDAC0    | 0  | RW     | <b>Current Digital to Analog Converter 0 access control bit</b><br>Access control only for IDAC0 |
| 19    | I2C1     | 0  | RW     | <b>I2C 1 access control bit</b><br>Access control only for I2C1                                  |
| 18    | I2C0     | 0  | RW     | <b>I2C 0 access control bit</b><br>Access control only for I2C0                                  |
| 17    | GPIO     | 0  | RW     | <b>General purpose Input/Output access control bit</b><br>Access control only for GPIO           |
| 16    | GPCRC    | 0  | RW     | <b>General Purpose CRC access control bit</b><br>Access control only for GPCRC                   |
| 15    | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |

| Bit | Name            | Reset   | Access | Description   |
|-----|-----------------|---|--------|---|
| 14  | FPUEH           | 0   | RW     | <b>FPU Exception Handler access control bit</b><br>Access control only for FPUEH                        |
| 13  | EMU             | 0   | RW     | <b>Energy Management Unit access control bit</b><br>Access control only for EMU                         |
| 12  | PRS             | 0   | RW     | <b>Peripheral Reflex System access control bit</b><br>Access control only for PRS                       |
| 11  | VDAC0           | 0   | RW     | <b>Digital to Analog Converter 0 access control bit</b><br>Access control only for VDAC0                |
| 10  | CSEN            | 0   | RW     | <b>Capacitive touch sense module access control bit</b><br>Access control only for CSEN                 |
| 9   | CRYPTO1         | 0   | RW     | <b>Advanced Encryption Standard Accelerator 1 access control bit</b><br>Access control only for CRYPTO1 |
| 8   | CRYPTO0         | 0   | RW     | <b>Advanced Encryption Standard Accelerator 0 access control bit</b><br>Access control only for CRYPTO0 |
| 7   | CRYOTIMER       | 0   | RW     | <b>CRYOTIMER access control bit</b><br>Access control only for CRYOTIMER                                |
| 6   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 5   | CMU             | 0   | RW     | <b>Clock Management Unit access control bit</b><br>Access control only for CMU                          |
| 4:3 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 2   | ADC0            | 0   | RW     | <b>Analog to Digital Converter 0 access control bit</b><br>Access control only for ADC0                 |
| 1   | ACMP1           | 0   | RW     | <b>Analog Comparator 1 access control bit</b><br>Access control only for ACMP1                          |
| 0   | ACMP0           | 0   | RW     | <b>Analog Comparator 0 access control bit</b><br>Access control only for ACMP0                          |

**13.5.7 SMU\_PPUPATD1 - PPU Privilege Access Type Descriptor 1**

Set peripheral bits to 1 to mark as privileged access only

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |       |       |        |        |        |       |        |        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|-------|-------|--------|--------|--------|-------|--------|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14    | 13    | 12     | 11     | 10     | 9     | 8      | 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |  |  |
| 0x054         |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |       |       |        |        |        |       |        |        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       | 0     | 0     | 0      | 0      | 0      | 0     | 0      | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |    |    |    |    |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      | RW    | RW    | RW     | RW     | RW     | RW    | RW     | RW     | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | WTIMER0 | WDOG1 | WDOG0 | USART2 | USART1 | USART0 | TRNG0 | TIMER1 | TIMER0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |  |  |

| Bit   | Name     | Reset   | Access | Description   |
|-------|----------|---|--------|---|
| 31:13 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 12    | WTIMER0  | 0   | RW     | <b>Wide Timer 0 access control bit</b><br>Access control only for WTIMER0   |
| 11    | WDOG1    | 0   | RW     | <b>Watchdog 1 access control bit</b><br>Access control only for WDOG1   |
| 10    | WDOG0    | 0   | RW     | <b>Watchdog 0 access control bit</b><br>Access control only for WDOG0   |
| 9     | USART2   | 0   | RW     | <b>Universal Synchronous/Asynchronous Receiver/Transmitter 2 access control bit</b><br>Access control only for USART2 |
| 8     | USART1   | 0   | RW     | <b>Universal Synchronous/Asynchronous Receiver/Transmitter 1 access control bit</b><br>Access control only for USART1 |
| 7     | USART0   | 0   | RW     | <b>Universal Synchronous/Asynchronous Receiver/Transmitter 0 access control bit</b><br>Access control only for USART0 |
| 6     | TRNG0    | 0   | RW     | <b>True Random Number Generator 0 access control bit</b><br>Access control only for TRNG0                             |
| 5     | TIMER1   | 0   | RW     | <b>Timer 1 access control bit</b><br>Access control only for TIMER1   |
| 4     | TIMER0   | 0   | RW     | <b>Timer 0 access control bit</b><br>Access control only for TIMER0   |
| 3     | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 2     | SMU      | 0   | RW     | <b>Security Management Unit access control bit</b><br>Access control only for SMU                                     |
| 1     | RTCC     | 0   | RW     | <b>Real-Time Counter and Calendar access control bit</b><br>Access control only for RTCC                              |

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| Bit | Name | Reset | Access | Description  |
|-----|------|-------|--------|--|
| 0   | RMU  | 0     | RW     | <b>Reset Management Unit access control bit</b><br>Access control only for RMU |

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## 13.5.8 SMU\_PPUFS - PPU Fault Status

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |          |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|----------|---|---|---|---|
| 0x090         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4        | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | 0x00     |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | R        |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | PERIPHID |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description |
|------|----------|--|--------|-------------|
| 31:7 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |             |
| 6:0  | PERIPHID | 0x00   | R      |             |

Holds the peripheral ID of the first peripheral that was accessed resulting in an access fault. This ID is not valid unless one of the PPU interrupt flags is set. Any other access faults that occur are not captured until all the PPU interrupt flags are cleared

| Value | Mode      | Description                                |
|-------|-----------|--|
| 0     | ACMP0     | Analog Comparator 0                        |
| 1     | ACMP1     | Analog Comparator 1                        |
| 2     | ADC0      | Analog to Digital Converter 0              |
| 5     | CMU       | Clock Management Unit                      |
| 7     | CRYOTIMER | CRYOTIMER                                  |
| 8     | CRYPTO0   | Advanced Encryption Standard Accelerator 0 |
| 9     | CRYPTO1   | Advanced Encryption Standard Accelerator 1 |
| 10    | CSEN      | Capacitive touch sense module              |
| 11    | VDAC0     | Digital to Analog Converter 0              |
| 12    | PRS       | Peripheral Reflex System                   |
| 13    | EMU       | Energy Management Unit                     |
| 14    | FPUEH     | FPU Exception Handler                      |
| 16    | GPCRC     | General Purpose CRC                        |
| 17    | GPIO      | General purpose Input/Output               |
| 18    | I2C0      | I2C 0                                      |
| 19    | I2C1      | I2C 1                                      |
| 20    | IDAC0     | Current Digital to Analog Converter 0      |
| 21    | MSC       | Memory System Controller                   |
| 22    | LDMA      | Linked Direct Memory Access Controller     |
| 23    | LESENSE   | Low Energy Sensor Interface                |
| 24    | LETIMER0  | Low Energy Timer 0                         |
| 25    | LEUART0   | Low Energy UART 0                          |

| Bit | Name | Reset   | Access | Description   |
|-----|------|---------|--------|---|
| 27  |      | PCNT0   |        | Pulse Counter 0   |
| 32  |      | RMU     |        | Reset Management Unit                                     |
| 33  |      | RTCC    |        | Real-Time Counter and Calendar                            |
| 34  |      | SMU     |        | Security Management Unit                                  |
| 36  |      | TIMER0  |        | Timer 0   |
| 37  |      | TIMER1  |        | Timer 1   |
| 38  |      | TRNG0   |        | True Random Number Generator 0                            |
| 39  |      | USART0  |        | Universal Synchronous/Asynchronous Receiver/Transmitter 0 |
| 40  |      | USART1  |        | Universal Synchronous/Asynchronous Receiver/Transmitter 1 |
| 41  |      | USART2  |        | Universal Synchronous/Asynchronous Receiver/Transmitter 2 |
| 42  |      | WDOG0   |        | Watchdog 0  |
| 43  |      | WDOG1   |        | Watchdog 1  |
| 44  |      | WTIMER0 |        | Wide Timer 0  |

## 14. RTCC - Real Time Counter and Calendar



### Quick Facts

#### What?

The Real Time Counter and Calendar (RTCC) is a 32-bit counter ensuring timekeeping in low energy modes. The RTCC also includes a calendar mode for easy time and date keeping. In addition, the RTCC includes 128 bytes of general purpose retention data, allowing persistent data storage in all energy modes except EM4 Shutoff.

#### Why?

Timekeeping over long time periods while using as little power as possible is required in many low power applications.

#### How?

A low frequency oscillator is used as clock signal and the RTCC has three different Capture/Compare channels which can trigger wake-up, generate PRS signalling, or capture system events. 32-bit resolution and selectable prescaling allow the system to stay in low energy modes for long periods of time and still maintain reliable timekeeping.

### 14.1 Introduction

The Real Time Counter and Calendar (RTCC) contains a 32-bit counter/calendar in combination with a 15-bit pre-counter to allow flexible prescaling of the main counter. The RTCC is available in all energy modes except EM4 Shutoff.

Three individually configurable Capture/Compare channels are available in the RTCC. These can be used to trigger interrupts, generate PRS signals, capture system events, and to wake the device up from a low energy mode. The RTCC also includes 128 bytes of general purpose storage and a Binary Coded Decimal (BCD) calendar mode, enabling easy time and date keeping.

### 14.2 Features

- 32-bit Real Time Counter.
- 15-bit pre-counter, for flexible frequency scaling or for use as an independent counter.
- EM4 Hibernate operation and wakeup.
- 128 byte general purpose retention data.
- Oscillator failure detection.
- Can continue through system reset; only reset by power loss, pin, or software reset.
- Calendar mode.
  - BCD encoding.
  - Three programmable alarms.
  - Leap year correction.
- Three Capture/Compare registers.
  - Capture of PRS events from other parts of the system.
  - Compare match or input capture can trigger interrupts.
  - Compare register 1, RTCC\_CC1\_CCV can be used as a top value for the main counter.
  - Compare register 0, RTCC\_CC0\_CCV can be used as a top value for the pre-counter.
  - Compare match events are available to other peripherals through the Peripheral Reflex System (PRS).

### 14.3 Functional Description

The RTCC is a 32-bit up-counter with three Capture/Compare channels. In addition, the RTCC includes a 15-bit pre-counter which can be used as an independent counter or to prescale the main counter. An overview of the RTCC module is shown in [Figure 14.1 RTCC Overview on page 418](#).

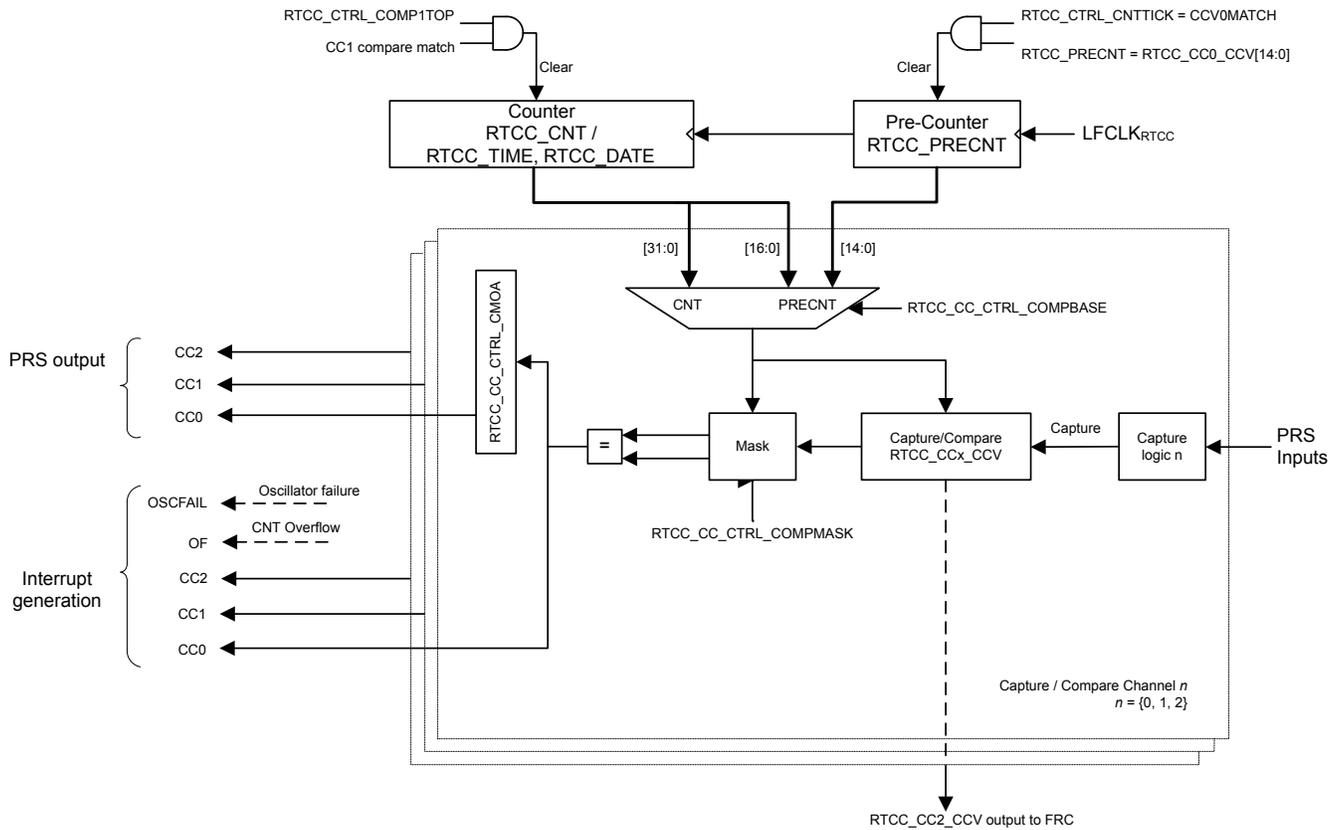


Figure 14.1. RTCC Overview

### 14.3.1 Counter

The RTCC consists of two counters; the 32-bit main counter, RTCC\_CNT (RTCC\_TIME and RTCC\_DATE in calendar mode), and a 15-bit pre-counter, RTCC\_PRECNT. The pre-counter can be used as an independent counter or to generate a specific frequency for the main counter. In both configurations, the pre-counter can be used to generate compare match events or be captured in the Capture/Compare channels as a result of an external PRS event. Refer to [14.3.2 Capture/Compare Channels](#) for details on how to configure the Capture/Compare channels for use with the pre-counter.

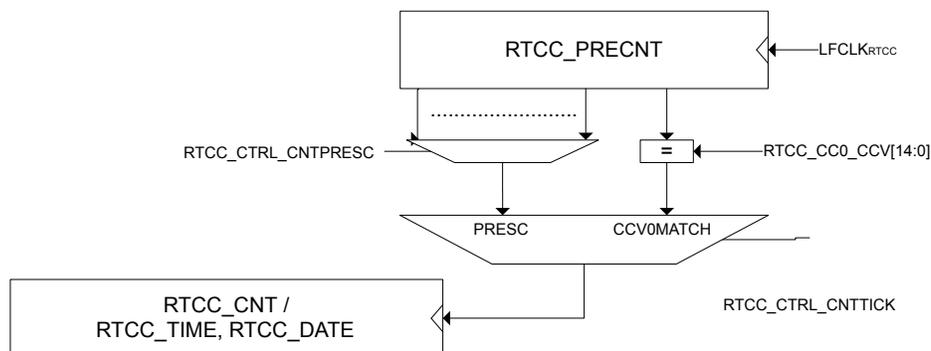


Figure 14.2. RTCC counters

The RTCC is enabled by setting the ENABLE bit in RTCC\_CTRL. When the RTCC is enabled, the pre-counter (RTCC\_PRECNT) increments upon each positive clock edge of LFCLK<sub>RTCC</sub>. If CNTTICK in RTCC\_CTRL is set to PRESC, the pre-counter will continue to count up, wrapping around to zero when it overflows. If CNTTICK in RTCC\_CTRL is set to CCV0MATCH, the pre-counter will wrap around when it hits the value configured in RTCC\_CC0\_CCV.

The main counter of the RTCC, RTCC\_CNT, has two modes; normal mode and calendar mode. In normal mode, the main counter is available in RTCC\_CNT and increments upon each tick given from the pre-counter. Refer to [14.3.1.1 Normal Mode](#) for a description on how to configure the frequency of these ticks. In calendar mode, the counter value is available in RTCC\_TIME and RTCC\_DATE, keeping track of seconds, minutes, hours, day of month, day of week, months, and years, all encoded in BCD format. Refer to [14.3.1.2 Calendar Mode](#) for details on this mode. The mode of the main counter is configured in CNTMODE in RTCC\_CTRL. The differences between the two modes are summarized below.

- **Normal mode**

- Incremental counter, RTCC\_CNT.
- RTCC\_CCx\_CCV used for Capture/Compare value.

- **Calendar mode**

- BCD counters, RTCC\_DATE, RTCC\_TIME.
- RTCC\_CCx\_TIME and RTCC\_CCx\_DATE used for Capture/Compare value.

**Note:** The mode of the RTCC must be configured for CALENDAR mode in RTCC\_CTRL\_CNTMODE before writing to the mode dependent registers, RTCC\_TIME, RTCC\_DATE, RTCC\_CCx\_TIME, and RTCC\_CCx\_DATE. Writes to these registers when in NORMAL mode will be ignored.

### 14.3.1.1 Normal Mode

The main counter can receive a tick based on different tapplings from the pre-counter, allowing the ticks to be power of 2 divisions of the  $LFCLK_{RTCC}$ . For more accurate configuration of the tick frequency,  $RTCC\_CC0\_CCV[14:0]$  can be used as a top value for  $RTCC\_PRECNT$ . When reaching the top value, the main counter receives a tick and the pre-counter wraps around. [Table 14.1 RTCC Resolution Vs Overflow,  \$F\_{LFCLK} = 32768\$  Hz on page 420](#) summarizes the resolutions available when using a 32768 Hz oscillator as source for  $LFCLK_{RTCC}$ .

**Table 14.1. RTCC Resolution Vs Overflow,  $F_{LFCLK} = 32768$  Hz**

| RTCC_CTRL_CNTTICK | RTCC_CTRL_CNTPRESC | Main counter period, $T_{CNT}$     | Overflow                       |
|-------------------|--------------------|------------------------------------|--------------------------------|
| CCV0MATCH         | Don't care         | $(RTCC\_CC0\_CCV + 1)/F_{LFCLK}$ s | $2^{32} \cdot T_{CNT}$ seconds |
| PRESC             | DIV1               | 30.5 $\mu$ s                       | 36.4 hours                     |
|                   | DIV2               | 61 $\mu$ s                         | 72.8 hours                     |
|                   | DIV4               | 122 $\mu$ s                        | 145.6 hours                    |
|                   | DIV8               | 244 $\mu$ s                        | 12 days                        |
|                   | DIV16              | 488 $\mu$ s                        | 24 days                        |
|                   | DIV32              | 977 $\mu$ s                        | 48 days                        |
|                   | DIV64              | 1.95 ms                            | 97 days                        |
|                   | DIV128             | 3.91 ms                            | 194 days                       |
|                   | DIV256             | 7.81 ms                            | 388 days                       |
|                   | DIV512             | 15.6 ms                            | 776 days                       |
|                   | DIV1024            | 31.25 ms                           | 4.2 years                      |
|                   | DIV2048            | 62.5 ms                            | 8.5 years                      |
|                   | DIV4096            | 0.125 s                            | 17 years                       |
|                   | DIV8192            | 0.25 s                             | 34 years                       |
| DIV16384          | 0.5 s              | 68 years                           |                                |
| DIV32768          | 1 s                | 136 years                          |                                |

By default, the counter will keep counting until it reaches the top value, 0xFFFFFFFF, before it wraps around and continues counting from zero. By setting  $CCV1TOP$  in  $RTCC\_CTRL$ , a Capture/Compare channel 1 compare match will result in the main counter wrapping to 0. The timer will then wrap around on a channel 1 compare match ( $RTCC\_CNT = RTCC\_CC1\_CCV$ ). Before using the  $CCV1TOP$  setting, make sure to set this bit prior to or at the same time the RTCC is enabled. Setting  $CCV1TOP$  after enabling the RTCC ( $RTCC\_CTRL\_MODE \neq DISABLED$ ) may cause unintended operation (e.g. if  $RTCC\_CNT > RTCC\_CC1\_CCV$ ,  $RTCC\_CNT$  will wrap when reaching 0xFFFFFFFF rather than  $RTCC\_CC1\_CCV$ ).

**Note:** If the RTCC is being reconfigured, and capture compare channel 1 has previously been used, a  $CCV1TOP$  wrap event might be pending. This would lead to the first tick of the main counter being a wrap to 0. To clear any pending wrap events, use the following procedure before reconfiguring the RTCC:

1.  $RTCC \rightarrow CC[1].CTRL = RTCC\_CC\_CTRL\_MODE\_OFF$ ;
2.  $RTCC \rightarrow CTRL = RTCC\_CTRL\_CNTTICK\_PRESC | RTCC\_CTRL\_CNTMODE\_NORMAL | RTCC\_CTRL\_ENABLE$ ;
3.  $rtcc\_cnt\_pre = RTCC \rightarrow CNT$ ;
4.  $while(RTCC \rightarrow CNT == rtcc\_cnt\_pre)$ ;
5. Reconfigure the RTCC

### 14.3.1.2 Calendar Mode

The RTCC includes a calendar mode which implements time and date decoding in hardware. Calendar mode is enabled by configuring CNTMODE in RTCC\_CTRL to CALENDAR. When in calendar mode, the counter value is available in RTCC\_TIME and RTCC\_DATE. RTCC\_TIME shows seconds, minutes, and hours while RTCC\_DATE shows day of month, month, year, and day of week. RTCC\_TIME and RTCC\_DATE are encoded in BCD format. In calendar mode, the pre-counter should be configured to give ticks with a period of one second, i.e. RTCC\_CTRL\_CNTTICK should be set to PRESC, and the CNTPRESC bitfield of the RTCC\_CTRL register should be set to DIV32768 if a 32768 Hz clock source is used.

In calendar mode, the time and date registers of the capture compare channels, RTCC\_CCx\_TIME and RTCC\_CCx\_DATE, are used to set compare values. Compare values can be set on seconds, minutes, hours, days, and months. Whether day of week or day of month is used for a Capture/Compare channel, it is configured in RTCC\_CCx\_CTRL\_DAYCC of the respective Capture/Compare channel.

The RTCC will automatically compensate for 28-, 29- (leap year), 30-, and 31-day months. The day of week counter, RTCC\_DATE\_DAYOW, is a three bit counter incrementing when RTCC\_TIME\_HOURT overflows, wrapping around every seventh day. Automatic leap year correction, extending the month of February from 28 to 29 days every fourth year is by default enabled, but can be disabled by setting the LYEARCORRDIS bit in RTCC\_CTRL. The pseudo-code for leap year correction is as follows:

```
if RTCC_DATE YEART modulo 2 = 0:
  if RTCC_DATE YEARU modulo 4 = 0:
    leap_year = true
  else:
    leap_year = false
else:
  if (RTCC_DATE YEARU + 2) modulo 4 = 0:
    leap_year = true
  else:
    leap_year = false
```

The seconds, minute, hour segments are represented in 24-hour BCD format. The month segments are enumerated as shown in [Table 14.2 RTCC calendar enumeration on page 421](#).

**Table 14.2. RTCC calendar enumeration**

| Month     | RTCC_DATE_MONTHT | RTCC_DATE_MONTHU |
|-----------|------------------|------------------|
| January   | 0b0              | 0b0001           |
| February  | 0b0              | 0b0010           |
| March     | 0b0              | 0b0011           |
| April     | 0b0              | 0b0100           |
| May       | 0b0              | 0b0101           |
| June      | 0b0              | 0b0110           |
| July      | 0b0              | 0b0111           |
| August    | 0b0              | 0b1000           |
| September | 0b0              | 0b1001           |
| October   | 0b1              | 0b0000           |
| November  | 0b1              | 0b0001           |
| December  | 0b1              | 0b0010           |

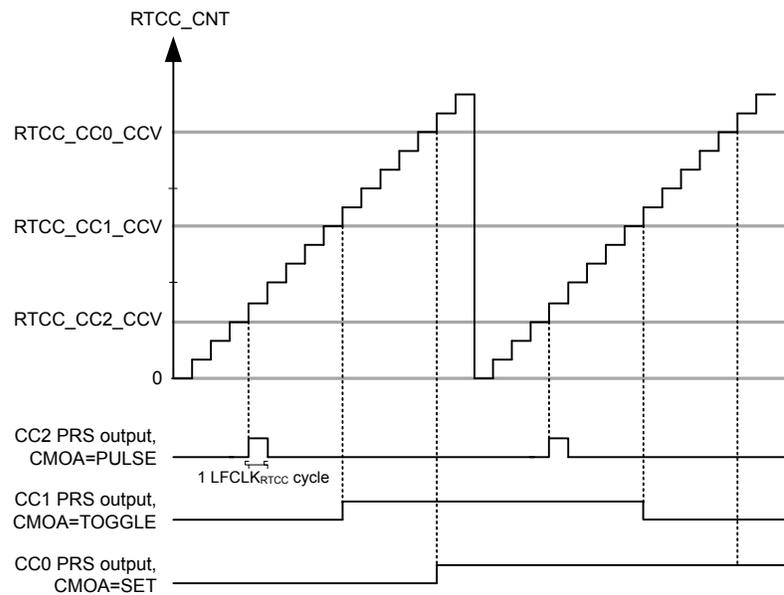
### 14.3.1.3 RTCC Initialization

The counters of the RTCC, RTCC\_CNT (RTCC\_TIME and RTCC\_DATE in calendar mode) and RTCC\_PRECNT, can at any time be written by software, as long as the registers are not locked using RTCC\_LOCKKEY. All RTCC registers use the immediate synchronization scheme, described in [4.3.1 Writing](#).

**Note:** Writing to the RTCC\_PRECNT register may alter the frequency of the ticks for the RTCC\_CNT register.

### 14.3.2 Capture/Compare Channels

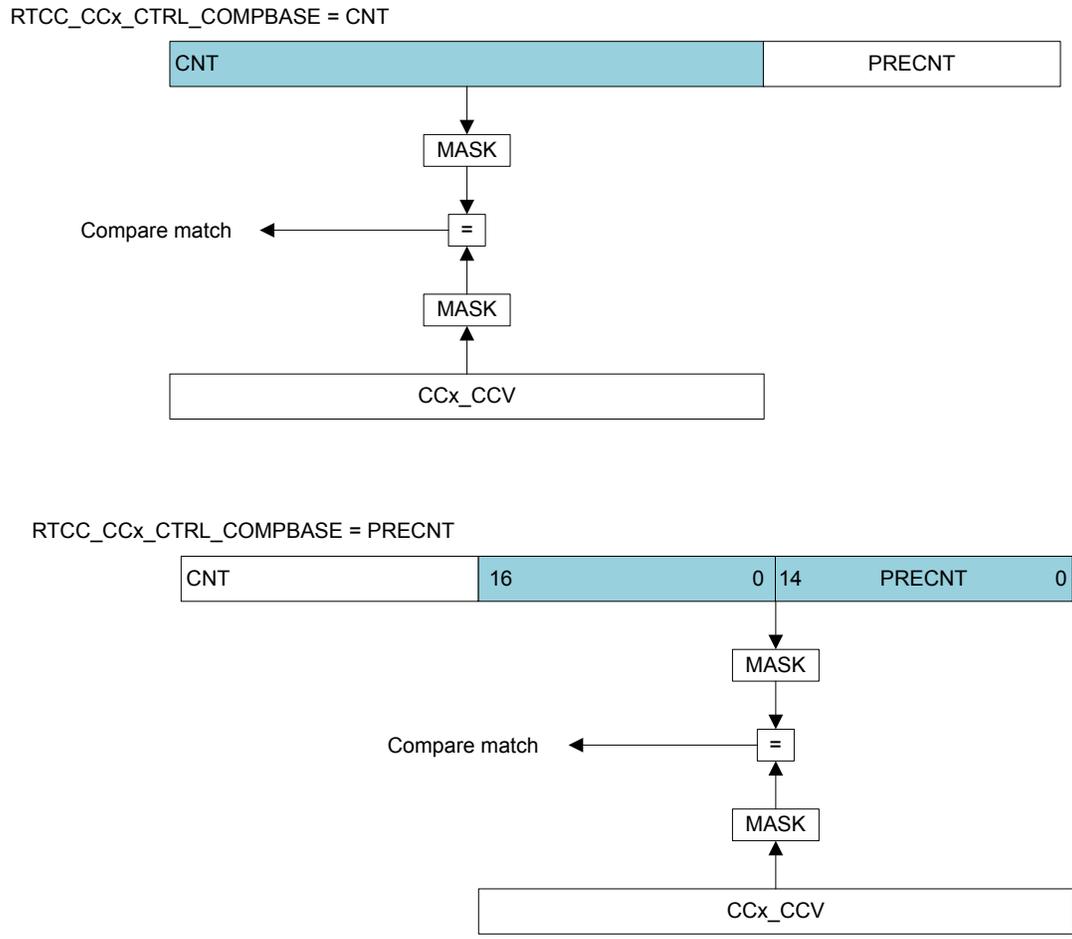
Three capture/compare channels are available in the RTCC. Each channel can be configured as input capture or output compare, by setting the corresponding MODE in the RTCC\_CCx\_CTRL register.



**Figure 14.3. RTCC Compare match and PRS output illustration**

In input capture mode the RTCC\_CNT (RTCC\_TIME and RTCC\_DATE in calendar mode) register is captured into the RTCC\_CCx\_CCv (RTCC\_CCx\_TIME and RTCC\_CCx\_DATE in calendar mode) register when an edge is detected on the selected PRS input channel. The active capture edge is configured in the ICEDGE control bits.

In output compare mode the compare values are set by writing to the RTCC compare channel registers RTCC\_CCx\_CCv (RTCC\_CCx\_TIME and RTCC\_CCx\_DATE in calendar mode). These values will be compared to the main counter, RTCC\_CNT (RTCC\_TIME and RTCC\_DATE in calendar mode), or a mixture of the main counter and the pre-counter, as illustrated in [Figure 14.4 RTCC Compare base illustration on page 424](#). Compare base for the capture compare channels is set by configuring COMP-BASE in RTCC\_CCx\_CTRL.



**Figure 14.4. RTCC Compare base illustration**

Table 14.3 RTCC Capture/Compare Subjects on page 424 summarizes which registers being subject to comparison for different configurations of RTCC\_CTRL\_CNTMODE and RTCC\_CCx\_CTRL\_COMPBASE.

**Table 14.3. RTCC Capture/Compare Subjects**

| RTCC_CTRL_CNTMODE               | NORMAL  | CALENDAR  |
|---------------------------------|---|---|
| RTCC_CCx_CTRL_COMPBASE = CNT    | RTCC_CNT vs. RTCC_CCx_CCV                           | RTCC_TIME vs. RTCC_CCx_TIME and RTCC_DATE vs. RTCC_CCx_DATE |
| RTCC_CCx_CTRL_COMPBASE = PRECNT | {RTCC_CNT[16:0],RTCC_PRECNT[14:0]} vs. RTCC_CCx_CCV | RTCC_PRECNT vs. RTCC_CCx_CCV[14:0]                          |

Figure 14.5 RTCC Compare in calendar mode, COMPBASE = CNT on page 425 illustrates how the compare events are evaluated when in calendar mode with RTCC\_CCx\_CTRL\_COMPBASE = CNT. The SECU, SECT, MINU, MINT, HOURU, HOURS, MONTHU, and MONTHT bitfields in RTCC\_CCx\_TIME and RTCC\_CCx\_DATE are compared to the corresponding bitfields in RTCC\_DATE and RTCC\_TIME. The DAYU and DAYT bitfields in RTCC\_CCx\_DATE will be compared to {RTCC\_DATE\_DAYOMT, RTCC\_DATE\_DAYOMU} if DAYCC in RTCC\_CCx\_CTRL is set to MONTH. If DAYCC in RTCC\_CCx\_CTRL is set to WEEK, the DAYU and DAYT bitfields in RTCC\_CCx\_DATE will be compared to {0b000, RTCC\_DATE\_DAYOW}.

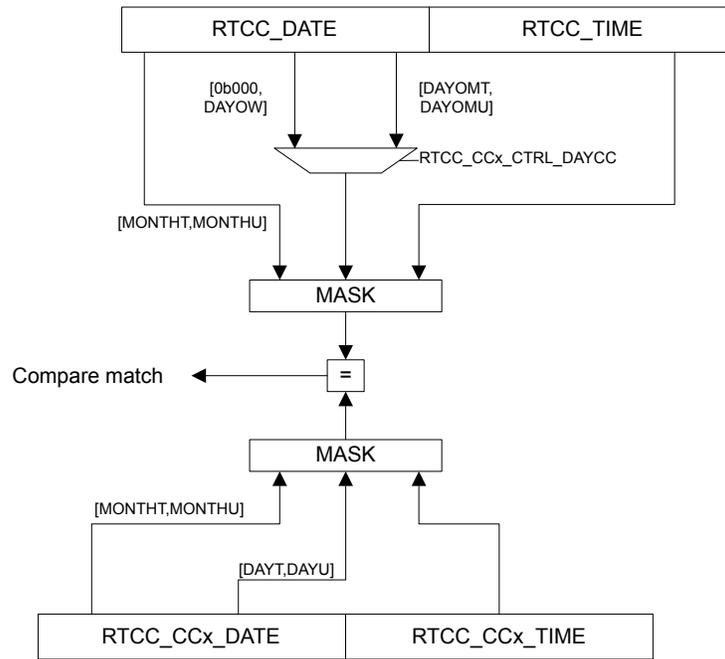


Figure 14.5. RTCC Compare in calendar mode, COMPBASE = CNT

To generate periodically recurring events, it is possible to mask out parts of the compare match values. By configuring COMPMASK in RTCC\_CCx\_CTRL, parts of the compare values will be masked out, limiting which part of the compare register being subject to comparison with the counter. Figure 14.6 RTCC Compare mask illustration, COMPMASK=11 on page 425 illustrates the effect of COMPMASK when in normal mode and calendar mode.

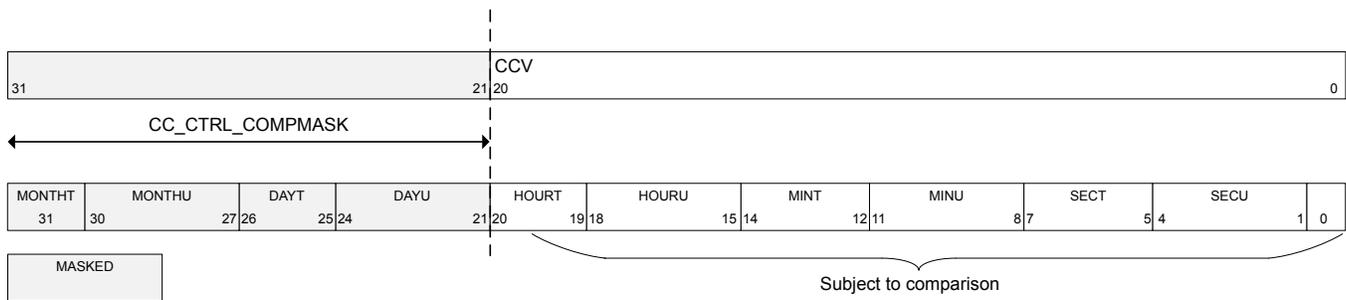


Figure 14.6. RTCC Compare mask illustration, COMPMASK=11

Upon a compare match, the respective Capture/Compare interrupt flag CCx is set. Additionally, the event selected by the CMOA setting is generated on the corresponding PRS output. This is illustrated in Figure 14.3 RTCC Compare match and PRS output illustration on page 423.

### 14.3.3 Interrupts and PRS Output

The RTCC has one interrupt for each of its 3 Capture/Compare channels, CC0, CC1, and CC2. Each Capture/Compare channel has a PRS output with configurable actions upon compare match.

The interrupt flag CNTTICK is set each time the main counter receives a tick (each second in calendar mode). In calendar mode, there are also interrupt flags being set each minute, hour, day, week, and month.

Upon oscillator failure detection, the OSCFAIL flag will be set.

### 14.3.3.1 Main Counter Tick PRS Output

To output the ticks for the main counter on PRS, it is possible to use a Capture/Compare channel and mask all the bits, i.e. `RTCC_CCx_CTRL_COMPBASE=CNT` and `RTCC_CCx_CTRL_COMPMASK=31`. PRS output of main counter ticks does not work if the main counter is not prescaled.

**Note:** To be able to mask all bits in the main counter, `RTCC_CTRL_CNTMODE` has to be set to `CALENDAR`. In `NORMAL` mode, the least significant bit can not be masked out.

### 14.3.4 Energy Mode Availability

The RTCC is available in all energy modes except EM4 Shutoff. To enable RTCC operation in EM4 Hibernate, the `EMU_EM4CTRL` register in the EMU has to be configured. Any enabled RTCC interrupt will wake the system up from EM4 Hibernate; if `EM4WU` in `RTCC_EM4WUEN` is set. Refer to [11. EMU - Energy Management Unit](#) for details on how to configure the EMU.

### 14.3.5 Register Lock

To prevent accidental writes to the RTCC registers, the `RTCC_LOCKKEY` register can be written to any value other than the unlock value. To unlock the register, write the unlock value to `RTCC_LOCKKEY`. Registers affected by this lock are:

- `RTCC_CTRL`
- `RTCC_PRECNT`
- `RTCC_CNT`
- `RTCC_TIME`
- `RTCC_DATE`
- `RTCC_IEN`
- `RTCC_POWERDOWN`
- `RTCC_CCx_CTRL`
- `RTCC_CCx_CCV`
- `RTCC_CCx_TIME`
- `RTCC_CCx_DATE`

### 14.3.6 Oscillator Failure Detection

To be able to detect OSC failure, the RTCC includes a security mechanism ensuring that at least three OSC cycles are detected within one period of the `ULFRCO`. If no OSC cycles are detected, the `OSCFAIL` interrupt flag is set. OSC failure detection is enabled by setting the `OSCFDETEN` bit in `RTCC_CTRL`.

### 14.3.7 Retention Registers

The RTCC includes 32 x 32 bit registers which can be retained in all energy modes except EM4 Shutoff. The registers are accessible through the `RETx_REG` registers. Retention is by default enabled in EM0 Active through EM4 Hibernate/Shutoff. The registers can be shut off to save power by setting the `RAM` bit in `RTCC_POWERDOWN`.

**Note:** The retention registers are mapped to a RAM instance and have undefined state out of reset.

### 14.3.8 Debug Session

By default, the RTCC is halted when code execution is halted from the debugger. By setting the `DEBUGRUN` bit in the `RTCC_CTRL` register, the RTCC will continue to run even when the debugger has halted the system.

## 14.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name                       | Type  | Description                                     |
|--------|----------------------------|-------|---|
| 0x000  | RTCC_CTRL                  | RW    | Control Register                                |
| 0x004  | RTCC_PRECNT                | RWH   | Pre-Counter Value Register                      |
| 0x008  | RTCC_CNT                   | RWH   | Counter Value Register                          |
| 0x00C  | RTCC_COMBCNT               | R     | Combined Pre-Counter and Counter Value Register |
| 0x010  | RTCC_TIME                  | RWH   | Time of Day Register                            |
| 0x014  | RTCC_DATE                  | RWH   | Date Register                                   |
| 0x018  | RTCC_IF                    | R     | RTCC Interrupt Flags                            |
| 0x01C  | RTCC_IFS                   | W1    | Interrupt Flag Set Register                     |
| 0x020  | RTCC_IFC                   | (R)W1 | Interrupt Flag Clear Register                   |
| 0x024  | RTCC_IEN                   | RW    | Interrupt Enable Register                       |
| 0x028  | RTCC_STATUS                | R     | Status Register                                 |
| 0x02C  | RTCC_CMD                   | W1    | Command Register                                |
| 0x030  | RTCC_SYNCBUSY              | R     | Synchronization Busy Register                   |
| 0x034  | RTCC_POWERDOWN             | RW    | Retention RAM Power-down Register               |
| 0x038  | RTCC_LOCK                  | RWH   | Configuration Lock Register                     |
| 0x03C  | RTCC_EM4WUEN               | RW    | Wake Up Enable                                  |
| 0x040  | RTCC_CC0_CTRL              | RW    | CC Channel Control Register                     |
| 0x044  | RTCC_CC0_CCV               | RWH   | Capture/Compare Value Register                  |
| 0x048  | RTCC_CC0_TIME              | RWH   | Capture/Compare Time Register                   |
| 0x04C  | RTCC_CC0_DATE              | RWH   | Capture/Compare Date Register                   |
| 0x050  | RTCC_CC1_CTRL              | RW    | CC Channel Control Register                     |
| 0x054  | RTCC_CC1_CCV               | RWH   | Capture/Compare Value Register                  |
| 0x058  | RTCC_CC1_TIME              | RWH   | Capture/Compare Time Register                   |
| 0x05C  | RTCC_CC1_DATE              | RWH   | Capture/Compare Date Register                   |
| 0x060  | RTCC_CC2_CTRL              | RW    | CC Channel Control Register                     |
| 0x064  | RTCC_CC2_CCV               | RWH   | Capture/Compare Value Register                  |
| 0x068  | RTCC_CC2_TIME              | RWH   | Capture/Compare Time Register                   |
| 0x06C  | RTCC_CC2_DATE              | RWH   | Capture/Compare Date Register                   |
| 0x104  | RTCC_RET0_REG              | RW    | Retention Register                              |
| ...    | RTCC_RET <sub>x</sub> _REG | RW    | Retention Register                              |
| 0x180  | RTCC_RET31_REG             | RW    | Retention Register                              |

## 14.5 Register Description

### 14.5.1 RTCC\_CTRL - Control Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |              |         |           |    |    |    |   |   |   |   |         |   |   |   |   |   |  |  |  |   |          |    |  |  |  |  |  |  |  |   |  |  |    |  |        |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------|---------|-----------|----|----|----|---|---|---|---|---------|---|---|---|---|---|--|--|--|---|----------|----|--|--|--|--|--|--|--|---|--|--|----|--|--------|
| 0x000         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15           | 14      | 13        | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5       | 4 | 3 | 2 | 1 | 0 |  |  |  |   |          |    |  |  |  |  |  |  |  |   |  |  |    |  |        |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0            | 0       | 0         |    |    | 0  |   |   |   |   | 0x0     |   |   |   | 0 | 0 |  |  |  | 0 |          |    |  |  |  |  |  |  |  | 0 |  |  |    |  |        |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW           | RW      | RW        |    |    |    |   |   |   |   | RW      |   |   |   |   |   |  |  |  |   | RW       | RW |  |  |  |  |  |  |  |   |  |  | RW |  |        |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LYEARCORRDIS | CNTMODE | OSCFDETEN |    |    |    |   |   |   |   | CNTTICK |   |   |   |   |   |  |  |  |   | CNTPRESC |    |  |  |  |  |  |  |  |   |  |  |    |  | ENABLE |

| Bit   | Name         | Reset  | Access | Description  |       |      |             |   |        |  |   |           |  |
|-------|--------------|--|--------|--|-------|------|-------------|---|--------|--|---|-----------|--|
| 31:18 | Reserved     | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |       |      |             |   |        |  |   |           |  |
| 17    | LYEARCORRDIS | 0  | RW     | <b>Leap Year Correction Disabled</b><br>When cleared, February has 29 days in leap years. When set, February always has 28 days.   |       |      |             |   |        |  |   |           |  |
| 16    | CNTMODE      | 0  | RW     | <b>Main Counter Mode</b><br>Configure count mode for the main counter.<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>NORMAL</td> <td>The main counter is incremented with 1 for each tick.</td> </tr> <tr> <td>1</td> <td>CALENDAR</td> <td>The main counter is in calendar mode.</td> </tr> </tbody> </table>   | Value | Mode | Description | 0 | NORMAL | The main counter is incremented with 1 for each tick.      | 1 | CALENDAR  | The main counter is in calendar mode.                      |
| Value | Mode         | Description  |        |  |       |      |             |   |        |  |   |           |  |
| 0     | NORMAL       | The main counter is incremented with 1 for each tick.  |        |  |       |      |             |   |        |  |   |           |  |
| 1     | CALENDAR     | The main counter is in calendar mode.  |        |  |       |      |             |   |        |  |   |           |  |
| 15    | OSCFDETEN    | 0  | RW     | <b>Oscillator Failure Detection Enable</b><br>When set, the OSCFAIL interrupt flag will be set if no ticks are detected on LFCLK <sub>RTCC</sub> within one ULFRCO cycle.  |       |      |             |   |        |  |   |           |  |
| 14:13 | Reserved     | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |       |      |             |   |        |  |   |           |  |
| 12    | CNTTICK      | 0  | RW     | <b>Counter Prescaler Mode</b><br>Select whether the main counter should tick on RTCC_CC0_CC0V[14:0] compare match with the pre-counter or tick on a pre-counter tap selected in CNTPRESC bitfield in the RTCC_CTRL register.<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>PRESC</td> <td>CNT register ticks according to configuration in CNTPRESC.</td> </tr> <tr> <td>1</td> <td>CCV0MATCH</td> <td>CNT register ticks when PRECNT matches RTCC_CC0_CC0V[14:0]</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | PRESC  | CNT register ticks according to configuration in CNTPRESC. | 1 | CCV0MATCH | CNT register ticks when PRECNT matches RTCC_CC0_CC0V[14:0] |
| Value | Mode         | Description  |        |  |       |      |             |   |        |  |   |           |  |
| 0     | PRESC        | CNT register ticks according to configuration in CNTPRESC.   |        |  |       |      |             |   |        |  |   |           |  |
| 1     | CCV0MATCH    | CNT register ticks when PRECNT matches RTCC_CC0_CC0V[14:0]   |        |  |       |      |             |   |        |  |   |           |  |
| 11:8  | CNTPRESC     | 0x0  | RW     | <b>Counter Prescaler Value</b><br>Configure counting frequency of the CNT register.<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>DIV1</td> <td>CLK<sub>CNT</sub> = LFECLK<sub>RTCC</sub>/1</td> </tr> <tr> <td>1</td> <td>DIV2</td> <td>CLK<sub>CNT</sub> = LFECLK<sub>RTCC</sub>/2</td> </tr> </tbody> </table>  | Value | Mode | Description | 0 | DIV1   | CLK <sub>CNT</sub> = LFECLK <sub>RTCC</sub> /1             | 1 | DIV2      | CLK <sub>CNT</sub> = LFECLK <sub>RTCC</sub> /2             |
| Value | Mode         | Description  |        |  |       |      |             |   |        |  |   |           |  |
| 0     | DIV1         | CLK <sub>CNT</sub> = LFECLK <sub>RTCC</sub> /1   |        |  |       |      |             |   |        |  |   |           |  |
| 1     | DIV2         | CLK <sub>CNT</sub> = LFECLK <sub>RTCC</sub> /2   |        |  |       |      |             |   |        |  |   |           |  |

| Bit | Name       | Reset   | Access | Description   |
|-----|------------|---|--------|---|
| 2   |            | DIV4  |        | $CLK_{CNT} = LFECLK_{RTCC}/4$   |
| 3   |            | DIV8  |        | $CLK_{CNT} = LFECLK_{RTCC}/8$   |
| 4   |            | DIV16   |        | $CLK_{CNT} = LFECLK_{RTCC}/16$  |
| 5   |            | DIV32   |        | $CLK_{CNT} = LFECLK_{RTCC}/32$  |
| 6   |            | DIV64   |        | $CLK_{CNT} = LFECLK_{RTCC}/64$  |
| 7   |            | DIV128  |        | $CLK_{CNT} = LFECLK_{RTCC}/128$   |
| 8   |            | DIV256  |        | $CLK_{CNT} = LFECLK_{RTCC}/256$   |
| 9   |            | DIV512  |        | $CLK_{CNT} = LFECLK_{RTCC}/512$   |
| 10  |            | DIV1024   |        | $CLK_{CNT} = LFECLK_{RTCC}/1024$  |
| 11  |            | DIV2048   |        | $CLK_{CNT} = LFECLK_{RTCC}/2048$  |
| 12  |            | DIV4096   |        | $CLK_{CNT} = LFECLK_{RTCC}/4096$  |
| 13  |            | DIV8192   |        | $CLK_{CNT} = LFECLK_{RTCC}/8192$  |
| 14  |            | DIV16384  |        | $CLK_{CNT} = LFECLK_{RTCC}/16384$   |
| 15  |            | DIV32768  |        | $CLK_{CNT} = LFECLK_{RTCC}/32768$   |
| 7:6 | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 5   | CCV1TOP    | 0   | RW     | <b>CCV1 Top Value Enable</b><br>When set, the counter wraps around on a CC1 event.  |
| 4   | PRECCV0TOP | 0   | RW     | <b>Pre-counter CCV0 Top Value Enable</b><br>When set, the pre-counter wraps around when PRECNT equals RTCC_CC0_CCV[14:0]. |
| 3   | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 2   | DEBUGRUN   | 0   | RW     | <b>Debug Mode Run Enable</b><br>Set this bit to keep the RTCC running during a debug halt.                                |
|     | Value      | Description   |        |   |
|     | 0          | RTCC is frozen in debug mode  |        |   |
|     | 1          | RTCC is running in debug mode   |        |   |
| 1   | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 0   | ENABLE     | 0   | RW     | <b>RTCC Enable</b><br>Enable the RTCC.  |

### 14.5.2 RTCC\_PRECNT - Pre-Counter Value Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x004         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PRECNT |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description  |
|-------|----------|--|--------|--|
| 31:15 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 14:0  | PRECNT   | 0x0000   | RWH    | <b>Pre-Counter Value</b><br>Gives access to the Pre-counter value of the RTCC. |

### 14.5.3 RTCC\_CNT - Counter Value Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x008         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CNT        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name | Reset      | Access | Description   |
|------|------|------------|--------|---|
| 31:0 | CNT  | 0x00000000 | RWH    | <b>Counter Value</b><br>Gives access to the main counter value of the RTCC. Register can not be written and will be read as zero when RTCC_CTRL_CNTMODE = CALENDAR. |

14.5.4 RTCC\_COMBCNT - Combined Pre-Counter and Counter Value Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x00C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14     | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0x00000      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000 |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> | R            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R      |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | CNTLSB       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PRECNT |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name   | Reset   | Access | Description  |
|-------|--------|---------|--------|--|
| 31:15 | CNTLSB | 0x00000 | R      | <b>Counter Value</b><br>Gives access to the 17 LSBs of the main counter, CNT. Register will be read as zero when RTCC_CTRL_CNTMODE = CALENDAR. |
| 14:0  | PRECNT | 0x0000  | R      | <b>Pre-Counter Value</b><br>Gives access to the pre-counter, PRECNT. Register will be read as zero when RTCC_CTRL_CNTMODE = CALENDAR.          |

### 14.5.5 RTCC\_TIME - Time of Day Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |       |       |    |    |    |    |    |      |    |    |    |   |   |      |   |   |   |   |   |      |   |  |  |  |  |      |  |  |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|-------|-------|----|----|----|----|----|------|----|----|----|---|---|------|---|---|---|---|---|------|---|--|--|--|--|------|--|--|--|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20    | 19    | 18 | 17 | 16 | 15 | 14 | 13   | 12 | 11 | 10 | 9 | 8 | 7    | 6 | 5 | 4 | 3 | 2 | 1    | 0 |  |  |  |  |      |  |  |  |  |
| 0x010         |              |    |    |    |    |    |    |    |    |    |    |       |       |    |    |    |    |    |      |    |    |    |   |   |      |   |   |   |   |   |      |   |  |  |  |  |      |  |  |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    | 0x0   | 0x0   |    |    |    |    |    | 0x0  |    |    |    |   |   | 0x0  |   |   |   |   |   |      |   |  |  |  |  |      |  |  |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    | RWH   | RWH   |    |    |    |    |    | RWH  |    |    |    |   |   | RWH  |   |   |   |   |   |      |   |  |  |  |  |      |  |  |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    | HOURT | HOURU |    |    |    |    |    | MINT |    |    |    |   |   | MINU |   |   |   |   |   | SECT |   |  |  |  |  | SECU |  |  |  |  |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:22 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 21:20 | HOURT           | 0x0   | RWH    | <b>Hours, Tens</b><br><br>Shows the tens part of the hour counter. Register can not be written and will be read as zero when RTCC_CTRL_CNTMODE = NORMAL.      |
| 19:16 | HOURU           | 0x0   | RWH    | <b>Hours, Units</b><br><br>Shows the unit part of the hour counter. Register can not be written and will be read as zero when RTCC_CTRL_CNTMODE = NORMAL.     |
| 15    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 14:12 | MINT            | 0x0   | RWH    | <b>Minutes, Tens</b><br><br>Shows the tens part of the minute counter. Register can not be written and will be read as zero when RTCC_CTRL_CNTMODE = NORMAL.  |
| 11:8  | MINU            | 0x0   | RWH    | <b>Minutes, Units</b><br><br>Shows the unit part of the minute counter. Register can not be written and will be read as zero when RTCC_CTRL_CNTMODE = NORMAL. |
| 7     | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 6:4   | SECT            | 0x0   | RWH    | <b>Seconds, Tens</b><br><br>Shows the tens part of the second counter. Register can not be written and will be read as zero when RTCC_CTRL_CNTMODE = NORMAL.  |
| 3:0   | SECU            | 0x0   | RWH    | <b>Seconds, Units</b><br><br>Shows the unit part of the second counter. Register can not be written and will be read as zero when RTCC_CTRL_CNTMODE = NORMAL. |

### 14.5.6 RTCC\_DATE - Date Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |       |    |    |    |       |    |    |    |    |       |    |    |    |    |        |    |    |   |        |   |   |   |        |   |   |        |   |  |
|---------------|--------------|----|----|----|----|-------|----|----|----|-------|----|----|----|----|-------|----|----|----|----|--------|----|----|---|--------|---|---|---|--------|---|---|--------|---|--|
|               | 31           | 30 | 29 | 28 | 27 | 26    | 25 | 24 | 23 | 22    | 21 | 20 | 19 | 18 | 17    | 16 | 15 | 14 | 13 | 12     | 11 | 10 | 9 | 8      | 7 | 6 | 5 | 4      | 3 | 2 | 1      | 0 |  |
| 0x014         |              |    |    |    |    |       |    |    |    |       |    |    |    |    |       |    |    |    |    |        |    |    |   |        |   |   |   |        |   |   |        |   |  |
| <b>Reset</b>  |              |    |    |    |    | 0x0   |    |    |    | 0x0   |    |    |    |    | 0x0   |    |    |    |    | 0      |    |    |   | 0x0    |   |   |   | 0x0    |   |   | 0x0    |   |  |
| <b>Access</b> |              |    |    |    |    | RWH   |    |    |    | RWH   |    |    |    |    | RWH   |    |    |    |    | RWH    |    |    |   | RWH    |   |   |   | RWH    |   |   | RWH    |   |  |
| <b>Name</b>   |              |    |    |    |    | DAYOW |    |    |    | YEART |    |    |    |    | YEARU |    |    |    |    | MONTHT |    |    |   | MONTHU |   |   |   | DAYOMT |   |   | DAYOMU |   |  |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 31:27 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 26:24 | DAYOW           | 0x0   | RWH    | <b>Day of Week</b><br>Shows the day of week counter. Register can not be written and will be read as zero when RTCC_CTRL_CNTMODE = NORMAL.                           |
| 23:20 | YEART           | 0x0   | RWH    | <b>Year, Tens</b><br>Shows the tens part of the year counter. Register can not be written and will be read as zero when RTCC_CTRL_CNTMODE = NORMAL.                  |
| 19:16 | YEARU           | 0x0   | RWH    | <b>Year, Units</b><br>Shows the unit part of the year counter. Register can not be written and will be read as zero when RTCC_CTRL_CNTMODE = NORMAL.                 |
| 15:13 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 12    | MONTHT          | 0   | RWH    | <b>Month, Tens</b><br>Shows the tens part of the month counter. Register can not be written and will be read as zero when RTCC_CTRL_CNTMODE = NORMAL.                |
| 11:8  | MONTHU          | 0x0   | RWH    | <b>Month, Units</b><br>Shows the unit part of the month counter. Register can not be written and will be read as zero when RTCC_CTRL_CNTMODE = NORMAL.               |
| 7:6   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 5:4   | DAYOMT          | 0x0   | RWH    | <b>Day of Month, Tens</b><br>Shows the tens part of the day of month counter. Register can not be written and will be read as zero when RTCC_CTRL_CNTMODE = NORMAL.  |
| 3:0   | DAYOMU          | 0x0   | RWH    | <b>Day of Month, Units</b><br>Shows the unit part of the day of month counter. Register can not be written and will be read as zero when RTCC_CTRL_CNTMODE = NORMAL. |





## 14.5.9 RTCC\_IFC - Interrupt Flag Clear Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |           |         |         |          |         |         |         |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------|---------|---------|----------|---------|---------|---------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|--|
| 0x020         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11        | 10      | 9       | 8        | 7       | 6       | 5       | 4     | 3     | 2     | 1     | 0     |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0         | 0       | 0       | 0        | 0       | 0       | 0       | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | (R)W1     | (R)W1   | (R)W1   | (R)W1    | (R)W1   | (R)W1   | (R)W1   | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MONTHTICK | DAYOWOF | DAYTICK | HOURTICK | MINTICK | CNTTICK | OSCFAIL | CC2   | CC1   | CC0   | OF    |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |  |

| Bit   | Name      | Reset  | Access | Description   |
|-------|-----------|--|--------|---|
| 31:11 | Reserved  | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 10    | MONTHTICK | 0  | (R)W1  | <b>Clear MONTHTICK Interrupt Flag</b><br><br>Write 1 to clear the MONTHTICK interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 9     | DAYOWOF   | 0  | (R)W1  | <b>Clear DAYOWOF Interrupt Flag</b><br><br>Write 1 to clear the DAYOWOF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 8     | DAYTICK   | 0  | (R)W1  | <b>Clear DAYTICK Interrupt Flag</b><br><br>Write 1 to clear the DAYTICK interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 7     | HOURTICK  | 0  | (R)W1  | <b>Clear HOURTICK Interrupt Flag</b><br><br>Write 1 to clear the HOURTICK interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |
| 6     | MINTICK   | 0  | (R)W1  | <b>Clear MINTICK Interrupt Flag</b><br><br>Write 1 to clear the MINTICK interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 5     | CNTTICK   | 0  | (R)W1  | <b>Clear CNTTICK Interrupt Flag</b><br><br>Write 1 to clear the CNTTICK interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 4     | OSCFAIL   | 0  | (R)W1  | <b>Clear OSCFAIL Interrupt Flag</b><br><br>Write 1 to clear the OSCFAIL interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 3     | CC2       | 0  | (R)W1  | <b>Clear CC2 Interrupt Flag</b><br><br>Write 1 to clear the CC2 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).             |
| 2     | CC1       | 0  | (R)W1  | <b>Clear CC1 Interrupt Flag</b><br><br>Write 1 to clear the CC1 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).             |
| 1     | CC0       | 0  | (R)W1  | <b>Clear CC0 Interrupt Flag</b><br><br>Write 1 to clear the CC0 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).             |

| Bit  | Name | Reset | Access | Description                    |
|--|------|-------|--------|--------------------------------|
| 0  | OF   | 0     | (R)W1  | <b>Clear OF Interrupt Flag</b> |
| Write 1 to clear the OF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.) |      |       |        |                                |

#### 14.5.10 RTCC\_IEN - Interrupt Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |           |         |         |          |         |         |         |     |     |     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------|---------|---------|----------|---------|---------|---------|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0x024         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11        | 10      | 9       | 8        | 7       | 6       | 5       | 4   | 3   | 2   | 1  | 0  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0         | 0       | 0       | 0        | 0       | 0       | 0       | 0   | 0   | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW        | RW      | RW      | RW       | RW      | RW      | RW      | RW  | RW  | RW  | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MONTHTICK | DAYOWOF | DAYTICK | HOURTICK | MINTICK | CNTTICK | OSCFAIL | CC2 | CC1 | CC0 | OF |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:11 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 10    | MONTHTICK       | 0   | RW     | <b>MONTHTICK Interrupt Enable</b><br>Enable/disable the MONTHTICK interrupt |
| 9     | DAYOWOF         | 0   | RW     | <b>DAYOWOF Interrupt Enable</b><br>Enable/disable the DAYOWOF interrupt     |
| 8     | DAYTICK         | 0   | RW     | <b>DAYTICK Interrupt Enable</b><br>Enable/disable the DAYTICK interrupt     |
| 7     | HOURTICK        | 0   | RW     | <b>HOURTICK Interrupt Enable</b><br>Enable/disable the HOURTICK interrupt   |
| 6     | MINTICK         | 0   | RW     | <b>MINTICK Interrupt Enable</b><br>Enable/disable the MINTICK interrupt     |
| 5     | CNTTICK         | 0   | RW     | <b>CNTTICK Interrupt Enable</b><br>Enable/disable the CNTTICK interrupt     |
| 4     | OSCFAIL         | 0   | RW     | <b>OSCFAIL Interrupt Enable</b><br>Enable/disable the OSCFAIL interrupt     |
| 3     | CC2             | 0   | RW     | <b>CC2 Interrupt Enable</b><br>Enable/disable the CC2 interrupt             |
| 2     | CC1             | 0   | RW     | <b>CC1 Interrupt Enable</b><br>Enable/disable the CC1 interrupt             |
| 1     | CC0             | 0   | RW     | <b>CC0 Interrupt Enable</b><br>Enable/disable the CC0 interrupt             |
| 0     | OF              | 0   | RW     | <b>OF Interrupt Enable</b><br>Enable/disable the OF interrupt               |

### 14.5.11 RTCC\_STATUS - Status Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x028         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description |
|------|----------|--|--------|-------------|
| 31:0 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |             |

### 14.5.12 RTCC\_CMD - Command Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x02C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description |
|------|----------|--|--------|-------------|
| 31:1 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |             |

|   |           |   |    |   |
|---|-----------|---|----|---|
| 0 | CLRSTATUS | 0 | W1 | <b>Clear RTCC_STATUS Register</b><br>Write a 1 to clear the RTCC_STATUS register. |
|---|-----------|---|----|---|

### 14.5.13 RTCC\_SYNCBUSY - Synchronization Busy Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x030         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description |
|------|----------|--|--------|-------------|
| 31:6 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |             |

|   |     |   |   |  |
|---|-----|---|---|--|
| 5 | CMD | 0 | R | <b>CMD Register Busy</b><br>Set when the value written to CMD is being synchronized. |
|---|-----|---|---|--|

|     |          |  |  |  |
|-----|----------|--|--|--|
| 4:0 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |  |  |
|-----|----------|--|--|--|

#### 14.5.14 RTCC\_POWERDOWN - Retention RAM Power-down Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |     |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-----|--|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0   |  |  |
| 0x034         |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |     |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0   |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | RW  |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | RAM |  |  |

| Bit  | Name     | Reset   | Access | Description  |
|------|----------|---|--------|--|
| 31:1 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 0    | RAM      | 0   | RW     | <b>Retention RAM Power-down</b><br>Shut off power to the Retention RAM. Once it is powered down, it cannot be powered up again |

#### 14.5.15 RTCC\_LOCK - Configuration Lock Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16      | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| 0x038         |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH     |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LOCKKEY |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |

| Bit   | Name     | Reset   | Access | Description   |
|-------|----------|---|--------|---|
| 31:16 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 15:0  | LOCKKEY  | 0x0000  | RWH    | <b>Configuration Lock Key</b><br>Write any other value than the unlock code to lock RTCC_CTRL, RTCC_PRECNT, RTCC_CNT, RTCC_TIME, RTCC_DATE, RTCC_IEN, RTCC_POWERDOWN, and RTCC_CCx_XXX registers from editing. Write the unlock code to unlock. When reading the register, bit 0 is set when the lock is enabled. |

| Mode            | Value  | Description                |
|-----------------|--------|----------------------------|
| Read Operation  |        |                            |
| UNLOCKED        | 0      | All registers are unlocked |
| LOCKED          | 1      | Registers are locked       |
| Write Operation |        |                            |
| LOCK            | 0      | Lock registers             |
| UNLOCK          | 0xAEE8 | Unlock all RTCC registers  |

14.5.16 RTCC\_EM4WUEN - Wake Up Enable

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------|
| 0x03C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0     |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0     |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | RW    |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | EM4WU |

| Bit  | Name     | Reset   | Access | Description   |
|------|----------|---|--------|---|
| 31:1 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 0    | EM4WU    | 0   | RW     | <b>EM4 Wake-up Enable</b><br>Write 1 to enable wake-up request, write 0 to disable wake-up request. |

### 14.5.17 RTCC\_CCx\_CTRL - CC Channel Control Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |       |          |    |    |    |    |    |          |   |       |   |   |   |   |        |      |      |     |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|----------|----|----|----|----|----|----------|---|-------|---|---|---|---|--------|------|------|-----|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17    | 16       | 15 | 14 | 13 | 12 | 11 | 10       | 9 | 8     | 7 | 6 | 5 | 4 | 3      | 2    | 1    | 0   |  |
| 0x040         |              |    |    |    |    |    |    |    |    |    |    |    |    |    |       |          |    |    |    |    |    |          |   |       |   |   |   |   |        |      |      |     |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    | 0     | 0x00     |    |    |    |    |    | 0        |   | 0x0   |   |   |   |   | 0x0    | 0x0  | 0x0  | 0x0 |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    | RW    | RW       |    |    |    |    |    | RW       |   | RW    |   |   |   |   | RW     | RW   | RW   | RW  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    | DAYCC | COMPMASK |    |    |    |    |    | COMPBASE |   | PRSEL |   |   |   |   | ICEDGE | CMOA | MODE |     |  |

| Bit   | Name            | Reset   | Access | Description   |       |      |             |   |        |   |   |        |  |   |        |                                 |   |        |                                 |   |        |                                 |   |        |                                 |
|-------|-----------------|---|--------|---|-------|------|-------------|---|--------|---|---|--------|--|---|--------|---------------------------------|---|--------|---------------------------------|---|--------|---------------------------------|---|--------|---------------------------------|
| 31:18 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |      |             |   |        |   |   |        |  |   |        |                                 |   |        |                                 |   |        |                                 |   |        |                                 |
| 17    | DAYCC           | 0   | RW     | <b>Day Capture/Compare Selection</b><br>Select whether day of week, or day of month is subject for Capture/Compare.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>MONTH</td> <td>Day of month is selected for Capture/Compare.</td> </tr> <tr> <td>1</td> <td>WEEK</td> <td>Day of week is selected for Capture/Compare.</td> </tr> </tbody> </table>   | Value | Mode | Description | 0 | MONTH  | Day of month is selected for Capture/Compare.   | 1 | WEEK   | Day of week is selected for Capture/Compare.                     |   |        |                                 |   |        |                                 |   |        |                                 |   |        |                                 |
| Value | Mode            | Description   |        |   |       |      |             |   |        |   |   |        |  |   |        |                                 |   |        |                                 |   |        |                                 |   |        |                                 |
| 0     | MONTH           | Day of month is selected for Capture/Compare.   |        |   |       |      |             |   |        |   |   |        |  |   |        |                                 |   |        |                                 |   |        |                                 |   |        |                                 |
| 1     | WEEK            | Day of week is selected for Capture/Compare.  |        |   |       |      |             |   |        |   |   |        |  |   |        |                                 |   |        |                                 |   |        |                                 |   |        |                                 |
| 16:12 | COMPMASK        | 0x00  | RW     | <b>Capture Compare Channel Comparison Mask</b><br>The COMPMASK most significant bits of the compare value will not be subject to comparison.  |       |      |             |   |        |   |   |        |  |   |        |                                 |   |        |                                 |   |        |                                 |   |        |                                 |
| 11    | COMPBASE        | 0   | RW     | <b>Capture Compare Channel Comparison Base</b><br>Configure comparison base for compare channel<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>CNT</td> <td>RTCC_CCx_CCV is compared with RTCC_CNT register. RTCC_CCx_TIME/DATE compare with RTCC_TIME/DATE in calendar mode.</td> </tr> <tr> <td>1</td> <td>PRECNT</td> <td>Least significant bits of RTCC_CCx_CCV are compared with PRECNT.</td> </tr> </tbody> </table>   | Value | Mode | Description | 0 | CNT    | RTCC_CCx_CCV is compared with RTCC_CNT register. RTCC_CCx_TIME/DATE compare with RTCC_TIME/DATE in calendar mode. | 1 | PRECNT | Least significant bits of RTCC_CCx_CCV are compared with PRECNT. |   |        |                                 |   |        |                                 |   |        |                                 |   |        |                                 |
| Value | Mode            | Description   |        |   |       |      |             |   |        |   |   |        |  |   |        |                                 |   |        |                                 |   |        |                                 |   |        |                                 |
| 0     | CNT             | RTCC_CCx_CCV is compared with RTCC_CNT register. RTCC_CCx_TIME/DATE compare with RTCC_TIME/DATE in calendar mode.               |        |   |       |      |             |   |        |   |   |        |  |   |        |                                 |   |        |                                 |   |        |                                 |   |        |                                 |
| 1     | PRECNT          | Least significant bits of RTCC_CCx_CCV are compared with PRECNT.  |        |   |       |      |             |   |        |   |   |        |  |   |        |                                 |   |        |                                 |   |        |                                 |   |        |                                 |
| 10    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |      |             |   |        |   |   |        |  |   |        |                                 |   |        |                                 |   |        |                                 |   |        |                                 |
| 9:6   | PRSEL           | 0x0   | RW     | <b>Compare/Capture Channel PRS Input Channel Selection</b><br>Select PRS input channel for Compare/Capture channel.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>PRSCH0</td> <td>PRS Channel 0 selected as input</td> </tr> <tr> <td>1</td> <td>PRSCH1</td> <td>PRS Channel 1 selected as input</td> </tr> <tr> <td>2</td> <td>PRSCH2</td> <td>PRS Channel 2 selected as input</td> </tr> <tr> <td>3</td> <td>PRSCH3</td> <td>PRS Channel 3 selected as input</td> </tr> <tr> <td>4</td> <td>PRSCH4</td> <td>PRS Channel 4 selected as input</td> </tr> <tr> <td>5</td> <td>PRSCH5</td> <td>PRS Channel 5 selected as input</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | PRSCH0 | PRS Channel 0 selected as input   | 1 | PRSCH1 | PRS Channel 1 selected as input                                  | 2 | PRSCH2 | PRS Channel 2 selected as input | 3 | PRSCH3 | PRS Channel 3 selected as input | 4 | PRSCH4 | PRS Channel 4 selected as input | 5 | PRSCH5 | PRS Channel 5 selected as input |
| Value | Mode            | Description   |        |   |       |      |             |   |        |   |   |        |  |   |        |                                 |   |        |                                 |   |        |                                 |   |        |                                 |
| 0     | PRSCH0          | PRS Channel 0 selected as input   |        |   |       |      |             |   |        |   |   |        |  |   |        |                                 |   |        |                                 |   |        |                                 |   |        |                                 |
| 1     | PRSCH1          | PRS Channel 1 selected as input   |        |   |       |      |             |   |        |   |   |        |  |   |        |                                 |   |        |                                 |   |        |                                 |   |        |                                 |
| 2     | PRSCH2          | PRS Channel 2 selected as input   |        |   |       |      |             |   |        |   |   |        |  |   |        |                                 |   |        |                                 |   |        |                                 |   |        |                                 |
| 3     | PRSCH3          | PRS Channel 3 selected as input   |        |   |       |      |             |   |        |   |   |        |  |   |        |                                 |   |        |                                 |   |        |                                 |   |        |                                 |
| 4     | PRSCH4          | PRS Channel 4 selected as input   |        |   |       |      |             |   |        |   |   |        |  |   |        |                                 |   |        |                                 |   |        |                                 |   |        |                                 |
| 5     | PRSCH5          | PRS Channel 5 selected as input   |        |   |       |      |             |   |        |   |   |        |  |   |        |                                 |   |        |                                 |   |        |                                 |   |        |                                 |

| Bit | Name  | Reset         | Access  | Description                        |
|-----|---|---------------|---|------------------------------------|
|     | 6   | PRSCH6        |   | PRS Channel 6 selected as input    |
|     | 7   | PRSCH7        |   | PRS Channel 7 selected as input    |
|     | 8   | PRSCH8        |   | PRS Channel 8 selected as input    |
|     | 9   | PRSCH9        |   | PRS Channel 9 selected as input    |
|     | 10  | PRSCH10       |   | PRS Channel 10 selected as input   |
|     | 11  | PRSCH11       |   | PRS Channel 11 selected as input   |
| 5:4 | ICEDGE  | 0x0           | RW  | <b>Input Capture Edge Select</b>   |
|     | These bits control which edges the PRS edge detector triggers on. |               |   |                                    |
|     | Value   | Mode          | Description                                       |                                    |
|     | 0   | RISING        | Rising edges detected                             |                                    |
|     | 1   | FALLING       | Falling edges detected                            |                                    |
|     | 2   | BOTH          | Both edges detected                               |                                    |
|     | 3   | NONE          | No edge detection, signal is left as it is        |                                    |
| 3:2 | CMOA  | 0x0           | RW  | <b>Compare Match Output Action</b> |
|     | Select output action on compare match.                            |               |   |                                    |
|     | Value   | Mode          | Description                                       |                                    |
|     | 0   | PULSE         | A single clock cycle pulse is generated on output |                                    |
|     | 1   | TOGGLE        | Toggle output on compare match                    |                                    |
|     | 2   | CLEAR         | Clear output on compare match                     |                                    |
|     | 3   | SET           | Set output on compare match                       |                                    |
| 1:0 | MODE  | 0x0           | RW  | <b>CC Channel Mode</b>             |
|     | These bits select the mode for Compare/Capture channel.           |               |   |                                    |
|     | Value   | Mode          | Description                                       |                                    |
|     | 0   | OFF           | Compare/Capture channel turned off                |                                    |
|     | 1   | INPUTCAPTURE  | Input capture                                     |                                    |
|     | 2   | OUTPUTCOMPARE | Output compare                                    |                                    |

### 14.5.18 RTCC\_CCx\_CCV - Capture/Compare Value Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x044         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CCV        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit  | Name | Reset      | Access | Description                  |
|--|------|------------|--------|------------------------------|
| 31:0   | CCV  | 0x00000000 | RWH    | <b>Capture/Compare Value</b> |
| Shows the Capture/Compare Value for the channel. Register can not be written and will be read as zero when RTCC_CTRL_CNTMODE = CALENDAR. |      |            |        |                              |



### 14.5.20 RTCC\_CCx\_DATE - Capture/Compare Date Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |   |   |        |   |   |   |     |   |   |   |      |  |  |  |      |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|---|---|--------|---|---|---|-----|---|---|---|------|--|--|--|------|
| 0x04C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11     | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3   | 2 | 1 | 0 |      |  |  |  |      |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0      |    |   |   | 0x0    |   |   |   | 0x0 |   |   |   | 0x0  |  |  |  | 0x0  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH    |    |   |   | RWH    |   |   |   |     |   |   |   | RWH  |  |  |  | RWH  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MONTHT |    |   |   | MONTHU |   |   |   |     |   |   |   | DAYT |  |  |  | DAYU |

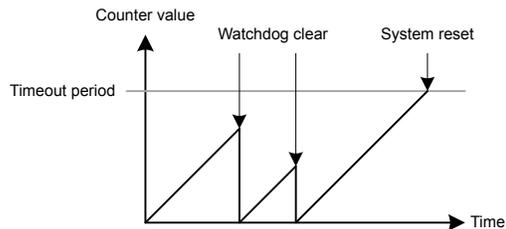
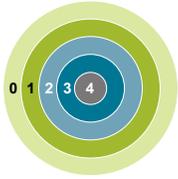
| Bit   | Name     | Reset   | Access | Description   |
|-------|----------|---|--------|---|
| 31:13 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 12    | MONTHT   | 0   | RWH    | <b>Month, Tens</b><br>Shows the tens part of the Capture/Compare value for months. Register can not be written and will be read as zero when RTCC_CTRL_CNTMODE = NORMAL.            |
| 11:8  | MONTHU   | 0x0   | RWH    | <b>Month, Units</b><br>Shows the unit part of the Capture/Compare value for months. Register can not be written and will be read as zero when RTCC_CTRL_CNTMODE = NORMAL.           |
| 7:6   | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 5:4   | DAYT     | 0x0   | RWH    | <b>Day of Month/week, Tens</b><br>Shows the tens part of the Capture/Compare value for days. Register can not be written and will be read as zero when RTCC_CTRL_CNTMODE = NORMAL.  |
| 3:0   | DAYU     | 0x0   | RWH    | <b>Day of Month/week, Units</b><br>Shows the unit part of the Capture/Compare value for days. Register can not be written and will be read as zero when RTCC_CTRL_CNTMODE = NORMAL. |

### 14.5.21 RTCC\_RETx\_REG - Retention Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |           |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x104         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0XXXXXXXX |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | REG       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name | Reset          | Access | Description                               |
|------|------|----------------|--------|---|
| 31:0 | REG  | 0XXXXXXXX<br>X | RW     | <b>General Purpose Retention Register</b> |

## 15. WDOG - Watchdog Timer



### Quick Facts

#### What?

The Watchdog Timer (WDOG) resets the system in case of a fault condition, and can be enabled in all energy modes as long as the low frequency clock source is available.

#### Why?

If a software failure or external event renders the MCU unresponsive, a Watchdog timeout will reset the system to a known, safe state.

#### How?

An enabled Watchdog Timer implements a configurable timeout period. If the CPU fails to re-start the Watchdog Timer before it times out, a full system reset will be triggered. The Watchdog consumes insignificant power, and allows the device to remain safely in low energy modes for up to 256 seconds at a time.

### 15.1 Introduction

The purpose of the watchdog timer is to generate a reset in case of a system failure to increase application reliability. The failure can be caused by a variety of events, such as an ESD pulse or a software failure.

### 15.2 Features

- Clock input from selectable oscillators
  - Internal 32 kHz LFRCO oscillator
  - Internal 1 kHz ULFRCO oscillator
  - External 32.768 kHz LFXO XTAL oscillator
  - HFCORECLK
- Configurable timeout period from 9 to 256k watchdog clock cycles
- Individual selection to keep running or freeze when entering EM2 Deep Sleep or EM3 Stop
- Selection to keep running or freeze when entering debug mode
- Selection to block the CPU from entering Energy Mode 4
- Selection to block the CMU from disabling the selected watchdog clock
- Configurable warning interrupt at 25%,50%, or 75% of the timeout period
- Configurable window interrupt at 12.5%,25%,37.5%,50%,62.5%,75%,87.5% of the timeout period
- Timeout interrupt
- PRS as a watchdog clear
- Interrupt for the event where a PRS rising edge is absent before a software reset

### 15.3 Functional Description

The watchdog is enabled by setting the EN bit in WDOGn\_CTRL. When enabled, the watchdog counts up to the period value configured through the PERSEL field in WDOGn\_CTRL. If the watchdog timer is not cleared to 0 (by writing a 1 to the CLEAR bit in WDOGn\_CMD) before the period is reached, the chip is reset. If a timely clear command is issued, the timer starts counting up from 0 again. The watchdog can optionally be locked by writing the LOCK bit in WDOGn\_CTRL. Once locked, it cannot be disabled or reconfigured by software.

When the EN bit in WDOGn\_CTRL is cleared to 0, the watchdog counter is reset.

### 15.3.1 Clock Source

Three clock sources are available for use with the watchdog, through the CLKSEL field in WDOGn\_CTRL. The corresponding clocks must be enabled in the CMU. The SWOSCBLOCK bit in WDOGn\_CTRL can be written to prevent accidental disabling of the selected clocks. Also, setting this bit will automatically start the selected oscillator source when the watchdog is enabled. The PERSEL field in WDOGn\_CTRL is used to divide the selected watchdog clock, and the timeout for the watchdog timer can be calculated with the formula:

$$T_{\text{TIMEOUT}} = (2^{3+\text{PERSEL}} + 1) / f$$

where  $f$  is the frequency of the selected clock.

When the watchdog is enabled, it is recommended to clear the watchdog before changing PERSEL.

To use this module, the LE interface clock must be enabled in CMU\_HFBUSCLKEN0.

### 15.3.2 Debug Functionality

The watchdog timer can either keep running or be frozen when the device is halted by a debugger. This configuration is done through the DEBUGRUN bit in WDOGn\_CTRL. When code execution is resumed, the watchdog will continue counting where it left off.

### 15.3.3 Energy Mode Handling

The watchdog timer can be configured to either keep on running or freeze when entering EM2 Deep Sleep or EM3 Stop. The configuration is done individually for each energy mode in the EM2RUN and EM3RUN bits in WDOGn\_CTRL. When the watchdog has been frozen and is re-entering an energy mode where it is running, the watchdog timer will continue counting where it left off. For the watchdog there is no difference between EM0 Active and EM1 Sleep. The watchdog does not run in EM4 Hibernate/Shutoff. If EM4BLOCK in WDOGn\_CTRL is set, the CPU will be prevented from entering EM4 Hibernate/Shutoff by software request.

**Note:**

If the WDOG is clocked by the LFXO or LFRCO, writing the SWOSCBLOCK bit will prevent the CPU from entering EM3 Stop. When running from the ULFRCO, writing the SWOSCBLOCK bit will prevent the CPU from entering EM4 Hibernate/Shutoff.

### 15.3.4 Register Access

Since this module is a Low Energy Peripheral, and runs off a clock which is asynchronous to the HFCORECLK, special considerations must be taken when accessing registers. Refer to [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#) for a description on how to perform register accesses to Low Energy Peripherals. Note that clearing the EN bit in WDOGn\_CTRL will reset the WDOG module, which will halt any ongoing register synchronization.

**Note:**

Never write to the WDOG registers when it is disabled, except to enable the watchdog by setting the EN bitfield in WDOGn\_CTRL.

### 15.3.5 Warning Interrupt

The watchdog implements a warning interrupt which can be configured to occur at approximately 25%, 50%, or 75% of the timeout period through the WARNSEL field of the WDOGn\_CTRL register. This interrupt can be used to wake up the cpu for clearing the watchdog. The warning point for the watchdog timer can be calculated with the formula:

$$T_{\text{WARNING}} = (2^{3+\text{PERSEL}}) * (\text{WARNSEL} / 4) + 1) / f,$$

where  $f$  is the frequency of the selected clock.

When the watchdog is enabled, it is recommended to clear the watchdog before changing WARNSEL.

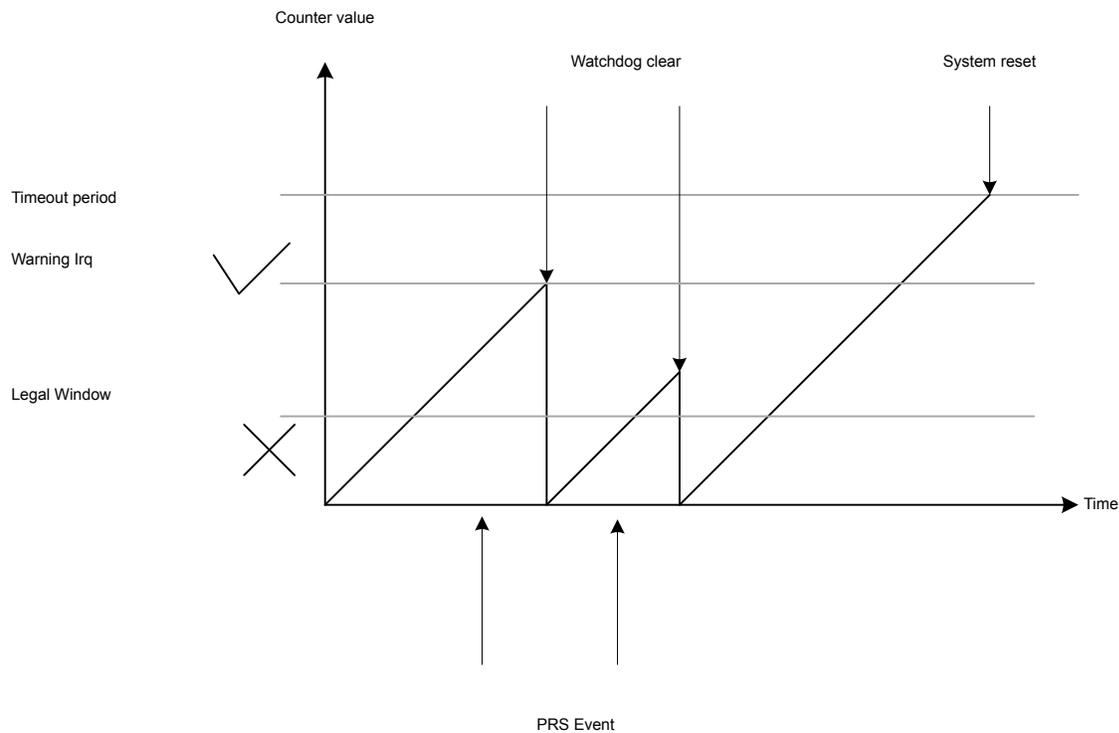
### 15.3.6 Window Interrupt

This interrupt occurs when the watchdog is cleared below a certain threshold. This threshold is given by the formula:

$$T_{\text{WARNING}} = (2^{3+\text{PERSEL}}) * (\text{WINSEL}/8) + 1)/f,$$

where  $f$  is the frequency of the selected clock.

This value will be approximately 12.5%, 25%, 37.5%, 50%, 62.5%, 75%, or 87.5% of the timeout value based on the WINSEL field of the WDOGn\_CTRL. [Figure 15.2 WDOG Warning, Window, and Timeout on page 448](#) illustrates the warning, the window, and the timeout interrupts. Also, it shows where the prs rising edge needs to happen. The prs edge detection feature is discussed later.



**Figure 15.2. WDOG Warning, Window, and Timeout**

When the watchdog is enabled, it is recommended to clear the watchdog before changing WINSEL.

### 15.3.7 PRS as Watchdog Clear

The first PRS channel (selected by register WDOGn\_PCH0\_PRSCTRL) can be used to clear the watchdog counter. To enable this feature, CLRSRC must be set to 1. [Figure 15.2 PRS Clearing WDOG on page 449](#) shows how the PRS channel takes over the WDOG clear function. Clearing the WDOG with the PRS is mutually exclusive of clearing the WDT by software.

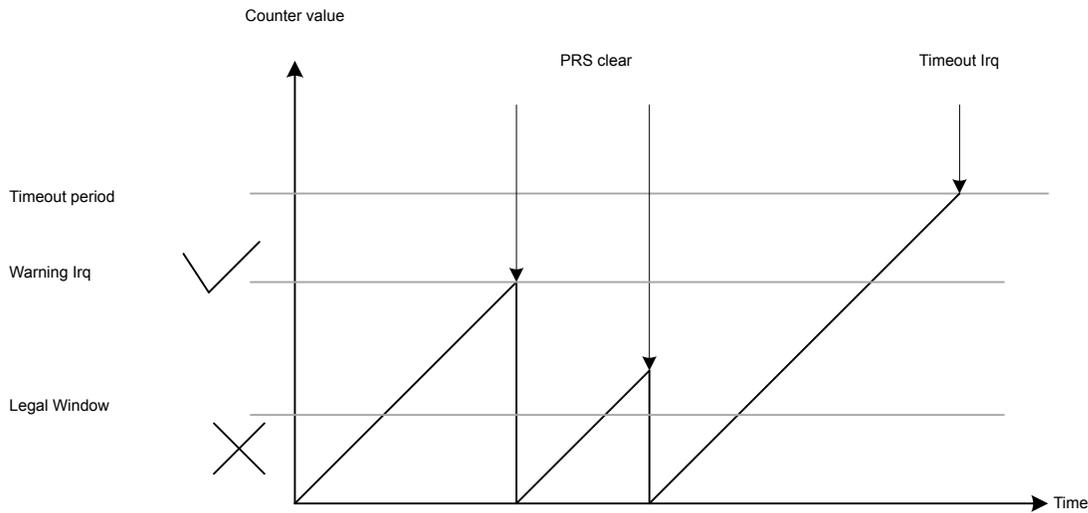


Figure 15.2. PRS Clearing WDOG

### 15.3.8 PRS Rising Edge Monitoring

PRS channels can be used to monitor multiple processes. If enabled, every time the watch dog timer is cleared the PRS channels are checked and any channel which has not seen an event can trigger an interrupt.

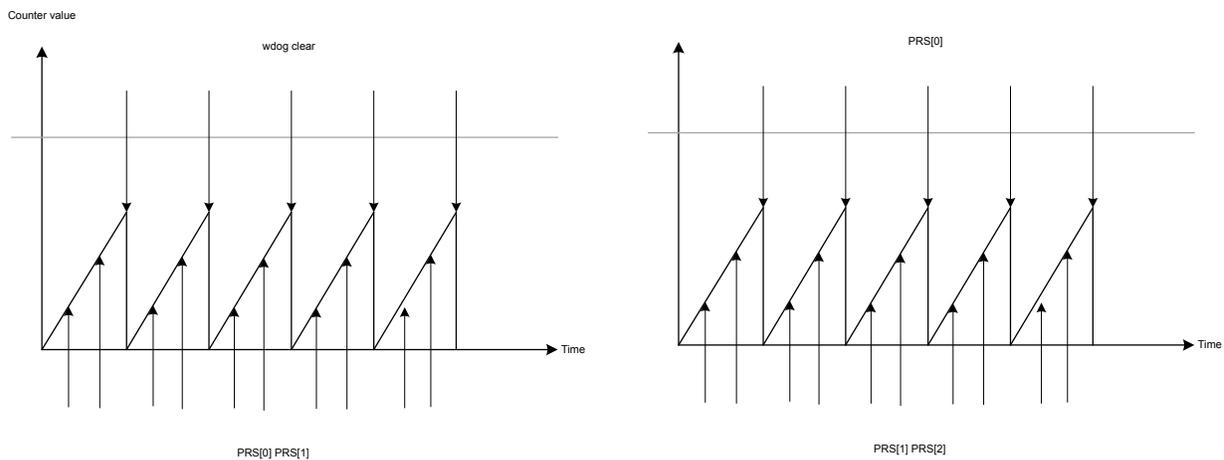


Figure 15.3. PRS Edge Monitoring in WDOG

## 15.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name               | Type  | Description                   |
|--------|--------------------|-------|-------------------------------|
| 0x000  | WDOG_CTRL          | RW    | Control Register              |
| 0x004  | WDOG_CMD           | W1    | Command Register              |
| 0x008  | WDOG_SYNCBUSY      | R     | Synchronization Busy Register |
| 0x00C  | WDOGn_PCH0_PRSCTRL | RW    | PRS Control Register          |
| 0x010  | WDOGn_PCH1_PRSCTRL | RW    | PRS Control Register          |
| 0x01C  | WDOG_IF            | R     | Watchdog Interrupt Flags      |
| 0x020  | WDOG_IFS           | W1    | Interrupt Flag Set Register   |
| 0x024  | WDOG_IFC           | (R)W1 | Interrupt Flag Clear Register |
| 0x028  | WDOG_IEN           | RW    | Interrupt Enable Register     |

## 15.5 Register Description

### 15.5.1 WDOG\_CTRL - Control Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |        |    |    |    |        |    |    |    |    |    |    |    |    |         |    |    |    |    |        |    |    |   |   |   |   |            |          |      |        |        |          |    |
|---------------|--------------|--------|----|----|----|--------|----|----|----|----|----|----|----|----|---------|----|----|----|----|--------|----|----|---|---|---|---|------------|----------|------|--------|--------|----------|----|
| 0x000         | 31           | 30     | 29 | 28 | 27 | 26     | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17      | 16 | 15 | 14 | 13 | 12     | 11 | 10 | 9 | 8 | 7 | 6 | 5          | 4        | 3    | 2      | 1      | 0        |    |
| <b>Reset</b>  | 0            | 0      |    |    |    | 0x0    |    |    |    |    |    |    |    |    | 0x0     |    |    |    |    | 0x0    |    |    |   |   |   |   | 0          | 0        | 0    | 0      | 0      | 0        | 0  |
| <b>Access</b> | RW           | RW     |    |    |    | RW     |    |    |    |    |    |    |    |    | RW      |    |    |    |    | RW     |    |    |   |   |   |   | RW         | RW       | RW   | RW     | RW     | RW       | RW |
| <b>Name</b>   | WDOGRSTDIS   | CLRSRC |    |    |    | WINSEL |    |    |    |    |    |    |    |    | WARNSEL |    |    |    |    | CLKSEL |    |    |   |   |   |   | SWOSCBLOCK | EM4BLOCK | LOCK | EM3RUN | EM2RUN | DEBUGRUN | EN |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31    | WDOGRSTDIS      | 0   | RW     | <b>Watchdog Reset Disable</b><br>Disable watchdog reset output.         |
|       | Value           | Mode  |        | Description   |
|       | 0               | EN  |        | A timeout will cause a watchdog reset                                   |
|       | 1               | DIS   |        | A timeout will not cause a watchdog reset                               |
| 30    | CLRSRC          | 0   | RW     | <b>Watchdog Clear Source</b><br>Select watchdog clear source.           |
|       | Value           | Mode  |        | Description   |
|       | 0               | SW  |        | A write to the clear bit will clear the watchdog counter                |
|       | 1               | PCH0  |        | A rising edge on the PRS Channel0 will clear the watchdog counter       |
| 29:27 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 26:24 | WINSEL          | 0x0   | RW     | <b>Watchdog Illegal Window Select</b><br>Select watchdog illegal limit. |
|       | Value           |   |        | Description   |
|       | 0               |   |        | Disabled.   |
|       | 1               |   |        | Window limit is 12.5% of the Timeout.                                   |
|       | 2               |   |        | Window limit is 25.0% of the Timeout.                                   |
|       | 3               |   |        | Window limit is 37.5% of the Timeout.                                   |
|       | 4               |   |        | Window limit is 50.0% of the Timeout.                                   |
|       | 5               |   |        | Window limit is 62.5% of the Timeout.                                   |
|       | 6               |   |        | Window limit is 75.0% of the Timeout.                                   |
|       | 7               |   |        | Window limit is 87.5% of the Timeout.                                   |

| Bit   | Name     | Reset   | Access | Description   |
|-------|----------|---|--------|---|
| 23:18 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 17:16 | WARNSEL  | 0x0   | RW     | <b>Watchdog Timeout Period Select</b><br>Select watchdog warning timeout period.                            |
|       | Value    |   |        | Description   |
|       | 0        |   |        | Disabled.   |
|       | 1        |   |        | Warning timeout is 25% of the Timeout.  |
|       | 2        |   |        | Warning timeout is 50% of the Timeout.  |
|       | 3        |   |        | Warning timeout is 75% of the Timeout.  |
| 15:14 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 13:12 | CLKSEL   | 0x0   | RW     | <b>Watchdog Clock Select</b><br>Selects the WDOG oscillator, i.e. the clock on which the watchdog will run. |
|       | Value    | Mode  |        | Description   |
|       | 0        | ULFRCO  |        | ULFRCO  |
|       | 1        | LFRCO   |        | LFRCO   |
|       | 2        | LFXO  |        | LFXO  |
|       | 3        | HFCORECLK   |        | HFCORECLK   |
| 11:8  | PERSEL   | 0xF   | RW     | <b>Watchdog Timeout Period Select</b><br>Select watchdog timeout period.                                    |
|       | Value    |   |        | Description   |
|       | 0        |   |        | Timeout period of 9 watchdog clock cycles.  |
|       | 1        |   |        | Timeout period of 17 watchdog clock cycles.   |
|       | 2        |   |        | Timeout period of 33 watchdog clock cycles.   |
|       | 3        |   |        | Timeout period of 65 watchdog clock cycles.   |
|       | 4        |   |        | Timeout period of 129 watchdog clock cycles.  |
|       | 5        |   |        | Timeout period of 257 watchdog clock cycles.  |
|       | 6        |   |        | Timeout period of 513 watchdog clock cycles.  |
|       | 7        |   |        | Timeout period of 1k watchdog clock cycles.   |
|       | 8        |   |        | Timeout period of 2k watchdog clock cycles.   |
|       | 9        |   |        | Timeout period of 4k watchdog clock cycles.   |
|       | 10       |   |        | Timeout period of 8k watchdog clock cycles.   |
|       | 11       |   |        | Timeout period of 16k watchdog clock cycles.  |
|       | 12       |   |        | Timeout period of 32k watchdog clock cycles.  |
|       | 13       |   |        | Timeout period of 64k watchdog clock cycles.  |
|       | 14       |   |        | Timeout period of 128k watchdog clock cycles.   |

| Bit | Name            | Reset   | Access | Description  |
|-----|-----------------|---|--------|--|
| 15  |                 |   |        | Timeout period of 256k watchdog clock cycles.  |
| 7   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 6   | SWOSCBLOCK      | 0   | RW     | <b>Software Oscillator Disable Block</b><br>Set to disallow disabling of the selected WDOG oscillator. Writing this bit to 1 will turn on the selected WDOG oscillator if it is not already running. |
|     | Value           |   |        | Description  |
|     | 0               |   |        | Software is allowed to disable the selected WDOG oscillator. See CMU for detailed description. Note that also CMU registers are lockable.  |
|     | 1               |   |        | Software is not allowed to disable the selected WDOG oscillator.   |
| 5   | EM4BLOCK        | 0   | RW     | <b>Energy Mode 4 Block</b><br>Set to disallow EM4 entry by software.   |
|     | Value           |   |        | Description  |
|     | 0               |   |        | EM4 can be entered by software. See EMU for detailed description.  |
|     | 1               |   |        | EM4 cannot be entered by software.   |
| 4   | LOCK            | 0   | RW     | <b>Configuration Lock</b><br>Set to lock the watchdog configuration. This bit can only be cleared by reset.  |
|     | Value           |   |        | Description  |
|     | 0               |   |        | Watchdog configuration can be changed.   |
|     | 1               |   |        | Watchdog configuration cannot be changed.  |
| 3   | EM3RUN          | 0   | RW     | <b>Energy Mode 3 Run Enable</b><br>Set to keep watchdog running in EM3.  |
|     | Value           |   |        | Description  |
|     | 0               |   |        | Watchdog timer is frozen in EM3.   |
|     | 1               |   |        | Watchdog timer is running in EM3.  |
| 2   | EM2RUN          | 0   | RW     | <b>Energy Mode 2 Run Enable</b><br>Set to keep watchdog running in EM2.  |
|     | Value           |   |        | Description  |
|     | 0               |   |        | Watchdog timer is frozen in EM2.   |
|     | 1               |   |        | Watchdog timer is running in EM2.  |
| 1   | DEBUGRUN        | 0   | RW     | <b>Debug Mode Run Enable</b><br>Set to keep watchdog running in debug mode.  |
|     | Value           |   |        | Description  |
|     | 0               |   |        | Watchdog timer is frozen in debug mode.  |
|     | 1               |   |        | Watchdog timer is running in debug mode.   |

| Bit | Name | Reset | Access | Description  |
|-----|------|-------|--------|--|
| 0   | EN   | 0     | RW     | <b>Watchdog Timer Enable</b><br>Set to enabled watchdog timer. |

### 15.5.2 WDOG\_CMD - Command Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------|
| 0x004         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0     |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0     |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | W1    |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | CLEAR |

| Bit  | Name            | Reset   | Access | Description  |
|------|-----------------|---|--------|--|
| 31:1 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 0    | CLEAR           | 0   | W1     | <b>Watchdog Timer Clear</b><br>Clear watchdog timer. The bit must be written 4 watchdog cycles before the timeout. |
|      | Value           | Mode  |        | Description  |
|      | 0               | UNCHANGED   |        | Watchdog timer is unchanged.   |
|      | 1               | CLEARED   |        | Watchdog timer is cleared to 0.  |



**15.5.4 WDOGn\_PCHx\_PRSCTRL - PRS Control Register (Async Reg)**

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |              |   |   |   |   |       |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|--------------|---|---|---|---|-------|---|---|---|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8            | 7 | 6 | 5 | 4 | 3     | 2 | 1 | 0 |  |
| 0x00C         |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |              |   |   |   |   |       |   |   |   |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | 0            |   |   |   |   | 0x0   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | RW           |   |   |   |   | RW    |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | PRSMISSRSTEN |   |   |   |   | PRSEL |   |   |   |  |

| Bit  | Name            | Reset   | Access | Description  |
|------|-----------------|---|--------|--|
| 31:9 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 8    | PRSMISSRSTEN    | 0   | RW     | <b>PRS Missing Event Will Trigger a Watchdog Reset</b><br>When set, a PRS missing event will trigger a watchdog reset. |
| 7:4  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 3:0  | PRSEL           | 0x0   | RW     | <b>PRS Channel PRS Select</b><br>These bits select the PRS input for the PRS channel.                                  |
|      | Value           | Mode  |        | Description  |
|      | 0               | PRSCH0  |        | PRS Channel 0 selected as input  |
|      | 1               | PRSCH1  |        | PRS Channel 1 selected as input  |
|      | 2               | PRSCH2  |        | PRS Channel 2 selected as input  |
|      | 3               | PRSCH3  |        | PRS Channel 3 selected as input  |
|      | 4               | PRSCH4  |        | PRS Channel 4 selected as input  |
|      | 5               | PRSCH5  |        | PRS Channel 5 selected as input  |
|      | 6               | PRSCH6  |        | PRS Channel 6 selected as input  |
|      | 7               | PRSCH7  |        | PRS Channel 7 selected as input  |
|      | 8               | PRSCH8  |        | PRS Channel 8 selected as input  |
|      | 9               | PRSCH9  |        | PRS Channel 9 selected as input  |
|      | 10              | PRSCH10   |        | PRS Channel 10 selected as input   |
|      | 11              | PRSCH11   |        | PRS Channel 11 selected as input   |

## 15.5.5 WDOG\_IF - Watchdog Interrupt Flags

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |      |    |      |   |     |   |      |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------|----|------|---|-----|---|------|---|------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|
| 0x01C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11   | 10 | 9    | 8 | 7   | 6 | 5    | 4 | 3    | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R    | 0  | R    | 0 | R   | 0 | R    | 0 | R    | 0 | R | 0 | R | 0 | R | 0 | R | 0 | R | 0 | R | 0 | R | 0 | R | 0 | R | 0 | R | 0 |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R    |    | R    |   | R   |   | R    |   | R    |   | R |   | R |   | R |   | R |   | R |   | R |   | R |   | R |   | R |   | R |   | R |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PEM1 |    | PEM0 |   | WIN |   | WARN |   | TOUT |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |

| Bit  | Name     | Reset  | Access | Description   |
|------|----------|--|--------|---|
| 31:5 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 4    | PEM1     | 0  | R      | <b>PRS Channel One Event Missing Interrupt Flag</b><br>Set when a WDOG clear happens before a prs event has been detected on PRS channel one.   |
| 3    | PEM0     | 0  | R      | <b>PRS Channel Zero Event Missing Interrupt Flag</b><br>Set when a WDOG clear happens before a prs event has been detected on PRS channel zero. |
| 2    | WIN      | 0  | R      | <b>WDOG Window Interrupt Flag</b><br>Set when a WDOG clear happens below the window limit value.  |
| 1    | WARN     | 0  | R      | <b>WDOG Warning Timeout Interrupt Flag</b><br>Set when a WDOG warning timeout has occurred.   |
| 0    | TOUT     | 0  | R      | <b>WDOG Timeout Interrupt Flag</b><br>Set when a WDOG timeout has occurred.   |

## 15.5.6 WDOG\_IFS - Interrupt Flag Set Register

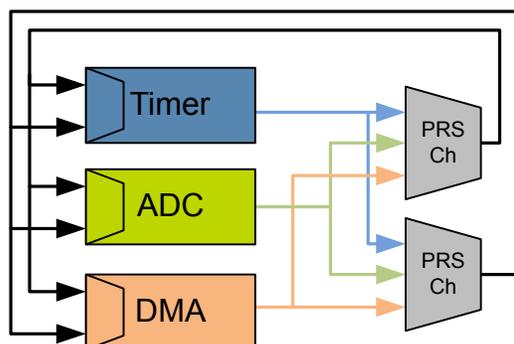
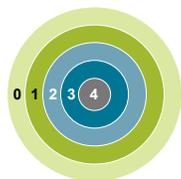
| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |      |      |     |      |      |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------|------|-----|------|------|---|---|---|---|---|---|---|
| 0x020         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11   | 10   | 9   | 8    | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0    | 0    | 0   | 0    | 0    |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W1   | W1   | W1  | W1   | W1   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PEM1 | PEM0 | WIN | WARN | TOUT |   |   |   |   |   |   |   |

| Bit  | Name            | Reset   | Access | Description  |
|------|-----------------|---|--------|--|
| 31:5 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 4    | PEM1            | 0   | W1     | <b>Set PEM1 Interrupt Flag</b><br>Write 1 to set the PEM1 interrupt flag |
| 3    | PEM0            | 0   | W1     | <b>Set PEM0 Interrupt Flag</b><br>Write 1 to set the PEM0 interrupt flag |
| 2    | WIN             | 0   | W1     | <b>Set WIN Interrupt Flag</b><br>Write 1 to set the WIN interrupt flag   |
| 1    | WARN            | 0   | W1     | <b>Set WARN Interrupt Flag</b><br>Write 1 to set the WARN interrupt flag |
| 0    | TOUT            | 0   | W1     | <b>Set TOUT Interrupt Flag</b><br>Write 1 to set the TOUT interrupt flag |





## 16. PRS - Peripheral Reflex System



### Quick Facts

#### What?

The Peripheral Reflex System (PRS) allows configurable, fast, and autonomous communication between peripherals.

#### Why?

Events and signals from one peripheral can be used as input signals or triggered by other peripherals. Besides, PRS reduces latency and ensures predictable timing by reducing software overhead and thus current consumption.

#### How?

Without CPU intervention the peripherals can send Reflex signals (both pulses and level) to each other in single or chained steps. The peripherals can be set up to perform actions based on the incoming Reflex signals. This results in improved system performance and reduced energy consumption.

### 16.1 Introduction

The Peripheral Reflex System (PRS) is a network allowing direct communication between different peripheral modules without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these Reflex signals through Reflex channels to consumer peripherals which perform actions depending on the Reflex signals received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

### 16.2 Features

- 12 Configurable Reflex Channels
  - Each channel can be connected to any producing peripheral, including the PRS channels
  - Consumers can choose which channel to listen to
  - Selectable edge detector (Rising, falling and both edges)
  - Configurable AND and OR between channels
  - Optional channel invert
  - PRS can generate event to CPU
  - Two independent DMA requests based on PRS channels
- Software controlled channel output
  - Configurable level
  - Triggered pulses

## 16.3 Functional Description

An overview of the PRS module is shown in [Figure 16.1 PRS Overview on page 462](#). The PRS contains 12 Reflex channels. All channels can select any Reflex signal offered by the producers. The consumers can choose which PRS channel to listen to and perform actions based on the Reflex signals routed through that channel. The Reflex signals can be both edge signals and level signals.

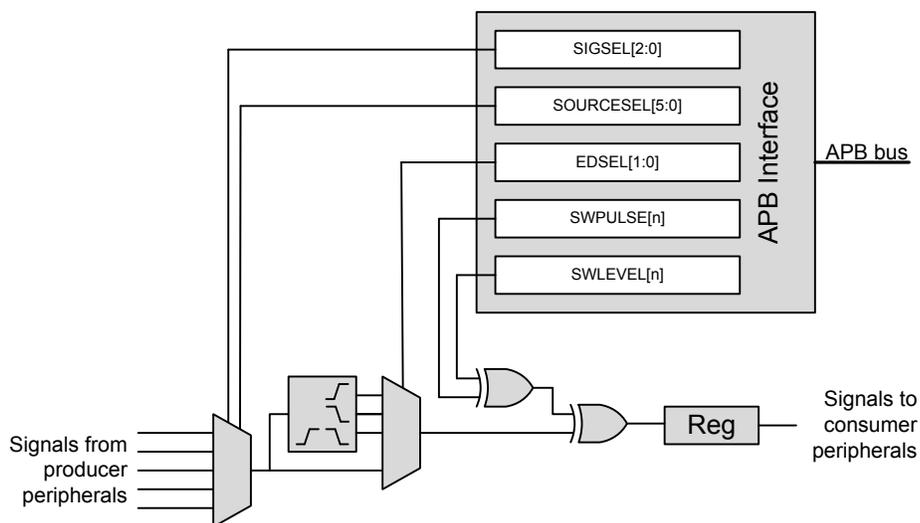


Figure 16.1. PRS Overview

### 16.3.1 Channel Functions

Different functions can be applied to a Reflex signal within the PRS. Each channel includes an edge detector to enable generation of pulse signals from level signals. The PRS channels can also be manually triggered by writing to PRS\_SWPULSE or PRS\_SWLEVEL. SWLEVEL[n] is a programmable level for each channel and holds the value it is programmed to. Setting SWPULSE[n] will cause the PRS channel to output a high pulse that is one HFCLK cycle wide. The SWLEVEL[n] and SWPULSE[n] signals are then XOR'ed with the selected input from the producers to form the output signal sent to the consumers listening to the channel. For example, when SWLEVEL[n] is set, if a producer produces a signal of 1, this will cause a channel output of 0.

#### 16.3.1.1 Operational Mode

Reflex channels can operate in two modes, synchronous or asynchronous. In synchronous mode Reflex signals are clocked on the HFCLK, and can be used by any Reflex consumer. However, this will not work in EM2/EM3, since the HFCLK will be turned off.

Asynchronous Reflex channels are not clocked on HFCLK, and can be used even in EM2/EM3. However, the asynchronous mode can only be used by a subset of the Reflex consumers.

The asynchronous Reflex signals generated by the producers are indicated in the SIGSEL field of PRS\_CHx\_CTRL register. The consumers capable of utilizing asynchronous Reflex signals include the LEUART and the PCNT. The USART can also utilize some particular asynchronous signals. Refer to the respective modules for details on how to configure them to use the PRS.

**Note:** If a Reflex channel with ASYNC field of PRS\_CHx\_CTRL register set to '1' is used in a consumer not supporting asynchronous reflexes, the behaviour is undefined

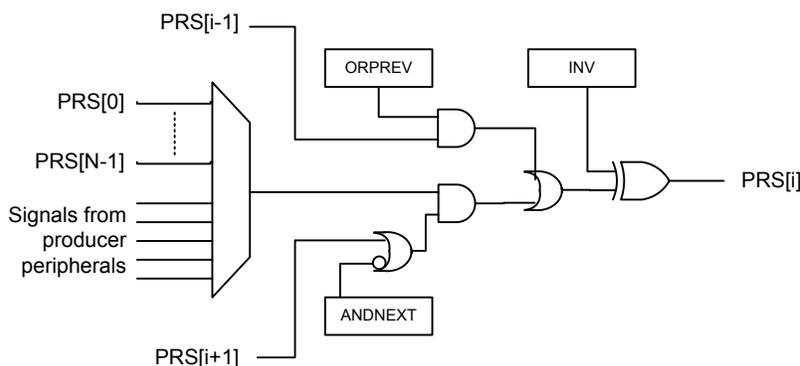
### 16.3.1.2 Edge Detection and Clock Domains

Using EDSEL in PRS\_CHx\_CTRL, edge detection can be applied to a PRS signal. When edge detection is enabled, changes in the PRS input will result in a pulse on the PRS channel. This requires that the ASYNC bit in PRS\_CHx\_CTRL is cleared. Signals on the PRS input must be at least one HFCLK period wide in order to be detected properly. This applies to all cases when ASYNC is not used in the PRS.

For communication between peripherals on different prescaled clocks (e.g. between peripherals on HFCLK and HFPERCLK), there are two options. One option is to use level signals. No additional action is needed for level signals, but software must make sure that the level signals are held long enough for the destination domain to detect them. The other option is to use pulse signals. For pulse signals, edge detection should be enabled (by configuring EDSEL in PRS\_CHx\_CTRL to positive edge, negative edge, or both) and STRETCH in PRS\_CHx\_CTRL should be set. When edge detection and stretch are enabled on a PRS source, the output on the PRS channel is held long enough for the destination domain to detect the pulse. This also works if there are multiple destination domains running at different frequencies.

### 16.3.1.3 Configurable PRS Logic

Each PRS channel has three logic functions that can be used by themselves or in combination. The selected PRS source can be AND'ed with the next PRS channel output, OR'ed with the previous PRS channel output and inverted. This is shown in [Figure 16.1 PRS Overview on page 462](#). The order of the functions is important. If OR and AND are enabled at the same time, AND is applied first, and then OR. Note that the previous and next channel options wrap around. Using the ORPREV option on the first PRS channel OR's with the output of the last PRS channel. Likewise, using the ANDNEXT option on the last PRS channel AND's with the output of the first PRS channel.



**Figure 16.2. Configurable PRS Logic**

In addition to the logic functions that can combine a PRS channel with one of its neighbors, a PRS channel can also select any other PRS channel as input. This can allow relatively complex logic functions to be created.

### 16.3.2 Producers

Through SOURCESEL in PRS\_CHx\_CTRL, each PRS channel selects signal producers. Each producer outputs one or more signals which can be selected by setting the SIGSEL field in PRS\_CHx\_CTRL. Setting the SOURCESEL bits to 0 (Off) leads to a constant 0 output from the input mux. An overview of the available producers can be found in the SOURCESEL and SIGSEL fields in PRS\_CHx\_CTRL. Note that GPIO producers are selected in the GPIO module using the edge interrupt configuration settings described in [33.3.5.1 Edge Interrupt Generation](#). GPIOPIN0 uses the selection for the EXTIO interrupt, GPIOPIN1 uses the selection for the EXT11 interrupt, and so on.

### 16.3.3 Consumers

Consumer peripherals (Listed in [Table 16.1 Reflex Consumers on page 464](#)) can be set to listen to a PRS channel and perform an action based on the signal received on that channel. While most consumers can handle either only pulse input or only level input, some can handle both pulse and level inputs.

**Table 16.1. Reflex Consumers**

| Module | Reflex Input  | Input Format  |
|--------|---|---------------|
| TIMER  | Compare/Capture Channel   | Pulse / Level |
|        | Alternate Input for DTI<br>(Available only in specific TIMERS<br>See data sheet for details)          | Level         |
|        | Alternate Input for DTI Fault 0<br>(Available only in specific TIMERS<br>See data sheet for details)  | Level         |
|        | Alternate Input for DTI Fault 1<br>(Available only in specific TIMERS<br>See data sheet for details)  | Level         |
| WTIMER | Compare/Capture Channel   | Pulse / Level |
|        | Alternate Input for DTI<br>(Available only in specific WTIMERS<br>See data sheet for details)         | Level         |
|        | Alternate Input for DTI Fault 0<br>(Available only in specific WTIMERS<br>See data sheet for details) | Level         |
|        | Alternate Input for DTI Fault 1<br>(Available only in specific WTIMERS<br>See data sheet for details) | Level         |
| USART  | RX/TX Trigger   | Pulse         |
|        | Alternate Input for IrDA  | Level         |
|        | Alternate Input for RX  | Level         |
|        | Alternate Input for CLK   | Level         |
| VDAC   | Channel 0 Trigger   | Pulse         |
|        | Channel 1 Trigger   | Pulse         |
| ADC    | Single Sample Trigger   | Pulse         |
|        | Scan Sequence Trigger   | Pulse         |
| IDAC   | Alternate Input for OUTMODE   | Level         |
| CMU    | Alternate Input for Calibration Up-Counter  | Level         |
|        | Alternate Input for Calibration Down-Counter  | Level         |
| LEUART | Alternate Input for RX  | Level         |
| PCNT   | Compare/Clear Trigger   | Pulse/Level   |
|        | Alternate Input for S0IN  | Level         |
|        | Alternate Input for S1IN  | Level         |

| Module   | Reflex Input            | Input Format |
|----------|-------------------------|--------------|
| LESENSE  | Scan Start              | Pulse        |
|          | LESENSE Decoder Bit 0   | Level        |
|          | LESENSE Decoder Bit 1   | Level        |
|          | LESENSE Decoder Bit 2   | Level        |
|          | LESENSE Decoder Bit 3   | Level        |
| WDOG     | Peripheral Watchdog     | Pulse        |
| LETIMER  | Start LETIMER           | Pulse        |
|          | Stop LETIMER            | Pulse        |
|          | Clear LETIMER           | Pulse        |
| RTCC     | Compare/Capture Channel | Pulse/Level  |
| PRS      | Set Event               | Pulse        |
|          | DMA Request 0           | Pulse        |
|          | DMA Request 1           | Pulse        |
| CAPSENSE | Start Conversion        | Pulse        |

#### 16.3.4 Event on PRS

The PRS can be used to send events to the MCU. This is very useful in combination with the Wait For Event (WFE) instruction. A single PRS channel can be selected for this using SEVONPRSEL in PRS\_CTRL, and the feature is enabled by setting SEVONPRS in the same register.

Using SEVONPRS, one can e.g. set up a timer to trigger an event to the MCU periodically, every time letting the MCU pass through a WFE instruction in its program. This can help in performance-critical sections where timing is known, and the goal is to wait for an event, then execute some code, then wait for an event, then execute some code and so on.

#### 16.3.5 DMA Request on PRS

Up to two independent DMA requests can be generated by the PRS. The PRS signals triggering the DMA requests are selected using the LDMA\_CHx\_REQSEL register, by setting SOURCESEL to PRS and SIGSEL to either PRSREQ0 or PRSREQ1. The DMA requests are cleared when the DMA services the requests. The requests are set whenever the selected PRS signals are high.

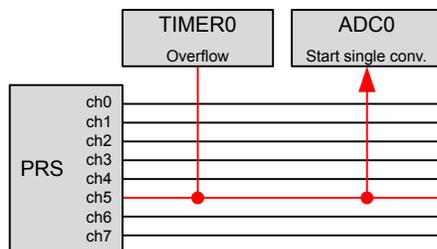
The selected PRS signals must have ASYNC cleared when they are used as inputs to the DMA. Edge detection in the PRS can be enabled to only trigger transfers on edges.

### 16.3.6 Example

The example below (illustrated in [Figure 16.3 TIMER0 Overflow Starting ADC0 Single Conversions Through PRS Channel 5. on page 466](#)) shows how to set up ADC0 to start single conversions every time TIMER0 overflows (one HFPERCLK cycle high pulse), using PRS channel 5:

- Set SOURCESEL in PRS\_CH5\_CTRL to TIMER0 as input to PRS channel 5.
- Set SIGSEL in PRS\_CH5\_CTRL to select the overflow signal (TIMER0OF from TIMER0).
- Configure ADC0 with the desired conversion set-up.
- Set SINGLEPRSEN in ADC0\_SINGLECTRL to 1 to enable single conversions to be started by a high PRS input signal.
- Set SINGLEPRSSEL in ADC0\_SINGLECTRL to 0x5 to select PRS channel 5 as input to start the single conversion.
- Start TIMER0 with the desired TOP value, an overflow PRS signal is output automatically on overflow.

Note that the ADC results needs to be fetched either by the CPU or DMA.



**Figure 16.3. TIMER0 Overflow Starting ADC0 Single Conversions Through PRS Channel 5.**

### 16.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name          | Type | Description                     |
|--------|---------------|------|---------------------------------|
| 0x000  | PRS_SWPULSE   | W1   | Software Pulse Register         |
| 0x004  | PRS_SWLEVEL   | RW   | Software Level Register         |
| 0x008  | PRS_ROUTEPEEN | RW   | I/O Routing Pin Enable Register |
| 0x010  | PRS_ROUTELOC0 | RW   | I/O Routing Location Register   |
| 0x014  | PRS_ROUTELOC1 | RW   | I/O Routing Location Register   |
| 0x018  | PRS_ROUTELOC2 | RW   | I/O Routing Location Register   |
| 0x030  | PRS_CTRL      | RW   | Control Register                |
| 0x034  | PRS_DMAREQ0   | RW   | DMA Request 0 Register          |
| 0x038  | PRS_DMAREQ1   | RW   | DMA Request 1 Register          |
| 0x040  | PRS_PEEK      | R    | PRS Channel Values              |
| 0x050  | PRS_CH0_CTRL  | RW   | Channel Control Register        |
| ...    | PRS_CHx_CTRL  | RW   | Channel Control Register        |
| 0x07C  | PRS_CH11_CTRL | RW   | Channel Control Register        |

## 16.5 Register Description

### 16.5.1 PRS\_SWPULSE - Software Pulse Register

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |           |           |          |          |          |          |          |          |          |          |          |          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------|-----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0x000  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11        | 10        | 9        | 8        | 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Reset  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0         | 0         | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |    |
| Access |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W1        | W1        | W1       | W1       | W1       | W1       | W1       | W1       | W1       | W1       | W1       | W1       | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 |
| Name   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CH11PULSE | CH10PULSE | CH9PULSE | CH8PULSE | CH7PULSE | CH6PULSE | CH5PULSE | CH4PULSE | CH3PULSE | CH2PULSE | CH1PULSE | CH0PULSE |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

| Bit   | Name      | Reset  | Access | Description                                      |
|-------|-----------|--|--------|--|
| 31:12 | Reserved  | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 11    | CH11PULSE | 0  | W1     | <b>Channel 11 Pulse Generation</b><br>See bit 0. |
| 10    | CH10PULSE | 0  | W1     | <b>Channel 10 Pulse Generation</b><br>See bit 0. |
| 9     | CH9PULSE  | 0  | W1     | <b>Channel 9 Pulse Generation</b><br>See bit 0.  |
| 8     | CH8PULSE  | 0  | W1     | <b>Channel 8 Pulse Generation</b><br>See bit 0.  |
| 7     | CH7PULSE  | 0  | W1     | <b>Channel 7 Pulse Generation</b><br>See bit 0.  |
| 6     | CH6PULSE  | 0  | W1     | <b>Channel 6 Pulse Generation</b><br>See bit 0.  |
| 5     | CH5PULSE  | 0  | W1     | <b>Channel 5 Pulse Generation</b><br>See bit 0.  |
| 4     | CH4PULSE  | 0  | W1     | <b>Channel 4 Pulse Generation</b><br>See bit 0.  |
| 3     | CH3PULSE  | 0  | W1     | <b>Channel 3 Pulse Generation</b><br>See bit 0.  |
| 2     | CH2PULSE  | 0  | W1     | <b>Channel 2 Pulse Generation</b><br>See bit 0.  |
| 1     | CH1PULSE  | 0  | W1     | <b>Channel 1 Pulse Generation</b><br>See bit 0.  |
| 0     | CH0PULSE  | 0  | W1     | <b>Channel 0 Pulse Generation</b>                |

Write to 1 to generate one HFCLK cycle high pulse. This pulse is XOR'ed with the corresponding bit in the SWLEVEL register and the selected PRS input signal to generate the channel output.

### 16.5.2 PRS\_SWLEVEL - Software Level Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |           |           |          |          |          |          |          |          |          |          |          |          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------|-----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0x004         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11        | 10        | 9        | 8        | 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0         | 0         | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |    |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW        | RW        | RW       | RW       | RW       | RW       | RW       | RW       | RW       | RW       | RW       | RW       | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CH11LEVEL | CH10LEVEL | CH9LEVEL | CH8LEVEL | CH7LEVEL | CH6LEVEL | CH5LEVEL | CH4LEVEL | CH3LEVEL | CH2LEVEL | CH1LEVEL | CH0LEVEL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

| Bit   | Name                    | Reset   | Access | Description                      |
|-------|-------------------------|---|--------|----------------------------------|
| 31:12 | Reserved                | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |                                  |
| 11    | CH11LEVEL<br>See bit 0. | 0   | RW     | <b>Channel 11 Software Level</b> |
| 10    | CH10LEVEL<br>See bit 0. | 0   | RW     | <b>Channel 10 Software Level</b> |
| 9     | CH9LEVEL<br>See bit 0.  | 0   | RW     | <b>Channel 9 Software Level</b>  |
| 8     | CH8LEVEL<br>See bit 0.  | 0   | RW     | <b>Channel 8 Software Level</b>  |
| 7     | CH7LEVEL<br>See bit 0.  | 0   | RW     | <b>Channel 7 Software Level</b>  |
| 6     | CH6LEVEL<br>See bit 0.  | 0   | RW     | <b>Channel 6 Software Level</b>  |
| 5     | CH5LEVEL<br>See bit 0.  | 0   | RW     | <b>Channel 5 Software Level</b>  |
| 4     | CH4LEVEL<br>See bit 0.  | 0   | RW     | <b>Channel 4 Software Level</b>  |
| 3     | CH3LEVEL<br>See bit 0.  | 0   | RW     | <b>Channel 3 Software Level</b>  |
| 2     | CH2LEVEL<br>See bit 0.  | 0   | RW     | <b>Channel 2 Software Level</b>  |
| 1     | CH1LEVEL<br>See bit 0.  | 0   | RW     | <b>Channel 1 Software Level</b>  |
| 0     | CH0LEVEL                | 0   | RW     | <b>Channel 0 Software Level</b>  |

The value in this register is XOR'ed with the corresponding bit in the SWPULSE register and the selected PRS input signal to generate the channel output.

## 16.5.3 PRS\_ROUTEPEN - I/O Routing Pin Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |         |        |        |        |        |        |        |        |        |        |        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|---------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0x008         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11      | 10      | 9      | 8      | 7      | 6      | 5      | 4      | 3      | 2      | 1      | 0      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       | 0       | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |    |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      | RW      | RW     | RW     | RW     | RW     | RW     | RW     | RW     | RW     | RW     | RW     | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CH11PEN | CH10PEN | CH9PEN | CH8PEN | CH7PEN | CH6PEN | CH5PEN | CH4PEN | CH3PEN | CH2PEN | CH1PEN | CH0PEN |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 31:12 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 11    | CH11PEN         | 0   | RW     | <b>CH11 Pin Enable</b><br>When set, GPIO output from PRS channel 11 is enabled |
| 10    | CH10PEN         | 0   | RW     | <b>CH10 Pin Enable</b><br>When set, GPIO output from PRS channel 10 is enabled |
| 9     | CH9PEN          | 0   | RW     | <b>CH9 Pin Enable</b><br>When set, GPIO output from PRS channel 9 is enabled   |
| 8     | CH8PEN          | 0   | RW     | <b>CH8 Pin Enable</b><br>When set, GPIO output from PRS channel 8 is enabled   |
| 7     | CH7PEN          | 0   | RW     | <b>CH7 Pin Enable</b><br>When set, GPIO output from PRS channel 7 is enabled   |
| 6     | CH6PEN          | 0   | RW     | <b>CH6 Pin Enable</b><br>When set, GPIO output from PRS channel 6 is enabled   |
| 5     | CH5PEN          | 0   | RW     | <b>CH5 Pin Enable</b><br>When set, GPIO output from PRS channel 5 is enabled   |
| 4     | CH4PEN          | 0   | RW     | <b>CH4 Pin Enable</b><br>When set, GPIO output from PRS channel 4 is enabled   |
| 3     | CH3PEN          | 0   | RW     | <b>CH3 Pin Enable</b><br>When set, GPIO output from PRS channel 3 is enabled   |
| 2     | CH2PEN          | 0   | RW     | <b>CH2 Pin Enable</b><br>When set, GPIO output from PRS channel 2 is enabled   |
| 1     | CH1PEN          | 0   | RW     | <b>CH1 Pin Enable</b><br>When set, GPIO output from PRS channel 1 is enabled   |
| 0     | CH0PEN          | 0   | RW     | <b>CH0 Pin Enable</b><br>When set, GPIO output from PRS channel 0 is enabled   |

## 16.5.4 PRS\_ROUTELOC0 - I/O Routing Location Register

| Offset        | Bit Position |    |    |    |    |        |    |    |    |    |    |    |    |        |    |    |    |    |    |    |    |        |   |   |   |   |   |   |   |   |   |        |  |
|---------------|--------------|----|----|----|----|--------|----|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|--------|---|---|---|---|---|---|---|---|---|--------|--|
| 0x010         | 31           | 30 | 29 | 28 | 27 | 26     | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18     | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10     | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0      |  |
| <b>Reset</b>  |              |    |    |    |    | 0x00   |    |    |    |    |    |    |    | 0x00   |    |    |    |    |    |    |    | 0x00   |   |   |   |   |   |   |   |   |   | 0x00   |  |
| <b>Access</b> |              |    |    |    |    | RW     |    |    |    |    |    |    |    | RW     |    |    |    |    |    |    |    | RW     |   |   |   |   |   |   |   |   |   | RW     |  |
| <b>Name</b>   |              |    |    |    |    | CH3LOC |    |    |    |    |    |    |    | CH2LOC |    |    |    |    |    |    |    | CH1LOC |   |   |   |   |   |   |   |   |   | CH0LOC |  |

| Bit   | Name            | Reset   | Access      | Description  |
|-------|-----------------|---|-------------|--|
| 31:30 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 29:24 | CH3LOC          | 0x00  | RW          | <b>I/O Location</b><br>Decides the location of the channel I/O pin |
|       | Value           | Mode  | Description |  |
|       | 0               | LOC0  | Location 0  |  |
|       | 1               | LOC1  | Location 1  |  |
|       | 2               | LOC2  | Location 2  |  |
|       | 3               | LOC3  | Location 3  |  |
|       | 4               | LOC4  | Location 4  |  |
|       | 5               | LOC5  | Location 5  |  |
|       | 6               | LOC6  | Location 6  |  |
|       | 7               | LOC7  | Location 7  |  |
|       | 8               | LOC8  | Location 8  |  |
|       | 9               | LOC9  | Location 9  |  |
|       | 10              | LOC10   | Location 10 |  |
|       | 11              | LOC11   | Location 11 |  |
|       | 12              | LOC12   | Location 12 |  |
|       | 13              | LOC13   | Location 13 |  |
|       | 14              | LOC14   | Location 14 |  |
| 23:22 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 21:16 | CH2LOC          | 0x00  | RW          | <b>I/O Location</b><br>Decides the location of the channel I/O pin |
|       | Value           | Mode  | Description |  |
|       | 0               | LOC0  | Location 0  |  |
|       | 1               | LOC1  | Location 1  |  |
|       | 2               | LOC2  | Location 2  |  |

| Bit   | Name            | Reset   | Access      | Description  |
|-------|-----------------|---|-------------|--|
|       | 3               | LOC3  |             | Location 3   |
|       | 4               | LOC4  |             | Location 4   |
|       | 5               | LOC5  |             | Location 5   |
|       | 6               | LOC6  |             | Location 6   |
|       | 7               | LOC7  |             | Location 7   |
| 15:14 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 13:8  | CH1LOC          | 0x00  | RW          | <b>I/O Location</b><br>Decides the location of the channel I/O pin |
|       | Value           | Mode  | Description |  |
|       | 0               | LOC0  | Location 0  |  |
|       | 1               | LOC1  | Location 1  |  |
|       | 2               | LOC2  | Location 2  |  |
|       | 3               | LOC3  | Location 3  |  |
|       | 4               | LOC4  | Location 4  |  |
|       | 5               | LOC5  | Location 5  |  |
|       | 6               | LOC6  | Location 6  |  |
|       | 7               | LOC7  | Location 7  |  |
| 7:6   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 5:0   | CH0LOC          | 0x00  | RW          | <b>I/O Location</b><br>Decides the location of the channel I/O pin |
|       | Value           | Mode  | Description |  |
|       | 0               | LOC0  | Location 0  |  |
|       | 1               | LOC1  | Location 1  |  |
|       | 2               | LOC2  | Location 2  |  |
|       | 3               | LOC3  | Location 3  |  |
|       | 4               | LOC4  | Location 4  |  |
|       | 5               | LOC5  | Location 5  |  |
|       | 6               | LOC6  | Location 6  |  |
|       | 7               | LOC7  | Location 7  |  |
|       | 8               | LOC8  | Location 8  |  |
|       | 9               | LOC9  | Location 9  |  |
|       | 10              | LOC10   | Location 10 |  |
|       | 11              | LOC11   | Location 11 |  |
|       | 12              | LOC12   | Location 12 |  |
|       | 13              | LOC13   | Location 13 |  |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
|-----|------|-------|--------|-------------|

## 16.5.5 PRS\_ROUTELOC1 - I/O Routing Location Register

| Offset        | Bit Position |    |    |    |        |    |    |    |    |    |    |    |        |    |    |    |    |    |    |    |        |    |   |   |   |   |   |   |   |        |   |   |
|---------------|--------------|----|----|----|--------|----|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|--------|----|---|---|---|---|---|---|---|--------|---|---|
| 0x014         | 31           | 30 | 29 | 28 | 27     | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19     | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11     | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2      | 1 | 0 |
| <b>Reset</b>  |              |    |    |    | 0x00   |    |    |    |    |    |    |    | 0x00   |    |    |    |    |    |    |    | 0x00   |    |   |   |   |   |   |   |   | 0x00   |   |   |
| <b>Access</b> |              |    |    |    | RW     |    |    |    |    |    |    |    | RW     |    |    |    |    |    |    |    | RW     |    |   |   |   |   |   |   |   | RW     |   |   |
| <b>Name</b>   |              |    |    |    | CH7LOC |    |    |    |    |    |    |    | CH6LOC |    |    |    |    |    |    |    | CH5LOC |    |   |   |   |   |   |   |   | CH4LOC |   |   |

| Bit   | Name            | Reset   | Access      | Description  |
|-------|-----------------|---|-------------|--|
| 31:30 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 29:24 | CH7LOC          | 0x00  | RW          | <b>I/O Location</b><br>Decides the location of the channel I/O pin |
|       | Value           | Mode  | Description |  |
|       | 0               | LOC0  | Location 0  |  |
|       | 1               | LOC1  | Location 1  |  |
|       | 2               | LOC2  | Location 2  |  |
|       | 3               | LOC3  | Location 3  |  |
|       | 4               | LOC4  | Location 4  |  |
|       | 5               | LOC5  | Location 5  |  |
|       | 6               | LOC6  | Location 6  |  |
|       | 7               | LOC7  | Location 7  |  |
|       | 8               | LOC8  | Location 8  |  |
|       | 9               | LOC9  | Location 9  |  |
|       | 10              | LOC10   | Location 10 |  |
| 23:22 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 21:16 | CH6LOC          | 0x00  | RW          | <b>I/O Location</b><br>Decides the location of the channel I/O pin |
|       | Value           | Mode  | Description |  |
|       | 0               | LOC0  | Location 0  |  |
|       | 1               | LOC1  | Location 1  |  |
|       | 2               | LOC2  | Location 2  |  |
|       | 3               | LOC3  | Location 3  |  |
|       | 4               | LOC4  | Location 4  |  |
|       | 5               | LOC5  | Location 5  |  |
|       | 6               | LOC6  | Location 6  |  |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 7     |                 | LOC7  |        | Location 7   |
| 8     |                 | LOC8  |        | Location 8   |
| 9     |                 | LOC9  |        | Location 9   |
| 10    |                 | LOC10   |        | Location 10  |
| 11    |                 | LOC11   |        | Location 11  |
| 12    |                 | LOC12   |        | Location 12  |
| 13    |                 | LOC13   |        | Location 13  |
| 14    |                 | LOC14   |        | Location 14  |
| 15    |                 | LOC15   |        | Location 15  |
| 16    |                 | LOC16   |        | Location 16  |
| 17    |                 | LOC17   |        | Location 17  |
| 15:14 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 13:8  | CH5LOC          | 0x00  | RW     | <b>I/O Location</b><br>Decides the location of the channel I/O pin |
|       | Value           | Mode  |        | Description  |
|       | 0               | LOC0  |        | Location 0   |
|       | 1               | LOC1  |        | Location 1   |
|       | 2               | LOC2  |        | Location 2   |
|       | 3               | LOC3  |        | Location 3   |
|       | 4               | LOC4  |        | Location 4   |
|       | 5               | LOC5  |        | Location 5   |
|       | 6               | LOC6  |        | Location 6   |
| 7:6   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 5:0   | CH4LOC          | 0x00  | RW     | <b>I/O Location</b><br>Decides the location of the channel I/O pin |
|       | Value           | Mode  |        | Description  |
|       | 0               | LOC0  |        | Location 0   |
|       | 1               | LOC1  |        | Location 1   |
|       | 2               | LOC2  |        | Location 2   |
|       | 3               | LOC3  |        | Location 3   |
|       | 4               | LOC4  |        | Location 4   |
|       | 5               | LOC5  |        | Location 5   |
|       | 6               | LOC6  |        | Location 6   |

### 16.5.6 PRS\_ROUTELOC2 - I/O Routing Location Register

| Offset        | Bit Position |    |    |    |         |    |    |    |    |    |    |    |         |    |    |    |    |    |    |    |        |    |   |   |   |   |   |   |        |   |   |   |  |
|---------------|--------------|----|----|----|---------|----|----|----|----|----|----|----|---------|----|----|----|----|----|----|----|--------|----|---|---|---|---|---|---|--------|---|---|---|--|
| 0x018         | 31           | 30 | 29 | 28 | 27      | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19      | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11     | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3      | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    | 0x00    |    |    |    |    |    |    |    | 0x00    |    |    |    |    |    |    |    | 0x00   |    |   |   |   |   |   |   | 0x00   |   |   |   |  |
| <b>Access</b> |              |    |    |    | RW      |    |    |    |    |    |    |    | RW      |    |    |    |    |    |    |    | RW     |    |   |   |   |   |   |   | RW     |   |   |   |  |
| <b>Name</b>   |              |    |    |    | CH11LOC |    |    |    |    |    |    |    | CH10LOC |    |    |    |    |    |    |    | CH9LOC |    |   |   |   |   |   |   | CH8LOC |   |   |   |  |

| Bit   | Name            | Reset   | Access      | Description  |
|-------|-----------------|---|-------------|--|
| 31:30 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 29:24 | CH11LOC         | 0x00  | RW          | <b>I/O Location</b><br>Decides the location of the channel I/O pin |
|       | Value           | Mode  | Description |  |
|       | 0               | LOC0  | Location 0  |  |
|       | 1               | LOC1  | Location 1  |  |
|       | 2               | LOC2  | Location 2  |  |
|       | 3               | LOC3  | Location 3  |  |
|       | 4               | LOC4  | Location 4  |  |
|       | 5               | LOC5  | Location 5  |  |
| 23:22 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 21:16 | CH10LOC         | 0x00  | RW          | <b>I/O Location</b><br>Decides the location of the channel I/O pin |
|       | Value           | Mode  | Description |  |
|       | 0               | LOC0  | Location 0  |  |
|       | 1               | LOC1  | Location 1  |  |
|       | 2               | LOC2  | Location 2  |  |
|       | 3               | LOC3  | Location 3  |  |
|       | 4               | LOC4  | Location 4  |  |
|       | 5               | LOC5  | Location 5  |  |
| 15:14 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 13:8  | CH9LOC          | 0x00  | RW          | <b>I/O Location</b><br>Decides the location of the channel I/O pin |
|       | Value           | Mode  | Description |  |
|       | 0               | LOC0  | Location 0  |  |

| Bit | Name            | Reset   | Access | Description  |
|-----|-----------------|---|--------|--|
| 1   |                 | LOC1  |        | Location 1   |
| 2   |                 | LOC2  |        | Location 2   |
| 3   |                 | LOC3  |        | Location 3   |
| 4   |                 | LOC4  |        | Location 4   |
| 5   |                 | LOC5  |        | Location 5   |
| 6   |                 | LOC6  |        | Location 6   |
| 7   |                 | LOC7  |        | Location 7   |
| 8   |                 | LOC8  |        | Location 8   |
| 9   |                 | LOC9  |        | Location 9   |
| 10  |                 | LOC10   |        | Location 10  |
| 11  |                 | LOC11   |        | Location 11  |
| 12  |                 | LOC12   |        | Location 12  |
| 13  |                 | LOC13   |        | Location 13  |
| 14  |                 | LOC14   |        | Location 14  |
| 15  |                 | LOC15   |        | Location 15  |
| 16  |                 | LOC16   |        | Location 16  |
| 7:6 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 5:0 | CH8LOC          | 0x00  | RW     | <b>I/O Location</b><br>Decides the location of the channel I/O pin |
|     | Value           | Mode  |        | Description  |
|     | 0               | LOC0  |        | Location 0   |
|     | 1               | LOC1  |        | Location 1   |
|     | 2               | LOC2  |        | Location 2   |
|     | 3               | LOC3  |        | Location 3   |
|     | 4               | LOC4  |        | Location 4   |
|     | 5               | LOC5  |        | Location 5   |
|     | 6               | LOC6  |        | Location 6   |
|     | 7               | LOC7  |        | Location 7   |
|     | 8               | LOC8  |        | Location 8   |
|     | 9               | LOC9  |        | Location 9   |
|     | 10              | LOC10   |        | Location 10  |

### 16.5.7 PRS\_CTRL - Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |            |   |   |          |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|------------|---|---|----------|---|
| 0x030         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4          | 3 | 2 | 1        | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | 0x0        |   |   | 0        |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | RW         |   |   | RW       |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | SEVONPRSEL |   |   | SEVONPRS |   |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 31:5 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 4:1  | SEVONPRSEL      | 0x0   | RW     | <b>SEVONPRS PRS Channel Select</b><br>Selects PRS channel for SEVONPRS  |
|      | Value           | Mode  |        | Description   |
|      | 0               | PRSCH0  |        | PRS Channel 0 selected  |
|      | 1               | PRSCH1  |        | PRS Channel 1 selected  |
|      | 2               | PRSCH2  |        | PRS Channel 2 selected  |
|      | 3               | PRSCH3  |        | PRS Channel 3 selected  |
|      | 4               | PRSCH4  |        | PRS Channel 4 selected  |
|      | 5               | PRSCH5  |        | PRS Channel 5 selected  |
|      | 6               | PRSCH6  |        | PRS Channel 6 selected  |
|      | 7               | PRSCH7  |        | PRS Channel 7 selected  |
|      | 8               | PRSCH8  |        | PRS Channel 8 selected  |
|      | 9               | PRSCH9  |        | PRS Channel 9 selected  |
|      | 10              | PRSCH10   |        | PRS Channel 10 selected   |
|      | 11              | PRSCH11   |        | PRS Channel 11 selected   |
| 0    | SEVONPRS        | 0   | RW     | <b>Set Event on PRS</b><br>When set, an event is generated to the CPU when the PRS channel selected by SEVONPRSEL is high |

### 16.5.8 PRS\_DMAREQ0 - DMA Request 0 Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |       |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x034         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13    | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0   |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PRSEL |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset   | Access | Description |
|-------|----------|---|--------|-------------|
| 31:10 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |             |

|     |       |     |    |  |
|-----|-------|-----|----|--|
| 9:6 | PRSEL | 0x0 | RW | <b>DMA Request 0 PRS Channel Select</b><br>Selects PRS channel for DMA request 0 from the PRS (PRSREQ0). |
|-----|-------|-----|----|--|

| Value | Mode    | Description             |
|-------|---------|-------------------------|
| 0     | PRSCH0  | PRS Channel 0 selected  |
| 1     | PRSCH1  | PRS Channel 1 selected  |
| 2     | PRSCH2  | PRS Channel 2 selected  |
| 3     | PRSCH3  | PRS Channel 3 selected  |
| 4     | PRSCH4  | PRS Channel 4 selected  |
| 5     | PRSCH5  | PRS Channel 5 selected  |
| 6     | PRSCH6  | PRS Channel 6 selected  |
| 7     | PRSCH7  | PRS Channel 7 selected  |
| 8     | PRSCH8  | PRS Channel 8 selected  |
| 9     | PRSCH9  | PRS Channel 9 selected  |
| 10    | PRSCH10 | PRS Channel 10 selected |
| 11    | PRSCH11 | PRS Channel 11 selected |

|     |          |   |  |  |
|-----|----------|---|--|--|
| 5:0 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |  |
|-----|----------|---|--|--|

### 16.5.9 PRS\_DMAREQ1 - DMA Request 1 Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |       |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x038         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17    | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0   |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    | RW    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    | PRSEL |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset   | Access | Description |
|-------|----------|---|--------|-------------|
| 31:10 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |             |

| Bit | Name  | Reset   | Access                  | Description  |
|-----|-------|---------|-------------------------|--|
| 9:6 | PRSEL | 0x0     | RW                      | <b>DMA Request 1 PRS Channel Select</b><br>Selects PRS channel for DMA request 1 from the PRS (PRSREQ1). |
|     | Value | Mode    | Description             |  |
|     | 0     | PRSCH0  | PRS Channel 0 selected  |  |
|     | 1     | PRSCH1  | PRS Channel 1 selected  |  |
|     | 2     | PRSCH2  | PRS Channel 2 selected  |  |
|     | 3     | PRSCH3  | PRS Channel 3 selected  |  |
|     | 4     | PRSCH4  | PRS Channel 4 selected  |  |
|     | 5     | PRSCH5  | PRS Channel 5 selected  |  |
|     | 6     | PRSCH6  | PRS Channel 6 selected  |  |
|     | 7     | PRSCH7  | PRS Channel 7 selected  |  |
|     | 8     | PRSCH8  | PRS Channel 8 selected  |  |
|     | 9     | PRSCH9  | PRS Channel 9 selected  |  |
|     | 10    | PRSCH10 | PRS Channel 10 selected |  |
|     | 11    | PRSCH11 | PRS Channel 11 selected |  |

|     |          |   |  |  |
|-----|----------|---|--|--|
| 5:0 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |  |
|-----|----------|---|--|--|

16.5.10 PRS\_PEEK - PRS Channel Values

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |         |        |        |        |        |        |        |        |        |        |        |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|---------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x040         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11      | 10      | 9      | 8      | 7      | 6      | 5      | 4      | 3      | 2      | 1      | 0      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       | 0       | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R       | R       | R      | R      | R      | R      | R      | R      | R      | R      | R      | R      | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CH11VAL | CH10VAL | CH9VAL | CH8VAL | CH7VAL | CH6VAL | CH5VAL | CH4VAL | CH3VAL | CH2VAL | CH1VAL | CH0VAL |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name                  | Reset   | Access | Description                     |
|-------|-----------------------|---|--------|---------------------------------|
| 31:12 | Reserved              | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |                                 |
| 11    | CH11VAL<br>See bit 0. | 0   | R      | <b>Channel 11 Current Value</b> |
| 10    | CH10VAL<br>See bit 0. | 0   | R      | <b>Channel 10 Current Value</b> |
| 9     | CH9VAL<br>See bit 0.  | 0   | R      | <b>Channel 9 Current Value</b>  |
| 8     | CH8VAL<br>See bit 0.  | 0   | R      | <b>Channel 8 Current Value</b>  |
| 7     | CH7VAL<br>See bit 0.  | 0   | R      | <b>Channel 7 Current Value</b>  |
| 6     | CH6VAL<br>See bit 0.  | 0   | R      | <b>Channel 6 Current Value</b>  |
| 5     | CH5VAL<br>See bit 0.  | 0   | R      | <b>Channel 5 Current Value</b>  |
| 4     | CH4VAL<br>See bit 0.  | 0   | R      | <b>Channel 4 Current Value</b>  |
| 3     | CH3VAL<br>See bit 0.  | 0   | R      | <b>Channel 3 Current Value</b>  |
| 2     | CH2VAL<br>See bit 0.  | 0   | R      | <b>Channel 2 Current Value</b>  |
| 1     | CH1VAL<br>See bit 0.  | 0   | R      | <b>Channel 1 Current Value</b>  |
| 0     | CH0VAL                | 0   | R      | <b>Channel 0 Current Value</b>  |

When ASYNC = 0, sample the current output value of channel 0. Any enabled edge detection will not be visible. This value may be one or two clock delayed. When ASYNC = 1, no value is returned

### 16.5.11 PRS\_CHx\_CTRL - Channel Control Register

| Offset        | Bit Position |       |    |         |        |     |         |    |    |    |    |       |    |    |    |    |    |    |    |    |    |           |   |   |   |   |   |   |   |   |        |     |
|---------------|--------------|-------|----|---------|--------|-----|---------|----|----|----|----|-------|----|----|----|----|----|----|----|----|----|-----------|---|---|---|---|---|---|---|---|--------|-----|
| 0x050         | 31           | 30    | 29 | 28      | 27     | 26  | 25      | 24 | 23 | 22 | 21 | 20    | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10        | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1      | 0   |
| <b>Reset</b>  |              | 0     |    | 0       | 0      | 0   | 0       |    |    |    |    | 0x0   |    |    |    |    |    |    |    |    |    | 0x00      |   |   |   |   |   |   |   |   |        | 0x0 |
| <b>Access</b> |              | RW    |    | RW      | RW     | RW  | RW      |    |    |    |    | RW    |    |    |    |    |    |    |    |    |    | RW        |   |   |   |   |   |   |   |   |        | RW  |
| <b>Name</b>   |              | ASYNC |    | ANDNEXT | ORPREV | INV | STRETCH |    |    |    |    | EDSEL |    |    |    |    |    |    |    |    |    | SOURCESEL |   |   |   |   |   |   |   |   | SIGSEL |     |

| Bit   | Name     | Reset  | Access  | Description   |
|-------|----------|--|---|---|
| 31    | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |   |   |
| 30    | ASYNC    | 0  | RW  | <b>Asynchronous Reflex</b><br>Set to enable asynchronous mode of this reflex signal                               |
| 29    | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |   |   |
| 28    | ANDNEXT  | 0  | RW  | <b>And Next</b><br>If set, channel output is AND'ed with the next channel output                                  |
| 27    | ORPREV   | 0  | RW  | <b>Or Previous</b><br>If set, channel output is OR'ed with the previous channel output                            |
| 26    | INV      | 0  | RW  | <b>Invert Channel</b><br>If set, channel output is inverted   |
| 25    | STRETCH  | 0  | RW  | <b>Stretch Channel Output</b><br>If set, stretches channel output to ensure that the target clock domain sees it. |
| 24:22 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |   |   |
| 21:20 | EDSEL    | 0x0  | RW  | <b>Edge Detect Select</b><br>Select edge detection.   |
|       | Value    | Mode   | Description   |   |
|       | 0        | OFF  | Signal is left as it is   |   |
|       | 1        | POSEDGE  | A one HFCLK cycle pulse is generated for every positive edge of the incoming signal       |   |
|       | 2        | NEGEDGE  | A one HFCLK clock cycle pulse is generated for every negative edge of the incoming signal |   |
|       | 3        | BOTHEDGES  | A one HFCLK clock cycle pulse is generated for every edge of the incoming signal          |   |
| 19:15 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |   |   |

| Bit  | Name               | Reset   | Access | Description  |
|------|--------------------|---|--------|--|
| 14:8 | SOURCESEL          | 0x00  | RW     | <b>Source Select</b><br>Select input source to PRS channel.  |
|      | Value              | Mode  |        | Description  |
|      | 0b0000000          | NONE  |        | No source selected   |
|      | 0b0000001          | PRSL  |        | Peripheral Reflex System   |
|      | 0b0000010          | PRSH  |        | Peripheral Reflex System   |
|      | 0b0000011          | ACMP0   |        | Analog Comparator 0  |
|      | 0b0000100          | ACMP1   |        | Analog Comparator 1  |
|      | 0b0000101          | ADC0  |        | Analog to Digital Converter 0  |
|      | 0b0000111          | LESENSEL  |        | Low Energy Sensor Interface  |
|      | 0b0001000          | LESENSEH  |        | Low Energy Sensor Interface  |
|      | 0b0001001          | LESENSED  |        | Low Energy Sensor Interface  |
|      | 0b0001010          | LESENSE   |        | Low Energy Sensor Interface  |
|      | 0b0001011          | RTCC  |        | Real-Time Counter and Calendar   |
|      | 0b0001100          | GPIOL   |        | General purpose Input/Output   |
|      | 0b0001101          | GPIOH   |        | General purpose Input/Output   |
|      | 0b0001110          | LETIMER0  |        | Low Energy Timer 0   |
|      | 0b0001111          | PCNT0   |        | Pulse Counter 0  |
|      | 0b0010010          | CMU   |        | Clock Management Unit  |
|      | 0b0011000          | VDAC0   |        | Digital to Analog Converter 0  |
|      | 0b0011010          | CRYOTIMER   |        | CRYOTIMER  |
|      | 0b0110000          | USART0  |        | Universal Synchronous/Asynchronous Receiver/Transmitter 0  |
|      | 0b0110001          | USART1  |        | Universal Synchronous/Asynchronous Receiver/Transmitter 1  |
|      | 0b0110010          | USART2  |        | Universal Synchronous/Asynchronous Receiver/Transmitter 2  |
|      | 0b0111100          | TIMER0  |        | Timer 0  |
|      | 0b0111101          | TIMER1  |        | Timer 1  |
|      | 0b0111110          | WTIMER0   |        | Wide Timer 0   |
|      | 0b1000011          | CM4   |        |  |
| 7:3  | <i>Reserved</i>    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 2:0  | SIGSEL             | 0x0   | RW     | <b>Signal Select</b><br>Select signal input to PRS channel. Selected signal depends on SOURCESEL as indicated. |
|      | Value              | Mode  |        | Description  |
|      | <i>SOURCESEL =</i> | <i>0b000000</i>   |        | <i>(NONE)</i>  |
|      | 0bxxx              | OFF   |        | Channel input selection is turned off  |
|      | <i>SOURCESEL =</i> | <i>0b0000001</i>  |        | <i>(PRSL)</i>  |

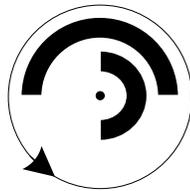
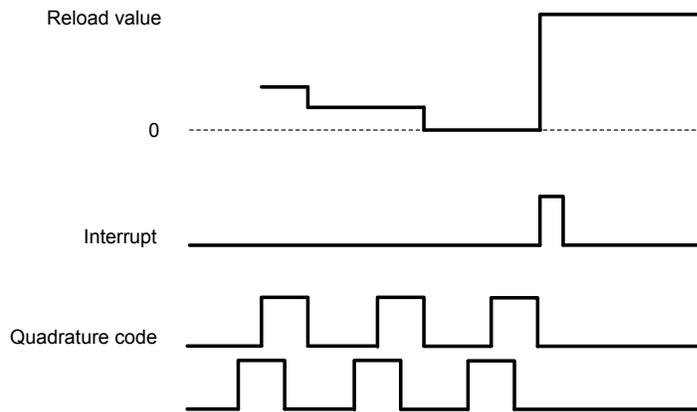
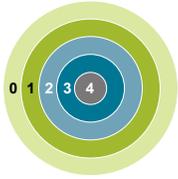
| Bit                | Name             | Reset           | Access | Description  |
|--------------------|------------------|-----------------|--------|--|
| 0b000              |                  | PRSCH0          |        | PRS channel 0 PRSCH0 (Asynchronous)                            |
| 0b001              |                  | PRSCH1          |        | PRS channel 1 PRSCH1 (Asynchronous)                            |
| 0b010              |                  | PRSCH2          |        | PRS channel 2 PRSCH2 (Asynchronous)                            |
| 0b011              |                  | PRSCH3          |        | PRS channel 3 PRSCH3 (Asynchronous)                            |
| 0b100              |                  | PRSCH4          |        | PRS channel 4 PRSCH4 (Asynchronous)                            |
| 0b101              |                  | PRSCH5          |        | PRS channel 5 PRSCH5 (Asynchronous)                            |
| 0b110              |                  | PRSCH6          |        | PRS channel 6 PRSCH6 (Asynchronous)                            |
| 0b111              |                  | PRSCH7          |        | PRS channel 7 PRSCH7 (Asynchronous)                            |
| <i>SOURCESEL =</i> | <i>0b0000010</i> |                 |        | <i>(PRSH)</i>  |
| 0b000              |                  | PRSCH8          |        | PRS channel 8 PRSCH8 (Asynchronous)                            |
| 0b001              |                  | PRSCH9          |        | PRS channel 9 PRSCH9 (Asynchronous)                            |
| 0b010              |                  | PRSCH10         |        | PRS channel 10 PRSCH10 (Asynchronous)                          |
| 0b011              |                  | PRSCH11         |        | PRS channel 11 PRSCH11 (Asynchronous)                          |
| <i>SOURCESEL =</i> | <i>0b0000011</i> |                 |        | <i>(ACMP0)</i>   |
| 0b000              |                  | ACMP0OUT        |        | Analog comparator output ACMP0OUT (Asynchronous)               |
| <i>SOURCESEL =</i> | <i>0b0000100</i> |                 |        | <i>(ACMP1)</i>   |
| 0b000              |                  | ACMP1OUT        |        | Analog comparator output ACMP1OUT (Asynchronous)               |
| <i>SOURCESEL =</i> | <i>0b0000101</i> |                 |        | <i>(ADC0)</i>  |
| 0b000              |                  | ADC0SINGLE      |        | ADC single conversion done ADC0SINGLE (Asynchronous)           |
| 0b001              |                  | ADC0SCAN        |        | ADC scan conversion done ADC0SCAN (Asynchronous)               |
| <i>SOURCESEL =</i> | <i>0b0000111</i> |                 |        | <i>(LESENSEL)</i>  |
| 0b000              |                  | LESENSESCANRES0 |        | LESENSE SCANRES register, bit 0 LESENSESCANRES0 (Asynchronous) |
| 0b001              |                  | LESENSESCANRES1 |        | LESENSE SCANRES register, bit 1 LESENSESCANRES1 (Asynchronous) |
| 0b010              |                  | LESENSESCANRES2 |        | LESENSE SCANRES register, bit 2 LESENSESCANRES2 (Asynchronous) |
| 0b011              |                  | LESENSESCANRES3 |        | LESENSE SCANRES register, bit 3 LESENSESCANRES3 (Asynchronous) |
| 0b100              |                  | LESENSESCANRES4 |        | LESENSE SCANRES register, bit 4 LESENSESCANRES4 (Asynchronous) |
| 0b101              |                  | LESENSESCANRES5 |        | LESENSE SCANRES register, bit 5 LESENSESCANRES5 (Asynchronous) |
| 0b110              |                  | LESENSESCANRES6 |        | LESENSE SCANRES register, bit 6 LESENSESCANRES6 (Asynchronous) |
| 0b111              |                  | LESENSESCANRES7 |        | LESENSE SCANRES register, bit 7 LESENSESCANRES7 (Asynchronous) |
| <i>SOURCESEL =</i> | <i>0b0001000</i> |                 |        | <i>(LESENSEH)</i>  |
| 0b000              |                  | LESENSESCANRES8 |        | LESENSE SCANRES register, bit 8 LESENSESCANRES8 (Asynchronous) |

| Bit                | Name             | Reset            | Access | Description  |
|--------------------|------------------|------------------|--------|--|
| 0b001              |                  | LESENSESCANRES9  |        | LESENSE SCANRES register, bit 9 LESENSESCANRES9 (Asynchronous)               |
| 0b010              |                  | LESENSESCANRES10 |        | LESENSE SCANRES register, bit 10 LESENSESCANRES10 (Asynchronous)             |
| 0b011              |                  | LESENSESCANRES11 |        | LESENSE SCANRES register, bit 11 LESENSESCANRES11 (Asynchronous)             |
| 0b100              |                  | LESENSESCANRES12 |        | LESENSE SCANRES register, bit 12 LESENSESCANRES12 (Asynchronous)             |
| 0b101              |                  | LESENSESCANRES13 |        | LESENSE SCANRES register, bit 13 LESENSESCANRES13 (Asynchronous)             |
| 0b110              |                  | LESENSESCANRES14 |        | LESENSE SCANRES register, bit 14 LESENSESCANRES14 (Asynchronous)             |
| 0b111              |                  | LESENSESCANRES15 |        | LESENSE SCANRES register, bit 15 LESENSESCANRES15 (Asynchronous)             |
| <i>SOURCESEL =</i> | <i>0b0001001</i> |                  |        | <i>(LESENSED)</i>  |
| 0b000              |                  | LESENSEDEC0      |        | LESENSE Decoder PRS out 0 LESENSEDEC0 (Asynchronous)                         |
| 0b001              |                  | LESENSEDEC1      |        | LESENSE Decoder PRS out 1 LESENSEDEC1 (Asynchronous)                         |
| 0b010              |                  | LESENSEDEC2      |        | LESENSE Decoder PRS out 2 LESENSEDEC2 (Asynchronous)                         |
| 0b011              |                  | LESENSEDECAMP    |        | LESENSE Decoder PRS compare value match channel LESENSEDECAMP (Asynchronous) |
| <i>SOURCESEL =</i> | <i>0b0001010</i> |                  |        | <i>(LESENSE)</i>   |
| 0b000              |                  | LESENSEMEASACT   |        | LESENSE Measurement active LESENSEMEASACT (Asynchronous)                     |
| <i>SOURCESEL =</i> | <i>0b0001011</i> |                  |        | <i>(RTCC)</i>  |
| 0b001              |                  | RTCCCV0          |        | RTCC Compare 0 RTCCCV0 (Asynchronous)  |
| 0b010              |                  | RTCCCV1          |        | RTCC Compare 1 RTCCCV1 (Asynchronous)  |
| 0b011              |                  | RTCCCV2          |        | RTCC Compare 2 RTCCCV2 (Asynchronous)  |
| <i>SOURCESEL =</i> | <i>0b0001100</i> |                  |        | <i>(GPIOIOL)</i>   |
| 0b000              |                  | GPIOPIN0         |        | GPIO pin 0 GPIOPIN0 (Asynchronous)   |
| 0b001              |                  | GPIOPIN1         |        | GPIO pin 1 GPIOPIN1 (Asynchronous)   |
| 0b010              |                  | GPIOPIN2         |        | GPIO pin 2 GPIOPIN2 (Asynchronous)   |
| 0b011              |                  | GPIOPIN3         |        | GPIO pin 3 GPIOPIN3 (Asynchronous)   |
| 0b100              |                  | GPIOPIN4         |        | GPIO pin 4 GPIOPIN4 (Asynchronous)   |
| 0b101              |                  | GPIOPIN5         |        | GPIO pin 5 GPIOPIN5 (Asynchronous)   |
| 0b110              |                  | GPIOPIN6         |        | GPIO pin 6 GPIOPIN6 (Asynchronous)   |
| 0b111              |                  | GPIOPIN7         |        | GPIO pin 7 GPIOPIN7 (Asynchronous)   |
| <i>SOURCESEL =</i> | <i>0b0001101</i> |                  |        | <i>(GPIOH)</i>   |
| 0b000              |                  | GPIOPIN8         |        | GPIO pin 8 GPIOPIN8 (Asynchronous)   |
| 0b001              |                  | GPIOPIN9         |        | GPIO pin 9 GPIOPIN9 (Asynchronous)   |
| 0b010              |                  | GPIOPIN10        |        | GPIO pin 10 GPIOPIN10 (Asynchronous)   |
| 0b011              |                  | GPIOPIN11        |        | GPIO pin 11 GPIOPIN11 (Asynchronous)   |

| Bit                | Name | Reset            | Access | Description   |
|--------------------|------|------------------|--------|---|
| 0b100              |      | GPIOPIN12        |        | GPIO pin 12 GPIOPIN12 (Asynchronous)  |
| 0b101              |      | GPIOPIN13        |        | GPIO pin 13 GPIOPIN13 (Asynchronous)  |
| 0b110              |      | GPIOPIN14        |        | GPIO pin 14 GPIOPIN14 (Asynchronous)  |
| 0b111              |      | GPIOPIN15        |        | GPIO pin 15 GPIOPIN15 (Asynchronous)  |
| <i>SOURCESEL =</i> |      | <i>0b0001110</i> |        | <i>(LETIMER0)</i>   |
| 0b000              |      | LETIMER0CH0      |        | LETIMER CH0 Out LETIMER0CH0 (Asynchronous)  |
| 0b001              |      | LETIMER0CH1      |        | LETIMER CH1 Out LETIMER0CH1 (Asynchronous)  |
| <i>SOURCESEL =</i> |      | <i>0b0001111</i> |        | <i>(PCNT0)</i>  |
| 0b000              |      | PCNT0TCC         |        | PCNT0 Triggered compare match PCNT0TCC (Asynchronous)   |
| 0b001              |      | PCNT0UFOF        |        | PCNT0 Counter overflow or underflow PCNT0UFOF (Asynchronous)                                  |
| 0b010              |      | PCNT0DIR         |        | PCNT0 Counter direction PCNT0DIR (Asynchronous)   |
| <i>SOURCESEL =</i> |      | <i>0b0010010</i> |        | <i>(CMU)</i>  |
| 0b000              |      | CMUCLKOUT0       |        | Clock Output 0 CMUCLKOUT0 (Asynchronous)  |
| 0b001              |      | CMUCLKOUT1       |        | Clock Output 1 CMUCLKOUT1 (Asynchronous)  |
| <i>SOURCESEL =</i> |      | <i>0b0011000</i> |        | <i>(VDAC0)</i>  |
| 0b000              |      | VDAC0CH0         |        | DAC ch0 conversion done VDAC0CH0  |
| 0b001              |      | VDAC0CH1         |        | DAC ch1 conversion done VDAC0CH1  |
| 0b010              |      | VDAC0OPA0        |        | OPA0 warmedup or outputvalid based on OPA0PRSOUMODE mode in OPACTRL. VDAC0OPA0 (Asynchronous) |
| 0b011              |      | VDAC0OPA1        |        | OPA1 warmedup or outputvalid based on OPA1PRSOUMODE mode in OPACTRL. VDAC0OPA1 (Asynchronous) |
| 0b100              |      | VDAC0OPA2        |        | OPA2 warmedup or outputvalid based on OPA2PRSOUMODE mode in OPACTRL. VDAC0OPA2 (Asynchronous) |
| <i>SOURCESEL =</i> |      | <i>0b0011010</i> |        | <i>(CRYOTIMER)</i>  |
| 0b000              |      | CRYOTIMERPERIOD  |        | CRYOTIMER Output CRYOTIMERPERIOD (Asynchronous)   |
| <i>SOURCESEL =</i> |      | <i>0b0110000</i> |        | <i>(USART0)</i>   |
| 0b000              |      | USART0IRTX       |        | USART 0 IRDA out USART0IRTX   |
| 0b001              |      | USART0TXC        |        | USART 0 TX complete USART0TXC   |
| 0b010              |      | USART0RXDATAV    |        | USART 0 RX Data Valid USART0RXDATAV   |
| 0b011              |      | USART0RTS        |        | USART 0 RTS USART0RTS   |
| 0b101              |      | USART0TX         |        | USART 0 TX USART0TX   |
| 0b110              |      | USART0CS         |        | USART 0 CS USART0CS   |
| <i>SOURCESEL =</i> |      | <i>0b0110001</i> |        | <i>(USART1)</i>   |
| 0b001              |      | USART1TXC        |        | USART 1 TX complete USART1TXC   |
| 0b010              |      | USART1RXDATAV    |        | USART 1 RX Data Valid USART1RXDATAV   |
| 0b011              |      | USART1RTS        |        | USART 1 RTS USART1RTS   |
| 0b101              |      | USART1TX         |        | USART 1 TX USART1TX   |
| 0b110              |      | USART1CS         |        | USART 1 CS USART1CS   |

| Bit   | Name               | Reset                | Access | Description                                |
|-------|--------------------|----------------------|--------|--|
|       | <i>SOURCESEL =</i> | <i>0b0110010</i>     |        | <i>(USART2)</i>                            |
| 0b000 |                    | USART2IRTX           |        | USART 2 IRDA out USART2IRTX (Asynchronous) |
| 0b001 |                    | USART2TXC            |        | USART 2 TX complete USART2TXC              |
| 0b010 |                    | USART2RXDATAV        |        | USART 2 RX Data Valid USART2RXDATAV        |
| 0b011 |                    | USART2RTS            |        | USART 2 RTS USART2RTS                      |
| 0b101 |                    | USART2TX             |        | USART 2 TX USART2TX                        |
| 0b110 |                    | USART2CS             |        | USART 2 CS USART2CS                        |
|       | <i>SOURCESEL =</i> | <i>0b0111100</i>     |        | <i>(TIMER0)</i>                            |
| 0b000 |                    | TIMER0UF             |        | Timer 0 Underflow TIMER0UF                 |
| 0b001 |                    | TIMER0OF             |        | Timer 0 Overflow TIMER0OF                  |
| 0b010 |                    | TIMER0CC0            |        | Timer 0 Compare/Capture 0 TIMER0CC0        |
| 0b011 |                    | TIMER0CC1            |        | Timer 0 Compare/Capture 1 TIMER0CC1        |
| 0b100 |                    | TIMER0CC2            |        | Timer 0 Compare/Capture 2 TIMER0CC2        |
|       | <i>SOURCESEL =</i> | <i>0b0111101</i>     |        | <i>(TIMER1)</i>                            |
| 0b000 |                    | TIMER1UF             |        | Timer 1 Underflow TIMER1UF                 |
| 0b001 |                    | TIMER1OF             |        | Timer 1 Overflow TIMER1OF                  |
| 0b010 |                    | TIMER1CC0            |        | Timer 1 Compare/Capture 0 TIMER1CC0        |
| 0b011 |                    | TIMER1CC1            |        | Timer 1 Compare/Capture 1 TIMER1CC1        |
| 0b100 |                    | TIMER1CC2            |        | Timer 1 Compare/Capture 2 TIMER1CC2        |
| 0b101 |                    | TIMER1CC3            |        | Timer 1 Compare/Capture 3 TIMER1CC3        |
|       | <i>SOURCESEL =</i> | <i>0b0111110</i>     |        | <i>(WTIMER0)</i>                           |
| 0b000 |                    | WTIMER0UF            |        | Timer 2 Underflow WTIMER0UF                |
| 0b001 |                    | WTIMER0OF            |        | Timer 2 Overflow WTIMER0OF                 |
| 0b010 |                    | WTIMER0CC0           |        | Timer 2 Compare/Capture 0 WTIMER0CC0       |
| 0b011 |                    | WTIMER0CC1           |        | Timer 2 Compare/Capture 1 WTIMER0CC1       |
| 0b100 |                    | WTIMER0CC2           |        | Timer 2 Compare/Capture 2 WTIMER0CC2       |
|       | <i>SOURCESEL =</i> | <i>0b1000011</i>     |        | <i>(CM4)</i>                               |
| 0b000 |                    | CM4TXEV              |        | CM4TXEV                                    |
| 0b001 |                    | CM4ICACHEPCHIT-SOF   |        | CM4ICACHEPCHITSOF                          |
| 0b010 |                    | CM4ICACHEPCMISSE-SOF |        | CM4ICACHEPCMISSESOF                        |

## 17. PCNT - Pulse Counter



### Quick Facts

#### What?

The Pulse Counter (PCNT) decodes incoming pulses. The module has a quadrature mode which may be used to decode the speed and direction of a mechanical shaft. PCNT can operate in EM0 Active down to EM3 Stop.

#### Why?

The PCNT generates an interrupt after a specific number of pulses (or rotations), eliminating the need for timing or I/O interrupts and CPU processing to measure pulse widths, etc.

#### How?

PCNT uses the LFACLK or may be externally clocked from a pin. The module incorporates a 16-bit up/down-counter to keep track of incoming pulses or rotations.

### 17.1 Introduction

The Pulse Counter (PCNT) can be used for counting incoming pulses on a single input or to decode quadrature encoded inputs in EM0 Active down to EM3 Stop. It can run from the internal LFACLK while counting pulses on the PCNTn\_S0IN pin. Or, alternately, the PCNTn\_S0IN pin may be used as an external clock source that runs both the PCNT counter and register access.

### 17.2 Features

- 16-bit counter with reload register
- Auxiliary counter for counting a single direction
- Single input oversampling up/down counter mode
- Externally clocked single input pulse up/down counter mode
- Quadrature decoder modes
  - Externally clocked quadrature decoder 1X mode
  - Oversampling quadrature decoder 1X, 2X and 4X modes
- Interrupt on counter underflow and overflow
- Interrupt when a direction change is detected (quadrature decoder mode only)
- Optional pulse width filter
- Optional input inversion/edge detect select
- Optional inputs from PRS
- Asynchronously triggered compare and clear

## 17.3 Functional Description

An overview of the PCNT module is shown in [Figure 17.1 PCNT Overview](#) on page 488.

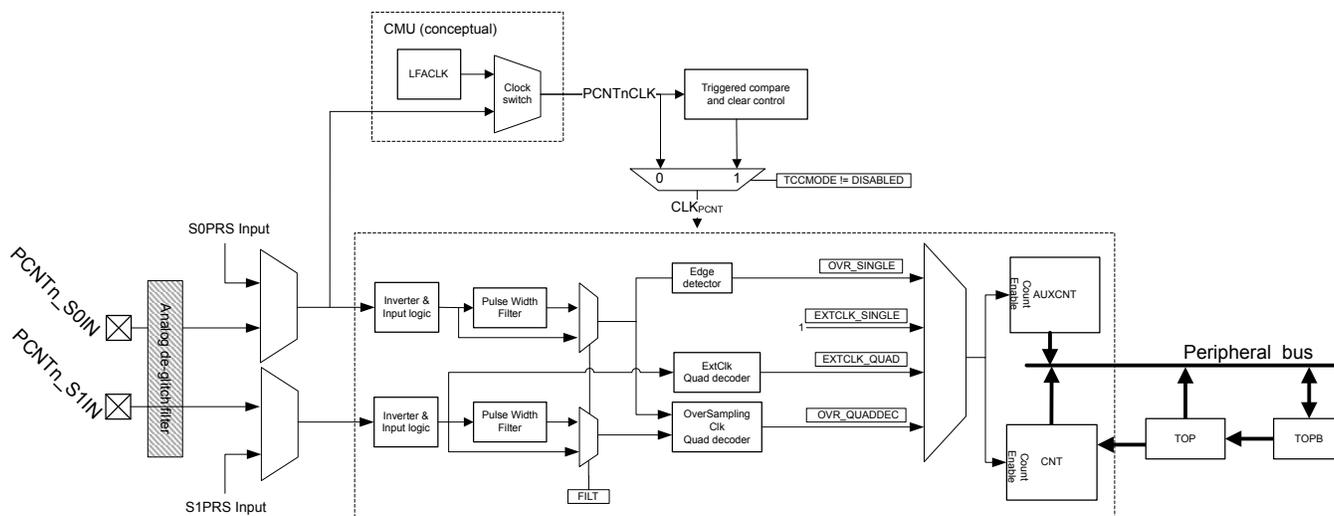


Figure 17.1. PCNT Overview

### 17.3.1 Pulse Counter Modes

The pulse counter can operate in single input oversampling mode (OVSSINGLE), externally clocked single input counter mode (EXTCLKSINGLE), externally clocked quadrature decoder mode (EXTCLKQUAD) and oversampling quadrature decoder modes (OVSQUAD1X, OVSQUAD2X and OVSQUAD4X). The following sections describe operation of each of these modes and how they are enabled. Input timing constraints are described in [17.3.6 Clock Sources](#) and [17.3.7 Input Filter](#).

#### 17.3.1.1 Single Input Oversampling Mode

This mode is enabled by writing OVSSINGLE to the MODE field in the PCNTn\_CTRL register and disabled by writing DISABLE to the same field. The LFACLK clock source to the pulse counter is configured by clearing PCNT0CLKSEL in the CMU\_PCNTCTRL in the Clock Management Unit (CMU) [12.5.43 CMU\\_PCNTCTRL - PCNT Control Register](#).

The optional pulse width filter is enabled by setting the FILT bit in the PCNTn\_CTRL register. Additionally, the PCNTn\_S0IN input may be inverted, so that falling edges are counted, by setting the EDGE bit in the PCNTn\_CTRL register.

If S1CDIR in the PCNTn\_CTRL register is cleared, PCNTn\_S0IN is the only observed input in this mode. The PCNTn\_S0IN input is sampled by the LFACLK and the number of detected positive or negative edges on PCNTn\_S0IN appears in PCNTn\_CNT. The counter may be configured to count down by setting the CNTDIR bit in PCNTn\_CTRL. Default is to count up.

The counting direction can also be controlled externally in this mode by setting S1CDIR. This will make the input value on PCNTn\_S1IN decide the direction counted on a PCNTn\_S0IN edge. If PCNTn\_S1IN is high, the count is done according to CNTDIR in PCNTn\_CTRL. If low, the count direction is opposite.

#### 17.3.1.2 Externally Clocked Single Input Counter Mode

This mode is enabled by writing EXTCLKSINGLE to the MODE field in the PCNTn\_CTRL register and disabled by writing DISABLE to the same field. The external pin clock source is configured by setting PCNT0CLKSEL in the CMU\_PCNTCTRL register ([12. CMU - Clock Management Unit](#)).

Positive edges on PCNTn\_S0IN are used to clock the counter. Similar to the oversampled mode, PCNTn\_S1IN is used to determine the count direction if S1CDIR is set. If not, CNTDIR in PCNTn\_CTRL solely defines count direction.

The digital pulse width filter is not available in this mode. The analog de-glitch filter in the GPIO pads is capable of removing some unwanted noise. However, this mode may be susceptible to spikes and unintended pulses from devices such as mechanical switches, and is therefore most suited to take input from electronic sensors etc. that generate single wire pulses.

### 17.3.1.3 Quadrature Decoder Modes

Two different types of quadrature decoding is supported in the pulse counter: the externally clocked (Asynchronous) quadrature decoding and the oversampling (Synchronous) quadrature decoding. The externally clocked mode supports 1X quadrature decoding whereas the oversampling mode supports 1X, 2X and 4X quadrature decoding. These modes are described in detail in [17.3.1.4 Externally Clocked Quadrature Decoder Mode](#) and [17.3.1.5 Oversampling Quadrature Decoder Mode](#) .

### 17.3.1.4 Externally Clocked Quadrature Decoder Mode

This mode is enabled by writing EXTCLKQUAD to the MODE field in PCNTn\_CTRL and disabled by writing DISABLE to the same field. The external pin clock source is configured by setting PCNT0CLKSEL in the CMU\_PCNTCTRL register (12. CMU - Clock Management Unit).

In this mode, both edges on PCNTn\_S0IN pin are used to sample PCNTn\_S1IN pin, in order to decode the quadrature code. A quadrature coded signal contains information about the relative speed and direction of a rotating shaft as illustrated by Figure 17.2 PCNT Quadrature Coding on page 490, hence the direction of the counter register PCNTn\_CNT is controlled automatically.

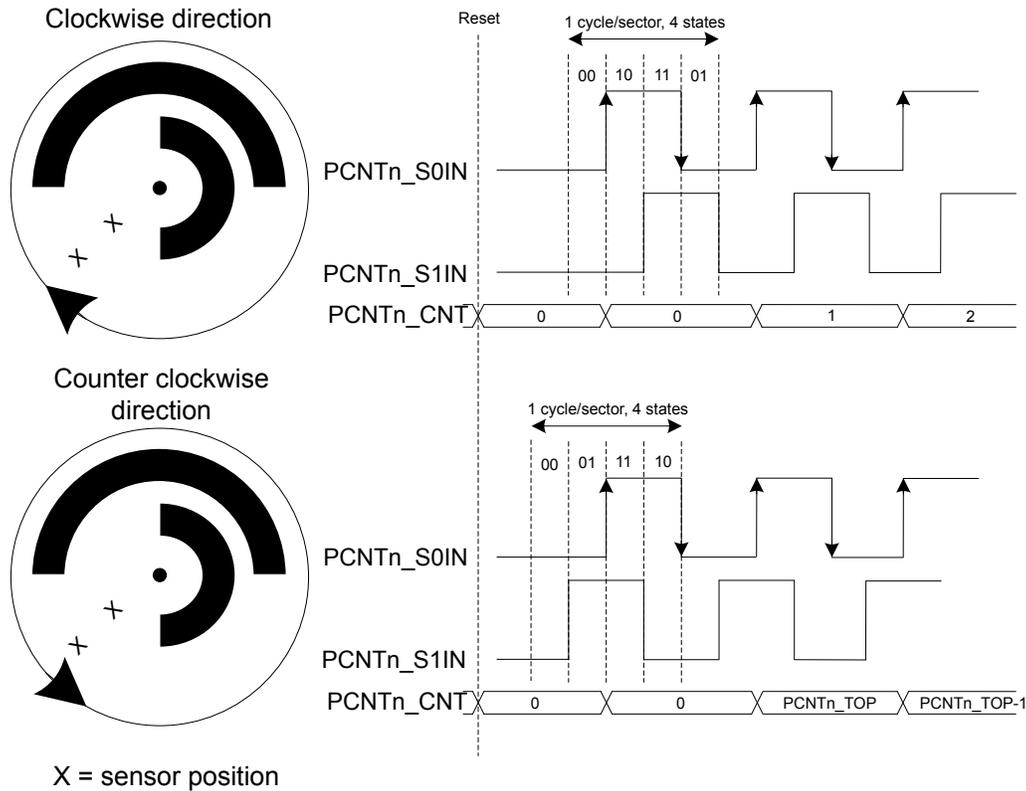


Figure 17.2. PCNT Quadrature Coding

If PCNTn\_S0IN leads PCNTn\_S1IN in phase, the direction is clockwise, and if it lags in phase the direction is counter-clockwise. Default behavior is illustrated by Figure 17.2 PCNT Quadrature Coding on page 490.

The counter direction may be read from the DIR bit in the PCNTn\_STATUS register. Additionally, the DIRCNG interrupt in the PCNTn\_IF register is generated when a direction change is detected. When a change is detected, the DIR bit in the PCNTn\_STATUS register must be read to determine the current new direction.

**Note:** The sector disc illustrated in the figure may be finer grained in some systems. Typically, they may generate 2-4 PCNTn\_S0IN wave periods per 360° rotation.

The direction of the quadrature code and control of the counter is generated by the simple binary function outlined by Table 17.1 PCNT QUAD Mode Counter Control Function on page 490. Note that this function also filters some invalid inputs that may occur when the shaft changes direction or temporarily toggles direction.

Table 17.1. PCNT QUAD Mode Counter Control Function

| Inputs       |              | Control/Status |                   |
|--------------|--------------|----------------|-------------------|
| S1IN posedge | S1IN negedge | Count Enable   | CNTDIR status bit |
| 0            | 0            | 0              | 0                 |

| Inputs       |              | Control/Status |                   |
|--------------|--------------|----------------|-------------------|
| S1IN posedge | S1IN negedge | Count Enable   | CNTDIR status bit |
| 0            | 1            | 1              | 0                 |
| 1            | 0            | 1              | 1                 |
| 1            | 1            | 0              | 0                 |

**Note:** PCNTn\_S1IN is sampled on both edges of PCNTn\_S0IN.

### 17.3.1.5 Oversampling Quadrature Decoder Mode

There are three Oversampling Quadrature Decoder Modes supported: 1X , 2X and 4X. These modes are enabled by writing OVSQUAD1X, OVSQUAD2X and OVSQUAD4X, respectively, to the MODE field in PCNTn\_CTRL and disabled by writing DISABLE to the same field. The LFACTK clock source to the pulse counter must be configured by clearing PCNT0CLKSEL in the CMU\_PCNTCTRL in the Clock Management Unit (CMU), [12. CMU - Clock Management Unit](#) .

The optional pulse width filter is enabled by setting the FILT bit in the PCNTn\_CTRL register. The filter applies to both inputs PCNTn\_S0IN and PCNTn\_S1IN. The filter length is configured by FILTLEN in PCNTn\_OVSCFG register.

Based on the modes selected, the decoder updates the counter on different events. In the OVSQUAD1X mode, the counter is updated on the rising edge of the PCNTn\_S0IN input when counting up, and on the negeedge of the PCNTn\_S0IN input when counting down. In the OVSQUAD2X mode, the counter is updated on both edges of PCNTn\_S0IN input. In the OVSQUAD4X mode the counter is updated on both edges of both inputs PCNTn\_S0IN and PCNTn\_S1IN. [Table 17.2 PCNT OVSQUAD 1X, 2X and 4X Mode Counter Control Function on page 492](#) outlines the increment or decrement of the counter based on the Quadrature Mode selected.

**Note:** The decoding behavior of OVSQUAD1X mode is slightly different compared to EXTCLKQUAD mode(also 1X mode). In the EXTCLKQUAD mode, the counter is updated only on the posedge of S0IN input. However, in the OVSQUAD1X mode, the counter is updated on the posedge of S0IN when counting up and on the negeedge of S0IN when counting down.

**Table 17.2. PCNT OVSQUAD 1X, 2X and 4X Mode Counter Control Function**

| Direction         | Previous State |      | Next State |      | OVSQUAD MODE |    |    |
|-------------------|----------------|------|------------|------|--------------|----|----|
|                   | S1IN           | S0IN | S1IN       | S0IN | 1X           | 2X | 4X |
| Clockwise         | 0              | 0    | 0          | 1    | +1           | +1 | +1 |
|                   | 0              | 1    | 1          | 1    |              |    | +1 |
|                   | 1              | 1    | 1          | 0    |              | +1 | +1 |
|                   | 1              | 0    | 0          | 0    |              |    | +1 |
| Counter Clockwise | 1              | 0    | 1          | 1    |              | -1 | -1 |
|                   | 1              | 1    | 0          | 1    |              |    | -1 |
|                   | 0              | 1    | 0          | 0    | -1           | -1 | -1 |
|                   | 0              | 0    | 1          | 0    |              |    | -1 |

[Figure 17.3 PCNT State Transitions for Different Oversampling Quadrature Decoder Modes on page 493](#) illustrates the different states of the quadrature input and the state transitions that updates the counter for the different modes. Each cycle of the input states results in 1 update, 2 updates and 4 updates of the counter for OVSQUAD1X, OVSQUAD2X and OVSQUAD4X modes respectively.

Relationship between inputs and its state

| STATE | S1IN | S0IN |
|-------|------|------|
| S0    | 0    | 0    |
| S1    | 0    | 1    |
| S2    | 1    | 1    |
| S3    | 1    | 0    |

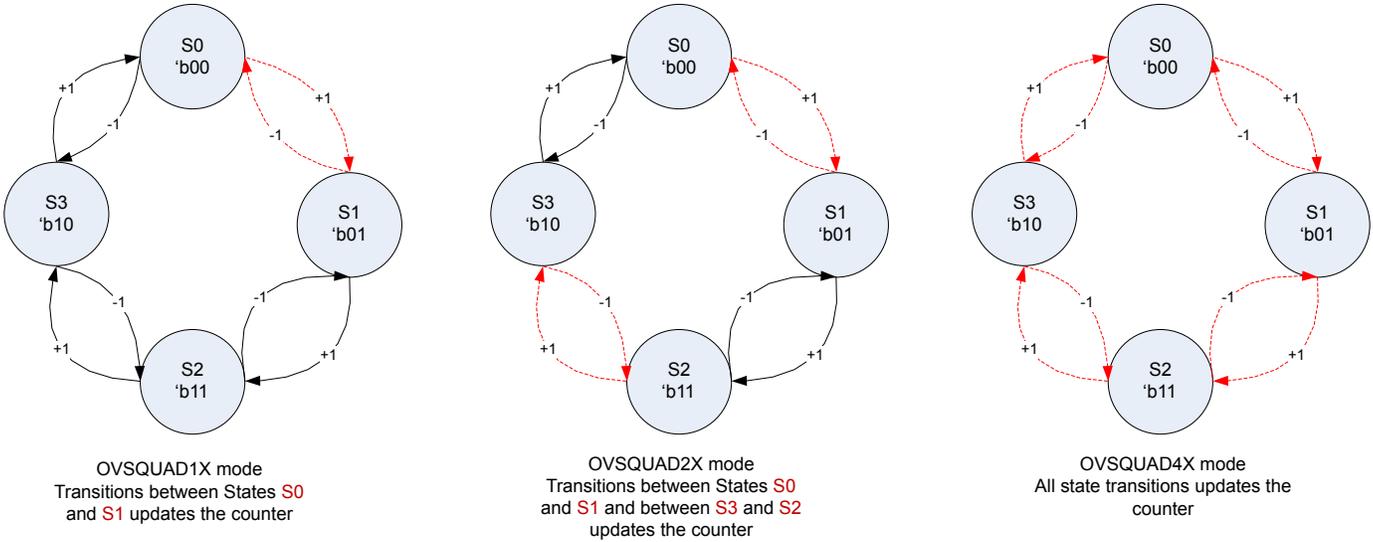


Figure 17.3. PCNT State Transitions for Different Oversampling Quadrature Decoder Modes

The counter direction can be read from the DIR bit in PCNTn\_STATUS register. Additionally, the DIRCNG interrupt in the PCNTn\_IF is generated when the direction change is detected. When a change is detected, the DIR bit in the PCNTn\_STATUS register must be read to determine the new direction.

In the oversampling quadrature decoder modes, the maximum input toggle frequency supported is 8KHz. For frequencies of 8KHz and higher, incorrect decoding occurs. The different decoding modes and the counter updates are further illustrated by Figure 17.4 PCNT Oversampling Quadrature Decoder 1X Mode on page 493, Figure 17.5 PCNT Oversampling Quadrature Decoder 2X Mode on page 494 and Figure 17.6 PCNT Oversampling Quadrature Decoder 4X Mode on page 494.

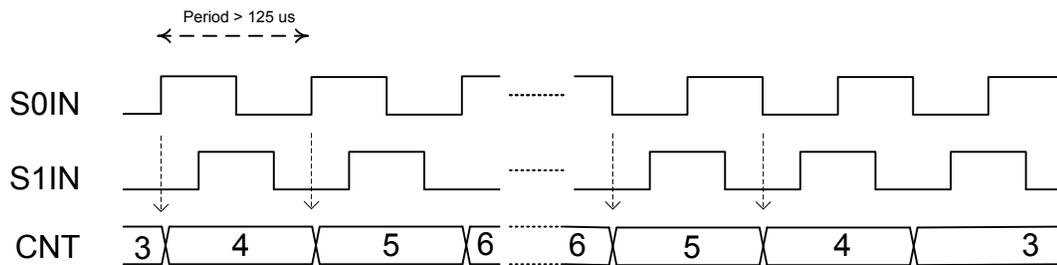


Figure 17.4. PCNT Oversampling Quadrature Decoder 1X Mode

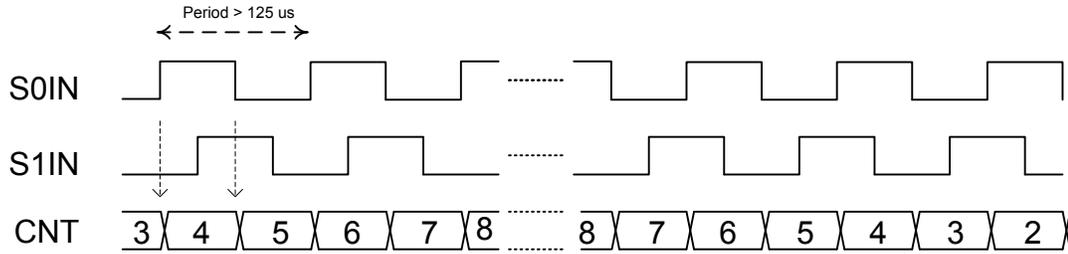


Figure 17.5. PCNT Oversampling Quadrature Decoder 2X Mode

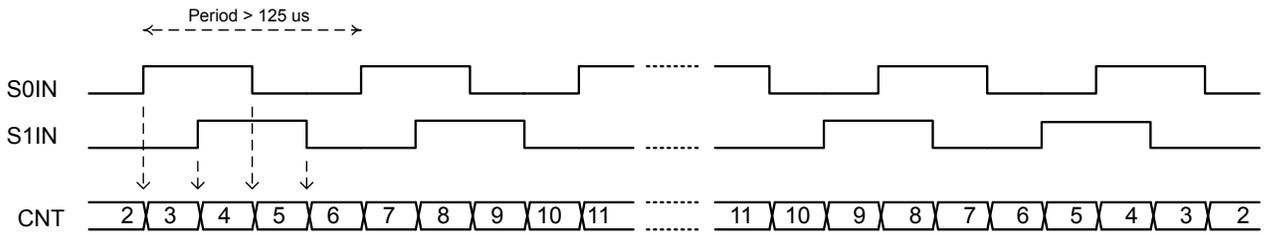


Figure 17.6. PCNT Oversampling Quadrature Decoder 4X Mode

The above modes, by default are prone to flutter effects in the inputs PCNTn\_S0IN and PCNTn\_S1IN. When this occurs, the counter changes directions rapidly causing DIRCNG interrupts and unnecessarily waking the core. To prevent this, set FLUTERRM in PCNTn\_OVSCFG register. When enabled, flutter is removed, thus preventing unnecessary wakeup of the core. The flutter removal logic works by preventing update of the counter value if the wheel keeps changing direction as a result of flutter. The counter is only updated if the current and previous state transition of the rotation are in the same direction. These state transitions are quadrature decoder mode specific. The highlighted state transitions in [Figure 17.3 PCNT State Transitions for Different Oversampling Quadrature Decoder Modes on page 493](#) are the ones considered for the different quadrature decoder modes. [Figure 17.7 PCNT Oversampling Quadrature Decoder with Flutter Removal on page 494](#) shows how the counter is updated for the different quadrature decoder modes with flutter removal FLUTERRM enabled in PCNTn\_OVSCFG.

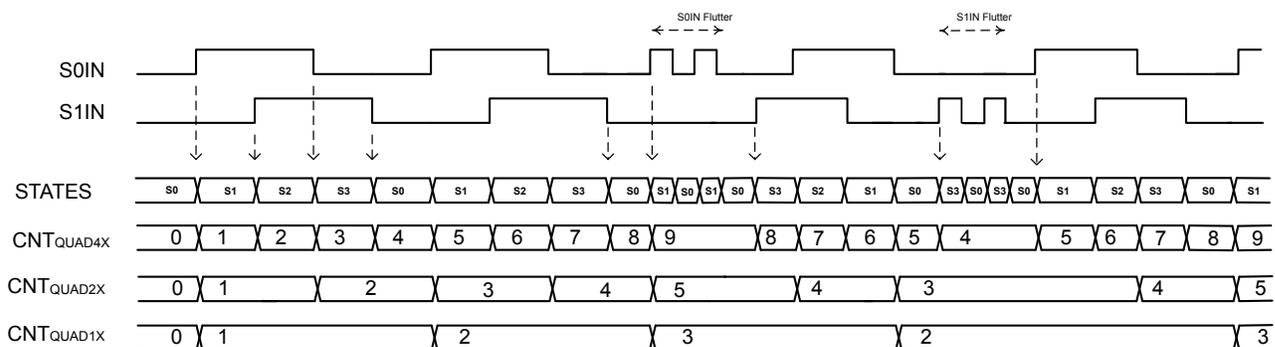
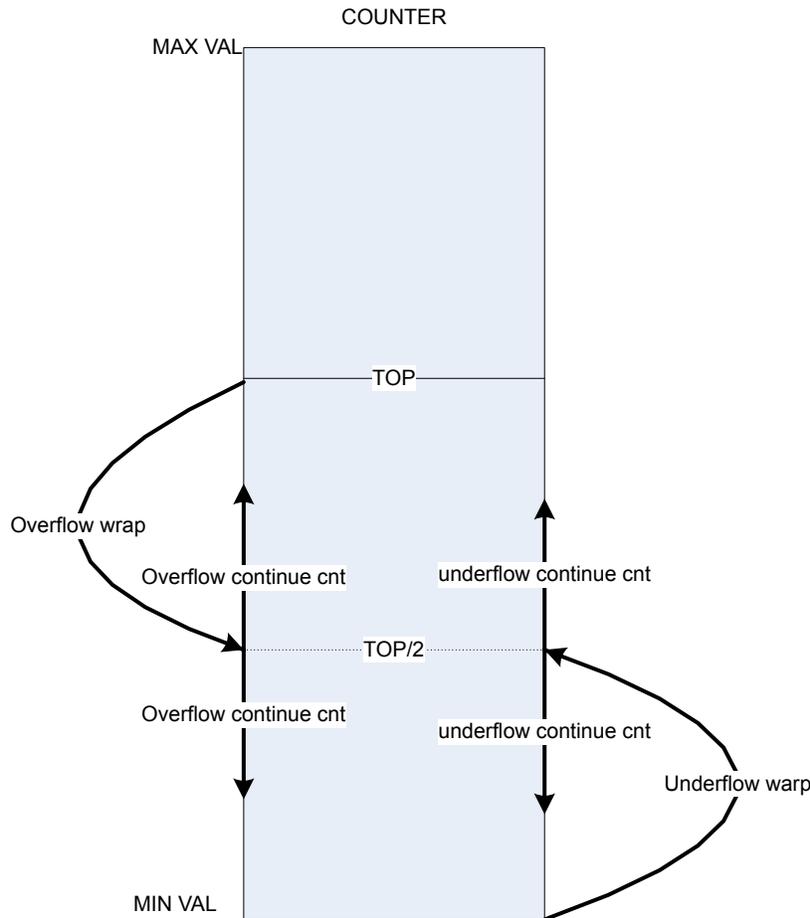


Figure 17.7. PCNT Oversampling Quadrature Decoder with Flutter Removal

### 17.3.2 Hysteresis

By default the pulse counter wraps to 0 when passing the configured top value, and wraps to the top value when counting down from 0. On these events, a system will likely want to wake up to store and track the overflow count. This is fine if the pulse counter is tracking a monotonic value or a value that does not change directions frequently. In the latter scenario, if the counter changes directions around the overflow/underflow point, the system will have to wake up frequently to keep track of the rotations, resulting in higher current consumption.

To solve this, the pulse counter has a way of introducing hysteresis to the counter. When HYST in PCNTn\_CTRL is set, the pulse counter will always wrap to TOP/2 on underflows and overflows. This takes the counter away from the area where it might overflow or underflow, removing the problem. [Figure 17.8 PCNT Hysteresis behavior of Counter on page 495](#) illustrates the hysteresis behavior.



**Figure 17.8. PCNT Hysteresis behavior of Counter**

Given a starting value of 0 for the counter, the absolute count value when hysteresis is enabled can be calculated with the equations [Figure 17.9 Absolute Position With Hysteresis and Even TOP Value on page 495](#) or [Figure 17.10 Absolute Position With Hysteresis and Odd TOP Value on page 495](#), depending on whether the TOP value is even or odd.

$$CNT_{abs} = CNT - UF_{CNT} \times (TOP/2+1) + OF_{CNT} \times (TOP/2+1)$$

**Figure 17.9. Absolute Position With Hysteresis and Even TOP Value**

$$CNT_{abs} = CNT - UF_{CNT} \times (TOP/2+1) + OF_{CNT} \times (TOP/2+2)$$

**Figure 17.10. Absolute Position With Hysteresis and Odd TOP Value**

### 17.3.3 Auxiliary Counter

To be able to keep explicit track of counting in one direction in addition to the regular counter which counts both up and down, the auxiliary counter can be used. The pulse counter can, for instance, be configured to keep track of the absolute rotation of the wheel, while at the same time the auxiliary counter can keep track of how much the wheel has reversed.

The auxiliary counter is enabled by configuring AUXCNTEV in PCNTn\_CTRL. It will always count up, but it can be configured whether it should count up on up-events, down-events or both, keeping track of rotation either way or general movement. The value of the auxiliary counter can be read from the PCNTn\_AUXCNT register.

Overflows on the auxiliary counter happen when the auxiliary counter passes the top value of the pulse counter, configured in PCNTn\_TOP. In that event, the AUXOF interrupt flag is set, and the auxiliary counter wraps to 0.

As the auxiliary counter, the main counter can be configured to count only on certain events. This is done through CNTEV in PCNTn\_CTRL, and it is possible like for the auxiliary counter, to make the main counter count on only up and down events. The difference between the counters is that where the auxiliary counter will only count up, the main counter will count up or down depending on the direction of the count event.

### 17.3.4 Triggered Compare and Clear

The pulse counter features triggered compare and clear. When enabled, a configurable trigger will induce a comparison between the main counter, PCNTn\_CNT, and the top value, PCNTn\_TOP. After the comparison, the counter is cleared. The trigger for a compare and clear event is configured in the TCCMODE bit-field in PCNTn\_CTRL. There are two options, LFA and PRS. If LFA is selected, the pulse counter will be compared with the top value, and cleared every  $2^N$  LFA clock cycle (where N is the value of TCCPRESC in PCNTn\_CTRL). If a PRS trigger is selected, the active PRS channel is configured in TCCPRSEL in PCNTn\_CTRL. The PRS input can be inverted by setting TCCPRSPOL, triggering the compare and clear on the negative edge of the PRS input. The PRS input can also be used as a gate for the pulse counter clock. This is enabled by setting PRSGATEEN in PCNTn\_CTRL.

**Note:** When PRSGATEEN is set, the clock to the entire pulse counter will be gated by the PRS input, meaning that register writes will not take effect while the gated clock is inactive.

Comparison with PCNTn\_TOP can be performed in three ways: range, greater than or equal, and less than or equal. TCCCOMP in PCNTn\_CTRL configures comparison mode. Upon a compare match, the TCC interrupt is set, and the PRS output from the pulse counter is set. The PRS output will remain set until the next compare and clear event. Triggered compare and clear is intended for use when the pulse counter is configured to count up. In this mode, PCNTn\_CNT will not wrap to 0 when hitting PCNTn\_TOP, it will keep counting. In addition, the counter will not overflow, it will rather stop counting, just setting the overflow interrupt flag.

Figure 17.11 PCNT Triggered Compare and Clear on page 497 shows an overview of the control circuitry for triggered compare and clear. The control circuitry includes two positive edge detectors (PED) and glitch filters, used to generate clocks for the pulse counter. The two clock outputs are mutually exclusive: If both edge detectors receive a pulse at the same time, the output pulse from one of them will be postponed until the other edge detectors output pulse has completed.

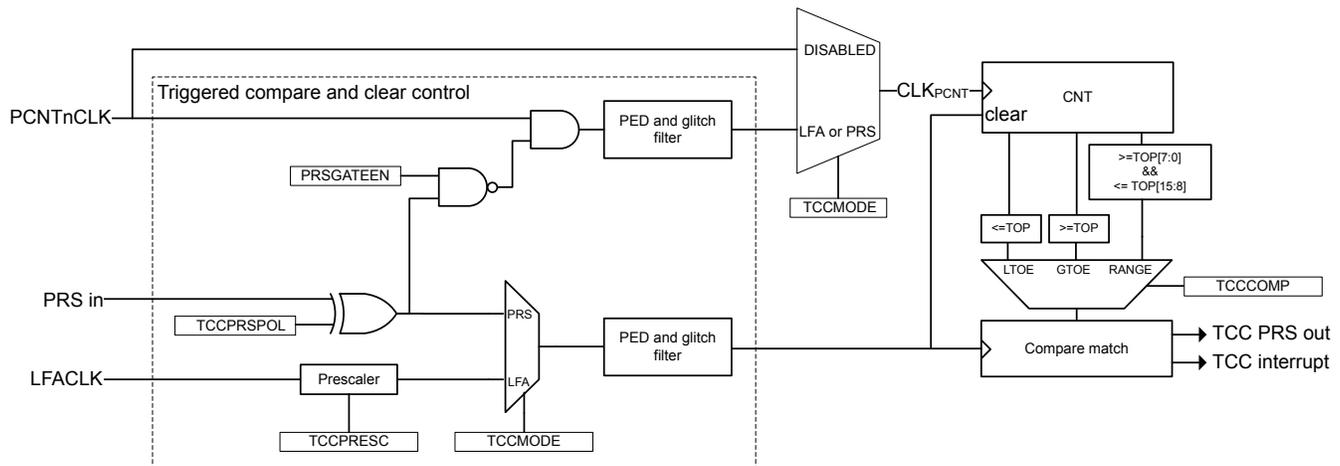


Figure 17.11. PCNT Triggered Compare and Clear

**Note:** TCCMODE, TCCPRESC, PRSGATEEN, TCCPRSPOL, and TCCPRSEL in PCNTn\_CTRL should only be altered when RSTEN in PCNTn\_CTRL is set.

### 17.3.5 Register Access

The counter-clock domain may be clocked externally. To update the counter-clock domain registers from software in this mode, 2-3 clock pulses on the external clock are needed to synchronize accesses to the externally clocked domain. Clock source switching is controlled from the registers in the CMU ([12. CMU - Clock Management Unit](#)).

When the RSTEN bit in the PCNTn\_CTRL register is set, the PCNT clock domain is asynchronously held in reset. The reset is synchronously released two PCNT clock edges after the RSTEN bit in the PCNTn\_CTRL register is cleared by software. This asynchronous reset restores the reset values in PCNTn\_TOP, PCNTn\_CNT and other control registers in the PCNT clock domain.

CNTRSTEN works in a similar manner as RSTEN, but only resetting the counter, CNT. Note that the counter is also reset by RSTEN.

AUXCNTRSTEN works in a similar manner as RSTEN, but only resetting the auxiliary counter, PCNTn\_AUXCNT. Note that the auxiliary counter is also reset by RSTEN.

Since this module is a Low Energy Peripheral, and runs off a clock which is asynchronous to the HFCORECLK, special considerations must be taken when accessing registers. Refer to [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#) for a description on how to perform register accesses to Low Energy Peripherals.

**Note:** PCNTn\_TOP and PCNTn\_CNT are read-only registers. When writing to PCNTn\_TOPB, make sure that the counter value, PCNTn\_CNT, can not exceed the value written to PCNTn\_TOPB within two clock cycles.

### 17.3.6 Clock Sources

The pulse counter may be clocked from two possible clock sources: LFACLK or an external clock. The clock selection is configured by the PCNT0CLKSEL bit in the CMU\_PCNTCTRL in the Clock Management Unit (CMU), [12. CMU - Clock Management Unit](#). The default clock source is the LFACLK.

This PCNT module may also use PCNTn\_S0IN as an external clock to clock the counter (EXTCLKSINGLE mode) and to sample PCNTn\_S1IN (EXTCLKQUAD mode). Setup, hold and max frequency constraints for PCNTn\_S0IN and PCNTn\_S1IN for these modes are specified in the device data sheet.

To use this module, the LE interface clock must be enabled in CMU\_HFBUSCLKEN0, in addition to the module clock in CMU\_PCNTCTRL.

**Note:** PCNT Clock Domain Reset, RSTEN, should be set when changing clock source for PCNT. If changing to an external clock source, the clock pin has to be enabled as input prior to de-asserting RSTEN. Changing clock source without asserting RSTEN results in undefined behaviour.

### 17.3.7 Input Filter

An optional pulse width filter is available in OVSSINGLE and OVSQUAD modes, when LFACLK is selected as a clock source for the Pulse Counter in CMU [12. CMU - Clock Management Unit](#). The filter is enabled by writing 1 to the FILT bit in the PCNTn\_CTRL register. When enabled, the high and low periods of PCNTn\_S0IN and PCNTn\_S1IN must be stable for a programmable number of consecutive clock cycles before the edge is passed to the edge detector. The filter length should be programmed in FILTLEN field of the PCNTn\_OVSCFG register.

The filter length is given by [Figure 17.12 PCNT Input Filter Length Equation on page 498](#):

$$\text{Filter length} = (\text{FILTLEN} + 5) \text{ LFACLK cycles}$$

**Figure 17.12. PCNT Input Filter Length Equation**

The maximum filter length configured is 260 LFACLK cycles.

In EXTCLKSINGLE and EXTCLKQUAD mode, there is no digital pulse width filter available.

### 17.3.8 Edge Polarity

The edge polarity can be set by configuring the EDGE bit in the PCNTn\_CTRL register. When this bit is cleared, the pulse counter counts positive edges of PCNTn\_S0IN input. When this bit is set, the pulse counter counts negative edges in OVSSINGLE mode. Also, when the EDGE bit is set in the OVSSINGLE and EXTCLKSINGLE modes, the PCNTn\_S1IN input is inverted. In OVSQUAD 1X-4X modes the EDGE bit inverts both inputs.

**Note:** The EDGE bit in PCNTn\_CTRL has no effect in EXTCLKQUAD mode.

### 17.3.9 PRS and PCNTn\_S0IN,PCNTn\_S1IN Inputs

It is possible to receive input from PRS on both PCNTn\_S0IN (or PCNTn\_S1IN) by setting S0PRSEN (or S1PRSEN) in PCNTn\_INPUT. The PRS channel used can be selected using S0PRSEL (or S1PRSEL) in PCNTn\_INPUT.

In the Oversampling quadrature decoder modes, the input frequency should be less than 8KHz to ensure correct functionality.

PCNT module generates three PRS outputs the TCC PRS output, the CNT OF/UF PRS output and the CNT DIR PRS output. The TCC PRS is generated on compare match of TCC event. The CNT OF/UF combined PRS is generated when the counter overflow or underflows. The CNT DIR PRS is a level PRS and indicates the current direction of count of counter CNT

**Note:** S0PRSEN,S1PRSEN,S0PRSEL,S1PRSEL should only be altered when RSTEN in PCNTn\_CTRL is set.

### 17.3.10 Interrupts

The interrupt generated by PCNT uses the PCNTn\_INT interrupt vector. Software must read the PCNTn\_IF register to determine which module interrupt that generated the vector invocation.

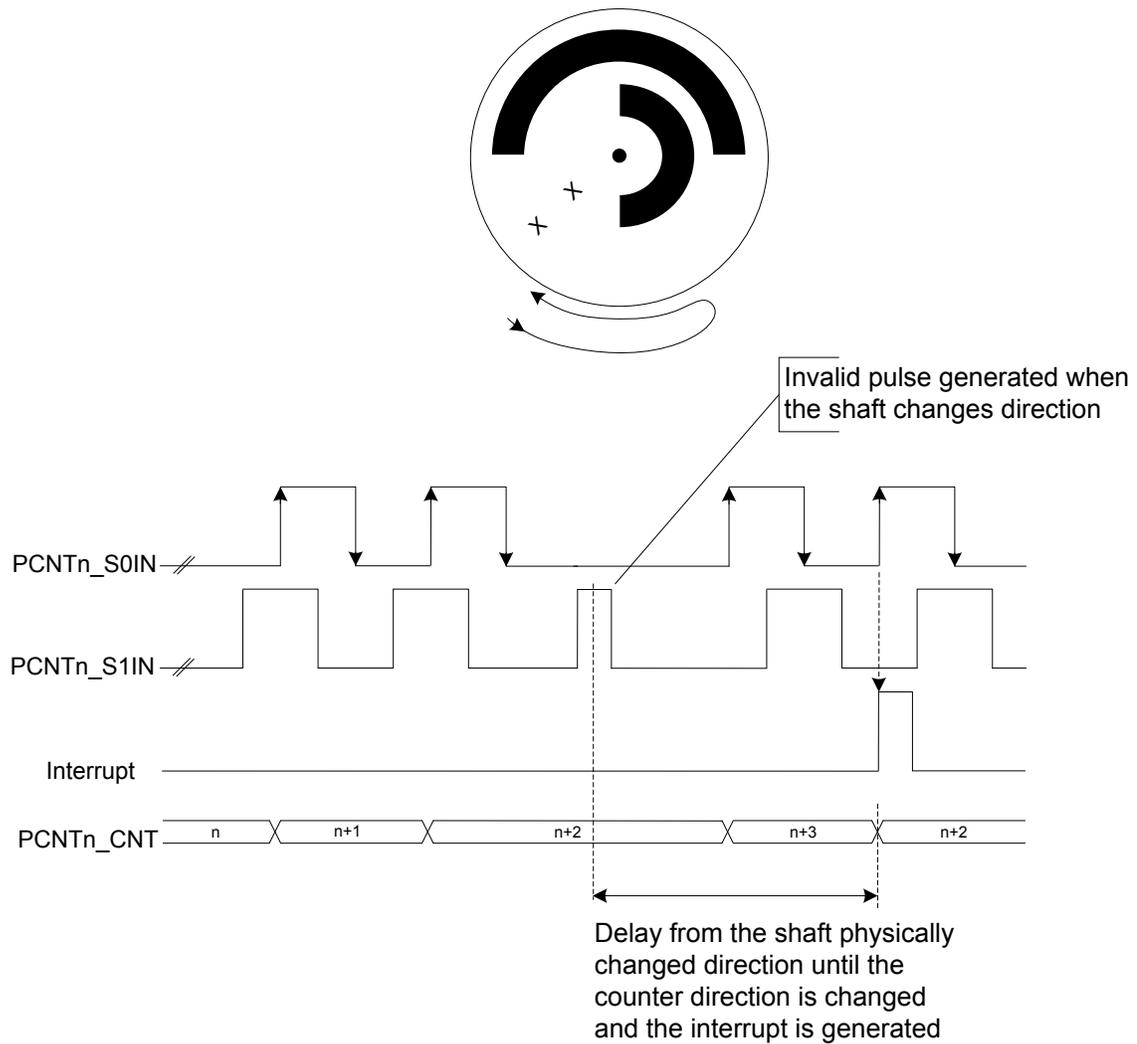
#### 17.3.10.1 Underflow and Overflow Interrupts

The underflow interrupt flag (UF) is set when the counter counts down from 0. I.e. when the value of the counter is 0 and a new pulse is received. The PCNTn\_CNT register is loaded with the PCNTn\_TOP value after this event.

The overflow interrupt flag (OF) is set when the counter counts up from the PCNTn\_TOP (reload) value. I.e. if PCNTn\_CNT = PCNTn\_TOP and a new pulse is received. The PCNTn\_CNT register is loaded with the value 0 after this event.

### 17.3.10.2 Direction Change Interrupt

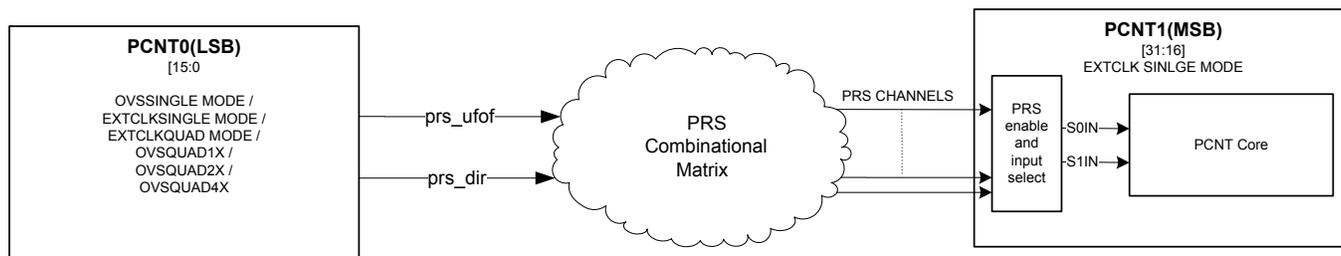
The PCNTn\_PCNT module sets the DIRCNG interrupt flag (PCNTn\_IF register) for EXTCLKQUAD and OVSQUAD1X-4X modes when the direction of the quadrature code changes. The behavior of this interrupt in the EXTCLKQUAD mode is illustrated by [Figure 17.13 PCNT Direction Change Interrupt \(DIRCNG\) Generation](#) on page 500.



**Figure 17.13. PCNT Direction Change Interrupt (DIRCNG) Generation**

### 17.3.11 Cascading Pulse Counters

When two or more Pulse Counters are available, it is possible to cascade them. For example two 16-bit Pulse Counters can be cascaded to form a 32-bit pulse counter. This can be done with the help of the CNT UF/OF PRS and CNT DIR PRS outputs. The figure [Figure 17.14 PCNT Cascading to two 16-bit PCNT to form a 32-bit PCNT on page 501](#) illustrates this structure.



**Figure 17.14. PCNT Cascading to two 16-bit PCNT to form a 32-bit PCNT**

For cascading of Pulse Counters to work, the PCNT1 according to the figure [Figure 17.14 PCNT Cascading to two 16-bit PCNT to form a 32-bit PCNT on page 501](#) should be programmed in EXTCLKSINGLE mode and its S0IN and S1IN inputs should be configured to prs\_ufof and prs\_dir of PCNT0 respectively. In addition to this, a strict programming sequence needs to be followed to ensure both PCNTs are in sync with each other.

- Configure PCNT0 registers. eg. PCNT0\_INPUT, PCNT0\_CTRL, PCNT0\_OVSCFG etc.
- Wait for PCNT0\_SYCNBUSY to be cleared to ensure the registers are synchronized to the asynchronous clock domain.
- Hold PCNT0 in sw reset by setting PCNT0\_CTRL\_RSTEN.
- Configure PCNT1\_CTRL to EXTCLKSINLGE mode with S1CDIR and CNTDIR bit set. Configure INPUT to accept "prs\_ufof" and "prs\_dir" of PCNT0 on S0IN and S1IN respectively.
- Wait for PCNTn\_SYCNBUSY to be cleared to ensure the registers are synchronized to the asynchronous clock domain. Use three PRS\_SWPULSE on the S0IN prs channel to ensure this synchronization.
- Hold PCNT1 in sw reset by setting PCNT1\_CTRL\_RSTEN.
- Clear PCNT1\_CTRL\_RSTEN and synchronize it by asserting two PRS\_SWPULSE on the S0IN input.
- Finally clear PCNT0\_CTRL\_RSTEN and start counting.

**Note:** When RSTEN in PCNTn\_CTRL is set, the TOP value in the Pulse Counter gets cleared. Therefore, in order to update the TOP value while RSTEN is set, assert TOPBFEN bit in PCNTn\_CTRL. This will update the TOP value with the TOPB value even without having to synchronize the TOPB value. This only works if TOPBFEN and TOPB are configured while RSTEN in PCNTn\_CTRL is set.

## 17.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name            | Type  | Description                      |
|--------|-----------------|-------|----------------------------------|
| 0x000  | PCNTn_CTRL      | RW    | Control Register                 |
| 0x004  | PCNTn_CMD       | W1    | Command Register                 |
| 0x008  | PCNTn_STATUS    | R     | Status Register                  |
| 0x00C  | PCNTn_CNT       | R     | Counter Value Register           |
| 0x010  | PCNTn_TOP       | R     | Top Value Register               |
| 0x014  | PCNTn_TOPB      | RW    | Top Value Buffer Register        |
| 0x018  | PCNTn_IF        | R     | Interrupt Flag Register          |
| 0x01C  | PCNTn_IFS       | W1    | Interrupt Flag Set Register      |
| 0x020  | PCNTn_IFC       | (R)W1 | Interrupt Flag Clear Register    |
| 0x024  | PCNTn_IEN       | RW    | Interrupt Enable Register        |
| 0x02C  | PCNTn_ROUTELOC0 | RW    | I/O Routing Location Register    |
| 0x040  | PCNTn_FREEZE    | RW    | Freeze Register                  |
| 0x044  | PCNTn_SYNCBUSY  | R     | Synchronization Busy Register    |
| 0x064  | PCNTn_AUXCNT    | R     | Auxiliary Counter Value Register |
| 0x068  | PCNTn_INPUT     | RW    | PCNT Input Register              |
| 0x06C  | PCNTn_OVSCFG    | RW    | Oversampling Config Register     |

## 17.5 Register Description

### 17.5.1 PCNTn\_CTRL - Control Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |          |    |           |           |         |    |    |          |    |    |         |      |        |          |     |       |     |        |      |           |             |          |       |      |    |      |     |   |
|---------------|--------------|----|----|----|----------|----|-----------|-----------|---------|----|----|----------|----|----|---------|------|--------|----------|-----|-------|-----|--------|------|-----------|-------------|----------|-------|------|----|------|-----|---|
| 0x000         | 31           | 30 | 29 | 28 | 27       | 26 | 25        | 24        | 23      | 22 | 21 | 20       | 19 | 18 | 17      | 16   | 15     | 14       | 13  | 12    | 11  | 10     | 9    | 8         | 7           | 6        | 5     | 4    | 3  | 2    | 1   | 0 |
| <b>Reset</b>  | 0            |    |    |    | 0x0      |    | 0         | 0         | 0x0     |    |    | 0x0      |    |    | 0x0     |      | 0      | 0        | 0x0 |       | 0x0 |        | 0    | 0         | 0           | 0        | 0     | 0    | 0  | 0    | 0x0 |   |
| <b>Access</b> | RW           |    |    |    | RW       |    | RW        | RW        | RW      |    |    | RW       |    |    | RW      |      | RW     | RW       | RW  | RW    | RW  |        | RW   | RW        | RW          | RW       | RW    | RW   | RW |      | RW  |   |
| <b>Name</b>   | TOPBHFSEL    |    |    |    | TCCPRSEL |    | TCCPRSPOL | PRSGATEEN | TCCCOMP |    |    | TCCPRESC |    |    | TCCMODE | EDGE | CNTDIR | AUXCNTEV |     | CNTEV |     | S1CDIR | HYST | DEBUGHALT | AUXCNTRSTEN | CNTRSTEN | RSTEN | FILT |    | MODE |     |   |

| Bit   | Name            | Reset   | Access   | Description  |
|-------|-----------------|---|--|--|
| 31    | TOPBHFSEL       | 0   | RW   | <b>TOPB High Frequency Value Select</b><br>Apply High frequency value of TOPB to TOP register. Should be used only when RSTEN in PCNTn_CTRL is set |
| 30    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |  |
| 29:26 | TCCPRSEL        | 0x0   | RW   | <b>TCC PRS Channel Select</b><br>Select PRS channel used as compare and clear trigger.   |
|       | Value           | Mode  | Description  |  |
|       | 0               | PRSCH0  | PRS Channel 0 selected.                              |  |
|       | 1               | PRSCH1  | PRS Channel 1 selected.                              |  |
|       | 2               | PRSCH2  | PRS Channel 2 selected.                              |  |
|       | 3               | PRSCH3  | PRS Channel 3 selected.                              |  |
|       | 4               | PRSCH4  | PRS Channel 4 selected.                              |  |
|       | 5               | PRSCH5  | PRS Channel 5 selected.                              |  |
|       | 6               | PRSCH6  | PRS Channel 6 selected.                              |  |
|       | 7               | PRSCH7  | PRS Channel 7 selected.                              |  |
|       | 8               | PRSCH8  | PRS Channel 8 selected.                              |  |
|       | 9               | PRSCH9  | PRS Channel 9 selected.                              |  |
|       | 10              | PRSCH10   | PRS Channel 10 selected.                             |  |
|       | 11              | PRSCH11   | PRS Channel 11 selected.                             |  |
| 25    | TCCPRSPOL       | 0   | RW   | <b>TCC PRS Polarity Select</b><br>Configure which edge on the PRS input is used to trigger a compare and clear event                               |
|       | Value           | Mode  | Description  |  |
|       | 0               | RISING  | Rising edge on PRS trigger compare and clear event.  |  |
|       | 1               | FALLING   | Falling edge on PRS trigger compare and clear event. |  |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 24    | PRSGATEEN       | 0   | RW     | <b>PRS Gate Enable</b><br>When set, the clock input to the pulse counter will be gated when the selected PRS input is the inverse of TCCPRSPOL.  |
| 23:22 | TCCCOMP         | 0x0   | RW     | <b>Triggered Compare and Clear Compare Mode</b><br>Selects the mode for comparison upon a compare and clear event.   |
|       | Value           | Mode  |        | Description  |
|       | 0               | LTOE  |        | Compare match if PCNT_CNT is less than, or equal to PCNT_TOP.  |
|       | 1               | GTOE  |        | Compare match if PCNT_CNT is greater than or equal to PCNT_TOP.  |
|       | 2               | RANGE   |        | Compare match if PCNT_CNT is less than, or equal to PCNT_TOP[15:8], and greater than, or equal to PCNT_TOP[7:0].   |
| 21    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 20:19 | TCCPRESC        | 0x0   | RW     | <b>Set the LFA Prescaler for Triggered Compare and Clear</b><br>Selects the prescaler value for LFA compare and clear events   |
|       | Value           | Mode  |        | Description  |
|       | 0               | DIV1  |        | Compare and clear event each LFA cycle.  |
|       | 1               | DIV2  |        | Compare and clear performed on every other LFA cycle.  |
|       | 2               | DIV4  |        | Compare and clear performed on every 4th LFA cycle.  |
|       | 3               | DIV8  |        | Compare and clear performed on every 8th LFA cycle.  |
| 18    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 17:16 | TCCMODE         | 0x0   | RW     | <b>Sets the Mode for Triggered Compare and Clear</b><br>Selects whether compare and clear should be triggered on each LFA clock, or from PRS   |
|       | Value           | Mode  |        | Description  |
|       | 0               | DISABLED  |        | Triggered compare and clear not enabled.   |
|       | 1               | LFA   |        | Compare and clear performed on each (optionally prescaled) LFA clock cycle.  |
|       | 2               | PRS   |        | Compare and clear performed on positive PRS edges.   |
| 15    | EDGE            | 0   | RW     | <b>Edge Select</b><br>Determines the polarity of the incoming edges. This bit should be written when PCNT is in DISABLE mode, otherwise the behavior is unpredictable. This bit used only in OVSSINGLE, EXTCLKSINGLE and OVSQUAD1X-4X modes. |
|       | Value           | Mode  |        | Description  |
|       | 0               | POS   |        | Positive edges on the PCNTn_S0IN inputs are counted in OVSSINGLE mode. Does not invert PCNTn_S1IN input in OVSSINGLE and EXTCLKSINGLE modes  |
|       | 1               | NEG   |        | Negative edges on the PCNTn_S0IN inputs are counted in OVSSINGLE mode. Inverts the PCNTn_S1IN input in OVSSINGLE and EXTCLKSINGLE modes  |

| Bit   | Name        | Reset | Access | Description  |
|-------|-------------|-------|--------|--|
| 14    | CNTDIR      | 0     | RW     | <b>Non-Quadrature Mode Counter Direction Control</b><br><br>The direction of the counter must be set in the OVSSINGLE and EXTCLKSINGLE modes. This bit is ignored in EXTCLKQUAD mode as the direction is automatically detected.   |
|       | Value       | Mode  |        | Description  |
|       | 0           | UP    |        | Up counter mode.   |
|       | 1           | DOWN  |        | Down counter mode.   |
| 13:12 | AUXCNTEV    | 0x0   | RW     | <b>Controls When the Auxiliary Counter Counts</b><br><br>Selects whether the auxiliary counter responds to up-count events, down-count events or both  |
|       | Value       | Mode  |        | Description  |
|       | 0           | NONE  |        | Never counts.  |
|       | 1           | UP    |        | Counts up on up-count events.  |
|       | 2           | DOWN  |        | Counts up on down-count events.  |
|       | 3           | BOTH  |        | Counts up on both up-count and down-count events.  |
| 11:10 | CNTEV       | 0x0   | RW     | <b>Controls When the Counter Counts</b><br><br>Selects whether the regular counter responds to up-count events, down-count events or both  |
|       | Value       | Mode  |        | Description  |
|       | 0           | BOTH  |        | Counts up on up-count and down on down-count events.   |
|       | 1           | UP    |        | Only counts up on up-count events.   |
|       | 2           | DOWN  |        | Only counts down on down-count events.   |
|       | 3           | NONE  |        | Never counts.  |
| 9     | S1CDIR      | 0     | RW     | <b>Count Direction Determined By S1</b><br><br>S1 gives the direction of counting when in the OVSSINGLE or EXTCLKSINGLE modes. When S1 is high, the count direction is given by CNTDIR, and when S1 is low, the count direction is the opposite  |
| 8     | HYST        | 0     | RW     | <b>Enable Hysteresis</b><br><br>When hysteresis is enabled, the PCNT will always overflow and underflow to TOP/2.  |
| 7     | DEBUGHALT   | 0     | RW     | <b>Debug Mode Halt Enable</b><br><br>Set to halt the PCNT in debug mode only in OVSSINGLE and OVSQUAD modes. When in EXTCLKSINGLE or EXTCLKQUAD modes, DEBUGHALT does not halt the Pulse Counter.  |
|       | Value       |       |        | Description  |
|       | 0           |       |        | PCNT is running in debug mode.   |
|       | 1           |       |        | PCNT is frozen in debug mode.  |
| 6     | AUXCNTRSTEN | 0     | RW     | <b>Enable AUXCNT Reset</b><br><br>The auxiliary counter, AUXCNT, is asynchronously held in reset when this bit is set. The reset is synchronously released two PCNT clock edges after this bit is cleared. If an external clock is used, the reset should be performed by setting and clearing the bit without pending for SYNCBUSY bit. |

| Bit | Name     | Reset        | Access | Description  |
|-----|----------|--------------|--------|--|
| 5   | CNTRSTEN | 0            | RW     | <b>Enable CNT Reset</b><br><br>The counter, CNT, is asynchronously held in reset when this bit is set. The reset is synchronously released two PCNT clock edges after this bit is cleared. If an external clock is used, the reset should be performed by setting and clearing the bit without pending for SYNCBUSY bit. This action clears the counter to its reset value |
| 4   | RSTEN    | 0            | RW     | <b>Enable PCNT Clock Domain Reset</b><br><br>The PCNT clock domain is asynchronously held in reset when this bit is set. The reset is synchronously released two PCNT clock edges after this bit is cleared. If an external clock is used, the reset should be performed by setting and clearing the bit without pending for SYNCBUSY bit.                                 |
| 3   | FILT     | 0            | RW     | <b>Enable Digital Pulse Width Filter</b><br><br>The filter passes all high and low periods that are at least (FILTLEN+5) clock cycles wide. This filter is only available in OVSSINGLE,OVSQUAD1X-4X modes.   |
| 2:0 | MODE     | 0x0          | RW     | <b>Mode Select</b><br><br>Selects the mode of operation. The corresponding clock source must be selected from the CMU.   |
|     | Value    | Mode         |        | Description  |
|     | 0        | DISABLE      |        | The module is disabled.  |
|     | 1        | OVSSINGLE    |        | Single input LFACLK oversampling mode (available in EM0-EM3).  |
|     | 2        | EXTCLKSINGLE |        | Externally clocked single input counter mode (available in EM0-EM3).   |
|     | 3        | EXTCLKQUAD   |        | Externally clocked quadrature decoder mode (available in EM0-EM3).   |
|     | 4        | OVSQUAD1X    |        | LFACLK oversampling quadrature decoder 1X mode (available in EM0-EM3).   |
|     | 5        | OVSQUAD2X    |        | LFACLK oversampling quadrature decoder 2X mode (available in EM0-EM3).   |
|     | 6        | OVSQUAD4X    |        | LFACLK oversampling quadrature decoder 4X mode (available in EM0-EM3).   |

### 17.5.2 PCNTn\_CMD - Command Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |         |        |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---------|--------|--|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1       | 0      |  |  |
| 0x004         |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |         |        |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | 0       | 0      |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | W1      | W1     |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | LTOPBIM | LCNTIM |  |  |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 31:2 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 1    | LTOPBIM         | 0   | W1     | <b>Load TOPB Immediately</b><br>This bit has no effect since TOPB is not buffered and it is loaded directly into TOP. |
| 0    | LCNTIM          | 0   | W1     | <b>Load CNT Immediately</b><br>Load PCNTn_TOP into PCNTn_CNT on the next counter clock cycle.                         |

### 17.5.3 PCNTn\_STATUS - Status Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |     |   |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-----|---|--|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1   | 0 |  |  |
| 0x008         |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |     |   |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | 0   | 0 |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | R   | R |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | DIR |   |  |  |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 31:1 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 0    | DIR             | 0   | R      | <b>Current Counter Direction</b><br>Current direction status of the counter. This bit is valid in EXTCLKQUAD mode only. |
|      | Value           | Mode  |        | Description   |
|      | 0               | UP  |        | Up counter mode (clockwise in EXTCLKQUAD mode with the EDGE bit in PCNTn_CTRL set to 0).                                |
|      | 1               | DOWN  |        | Down counter mode.  |

## 17.5.4 PCNTn\_CNT - Counter Value Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x00C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CNT    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset   | Access | Description   |
|-------|----------|---|--------|---|
| 31:16 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 15:0  | CNT      | 0x0000  | R      | <b>Counter Value</b><br>Gives read access to the counter. |

## 17.5.5 PCNTn\_TOP - Top Value Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x010         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00FF |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | TOP    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset   | Access | Description   |
|-------|----------|---|--------|---|
| 31:16 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 15:0  | TOP      | 0x00FF  | R      | <b>Counter Top Value</b><br>When counting down, this value is reloaded into PCNTn_CNT when counting past 0. When counting up, 0 is written to the PCNTn_CNT register when counting past this value. |

### 17.5.6 PCNTn\_TOPB - Top Value Buffer Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x014         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00FF |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | TOPB   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset   | Access | Description  |
|-------|----------|---|--------|--|
| 31:16 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 15:0  | TOPB     | 0x00FF  | RW     | <b>Counter Top Buffer</b><br>Loaded automatically to TOP when written. |

### 17.5.7 PCNTn\_IF - Interrupt Flag Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |         |     |       |        |    |    |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---------|-----|-------|--------|----|----|---|---|
| 0x018         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7       | 6   | 5     | 4      | 3  | 2  | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0       | 0   | 0     | 0      | 0  | 0  |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | R       | R   | R     | R      | R  | R  |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | OQSTERR | TCC | AUXOF | DIRCNG | OF | UF |   |   |

| Bit  | Name     | Reset   | Access | Description  |
|------|----------|---|--------|--|
| 31:6 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 5    | OQSTERR  | 0   | R      | <b>Oversampling Quadrature State Error Interrupt</b><br>Set in the Oversampling Quadrature Mode when incorrect state transition occurs |
| 4    | TCC      | 0   | R      | <b>Triggered Compare Interrupt Read Flag</b><br>Set upon triggered compare match   |
| 3    | AUXOF    | 0   | R      | <b>Auxiliary Overflow Interrupt Read Flag</b><br>Set when an Auxiliary CNT overflow occurs   |
| 2    | DIRCNG   | 0   | R      | <b>Direction Change Detect Interrupt Flag</b><br>Set when the count direction changes. Set in EXTCLKQUAD mode only.                    |
| 1    | OF       | 0   | R      | <b>Overflow Interrupt Read Flag</b><br>Set when a CNT overflow occurs  |
| 0    | UF       | 0   | R      | <b>Underflow Interrupt Read Flag</b><br>Set when a CNT underflow occurs  |

## 17.5.8 PCNTn\_IFS - Interrupt Flag Set Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |         |     |       |        |    |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---------|-----|-------|--------|----|----|
| 0x01C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5       | 4   | 3     | 2      | 1  | 0  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | 0       | 0   | 0     | 0      | 0  | 0  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | W1      | W1  | W1    | W1     | W1 | W1 |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | OQSTERR | TCC | AUXOF | DIRCNG | OF | UF |

| Bit  | Name            | Reset   | Access | Description  |
|------|-----------------|---|--------|--|
| 31:6 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 5    | OQSTERR         | 0   | W1     | <b>Set OQSTERR Interrupt Flag</b><br>Write 1 to set the OQSTERR interrupt flag |
| 4    | TCC             | 0   | W1     | <b>Set TCC Interrupt Flag</b><br>Write 1 to set the TCC interrupt flag         |
| 3    | AUXOF           | 0   | W1     | <b>Set AUXOF Interrupt Flag</b><br>Write 1 to set the AUXOF interrupt flag     |
| 2    | DIRCNG          | 0   | W1     | <b>Set DIRCNG Interrupt Flag</b><br>Write 1 to set the DIRCNG interrupt flag   |
| 1    | OF              | 0   | W1     | <b>Set OF Interrupt Flag</b><br>Write 1 to set the OF interrupt flag           |
| 0    | UF              | 0   | W1     | <b>Set UF Interrupt Flag</b><br>Write 1 to set the UF interrupt flag           |

## 17.5.9 PCNTn\_IFC - Interrupt Flag Clear Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |         |       |       |        |       |       |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---------|-------|-------|--------|-------|-------|
| 0x020         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5       | 4     | 3     | 2      | 1     | 0     |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | 0       | 0     | 0     | 0      | 0     | 0     |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | (R)W1   | (R)W1 | (R)W1 | (R)W1  | (R)W1 | (R)W1 |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | OQSTERR | TCC   | AUXOF | DIRCNG | OF    | UF    |

| Bit  | Name     | Reset  | Access | Description   |
|------|----------|--|--------|---|
| 31:6 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 5    | OQSTERR  | 0  | (R)W1  | <b>Clear OQSTERR Interrupt Flag</b><br>Write 1 to clear the OQSTERR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 4    | TCC      | 0  | (R)W1  | <b>Clear TCC Interrupt Flag</b><br>Write 1 to clear the TCC interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).         |
| 3    | AUXOF    | 0  | (R)W1  | <b>Clear AUXOF Interrupt Flag</b><br>Write 1 to clear the AUXOF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 2    | DIRCNG   | 0  | (R)W1  | <b>Clear DIRCNG Interrupt Flag</b><br>Write 1 to clear the DIRCNG interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |
| 1    | OF       | 0  | (R)W1  | <b>Clear OF Interrupt Flag</b><br>Write 1 to clear the OF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).           |
| 0    | UF       | 0  | (R)W1  | <b>Clear UF Interrupt Flag</b><br>Write 1 to clear the UF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).           |

## 17.5.10 PCNTn\_IEN - Interrupt Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |         |     |       |        |    |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---------|-----|-------|--------|----|----|
| 0x024         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5       | 4   | 3     | 2      | 1  | 0  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | 0       | 0   | 0     | 0      | 0  | 0  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | RW      | RW  | RW    | RW     | RW | RW |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | OQSTERR | TCC | AUXOF | DIRCNG | OF | UF |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 31:6 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 5    | OQSTERR         | 0   | RW     | <b>OQSTERR Interrupt Enable</b><br>Enable/disable the OQSTERR interrupt |
| 4    | TCC             | 0   | RW     | <b>TCC Interrupt Enable</b><br>Enable/disable the TCC interrupt         |
| 3    | AUXOF           | 0   | RW     | <b>AUXOF Interrupt Enable</b><br>Enable/disable the AUXOF interrupt     |
| 2    | DIRCNG          | 0   | RW     | <b>DIRCNG Interrupt Enable</b><br>Enable/disable the DIRCNG interrupt   |
| 1    | OF              | 0   | RW     | <b>OF Interrupt Enable</b><br>Enable/disable the OF interrupt           |
| 0    | UF              | 0   | RW     | <b>UF Interrupt Enable</b><br>Enable/disable the UF interrupt           |

### 17.5.11 PCNTn\_ROUTELOC0 - I/O Routing Location Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |   |   |   |   |   |   |         |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---------|---|---|---|
| 0x02C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3       | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00    |    |    |    |    |    |   |   |   |   |   |   | 0x00    |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      |    |    |    |    |    |   |   |   |   |   |   | RW      |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | S1INLOC |    |    |    |    |    |   |   |   |   |   |   | S0INLOC |   |   |   |

| Bit   | Name            | Reset   | Access | Description |
|-------|-----------------|---|--------|-------------|
| 31:14 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |             |

13:8 S1INLOC 0x00 RW **I/O Location**

Defines the location of the PCNT S1IN input pin.

| Value | Mode  | Description |
|-------|-------|-------------|
| 0     | LOC0  | Location 0  |
| 1     | LOC1  | Location 1  |
| 2     | LOC2  | Location 2  |
| 3     | LOC3  | Location 3  |
| 4     | LOC4  | Location 4  |
| 5     | LOC5  | Location 5  |
| 6     | LOC6  | Location 6  |
| 7     | LOC7  | Location 7  |
| 8     | LOC8  | Location 8  |
| 9     | LOC9  | Location 9  |
| 10    | LOC10 | Location 10 |
| 11    | LOC11 | Location 11 |
| 12    | LOC12 | Location 12 |
| 13    | LOC13 | Location 13 |
| 14    | LOC14 | Location 14 |
| 15    | LOC15 | Location 15 |
| 16    | LOC16 | Location 16 |
| 17    | LOC17 | Location 17 |
| 18    | LOC18 | Location 18 |
| 19    | LOC19 | Location 19 |
| 20    | LOC20 | Location 20 |
| 21    | LOC21 | Location 21 |
| 22    | LOC22 | Location 22 |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
|     | 23   | LOC23 |        | Location 23 |
|     | 24   | LOC24 |        | Location 24 |
|     | 25   | LOC25 |        | Location 25 |
|     | 26   | LOC26 |        | Location 26 |
|     | 27   | LOC27 |        | Location 27 |
|     | 28   | LOC28 |        | Location 28 |
|     | 29   | LOC29 |        | Location 29 |
|     | 30   | LOC30 |        | Location 30 |
|     | 31   | LOC31 |        | Location 31 |

7:6 *Reserved* *To ensure compatibility with future devices, always write bits to 0. More information in [1.2 Conventions](#)*

5:0 S0INLOC 0x00 RW **I/O Location**

Defines the location of the PCNT S0IN input pin.

| Value | Mode  | Description |
|-------|-------|-------------|
| 0     | LOC0  | Location 0  |
| 1     | LOC1  | Location 1  |
| 2     | LOC2  | Location 2  |
| 3     | LOC3  | Location 3  |
| 4     | LOC4  | Location 4  |
| 5     | LOC5  | Location 5  |
| 6     | LOC6  | Location 6  |
| 7     | LOC7  | Location 7  |
| 8     | LOC8  | Location 8  |
| 9     | LOC9  | Location 9  |
| 10    | LOC10 | Location 10 |
| 11    | LOC11 | Location 11 |
| 12    | LOC12 | Location 12 |
| 13    | LOC13 | Location 13 |
| 14    | LOC14 | Location 14 |
| 15    | LOC15 | Location 15 |
| 16    | LOC16 | Location 16 |
| 17    | LOC17 | Location 17 |
| 18    | LOC18 | Location 18 |
| 19    | LOC19 | Location 19 |
| 20    | LOC20 | Location 20 |
| 21    | LOC21 | Location 21 |
| 22    | LOC22 | Location 22 |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
| 23  |      | LOC23 |        | Location 23 |
| 24  |      | LOC24 |        | Location 24 |
| 25  |      | LOC25 |        | Location 25 |
| 26  |      | LOC26 |        | Location 26 |
| 27  |      | LOC27 |        | Location 27 |
| 28  |      | LOC28 |        | Location 28 |
| 29  |      | LOC29 |        | Location 29 |
| 30  |      | LOC30 |        | Location 30 |
| 31  |      | LOC31 |        | Location 31 |

### 17.5.12 PCNTn\_FREEZE - Freeze Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |           |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-----------|
| 0x040         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0         |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0         |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | RW        |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | REGFREEZE |

| Bit  | Name            | Reset   | Access   | Description                   |
|--|-----------------|---|--|-------------------------------|
| 31:1   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |                               |
| 0  | REGFREEZE       | 0   | RW   | <b>Register Update Freeze</b> |
| When set, the update of the PCNT clock domain is postponed until this bit is cleared. Use this bit to update several registers simultaneously. |                 |   |  |                               |
|  | Value           | Mode  | Description  |                               |
|  | 0               | UPDATE  | Each write access to a PCNT register is updated into the Low Frequency domain as soon as possible. |                               |
|  | 1               | FREEZE  | The PCNT clock domain is not updated with the new written value.                                   |                               |



## 17.5.15 PCNTn\_INPUT - PCNT Input Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |         |    |    |          |    |    |    |    |    |         |    |   |          |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|---------|----|----|----------|----|----|----|----|----|---------|----|---|----------|---|---|---|---|---|---|---|---|
| 0x068         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20      | 19 | 18 | 17       | 16 | 15 | 14 | 13 | 12 | 11      | 10 | 9 | 8        | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    | 0       |    |    | 0x0      |    |    |    |    |    | 0       |    |   | 0x0      |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    | RW      |    |    | RW       |    |    |    |    |    | RW      |    |   | RW       |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    | S1PRSEN |    |    | S1PRSSEL |    |    |    |    |    | S0PRSEN |    |   | S0PRSSEL |   |   |   |   |   |   |   |   |

| Bit   | Name            | Reset   | Access                   | Description   |
|-------|-----------------|---|--------------------------|---|
| 31:12 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                          |   |
| 11    | S1PRSEN         | 0   | RW                       | <b>S1IN PRS Enable</b><br>When set, the PRS channel is selected as input to S1IN. |
| 10    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                          |   |
| 9:6   | S1PRSSEL        | 0x0   | RW                       | <b>S1IN PRS Channel Select</b><br>Select PRS channel as input to S1IN.            |
|       | Value           | Mode  | Description              |   |
|       | 0               | PRSCH0  | PRS Channel 0 selected.  |   |
|       | 1               | PRSCH1  | PRS Channel 1 selected.  |   |
|       | 2               | PRSCH2  | PRS Channel 2 selected.  |   |
|       | 3               | PRSCH3  | PRS Channel 3 selected.  |   |
|       | 4               | PRSCH4  | PRS Channel 4 selected.  |   |
|       | 5               | PRSCH5  | PRS Channel 5 selected.  |   |
|       | 6               | PRSCH6  | PRS Channel 6 selected.  |   |
|       | 7               | PRSCH7  | PRS Channel 7 selected.  |   |
|       | 8               | PRSCH8  | PRS Channel 8 selected.  |   |
|       | 9               | PRSCH9  | PRS Channel 9 selected.  |   |
|       | 10              | PRSCH10   | PRS Channel 10 selected. |   |
|       | 11              | PRSCH11   | PRS Channel 11 selected. |   |
| 5     | S0PRSEN         | 0   | RW                       | <b>S0IN PRS Enable</b><br>When set, the PRS channel is selected as input to S0IN. |
| 4     | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                          |   |
| 3:0   | S0PRSSEL        | 0x0   | RW                       | <b>S0IN PRS Channel Select</b><br>Select PRS channel as input to S0IN.            |
|       | Value           | Mode  | Description              |   |

| Bit | Name | Reset   | Access | Description              |
|-----|------|---------|--------|--------------------------|
| 0   |      | PRSCH0  |        | PRS Channel 0 selected.  |
| 1   |      | PRSCH1  |        | PRS Channel 1 selected.  |
| 2   |      | PRSCH2  |        | PRS Channel 2 selected.  |
| 3   |      | PRSCH3  |        | PRS Channel 3 selected.  |
| 4   |      | PRSCH4  |        | PRS Channel 4 selected.  |
| 5   |      | PRSCH5  |        | PRS Channel 5 selected.  |
| 6   |      | PRSCH6  |        | PRS Channel 6 selected.  |
| 7   |      | PRSCH7  |        | PRS Channel 7 selected.  |
| 8   |      | PRSCH8  |        | PRS Channel 8 selected.  |
| 9   |      | PRSCH9  |        | PRS Channel 9 selected.  |
| 10  |      | PRSCH10 |        | PRS Channel 10 selected. |
| 11  |      | PRSCH11 |        | PRS Channel 11 selected. |

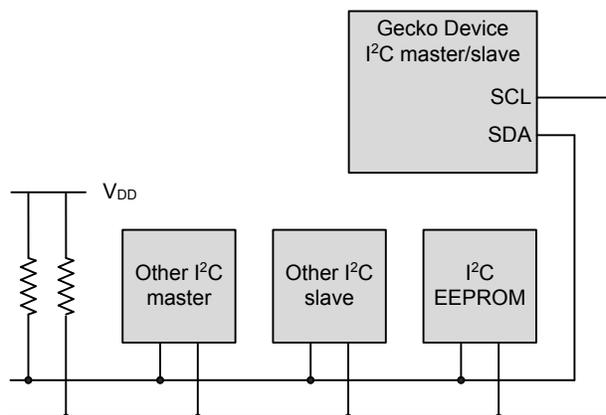
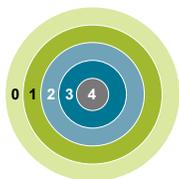
#### 17.5.16 PCNTn\_OVSCFG - Oversampling Config Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |    |   |   |   |   |   |        |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|----|---|---|---|---|---|--------|---|---|---|---|--|
| 0x06C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11       | 10 | 9 | 8 | 7 | 6 | 5 | 4      | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0        |    |   |   |   |   |   | 0x00   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW       |    |   |   |   |   |   | RW     |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | FLUTERRM |    |   |   |   |   |   | FILLEN |   |   |   |   |  |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:13 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 12    | FLUTERRM        | 0   | RW     | <b>Flutter Remove</b><br>When set, removes flutter from Quaddecoder inputs S0IN and S1IN. Available only in OVSQUAD1X-4X modes  |
| 11:8  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 7:0   | FILLEN          | 0x00  | RW     | <b>Configure Filter Length for Inputs S0IN and S1IN</b><br>Used only in OVSINGLE,OVSQUAD1X-4X modes. To use this first enable FILT in PCNTn_CTRL register. Filter length = (FILLEN + 5) LFACTK cycles |

## 18. I<sup>2</sup>C - Inter-Integrated Circuit Interface



### Quick Facts

#### What?

The I<sup>2</sup>C interface allows communication on I<sup>2</sup>C-buses with the lowest energy consumption possible.

#### Why?

I<sup>2</sup>C is a popular serial bus that enables communication with a number of external devices using only two I/O pins.

#### How?

With the help of DMA, the I<sup>2</sup>C interface allows I<sup>2</sup>C communication with minimal CPU intervention. Address recognition is available in all energy modes (except EM4), allowing the MCU to wait for data on the I<sup>2</sup>C-bus with sub- $\mu$ A current consumption.

### 18.1 Introduction

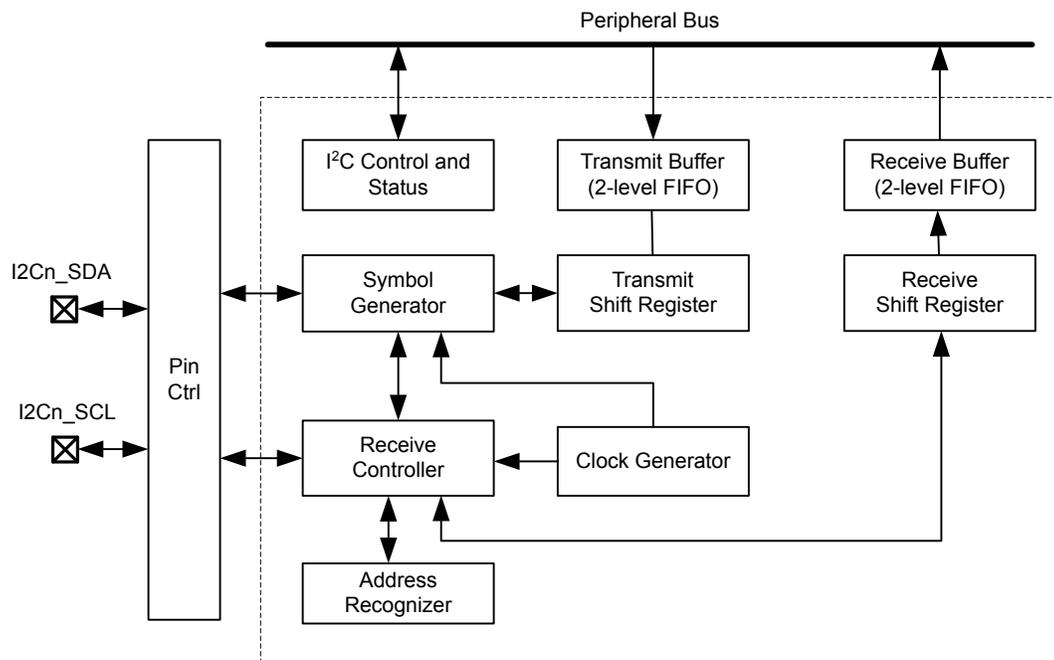
The I<sup>2</sup>C module provides an interface between the MCU and a serial I<sup>2</sup>C-bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I<sup>2</sup>C module allows precise control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in all energy modes (except EM4).

### 18.2 Features

- True multi-master capability
- Support for different bus speeds
  - Standard-mode (Sm) bit rate up to 100 kbit/s
  - Fast-mode (Fm) bit rate up to 400 kbit/s
  - Fast-mode Plus (Fm+) bit rate up to 1 Mbit/s
- Arbitration for both master and slave (allows SMBus ARP)
- Clock synchronization and clock stretching
- Hardware address recognition
  - 7-bit masked address
  - General call address
  - Active in all energy modes (except EM4)
- 10-bit address support
- Error handling
  - Clock low timeout
  - Clock high timeout
  - Arbitration lost
  - Bus error detection
- Separate receive/ transmit 2-level buffers, with additional separate shift registers
- Full DMA support

### 18.3 Functional Description

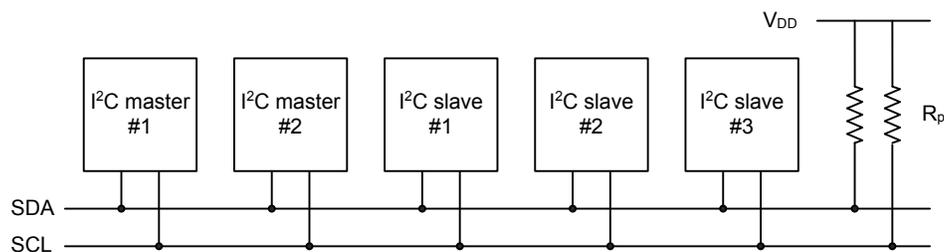
An overview of the I2C module is shown in [Figure 18.1 I2C Overview on page 520](#).



**Figure 18.1. I2C Overview**

### 18.3.1 I2C-Bus Overview

The I<sup>2</sup>C-bus uses two wires for communication; a serial data line (SDA) and a serial clock line (SCL) as shown in [Figure 18.2 I2C-Bus Example on page 521](#). As a true multi-master bus it includes collision detection and arbitration to resolve situations where multiple masters transmit data at the same time without data loss.



**Figure 18.2. I2C-Bus Example**

Each device on the bus is addressable by a unique address, and an I<sup>2</sup>C master can address all the devices on the bus, including other masters.

Both the bus lines are open-drain. The maximum value of the pull-up resistor can be calculated as a function of the maximal rise-time  $t_r$  for the given bus speed, and the estimated bus capacitance  $C_b$  as shown in [Figure 18.3 I2C Pull-up Resistor Equation on page 521](#).

$$R_p(\text{max}) = t_r / (0.8473 \times C_b)$$

**Figure 18.3. I2C Pull-up Resistor Equation**

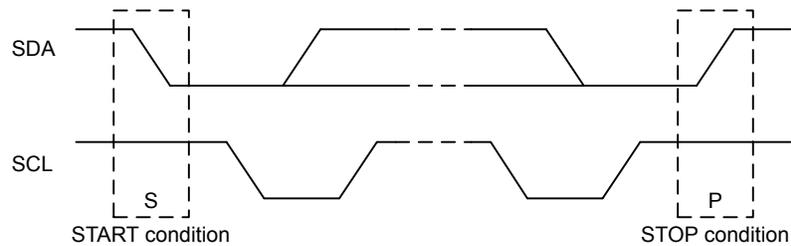
The maximal rise times for 100 kHz, 400 kHz and 1 MHz I<sup>2</sup>C are 1  $\mu$ s, 300 ns and 120 ns respectively.

**Note:**

- The GPIO drive strength can be used to control slew rate.
- If  $V_{dd}$  drops below the voltage on SCL and SDA lines, the MCU could become back powered and pull the SCL and SDA lines low.

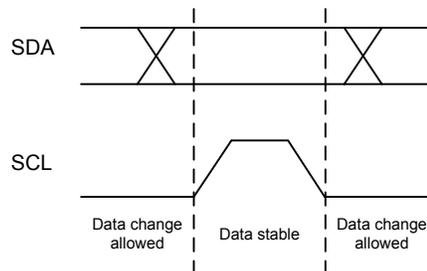
### 18.3.1.1 START and STOP Conditions

START and STOP conditions are used to initiate and stop transactions on the I<sup>2</sup>C-bus. All transactions on the bus begin with a START condition (S) and end with a STOP condition (P). As shown in [Figure 18.4 I<sup>2</sup>C START and STOP Conditions on page 522](#), a START condition is generated by pulling the SDA line low while SCL is high, and a STOP condition is generated by pulling the SDA line high while SCL is high.



**Figure 18.4. I<sup>2</sup>C START and STOP Conditions**

The START and STOP conditions are easily identifiable bus events as they are the only conditions on the bus where a transition is allowed on SDA while SCL is high. During the actual data transmission, SDA is only allowed to change while SCL is low, and must be stable while SCL is high. One bit is transferred per clock pulse on the I<sup>2</sup>C-bus as shown in [Figure 18.5 I<sup>2</sup>C Bit Transfer on I<sup>2</sup>C-Bus on page 522](#).



**Figure 18.5. I<sup>2</sup>C Bit Transfer on I<sup>2</sup>C-Bus**

### 18.3.1.2 Bus Transfer

When a master wants to initiate a transfer on the bus, it waits until the bus is idle and transmits a START condition on the bus. The master then transmits the address of the slave it wishes to interact with and a single R/W bit telling whether it wishes to read from the slave (R/W bit set to 1) or write to the slave (R/W bit set to 0).

After the 7-bit address and the R/W bit, the master releases the bus, allowing the slave to acknowledge the request. During the next bit-period, the slave pulls SDA low (ACK) if it acknowledges the request, or keeps it high if it does not acknowledge it (NACK).

Following the address acknowledge, either the slave or master transmits data, depending on the value of the R/W bit. After every 8 bits (one byte) transmitted on the SDA line, the transmitter releases the line to allow the receiver to transmit an ACK or a NACK. Both the data and the address are transmitted with the most significant bit first.

The number of bytes in a bus transfer is unrestricted. The master ends the transmission after a (N)ACK by sending a STOP condition on the bus. After a STOP condition, any master wishing to initiate a transfer on the bus can try to gain control of it. If the current master wishes to make another transfer immediately after the current, it can start a new transfer directly by transmitting a repeated START condition (Sr) instead of a STOP followed by a START.

Examples of I<sup>2</sup>C transfers are shown in [Figure 18.6 I2C Single Byte Write to Slave on page 523](#), [Figure 18.7 I2C Double Byte Read from Slave on page 523](#), and [Figure 18.8 I2C Single Byte Write, then Repeated Start and Single Byte Read on page 523](#). The identifiers used are:

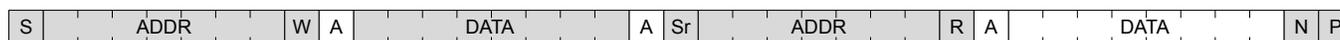
- ADDR - Address
- DATA - Data
- S - Start bit
- Sr - Repeated start bit
- P - Stop bit
- W/R - Read(1)/Write(0)
- A - ACK
- N - NACK



**Figure 18.6. I2C Single Byte Write to Slave**



**Figure 18.7. I2C Double Byte Read from Slave**



**Figure 18.8. I2C Single Byte Write, then Repeated Start and Single Byte Read**

### 18.3.1.3 Addresses

I<sup>2</sup>C supports both 7-bit and 10-bit addresses. When using 7-bit addresses, the first byte transmitted after the START-condition contains the address of the slave that the master wants to contact. In the 7-bit address space, several addresses are reserved. These addresses are summarized in [Table 18.1 I2C Reserved I2C Addresses on page 524](#), and include a General Call address which can be used to broadcast a message to all slaves on the I<sup>2</sup>C-bus.

**Table 18.1. I2C Reserved I2C Addresses**

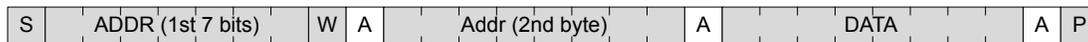
| I <sup>2</sup> C Address | R/W | Description                         |
|--------------------------|-----|-------------------------------------|
| 0000-000                 | 0   | General Call address                |
| 0000-000                 | 1   | START byte                          |
| 0000-001                 | X   | Reserved for the C-Bus format       |
| 0000-010                 | X   | Reserved for a different bus format |
| 0000-011                 | X   | Reserved for future purposes        |
| 0000-1XX                 | X   | Reserved for future purposes        |
| 1111-1XX                 | X   | Reserved for future purposes        |
| 1111-0XX                 | X   | 10 Bit slave addressing mode        |

### 18.3.1.4 10-bit Addressing

To address a slave using a 10-bit address, two bytes are required to specify the address instead of one. The seven first bits of the first byte must then be 1111 0XX, where XX are the two most significant bits of the 10-bit address. As with 7-bit addresses, the eighth bit of the first byte determines whether the master wishes to read from or write to the slave. The second byte contains the eight least significant bits of the slave address.

When a slave receives a 10-bit address, it must acknowledge both the address bytes if they match the address of the slave.

When performing a master transmitter operation, the master transmits the two address bytes and then the remaining data, as shown in [Figure 18.9 I2C Master Transmitter/Slave Receiver with 10-bit Address on page 524](#).



**Figure 18.9. I2C Master Transmitter/Slave Receiver with 10-bit Address**

When performing a master receiver operation however, the master first transmits the two address bytes in a master transmitter operation, then sends a repeated START followed by the first address byte and then receives data from the addressed slave. The slave addressed by the 10-bit address in the first two address bytes must remember that it was addressed, and respond with data if the address transmitted after the repeated start matches its own address. An example of this (with one byte transmitted) is shown in [Figure 18.10 I2C Master Receiver/Slave Transmitter with 10-bit Address on page 524](#).



**Figure 18.10. I2C Master Receiver/Slave Transmitter with 10-bit Address**

### 18.3.1.5 Arbitration, Clock Synchronization, Clock Stretching

Arbitration and clock synchronization are features aimed at allowing multi-master buses. Arbitration occurs when two devices try to drive the bus at the same time. If one device drives it low, while the other drives it high, the one attempting to drive it high will not be able to do so due to the open-drain bus configuration. Both devices sample the bus, and the one that was unable to drive the bus in the desired direction detects the collision and backs off, letting the other device continue communication on the bus undisturbed.

Clock synchronization is a means of synchronizing the clock outputs from several masters driving the bus at once, and is a requirement for effective arbitration.

Slaves on the bus are allowed to force the clock output on the bus low in order to pause the communication on the bus and give themselves time to process data or perform any real-time tasks they might have. This is called clock stretching.

Arbitration is supported by the I<sup>2</sup>C module for both masters and slaves. Clock synchronization and clock stretching is also supported.

### 18.3.2 Enable and Reset

The I<sup>2</sup>C is enabled by setting the EN bit in the I2Cn\_CTRL register. Whenever this bit is cleared, the internal state of the I<sup>2</sup>C is reset, terminating any ongoing transfers.

**Note:** When enabling the I<sup>2</sup>C, the ABORT command or the Bus Idle Timeout feature must be applied prior to use even if the BUSY flag is not set.

### 18.3.3 Safely Disabling and Changing Slave Configuration

The I<sup>2</sup>C slave is partially asynchronous, and some precautions are necessary to always ensure a safe slave disable or slave configuration change. These measures should be taken, if (while the slave is enabled) the user cannot guarantee that an address match will not occur at the exact time of slave disable or slave configuration change.

Worst case consequences for an address match while disabling slave or changing configuration is that the slave may end up in an undefined state. To reset the slave back to a known state, the EN bit in I2Cn\_CTRL must be reset. This should be done regardless of whether the slave is going to be re-enabled or not.

### 18.3.4 Clock Generation

The SCL signal generated by the I<sup>2</sup>C master determines the maximum transmission rate on the bus. The clock is generated as a division of the peripheral clock, and is given by the following equation:

$$f_{SCL} = f_{HFPERCLK} / (((N_{low} + N_{high}) \times (DIV + 1)) + 8),$$

**Figure 18.11. I2C Maximum Transmission Rate**

$N_{low}$  and  $N_{high}$  in combination with the synchronization cycles (discussed below) specify the number of prescaled clock cycles in the low and high periods of the clock signal respectively. The worst case low and high periods of the signal are:

$$T_{high} \geq ((N_{high}) \times (DIV + 1) + 4) / f_{HFPERCLK},$$

$$T_{low} \geq (N_{low} \times (DIV + 1) + 4) / f_{HFPERCLK}.$$

**Figure 18.12. I2C High and Low Cycles Equations**

In worst case,  $T_{high}$  and  $T_{low}$  can be 1  $f_{HFPERCLK}$  cycle longer than the number found by above equations due to synchronization uncertainty (i.e., if the synchronization takes 3  $f_{HFPERCLK}$  cycles instead of 2). Similarly, in the worst case the number 8 in the denominator in  $f_{SCL}$  equation can be 9 (if the synchronization cycles were 3 instead of 2 in  $T_{high}$  or  $T_{low}$ ) or 10 (if synchronization cycles were 3 in both  $T_{high}$  and  $T_{low}$ ). The values of  $N_{low}$  and  $N_{high}$  and thus the ratio between the high and low parts of the clock signal is controlled by CLHR in the I2Cn\_CTRL register.

**Note:** DIV must be set to 1 during slave mode operation.

### 18.3.5 Arbitration

Arbitration is enabled by default, but can be disabled by setting the ARBDIS bit in I2Cn\_CTRL. When arbitration is enabled, the value on SDA is sensed every time the I<sup>2</sup>C module attempts to change its value. If the sensed value is different than the value the I<sup>2</sup>C module tried to output, it is interpreted as a simultaneous transmission by another device, and that the I<sup>2</sup>C module has lost arbitration.

Whenever arbitration is lost, the ARBLOST interrupt flag in I2Cn\_IF is set, any lines held are released, and the I<sup>2</sup>C device goes idle. If an I<sup>2</sup>C master loses arbitration during the transmission of an address, another master may be trying to address it. The master therefore receives the rest of the address, and if the address matches the slave address of the master, the master goes into either slave transmitter or slave receiver mode.

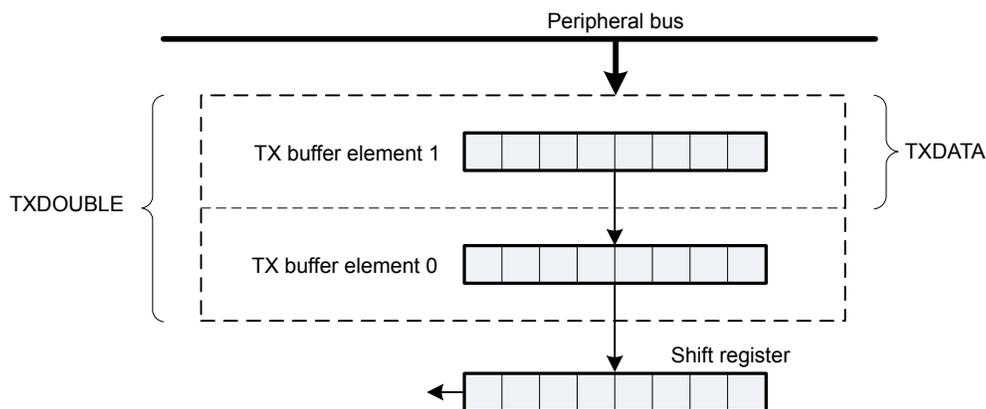
**Note:** Arbitration can be lost both when operating as a master and when operating as a slave.

### 18.3.6 Buffers

The I2C peripheral includes separate receive and transmit buffers and shift registers.

#### 18.3.6.1 Transmit Buffer and Shift Register

The I<sup>2</sup>C transmitter has a 2-level FIFO transmit buffer and a transmit shift register as shown in [Figure 18.1 I2C Overview on page 520](#). A byte is loaded into the transmit buffer by writing to I2Cn\_TXDATA or 2 bytes can be loaded simultaneously in the transmit buffer by writing to I2Cn\_TXDOUBLE. [Figure 18.13 I2C Transmit Buffer Operation on page 526](#) shows the basics of the transmit buffer. When the transmit shift register is empty and ready for new data, the byte from the transmit buffer is then loaded into the shift register. The byte is then kept in the shift register until it is transmitted. When a byte has been transmitted, a new byte is loaded into the shift register (if available in the transmit buffer). If the transmit buffer is empty, then the shift register also remains empty. The TXC flag in I2Cn\_STATUS and the TXC interrupt flags in I2Cn\_IF are then set, signaling that the transmit shift register is out of data. TXC is cleared when new data becomes available, but the TXC interrupt flag must be cleared by software.



**Figure 18.13. I2C Transmit Buffer Operation**

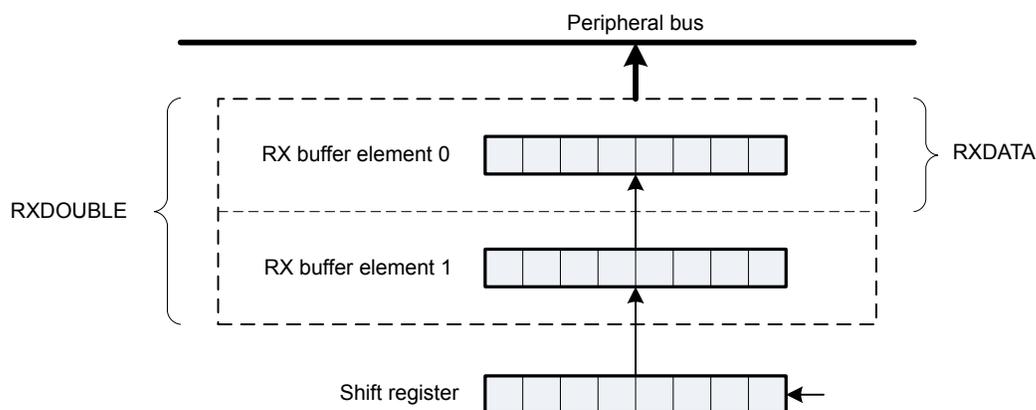
The TXBL flags in the I2Cn\_STATUS and I2Cn\_IF are used to indicate the level of the transmit buffer. TXBIL in I2Cn\_CTRL controls the level at which these flag bits are set. If TXBIL is cleared, the flags are set whenever the transmit buffer becomes empty (used when transmitting using I2Cn\_TXDOUBLE). If TXBIL is set, the flags are set whenever the transmit buffer goes from full to half-empty or empty (used when transmitting with I2Cn\_TXDATA). Both the TXBL status flag and the TXBL interrupt flag are cleared automatically when the condition becomes false.

If an attempt is made to write more bytes to the transmit buffer than the space available, the TXOF interrupt flag in I2Cn\_IF is set, indicating the overflow. The data already in the buffer remains preserved, and no new data is written.

The transmit buffer and the transmit shift register can be cleared by setting command bit CLEAR\_TX in I2Cn\_CMD. This will prevent the I<sup>2</sup>C module from transmitting the data in the buffer and the shift register, and will make them available for new data. Any byte currently being transmitted will not be aborted. Transmission of this byte will be completed.

### 18.3.6.2 Receive Buffer and Shift Register

The I<sup>2</sup>C receiver uses a 2-level FIFO receive buffer and a receive shift register as shown in [Figure 18.14 I2C Receive Buffer Operation on page 527](#). When a byte has been fully received by the receive shift register, it is loaded into the receive buffer if there is room for it, making the shift register empty to receive another byte. Otherwise, the byte waits in the shift register until space becomes available in the buffer.



**Figure 18.14. I2C Receive Buffer Operation**

When a byte becomes available in the receive buffer, the RXDATAV in I2Cn\_STATUS and RXDATAV interrupt flag in I2Cn\_IF are set. When the buffer becomes full, RXFULL in the I2Cn\_STATUS and I2Cn\_IF are set. The status flags RXDATAV and RXFULL are automatically cleared by hardware when their condition is no longer true. This also goes for the RXDATAV interrupt flag, but the RXFULL interrupt flag must be cleared by software. When the RXFULL flag is set, notifying that the buffer is full, space is still available in the receive shift register for one more byte.

The data can be fetched from the buffer in two ways. I2Cn\_RXDATA gives access to the received byte (if two bytes are received then the one received first is fetched first). I2Cn\_RXDOUBLE makes it possible to read the two received bytes simultaneously. If an attempt is made to read more bytes from the buffer than available, the RXUF interrupt flag in I2Cn\_IF is set to signal the underflow, and the data read from the buffer is undefined.

When using I2Cn\_RXDOUBLE to pick data, AUTOACK in I2Cn\_CTRL should be set to 1. This ensures that an ACK is automatically sent out after the first byte is received so that the reception of the next byte can begin. In order to stop receiving data bytes, a NACK must be sent out through the I2Cn\_CMD register.

I2Cn\_RXDATAP and I2Cn\_RXDOUBLEP can be used to read data from the receive buffer without removing it from the buffer. The RXUF interrupt flag in I2Cn\_IF will never be set as a result of reading from I2Cn\_RXDATAP and I2Cn\_RXDOUBLEP, but the data read through I2Cn\_RXDATAP when the receive buffer is empty is still undefined.

Once a transaction is complete (STOP sent or received), the receive buffer needs to be flushed (all received data must be read) before starting a new transaction.

### 18.3.7 Master Operation

A bus transaction is initiated by transmitting a START condition (S) on the bus. This is done by setting the START bit in I2Cn\_CMD. The command schedules a START condition, and makes the I<sup>2</sup>C module generate a start condition whenever the bus becomes free.

The I<sup>2</sup>C-bus is considered busy whenever another device on the bus transmits a START condition. Until a STOP condition is detected, the bus is owned by the master issuing the START condition. The bus is considered free when a STOP condition is transmitted on the bus. After a STOP is detected, all masters that have data to transmit send a START condition and begin transmitting data. Arbitration ensures that collisions are avoided.

When the START condition has been transmitted, the master must transmit a slave address (ADDR) with an R/W bit on the bus. If this address is available in the transmit buffer, the master transmits it immediately, but if the buffer is empty, the master holds the I<sup>2</sup>C-bus while waiting for software to write the address to the transmit buffer.

After the address has been transmitted, a sequence of bytes can be read from or written to the slave, depending on the value of the R/W bit (bit 0 in the address byte). If the bit was cleared, the master has entered a master transmitter role, where it now transmits data to the slave. If the bit was set, it has entered a master receiver role, where it now should receive data from the slave. In either case, an unlimited number of bytes can be transferred in one direction during the transmission.

At the end of the transmission, the master either transmits a repeated START condition (Sr) if it wishes to continue with another transfer, or transmits a STOP condition (P) if it wishes to release the bus. When operating in the master mode, HFPERCLK frequency must be higher than 2 MHz for Standard-mode, 9 MHz for Fast-mode, and 20 MHz for Fast-mode Plus.

### 18.3.7.1 Master State Machine

The master state machine is shown in [Figure 18.15 I2C Master State Machine on page 529](#). A master operation starts in the far left of the state machine, and follows the solid lines through the state machine, ending the operation or continuing with a new operation when arriving at the right side of the state machine.

Branches in the path through the state machine are the results of bus events and choices made by software, either directly or indirectly. The dotted lines show where I<sup>2</sup>C-specific interrupt flags are set along the path and the full-drawn circles show places where interaction may be required by software to let the transmission proceed.

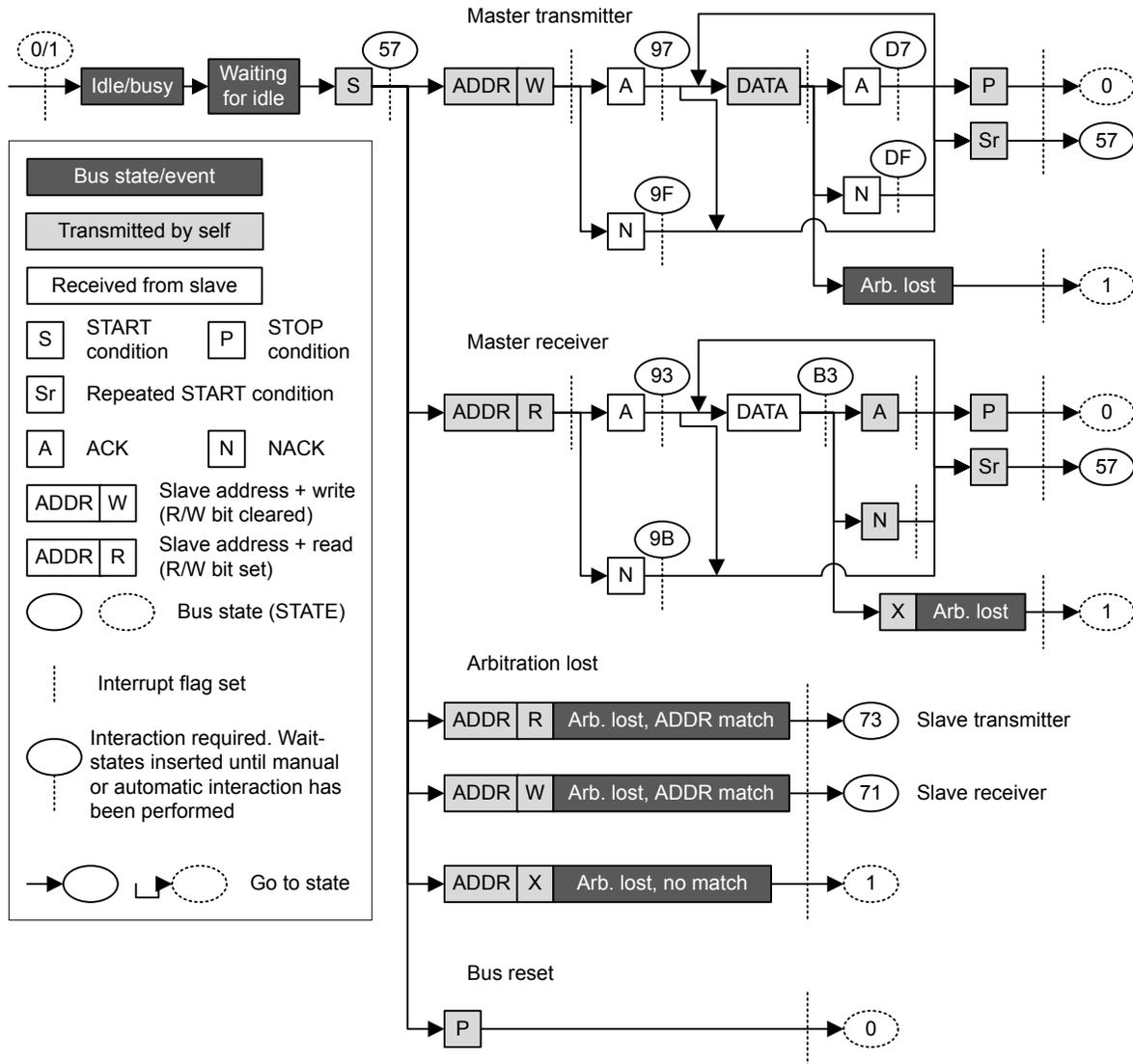


Figure 18.15. I2C Master State Machine

### 18.3.7.2 Interactions

Whenever the I<sup>2</sup>C module is waiting for interaction from software, it holds the bus clock SCL low, freezing all bus activities, and the BUSHOLD interrupt flag in I2Cn\_IF is set. The action(s) required by software depends on the current state the of the I<sup>2</sup>C module. This state can be read from the I2Cn\_STATE register.

As an example, [Table 18.3 I2C Master Transmitter on page 532](#) shows the different states the I<sup>2</sup>C goes through when operating as a Master Transmitter, i.e., a master that transmits data to a slave. As seen in the table, when a start condition has been transmitted, a requirement is that there is an address and an R/W bit in the transmit buffer. If the transmit buffer is empty, then the BUSHOLD interrupt flag is set, and the bus is held until data becomes available in the buffer. While waiting for the address, I2Cn\_STATE has a value 0x57, which can be used to identify exactly what the I<sup>2</sup>C module is waiting for.

**Note:** The bus would never stop at state 0x57 if the address was available in the transmit buffer.

The different interactions used by the I<sup>2</sup>C module are listed in [Table 18.2 I2C Interactions in Prioritized Order on page 530](#) in a prioritized order. If the I<sup>2</sup>C module is in such a state that multiple courses of action are possible, then the action chosen is the one that has the highest priority. For example, after sending out a START, if an address is present in the buffer and a STOP is also pending, then the I<sup>2</sup>C will send out the STOP since it has the higher priority.

**Table 18.2. I2C Interactions in Prioritized Order**

| Interaction      | Priority | Software action  | Automatically continues if  |
|------------------|----------|--|---|
| STOP*            | 1        | Set the STOP command bit in I2Cn_CMD                             | PSTOP is set (STOP pending) in I2Cn_STATUS                              |
| ABORT            | 2        | Set the ABORT command bit in I2Cn_CMD                            | Never, the transmission is aborted                                      |
| CONT*            | 3        | Set the CONT command bit in I2Cn_CMD                             | PCONT is set in I2Cn_STATUS (CONT pending)                              |
| NACK*            | 4        | Set the NACK command bit in I2Cn_CMD                             | PNACK is set in I2Cn_STATUS (NACK pending)                              |
| ACK*             | 5        | Set the ACK command bit in I2Cn_CMD                              | AUTOACK is set in I2Cn_CTRL or PACK is set in I2Cn_STATUS (ACK pending) |
| ADDR+W -> TXDATA | 6        | Write an address to the transmit buffer with the R/W bit set     | Address is available in transmit buffer with R/W bit set                |
| ADDR+R -> TXDATA | 7        | Write an address to the transmit buffer with the R/W bit cleared | Address is available in transmit buffer with R/W bit cleared            |
| START*           | 8        | Set the START command bit in I2Cn_CMD                            | PSTART is set in I2Cn_STATUS (START pending)                            |
| TXDATA/ TXDOUBLE | 9        | Write data to the transmit buffer                                | Data is available in transmit buffer                                    |
| RXDATA/ RXDOUBLE | 10       | Read data from receive buffer                                    | Space is available in receive buffer                                    |
| None             | 11       | No interaction is required                                       |   |

The commands marked with a \* in [Table 18.2 I2C Interactions in Prioritized Order on page 530](#) can be issued before an interaction is required. When such a command is issued before it can be used/consumed by the I<sup>2</sup>C module, the command is set in a pending state, which can be read from the STATUS register. A pending START command can for instance be identified by PSTART having a high value.

Whenever the I<sup>2</sup>C module requires an interaction, it checks the pending commands. If one or a combination of these can fulfill an interaction, they are consumed by the module and the transmission continues without setting the BUSHOLD interrupt flag in I2Cn\_IF to get an interaction from software. The pending status of a command goes low when it is consumed.

When several interactions are possible from a set of pending commands, the interaction with the highest priority, i.e., the interaction closest to the top of [Table 18.2 I2C Interactions in Prioritized Order on page 530](#) is applied to the bus.

Pending commands can be cleared by setting the CLEARPC command bit in I2Cn\_CMD.

### 18.3.7.3 Automatic ACK Interaction

When receiving addresses and data, an ACK command in I2Cn\_CMD is normally required after each received byte. When AUTOACK is set in I2Cn\_CTRL, an ACK is always pending, and the ACK-pending bit PACK in I2Cn\_STATUS is thus always set, even after an ACK has been consumed. This is used when data is picked using I2Cn\_RXDOUBLE and can also be used with I2Cn\_RXDATA in order to reduce the amount of software interaction required during a transfer.

### 18.3.7.4 Reset State

After a reset, the state of the I<sup>2</sup>C-bus is unknown. To avoid interrupting transfers on the I<sup>2</sup>C-bus after a reset of the I<sup>2</sup>C module or the entire MCU, the I<sup>2</sup>C-bus is assumed to be busy when coming out of a reset, and the BUSY flag in I2Cn\_STATUS is thus set. To be able to carry through master operations on the I<sup>2</sup>C-bus, the bus must be idle.

The bus goes idle when a STOP condition is detected on the bus, but on buses with little activity, the time before the I<sup>2</sup>C module detects that the bus is idle can be significant. There are two ways of assuring that the I<sup>2</sup>C module gets out of the busy state.

- Use the ABORT command in I2Cn\_CMD. When the ABORT command is issued, the I<sup>2</sup>C module is instructed that the bus is idle. The I<sup>2</sup>C module can then initiate master operations.
- Use the Bus Idle Timeout. When SCL has been high for a long period of time, it is very likely that the bus is idle. Set BITO in I2Cn\_CTRL to an appropriate timeout period and set GIBITO in I2Cn\_CTRL. If activity has not been detected on the bus within the timeout period, the bus is then automatically assumed idle, and master operations can be initiated.

**Note:** If operating in slave mode, the above approach is not necessary.

### 18.3.7.5 Master Transmitter

To transmit data to a slave, the master must operate as a master transmitter. [Table 18.3 I2C Master Transmitter on page 532](#) shows the states the I<sup>2</sup>C module goes through while acting as a master transmitter. Every state where an interaction is required has the possible interactions listed, along with the result of the interactions. The table also shows which interrupt flags are set in the different states. The interrupt flags enclosed in parenthesis may be set. If the BUSHOLD interrupt in I2Cn\_IF is set, the module is waiting for an interaction, and the bus is frozen. The value of I2Cn\_STATE will be equal to the values given in the table when the BUSHOLD interrupt flag is set, and can be used to determine which interaction is required to make the transmission continue.

The interrupt flag START in I2Cn\_IF is set when the I<sup>2</sup>C module transmits the START.

A master operation is started by issuing a START command by setting START in I2Cn\_CMD. ADDR+W, i.e., the address of the slave + the R/W bit is then required by the I<sup>2</sup>C module. If this is not available in the transmit buffer, then the bus is held and the BUSHOLD interrupt flag is set. The value of I2Cn\_STATE will then be 0x57. As seen in the table, the I<sup>2</sup>C module also stops in this state if the address is not available after a repeated start condition.

To continue, write a byte to I2Cn\_TXDATA with the address of the slave in the 7 most significant bits and the least significant bit cleared (ADDR+W). This address will then be transmitted, and the slave will reply with an ACK or a NACK. If no slave replies to the address, the response will also be NACK. If the address was acknowledged, the master now has four choices. It can send data by placing it in I2Cn\_TXDATA/ I2Cn\_TXDOUBLE (the master should check the TXBL interrupt flag before writing to the transmit buffer), this data is then transmitted. The master can also stop the transmission by sending a STOP, it can send a repeated start by sending START, or it can send a STOP and then a START as soon as possible. If the master wishes to make another transfer immediately after the current, the preferred way is to start a new transfer directly by transmitting a repeated START instead of a STOP followed by a START. This is so because if a STOP is sent out, then any master wishing to initiate a transfer on the bus can try to gain control of it.

If a NACK was received, the master has to issue a CONT command in addition to providing data in order to continue transmission. This is not standard I<sup>2</sup>C, but is provided for flexibility. The rest of the options are similar to when an ACK was received.

If a new byte was transmitted, an ACK or NACK is received after the transmission of the byte, and the master has the same options as for when the address was sent.

The master may lose arbitration at any time during transmission. In this case, the ARBLOST interrupt flag in I2Cn\_IF is set. If the arbitration was lost during the transfer of an address, and SLAVE in I2Cn\_CTRL is set, the master then checks which address was transmitted. If it was the address of the master, then the master goes to slave mode.

After a master has transmitted a START and won any arbitration, it owns the bus until it transmits a STOP. After a STOP, the bus is released, and arbitration decides which bus master gains the bus next. The MSTOP interrupt flag in I2Cn\_IF is set when a STOP condition is transmitted by the master.

**Table 18.3. I2C Master Transmitter**

| I2Cn_STATE | Description                | I2Cn_IF                                       | Required interaction | Response   |
|------------|----------------------------|---|----------------------|--|
| 0x57       | Start transmitted          | START interrupt flag (BUSHOLD interrupt flag) | ADDR+W -> TXDATA     | ADDR+W will be sent  |
|            |                            |   | STOP                 | STOP will be sent and bus released.  |
|            |                            |   | STOP + START         | STOP will be sent and bus released. Then a START will be sent when bus becomes idle. |
| 0x57       | Repeated start transmitted | START interrupt flag (BUSHOLD interrupt flag) | ADDR+W -> TXDATA     | ADDR+W will be sent  |
|            |                            |   | STOP                 | STOP will be sent and bus released.  |
|            |                            |   | STOP + START         | STOP will be sent and bus released. Then a START will be sent when bus becomes idle. |
| -          | ADDR+W transmitted         | TXBL interrupt flag (TXC interrupt flag)      | None                 |  |

| I2Cn_STATE | Description                       | I2Cn_IF                                     | Required interaction | Response  |
|------------|-----------------------------------|---|----------------------|---|
| 0x97       | ADDR+W transmitted, ACK received  | ACK interrupt flag (BUSHOLD interrupt flag) | TXDATA               | DATA will be sent   |
|            |                                   |   | STOP                 | STOP will be sent. Bus will be released   |
|            |                                   |   | START                | Repeated start condition will be sent   |
|            |                                   |   | STOP + START         | STOP will be sent and the bus released. Then a START will be sent when the bus becomes idle |
| 0x9F       | ADDR+W transmitted, NACK received | NACK (BUSHOLD interrupt flag)               | CONT + TXDATA        | DATA will be sent   |
|            |                                   |   | STOP                 | STOP will be sent. Bus will be released   |
|            |                                   |   | START                | Repeated start condition will be sent   |
|            |                                   |   | STOP + START         | STOP will be sent and the bus released. Then a START will be sent when the bus becomes idle |
| -          | Data transmitted                  | TXBL interrupt flag (TXC interrupt flag)    | None                 |   |
| 0xD7       | Data transmitted, ACK received    | ACK interrupt flag (BUSHOLD interrupt flag) | TXDATA               | DATA will be sent   |
|            |                                   |   | STOP                 | STOP will be sent. Bus will be released   |
|            |                                   |   | START                | Repeated start condition will be sent   |
|            |                                   |   | STOP + START         | STOP will be sent and the bus released. Then a START will be sent when the bus becomes idle |
| 0xDF       | Data transmitted, NACK received   | NACK (BUSHOLD interrupt flag)               | CONT + TXDATA        | DATA will be sent   |
|            |                                   |   | STOP                 | STOP will be sent. Bus will be released   |
|            |                                   |   | START                | Repeated start condition will be sent   |
|            |                                   |   | STOP + START         | STOP will be sent and the bus released. Then a START will be sent when the bus becomes idle |
| -          | Stop transmitted                  | MSTOP interrupt flag                        | None                 |   |
|            |                                   |   | START                | START will be sent when bus becomes idle  |
| -          | Arbitration lost                  | ARBLOST interrupt flag                      | None                 |   |
|            |                                   |   | START                | START will be sent when bus becomes idle  |

### 18.3.7.6 Master Receiver

To receive data from a slave, the master must operate as a master receiver, see [Table 18.4 I2C Master Receiver on page 534](#). This is done by transmitting ADDR+R as the address byte instead of ADDR+W, which is transmitted to become a master transmitter. The address byte loaded into the data register thus has to contain the 7-bit slave address in the 7 most significant bits of the byte, and have the least significant bit set.

When the address has been transmitted, the master receives an ACK or a NACK. If an ACK is received, the ACK interrupt flag in I2Cn\_IF is set, and if space is available in the receive shift register, reception of a byte from the slave begins. If the receive buffer and shift register is full however, the bus is held until data is read from the receive buffer or another interaction is made. Note that the STOP and START interactions have a higher priority than the data-available interaction, so if a STOP or START command is pending, the highest priority interaction will be performed, and data will not be received from the slave.

If a NACK was received, the CONT command in I2Cn\_CMD has to be issued in order to continue receiving data, even if there is space available in the receive buffer and/or shift register.

After a data byte has been received the master must ACK or NACK the received byte. If an ACK is pending or AUTOACK in I2Cn\_CTRL is set, an ACK is sent automatically and reception continues if space is available in the receive buffer.

If a NACK is sent, the CONT command must be used in order to continue transmission. If an ACK or NACK is issued along with a START or STOP or both, then the ACK/NACK is transmitted and the reception is ended. If START in I2Cn\_CMD is set alone, a repeated start condition is transmitted after the ACK/NACK. If STOP in I2Cn\_CMD is set, a stop condition is sent regardless of whether START is set. If START is set in this case, it is set as pending.

As when operating as a master transmitter, arbitration can be lost as a master receiver. When this happens the ARBLOST interrupt flag in I2Cn\_IF is set, and the master has a possibility of being selected as a slave given the correct conditions.

**Table 18.4. I2C Master Receiver**

| I2Cn_STATE | Description                       | I2Cn_IF                                       | Required interaction | Response  |
|------------|-----------------------------------|---|----------------------|---|
| 0x57       | START transmitted                 | START interrupt flag (BUSHOLD interrupt flag) | ADDR+R -> TXDATA     | ADDR+R will be sent   |
|            |                                   |   | STOP                 | STOP will be sent and bus released.   |
|            |                                   |   | STOP + START         | STOP will be sent and bus released. Then a START will be sent when bus becomes idle.        |
| 0x57       | Repeated START transmitted        | START interrupt flag (BUSHOLD interrupt flag) | ADDR+R -> TXDATA     | ADDR+R will be sent   |
|            |                                   |   | STOP                 | STOP will be sent and bus released.   |
|            |                                   |   | STOP + START         | STOP will be sent and bus released. Then a START will be sent when bus becomes idle.        |
| -          | ADDR+R transmitted                | TXBL interrupt flag (TXC interrupt flag)      | None                 |   |
| 0x93       | ADDR+R transmitted, ACK received  | ACK interrupt flag (BUSHOLD)                  | RXDATA               | Start receiving   |
|            |                                   |   | STOP                 | STOP will be sent and the bus released  |
|            |                                   |   | START                | Repeated START will be sent   |
|            |                                   |   | STOP + START         | STOP will be sent and the bus released. Then a START will be sent when the bus becomes idle |
| 0x9B       | ADDR+R transmitted, NACK received | NACK (BUSHOLD)                                | CONT + RXDATA        | Continue, start receiving   |
|            |                                   |   | STOP                 | STOP will be sent and the bus released  |
|            |                                   |   | START                | Repeated START will be sent   |
|            |                                   |   | STOP + START         | STOP will be sent and the bus released. Then a START will be sent when the bus becomes idle |

| I2Cn_STATE | Description      | I2Cn_IF                                       | Required interaction    | Response  |
|------------|------------------|---|-------------------------|---|
| 0xB3       | Data received    | RXDATA interrupt flag(BUSHOLD interrupt flag) | ACK + RXDATA            | ACK will be transmitted, reception continues  |
|            |                  |   | NACK + CONT + RXDATA    | NACK will be transmitted, reception continues   |
|            |                  |   | ACK/NACK + STOP         | ACK/NACK will be sent and the bus will be released.   |
|            |                  |   | ACK/NACK + START        | ACK/NACK will be sent, and then a repeated start condition.   |
|            |                  |   | ACK/NACK + STOP + START | ACK/NACK will be sent and the bus will be released. Then a START will be sent when the bus becomes idle |
| -          | Stop received    | MSTOP interrupt flag                          | None                    |   |
|            |                  |   | START                   | START will be sent when bus becomes idle  |
| -          | Arbitration lost | ARBLOST interrupt flag                        | None                    |   |
|            |                  |   | START                   | START will be sent when bus becomes idle  |

### 18.3.8 Bus States

The I2Cn\_STATE register can be used to determine which state the I<sup>2</sup>C module and the I<sup>2</sup>C bus are in at a given time. The register consists of the STATE bit-field, which shows which state the I<sup>2</sup>C module is at in any ongoing transmission, and a set of single-bits, which reveal the transmission mode, whether the bus is busy or idle, and whether the bus is held by this I<sup>2</sup>C module waiting for a software response.

The possible values of the STATE field are summarized in [Table 18.5 I2C STATE Values on page 536](#). When this field is cleared, the I<sup>2</sup>C module is not a part of any ongoing transmission. The remaining status bits in the I2Cn\_STATE register are listed in [Table 18.6 I2C Transmission Status on page 536](#).

**Table 18.5. I2C STATE Values**

| Mode    | Value | Description   |
|---------|-------|---|
| IDLE    | 0     | No transmission is being performed by this module.                        |
| WAIT    | 1     | Waiting for idle. Will send a start condition as soon as the bus is idle. |
| START   | 2     | Start being transmitted   |
| ADDR    | 3     | Address being transmitted or has been received                            |
| ADDRACK | 4     | Address ACK/NACK being transmitted or received                            |
| DATA    | 5     | Data being transmitted or received  |
| DATAACK | 6     | Data ACK/NACK being transmitted or received                               |

**Table 18.6. I2C Transmission Status**

| Bit         | Description   |
|-------------|---|
| BUSY        | Set whenever there is activity on the bus. Whether or not this module is responsible for the activity cannot be determined by this byte.            |
| MASTER      | Set when operating as a master. Cleared at all other times.   |
| TRANSMITTER | Set when operating as a transmitter; either a master transmitter or a slave transmitter. Cleared at all other times                                 |
| BUSHOLD     | Set when the bus is held by this I <sup>2</sup> C module because an action is required by software.   |
| NACK        | Only valid when bus is held and STATE is ADDRACK or DATAACK. In that case it is set if a NACK was received. In all other cases, the bit is cleared. |

**Note:** I2Cn\_STATE reflects the internal state of the I<sup>2</sup>C module, and therefore only held constant as long as the bus is held, i.e., as long as BUSHOLD in I2Cn\_STATUS is set.

### 18.3.9 Slave Operation

The I<sup>2</sup>C module operates in master mode by default. To enable slave operation, i.e., to allow the device to be addressed as an I<sup>2</sup>C slave, the SLAVE bit in I2Cn\_CTRL must be set. In this case the I<sup>2</sup>C module operates in a mixed mode, both capable of starting transmissions as a master, and being addressed as a slave. When operating in the slave mode, HFPERCLK frequency must be higher than 2 MHz for Standard-mode, 5 MHz for Fast-mode, and 14 MHz for Fast-mode Plus.

### 18.3.9.1 Slave State Machine

The slave state machine is shown in [Figure 18.16 I<sup>2</sup>C Slave State Machine on page 537](#). The dotted lines show where I<sup>2</sup>C-specific interrupt flags are set. The full-drawn circles show places where interaction may be required by software to let the transmission proceed.

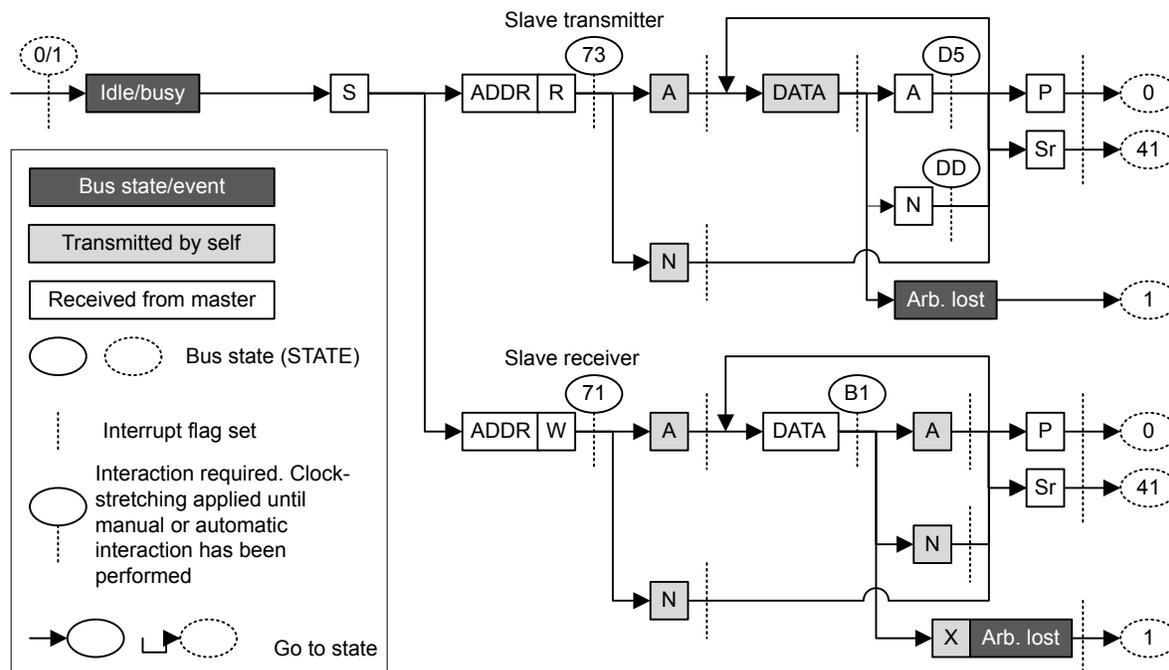


Figure 18.16. I<sup>2</sup>C Slave State Machine

### 18.3.9.2 Address Recognition

The I<sup>2</sup>C module provides automatic address recognition for 7-bit addresses. 10-bit address recognition is not fully automatic, but can be assisted by the 7-bit address comparator as shown in [18.3.11 Using 10-bit Addresses](#). Address recognition is supported in all energy modes (except EM4).

The slave address, i.e., the address which the I<sup>2</sup>C module should be addressed with, is defined in the I2Cn\_SADDR register. In addition to the address, a mask must be specified, telling the address comparator which bits of an incoming address to compare with the address defined in I2Cn\_SADDR. The mask is defined in I2Cn\_SADDRMASK, and for every zero in the mask, the corresponding bit in the slave address is treated as a don't-care, i.e., the 0-masked bits are ignored.

An incoming address that fails address recognition is automatically replied to with a NACK. Since only the bits defined by the mask are checked, a mask with a value 0x00 will result in all addresses being accepted. A mask with a value 0x7F will only match the exact address defined in I2Cn\_SADDR, while a mask 0x70 will match all addresses where the three most significant bits in I2Cn\_SADDR and the incoming address are equal.

If GCAMEN in I2Cn\_CTRL is not set, the start-byte, i.e., the general call address with the R/W bit set is ignored unless it is included in the defined slave address and the address mask.

When an address is accepted by the address comparator, the decision of whether to ACK or NACK the address is passed to software.

### 18.3.9.3 Slave Transmitter

When SLAVE in I2Cn\_CTRL is set, the RSTART interrupt flag in I2Cn\_IF will be set when repeated START conditions are detected. After a START or repeated START condition, the bus master will transmit an address along with an R/W bit. If there is no room in the receive shift register for the address, the bus will be held by the slave until room is available in the shift register. Transmission then continues and the address is loaded into the shift register. If this address does not pass address recognition, it is automatically NACK'ed by the slave, and the slave goes to an idle state. The address byte is in this case discarded, making the shift register ready for a new address. It is not loaded into the receive buffer.

If the address was accepted and the R/W bit was set (R), indicating that the master wishes to read from the slave, the slave now goes into the slave transmitter mode. Software interaction is now required to decide whether the slave wants to acknowledge the request or not. The accepted address byte is loaded into the receive buffer like a regular data byte. If no valid interaction is pending, the bus is held until the slave responds with a command. The slave can reject the request with a single NACK command.

The slave will in that case go to an idle state, and wait for the next start condition. To continue the transmission, the slave must make sure data is loaded into the transmit buffer and send an ACK. The loaded data will then be transmitted to the master, and an ACK or NACK will be received from the master.

Data transmission can also continue after a NACK if a CONT command is issued along with the NACK. This is not standard I<sup>2</sup>C however.

If the master responds with an ACK, it may expect another byte of data, and data should be made available in the transmit buffer. If data is not available, the bus is held until data is available.

If the response is a NACK however, this is an indication of that the master has received enough bytes and wishes to end the transmission. The slave now automatically goes idle, unless CONT in I2Cn\_CMD is set and data is available for transmission. The latter is not standard I<sup>2</sup>C.

The master ends the transmission by sending a STOP or a repeated START. The SSTOP interrupt flag in I2Cn\_IF is set when the master transmits a STOP condition. If the transmission is ended with a repeated START, then the SSTOP interrupt flag is not set.

**Note:** The SSTOP interrupt flag in I2Cn\_IF will be set regardless of whether the slave is participating in the transmission or not, as long as SLAVE in I2Cn\_CTRL is set and a STOP condition is detected.

If arbitration is lost at any time during transmission, the ARBLOST interrupt flag in I2Cn\_IF is set, the bus is released and the slave goes idle.

See [Table 18.7 I2C Slave Transmitter on page 538](#) for more information.

**Table 18.7. I2C Slave Transmitter**

| I2Cn_STATE | Description                     | I2Cn_IF  | Required interaction | Response                           |
|------------|---------------------------------|--|----------------------|------------------------------------|
| 0x41       | Repeated START received         | RSTART interrupt flag (BUSHOLD interrupt flag) | RXDATA               | Receive and compare address        |
| 0x75       | ADDR + R received               | ADDR interrupt flag                            | ACK + TXDATA         | ACK will be sent, then DATA        |
|            |                                 | RXDATA interrupt flag                          | NACK                 | NACK will be sent, slave goes idle |
|            |                                 | (BUSHOLD interrupt flag)                       | NACK + CONT + TXDATA | NACK will be sent, then DATA.      |
| -          | Data transmitted                | TXBL interrupt flag (TXC interrupt flag)       | None                 |                                    |
| 0xD5       | Data transmitted, ACK received  | ACK interrupt flag (BUSHOLD interrupt flag)    | TXDATA               | DATA will be transmitted           |
| 0xDD       | Data transmitted, NACK received | NACK interrupt flag                            | None                 | The slave goes idle                |
|            |                                 | (BUSHOLD interrupt flag)                       | CONT + TXDATA        | DATA will be transmitted           |

| I2Cn_STATE | Description      | I2Cn_IF                | Required interaction | Response                                     |
|------------|------------------|------------------------|----------------------|--|
| -          | Stop received    | SSTOP interrupt flag   | None                 | The slave goes idle                          |
|            |                  |                        | START                | START will be sent when bus becomes idle     |
| -          | Arbitration lost | ARBLOST interrupt flag | None                 | The slave goes idle                          |
|            |                  |                        | START                | START will be sent when the bus becomes idle |

### 18.3.9.4 Slave Receiver

A slave receiver operation is started in the same way as a slave transmitter operation, with the exception that the address transmitted by the master has the R/W bit cleared (W), indicating that the master wishes to write to the slave. The slave then goes into slave receiver mode.

To receive data from the master, the slave should respond to the address with an ACK and make sure space is available in the receive buffer. Transmission will then continue, and the slave will receive a byte from the master.

If a NACK is sent without a CONT, the transmission is ended for the slave, and it goes idle. If the slave issues both the NACK and CONT commands and has space available in the receive buffer, it will be open for continuing reception from the master.

When a byte has been received from the master, the slave must ACK or NACK the byte. The responses here are the same as for the reception of the address byte.

The master ends the transmission by sending a STOP or a repeated START. The SSTOP interrupt flag is set when the master transmits a STOP condition. If the transmission is ended with a repeated START, then the SSTOP interrupt flag in I2Cn\_IF is not set.

**Note:** The SSTOP interrupt flag in I2Cn\_IF will be set regardless of whether the slave is participating in the transmission or not, as long as SLAVE in I2Cn\_CTRL is set and a STOP condition is detected

If arbitration is lost at any time during transmission, the ARBLOST interrupt flag in I2Cn\_IF is set, the bus is released and the slave goes idle.

See [Table 18.8 I2C - Slave Receiver on page 540](#) for more information.

**Table 18.8. I2C - Slave Receiver**

| I2Cn_STATE | Description             | I2Cn_IF   | Required interaction | Response                                     |
|------------|-------------------------|---|----------------------|--|
| -          | Repeated START received | RSTART interrupt flag (BUSHOLD interrupt flag)                        | RXDATA               | Receive and compare address                  |
| 0x71       | ADDR + W received       | ADDR interrupt flag<br>RXDATA interrupt flag (BUSHOLD interrupt flag) | ACK + RXDATA         | ACK will be sent and data will be received   |
|            |                         |   | NACK                 | NACK will be sent, slave goes idle           |
|            |                         |   | NACK + CONT + RXDATA | NACK will be sent and DATA will be received. |
| 0xB1       | Data received           | RXDATA interrupt flag (BUSHOLD interrupt flag)                        | ACK + RXDATA         | ACK will be sent and data will be received   |
|            |                         |   | NACK                 | NACK will be sent and slave will go idle     |
|            |                         |   | NACK + CONT + RXDATA | NACK will be sent and data will be received  |
| -          | Stop received           | SSTOP interrupt flag  | None                 | The slave goes idle                          |
|            |                         |   | START                | START will be sent when bus becomes idle     |
| -          | Arbitration lost        | ARBLOST interrupt flag  | None                 | The slave goes idle                          |
|            |                         |   | START                | START will be sent when the bus becomes idle |

### 18.3.10 Transfer Automation

The I<sup>2</sup>C can be set up to complete transfers with a minimal amount of interaction.

### 18.3.10.1 DMA

DMA can be used to automatically load data into the transmit buffer and load data out from the receive buffer. When using DMA, software is thus relieved of moving data to and from memory after each transferred byte.

### 18.3.10.2 Automatic ACK

When AUTOACK in I2Cn\_CTRL is set, an ACK is sent automatically whenever an ACK interaction is possible and no higher priority interactions are pending.

### 18.3.10.3 Automatic STOP

A STOP can be generated automatically on two conditions. These apply only to the master transmitter.

If AUTOSN in I2Cn\_CTRL is set, the I<sup>2</sup>C module ends a transmission by transmitting a STOP condition when operating as a master transmitter and a NACK is received.

If AUTOSE in I2Cn\_CTRL is set, the I<sup>2</sup>C module always ends a transmission when there is no more data in the transmit buffer. If data has been transmitted on the bus, the transmission is ended after the (N)ACK has been received by the slave. If a START is sent when no data is available in the transmit buffer and AUTOSE is set, then the STOP condition is sent immediately following the START. Software must thus make sure data is available in the transmit buffer before the START condition has been fully transmitted if data is to be transferred.

### 18.3.11 Using 10-bit Addresses

When using 10-bit addresses in slave mode, set the I2Cn\_SADDR register to 1111 0XX where XX are the two most significant bits of the 10-bit address, and set I2Cn\_SADDRMASK to 0xFF. Address matches will now be given on all 10-bit addresses where the two most significant bits are correct.

When receiving an address match, the slave must acknowledge the address and receive the first data byte. This byte contains the second part of the 10-bit address. If it matches the address of the slave, the slave should ACK the byte to continue the transmission, and if it does not match, the slave should NACK it.

When the master is operating as a master transmitter, the data bytes will follow after the second address byte. When the master is operating as a master receiver however, a repeated START condition is sent after the second address byte. The address sent after this repeated START is equal to the first of the address bytes transmitted previously, but now with the R/W byte set, and only the slave that found a match on the entire 10-bit address in the previous message should ACK this address. The repeated start should take the master into a master receiver mode, and after the single address byte sent this time around, the slave begins transmission to the master.

### 18.3.12 Error Handling

**Note:** The setting of GCAMEN and SLAVE fields in the I2Cn\_CTRL register and the registers I2Cn\_SADDR and I2Cn\_ROUTELOC0 are considered static. This means that these need to be set before an I<sup>2</sup>C transaction starts and need to stay stable during the entire transaction.

#### 18.3.12.1 ABORT Command

Some bus errors may require software intervention to be resolved. The I<sup>2</sup>C module provides an ABORT command, which can be set in I2Cn\_CMD, to help resolve bus errors.

When the bus for some reason is locked up and the I<sup>2</sup>C module is in the middle of a transmission it cannot get out of, or for some other reason the I<sup>2</sup>C wants to abort a transmission, the ABORT command can be used.

Setting the ABORT command will make the I<sup>2</sup>C module discard any data currently being transmitted or received, release the SDA and SCL lines and go to an idle mode. ABORT effectively makes the I<sup>2</sup>C module forget about any ongoing transfers.

#### 18.3.12.2 Bus Reset

A bus reset can be performed by setting the START and STOP commands in I2Cn\_CMD while the transmit buffer is empty. A START condition will then be transmitted, immediately followed by a STOP condition. A bus reset can also be performed by transmitting a START command with the transmit buffer empty and AUTOSE set.

### 18.3.12.3 I<sup>2</sup>C-Bus Errors

An I<sup>2</sup>C-bus error occurs when a START or STOP condition is misplaced, which happens when the value on SDA changes while SCL is high during bit-transmission on the I<sup>2</sup>C-bus. If the I<sup>2</sup>C module is part of the current transmission when a bus error occurs, any data currently being transmitted or received is discarded, SDA and SCL are released, the BUSERR interrupt flag in I2Cn\_IF is set to indicate the error, and the module automatically takes a course of action as defined in [Table 18.9 I<sup>2</sup>C Bus Error Response on page 542](#).

**Table 18.9. I<sup>2</sup>C Bus Error Response**

|                             | Misplaced START                    | Misplaced STOP                        |
|-----------------------------|------------------------------------|---------------------------------------|
| In a master/slave operation | Treated as START. Receive address. | Go idle. Perform any pending actions. |

### 18.3.12.4 Bus Lockup

A lockup occurs when a master or slave on the I<sup>2</sup>C-bus has locked the SDA or SCL at a low value, preventing other devices from putting high values on the bus, and thus making communication on the bus impossible.

Many slave-only devices operating on an I<sup>2</sup>C-bus are not capable of driving SCL low, but in the rare case that SCL is stuck LOW, the advice is to apply a hardware reset signal to the slaves on the bus. If this does not work, cycle the power to the devices in order to make them release SCL.

When SDA is stuck low and SCL is free, a master should send 9 clock pulses on SCL while tristating the SDA. This procedure is performed in the GPIO module after clearing the I2C\_ROUTE register and disabling the I2C module. The device that held the bus low should release it sometime within those 9 clocks. If not, use the same approach as for when SCL is stuck, resetting and possibly cycling power to the slaves.

Lockup of SDA can be detected by keeping count of the number of continuous arbitration losses during address transmission. If arbitration is also lost during the transmission of a general call address, i.e., during the transmission of the STOP condition, which should never happen during normal operation, this is a good indication of SDA lockup.

Detection of SCL lockups can be done using the timeout functionality defined in [18.3.12.6 Clock Low Timeout](#)

### 18.3.12.5 Bus Idle Timeout

When SCL has been high for a significant amount of time, this is a good indication of that the bus is idle. On an SMBus system, the bus is only allowed to be in this state for a maximum of 50  $\mu$ s before the bus is considered idle.

The bus idle timeout BITO in I2Cn\_CTRL can be used to detect situations where the bus goes idle in the middle of a transmission. The timeout can be configured in BITO, and when the bus has been idle for the given amount of time, the BITO interrupt flag in I2Cn\_IF is set. The bus can also be set idle automatically on a bus idle timeout. This is enabled by setting GIBITO in I2Cn\_CTRL.

When the bus idle timer times out, it wraps around and continues counting as long as its condition is true. If the bus is not set idle using GIBITO or the ABORT command in I2Cn\_CMD, this will result in periodic timeouts.

**Note:** This timeout will be generated even if SDA is held low.

The bus idle timeout is active as long as the bus is busy, i.e., BUSY in I2Cn\_STATUS is set. The timeout can be used to get the I<sup>2</sup>C module out of the busy-state it enters when reset, see [18.3.7.4 Reset State](#).

### 18.3.12.6 Clock Low Timeout

The clock timeout, which can be configured in CLTO in I2Cn\_CTRL, starts counting whenever SCL goes low, and times out if SCL does not go high within the configured timeout. A clock low timeout results in CLTOIF in I2Cn\_IF being set, allowing software to take action.

When the timer times out, it wraps around and continues counting as long as SCL is low. An SCL lockup will thus result in periodic clock low timeouts as long as SCL is low.

### 18.3.12.7 Clock Low Error

The I<sup>2</sup>C module can continue transmission in parallel with another device for the entire transaction, as long as the two communications are identical. A case may arise when (before an arbitration has been decided upon) the I<sup>2</sup>C module decides to send out a repeated START or a STOP condition while the other device is still sending data. In the I<sup>2</sup>C protocol specifications, such a combination results in an undefined condition. The I<sup>2</sup>C deals with this by generating a clock low error. This means that if the I<sup>2</sup>C is transmitting a repeated START or a STOP condition and another device (another master or a misbehaving slave) pulls SCL low before the I<sup>2</sup>C sends out the START/STOP condition on SDA, a clock low error is generated. The CLERR interrupt flag is then set in the I2Cn\_IF register, any held lines are released and the I<sup>2</sup>C device goes to idle.

### 18.3.13 DMA Support

The I<sup>2</sup>C module has full DMA support. A request for the DMA controller to write to the I<sup>2</sup>C transmit buffer can come from TXBL (transmit buffer has room for more data). The DMA controller can write to the transmit buffer using the I2Cn\_TXDATA or the I2Cn\_TXDOUBLE register. In order to write to the I2Cn\_TXDOUBLE register (i.e., transferring 2 bytes simultaneously to the transmit buffer using the DMA), DMA\_USEBURSTS needs to be set to 1 for the selected DMA channel. This ensures that the transfer is made to the transmit buffer only when both buffer elements are empty. For performing a DMA write to the I2Cn\_TXDATA register, DMA\_USEBURSTC needs to be set to 1 for the selected DMA channel. This ensures that a DMA transfer is made even when the transmit buffer is half-empty.

A request for the DMA controller to read from the I<sup>2</sup>C receive buffer can come from RXDATAV (data available in the receive buffer). To receive from I2Cn\_RXDOUBLE (i.e., receive only when both buffer elements are full), DMA\_USEBURSTS needs to be set to 1 for the selected DMA channel. In order to receive from I2Cn\_RXDATA through the DMA, DMA\_USEBURSTC needs to be set to 1. This ensures that the data gets picked up even when the receive buffer is half-full.

### 18.3.14 Interrupts

The interrupts generated by the I<sup>2</sup>C module are combined into one interrupt vector, I2C\_INT. If I<sup>2</sup>C interrupts are enabled, an interrupt will be made if one or more of the interrupt flags in I2Cn\_IF and their corresponding bits in I2Cn\_IEN are set.

### 18.3.15 Wake-up

The I<sup>2</sup>C receive section can be active all the way down to energy mode EM3 Stop, and can wake up the CPU on address interrupt. All address match modes are supported.

## 18.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name           | Type  | Description                              |
|--------|----------------|-------|--|
| 0x000  | I2Cn_CTRL      | RW    | Control Register                         |
| 0x004  | I2Cn_CMD       | W1    | Command Register                         |
| 0x008  | I2Cn_STATE     | R     | State Register                           |
| 0x00C  | I2Cn_STATUS    | R     | Status Register                          |
| 0x010  | I2Cn_CLKDIV    | RW    | Clock Division Register                  |
| 0x014  | I2Cn_SADDR     | RW    | Slave Address Register                   |
| 0x018  | I2Cn_SADDRMASK | RW    | Slave Address Mask Register              |
| 0x01C  | I2Cn_RXDATA    | R(a)  | Receive Buffer Data Register             |
| 0x020  | I2Cn_RXDOUBLE  | R(a)  | Receive Buffer Double Data Register      |
| 0x024  | I2Cn_RXDATAP   | R     | Receive Buffer Data Peek Register        |
| 0x028  | I2Cn_RXDOUBLEP | R     | Receive Buffer Double Data Peek Register |
| 0x02C  | I2Cn_TXDATA    | W     | Transmit Buffer Data Register            |
| 0x030  | I2Cn_TXDOUBLE  | W     | Transmit Buffer Double Data Register     |
| 0x034  | I2Cn_IF        | R     | Interrupt Flag Register                  |
| 0x038  | I2Cn_IFS       | W1    | Interrupt Flag Set Register              |
| 0x03C  | I2Cn_IFC       | (R)W1 | Interrupt Flag Clear Register            |
| 0x040  | I2Cn_IEN       | RW    | Interrupt Enable Register                |
| 0x044  | I2Cn_ROUTEPEN  | RW    | I/O Routing Pin Enable Register          |
| 0x048  | I2Cn_ROUTELOC0 | RW    | I/O Routing Location Register            |

## 18.5 Register Description

### 18.5.1 I2Cn\_CTRL - Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |      |    |        |     |    |      |    |     |   |      |    |       |        |        |        |        |         |       |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|------|----|--------|-----|----|------|----|-----|---|------|----|-------|--------|--------|--------|--------|---------|-------|----|
| 0x000         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17   | 16 | 15     | 14  | 13 | 12   | 11 | 10  | 9 | 8    | 7  | 6     | 5      | 4      | 3      | 2      | 1       | 0     |    |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0  |    | 0      | 0x0 |    |      |    | 0x0 |   | 0    | 0  | 0     | 0      | 0      | 0      | 0      | 0       | 0     | 0  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    | RW   |    | RW     | RW  |    |      |    | RW  |   | RW   | RW | RW    | RW     | RW     | RW     | RW     | RW      | RW    | RW |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    | CLTO |    | GIBITO |     |    | BITO |    |     |   | CLHR |    | TXBIL | GCAMEN | ARBDIS | AUTOSN | AUTOSE | AUTOACK | SLAVE | EN |

| Bit   | Name     | Reset   | Access | Description |
|-------|----------|---|--------|-------------|
| 31:19 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |             |

|       |      |     |    |                          |
|-------|------|-----|----|--------------------------|
| 18:16 | CLTO | 0x0 | RW | <b>Clock Low Timeout</b> |
|-------|------|-----|----|--------------------------|

Use to generate a timeout when CLK has been low for the given amount of time. Wraps around and continues counting when the timeout is reached. The timeout value can be calculated by

$$\text{timeout} = \text{PCC} / (\text{f}_{\text{SCL}} \times (\text{N}_{\text{low}} + \text{N}_{\text{high}}))$$

| Value | Mode    | Description   |
|-------|---------|---|
| 0     | OFF     | Timeout disabled  |
| 1     | 40PCC   | Timeout after 40 prescaled clock cycles. In standard mode at 100 kHz, this results in a 50us timeout.     |
| 2     | 80PCC   | Timeout after 80 prescaled clock cycles. In standard mode at 100 kHz, this results in a 100us timeout.    |
| 3     | 160PCC  | Timeout after 160 prescaled clock cycles. In standard mode at 100 kHz, this results in a 200us timeout.   |
| 4     | 320PCC  | Timeout after 320 prescaled clock cycles. In standard mode at 100 kHz, this results in a 400us timeout.   |
| 5     | 1024PCC | Timeout after 1024 prescaled clock cycles. In standard mode at 100 kHz, this results in a 1280us timeout. |

|    |        |   |    |                                    |
|----|--------|---|----|------------------------------------|
| 15 | GIBITO | 0 | RW | <b>Go Idle on Bus Idle Timeout</b> |
|----|--------|---|----|------------------------------------|

When set, the bus automatically goes idle on a bus idle timeout, allowing new transfers to be initiated.

| Value | Description  |
|-------|--|
| 0     | A bus idle timeout has no effect on the bus state.   |
| 1     | A bus idle timeout tells the I <sup>2</sup> C module that the bus is idle, allowing new transfers to be initiated. |

|    |          |   |  |  |
|----|----------|---|--|--|
| 14 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |  |
|----|----------|---|--|--|

| Bit   | Name  | Reset  | Access | Description                              |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |
|---|---|--|--------|--|-------|-------------|-------------|---|----------|--|---|------------|--|---|-------|--|---|--------|---|
| 13:12   | BITO  | 0x0  | RW     | <b>Bus Idle Timeout</b>                  |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |
| <p>Use to generate a timeout when SCL has been high for a given amount time between a START and STOP condition. When in a bus transaction, i.e. the BUSY flag is set, a timer is started whenever SCL goes high. When the timer reaches the value defined by BITO, it sets the BITO interrupt flag. The BITO interrupt flag will then be set periodically as long as SCL remains high. The bus idle timeout is active as long as BUSY is set. It is thus stopped automatically on a timeout if GIBITO is set. It is also stopped a STOP condition is detected and when the ABORT command is issued. The timeout is activated whenever the bus goes BUSY, i.e. a START condition is detected. The timeout value can be calculated by</p> $\text{timeout} = \text{PCC} / (\text{f}_{\text{SCL}} \times (\text{N}_{\text{low}} + \text{N}_{\text{high}}))$ |   |  |        |  |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |
| <table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>OFF</td> <td>Timeout disabled</td> </tr> <tr> <td>1</td> <td>40PCC</td> <td>Timeout after 40 prescaled clock cycles. In standard mode at 100 kHz, this results in a 50us timeout.</td> </tr> <tr> <td>2</td> <td>80PCC</td> <td>Timeout after 80 prescaled clock cycles. In standard mode at 100 kHz, this results in a 100us timeout.</td> </tr> <tr> <td>3</td> <td>160PCC</td> <td>Timeout after 160 prescaled clock cycles. In standard mode at 100 kHz, this results in a 200us timeout.</td> </tr> </tbody> </table>   |   |  |        |  | Value | Mode        | Description | 0   | OFF      | Timeout disabled   | 1 | 40PCC      | Timeout after 40 prescaled clock cycles. In standard mode at 100 kHz, this results in a 50us timeout.  | 2 | 80PCC | Timeout after 80 prescaled clock cycles. In standard mode at 100 kHz, this results in a 100us timeout.           | 3 | 160PCC | Timeout after 160 prescaled clock cycles. In standard mode at 100 kHz, this results in a 200us timeout. |
| Value   | Mode  | Description  |        |  |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |
| 0   | OFF   | Timeout disabled   |        |  |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |
| 1   | 40PCC   | Timeout after 40 prescaled clock cycles. In standard mode at 100 kHz, this results in a 50us timeout.  |        |  |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |
| 2   | 80PCC   | Timeout after 80 prescaled clock cycles. In standard mode at 100 kHz, this results in a 100us timeout.   |        |  |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |
| 3   | 160PCC  | Timeout after 160 prescaled clock cycles. In standard mode at 100 kHz, this results in a 200us timeout.  |        |  |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |
| 11:10   | <i>Reserved</i>   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i>                              |        |  |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |
| 9:8   | CLHR  | 0x0  | RW     | <b>Clock Low High Ratio</b>              |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |
| <p>Determines the ratio between the low and high parts of the clock signal generated on SCL as master.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>STANDARD</td> <td>The ratio between low period and high period counters (<math>\text{N}_{\text{low}}:\text{N}_{\text{high}}</math>) is 4:4</td> </tr> <tr> <td>1</td> <td>ASYMMETRIC</td> <td>The ratio between low period and high period counters (<math>\text{N}_{\text{low}}:\text{N}_{\text{high}}</math>) is 6:3</td> </tr> <tr> <td>2</td> <td>FAST</td> <td>The ratio between low period and high period counters (<math>\text{N}_{\text{low}}:\text{N}_{\text{high}}</math>) is 11:6</td> </tr> </tbody> </table>  |   |  |        |  | Value | Mode        | Description | 0   | STANDARD | The ratio between low period and high period counters ( $\text{N}_{\text{low}}:\text{N}_{\text{high}}$ ) is 4:4                            | 1 | ASYMMETRIC | The ratio between low period and high period counters ( $\text{N}_{\text{low}}:\text{N}_{\text{high}}$ ) is 6:3  | 2 | FAST  | The ratio between low period and high period counters ( $\text{N}_{\text{low}}:\text{N}_{\text{high}}$ ) is 11:6 |   |        |   |
| Value   | Mode  | Description  |        |  |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |
| 0   | STANDARD  | The ratio between low period and high period counters ( $\text{N}_{\text{low}}:\text{N}_{\text{high}}$ ) is 4:4  |        |  |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |
| 1   | ASYMMETRIC  | The ratio between low period and high period counters ( $\text{N}_{\text{low}}:\text{N}_{\text{high}}$ ) is 6:3  |        |  |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |
| 2   | FAST  | The ratio between low period and high period counters ( $\text{N}_{\text{low}}:\text{N}_{\text{high}}$ ) is 11:6   |        |  |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |
| 7   | TXBIL   | 0  | RW     | <b>TX Buffer Interrupt Level</b>         |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |
| <p>Determines the interrupt and status level of the transmit buffer.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>EMPTY</td> <td>TXBL status and the TXBL interrupt flag are set when the transmit buffer becomes empty. TXBL is cleared when the buffer becomes non-empty.</td> </tr> <tr> <td>1</td> <td>HALFFULL</td> <td>TXBL status and the TXBL interrupt flag are set when the transmit buffer goes from full to half-full or empty. TXBL is cleared when the buffer becomes full.</td> </tr> </tbody> </table>  |   |  |        |  | Value | Mode        | Description | 0   | EMPTY    | TXBL status and the TXBL interrupt flag are set when the transmit buffer becomes empty. TXBL is cleared when the buffer becomes non-empty. | 1 | HALFFULL   | TXBL status and the TXBL interrupt flag are set when the transmit buffer goes from full to half-full or empty. TXBL is cleared when the buffer becomes full. |   |       |  |   |        |   |
| Value   | Mode  | Description  |        |  |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |
| 0   | EMPTY   | TXBL status and the TXBL interrupt flag are set when the transmit buffer becomes empty. TXBL is cleared when the buffer becomes non-empty.                   |        |  |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |
| 1   | HALFFULL  | TXBL status and the TXBL interrupt flag are set when the transmit buffer goes from full to half-full or empty. TXBL is cleared when the buffer becomes full. |        |  |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |
| 6   | GCAMEN  | 0  | RW     | <b>General Call Address Match Enable</b> |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |
| <p>Set to enable address match on general call in addition to the programmed slave address.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>General call address will be NACK'ed if it is not included by the slave address and address mask.</td> </tr> </tbody> </table>   |   |  |        |  | Value | Description | 0           | General call address will be NACK'ed if it is not included by the slave address and address mask. |          |  |   |            |  |   |       |  |   |        |   |
| Value   | Description   |  |        |  |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |
| 0   | General call address will be NACK'ed if it is not included by the slave address and address mask. |  |        |  |       |             |             |   |          |  |   |            |  |   |       |  |   |        |   |

| Bit | Name    | Reset | Access | Description  |
|-----|---------|-------|--------|--|
|     |         |       |        | 1<br>When a general call address is received, a software response is required.   |
| 5   | ARBDIS  | 0     | RW     | <b>Arbitration Disable</b><br>A master or slave will not release the bus upon losing arbitration.  |
|     | Value   |       |        | Description  |
|     | 0       |       |        | When a device loses arbitration, the ARB interrupt flag is set and the bus is released.  |
|     | 1       |       |        | When a device loses arbitration, the ARB interrupt flag is set, but communication proceeds.  |
| 4   | AUTOSN  | 0     | RW     | <b>Automatic STOP on NACK</b><br>Write to 1 to make a master transmitter send a STOP when a NACK is received from a slave.   |
|     | Value   |       |        | Description  |
|     | 0       |       |        | Stop is not automatically sent if a NACK is received from a slave.   |
|     | 1       |       |        | The master automatically sends a STOP if a NACK is received from a slave.  |
| 3   | AUTOSE  | 0     | RW     | <b>Automatic STOP When Empty</b><br>Write to 1 to make a master transmitter send a STOP when no more data is available for transmission.   |
|     | Value   |       |        | Description  |
|     | 0       |       |        | A stop must be sent manually when no more data is to be transmitted.   |
|     | 1       |       |        | The master automatically sends a STOP when no more data is available for transmission.   |
| 2   | AUTOACK | 0     | RW     | <b>Automatic Acknowledge</b><br>Set to enable automatic acknowledges.  |
|     | Value   |       |        | Description  |
|     | 0       |       |        | Software must give one ACK command for each ACK transmitted on the I <sup>2</sup> C bus.   |
|     | 1       |       |        | Addresses that are not automatically NACK'ed, and all data is automatically acknowledged.  |
| 1   | SLAVE   | 0     | RW     | <b>Addressable as Slave</b><br>Set this bit to allow the device to be selected as an I <sup>2</sup> C slave.   |
|     | Value   |       |        | Description  |
|     | 0       |       |        | All addresses will be responded to with a NACK   |
|     | 1       |       |        | Addresses matching the programmed slave address or the general call address (if enabled) require a response from software. Other addresses are automatically responded to with a NACK. |
| 0   | EN      | 0     | RW     | <b>I<sup>2</sup>C Enable</b><br>Use this bit to enable or disable the I <sup>2</sup> C module.   |

| Bit | Name  | Reset | Access | Description  |
|-----|-------|-------|--------|--|
|     | Value |       |        | Description  |
|     | 0     |       |        | The I <sup>2</sup> C module is disabled. And its internal state is cleared |
|     | 1     |       |        | The I <sup>2</sup> C module is enabled.                                    |

### 18.5.2 I2Cn\_CMD - Command Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |         |         |       |      |      |     |      |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---------|---------|-------|------|------|-----|------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0x004         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7       | 6       | 5     | 4    | 3    | 2   | 1    | 0     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0       | 0       | 0     | 0    | 0    | 0   | 0    | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | W1      | W1      | W1    | W1   | W1   | W1  | W1   | W1    | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | CLEARPC | CLEARTX | ABORT | CONT | NACK | ACK | STOP | START |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

| Bit  | Name     | Reset   | Access | Description   |
|------|----------|---|--------|---|
| 31:8 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 7    | CLEARPC  | 0   | W1     | <b>Clear Pending Commands</b><br>Set to clear pending commands.   |
| 6    | CLEARTX  | 0   | W1     | <b>Clear TX</b><br>Set to clear transmit buffer and shift register. Will not abort ongoing transfer.  |
| 5    | ABORT    | 0   | W1     | <b>Abort Transmission</b><br>Abort the current transmission making the bus go idle. When used in combination with STOP, a STOP condition is sent as soon as possible before aborting the transmission. The stop condition is subject to clock synchronization.  |
| 4    | CONT     | 0   | W1     | <b>Continue Transmission</b><br>Set to continue transmission after a NACK has been received.  |
| 3    | NACK     | 0   | W1     | <b>Send NACK</b><br>Set to transmit a NACK the next time an acknowledge is required.  |
| 2    | ACK      | 0   | W1     | <b>Send ACK</b><br>Set to transmit an ACK the next time an acknowledge is required.   |
| 1    | STOP     | 0   | W1     | <b>Send Stop Condition</b><br>Set to send stop condition as soon as possible.   |
| 0    | START    | 0   | W1     | <b>Send Start Condition</b><br>Set to send start condition as soon as possible. If a transmission is ongoing and not owned, the start condition will be sent as soon as the bus is idle. If the current transmission is owned by this module, a repeated start condition will be sent. Use in combination with a STOP command to automatically send a STOP, then a START when the bus becomes idle. |

### 18.5.3 I2Cn\_STATE - State Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |       |         |        |             |        |      |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|-------|---------|--------|-------------|--------|------|---|---|---|
| 0x008         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8     | 7       | 6      | 5           | 4      | 3    | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | 0x0   | 0       | 0      | 0           | 0      | 1    |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | R     | R       | R      | R           | R      | R    | R |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | STATE | BUSHOLD | NACKED | TRANSMITTER | MASTER | BUSY |   |   |   |

| Bit   | Name        | Reset   | Access | Description   |       |      |             |   |      |                                     |   |      |   |   |       |                               |   |      |                                 |   |         |  |   |      |                              |   |         |                                       |
|-------|-------------|---|--------|---|-------|------|-------------|---|------|-------------------------------------|---|------|---|---|-------|-------------------------------|---|------|---------------------------------|---|---------|--|---|------|------------------------------|---|---------|---------------------------------------|
| 31:8  | Reserved    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |      |             |   |      |                                     |   |      |   |   |       |                               |   |      |                                 |   |         |  |   |      |                              |   |         |                                       |
| 7:5   | STATE       | 0x0   | R      | <b>Transmission State</b><br><br>The state of any current transmission. Cleared if the I <sup>2</sup> C module is idle.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>IDLE</td> <td>No transmission is being performed.</td> </tr> <tr> <td>1</td> <td>WAIT</td> <td>Waiting for idle. Will send a start condition as soon as the bus is idle.</td> </tr> <tr> <td>2</td> <td>START</td> <td>Start transmitted or received</td> </tr> <tr> <td>3</td> <td>ADDR</td> <td>Address transmitted or received</td> </tr> <tr> <td>4</td> <td>ADDRACK</td> <td>Address ack/nack transmitted or received</td> </tr> <tr> <td>5</td> <td>DATA</td> <td>Data transmitted or received</td> </tr> <tr> <td>6</td> <td>DATAACK</td> <td>Data ack/nack transmitted or received</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | IDLE | No transmission is being performed. | 1 | WAIT | Waiting for idle. Will send a start condition as soon as the bus is idle. | 2 | START | Start transmitted or received | 3 | ADDR | Address transmitted or received | 4 | ADDRACK | Address ack/nack transmitted or received | 5 | DATA | Data transmitted or received | 6 | DATAACK | Data ack/nack transmitted or received |
| Value | Mode        | Description   |        |   |       |      |             |   |      |                                     |   |      |   |   |       |                               |   |      |                                 |   |         |  |   |      |                              |   |         |                                       |
| 0     | IDLE        | No transmission is being performed.   |        |   |       |      |             |   |      |                                     |   |      |   |   |       |                               |   |      |                                 |   |         |  |   |      |                              |   |         |                                       |
| 1     | WAIT        | Waiting for idle. Will send a start condition as soon as the bus is idle.   |        |   |       |      |             |   |      |                                     |   |      |   |   |       |                               |   |      |                                 |   |         |  |   |      |                              |   |         |                                       |
| 2     | START       | Start transmitted or received   |        |   |       |      |             |   |      |                                     |   |      |   |   |       |                               |   |      |                                 |   |         |  |   |      |                              |   |         |                                       |
| 3     | ADDR        | Address transmitted or received   |        |   |       |      |             |   |      |                                     |   |      |   |   |       |                               |   |      |                                 |   |         |  |   |      |                              |   |         |                                       |
| 4     | ADDRACK     | Address ack/nack transmitted or received  |        |   |       |      |             |   |      |                                     |   |      |   |   |       |                               |   |      |                                 |   |         |  |   |      |                              |   |         |                                       |
| 5     | DATA        | Data transmitted or received  |        |   |       |      |             |   |      |                                     |   |      |   |   |       |                               |   |      |                                 |   |         |  |   |      |                              |   |         |                                       |
| 6     | DATAACK     | Data ack/nack transmitted or received   |        |   |       |      |             |   |      |                                     |   |      |   |   |       |                               |   |      |                                 |   |         |  |   |      |                              |   |         |                                       |
| 4     | BUSHOLD     | 0   | R      | <b>Bus Held</b><br><br>Set if the bus is currently being held by this I <sup>2</sup> C module.  |       |      |             |   |      |                                     |   |      |   |   |       |                               |   |      |                                 |   |         |  |   |      |                              |   |         |                                       |
| 3     | NACKED      | 0   | R      | <b>Nack Received</b><br><br>Set if a NACK was received and STATE is ADDRACK or DATAACK.   |       |      |             |   |      |                                     |   |      |   |   |       |                               |   |      |                                 |   |         |  |   |      |                              |   |         |                                       |
| 2     | TRANSMITTER | 0   | R      | <b>Transmitter</b><br><br>Set when operating as a master transmitter or a slave transmitter. When cleared, the system may be operating as a master receiver, a slave receiver or the current mode is not known.   |       |      |             |   |      |                                     |   |      |   |   |       |                               |   |      |                                 |   |         |  |   |      |                              |   |         |                                       |
| 1     | MASTER      | 0   | R      | <b>Master</b><br><br>Set when operating as an I <sup>2</sup> C master. When cleared, the system may be operating as an I <sup>2</sup> C slave.  |       |      |             |   |      |                                     |   |      |   |   |       |                               |   |      |                                 |   |         |  |   |      |                              |   |         |                                       |
| 0     | BUSY        | 1   | R      | <b>Bus Busy</b><br><br>Set when the bus is busy. Whether the I <sup>2</sup> C module is in control of the bus or not has no effect on the value of this bit. When the MCU comes out of reset, the state of the bus is not known, and thus BUSY is set. Use the ABORT command or a bus idle timeout to force the I <sup>2</sup> C module out of the BUSY state.  |       |      |             |   |      |                                     |   |      |   |   |       |                               |   |      |                                 |   |         |  |   |      |                              |   |         |                                       |

## 18.5.4 I2Cn\_STATUS - Status Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |         |      |     |        |       |       |      |       |        |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|---------|------|-----|--------|-------|-------|------|-------|--------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9      | 8       | 7    | 6   | 5      | 4     | 3     | 2    | 1     | 0      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0      | 0       | 1    | 0   | 0      | 0     | 0     | 0    | 0     | 0      | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R      | R       | R    | R   | R      | R     | R     | R    | R     | R      | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RXFULL | RXDATAV | TXBL | TXC | PABORT | PCONT | PNACK | PACK | PSTOP | PSTART |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset   | Access | Description  |
|-------|----------|---|--------|--|
| 31:10 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 9     | RXFULL   | 0   | R      | <b>RX FIFO Full</b><br>Set when the receive buffer is full. Cleared when the receive buffer is no longer full. When this bit is set, there is still room for one more frame in the receive shift register. |
| 8     | RXDATAV  | 0   | R      | <b>RX Data Valid</b><br>Set when data is available in the receive buffer. Cleared when the receive buffer is empty.  |
| 7     | TXBL     | 1   | R      | <b>TX Buffer Level</b><br>Indicates the level of the transmit buffer. Set when the transmit buffer is empty, and cleared when it is full.  |
| 6     | TXC      | 0   | R      | <b>TX Complete</b><br>Set when a transmission has completed and no more data is available in the transmit buffer. Cleared when a new transmission starts.  |
| 5     | PABORT   | 0   | R      | <b>Pending Abort</b><br>An abort is pending and will be transmitted as soon as possible.   |
| 4     | PCONT    | 0   | R      | <b>Pending Continue</b><br>A continue is pending and will be transmitted as soon as possible.  |
| 3     | PNACK    | 0   | R      | <b>Pending NACK</b><br>A not-acknowledge is pending and will be transmitted as soon as possible.   |
| 2     | PACK     | 0   | R      | <b>Pending ACK</b><br>An acknowledge is pending and will be transmitted as soon as possible.   |
| 1     | PSTOP    | 0   | R      | <b>Pending STOP</b><br>A stop condition is pending and will be transmitted as soon as possible.  |
| 0     | PSTART   | 0   | R      | <b>Pending START</b><br>A start condition is pending and will be transmitted as soon as possible.  |

## 18.5.5 I2Cn\_CLKDIV - Clock Division Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |       |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|-------|---|---|---|
| 0x010         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3     | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0x000 |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | RW    |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | DIV   |   |   |   |

| Bit  | Name     | Reset  | Access | Description  |
|------|----------|--|--------|--|
| 31:9 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 8:0  | DIV      | 0x000  | RW     | <b>Clock Divider</b><br>Specifies the clock divider for the I <sup>2</sup> C. Note that DIV must be 1 or higher when slave is enabled. |

## 18.5.6 I2Cn\_SADDR - Slave Address Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |      |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|------|---|---|---|
| 0x014         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3    | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0x00 |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | RW   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | ADDR |   |   |   |

| Bit  | Name     | Reset  | Access | Description  |
|------|----------|--|--------|--|
| 31:8 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 7:1  | ADDR     | 0x00   | RW     | <b>Slave Address</b><br>Specifies the slave address of the device. |
| 0    | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |

## 18.5.7 I2Cn\_SADDRMASK - Slave Address Mask Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |      |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|------|---|---|---|---|---|---|---|
| 0x018         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x00 |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RW   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | MASK |   |   |   |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description  |
|------|----------|--|--------|--|
| 31:8 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 7:1  | MASK     | 0x00   | RW     | <b>Slave Address Mask</b><br><br>Specifies the significant bits of the slave address. Setting the mask to 0x00 will match all addresses, while setting it to 0x7F will only match the exact address specified by ADDR. |
| 0    | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |

## 18.5.8 I2Cn\_RXDATA - Receive Buffer Data Register (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |        |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|--------|---|---|---|---|---|---|---|
| 0x01C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x00   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | R      |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RXDATA |   |   |   |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description  |
|------|----------|--|--------|--|
| 31:8 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 7:0  | RXDATA   | 0x00   | R      | <b>RX Data</b><br><br>Use this register to read from the receive buffer. Buffer is emptied on read access. |

## 18.5.9 I2Cn\_RXDOUBLE - Receive Buffer Double Data Register (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |   |   |         |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---------|---|---|---|---|---|---|---|
| 0x020         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00    |    |    |    |    |    |   |   | 0x00    |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R       |    |    |    |    |    |   |   | R       |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RXDATA1 |    |    |    |    |    |   |   | RXDATA0 |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description   |
|-------|----------|--|--------|---|
| 31:16 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 15:8  | RXDATA1  | 0x00   | R      | <b>RX Data 1</b><br>Second byte read from buffer. Buffer is emptied on read access. |
| 7:0   | RXDATA0  | 0x00   | R      | <b>RX Data 0</b><br>First byte read from buffer. Buffer is emptied on read access.  |

## 18.5.10 I2Cn\_RXDATAP - Receive Buffer Data Peek Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |         |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---------|---|---|---|---|---|---|---|
| 0x024         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x00    |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | R       |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RXDATAP |   |   |   |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description   |
|------|----------|--|--------|---|
| 31:8 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 7:0  | RXDATAP  | 0x00   | R      | <b>RX Data Peek</b><br>Use this register to read from the receive buffer. Buffer is not emptied on read access. |

### 18.5.11 I2Cn\_RXDOUBLEP - Receive Buffer Double Data Peek Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |    |    |    |    |    |   |   |          |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|----|----|---|---|----------|---|---|---|---|---|---|---|
| 0x028         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00     |    |    |    |    |    |   |   | 0x00     |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R        |    |    |    |    |    |   |   | R        |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RXDATAP1 |    |    |    |    |    |   |   | RXDATAPO |   |   |   |   |   |   |   |

| Bit   | Name     | Reset   | Access | Description  |
|-------|----------|---|--------|--|
| 31:16 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 15:8  | RXDATAP1 | 0x00  | R      | <b>RX Data 1 Peek</b><br>Second byte read from buffer. Buffer is not emptied on read access. |
| 7:0   | RXDATAPO | 0x00  | R      | <b>RX Data 0 Peek</b><br>First byte read from buffer. Buffer is not emptied on read access.  |

### 18.5.12 I2Cn\_TXDATA - Transmit Buffer Data Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |        |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|--------|---|---|---|---|---|---|---|
| 0x02C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x00   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | W      |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | TXDATA |   |   |   |   |   |   |   |

| Bit  | Name     | Reset   | Access | Description   |
|------|----------|---|--------|---|
| 31:8 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 7:0  | TXDATA   | 0x00  | W      | <b>TX Data</b><br>Use this register to write a byte to the transmit buffer. |

18.5.13 I2Cn\_TXDOUBLE - Transmit Buffer Double Data Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |   |   |         |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---------|---|---|---|---|---|---|---|
| 0x030         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00    |    |    |    |    |    |   |   | 0x00    |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W       |    |    |    |    |    |   |   | W       |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | TXDATA1 |    |    |    |    |    |   |   | TXDATA0 |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description                                       |
|-------|----------|--|--------|---|
| 31:16 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 15:8  | TXDATA1  | 0x00   | W      | <b>TX Data</b><br>Second byte to write to buffer. |
| 7:0   | TXDATA0  | 0x00   | W      | <b>TX Data</b><br>First byte to write to buffer.  |

## 18.5.14 I2Cn\_IF - Interrupt Flag Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |       |        |       |      |      |      |      |         |        |         |       |      |     |         |      |     |      |        |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|-------|--------|-------|------|------|------|------|---------|--------|---------|-------|------|-----|---------|------|-----|------|--------|-------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x034         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18    | 17     | 16    | 15   | 14   | 13   | 12   | 11      | 10     | 9       | 8     | 7    | 6   | 5       | 4    | 3   | 2    | 1      | 0     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    | 0     | 0      | 0     | 0    | 0    | 0    | 0    | 0       | 0      | 0       | 0     | 0    | 0   | 0       | 0    | 0   | 0    | 0      | 0     | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    | R     | R      | R     | R    | R    | R    | R    | R       | R      | R       | R     | R    | R   | R       | R    | R   | R    | R      | R     | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    | CLERR | RXFULL | SSTOP | CLTO | BITO | RXUF | TXOF | BUSHOLD | BUSERR | ARBLOST | MSTOP | NACK | ACK | RXDATAV | TXBL | TXC | ADDR | RSTART | START |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset   | Access | Description  |
|-------|----------|---|--------|--|
| 31:19 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 18    | CLERR    | 0   | R      | <b>Clock Low Error Interrupt Flag</b><br>Set when the clock is pulled low before a START or a STOP condition could be transmitted.   |
| 17    | RXFULL   | 0   | R      | <b>Receive Buffer Full Interrupt Flag</b><br>Set when the receive buffer becomes full.   |
| 16    | SSTOP    | 0   | R      | <b>Slave STOP Condition Interrupt Flag</b><br>Set when a STOP condition has been received. Will be set regardless of the slave being involved in the transaction or not.   |
| 15    | CLTO     | 0   | R      | <b>Clock Low Timeout Interrupt Flag</b><br>Set on each clock low timeout. The timeout value can be set in CLTO bit field in the I2Cn_CTRL register.  |
| 14    | BITO     | 0   | R      | <b>Bus Idle Timeout Interrupt Flag</b><br>Set on each bus idle timeout. The timeout value can be set in the BITO bit field in the I2Cn_CTRL register.  |
| 13    | RXUF     | 0   | R      | <b>Receive Buffer Underflow Interrupt Flag</b><br>Set when data is read from the receive buffer through the I2Cn_RXDATA register while the receive buffer is empty. It is also set when data is read through the I2Cn_RXDOUBLE while the buffer is not full. |
| 12    | TXOF     | 0   | R      | <b>Transmit Buffer Overflow Interrupt Flag</b><br>Set when data is written to the transmit buffer while the transmit buffer is full.   |
| 11    | BUSHOLD  | 0   | R      | <b>Bus Held Interrupt Flag</b><br>Set when the bus becomes held by the I <sup>2</sup> C module.  |
| 10    | BUSERR   | 0   | R      | <b>Bus Error Interrupt Flag</b><br>Set when a bus error is detected. The bus error is resolved automatically, but the current transfer is aborted.   |
| 9     | ARBLOST  | 0   | R      | <b>Arbitration Lost Interrupt Flag</b><br>Set when arbitration is lost.  |
| 8     | MSTOP    | 0   | R      | <b>Master STOP Condition Interrupt Flag</b><br>Set when a STOP condition has been successfully transmitted. If arbitration is lost during the transmission of the STOP condition, then the MSTOP interrupt flag is not set.                                  |
| 7     | NACK     | 0   | R      | <b>Not Acknowledge Received Interrupt Flag</b><br>Set when a NACK has been received.   |
| 6     | ACK      | 0   | R      | <b>Acknowledge Received Interrupt Flag</b><br>Set when an ACK has been received.   |

| Bit | Name    | Reset | Access | Description   |
|-----|---------|-------|--------|---|
| 5   | RXDATAV | 0     | R      | <b>Receive Data Valid Interrupt Flag</b><br>Set when data is available in the receive buffer. Cleared automatically when the receive buffer is read.              |
| 4   | TXBL    | 1     | R      | <b>Transmit Buffer Level Interrupt Flag</b><br>Set when the transmit buffer becomes empty. Cleared automatically when new data is written to the transmit buffer. |
| 3   | TXC     | 0     | R      | <b>Transfer Completed Interrupt Flag</b><br>Set when the transmit shift register becomes empty and there is no more data in the transmit buffer.                  |
| 2   | ADDR    | 0     | R      | <b>Address Interrupt Flag</b><br>Set when incoming address is accepted, i.e. own address or general call address is received.                                     |
| 1   | RSTART  | 0     | R      | <b>Repeated START Condition Interrupt Flag</b><br>Set when a repeated start condition is detected.  |
| 0   | START   | 0     | R      | <b>START Condition Interrupt Flag</b><br>Set when a start condition is successfully transmitted.  |

## 18.5.15 I2Cn\_IFS - Interrupt Flag Set Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |       |        |       |      |      |      |      |         |        |         |       |      |     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|-------|--------|-------|------|------|------|------|---------|--------|---------|-------|------|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--|
| 0x038         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18    | 17     | 16    | 15   | 14   | 13   | 12   | 11      | 10     | 9       | 8     | 7    | 6   | 5  | 4  | 3  | 2  | 1  | 0  |    |    |    |    |    |    |    |    |    |    |    |    |    |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    | 0     | 0      | 0     | 0    | 0    | 0    | 0    | 0       | 0      | 0       | 0     | 0    | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |    |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    | W1    | W1     | W1    | W1   | W1   | W1   | W1   | W1      | W1     | W1      | W1    | W1   | W1  | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    | CLERR | RXFULL | SSTOP | CLTO | BITO | RXUF | TXOF | BUSHOLD | BUSERR | ARBLOST | MSTOP | NACK | ACK |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |  |

| Bit   | Name     | Reset  | Access | Description  |
|-------|----------|--|--------|--|
| 31:19 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 18    | CLERR    | 0  | W1     | <b>Set CLERR Interrupt Flag</b><br>Write 1 to set the CLERR interrupt flag     |
| 17    | RXFULL   | 0  | W1     | <b>Set RXFULL Interrupt Flag</b><br>Write 1 to set the RXFULL interrupt flag   |
| 16    | SSTOP    | 0  | W1     | <b>Set SSTOP Interrupt Flag</b><br>Write 1 to set the SSTOP interrupt flag     |
| 15    | CLTO     | 0  | W1     | <b>Set CLTO Interrupt Flag</b><br>Write 1 to set the CLTO interrupt flag       |
| 14    | BITO     | 0  | W1     | <b>Set BITO Interrupt Flag</b><br>Write 1 to set the BITO interrupt flag       |
| 13    | RXUF     | 0  | W1     | <b>Set RXUF Interrupt Flag</b><br>Write 1 to set the RXUF interrupt flag       |
| 12    | TXOF     | 0  | W1     | <b>Set TXOF Interrupt Flag</b><br>Write 1 to set the TXOF interrupt flag       |
| 11    | BUSHOLD  | 0  | W1     | <b>Set BUSHOLD Interrupt Flag</b><br>Write 1 to set the BUSHOLD interrupt flag |
| 10    | BUSERR   | 0  | W1     | <b>Set BUSERR Interrupt Flag</b><br>Write 1 to set the BUSERR interrupt flag   |
| 9     | ARBLOST  | 0  | W1     | <b>Set ARBLOST Interrupt Flag</b><br>Write 1 to set the ARBLOST interrupt flag |
| 8     | MSTOP    | 0  | W1     | <b>Set MSTOP Interrupt Flag</b><br>Write 1 to set the MSTOP interrupt flag     |
| 7     | NACK     | 0  | W1     | <b>Set NACK Interrupt Flag</b><br>Write 1 to set the NACK interrupt flag       |
| 6     | ACK      | 0  | W1     | <b>Set ACK Interrupt Flag</b><br>Write 1 to set the ACK interrupt flag         |
| 5:4   | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |

| Bit | Name   | Reset | Access | Description  |
|-----|--------|-------|--------|--|
| 3   | TXC    | 0     | W1     | <b>Set TXC Interrupt Flag</b><br>Write 1 to set the TXC interrupt flag       |
| 2   | ADDR   | 0     | W1     | <b>Set ADDR Interrupt Flag</b><br>Write 1 to set the ADDR interrupt flag     |
| 1   | RSTART | 0     | W1     | <b>Set RSTART Interrupt Flag</b><br>Write 1 to set the RSTART interrupt flag |
| 0   | START  | 0     | W1     | <b>Set START Interrupt Flag</b><br>Write 1 to set the START interrupt flag   |



| Bit | Name            | Reset   | Access | Description   |
|-----|-----------------|---|--------|---|
| 8   | MSTOP           | 0   | (R)W1  | <b>Clear MSTOP Interrupt Flag</b><br><br>Write 1 to clear the MSTOP interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |
| 7   | NACK            | 0   | (R)W1  | <b>Clear NACK Interrupt Flag</b><br><br>Write 1 to clear the NACK interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 6   | ACK             | 0   | (R)W1  | <b>Clear ACK Interrupt Flag</b><br><br>Write 1 to clear the ACK interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).       |
| 5:4 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 3   | TXC             | 0   | (R)W1  | <b>Clear TXC Interrupt Flag</b><br><br>Write 1 to clear the TXC interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).       |
| 2   | ADDR            | 0   | (R)W1  | <b>Clear ADDR Interrupt Flag</b><br><br>Write 1 to clear the ADDR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 1   | RSTART          | 0   | (R)W1  | <b>Clear RSTART Interrupt Flag</b><br><br>Write 1 to clear the RSTART interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 0   | START           | 0   | (R)W1  | <b>Clear START Interrupt Flag</b><br><br>Write 1 to clear the START interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |

## 18.5.17 I2Cn\_IEN - Interrupt Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |       |        |       |      |      |      |      |         |        |         |       |      |     |         |      |     |      |        |       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|-------|--------|-------|------|------|------|------|---------|--------|---------|-------|------|-----|---------|------|-----|------|--------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0x040         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18    | 17     | 16    | 15   | 14   | 13   | 12   | 11      | 10     | 9       | 8     | 7    | 6   | 5       | 4    | 3   | 2    | 1      | 0     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    | 0     | 0      | 0     | 0    | 0    | 0    | 0    | 0       | 0      | 0       | 0     | 0    | 0   | 0       | 0    | 0   | 0    | 0      | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |    |    |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    | RW    | RW     | RW    | RW   | RW   | RW   | RW   | RW      | RW     | RW      | RW    | RW   | RW  | RW      | RW   | RW  | RW   | RW     | RW    | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    | CLERR | RXFULL | SSTOP | CLTO | BITO | RXUF | TXOF | BUSHOLD | BUSERR | ARBLOST | MSTOP | NACK | ACK | RXDATAV | TXBL | TXC | ADDR | RSTART | START |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:19 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 18    | CLERR           | 0   | RW     | <b>CLERR Interrupt Enable</b><br>Enable/disable the CLERR interrupt     |
| 17    | RXFULL          | 0   | RW     | <b>RXFULL Interrupt Enable</b><br>Enable/disable the RXFULL interrupt   |
| 16    | SSTOP           | 0   | RW     | <b>SSTOP Interrupt Enable</b><br>Enable/disable the SSTOP interrupt     |
| 15    | CLTO            | 0   | RW     | <b>CLTO Interrupt Enable</b><br>Enable/disable the CLTO interrupt       |
| 14    | BITO            | 0   | RW     | <b>BITO Interrupt Enable</b><br>Enable/disable the BITO interrupt       |
| 13    | RXUF            | 0   | RW     | <b>RXUF Interrupt Enable</b><br>Enable/disable the RXUF interrupt       |
| 12    | TXOF            | 0   | RW     | <b>TXOF Interrupt Enable</b><br>Enable/disable the TXOF interrupt       |
| 11    | BUSHOLD         | 0   | RW     | <b>BUSHOLD Interrupt Enable</b><br>Enable/disable the BUSHOLD interrupt |
| 10    | BUSERR          | 0   | RW     | <b>BUSERR Interrupt Enable</b><br>Enable/disable the BUSERR interrupt   |
| 9     | ARBLOST         | 0   | RW     | <b>ARBLOST Interrupt Enable</b><br>Enable/disable the ARBLOST interrupt |
| 8     | MSTOP           | 0   | RW     | <b>MSTOP Interrupt Enable</b><br>Enable/disable the MSTOP interrupt     |
| 7     | NACK            | 0   | RW     | <b>NACK Interrupt Enable</b><br>Enable/disable the NACK interrupt       |
| 6     | ACK             | 0   | RW     | <b>ACK Interrupt Enable</b><br>Enable/disable the ACK interrupt         |

| Bit | Name    | Reset | Access | Description   |
|-----|---------|-------|--------|---|
| 5   | RXDATAV | 0     | RW     | <b>RXDATAV Interrupt Enable</b><br>Enable/disable the RXDATAV interrupt |
| 4   | TXBL    | 0     | RW     | <b>TXBL Interrupt Enable</b><br>Enable/disable the TXBL interrupt       |
| 3   | TXC     | 0     | RW     | <b>TXC Interrupt Enable</b><br>Enable/disable the TXC interrupt         |
| 2   | ADDR    | 0     | RW     | <b>ADDR Interrupt Enable</b><br>Enable/disable the ADDR interrupt       |
| 1   | RSTART  | 0     | RW     | <b>RSTART Interrupt Enable</b><br>Enable/disable the RSTART interrupt   |
| 0   | START   | 0     | RW     | <b>START Interrupt Enable</b><br>Enable/disable the START interrupt     |

#### 18.5.18 I2Cn\_ROUTE PEN - I/O Routing Pin Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |        |        |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|--------|--------|
| 0x044         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1      | 0      |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | 0      | 0      |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | RW     | RW     |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | SCLPEN | SDAPEN |

| Bit  | Name            | Reset   | Access | Description  |
|------|-----------------|---|--------|--|
| 31:2 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 1    | SCLPEN          | 0   | RW     | <b>SCL Pin Enable</b><br>When set, the SCL pin of the I <sup>2</sup> C is enabled. |
| 0    | SDAPEN          | 0   | RW     | <b>SDA Pin Enable</b><br>When set, the SDA pin of the I <sup>2</sup> C is enabled. |

## 18.5.19 I2Cn\_ROUTELOC0 - I/O Routing Location Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |        |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|--------|---|---|---|---|---|---|---|---|---|
| 0x048         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9      | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00   |    |    |    |    |    | 0x00   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW     |    |    |    |    |    | RW     |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | SCLLOC |    |    |    |    |    | SDALOC |   |   |   |   |   |   |   |   |   |

| Bit   | Name            | Reset   | Access | Description |
|-------|-----------------|---|--------|-------------|
| 31:14 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |             |

|      |        |      |    |                     |
|------|--------|------|----|---------------------|
| 13:8 | SCLLOC | 0x00 | RW | <b>I/O Location</b> |
|------|--------|------|----|---------------------|

Decides the location of the I<sup>2</sup>C SCL pin.

| Value | Mode  | Description |
|-------|-------|-------------|
| 0     | LOC0  | Location 0  |
| 1     | LOC1  | Location 1  |
| 2     | LOC2  | Location 2  |
| 3     | LOC3  | Location 3  |
| 4     | LOC4  | Location 4  |
| 5     | LOC5  | Location 5  |
| 6     | LOC6  | Location 6  |
| 7     | LOC7  | Location 7  |
| 8     | LOC8  | Location 8  |
| 9     | LOC9  | Location 9  |
| 10    | LOC10 | Location 10 |
| 11    | LOC11 | Location 11 |
| 12    | LOC12 | Location 12 |
| 13    | LOC13 | Location 13 |
| 14    | LOC14 | Location 14 |
| 15    | LOC15 | Location 15 |
| 16    | LOC16 | Location 16 |
| 17    | LOC17 | Location 17 |
| 18    | LOC18 | Location 18 |
| 19    | LOC19 | Location 19 |
| 20    | LOC20 | Location 20 |
| 21    | LOC21 | Location 21 |
| 22    | LOC22 | Location 22 |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
|     | 23   | LOC23 |        | Location 23 |
|     | 24   | LOC24 |        | Location 24 |
|     | 25   | LOC25 |        | Location 25 |
|     | 26   | LOC26 |        | Location 26 |
|     | 27   | LOC27 |        | Location 27 |
|     | 28   | LOC28 |        | Location 28 |
|     | 29   | LOC29 |        | Location 29 |
|     | 30   | LOC30 |        | Location 30 |
|     | 31   | LOC31 |        | Location 31 |

7:6 *Reserved* *To ensure compatibility with future devices, always write bits to 0. More information in [1.2 Conventions](#)*

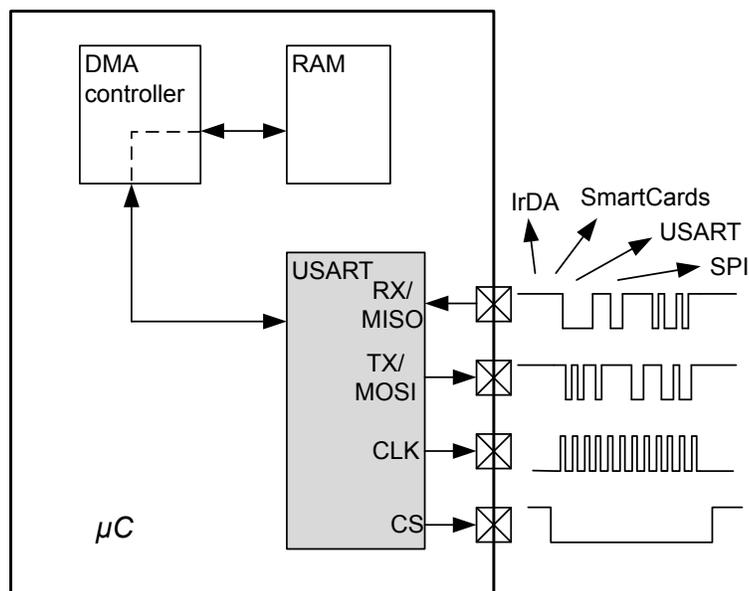
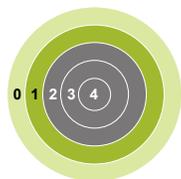
5:0 SDALOC 0x00 RW **I/O Location**

Decides the location of the I<sup>2</sup>C SDA pin.

| Value | Mode  | Description |
|-------|-------|-------------|
| 0     | LOC0  | Location 0  |
| 1     | LOC1  | Location 1  |
| 2     | LOC2  | Location 2  |
| 3     | LOC3  | Location 3  |
| 4     | LOC4  | Location 4  |
| 5     | LOC5  | Location 5  |
| 6     | LOC6  | Location 6  |
| 7     | LOC7  | Location 7  |
| 8     | LOC8  | Location 8  |
| 9     | LOC9  | Location 9  |
| 10    | LOC10 | Location 10 |
| 11    | LOC11 | Location 11 |
| 12    | LOC12 | Location 12 |
| 13    | LOC13 | Location 13 |
| 14    | LOC14 | Location 14 |
| 15    | LOC15 | Location 15 |
| 16    | LOC16 | Location 16 |
| 17    | LOC17 | Location 17 |
| 18    | LOC18 | Location 18 |
| 19    | LOC19 | Location 19 |
| 20    | LOC20 | Location 20 |
| 21    | LOC21 | Location 21 |
| 22    | LOC22 | Location 22 |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
| 23  |      | LOC23 |        | Location 23 |
| 24  |      | LOC24 |        | Location 24 |
| 25  |      | LOC25 |        | Location 25 |
| 26  |      | LOC26 |        | Location 26 |
| 27  |      | LOC27 |        | Location 27 |
| 28  |      | LOC28 |        | Location 28 |
| 29  |      | LOC29 |        | Location 29 |
| 30  |      | LOC30 |        | Location 30 |
| 31  |      | LOC31 |        | Location 31 |

## 19. USART - Universal Synchronous Asynchronous Receiver/Transmitter



### Quick Facts

#### What?

The USART handles high-speed UART, SPI-bus, SmartCards, and IrDA communication.

#### Why?

Serial communication is frequently used in embedded systems and the USART allows efficient communication with a wide range of external devices.

#### How?

The USART has a wide selection of operating modes, frame formats and baud rates. The multi-processor mode allows the USART to remain idle when not addressed. Triple buffering and DMA support makes high data rates possible with minimal CPU intervention and it is possible to transmit and receive large frames while the MCU remains in EM1 Sleep.

### 19.1 Introduction

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, and IrDA devices.

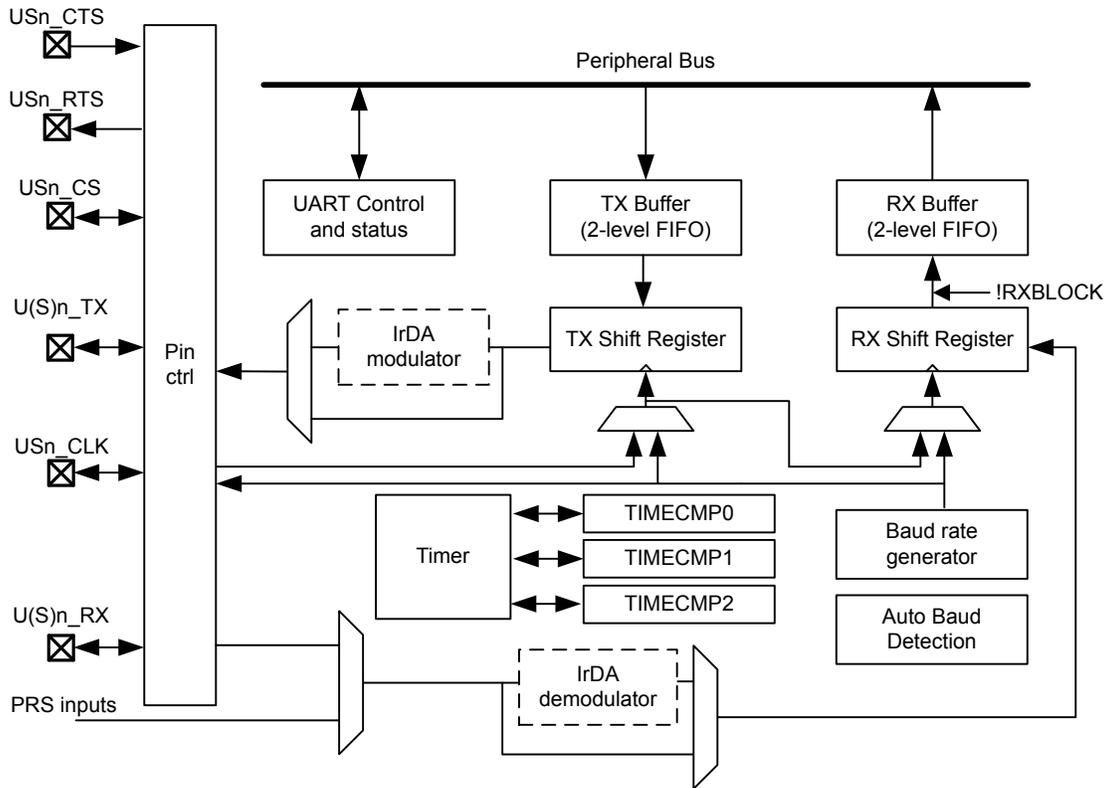
## 19.2 Features

- Asynchronous and synchronous (SPI) communication
- Full duplex and half duplex
- Separate TX/RX enable
- Separate receive / transmit multiple entry buffers, with additional separate shift registers
- Programmable baud rate, generated as a fractional division from the peripheral clock ( $\text{HFPERCLK}_{\text{USARTn}}$ )
- Max bit-rate
  - SPI master mode, peripheral clock rate/2
  - SPI slave mode, peripheral clock rate/8
  - UART mode, peripheral clock rate/16, 8, 6, or 4
- Asynchronous mode supports
  - Majority vote baud-reception
  - False start-bit detection
  - Break generation/detection
  - Multi-processor mode
- Synchronous mode supports
  - All 4 SPI clock polarity/phase configurations
  - Master and slave mode
- Data can be transmitted LSB first or MSB first
- Configurable number of data bits, 4-16 (plus the parity bit, if enabled)
  - HW parity bit generation and check
- Configurable number of stop bits in asynchronous mode: 0.5, 1, 1.5, 2
- HW collision detection
- Multi-processor mode
- IrDA modulator
- SmartCard (ISO7816) mode
- I2S mode
- Separate interrupt vectors for receive and transmit interrupts
- Loopback mode
  - Half duplex communication
  - Communication debugging
- PRS RX input
- 8 bit Timer
- Hardware Flow Control
- Automatic Baud Rate Detection

### 19.3 Functional Description

An overview of the USART module is shown in [Figure 19.1 USART Overview on page 569](#).

This section describes all possible USART features. Refer to the device data sheet to see what features a specific USART instance supports.



**Figure 19.1. USART Overview**

### 19.3.1 Modes of Operation

The USART operates in either asynchronous or synchronous mode.

In synchronous mode, a separate clock signal is transmitted with the data. This clock signal is generated by the bus master, and both the master and slave sample and transmit data according to this clock. Both master and slave modes are supported by the USART. The synchronous communication mode is compatible with the Serial Peripheral Interface Bus (SPI) standard.

In asynchronous mode, no separate clock signal is transmitted with the data on the bus. The USART receiver thus has to determine where to sample the data on the bus from the actual data. To make this possible, additional synchronization bits are added to the data when operating in asynchronous mode, resulting in a slight overhead.

Asynchronous or synchronous mode can be selected by configuring SYNC in USARTn\_CTRL. The options are listed with supported protocols in [Table 19.1 USART Asynchronous Vs. Synchronous Mode on page 570](#). Full duplex and half duplex communication is supported in both asynchronous and synchronous mode.

**Table 19.1. USART Asynchronous Vs. Synchronous Mode**

| SYNC | Communication Mode | Supported Protocols                                |
|------|--------------------|--|
| 0    | Asynchronous       | RS-232, RS-485 (w/external driver), IrDA, ISO 7816 |
| 1    | Synchronous        | SPI, MicroWire, 3-wire                             |

[Table 19.2 USART Pin Usage on page 570](#) explains the functionality of the different USART pins when the USART operates in different modes. Pin functionality enclosed in square brackets is optional, and depends on additional configuration parameters. LOOPBK and MASTER are discussed in [19.3.2.14 Local Loopback](#) and [19.3.3.3 Master Mode](#) respectively.

**Table 19.2. USART Pin Usage**

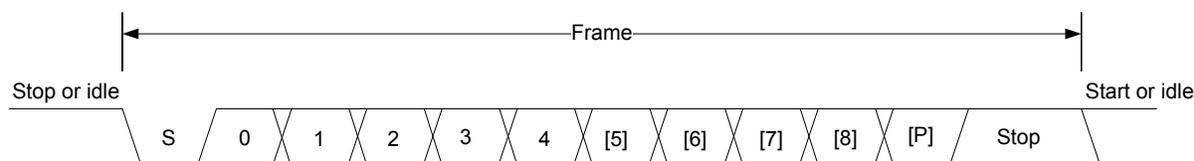
| SYNC | LOOPBK | MASTER | Pin functionality |                 |           |                     |
|------|--------|--------|-------------------|-----------------|-----------|---------------------|
|      |        |        | U(S)n_TX (MOSI)   | U(S)n_RX (MISO) | USn_CLK   | USn_CS              |
| 0    | 0      | x      | Data out          | Data in         | -         | [Driver enable]     |
| 0    | 1      | x      | Data out/in       | -               | -         | [Driver enable]     |
| 1    | 0      | 0      | Data in           | Data out        | Clock in  | Slave select        |
| 1    | 0      | 1      | Data out          | Data in         | Clock out | [Auto slave select] |
| 1    | 1      | 0      | Data out/in       | -               | Clock in  | Slave select        |
| 1    | 1      | 1      | Data out/in       | -               | Clock out | [Auto slave select] |

### 19.3.2 Asynchronous Operation

The USART operates in asynchronous mode when SYNC in USARTn\_CTRL is cleared to 0.

### 19.3.2.1 Frame Format

The frame format used in asynchronous mode consists of a set of data bits in addition to bits for synchronization and optionally a parity bit for error checking. A frame starts with one start-bit (S), where the line is driven low for one bit-period. This signals the start of a frame, and is used for synchronization. Following the start bit are 4 to 16 data bits and an optional parity bit. Finally, a number of stop-bits, where the line is driven high, end the frame. An example frame is shown in [Figure 19.2 USART Asynchronous Frame Format on page 571](#).



**Figure 19.2. USART Asynchronous Frame Format**

The number of data bits in a frame is set by `DATABITS` in `USARTn_FRAME`, see [Table 19.3 USART Data Bits on page 571](#), and the number of stop-bits is set by `STOPBITS` in `USARTn_FRAME`, see [Table 19.4 USART Stop Bits on page 571](#). Whether or not a parity bit should be included, and whether it should be even or odd is defined by `PARITY`, also in `USARTn_FRAME`. For communication to be possible, all parties of an asynchronous transfer must agree on the frame format being used.

**Table 19.3. USART Data Bits**

| DATA BITS [3:0] | Number of Data Bits |
|-----------------|---------------------|
| 0001            | 4                   |
| 0010            | 5                   |
| 0011            | 6                   |
| 0100            | 7                   |
| 0101            | 8 (Default)         |
| 0110            | 9                   |
| 0111            | 10                  |
| 1000            | 11                  |
| 1001            | 12                  |
| 1010            | 13                  |
| 1011            | 14                  |
| 1100            | 15                  |
| 1101            | 16                  |

**Table 19.4. USART Stop Bits**

| STOP BITS [1:0] | Number of Stop Bits |
|-----------------|---------------------|
| 00              | 0.5                 |
| 01              | 1 (Default)         |
| 10              | 1.5                 |
| 11              | 2                   |

The order in which the data bits are transmitted and received is defined by MSBF in USARTn\_CTRL. When MSBF is cleared, data in a frame is sent and received with the least significant bit first. When it is set, the most significant bit comes first.

The frame format used by the transmitter can be inverted by setting TXINV in USARTn\_CTRL, and the format expected by the receiver can be inverted by setting RXINV in USARTn\_CTRL. These bits affect the entire frame, not only the data bits. An inverted frame has a low idle state, a high start-bit, inverted data and parity bits, and low stop-bits.

### 19.3.2.2 Parity Bit Calculation and Handling

When parity bits are enabled, hardware automatically calculates and inserts any parity bits into outgoing frames, and verifies the received parity bits in incoming frames. This is true for both asynchronous and synchronous modes, even though it is mostly used in asynchronous communication. The possible parity modes are defined in [Table 19.5 USART Parity Bits on page 572](#). When even parity is chosen, a parity bit is inserted to make the number of high bits (data + parity) even. If odd parity is chosen, the parity bit makes the total number of high bits odd.

**Table 19.5. USART Parity Bits**

| PARITY BITS [1:0] | Description             |
|-------------------|-------------------------|
| 00                | No parity bit (Default) |
| 01                | Reserved                |
| 10                | Even parity             |
| 11                | Odd parity              |

### 19.3.2.3 Clock Generation

The USART clock defines the transmission and reception data rate. When operating in asynchronous mode, the baud rate (bit-rate) is given by [Figure 19.3 USART Baud Rate on page 573](#).

$$br = f_{HFPERCLK} / (\text{oversample} \times (1 + \text{USARTn\_CLKDIV}/256))$$

**Figure 19.3. USART Baud Rate**

where  $f_{HFPERCLK}$  is the peripheral clock ( $f_{HFPERCLK_{USARTn}}$ ) frequency and oversample is the oversampling rate as defined by OVS in  $\text{USARTn\_CTRL}$ , see [Table 19.6 USART Oversampling on page 573](#).

**Table 19.6. USART Oversampling**

| OVS [1:0] | Oversample |
|-----------|------------|
| 00        | 16         |
| 01        | 8          |
| 10        | 6          |
| 11        | 4          |

The USART has a fractional clock divider to allow the USART clock to be controlled more accurately than what is possible with a standard integral divider.

The clock divider used in the USART is a 20-bit value, with a 15-bit integral part and an 5-bit fractional part. The fractional part is configured in the lower 5 bits of DIV in  $\text{USART\_CLKDIV}$ .

Fractional clock division is implemented by distributing the selected fraction over thirty two baud periods. The fractional part of the divider tells how many of these periods should be extended by one peripheral clock cycle.

Given a desired baud rate  $br_{desired}$ , the clock divider  $\text{USARTn\_CLKDIV}$  can be calculated by using [Figure 19.4 USART Desired Baud Rate on page 573](#):

$$\text{USARTn\_CLKDIV} = 256 \times (f_{HFPERCLK} / (\text{oversample} \times br_{desired}) - 1)$$

**Figure 19.4. USART Desired Baud Rate**

[Table 19.7 USART Baud Rates @ 4MHz Peripheral Clock With 20 Bit CLKDIV on page 573](#) shows a set of desired baud rates and how accurately the USART is able to generate these baud rates when running at a 4 MHz peripheral clock, using 16x or 8x oversampling.

**Table 19.7. USART Baud Rates @ 4MHz Peripheral Clock With 20 Bit CLKDIV**

| Desired baud rate [baud/s] | USARTn_OVS =00                       |                           |         | USARTn_OVS =01                       |                           |         |
|----------------------------|--------------------------------------|---------------------------|---------|--------------------------------------|---------------------------|---------|
|                            | USARTn_CLKDIV/256 (to 32nd position) | Actual baud rate [baud/s] | Error % | USARTn_CLKDIV/256 (to 32nd position) | Actual baud rate [baud/s] | Error % |
| 600                        | 415.6563                             | 600.015                   | 0.003   | 832.3438                             | 599.9925                  | -0.001  |
| 1200                       | 207.3438                             | 1199.94                   | -0.005  | 415.6563                             | 1200.03                   | 0.003   |
| 2400                       | 103.1563                             | 2400.24                   | 0.010   | 207.3438                             | 2399.88                   | -0.005  |
| 4800                       | 51.09375                             | 4799.04                   | -0.020  | 103.1563                             | 4800.48                   | 0.010   |
| 9600                       | 25.03125                             | 9603.842                  | 0.040   | 51.09375                             | 9598.08                   | -0.020  |
| 14400                      | 16.375                               | 14388.49                  | -0.080  | 33.71875                             | 14401.44                  | 0.010   |
| 19200                      | 12.03125                             | 19184.65                  | -0.080  | 25.03125                             | 19207.68                  | 0.040   |
| 28800                      | 7.6875                               | 28776.98                  | -0.080  | 16.375                               | 28776.98                  | -0.080  |

| Desired baud rate [baud/s] | USARTn_OVS =00                       |                           |         | USARTn_OVS =01                       |                           |         |
|----------------------------|--------------------------------------|---------------------------|---------|--------------------------------------|---------------------------|---------|
|                            | USARTn_CLKDIV/256 (to 32nd position) | Actual baud rate [baud/s] | Error % | USARTn_CLKDIV/256 (to 32nd position) | Actual baud rate [baud/s] | Error % |
| 38400                      | 5.5                                  | 38461.54                  | 0.160   | 12.03125                             | 38369.3                   | -0.080  |
| 57600                      | 3.34375                              | 57553.96                  | -0.080  | 7.6875                               | 57553.96                  | -0.080  |
| 76800                      | 2.25                                 | 76923.08                  | 0.160   | 5.5                                  | 76923.08                  | 0.160   |
| 115200                     | 1.15625                              | 115942                    | 0.644   | 3.34375                              | 115107.9                  | -0.080  |
| 230400                     | 0.09375                              | 228571.4                  | -0.794  | 1.15625                              | 231884.1                  | 0.644   |

#### 19.3.2.4 Auto Baud Detection

Setting AUTOBAUDEN in USARTn\_CLKDIV uses the first frame received to automatically set the baud rate provided that it contains 0x55 (IrDA uses 0x00). AUTOBAUDEN can be used in a simple LIN configuration to auto detect the SYNC byte. The receiver will measure the number of local clock cycles between the beginning of the START bit and the beginning of the 8th data bit. The DIV field in USARTn\_CLKDIV will be overwritten with the new value. The OVS in USARTn\_CTRL and the +1 count of the Baud Rate equation are already factored into the result that gets written into the DIV field. To restart autobaud detection, clear AUTOBAUDEN and set it high again. Since the auto baud detection is done over 8 baud times, only the upper 3 bits of the fractional part of the clock divider are populated.

#### 19.3.2.5 Data Transmission

Asynchronous data transmission is initiated by writing data to the transmit buffer using one of the methods described in [19.3.2.6 Transmit Buffer Operation](#). When the transmission shift register is empty and ready for new data, a frame from the transmit buffer is loaded into the shift register, and if the transmitter is enabled, transmission begins. When the frame has been transmitted, a new frame is loaded into the shift register if available, and transmission continues. If the transmit buffer is empty, the transmitter goes to an idle state, waiting for a new frame to become available.

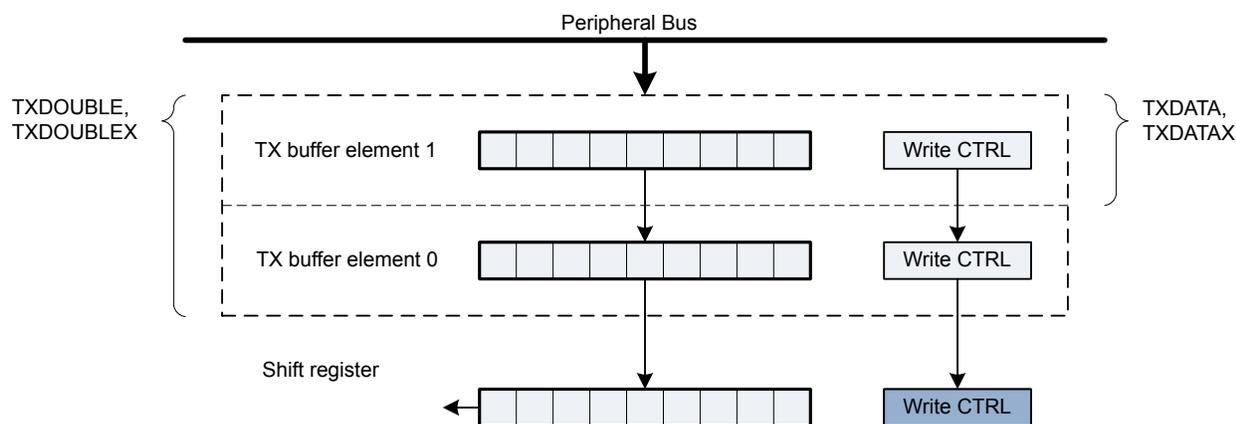
Transmission is enabled through the command register USARTn\_CMD by setting TXEN, and disabled by setting TXDIS in the same command register. When the transmitter is disabled using TXDIS, any ongoing transmission is aborted, and any frame currently being transmitted is discarded. When disabled, the TX output goes to an idle state, which by default is a high value. Whether or not the transmitter is enabled at a given time can be read from TXENS in USARTn\_STATUS.

When the USART transmitter is enabled and there is no data in the transmit shift register or transmit buffer, the TXC flag in USARTn\_STATUS and the TXC interrupt flag in USARTn\_IF are set, signaling that the transmission is complete. The TXC status flag is cleared when a new frame becomes available for transmission, but the TXC interrupt flag must be cleared by software.

### 19.3.2.6 Transmit Buffer Operation

The transmit-buffer is a multiple entry FIFO buffer. A frame can be loaded into the buffer by writing to USARTn\_TXDATA, USARTn\_TXDATAx, USARTn\_TXDOUBLE or USARTn\_TXDOUBLEX. Using USARTn\_TXDATA allows 8 bits to be written to the buffer, while using USARTn\_TXDOUBLE will write 2 frames of 8 bits to the buffer. If 9-bit frames are used, the 9th bit of the frames will in these cases be set to the value of BIT8DV in USARTn\_CTRL.

To set the 9th bit directly and/or use transmission control, USARTn\_TXDATAx and USARTn\_TXDOUBLEX must be used. USARTn\_TXDATAx allows 9 data bits to be written, as well as a set of control bits regarding the transmission of the written frame. Every frame in the buffer is stored with 9 data bits and additional transmission control bits. USARTn\_TXDOUBLEX allows two frames, complete with control bits to be written at once. When data is written to the transmit buffer using USARTn\_TXDATAx and USARTn\_TXDOUBLEX, the 9th bit(s) written to these registers override the value in BIT8DV in USARTn\_CTRL, and alone define the 9th bits that are transmitted if 9-bit frames are used. [Figure 19.5 USART Transmit Buffer Operation](#) on page 575 shows the basics of the transmit buffer when DATABITS in USARTn\_FRAME is configured to less than 10 bits.



**Figure 19.5. USART Transmit Buffer Operation**

When writing more frames to the transmit buffer than there is free space for, the TXOF interrupt flag in USARTn\_IF will be set, indicating the overflow. The data already in the transmit buffer is preserved in this case, and no data is written.

In addition to the interrupt flag TXC in USARTn\_IF and status flag TXC in USARTn\_STATUS which are set when the transmission is complete, TXBL in USARTn\_STATUS and the TXBL interrupt flag in USARTn\_IF are used to indicate the level of the transmit buffer. TXBIL in USARTn\_CTRL controls the level at which these bits are set. If TXBIL is cleared, they are set whenever the transmit buffer becomes empty, and if TXBIL is set, they are set whenever the transmit buffer goes from full to half-full or empty. Both the TXBL status flag and the TXBL interrupt flag are cleared automatically when their condition becomes false.

There is a TXIDLE status bit in USARTn\_STATUS to provide an indication of when the transmitter is idle. The combined count of TX buffer element 0, TX buffer element 1, and TX shift register is called TXBUFCNT in USARTn\_STATUS. For large frames, the count is only of TX buffer entry 0 and the TX shifter register.

The transmit buffer, including the transmit shift register can be cleared by setting CLEARTX in USARTn\_CMD. This will prevent the USART from transmitting the data in the buffer and shift register, and will make them available for new data. Any frame currently being transmitted will not be aborted. Transmission of this frame will be completed.

### 19.3.2.7 Frame Transmission Control

The transmission control bits, which can be written using USARTn\_TXDATAx and USARTn\_TXDOUBLEx, affect the transmission of the written frame. The following options are available:

- **Generate break:** By setting TXBREAK, the output will be held low during the stop-bit period to generate a framing error. A receiver that supports break detection detects this state, allowing it to be used e.g. for framing of larger data packets. The line is driven high before the next frame is transmitted so the next start condition can be identified correctly by the recipient. Continuous breaks lasting longer than a USART frame are thus not supported by the USART. GPIO can be used for this.
- **Disable transmitter after transmission:** If TXDISAT is set, the transmitter is disabled after the frame has been fully transmitted.
- **Enable receiver after transmission:** If RXENAT is set, the receiver is enabled after the frame has been fully transmitted. It is enabled in time to detect a start-bit directly after the last stop-bit has been transmitted.
- **Unblock receiver after transmission:** If UBRXAT is set, the receiver is unblocked and RXBLOCK is cleared after the frame has been fully transmitted.
- **Tristate transmitter after transmission:** If TXTRIAT is set, TXTRI is set after the frame has been fully transmitted, tristating the transmitter output. Tristating of the output can also be performed automatically by setting AUTOTRI. If AUTOTRI is set TXTRI is always read as 0.

**Note:** When in SmartCard mode with repeat enabled, none of the actions, except generate break, will be performed until the frame is transmitted without failure. Generation of a break in SmartCard mode with repeat enabled will cause the USART to detect a NACK on every frame.

### 19.3.2.8 Data Reception

Data reception is enabled by setting RXEN in USARTn\_CMD. When the receiver is enabled, it actively samples the input looking for a transition from high to low indicating the start baud of a new frame. When a start baud is found, reception of the new frame begins if the receive shift register is empty and ready for new data. When the frame has been received, it is pushed into the receive buffer, making the shift register ready for another frame of data, and the receiver starts looking for another start baud. If the receive buffer is full, the received frame remains in the shift register until more space in the receive buffer is available. If an incoming frame is detected while both the receive buffer and the receive shift register are full, the data in the shift register is overwritten, and the RXOF interrupt flag in USARTn\_IF is set to indicate the buffer overflow.

The receiver can be disabled by setting the command bit RXDIS in USARTn\_CMD. Any frame currently being received when the receiver is disabled is discarded. Whether or not the receiver is enabled at a given time can be read out from RXENS in USARTn\_STATUS.

### 19.3.2.9 Receive Buffer Operation

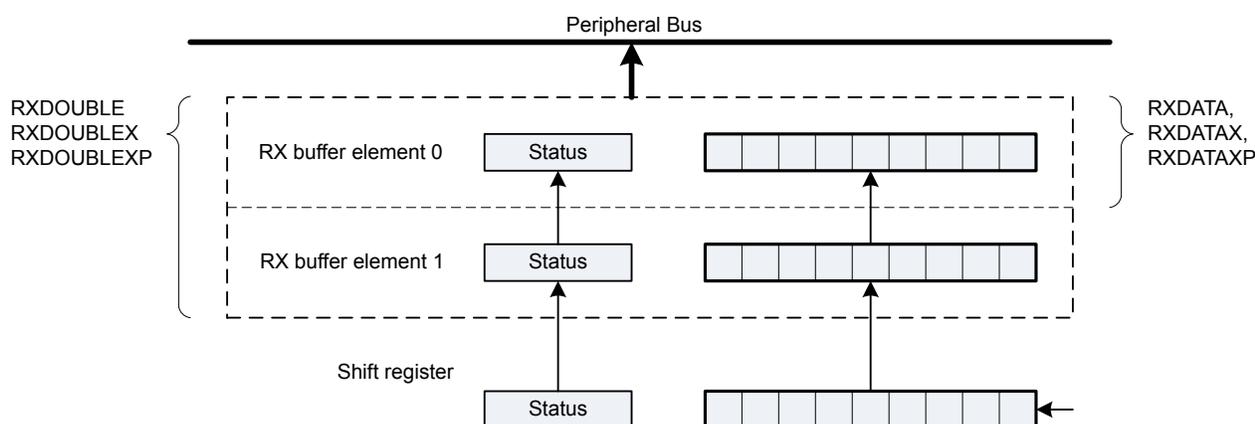
When data becomes available in the receive buffer, the RXDATAV flag in USARTn\_STATUS, and the RXDATAV interrupt flag in USARTn\_IF are set, and when the buffer becomes full, RXFULL in USARTn\_STATUS and the RXFULL interrupt flag in USARTn\_IF are set. The status flags RXDATAV and RXFULL are automatically cleared by hardware when their condition is no longer true. This also goes for the RXDATAV interrupt flag, but the RXFULL interrupt flag must be cleared by software. When the RXFULL flag is set, notifying that the buffer is full, space is still available in the receive shift register for one more frame.

Data can be read from the receive buffer in a number of ways. USARTn\_RXDATA gives access to the 8 least significant bits of the received frame, and USARTn\_RXDOUBLE makes it possible to read the 8 least significant bits of two frames at once, pulling two frames from the buffer. To get access to the 9th, most significant bit, USARTn\_RXDATA\_X must be used. This register also contains status information regarding the frame. USARTn\_RXDOUBLE\_X can be used to get two frames complete with the 9th bits and status bits.

When a frame is read from the receive buffer using USARTn\_RXDATA or USARTn\_RXDATA\_X, the frame is pulled out of the buffer, making room for a new frame. USARTn\_RXDOUBLE and USARTn\_RXDOUBLE\_X pull two frames out of the buffer. If an attempt is done to read more frames from the buffer than what is available, the RXUF interrupt flag in USARTn\_IF is set to signal the underflow, and the data read from the buffer is undefined.

Frames can be read from the receive buffer without removing the data by using USARTn\_RXDATA\_X\_P and USARTn\_RXDOUBLE\_X\_P. USARTn\_RXDATA\_X\_P gives access the first frame in the buffer with status bits, while USARTn\_RXDOUBLE\_X\_P gives access to both frames with status bits. The data read from these registers when the receive buffer is empty is undefined. If the receive buffer contains one valid frame, the first frame in USARTn\_RXDOUBLE\_X\_P will be valid. No underflow interrupt is generated by a read using these registers, i.e. RXUF in USARTn\_IF is never set as a result of reading from USARTn\_RXDATA\_X\_P or USARTn\_RXDOUBLE\_X\_P.

The basic operation of the receive buffer when DATABITS in USARTn\_FRAME is configured to less than 10 bits is shown in [Figure 19.6 USART Receive Buffer Operation on page 577](#).



**Figure 19.6. USART Receive Buffer Operation**

The receive buffer, including the receive shift register can be cleared by setting CLEARRX in USARTn\_CMD. Any frame currently being received will not be discarded.

### 19.3.2.10 Blocking Incoming Data

When using hardware frame recognition, as detailed in [19.3.2.20 Multi-Processor Mode](#) and [19.3.2.21 Collision Detection](#), it is necessary to be able to let the receiver sample incoming frames without passing the frames to software by loading them into the receive buffer. This is accomplished by blocking incoming data.

Incoming data is blocked as long as RXBLOCK in USARTn\_STATUS is set. When blocked, frames received by the receiver will not be loaded into the receive buffer, and software is not notified by the RXDATAV flag in USARTn\_STATUS or the RXDATAV interrupt flag in USARTn\_IF at their arrival. For data to be loaded into the receive buffer, RXBLOCK must be cleared in the instant a frame is fully received by the receiver. RXBLOCK is set by setting RXBLOCKEN in USARTn\_CMD and disabled by setting RXBLOCKDIS also in USARTn\_CMD. There is one exception where data is loaded into the receive buffer even when RXBLOCK is set. This is when an address frame is received when operating in multi-processor mode. See [19.3.2.20 Multi-Processor Mode](#) for more information.

Frames received containing framing or parity errors will not result in the FERR and PERR interrupt flags in USARTn\_IF being set while RXBLOCK in USARTn\_STATUS is set. Hardware recognition is not applied to these erroneous frames, and they are silently discarded.

**Note:**

- If a frame is received while RXBLOCK in USARTn\_STATUS is cleared, but stays in the receive shift register because the receive buffer is full, the received frame will be loaded into the receive buffer when space becomes available even if RXBLOCK is set at that time.
- The overflow interrupt flag RXOF in USARTn\_IF will be set if a frame in the receive shift register, waiting to be loaded into the receive buffer is overwritten by an incoming frame even though RXBLOCK in USARTn\_STATUS is set.

### 19.3.2.11 Clock Recovery and Filtering

The receiver samples the incoming signal at a rate 16, 8, 6 or 4 times higher than the given baud rate, depending on the oversampling mode given by OVS in USARTn\_CTRL. Lower oversampling rates make higher baud rates possible, but give less room for errors.

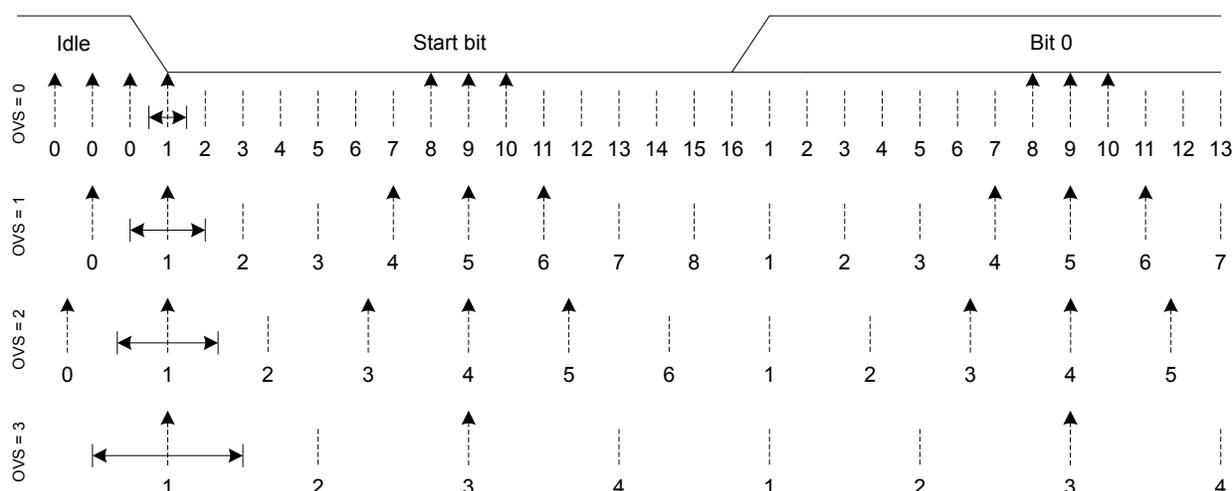
When a high-to-low transition is registered on the input while the receiver is idle, this is recognized as a start-bit, and the baud rate generator is synchronized with the incoming frame.

For oversampling modes 16, 8 and 6, every bit in the incoming frame is sampled three times to gain a level of noise immunity. These samples are aimed at the middle of the bit-periods, as visualized in [Figure 19.7 USART Sampling of Start and Data Bits on page 579](#). With OVS=0 in USARTn\_CTRL, the start and data bits are thus sampled at locations 8, 9 and 10 in the figure, locations 4, 5 and 6 for OVS=1 and locations 3, 4, and 5 for OVS=2. The value of a sampled bit is determined by majority vote. If two or more of the three bit-samples are high, the resulting bit value is high. If the majority is low, the resulting bit value is low.

Majority vote is used for all oversampling modes except 4x oversampling. In this mode, a single sample is taken at position 3 as shown in [Figure 19.7 USART Sampling of Start and Data Bits on page 579](#).

Majority vote can be disabled by setting MVDIS in USARTn\_CTRL.

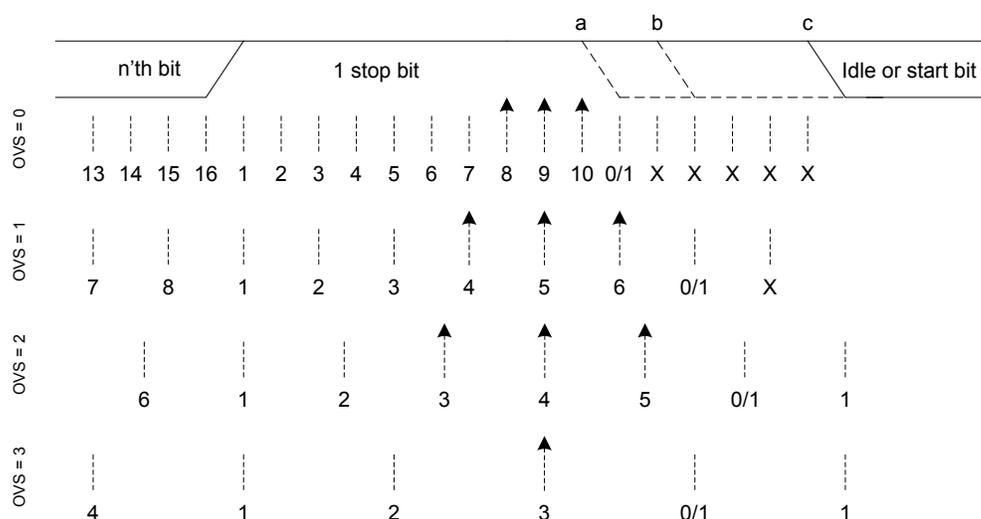
If the value of the start bit is found to be high, the reception of the frame is aborted, filtering out false start bits possibly generated by noise on the input.



**Figure 19.7. USART Sampling of Start and Data Bits**

If the baud rate of the transmitter and receiver differ, the location each bit is sampled will be shifted towards the previous or next bit in the frame. This is acceptable for small errors in the baud rate, but for larger errors, it will result in transmission errors.

When the number of stop bits is 1 or more, stop bits are sampled like the start and data bits as seen in [Figure 19.8 USART Sampling of Stop Bits when Number of Stop Bits are 1 or More on page 580](#). When a stop bit has been detected by sampling at positions 8, 9 and 10 for normal mode, or 4, 5 and 6 for smart mode, the USART is ready for a new start bit. As seen in [Figure 19.8 USART Sampling of Stop Bits when Number of Stop Bits are 1 or More on page 580](#), a stop-bit of length 1 normally ends at c, but the next frame will be received correctly as long as the start-bit comes after position a for OVS=0 and OVS=3, and b for OVS=1 and OVS=2.



**Figure 19.8. USART Sampling of Stop Bits when Number of Stop Bits are 1 or More**

When working with stop bit lengths of half a baud period, the above sampling scheme no longer suffices. In this case, the stop-bit is not sampled, and no framing error is generated in the receiver if the stop-bit is not generated. The line must still be driven high before the next start bit however for the USART to successfully identify the start bit.

#### 19.3.2.12 Parity Error

When parity bits are enabled, a parity check is automatically performed on incoming frames. When a parity error is detected in an incoming frame, the data parity error bit PERR in the frame is set, as well as the interrupt flag PERR in USARTn\_IF. Frames with parity errors are loaded into the receive buffer like regular frames.

PERR can be accessed by reading the frame from the receive buffer using the USARTn\_RXDATA, USARTn\_RXDATAXP, USARTn\_RXDOUBLEX or USARTn\_RXDOUBLEXP registers.

If ERRSTX in USARTn\_CTRL is set, the transmitter is disabled on received parity and framing errors. If ERRSRX in USARTn\_CTRL is set, the receiver is disabled on parity and framing errors.

#### 19.3.2.13 Framing Error and Break Detection

A framing error is the result of an asynchronous frame where the stop bit was sampled to a value of 0. This can be the result of noise and baud rate errors, but can also be the result of a break generated by the transmitter on purpose.

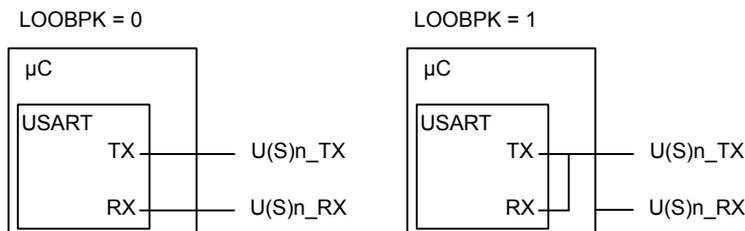
When a framing error is detected in an incoming frame, the framing error bit FERR in the frame is set. The interrupt flag FERR in USARTn\_IF is also set. Frames with framing errors are loaded into the receive buffer like regular frames.

FERR can be accessed by reading the frame from the receive buffer using the USARTn\_RXDATA, USARTn\_RXDATAXP, USARTn\_RXDOUBLEX or USARTn\_RXDOUBLEXP registers.

If ERRSTX in USARTn\_CTRL is set, the transmitter is disabled on parity and framing errors. If ERRSRX in USARTn\_CTRL is set, the receiver is disabled on parity and framing errors.

### 19.3.2.14 Local Loopback

The USART receiver samples U(S)n\_RX by default, and the transmitter drives U(S)n\_TX by default. This is not the only option however. When LOOPBK in USARTn\_CTRL is set, the receiver is connected to the U(S)n\_TX pin as shown in [Figure 19.9 USART Local Loopback on page 581](#). This is useful for debugging, as the USART can receive the data it transmits, but it is also used to allow the USART to read and write to the same pin, which is required for some half duplex communication modes. In this mode, the U(S)n\_TX pin must be enabled as an output in the GPIO.



**Figure 19.9. USART Local Loopback**

### 19.3.2.15 Asynchronous Half Duplex Communication

When doing full duplex communication, two data links are provided, making it possible for data to be sent and received at the same time. In half duplex mode, data is only sent in one direction at a time. There are several possible half duplex setups, as described in the following sections.

### 19.3.2.16 Single Data-link

In this setup, the USART both receives and transmits data on the same pin. This is enabled by setting LOOPBK in USARTn\_CTRL, which connects the receiver to the transmitter output. Because they are both connected to the same line, it is important that the USART transmitter does not drive the line when receiving data, as this would corrupt the data on the line.

When communicating over a single data-link, the transmitter must thus be tristated whenever not transmitting data. This is done by setting the command bit TXTRIEN in USARTn\_CMD, which tristates the transmitter. Before transmitting data, the command bit TXTRIDIS, also in USARTn\_CMD, must be set to enable transmitter output again. Whether or not the output is tristated at a given time can be read from TXTRI in USARTn\_STATUS. If TXTRI is set when transmitting data, the data is shifted out of the shift register, but is not put out on U(S)n\_TX.

When operating a half duplex data bus, it is common to have a bus master, which first transmits a request to one of the bus slaves, then receives a reply. In this case, the frame transmission control bits, which can be set by writing to USARTn\_TXDATAx, can be used to make the USART automatically disable transmission, tristate the transmitter and enable reception when the request has been transmitted, making it ready to receive a response from the slave.

The timer, [19.3.10 Timer](#), can also be used to add delay between the RX and TX frames so that the interrupt service routine has time to process data that was just received before transmitting more data. Also hardware flow control is another method to insert time for processing the frame. RTS and CTS can be used to halt either the link partner's transmitter or the local transmitter. See the section on hardware flow control, [19.3.4 Hardware Flow Control](#), for more details.

Tristating the transmitter can also be performed automatically by the USART by using AUTOTRI in USARTn\_CTRL. When AUTOTRI is set, the USART automatically tristates U(S)n\_TX whenever the transmitter is idle, and enables transmitter output when the transmitter goes active. If AUTOTRI is set TXTRI is always read as 0.

**Note:** Another way to tristate the transmitter is to enable wired-and or wired-or mode in GPIO. For wired-and mode, outputting a 1 will be the same as tristating the output, and for wired-or mode, outputting a 0 will be the same as tristating the output. This can only be done on buses with a pull-up or pull-down resistor respectively.

### 19.3.2.17 Single Data-link With External Driver

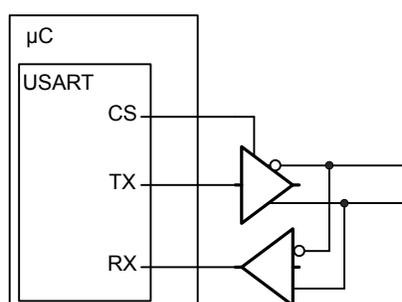
Some communication schemes, such as RS-485 rely on an external driver. Here, the driver has an extra input which enables it, and instead of tristating the transmitter when receiving data, the external driver must be disabled.

This can be done manually by assigning a GPIO to turn the driver on or off, or it can be handled automatically by the USART. If AUTOCS in USARTn\_CTRL is set, the USn\_CS output is automatically activated a configurable number of baud periods before the transmitter starts transmitting data, and deactivated a configurable number of baud periods after the last bit has been transmitted and there is no more data in the transmit buffer to transmit. The number of baud periods are controlled by CSSETUP and CSHOLD in USARTn\_TIMING. This feature can be used to turn the external driver on when transmitting data, and turn it off when the data has been transmitted.

The timer, [19.3.10 Timer](#), can also be used to configure CSSETUP and CSHOLD values between 1 to 256 baud-times by using TCMPVAL0, TCMPVAL1, or TCMPVAL2 for the TX sequencer.

USn\_CS is immediately deasserted when the transmitter becomes disabled.

[Figure 19.10 USART Half Duplex Communication with External Driver on page 582](#) shows an example configuration where USn\_CS is used to automatically enable and disable an external driver.



**Figure 19.10. USART Half Duplex Communication with External Driver**

The USn\_CS output is active low by default, but its polarity can be changed with CSINV in USARTn\_CTRL. AUTOCS works regardless of which mode the USART is in, so this functionality can also be used for automatic chip/slave select when in synchronous mode (e.g. SPI).

### 19.3.2.18 Two Data-links

Some limited devices only support half duplex communication even though two data links are available. In this case software is responsible for making sure data is not transmitted when incoming data is expected.

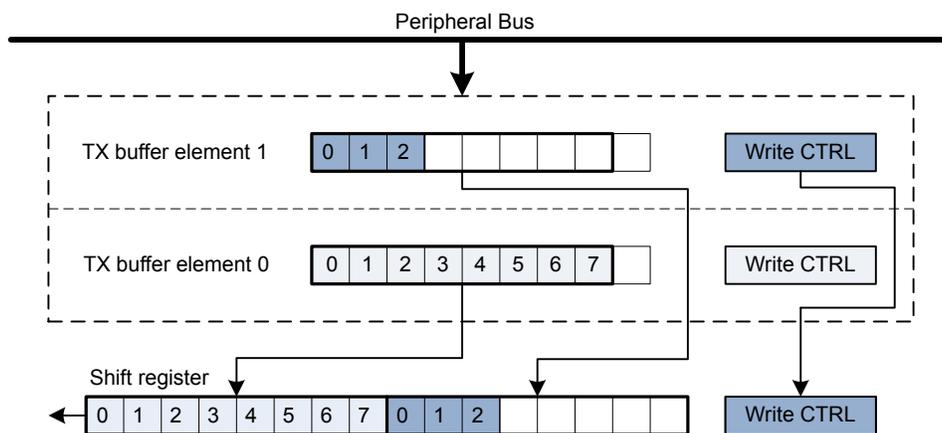
TXARXnEN in USARTn\_TRIGCTRL may be used to automatically start transmission after the end of the RX frame plus any TXSTDELAY and CSSETUP delay in USARTn\_TIMING. For enabling the receiver either use RXENAT in USARTn\_TXDATAx or RXATXnEN in USARTn\_TRIGCTRL.

### 19.3.2.19 Large Frames

As each frame in the transmit and receive buffers holds a maximum of 9 bits, both the elements in the buffers are combined when working with USART-frames of 10 or more data bits.

To transmit such a frame, at least two elements must be available in the transmit buffer. If only one element is available, the USART will wait for the second element before transmitting the combined frame. Both the elements making up the frame are consumed when transmitting such a frame.

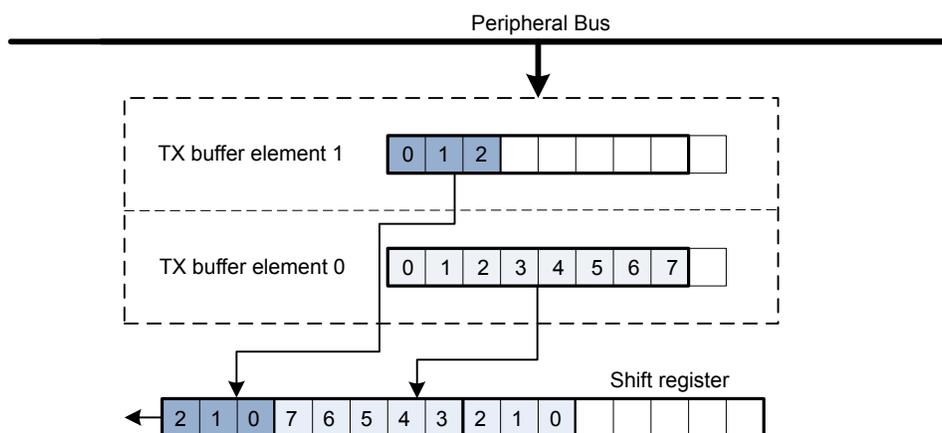
When using large frames, the 9th bits in the buffers are unused. For an 11 bit frame, the 8 least significant bits are thus taken from the first element in the buffer, and the 3 remaining bits are taken from the second element as shown in [Figure 19.11 USART Transmission of Large Frames on page 583](#). The first element in the transmit buffer, i.e. element 0 in [Figure 19.11 USART Transmission of Large Frames on page 583](#) is the first element written to the FIFO, or the least significant byte when writing two bytes at a time using USARTn\_TXDOUBLE.



**Figure 19.11. USART Transmission of Large Frames**

As shown in [Figure 19.11 USART Transmission of Large Frames on page 583](#), frame transmission control bits are taken from the second element in FIFO.

The two buffer elements can be written at the same time using the USARTn\_TXDOUBLE or USARTn\_TXDOUBLEX register. The TXDATAx0 bitfield then refers to buffer element 0, and TXDATAx1 refers to buffer element 1.

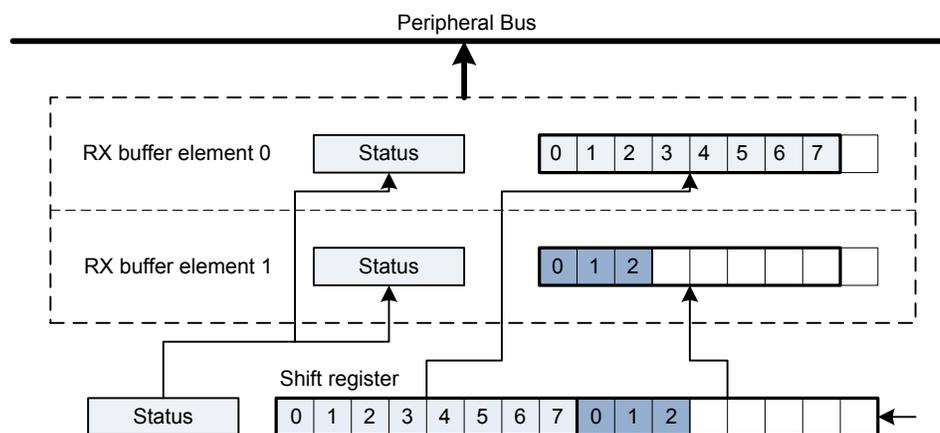


**Figure 19.12. USART Transmission of Large Frames, MSBF**

[Figure 19.12 USART Transmission of Large Frames, MSBF on page 583](#) illustrates the order of the transmitted bits when an 11 bit frame is transmitted with MSBF set. If MSBF is set and the frame is smaller than 10 bits, only the contents of transmit buffer 0 will be transmitted.

When receiving a large frame, `BYTESWAP` in `USARTn_CTRL` determines the order the way the large frame is split into the two buffer elements. If `BYTESWAP` is cleared, the least significant 8 bits of the received frame are loaded into the first element of the receive buffer, and the remaining bits are loaded into the second element, as shown in [Figure 19.13 USART Reception of Large Frames on page 584](#). The first byte read from the buffer thus contains the 8 least significant bits. Set `BYTESWAP` to reverse the order.

The status bits are loaded into both elements of the receive buffer. The frame is not moved from the receive shift register before there are two free spaces in the receive buffer.



**Figure 19.13. USART Reception of Large Frames**

The two buffer elements can be read at the same time using the `USARTn_RXDOUBLE` or `USARTn_RXDOUBLEX` register. `RXDATA0` then refers to buffer element 0 and `RXDATA1` refers to buffer element 1.

Large frames can be used in both asynchronous and synchronous modes.

### 19.3.2.20 Multi-Processor Mode

To simplify communication between multiple processors, the USART supports a special multi-processor mode. In this mode the 9th data bit in each frame is used to indicate whether the content of the remaining 8 bits is data or an address.

When multi-processor mode is enabled, an incoming 9-bit frame with the 9th bit equal to the value of `MPAB` in `USARTn_CTRL` is identified as an address frame. When an address frame is detected, the `MPAF` interrupt flag in `USARTn_IF` is set, and the address frame is loaded into the receive register. This happens regardless of the value of `RXBLOCK` in `USARTn_STATUS`.

Multi-processor mode is enabled by setting `MPM` in `USARTn_CTRL`, and the value of the 9th bit in address frames can be set in `MPAB`. Note that the receiver must be enabled for address frames to be detected. The receiver can be blocked however, preventing data from being loaded into the receive buffer while looking for address frames.

Basic usage of the multi-processor mode is as follows:

1. All slaves enable multi-processor mode and, enable and block the receiver. They will now not receive data unless it is an address frame. `MPAB` in `USARTn_CTRL` is set to identify frames with the 9th bit high as address frames.
2. The master sends a frame containing the address of a slave and with the 9th bit set
3. All slaves receive the address frame and get an interrupt. They can read the address from the receive buffer. The selected slave unblocks the receiver to start receiving data from the master.
4. The master sends data with the 9th bit cleared
5. Only the slave with RX enabled receives the data. When transmission is complete, the slave blocks the receiver and waits for a new address frame.

When a slave has received an address frame and wants to receive the following data, it must make sure the receiver is unblocked before the next frame has been completely received in order to prevent data loss.

`BIT8DV` in `USARTn_CTRL` can be used to specify the value of the 9th bit without writing to the transmit buffer with `USARTn_TXDATAx` or `USARTn_TXDOUBLEX`, giving higher efficiency in multi-processor mode, as the 9th bit is only set when writing address frames, and 8-bit writes to the USART can be used when writing the data frames.

### 19.3.2.21 Collision Detection

The USART supports a basic form of collision detection. When the receiver is connected to the output of the transmitter, either by using the LOOPBK bit in USARTn\_CTRL or through an external connection, this feature can be used to detect whether data transmitted on the bus by the USART did get corrupted by a simultaneous transmission by another device on the bus.

For collision detection to be enabled, CCEN in USARTn\_CTRL must be set, and the receiver enabled. The data sampled by the receiver is then continuously compared with the data output by the transmitter. If they differ, the CCF interrupt flag in USARTn\_IF is set. The collision check includes all bits of the transmitted frames. The CCF interrupt flag is set once for each bit sampled by the receiver that differs from the bit output by the transmitter. When the transmitter output is disabled, i.e. the transmitter is tristated, collisions are not registered.

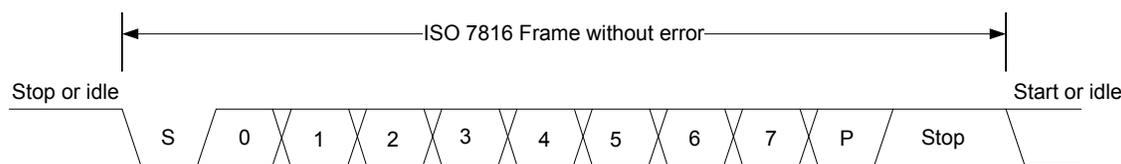
### 19.3.2.22 SmartCard Mode

In SmartCard mode, the USART supports the ISO 7816 I/O line T0 mode. With exception of the stop-bits (guard time), the 7816 data frame is equal to the regular asynchronous frame. In this mode, the receiver pulls the line low for one baud, half a baud into the guard time to indicate a parity error. This NAK can for instance be used by the transmitter to re-transmit the frame. SmartCard mode is a half duplex asynchronous mode, so the transmitter must be tristated whenever not transmitting data.

To enable SmartCard mode, set SCMODE in USARTn\_CTRL, set the number of databits in a frame to 8, and configure the number of stopbits to 1.5 by writing to STOPBITS in USARTn\_FRAME.

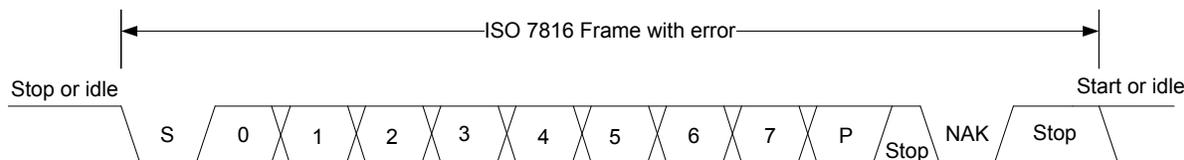
The SmartCard mode relies on half duplex communication on a single line, so for it to work, both the receiver and transmitter must work on the same line. This can be achieved by setting LOOPBK in USARTn\_CTRL or through an external connection. The TX output should be configured as open-drain in the GPIO module.

When no parity error is identified by the receiver, the data frame is as shown in [Figure 19.14 USART ISO 7816 Data Frame Without Error on page 586](#). The frame consists of 8 data bits, a parity bit, and 2 stop bits. The transmitter does not drive the output line during the guard time.



**Figure 19.14. USART ISO 7816 Data Frame Without Error**

If a parity error is detected by the receiver, it pulls the line I/O line low after half a stop bit, see [Figure 19.15 USART ISO 7816 Data Frame With Error on page 586](#). It holds the line low for one bit-period before it releases the line. In this case, the guard time is extended by one bit period before a new transmission can start, resulting in a total of 3 stop bits.



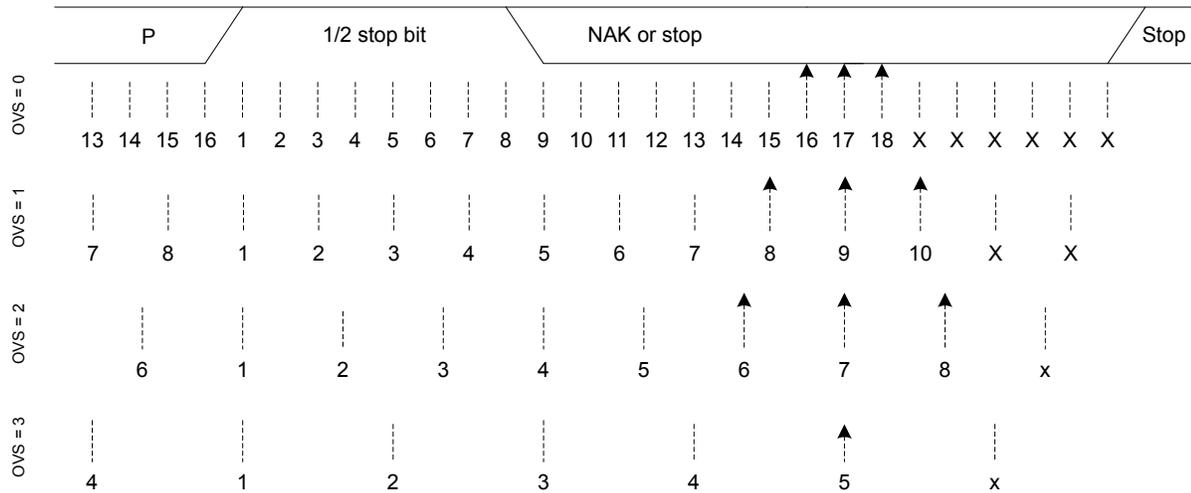
**Figure 19.15. USART ISO 7816 Data Frame With Error**

On a parity error, the NAK is generated by hardware. The NAK generated by the receiver is sampled as the stop-bit of the frame. Because of this, parity errors when in SmartCard mode are reported with both a parity error and a framing error.

When transmitting a T0 frame, the USART receiver on the transmitting side samples position 16, 17 and 18 in the stop-bit to detect the error signal when in 16x oversampling mode as shown in [Figure 19.16 USART SmartCard Stop Bit Sampling on page 587](#). Sampling at this location places the stop-bit sample in the middle of the bit-period used for the error signal (NAK).

If a NAK is transmitted by the receiver, it will thus appear as a framing error at the transmitter, and the FERR interrupt flag in USARTn\_IF will be set. If SCRETRANS USARTn\_CTRL is set, the transmitter will automatically retransmit a NACK'ed frame. The transmitter will retransmit the frame until it is ACK'ed by the receiver. This only works when the number of databits in a frame is configured to 8.

Set SKIPERRF in USARTn\_CTRL to make the receiver discard frames with parity errors. The PERR interrupt flag in USARTn\_IF is set when a frame is discarded because of a parity error.



**Figure 19.16. USART SmartCard Stop Bit Sampling**

For communication with a SmartCard, a clock signal needs to be generated for the card. This clock output can be generated using one of the timers. See the ISO 7816 specification for more info on this clock signal.

SmartCard T1 mode is also supported. The T1 frame format used is the same as the asynchronous frame format with parity bit enabled and one stop bit. The USART must then be configured to operate in asynchronous half duplex mode.

### 19.3.3 Synchronous Operation

Most of the features in asynchronous mode are available in synchronous mode. Multi-processor mode can be enabled for 9-bit frames, loopback is available and collision detection can be performed.

#### 19.3.3.1 Frame Format

The frames used in synchronous mode need no start and stop bits since a single clock is available to all parts participating in the communication. Parity bits cannot be used in synchronous mode.

The USART supports frame lengths of 4 to 16 bits per frame. Larger frames can be simulated by transmitting multiple smaller frames, i.e. a 22 bit frame can be sent using two 11-bit frames, and a 21 bit frame can be generated by transmitting three 7-bit frames. The number of bits in a frame is set using DATABITS in USARTn\_FRAME.

The frames in synchronous mode are by default transmitted with the least significant bit first like in asynchronous mode. The bit-order can be reversed by setting MSBF in USARTn\_CTRL.

The frame format used by the transmitter can be inverted by setting TXINV in USARTn\_CTRL, and the format expected by the receiver can be inverted by setting RXINV, also in USARTn\_CTRL.

### 19.3.3.2 Clock Generation

The bit-rate in synchronous mode is given by [Figure 19.17 USART Synchronous Mode Bit Rate on page 588](#). As in the case of asynchronous operation, the clock division factor have a 15-bit integral part and a 5-bit fractional part.

$$br = f_{HFPERCLK} / (2 \times (1 + USARTn\_CLKDIV/256))$$

**Figure 19.17. USART Synchronous Mode Bit Rate**

Given a desired baud rate  $br_{desired}$ , the clock divider  $USARTn\_CLKDIV$  can be calculated using [Figure 19.18 USART Synchronous Mode Clock Division Factor on page 588](#)

$$USARTn\_CLKDIV = 256 \times (f_{HFPERCLK} / (2 \times br_{desired}) - 1)$$

**Figure 19.18. USART Synchronous Mode Clock Division Factor**

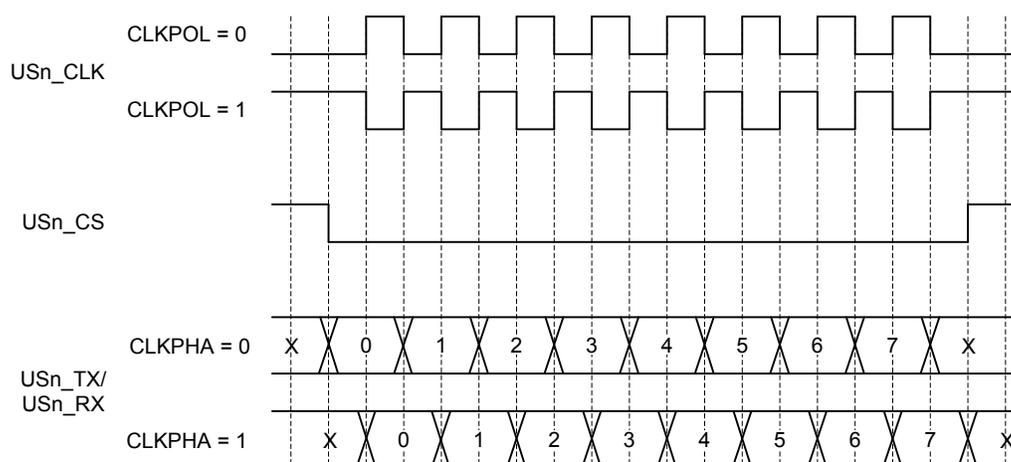
When the USART operates in master mode, the highest possible bit rate is half the peripheral clock rate. When operating in slave mode however, the highest bit rate is an eighth of the peripheral clock:

- Master mode:  $br_{max} = f_{HFPERCLK}/2$
- Slave mode:  $br_{max} = f_{HFPERCLK}/8$

On every clock edge data on the data lines, MOSI and MISO, is either set up or sampled. When  $CLKPHA$  in  $USARTn\_CTRL$  is cleared, data is sampled on the leading clock edge and set-up is done on the trailing edge. If  $CLKPHA$  is set however, data is set-up on the leading clock edge, and sampled on the trailing edge. In addition to this, the polarity of the clock signal can be changed by setting  $CLKPOL$  in  $USARTn\_CTRL$ , which also defines the idle state of the clock. This results in four different modes which are summarized in [Table 19.8 USART SPI Modes on page 588](#). [Figure 19.19 USART SPI Timing on page 588](#) shows the resulting timing of data set-up and sampling relative to the bus clock.

**Table 19.8. USART SPI Modes**

| SPI mode | CLKPOL | CLKPHA | Leading Edge    | Trailing Edge   |
|----------|--------|--------|-----------------|-----------------|
| 0        | 0      | 0      | Rising, sample  | Falling, set-up |
| 1        | 0      | 1      | Rising, set-up  | Falling, sample |
| 2        | 1      | 0      | Falling, sample | Rising, set-up  |
| 3        | 1      | 1      | Falling, set-up | Rising, sample  |



**Figure 19.19. USART SPI Timing**

If  $CPHA=1$ , the TX underflow flag,  $TXUF$ , will be set on the first setup clock edge of a frame in slave mode if TX data is not available. If  $CPHA=0$ ,  $TXUF$  is set if data is not available in the transmit buffer three  $HFPERCLK$  cycles prior to the first sample clock edge. The

RXDATAV flag is updated on the last sample clock edge of a transfer, while the RX overflow interrupt flag, RXOF, is set on the first sample clock edge if the receive buffer overflows. When a transfer has been performed, interrupt flags TXBL and TXC are updated on the first setup clock edge of the succeeding frame, or when CS is deasserted.

#### 19.3.3.3 Master Mode

When in master mode, the USART is in full control of the data flow on the synchronous bus. When operating in full duplex mode, the slave cannot transmit data to the master without the master transmitting to the slave. The master outputs the bus clock on USn\_CLK.

Communication starts whenever there is data in the transmit buffer and the transmitter is enabled. The USART clock then starts, and the master shifts bits out from the transmit shift register using the internal clock.

When there are no more frames in the transmit buffer and the transmit shift register is empty, the clock stops, and communication ends. When the receiver is enabled, it samples data using the internal clock when the transmitter transmits data. Operation of the RX and TX buffers is as in asynchronous mode.

#### 19.3.3.4 Operation of USn\_CS Pin

When operating in master mode, the USn\_CS pin can have one of two functions, or it can be disabled.

If USn\_CS is configured as an output, it can be used to automatically generate a chip select for a slave by setting AUTOCS in USARTn\_CTRL. If AUTOCS is set, USn\_CS is activated before a transmission begins, and deactivated after the last bit has been transmitted and there is no more data in the transmit buffer.

The time between when CS is asserted and the first bit is transmitted can be controlled using the USART Timer and with CSSETUP in USARTn\_TIMING. Any of the three comparators can be used to set this delay. If new data is ready for transmission before CS is deasserted, the data is sent without deasserting CS in between. CSHOLD in USARTn\_TIMING keeps CS asserted after the end of frame for the number of baud-times specified.

By default, USn\_CS is active low, but its polarity can be inverted by setting CSINV in USARTn\_CTRL.

When USn\_CS is configured as an input, it can be used by another master that wants control of the bus to make the USART release it. When USn\_CS is driven low, or high if CSINV is set, the interrupt flag SSM in USARTn\_IF is set, and if CSMA in USARTn\_CTRL is set, the USART goes to slave mode.

#### 19.3.3.5 AUTOTX

A synchronous master is required to transmit data to a slave in order to receive data from the slave. In some cases, only a few words are transmitted and a lot of data is then received from the slave. In that case, one solution is to keep feeding the TX with data to transmit, but that consumes system bandwidth. Instead AUTOTX can be used.

When AUTOTX in USARTn\_CTRL is set, the USART transmits data as long as there is available space in the RX shift register for the chosen frame size. This happens even though there is no data in the TX buffer. The TX underflow interrupt flag TXUF in USARTn\_IF is set on the first word that is transmitted which does not contain valid data.

During AUTOTX the USART will always send the previous sent bit, thus reducing the number of transitions on the TX output. So if the last bit sent was a 0, 0's will be sent during AUTOTX and if the last bit sent was a 1, 1's will be sent during AUTOTX.

#### 19.3.3.6 Slave Mode

When the USART is in slave mode, data transmission is not controlled by the USART, but by an external master. The USART is therefore not able to initiate a transmission, and has no control over the number of bytes written to the master.

The output and input to the USART are also swapped when in slave mode, making the receiver take its input from USn\_TX (MOSI) and the transmitter drive USn\_RX (MISO).

To transmit data when in slave mode, the slave must load data into the transmit buffer and enable the transmitter. The data will remain in the USART until the master starts a transmission by pulling the USn\_CS input of the slave low and transmitting data. For every frame the master transmits to the slave, a frame is transferred from the slave to the master. After a transmission, MISO remains in the same state as the last bit transmitted. This also applies if the master transmits to the slave and the slave TX buffer is empty.

If the transmitter is enabled in synchronous slave mode and the master starts transmission of a frame, the underflow interrupt flag TXUF in USARTn\_IF will be set if no data is available for transmission to the master.

If the slave needs to control its own chip select signal, this can be achieved by clearing CSPEN in the ROUTE register. The internal chip select signal can then be controlled through CSINV in the CTRL register. The chip select signal will be CSINV inverted, i.e. if CSINV is cleared, the chip select is active and vice versa.

### 19.3.3.7 Synchronous Half Duplex Communication

Half duplex communication in synchronous mode is very similar to half duplex communication in asynchronous mode as detailed in [19.3.2.15 Asynchronous Half Duplex Communication](#). The main difference is that in this mode, the master must generate the bus clock even when it is not transmitting data, i.e. it must provide the slave with a clock to receive data. To generate the bus clock, the master should transmit data with the transmitter tristated, i.e. TXTRI in USARTn\_STATUS set, when receiving data. If 2 bytes are expected from the slave, then transmit 2 bytes with the transmitter tristated, and the slave uses the generated bus clock to transmit data to the master. TXTRI can be set by setting the TXTRIEN command bit in USARTn\_CMD.

**Note:** When operating as SPI slave in half duplex mode, TX has to be tristated (not disabled) during data reception if the slave is to transmit data in the current transfer.

### 19.3.3.8 I2S

I2S is a synchronous format for transmission of audio data. The frame format is 32-bit, but since data is always transmitted with MSB first, an I2S device operating with 16-bit audio may choose to only process the 16 msb of the frame, and only transmit data in the 16 msb of the frame.

In addition to the bit clock used for regular synchronous transfers, I2S mode uses a separate word clock. When operating in mono mode, with only one channel of data, the word clock pulses once at the start of each new word. In stereo mode, the word clock toggles at the start of new words, and also gives away whether the transmitted word is for the left or right audio channel; A word transmitted while the word clock is low is for the left channel, and a word transmitted while the word clock is high is for the right.

When operating in I2S mode, the CS pin is used as a the word clock. In master mode, this is automatically driven by the USART, and in slave mode, the word clock is expected from an external master.

### 19.3.3.9 Word Format

The general I2S word format is 32 bits wide, but the USART also supports 16-bit and 8-bit words. In addition to this, it can be specified how many bits of the word should actually be used by the USART. These parameters are given by FORMAT in USARTn\_I2SCTRL.

As an example, configuring FORMAT to using a 32-bit word with 16-bit data will make each word on the I2S bus 32-bits wide, but when receiving data through the USART, only the 16 most significant bits of each word can be read out of the USART. Similarly, only the 16 most significant bits have to be written to the USART when transmitting. The rest of the bits will be transmitted as zeroes.

### 19.3.3.10 Major Modes

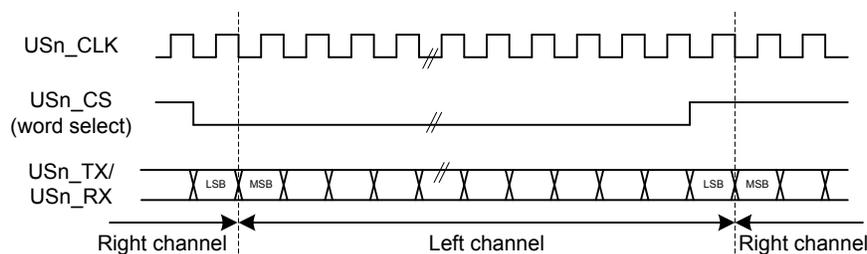
The USART supports a set of different I2S formats as shown in [Table 19.9 USART I2S Modes on page 591](#), but it is not limited to these modes. MONO, JUSTIFY and DELAY in USARTn\_I2SCTRL can be mixed and matched to create an appropriate format. MONO enables mono mode, i.e. one data stream instead of two which is the default. JUSTIFY aligns data within a word on the I2S bus, either left or right which can be seen in figures [Figure 19.22 USART Left-Justified I2S Waveform on page 592](#) and [Figure 19.23 USART Right-Justified I2S Waveform on page 592](#). Finally, DELAY specifies whether a new I2S word should be started directly on the edge of the word-select signal, or one bit-period after the edge.

**Table 19.9. USART I2S Modes**

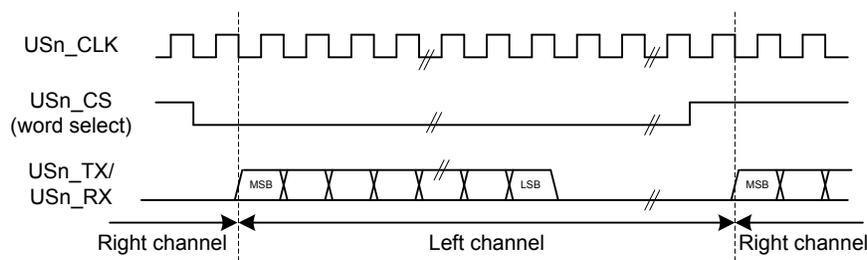
| Mode            | MONO | JUSTIFY | DELAY | CLKPOL |
|-----------------|------|---------|-------|--------|
| Regular I2S     | 0    | 0       | 1     | 0      |
| Left-Justified  | 0    | 0       | 0     | 1      |
| Right-Justified | 0    | 1       | 0     | 1      |
| Mono            | 1    | 0       | 0     | 0      |

The regular I2S waveform is shown in [Figure 19.20 USART Standard I2S Waveform on page 591](#) and [Figure 19.21 USART Standard I2S Waveform \(Reduced Accuracy\) on page 591](#). The first figure shows a waveform transmitted with full accuracy. The wordlength can be configured to 32-bit, 16-bit or 8-bit using FORMAT in USARTn\_I2SCTRL. In the second figure, I2S data is transmitted with reduced accuracy, i.e. the data transmitted has less bits than what is possible in the bus format.

Note that the msb of a word transmitted in regular I2S mode is delayed by one cycle with respect to word select

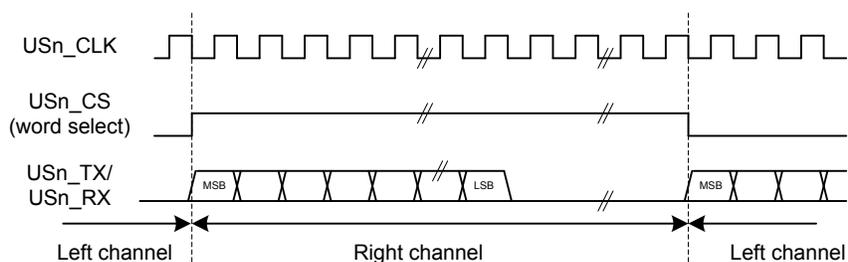


**Figure 19.20. USART Standard I2S Waveform**



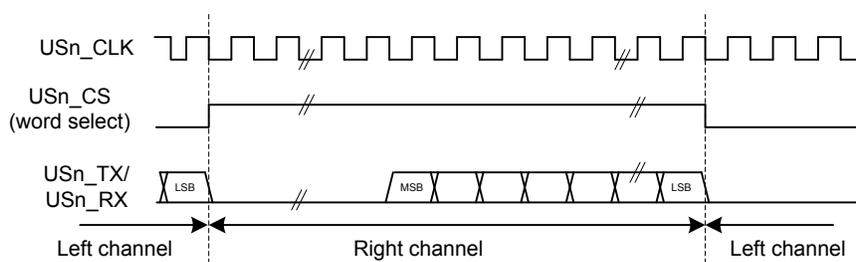
**Figure 19.21. USART Standard I2S Waveform (Reduced Accuracy)**

A left-justified stream is shown in [Figure 19.22 USART Left-Justified I2S Waveform on page 592](#). Note that the MSB comes directly after the edge on the word-select signal in contradiction to the regular I2S waveform where it comes one bit-period after.



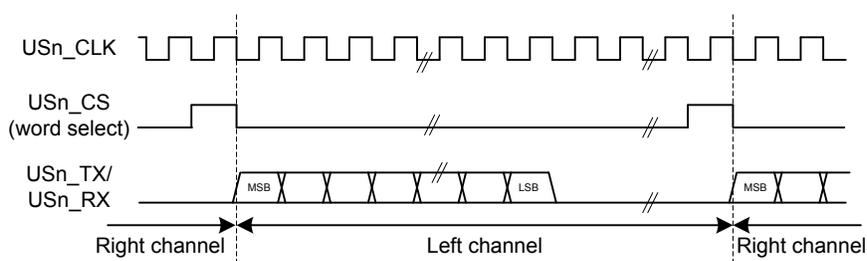
**Figure 19.22. USART Left-Justified I2S Waveform**

A right-justified stream is shown in [Figure 19.23 USART Right-Justified I2S Waveform on page 592](#). The left and right justified streams are equal when the data-size is equal to the word-width.



**Figure 19.23. USART Right-Justified I2S Waveform**

In mono-mode, the word-select signal pulses at the beginning of each word instead of toggling for each word. Mono I2S waveform is shown in [Figure 19.24 USART Mono I2S Waveform on page 592](#).



**Figure 19.24. USART Mono I2S Waveform**

### 19.3.3.11 Using I2S Mode

When using the USART in I2S mode, `DATABITS` in `USARTn_FRAME` must be set to 8 or 16 data-bits. 8 databits can be used in all modes, and 16 can be used in the modes where the number of bytes in the I2S word is even. In addition to this, `MSBF` in `USARTn_CTRL` should be set, and `CLKPOL` and `CLKPHA` in `USARTn_CTRL` should be cleared.

The USART does not have separate TX and RX buffers for left and right data, so when using I2S in stereo mode, the application must keep track of whether the buffers contain left or right data. This can be done by observing `TXBLRIGHT`, `RXDATAVRIGHT` and `RXFULLRIGHT` in `USARTn_STATUS`. `TXBLRIGHT` tells whether TX is expecting data for the left or right channel. It will be set with `TXBL` if right data is expected. The receiver will set `RXDATAVRIGHT` if there is at least one right element in the buffer, and `RXFULLRIGHT` if the buffer is full of right elements.

When using I2S with DMA, separate DMA requests can be used for left and right data by setting `DMA SPLIT` in `USARTn_I2SCTRL`.

In both master and slave mode the USART always starts transmitting on the LEFT channel after being enabled. In master mode, the transmission will stop if TX becomes empty. In that case, `TXC` is set. Continuing the transmission in this case will make the data-stream continue where it left off. To make the USART start on the LEFT channel after going empty, disable and re-enable TX.

### 19.3.4 Hardware Flow Control

Hardware flow control can be used to hold off the link partner's transmission until RX buffer space is available. Use `RTSPEN` and `CTSPEN` in `USARTn_ROUTE PEN` to allocate the hardware flow control to GPIOs. `RTS` is an out going signal which indicates that RX buffer space is available to receive a frame. The link partner is being requested to send its data when `RTS` is asserted. `CTS` is an incoming signal to stop the next TX data from going out. When `CTS` is negated, the frame currently being transmitted is completed before stopping. `CTS` indicates that the link partner has RX buffer space available, and the local transmitter is clear to send. Also use `CTSEN` in `USARTn_CTRLX` to enable the `CTS` input into the TX sequencer. For debug use set `DBGHALT` in `USARTn_CTRLX` which will force the `RTS` to request one frame from the link partner when the CPU core single steps.

### 19.3.5 Debug Halt

When `DBGHALT` in `USARTn_CTRLX` is clear, `RTS` is only dependent on the RX buffer having space available to receive data. Incoming data is always received until both the RX buffer is full and the RX shift register is full regardless of the state of `DBGHALT` or chip halt. Additional incoming data is discarded. When `DBGHALT` is set, `RTS` deasserts on RX buffer full or when chip halt is high. However, a low pulse detected on chip halt will keep `RTS` asserted when no frame is being received. At the start of frame reception, `RTS` will deassert if chip halt is high and `DBGHALT` is set. This behavior allows single stepping to pulse the chip halt low for a cycle, and receive the next frame. The link partner must stop transmitting when `RTS` is deasserted, or the RX buffer could overflow. All data in the transmit buffer is sent out even when chip halt is asserted; therefore, the DMA will need to be set to stop sending the USART TX data during chip halt.

### 19.3.6 PRS-triggered Transmissions

If a transmission must be started on an event with very little delay, the PRS system can be used to trigger the transmission. The PRS channel to use as a trigger can be selected using `TSEL` in `USARTn_TRIGCTRL`. When a positive edge is detected on this signal, the receiver is enabled if `RXTEN` in `USARTn_TRIGCTRL` is set, and the transmitter is enabled if `TXTEN` in `USARTn_TRIGCTRL` is set. Only one signal input is supported by the USART.

The `AUTOTX` feature can also be enabled via PRS. If an external SPI device sets a pin high when there is data to be read from the device, this signal can be routed to the USART through the PRS system and be used to make the USART clock data out of the external device. If `AUTOTXTEN` in `USARTn_TRIGCTRL` is set, the USART will transmit data whenever the PRS signal selected by `TSEL` is high given that there is enough room in the RX buffer for the chosen frame size. Note that if there is no data in the TX buffer when using `AUTOTX`, the TX underflow interrupt will be set.

`AUTOTXTEN` can also be combined with `TXTEN` to make the USART transmit a command to the external device prior to clocking out data. To do this, disable TX using the `TXDIS` command, load the TX buffer with the command and enable `AUTOTXTEN` and `TXTEN`. When the selected PRS input goes high, the USART will now transmit the loaded command, and then continue clocking out while both the PRS input is high and there is room in the RX buffer

### 19.3.7 PRS RX Input

The USART can be configured to receive data directly from a PRS channel by setting `RXP RS` in `USARTn_INPUT`. The PRS channel used is selected using `RXP RSSEL` in `USARTn_INPUT`. This way, for example, a differential RX signal can be input to the `ACMP` and the output routed via PRS to the USART.

### 19.3.8 PRS CLK Input

The USART can be configured to receive clock directly from a PRS channel by setting CLKPRS in USARTn\_INPUT. The PRS channel used is selected using CLKPRSEL in USARTn\_INPUT. This is useful in synchronous slave mode and can together with RX PRS input be used to input data from PRS.

### 19.3.9 DMA Support

The USART has full DMA support. The DMA controller can write to the transmit buffer using the registers USARTn\_TXDATA, USARTn\_TXDATAx, USARTn\_TXDOUBLE and USARTn\_TXDOUBLEx, and it can read from the receive buffer using the registers USARTn\_RXDATA, USARTn\_RXDATAx, USARTn\_RXDOUBLE and USARTn\_RXDOUBLEx. This enables single byte transfers, 9 bit data + control/status bits, double byte and double byte + control/status transfers both to and from the USART.

A request for the DMA controller to read from the USART receive buffer can come from the following source:

- Data available in the receive buffer
- Data available in the receive buffer and data is for the RIGHT I2S channel. Only used in I2S mode.

A write request can come from one of the following sources:

- Transmit buffer and shift register empty. No data to send.
- Transmit buffer has room for more data. This does not check the TXBIL for half full. For DMA use, it is either full or empty.
- Transmit buffer has room for RIGHT I2S data. Only used in I2S mode

Even though there are two sources for write requests to the DMA, only one should be used at a time, since the requests from both sources are cleared even though only one of the requests are used.

In some cases, it may be sensible to temporarily stop DMA access to the USART when an error such as a framing error has occurred. This is enabled by setting ERRSDMA in USARTn\_CTRL.

For Synchronous mode full duplex operation, if both receive buffer and transmit buffer are served by DMA, to make sure receive buffer is not overflowed the settings below should be followed.

- The DMA channel that serves receive buffer should have higher priority than the DMA channel that serves transmit buffer.
- TXBL should be used as write request for transmit buffer DMA channel.
- IGNORESREQ should be set for both DMA channel.

### 19.3.10 Timer

In addition to the TX sequence timer, there is a versatile 8 bit timer that can generate up to three event pulses. These pulses can be used to create timing for a variety of uses such as RX timeout, break detection, response timeout, and RX enable delay. Transmission delay, CS setup, inter-character spacing, and CS hold use the TX sequence counter. The TX sequencer counter can use the three 8 bit compare values or preset values for delays. There is one general counter with three comparators. Each comparator has a start source, a stop source, a restart enable, and a timer compare value. The start source enables the comparator, resets the counter, and starts the counter. If the counter is already running, the start source will reset the counter and restart it.

Any comparator could start the counter using the same start source but have different timing events programmed into TCMPVALn in USARTn\_TIMECMPn. The TCMP0, TCMP1, or TCMP2 events can be preempted by using the comparator stop source to disable the comparator before the counter reaches TCMPVAL0, TCMPVAL1, or TCMPVAL2. If one comparator gets disabled while the other comparator is still enabled, the counter continues counting. By default the counter will count up to 256 and stop unless a RESTARTEN is set in one of the USARTn\_TIMECMPn registers. By using RESTARTEN and an interval programmed into TCMPVAL, an interval timer can be set up. The TSTART field needs to be changed to DISABLE to stop the interval timer. The timer stops running once all of the comparators are disabled. If a comparator's start and stop sources both trigger the same cycle, the TCMPn event triggers, the comparator stays enabled, and the counter begins counting from zero.

The TXDELAY, CSSETUP, ICS, and CSHOLD in USARTn\_TIMING are used to program start of transmission delay, chip select setup delay, inter-character space, and chip select hold delay. Either a preset value of 0, 1, 2, 3, or 7 can be used for any of these delays; or the value in TCMPVALn may be used to set the delay. Using the preset values leaves the TCMPVALn free for other uses. The same TCMPVALn may be used for multiple events that require the same timing. The transmit sequencer's counter can run in parallel with the timer's counter. The counters and controls are shown in [Figure 19.25 USART Timer Block Diagram on page 596](#).

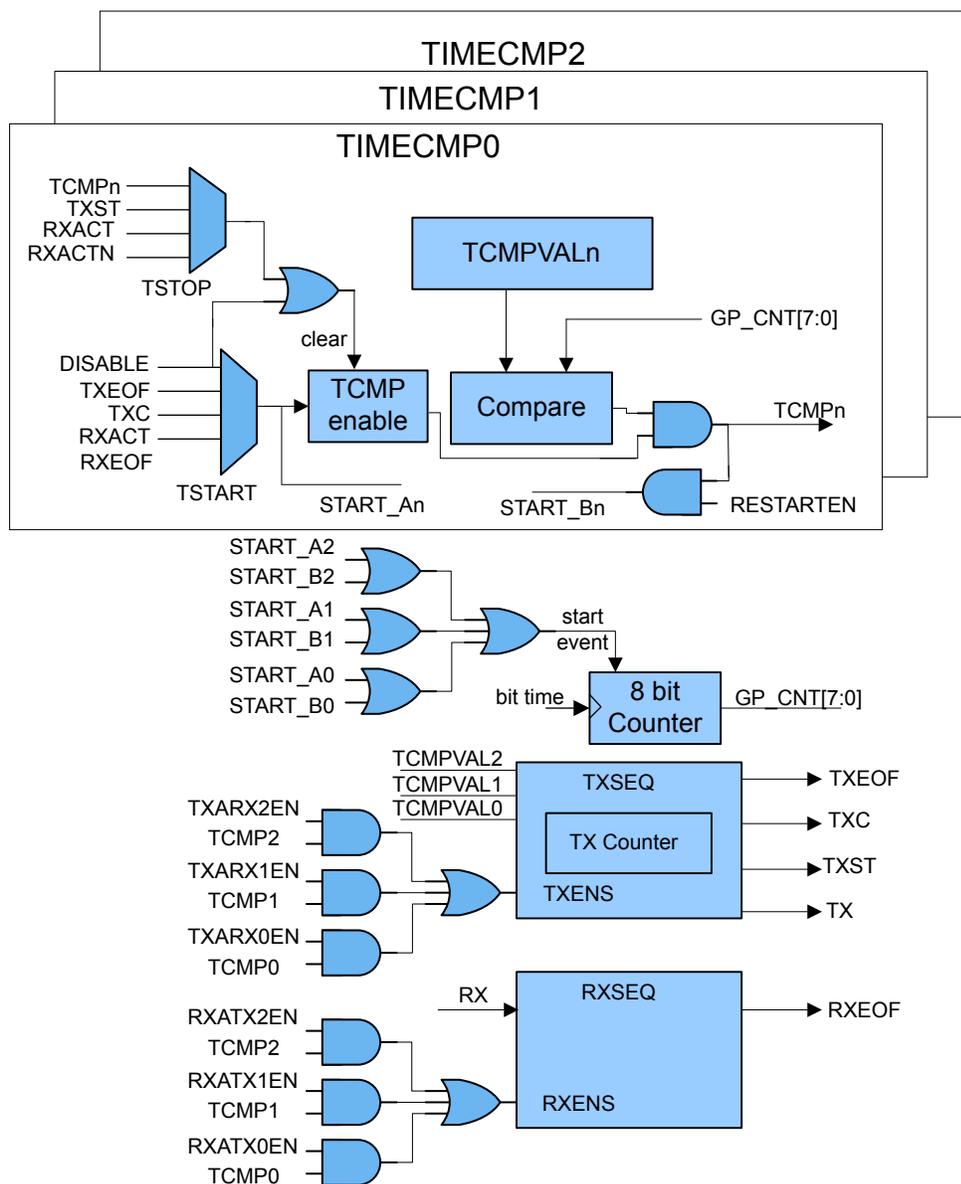


Figure 19.25. USART Timer Block Diagram

The following sections will go into more details on programming the various usage cases.

Table 19.10. USART Application Settings for USARTn\_TIMING and USARTn\_TIMECMPn

| Application            | TSTARTn                | TSTOPn         | TCMPVALn        | Other  |
|------------------------|------------------------|----------------|-----------------|--|
| Response Timeout       | TSTART0 = TXEOF        | TSTOP0 = RXACT | TCMPVAL0 = 0x08 | TCMP0 in USARTn_IEN  |
| Receiver Timeout       | TSTART1 = RXEOF        | TSTOP1 = RXACT | TCMPVAL1 = 0x08 | TCMP1 in USARTn_IEN  |
| Large Receiver Timeout | TSTART1 = RXEOF, TCMP1 | TSTOP1 = RXACT | TCMPVAL1 = 0xFF | TCMP1 in USARTn_IEN; TIME-RRESTARTED in USARTn_STATUS; RESTART1EN in USARTn_TIMECMP1 |

| Application                                      | TSTARTn                              | TSTOPn                          | TCMPVALn                         | Other   |
|--|--------------------------------------|---------------------------------|----------------------------------|---|
| Break Detect                                     | TSTART1 = RXACT                      | TSTOP1 = RXACTN                 | TCMPVAL1 = 0x0C                  | TCMP1 in USARTn_IEN   |
| TX delayed start of transmission and CS setup    | TSTART0 = DISABLE, TSTART1 = DISABLE | TSTOP0 = TCMP0, TSTOP1 = TCMP1  | TCMPVAL0 = 0x04, TCMPVAL1 = 0x02 | TXDELAY = TCMP0, CSSETUP = TCMP1 in USARTn_TIMING; AUTOCS in USARTn_CTRL            |
| TX inter-character spacing                       | TSTART2 = DISABLE                    | TSTOP2 = TCMP2                  | TCMPVAL2 = 0x03                  | ICS = TCMP2 in USARTn_TIMING; AUTOCS in USARTn_CTRL                                 |
| TX Chip Select End Delay                         | TSTART1 = DISABLE                    | TSTOP1 = TCMP1                  | TCMPVAL1 = 0x04                  | CSHOLD = TCMP1 in USARTn_TIMING; AUTOCS in USARTn_CTRL                              |
| Response Delay                                   | TSTART1 = RXEOF                      | TSTOP1 = TCMP1                  | TCMPVAL1 = 0x08                  | TXARX1EN in USARTn_TRIGCTRL   |
| Combined TX and RX Example                       | TSTART1 = RXEOF, TSTART0 = TXEOF     | TSTOP1 = TCMP1, TSTOP0 = TCMP0  | TCMPVAL1 = 0x1C, TCMPVAL0 = 0x10 | TXARX1EN, RXATX0EN in USARTn_TRIGCTRL; CSSETUP = 0x7, CSHOLD = 0x3 in USARTn_TIMING |
| Combined Delayed TX and Receiver Timeout Example | TSTART0 = TCMPVAL0, TSTART1 = RXEOF  | TSTOP0 = RXACTN, TSTOP1 = RXACT | TCMPVAL0 = 0x20, TCMPVAL1 = 0x0C | TXARX0EN in USARTn_TRIGCTRL; TCMP0 in USARTn_IEN                                    |

Table 19.10 USART Application Settings for USARTn\_TIMING and USARTn\_TIMECMPn on page 596 shows some examples of how the USART timer can be programmed for various applications. The following sections will describe more details for each applications shown in the table.

### 19.3.10.1 Response Timeout

Response Timeout is when a UART master sends a frame and expects the slave to respond within a certain number of baud-times. Refer to Table 19.10 USART Application Settings for USARTn\_TIMING and USARTn\_TIMECMPn on page 596 for specific register settings. Comparator 0 will be looking for TX end of frame to use as the timer start source. For this example, a receiver start of frame RXACT has not been detected for 8 baud-times, and the TCMP0 interrupt in USARTn\_IF is set. If an RX start bit is detected before the 8 baud-times, comparator 0 is disabled before the TCMP0 event can trigger.

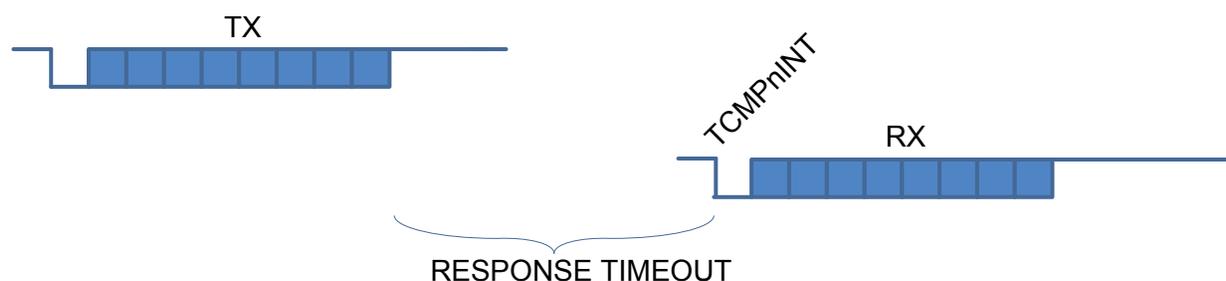


Figure 19.26. USART Response Timeout

### 19.3.10.2 RX Timeout

A receiver timeout function can be implemented by using the RX end of frame to start comparator 1 and look for the RX start bit RXACT to disable the comparator. See [Table 19.10 USART Application Settings for USARTn\\_TIMING and USARTn\\_TIMECMPn on page 596](#) for details on setting up this example. As long as the next RX start bit occurs before the counter reaches the comparator 1 value TCMPVAL1, the interrupt will not get set. In this example the RX Timeout was set to 8 baud-times. To get an RX timeout larger than 256 baud-times, RESTART1EN in USARTn\_TIMER can be used to restart the counter when it reaches TCMPVAL1. By setting TCMPVAL1 in USARTn\_TIMING to 0xFF, an interrupt will be generated after 256 baud-times. An interrupt service routine can then increment a memory location until the desired timeout is reached. Once the RX start bit is detected, comparator 1 will be disabled. If TIMERRESTARTED in USARTn\_STATUS is clear, the TCMP1 interrupt is the first interrupt after RXEOF.

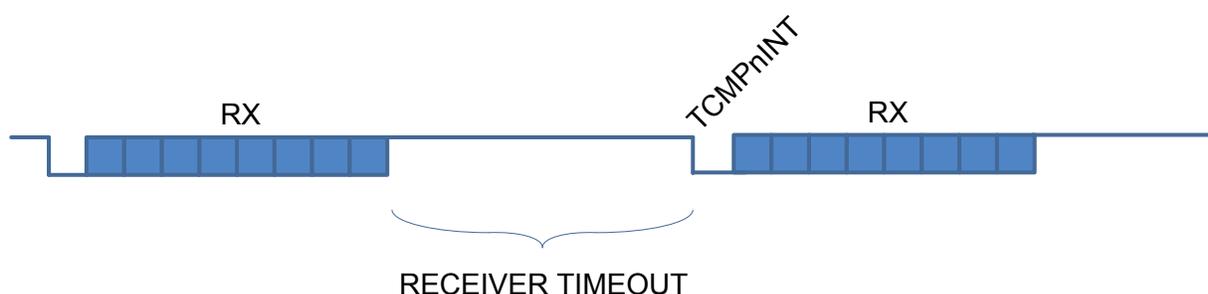


Figure 19.27. USART RX Timeout

### 19.3.10.3 Break Detect

LIN bus and half-duplex UARTs can take advantage of the timer configured for break detection where RX is held low for a number of baud-times to indicate a break condition. [Table 19.10 USART Application Settings for USARTn\\_TIMING and USARTn\\_TIMECMPn on page 596](#) shows the settings for this mode. Each time RX is active (default of low) such as for a start bit, the timer begins counting. If the counter reaches 12 baud-times before RX goes to inactive RXACTN (default of high), an interrupt is asserted.

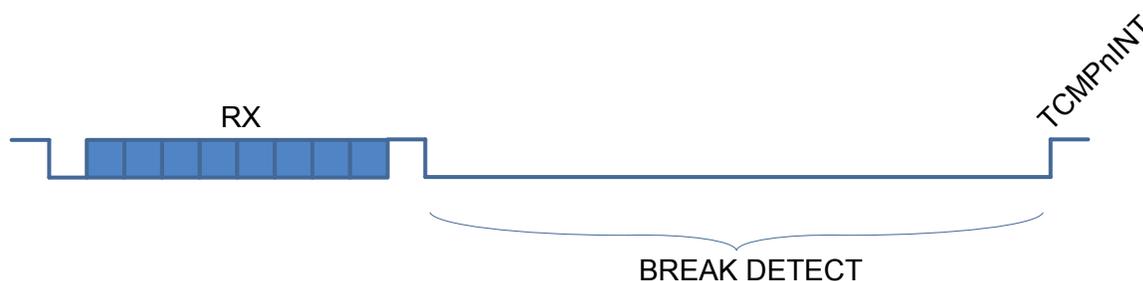


Figure 19.28. USART Break Detection

### 19.3.10.4 TX Start Delay

Some applications may require a delay before the start of transmission. This example in [Figure 19.29 USART TXSEQ Timing on page 599](#) shows the TXSEQ timer used to delay the start of transmission by 4 baud times before the start of CS, and by 2 baud times with CS asserted. See [Table 19.10 USART Application Settings for USARTn\\_TIMING and USARTn\\_TIMECMPn on page 596](#) for details on how to configure this mode. The TX sequencer could be enabled on PRS and start the TXSEQ counter running for 4 baud times as programmed in TCMPVAL0. Then CS is asserted for 2 baud times before the transmitter begins sending TX data. TXDELAY in USARTn\_TIMING is the initial delay before any CS assertion, and CSSETUP is the delay during CS assertion. There are several small preset timing values such as 1, 2, 3, or 7 that can be used for some of the TX sequencer timing which leaves TCMPVAL0, TCMPVAL1, and TCMPVAL2 free for other uses.

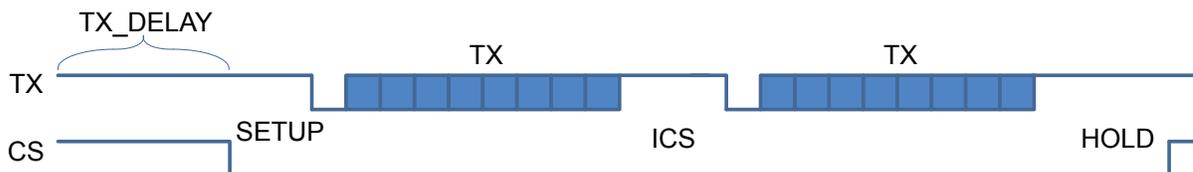


Figure 19.29. USART TXSEQ Timing

### 19.3.10.5 Inter-Character Space

In addition to delaying the start of frame transmission, it is sometimes necessary to also delay the time between each transmit character (inter-character space). After the first transmission, the inter-character space will delay the start of all subsequent transmissions until the transmit buffer is empty. See [Table 19.10 USART Application Settings for USARTn\\_TIMING and USARTn\\_TIMECMPn on page 596](#) for details on setting up this example. For this example in [Figure 19.29 USART TXSEQ Timing on page 599](#) ICS is set to TCMP2 in USARTn\_TIMING. To keep CS asserted during the inter-character space, set AUTOCS in USARTn\_CTRL. There are a few small preset timing values provided for TX sequence timing. Using these preset timing values can free up the TCMPVALn for other uses. For this example, the inter-character space is set to 0x03 and a preset value could be used.

### 19.3.10.6 TX Chip Select End Delay

The assertion of CS can be extended after the final character of the frame by using CSHOLD in USARTn\_TIMING. See [Table 19.10 USART Application Settings for USARTn\\_TIMING and USARTn\\_TIMECMPn on page 596](#) for details on setting up this example. AUTOCS in USARTn\_CTRL needs to be set to extend the CS assertion after the last TX character is transmitted as shown in [Figure 19.29 USART TXSEQ Timing on page 599](#).

### 19.3.10.7 Response Delay

A response delay can be used to hold off the transmitter until a certain number of baud-times after the RX frame. See [Table 19.10 USART Application Settings for USARTn\\_TIMING and USARTn\\_TIMECMPn on page 596](#) for details on setting up this example. TXARX1EN in USARTn\_TRIGCTRL tells the TX sequencer to trigger after RX EOF plus cmp1val baud times.

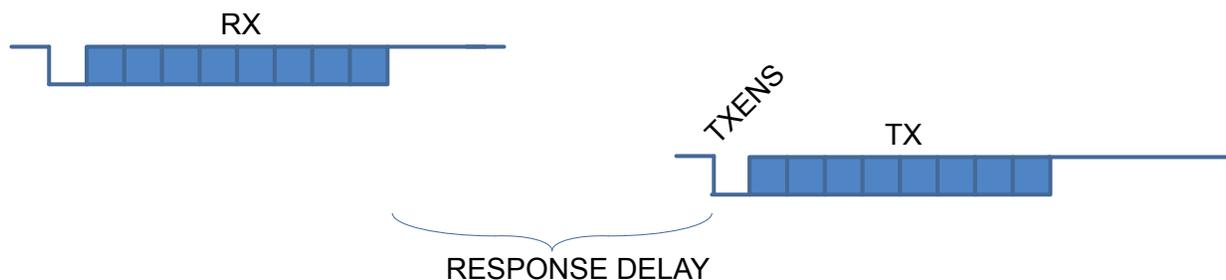


Figure 19.30. USART Response Delay

### 19.3.10.8 Combined TX and RX Example

This example describes how to alternate between TX and RX frames. This has a 28 baud-time space after RX and a 16 baud-time space after TX. The TSTART1 in USARTn\_TIMECMP1 is set to RXEOF which uses the the receiver end of frame to start the timer. The TSTOP1 is set to TCMP1 to generate an event after 28 baud times. Set TXARX1EN in USARTn\_TRIGCTRL, and the transmitter is held off until 28 baud times. TCMPVAL in USARTn\_TIMECMP1 is set to 0x1C for 28 baud times. By setting TSTART0 in USARTn\_TIMECMP0 to TXEOF, the timer will be started after the transmission has completed. RXATX0EN in USARTn\_TRIGCTRL is used to delay enabling of the receiver until 16 baud times after the transmitter has completed. Write 0x10 into TCMPVAL of USARTn\_TIMECMP0 for a 16 baud time delay. CS is also asserted 7 baud-times before start of transmission by setting CSSETUP to 0x7 in USARTn\_TIMING. To keep CS asserted for 3 baud-times after transmission completes, CSHOLD is set to 0x3 in USARTn\_TIMING. See [Table 19.10 USART Application Settings for USARTn\\_TIMING and USARTn\\_TIMECMPn on page 596](#) for details on setting up this example.

### 19.3.10.9 Combined TX Delay and RX Break Detect

This example describes how to delay TX transmission after an RX frame and how to have a break condition signal an interrupt. See [Table 19.10 USART Application Settings for USARTn\\_TIMING and USARTn\\_TIMECMPn on page 596](#) for details on setting up this example. The TX delay is set up by using transmit after RX, TXARX0EN in USARTn\_TRIGCTRL to start the timer. TSTART0 in USARTn\_TIMECMP0 is set to RXEOF which enables the transitter of the timer delay. For this example TCMPVAL in USARTn\_TIMECMP0 is set to 0x20 to create a 32 baud-time delay between the end of the RX frame and the start of the TX frame. The break detect is configured by setting TSTART1 to RXACT to detect the start bit, and setting TSTOP1 to RXACTN to detect RX going high. In this case the interrupt asserts after RX stays low for 12 baud-times, so TCMPVAL1 is set to 0x0C.

### 19.3.10.10 Other Stop Conditions

There is also a timer stop on TX start using the TXST setting in TSTOP of USARTn\_TIMECMPn. This can be used to see that the DMA has not written to the TXBUFFER for a given time.

### 19.3.11 Interrupts

The interrupts generated by the USART are combined into two interrupt vectors. Interrupts related to reception are assigned to one interrupt vector, and interrupts related to transmission are assigned to the other. Separating the interrupts in this way allows different priorities to be set for transmission and reception interrupts.

The transmission interrupt vector groups the transmission-related interrupts generated by the following interrupt flags:

- TXC
- TXBL
- TXOF
- CCF
- TXIDLE

The reception interrupt on the other hand groups the reception-related interrupts, triggered by the following interrupt flags:

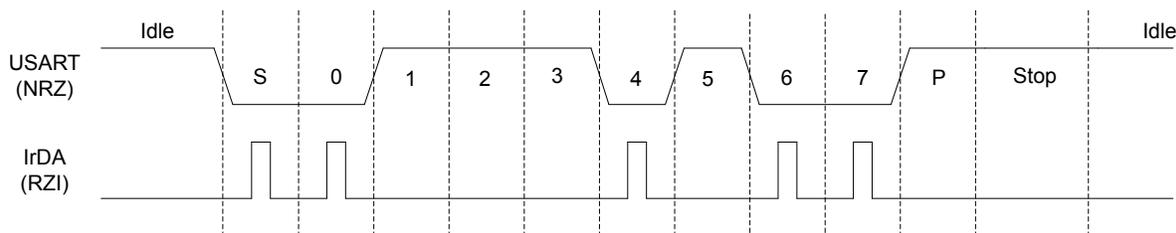
- RXDATAV
- RXFULL
- RXOF
- RXUF
- PERR
- FERR
- MPAF
- SSM
- TCMPn

If USART interrupts are enabled, an interrupt will be made if one or more of the interrupt flags in USART\_IF and their corresponding bits in USART\_IEN are set.

### 19.3.12 IrDA Modulator/ Demodulator

The IrDA modulator implements the physical layer of the IrDA specification, which is necessary for communication over IrDA. The modulator takes the signal output from the USART module, and modulates it before it leaves the USART. In the same way, the input signal is demodulated before it enters the actual USART module. The modulator implements the original Rev. 1.0 physical layer and one high speed extension which supports speeds from 2.4 kbps to 1.152 Mbps.

The data from and to the USART is represented in a NRZ (Non Return to Zero) format, where the signal value is at the same level through the entire bit period. For IrDA, the required format is RZI (Return to Zero Inverted), a format where a “1” is signalled by holding the line low, and a “0” is signalled by a short high pulse. An example is given in [Figure 19.31 USART Example RZI Signal for a given Asynchronous USART Frame on page 601](#).



**Figure 19.31. USART Example RZI Signal for a given Asynchronous USART Frame**

The IrDA module is enabled by setting IREN. The USART transmitter output and receiver input is then routed through the IrDA modulator.

The width of the pulses generated by the IrDA modulator is set by configuring IRPW in USARTn\_IRCTRL. Four pulse widths are available, each defined relative to the configured bit period as listed in [Table 19.11 USART IrDA Pulse Widths on page 601](#).

**Table 19.11. USART IrDA Pulse Widths**

| IRPW | Pulse width OVS=0 | Pulse width OVS=1 | Pulse width OVS=2 | Pulse width OVS=3 |
|------|-------------------|-------------------|-------------------|-------------------|
| 00   | 1/16              | 1/8               | 1/6               | 1/4               |
| 01   | 2/16              | 2/8               | 2/6               | N/A               |
| 10   | 3/16              | 3/8               | N/A               | N/A               |
| 11   | 4/16              | N/A               | N/A               | N/A               |

By default, no filter is enabled in the IrDA demodulator. A filter can be enabled by setting IRFILF in USARTn\_IRCTRL. When the filter is enabled, an incoming pulse has to last for 4 consecutive clock cycles to be detected by the IrDA demodulator.

Note that by default, the idle value of the USART data signal is high. This means that the IrDA modulator generates negative pulses, and the IrDA demodulator expects negative pulses. To make the IrDA module use RZI signalling, both TXINV and RXINV in USARTn\_CTRL must be set.

The IrDA module can also modulate a signal from the PRS system, and transmit a modulated signal to the PRS system. To use a PRS channel as transmitter source instead of the USART, set IRPRSEN in USARTn\_IRCTRL high. The channel is selected by configuring IRPRSSEL in USARTn\_IRCTRL.

## 19.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name              | Type  | Description                                    |
|--------|-------------------|-------|--|
| 0x000  | USARTn_CTRL       | RW    | Control Register                               |
| 0x004  | USARTn_FRAME      | RW    | USART Frame Format Register                    |
| 0x008  | USARTn_TRIGCTRL   | RW    | USART Trigger Control Register                 |
| 0x00C  | USARTn_CMD        | W1    | Command Register                               |
| 0x010  | USARTn_STATUS     | R     | USART Status Register                          |
| 0x014  | USARTn_CLKDIV     | RWH   | Clock Control Register                         |
| 0x018  | USARTn_RXDATAx    | R(a)  | RX Buffer Data Extended Register               |
| 0x01C  | USARTn_RXDATA     | R(a)  | RX Buffer Data Register                        |
| 0x020  | USARTn_RXDOUBLEx  | R(a)  | RX Buffer Double Data Extended Register        |
| 0x024  | USARTn_RXDOUBLE   | R(a)  | RX FIFO Double Data Register                   |
| 0x028  | USARTn_RXDATAxP   | R     | RX Buffer Data Extended Peek Register          |
| 0x02C  | USARTn_RXDOUBLExP | R     | RX Buffer Double Data Extended Peek Register   |
| 0x030  | USARTn_TXDATAx    | W     | TX Buffer Data Extended Register               |
| 0x034  | USARTn_TXDATA     | W     | TX Buffer Data Register                        |
| 0x038  | USARTn_TXDOUBLEx  | W     | TX Buffer Double Data Extended Register        |
| 0x03C  | USARTn_TXDOUBLE   | W     | TX Buffer Double Data Register                 |
| 0x040  | USARTn_IF         | R     | Interrupt Flag Register                        |
| 0x044  | USARTn_IFS        | W1    | Interrupt Flag Set Register                    |
| 0x048  | USARTn_IFC        | (R)W1 | Interrupt Flag Clear Register                  |
| 0x04C  | USARTn_IEN        | RW    | Interrupt Enable Register                      |
| 0x050  | USARTn_IRCTRL     | RW    | IrDA Control Register                          |
| 0x058  | USARTn_INPUT      | RW    | USART Input Register                           |
| 0x05C  | USARTn_I2SCTRL    | RW    | I2S Control Register                           |
| 0x060  | USARTn_TIMING     | RW    | Timing Register                                |
| 0x064  | USARTn_CTRLx      | RW    | Control Register Extended                      |
| 0x068  | USARTn_TIMECMP0   | RW    | Used to Generate Interrupts and Various Delays |
| 0x06C  | USARTn_TIMECMP1   | RW    | Used to Generate Interrupts and Various Delays |
| 0x070  | USARTn_TIMECMP2   | RW    | Used to Generate Interrupts and Various Delays |
| 0x074  | USARTn_ROUTEPEEN  | RW    | I/O Routing Pin Enable Register                |
| 0x078  | USARTn_ROUTELOC0  | RW    | I/O Routing Location Register                  |
| 0x07C  | USARTn_ROUTELOC1  | RW    | I/O Routing Location Register                  |

## 19.5 Register Description

## 19.5.1 USARTn\_CTRL - Control Register

| Offset | Bit Position |       |        |          |    |    |          |        |        |         |        |           |           |        |         |        |       |       |       |       |      |      |        |        |   |     |   |      |     |      |        |      |    |
|--------|--------------|-------|--------|----------|----|----|----------|--------|--------|---------|--------|-----------|-----------|--------|---------|--------|-------|-------|-------|-------|------|------|--------|--------|---|-----|---|------|-----|------|--------|------|----|
| 0x000  | 31           | 30    | 29     | 28       | 27 | 26 | 25       | 24     | 23     | 22      | 21     | 20        | 19        | 18     | 17      | 16     | 15    | 14    | 13    | 12    | 11   | 10   | 9      | 8      | 7 | 6   | 5 | 4    | 3   | 2    | 1      | 0    |    |
| Reset  | 0            | 0     | 0      | 0        |    |    | 0        | 0      | 0      | 0       | 0      | 0         | 0         | 0      | 0       | 0      | 0     | 0     | 0     | 0     | 0    | 0    | 0      | 0      |   | 0x0 |   | 0    | 0   | 0    | 0      | 0    | 0  |
| Access | RW           | RW    | RW     | RW       |    |    | RW       | RW     | RW     | RW      | RW     | RW        | RW        | RW     | RW      | RW     | RW    | RW    | RW    | RW    | RW   | RW   | RW     | RW     |   | RW  |   | RW   | RW  | RW   | RW     | RW   | RW |
| Name   | SMSDELAY     | MVDIS | AUTOTX | BYTESWAP |    |    | SSSEARLY | ERRSTX | ERRSRX | ERRSDMA | BIT8DV | SKIPPERRF | SCRETRANS | SCMODE | AUTOTRI | AUTOCS | CSINV | TXINV | RXINV | TXBIL | CSMA | MSBF | CLKPHA | CLKPOL |   | OVS |   | MPAB | MPM | CCEN | LOOPBK | SYNC |    |

| Bit   | Name            | Reset | Access | Description   |
|-------|-----------------|-------|--------|---|
| 31    | SMSDELAY        | 0     | RW     | <b>Synchronous Master Sample Delay</b><br>Delay Synchronous Master sample point to the next setup edge to improve timing and allow communication at higher speeds |
| 30    | MVDIS           | 0     | RW     | <b>Majority Vote Disable</b><br>Disable majority vote for 16x, 8x and 6x oversampling modes.  |
| 29    | AUTOTX          | 0     | RW     | <b>Always Transmit When RX Not Full</b><br>Transmits as long as RX is not full. If TX is empty, underflows are generated.   |
| 28    | BYTESWAP        | 0     | RW     | <b>Byteswap in Double Accesses</b><br>Set to switch the order of the bytes in double accesses.  |
|       | Value           |       |        | Description   |
|       | 0               |       |        | Normal byte order   |
|       | 1               |       |        | Byte order swapped  |
| 27:26 | <i>Reserved</i> |       |        | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i>                                   |
| 25    | SSSEARLY        | 0     | RW     | <b>Synchronous Slave Setup Early</b><br>Setup data on sample edge in synchronous slave mode to improve MOSI setup time  |
| 24    | ERRSTX          | 0     | RW     | <b>Disable TX on Error</b><br>When set, the transmitter is disabled on framing and parity errors (asynchronous mode only) in the receiver.                        |
|       | Value           |       |        | Description   |
|       | 0               |       |        | Received framing and parity errors have no effect on transmitter  |
|       | 1               |       |        | Received framing and parity errors disable the transmitter  |
| 23    | ERRSRX          | 0     | RW     | <b>Disable RX on Error</b><br>When set, the receiver is disabled on framing and parity errors (asynchronous mode only).   |
|       | Value           |       |        | Description   |
|       | 0               |       |        | Framing and parity errors have no effect on receiver  |

| Bit | Name      | Reset | Access | Description   |
|-----|-----------|-------|--------|---|
|     | 1         |       |        | Framing and parity errors disable the receiver  |
| 22  | ERRSDMA   | 0     | RW     | <b>Halt DMA on Error</b><br>When set, DMA requests will be cleared on framing and parity errors (asynchronous mode only).   |
|     | Value     |       |        | Description   |
|     | 0         |       |        | Framing and parity errors have no effect on DMA requests from the USART   |
|     | 1         |       |        | DMA requests from the USART are blocked while the PERR or FERR interrupt flags are set  |
| 21  | BIT8DV    | 0     | RW     | <b>Bit 8 Default Value</b><br>The default value of the 9th bit. If 9-bit frames are used, and an 8-bit write operation is done, leaving the 9th bit unspecified, the 9th bit is set to the value of BIT8DV. |
| 20  | SKIPPERRF | 0     | RW     | <b>Skip Parity Error Frames</b><br>When set, the receiver discards frames with parity errors (asynchronous mode only). The PERR interrupt flag is still set.  |
| 19  | SCRETRANS | 0     | RW     | <b>SmartCard Retransmit</b><br>When in SmartCard mode, a NACK'ed frame will be kept in the shift register and retransmitted if the transmitter is still enabled.  |
| 18  | SCMODE    | 0     | RW     | <b>SmartCard Mode</b><br>Use this bit to enable or disable SmartCard mode.  |
| 17  | AUTOTRI   | 0     | RW     | <b>Automatic TX Tristate</b><br>When enabled, TXTRI is set by hardware whenever the transmitter is idle, and TXTRI is cleared by hardware when transmission starts.   |
|     | Value     |       |        | Description   |
|     | 0         |       |        | The output on U(S)n_TX when the transmitter is idle is defined by TXINV   |
|     | 1         |       |        | U(S)n_TX is tristated whenever the transmitter is idle  |
| 16  | AUTOCS    | 0     | RW     | <b>Automatic Chip Select</b><br>When enabled, the output on USn_CS will be activated one baud-period before transmission starts, and deactivated when transmission ends.                                    |
| 15  | CSINV     | 0     | RW     | <b>Chip Select Invert</b><br>Default value is active low. This affects both the selection of external slaves, as well as the selection of the microcontroller as a slave.                                   |
|     | Value     |       |        | Description   |
|     | 0         |       |        | Chip select is active low   |
|     | 1         |       |        | Chip select is active high  |
| 14  | TXINV     | 0     | RW     | <b>Transmitter Output Invert</b><br>The output from the USART transmitter can optionally be inverted by setting this bit.   |
|     | Value     |       |        | Description   |
|     | 0         |       |        | Output from the transmitter is passed unchanged to U(S)n_TX   |

| Bit | Name   | Reset          | Access | Description  |
|-----|--------|----------------|--------|--|
|     | 1      |                |        | Output from the transmitter is inverted before it is passed to U(S)n_TX  |
| 13  | RXINV  | 0              | RW     | <b>Receiver Input Invert</b><br>Setting this bit will invert the input to the USART receiver.  |
|     | Value  |                |        | Description  |
|     | 0      |                |        | Input is passed directly to the receiver   |
|     | 1      |                |        | Input is inverted before it is passed to the receiver  |
| 12  | TXBIL  | 0              | RW     | <b>TX Buffer Interrupt Level</b><br>Determines the interrupt and status level of the transmit buffer.  |
|     | Value  | Mode           |        | Description  |
|     | 0      | EMPTY          |        | TXBL and the TXBL interrupt flag are set when the transmit buffer becomes empty. TXBL is cleared when the buffer becomes nonempty.   |
|     | 1      | HALFFULL       |        | TXBL and TXBLIF are set when the transmit buffer goes from full to half-full or empty. TXBL is cleared when the buffer becomes full.   |
| 11  | CSMA   | 0              | RW     | <b>Action on Slave-Select in Master Mode</b><br>This register determines the action to be performed when slave-select is configured as an input and driven low while in master mode. |
|     | Value  | Mode           |        | Description  |
|     | 0      | NOACTION       |        | No action taken  |
|     | 1      | GOTOSLAVEMODE  |        | Go to slave mode   |
| 10  | MSBF   | 0              | RW     | <b>Most Significant Bit First</b><br>Decides whether data is sent with the least significant bit first, or the most significant bit first.   |
|     | Value  |                |        | Description  |
|     | 0      |                |        | Data is sent with the least significant bit first  |
|     | 1      |                |        | Data is sent with the most significant bit first   |
| 9   | CLKPHA | 0              | RW     | <b>Clock Edge for Setup/Sample</b><br>Determines where data is set-up and sampled according to the bus clock when in synchronous mode.   |
|     | Value  | Mode           |        | Description  |
|     | 0      | SAMPLELEADING  |        | Data is sampled on the leading edge and set-up on the trailing edge of the bus clock in synchronous mode   |
|     | 1      | SAMPLETRAILING |        | Data is set-up on the leading edge and sampled on the trailing edge of the bus clock in synchronous mode   |
| 8   | CLKPOL | 0              | RW     | <b>Clock Polarity</b><br>Determines the clock polarity of the bus clock used in synchronous mode.  |
|     | Value  | Mode           |        | Description  |
|     | 0      | IDLELOW        |        | The bus clock used in synchronous mode has a low base value  |

| Bit | Name            | Reset  | Access   | Description   |
|-----|-----------------|--|--|---|
|     | 1               | IDLEHIGH   |  | The bus clock used in synchronous mode has a high base value  |
| 7   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i>                                    |  |   |
| 6:5 | OVS             | 0x0  | RW   | <b>Oversampling</b><br>Sets the number of clock periods in a UART bit-period. More clock cycles gives better robustness, while less clock cycles gives better performance.  |
|     | Value           | Mode   | Description  |   |
|     | 0               | X16  | Regular UART mode with 16X oversampling in asynchronous mode |   |
|     | 1               | X8   | Double speed with 8X oversampling in asynchronous mode       |   |
|     | 2               | X6   | 6X oversampling in asynchronous mode                         |   |
|     | 3               | X4   | Quadruple speed with 4X oversampling in asynchronous mode    |   |
| 4   | MPAB            | 0  | RW   | <b>Multi-Processor Address-Bit</b><br>Defines the value of the multi-processor address bit. An incoming frame with its 9th bit equal to the value of this bit marks the frame as a multi-processor address frame. |
| 3   | MPM             | 0  | RW   | <b>Multi-Processor Mode</b><br>Multi-processor mode uses the 9th bit of the USART frames to tell whether the frame is an address frame or a data frame.   |
|     | Value           | Description  |  |   |
|     | 0               | The 9th bit of incoming frames has no special function   |  |   |
|     | 1               | An incoming frame with the 9th bit equal to MPAB will be loaded into the receive buffer regardless of RXBLOCK and will result in the MPAB interrupt flag being set |  |   |
| 2   | CCEN            | 0  | RW   | <b>Collision Check Enable</b><br>Enables collision checking on data when operating in half duplex modus.  |
|     | Value           | Description  |  |   |
|     | 0               | Collision check is disabled  |  |   |
|     | 1               | Collision check is enabled. The receiver must be enabled for the check to be performed   |  |   |
| 1   | LOOPBK          | 0  | RW   | <b>Loopback Enable</b><br>Allows the receiver to be connected directly to the USART transmitter for loopback and half duplex communication.   |
|     | Value           | Description  |  |   |
|     | 0               | The receiver is connected to and receives data from U(S)n_RX   |  |   |
|     | 1               | The receiver is connected to and receives data from U(S)n_TX   |  |   |
| 0   | SYNC            | 0  | RW   | <b>USART Synchronous Mode</b><br>Determines whether the USART is operating in asynchronous or synchronous mode.   |
|     | Value           | Description  |  |   |
|     | 0               | The USART operates in asynchronous mode  |  |   |

---

| Bit | Name | Reset | Access | Description                            |
|-----|------|-------|--------|--|
| 1   |      |       |        | The USART operates in synchronous mode |

---

## 19.5.2 USARTn\_FRAME - USART Frame Format Register

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |          |    |    |    |        |    |    |    |    |    |          |   |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|--------|----|----|----|----|----|----------|---|---|---|---|---|---|---|---|---|
| 0x004  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19       | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9        | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset  |              |    |    |    |    |    |    |    |    |    |    |    | 0x1      |    |    |    | 0x0    |    |    |    |    |    | 0x5      |   |   |   |   |   |   |   |   |   |
| Access |              |    |    |    |    |    |    |    |    |    |    |    | RW       |    |    |    | RW     |    |    |    |    |    | RW       |   |   |   |   |   |   |   |   |   |
| Name   |              |    |    |    |    |    |    |    |    |    |    |    | STOPBITS |    |    |    | PARITY |    |    |    |    |    | DATABITS |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset   | Access  | Description   |
|-------|----------|---|---|---|
| 31:14 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |
| 13:12 | STOPBITS | 0x1   | RW  | <b>Stop-Bit Mode</b><br>Determines the number of stop-bits used.  |
|       | Value    | Mode  | Description   |   |
|       | 0        | HALF  | The transmitter generates a half stop bit. Stop-bits are not verified by receiver           |   |
|       | 1        | ONE   | One stop bit is generated and verified  |   |
|       | 2        | ONEANDAHALF   | The transmitter generates one and a half stop bit. The receiver verifies the first stop bit |   |
|       | 3        | TWO   | The transmitter generates two stop bits. The receiver checks the first stop-bit only        |   |
| 11:10 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |
| 9:8   | PARITY   | 0x0   | RW  | <b>Parity-Bit Mode</b><br>Determines whether parity bits are enabled, and whether even or odd parity should be used. Only available in asynchronous mode. |
|       | Value    | Mode  | Description   |   |
|       | 0        | NONE  | Parity bits are not used  |   |
|       | 2        | EVEN  | Even parity are used. Parity bits are automatically generated and checked by hardware.      |   |
|       | 3        | ODD   | Odd parity is used. Parity bits are automatically generated and checked by hardware.        |   |
| 7:4   | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |
| 3:0   | DATABITS | 0x5   | RW  | <b>Data-Bit Mode</b><br>This register sets the number of data bits in a USART frame.  |
|       | Value    | Mode  | Description   |   |
|       | 1        | FOUR  | Each frame contains 4 data bits   |   |
|       | 2        | FIVE  | Each frame contains 5 data bits   |   |

| Bit | Name | Reset    | Access | Description                      |
|-----|------|----------|--------|----------------------------------|
| 3   |      | SIX      |        | Each frame contains 6 data bits  |
| 4   |      | SEVEN    |        | Each frame contains 7 data bits  |
| 5   |      | EIGHT    |        | Each frame contains 8 data bits  |
| 6   |      | NINE     |        | Each frame contains 9 data bits  |
| 7   |      | TEN      |        | Each frame contains 10 data bits |
| 8   |      | ELEVEN   |        | Each frame contains 11 data bits |
| 9   |      | TWELVE   |        | Each frame contains 12 data bits |
| 10  |      | THIRTEEN |        | Each frame contains 13 data bits |
| 11  |      | FOURTEEN |        | Each frame contains 14 data bits |
| 12  |      | FIFTEEN  |        | Each frame contains 15 data bits |
| 13  |      | SIXTEEN  |        | Each frame contains 16 data bits |



| Bit | Name            | Reset   | Access | Description  |
|-----|-----------------|---|--------|--|
| 9   | TXARX2EN        | 0   | RW     | <b>Enable Transmit Trigger After RX End of Frame Plus TCMP2VAL</b><br>When set, an RX end of frame will trigger the transmitter after TCMP2VAL bit times to force a minimum response delay |
| 8   | TXARX1EN        | 0   | RW     | <b>Enable Transmit Trigger After RX End of Frame Plus TCMP1VAL</b><br>When set, an RX end of frame will trigger the transmitter after TCMP1VAL bit times to force a minimum response delay |
| 7   | TXARX0EN        | 0   | RW     | <b>Enable Transmit Trigger After RX End of Frame Plus TCMP0VAL</b><br>When set, an RX end of frame will trigger the transmitter after TCMP0VAL bit times to force a minimum response delay |
| 6   | AUTOTXTEN       | 0   | RW     | <b>AUTOTX Trigger Enable</b><br>When set, AUTOTX is enabled as long as the PRS channel selected by TSEL has a high value   |
| 5   | TXTEN           | 0   | RW     | <b>Transmit Trigger Enable</b><br>When set, the PRS channel selected by TSEL sets TXEN, enabling the transmitter on positive trigger edges.  |
| 4   | RXTEN           | 0   | RW     | <b>Receive Trigger Enable</b><br>When set, the PRS channel selected by TSEL sets RXEN, enabling the receiver on positive trigger edges.  |
| 3:0 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |

## 19.5.4 USARTn\_CMD - Command Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |         |          |         |            |           |           |          |       |      |       |      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|---------|----------|---------|------------|-----------|-----------|----------|-------|------|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0x00C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11      | 10      | 9        | 8       | 7          | 6         | 5         | 4        | 3     | 2    | 1     | 0    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       | 0       | 0        | 0       | 0          | 0         | 0         | 0        | 0     | 0    | 0     | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |    |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W1      | W1      | W1       | W1      | W1         | W1        | W1        | W1       | W1    | W1   | W1    | W1   | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CLEARRX | CLEARTX | TXTRIDIS | TXTRIEN | RXBLOCKDIS | RXBLOCKEN | MASTERDIS | MASTEREN | TXDIS | TXEN | RXDIS | RXEN |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

| Bit   | Name       | Reset   | Access | Description  |
|-------|------------|---|--------|--|
| 31:12 | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 11    | CLEARRX    | 0   | W1     | <b>Clear RX</b><br>Set to clear receive buffer and the RX shift register.  |
| 10    | CLEARTX    | 0   | W1     | <b>Clear TX</b><br>Set to clear transmit buffer and the TX shift register.   |
| 9     | TXTRIDIS   | 0   | W1     | <b>Transmitter Tristate Disable</b><br>Disables tristating of the transmitter output.  |
| 8     | TXTRIEN    | 0   | W1     | <b>Transmitter Tristate Enable</b><br>Tristates the transmitter output.  |
| 7     | RXBLOCKDIS | 0   | W1     | <b>Receiver Block Disable</b><br>Set to clear RXBLOCK, resulting in all incoming frames being loaded into the receive buffer.  |
| 6     | RXBLOCKEN  | 0   | W1     | <b>Receiver Block Enable</b><br>Set to set RXBLOCK, resulting in all incoming frames being discarded.  |
| 5     | MASTERDIS  | 0   | W1     | <b>Master Disable</b><br>Set to disable master mode, clearing the MASTER status bit and putting the USART in slave mode.   |
| 4     | MASTEREN   | 0   | W1     | <b>Master Enable</b><br>Set to enable master mode, setting the MASTER status bit. Master mode should not be enabled while TXENS is set to 1. To enable both master and TX mode, write MASTEREN before TXEN, or enable them both in the same write operation. |
| 3     | TXDIS      | 0   | W1     | <b>Transmitter Disable</b><br>Set to disable transmission.   |
| 2     | TXEN       | 0   | W1     | <b>Transmitter Enable</b><br>Set to enable data transmission.  |
| 1     | RXDIS      | 0   | W1     | <b>Receiver Disable</b><br>Set to disable data reception. If a frame is under reception when the receiver is disabled, the incoming frame is discarded.  |
| 0     | RXEN       | 0   | W1     | <b>Receiver Enable</b><br>Set to activate data reception on U(S)n_RX.  |

## 19.5.5 USARTn\_STATUS - USART Status Register

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |          |    |                |        |             |              |           |           |        |         |      |     |       |         |        |       |       |   |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|----|----------------|--------|-------------|--------------|-----------|-----------|--------|---------|------|-----|-------|---------|--------|-------|-------|---|---|
| 0x010  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17       | 16 | 15             | 14     | 13          | 12           | 11        | 10        | 9      | 8       | 7    | 6   | 5     | 4       | 3      | 2     | 1     | 0 |   |
| Reset  |              |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0      |    | 0              | 1      | 0           | 0            | 0         | 0         | 0      | 0       | 0    | 1   | 0     | 0       | 0      | 0     | 0     | 0 | 0 |
| Access |              |    |    |    |    |    |    |    |    |    |    |    |    |    | R        |    | R              | R      | R           | R            | R         | R         | R      | R       | R    | R   | R     | R       | R      | R     | R     | R | R |
| Name   |              |    |    |    |    |    |    |    |    |    |    |    |    |    | TXBUFCNT |    | TIMERRESTARTED | TXIDLE | RXFULLRIGHT | RXDATAVRIGHT | TXBSRIGHT | TXBDRIGHT | RXFULL | RXDATAV | TXBL | TXC | TXTRI | RXBLOCK | MASTER | TXENS | RXENS |   |   |

| Bit   | Name           | Reset | Access | Description   |
|-------|----------------|-------|--------|---|
| 31:18 | Reserved       |       |        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a>  |
| 17:16 | TXBUFCNT       | 0x0   | R      | <b>TX Buffer Count</b><br>Count of TX buffer entry 0, entry 1, and TX shift register. For large frames, the count is only of TX buffer entry 0 and the TX shifter register.   |
| 15    | Reserved       |       |        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a>  |
| 14    | TIMERRESTARTED | 0     | R      | <b>The USART Timer Restarted Itself</b><br>When the timer is restarting itself on each TCMP event, a TIMERRESTARTED value of 0x0 indicates the first TCMP event in the sequence of multiple TCMP events. Any non TCMP timer start events will clear TIMERRESTARTED. When there is a TCMP interrupt and TIMERRESTARTED is 0x0, an interrupt service routine can set a TCMP event counter variable in memory to 0x1 to indicate the first TCMP interrupt of the sequence. |
| 13    | TXIDLE         | 1     | R      | <b>TX Idle</b><br>Set when TX idle  |
| 12    | RXFULLRIGHT    | 0     | R      | <b>RX Full of Right Data</b><br>When set, the entire RX buffer contains right data. Only used in I2S mode   |
| 11    | RXDATAVRIGHT   | 0     | R      | <b>RX Data Right</b><br>When set, reading RXDATA or RXDATAx gives right data. Else left data is read. Only used in I2S mode   |
| 10    | TXBSRIGHT      | 0     | R      | <b>TX Buffer Expects Single Right Data</b><br>When set, the TX buffer expects at least a single right data. Else it expects left data. Only used in I2S mode  |
| 9     | TXBDRIGHT      | 0     | R      | <b>TX Buffer Expects Double Right Data</b><br>When set, the TX buffer expects double right data. Else it may expect a single right data or left data. Only used in I2S mode   |
| 8     | RXFULL         | 0     | R      | <b>RX FIFO Full</b><br>Set when the RXFIFO is full. Cleared when the receive buffer is no longer full. When this bit is set, there is still room for one more frame in the receive shift register.  |
| 7     | RXDATAV        | 0     | R      | <b>RX Data Valid</b><br>Set when data is available in the receive buffer. Cleared when the receive buffer is empty.   |
| 6     | TXBL           | 1     | R      | <b>TX Buffer Level</b><br>Indicates the level of the transmit buffer. If TXBIL is 0x0, TXBL is set whenever the transmit buffer is completely empty. Otherwise TXBL is set whenever the TX Buffer becomes half full.  |



## 19.5.7 USARTn\_RXDATAx - RX Buffer Data Extended Register (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |      |      |    |    |    |    |   |   |   |   |   |   |        |   |   |   |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------|------|----|----|----|----|---|---|---|---|---|---|--------|---|---|---|--|--|
| 0x018         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15   | 14   | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3      | 2 | 1 | 0 |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0    | 0    |    |    |    |    |   |   |   |   |   |   | 0x000  |   |   |   |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R    | R    |    |    |    |    |   |   |   |   |   |   | R      |   |   |   |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | FERR | PERR |    |    |    |    |   |   |   |   |   |   | RXDATA |   |   |   |  |  |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:16 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 15    | FERR            | 0   | R      | <b>Data Framing Error</b><br>Set if data in buffer has a framing error. Can be the result of a break condition. |
| 14    | PERR            | 0   | R      | <b>Data Parity Error</b><br>Set if data in buffer has a parity error (asynchronous mode only).                  |
| 13:9  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 8:0   | RXDATA          | 0x000   | R      | <b>RX Data</b><br>Use this register to access data read from the USART. Buffer is cleared on read access.       |

## 19.5.8 USARTn\_RXDATA - RX Buffer Data Register (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |        |  |  |  |  |  |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--------|--|--|--|--|--|--|--|
| 0x01C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |        |  |  |  |  |  |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0x00   |  |  |  |  |  |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | R      |  |  |  |  |  |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | RXDATA |  |  |  |  |  |  |  |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 31:8 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 7:0  | RXDATA          | 0x00  | R      | <b>RX Data</b><br>Use this register to access data read from USART. Buffer is cleared on read access. Only the 8 LSB can be read using this register. |

## 19.5.9 USARTn\_RXDOUBLEX - RX Buffer Double Data Extended Register (Actionable Reads)

| Offset        | Bit Position |       |    |    |    |    |    |    |    |    |    |         |    |    |    |    |       |       |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |         |
|---------------|--------------|-------|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|-------|-------|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|---------|
| 0x020         | 31           | 30    | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20      | 19 | 18 | 17 | 16 | 15    | 14    | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |         |
| <b>Reset</b>  | 0            | 0     |    |    |    |    |    |    |    |    |    | 0x000   |    |    |    |    | 0     | 0     |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  | 0x000   |
| <b>Access</b> | R            | R     |    |    |    |    |    |    |    |    |    | R       |    |    |    |    | R     | R     |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  | R       |
| <b>Name</b>   | FERR1        | PERR1 |    |    |    |    |    |    |    |    |    | RXDATA1 |    |    |    |    | FERR0 | PERR0 |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  | RXDATA0 |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31    | FERR1           | 0   | R      | <b>Data Framing Error 1</b><br>Set if data in buffer has a framing error. Can be the result of a break condition. |
| 30    | PERR1           | 0   | R      | <b>Data Parity Error 1</b><br>Set if data in buffer has a parity error (asynchronous mode only).                  |
| 29:25 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 24:16 | RXDATA1         | 0x000   | R      | <b>RX Data 1</b><br>Second frame read from buffer.  |
| 15    | FERR0           | 0   | R      | <b>Data Framing Error 0</b><br>Set if data in buffer has a framing error. Can be the result of a break condition. |
| 14    | PERR0           | 0   | R      | <b>Data Parity Error 0</b><br>Set if data in buffer has a parity error (asynchronous mode only).                  |
| 13:9  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 8:0   | RXDATA0         | 0x000   | R      | <b>RX Data 0</b><br>First frame read from buffer.   |

## 19.5.10 USARTn\_RXDOUBLE - RX FIFO Double Data Register (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |   |   |         |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---------|---|---|---|---|---|---|---|
| 0x024         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00    |    |    |    |    |    |   |   | 0x00    |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R       |    |    |    |    |    |   |   | R       |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RXDATA1 |    |    |    |    |    |   |   | RXDATA0 |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description  |
|-------|----------|--|--------|--|
| 31:16 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 15:8  | RXDATA1  | 0x00   | R      | <b>RX Data 1</b><br>Second frame read from buffer. |
| 7:0   | RXDATA0  | 0x00   | R      | <b>RX Data 0</b><br>First frame read from buffer.  |

## 19.5.11 USARTn\_RXDATAEXP - RX Buffer Data Extended Peek Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |       |       |    |    |    |    |   |   |   |   |         |   |   |   |   |   |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|-------|----|----|----|----|---|---|---|---|---------|---|---|---|---|---|--|--|
| 0x028         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15    | 14    | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5       | 4 | 3 | 2 | 1 | 0 |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0     | 0     |    |    |    |    |   |   |   |   | 0x000   |   |   |   |   |   |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R     | R     |    |    |    |    |   |   |   |   | R       |   |   |   |   |   |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | FERRP | PERRP |    |    |    |    |   |   |   |   | RXDATAP |   |   |   |   |   |  |  |

| Bit   | Name     | Reset  | Access | Description  |
|-------|----------|--|--------|--|
| 31:16 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 15    | FERRP    | 0  | R      | <b>Data Framing Error Peek</b><br>Set if data in buffer has a framing error. Can be the result of a break condition. |
| 14    | PERRP    | 0  | R      | <b>Data Parity Error Peek</b><br>Set if data in buffer has a parity error (asynchronous mode only).                  |
| 13:9  | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 8:0   | RXDATAP  | 0x000  | R      | <b>RX Data Peek</b><br>Use this register to access data read from the USART.   |

## 19.5.12 USARTn\_RXDOUBLEXP - RX Buffer Double Data Extended Peek Register

| Offset        | Bit Position |        |    |    |    |    |    |    |    |    |    |          |    |    |    |    |        |        |    |    |    |    |   |   |   |   |   |   |   |   |   |          |       |
|---------------|--------------|--------|----|----|----|----|----|----|----|----|----|----------|----|----|----|----|--------|--------|----|----|----|----|---|---|---|---|---|---|---|---|---|----------|-------|
| 0x02C         | 31           | 30     | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20       | 19 | 18 | 17 | 16 | 15     | 14     | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0        |       |
| <b>Reset</b>  | 0            | 0      |    |    |    |    |    |    |    |    |    | 0x000    |    |    |    |    | 0      | 0      |    |    |    |    |   |   |   |   |   |   |   |   |   |          | 0x000 |
| <b>Access</b> | R            | R      |    |    |    |    |    |    |    |    |    | R        |    |    |    |    | R      | R      |    |    |    |    |   |   |   |   |   |   |   |   |   | R        |       |
| <b>Name</b>   | FERRP1       | PERRP1 |    |    |    |    |    |    |    |    |    | RXDATAP1 |    |    |    |    | FERRP0 | PERRP0 |    |    |    |    |   |   |   |   |   |   |   |   |   | RXDATAP0 |       |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 31    | FERRP1          | 0   | R      | <b>Data Framing Error 1 Peek</b><br>Set if data in buffer has a framing error. Can be the result of a break condition. |
| 30    | PERRP1          | 0   | R      | <b>Data Parity Error 1 Peek</b><br>Set if data in buffer has a parity error (asynchronous mode only).                  |
| 29:25 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 24:16 | RXDATAP1        | 0x000   | R      | <b>RX Data 1 Peek</b><br>Second frame read from FIFO.  |
| 15    | FERRP0          | 0   | R      | <b>Data Framing Error 0 Peek</b><br>Set if data in buffer has a framing error. Can be the result of a break condition. |
| 14    | PERRP0          | 0   | R      | <b>Data Parity Error 0 Peek</b><br>Set if data in buffer has a parity error (asynchronous mode only).                  |
| 13:9  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 8:0   | RXDATAP0        | 0x000   | R      | <b>RX Data 0 Peek</b><br>First frame read from FIFO.   |

## 19.5.13 USARTn\_TXDATAx - TX Buffer Data Extended Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |         |         |         |        |    |   |   |   |   |   |   |   |   |   |   |  |         |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|---------|---------|---------|--------|----|---|---|---|---|---|---|---|---|---|---|--|---------|
| 0x030         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14      | 13      | 12      | 11     | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |         |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0      | 0       | 0       | 0       | 0      |    |   |   |   |   |   |   |   |   |   |   |  |         |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W      | W       | W       | W       | W      |    |   |   |   |   |   |   |   |   |   |   |  |         |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RXENAT | TXDISAT | TXBREAK | TXTRIAT | UBRXAT |    |   |   |   |   |   |   |   |   |   |   |  | TXDATAx |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:16 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 15    | RXENAT          | 0   | W      | <b>Enable RX After Transmission</b><br>Set to enable reception after transmission.  |
| 14    | TXDISAT         | 0   | W      | <b>Clear TXEN After Transmission</b><br>Set to disable transmitter and release data bus directly after transmission.  |
| 13    | TXBREAK         | 0   | W      | <b>Transmit Data as Break</b><br>Set to send data as a break. Recipient will see a framing error or a break condition depending on its configuration and the value of TXDATA. |
| 12    | TXTRIAT         | 0   | W      | <b>Set TXTRI After Transmission</b><br>Set to tristate transmitter by setting TXTRI after transmission.   |
| 11    | UBRXAT          | 0   | W      | <b>Unblock RX After Transmission</b><br>Set to clear RXBLOCK after transmission, unblocking the receiver.   |
| 10:9  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 8:0   | TXDATAx         | 0x000   | W      | <b>TX Data</b><br>Use this register to write data to the USART. If TXEN is set, a transfer will be initiated at the first opportunity.  |

**19.5.14 USARTn\_TXDATA - TX Buffer Data Register**

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |        |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|--------|---|---|---|---|---|---|---|
| 0x034         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x00   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | W      |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | TXDATA |   |   |   |   |   |   |   |

| Bit   | Name            | Reset   | Access | Description    |
|---|-----------------|---|--------|----------------|
| 31:8  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |                |
| 7:0   | TXDATA          | 0x00  | W      | <b>TX Data</b> |
| This frame will be added to TX buffer. Only 8 LSB can be written using this register. 9th bit and control bits will be cleared. |                 |   |        |                |

## 19.5.15 USARTn\_TXDOUBLEX - TX Buffer Double Data Extended Register

| Offset        | Bit Position |          |          |          |         |    |    |    |    |    |    |         |    |    |    |    |         |          |          |          |         |    |   |   |   |   |   |   |   |   |   |         |       |
|---------------|--------------|----------|----------|----------|---------|----|----|----|----|----|----|---------|----|----|----|----|---------|----------|----------|----------|---------|----|---|---|---|---|---|---|---|---|---|---------|-------|
| 0x038         | 31           | 30       | 29       | 28       | 27      | 26 | 25 | 24 | 23 | 22 | 21 | 20      | 19 | 18 | 17 | 16 | 15      | 14       | 13       | 12       | 11      | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0       |       |
| <b>Reset</b>  | 0            | 0        | 0        | 0        | 0       |    |    |    |    |    |    | 0x000   |    |    |    |    | 0       | 0        | 0        | 0        | 0       |    |   |   |   |   |   |   |   |   |   |         | 0x000 |
| <b>Access</b> | W            | W        | W        | W        | W       |    |    |    |    |    |    | W       |    |    |    |    | W       | W        | W        | W        | W       |    |   |   |   |   |   |   |   |   |   | W       |       |
| <b>Name</b>   | RXENAT1      | TXDISAT1 | TXBREAK1 | TXTRIAT1 | UBRXAT1 |    |    |    |    |    |    | TXDATA1 |    |    |    |    | RXENAT0 | TXDISAT0 | TXBREAK0 | TXTRIAT0 | UBRXAT0 |    |   |   |   |   |   |   |   |   |   | TXDATA0 |       |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 31    | RXENAT1         | 0   | W      | <b>Enable RX After Transmission</b><br>Set to enable reception after transmission.   |
| 30    | TXDISAT1        | 0   | W      | <b>Clear TXEN After Transmission</b><br>Set to disable transmitter and release data bus directly after transmission.   |
| 29    | TXBREAK1        | 0   | W      | <b>Transmit Data as Break</b><br>Set to send data as a break. Recipient will see a framing error or a break condition depending on its configuration and the value of USARTn_TXDATA. |
| 28    | TXTRIAT1        | 0   | W      | <b>Set TXTRI After Transmission</b><br>Set to tristate transmitter by setting TXTRI after transmission.  |
| 27    | UBRXAT1         | 0   | W      | <b>Unblock RX After Transmission</b><br>Set clear RXBLOCK after transmission, unblocking the receiver.   |
| 26:25 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 24:16 | TXDATA1         | 0x000   | W      | <b>TX Data</b><br>Second frame to write to FIFO.   |
| 15    | RXENAT0         | 0   | W      | <b>Enable RX After Transmission</b><br>Set to enable reception after transmission.   |
| 14    | TXDISAT0        | 0   | W      | <b>Clear TXEN After Transmission</b><br>Set to disable transmitter and release data bus directly after transmission.   |
| 13    | TXBREAK0        | 0   | W      | <b>Transmit Data as Break</b><br>Set to send data as a break. Recipient will see a framing error or a break condition depending on its configuration and the value of TXDATA.        |
| 12    | TXTRIAT0        | 0   | W      | <b>Set TXTRI After Transmission</b><br>Set to tristate transmitter by setting TXTRI after transmission.  |
| 11    | UBRXAT0         | 0   | W      | <b>Unblock RX After Transmission</b><br>Set clear RXBLOCK after transmission, unblocking the receiver.   |
| 10:9  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 8:0   | TXDATA0         | 0x000   | W      | <b>TX Data</b><br>First frame to write to buffer.  |

## 19.5.16 USARTn\_TXDOUBLE - TX Buffer Double Data Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |   |   |         |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---------|---|---|---|---|---|---|---|
| 0x03C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00    |    |    |    |    |    |   |   | 0x00    |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W       |    |    |    |    |    |   |   | W       |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | TXDATA1 |    |    |    |    |    |   |   | TXDATA0 |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description  |
|-------|----------|--|--------|--|
| 31:16 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 15:8  | TXDATA1  | 0x00   | W      | <b>TX Data</b><br>Second frame to write to buffer. |
| 7:0   | TXDATA0  | 0x00   | W      | <b>TX Data</b><br>First frame to write to buffer.  |

## 19.5.17 USARTn\_IF - Interrupt Flag Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |       |       |       |        |     |     |      |      |      |      |      |      |      |        |         |      |     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|-------|-------|--------|-----|-----|------|------|------|------|------|------|------|--------|---------|------|-----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|
| 0x040         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15    | 14    | 13    | 12     | 11  | 10  | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2      | 1       | 0    |     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0     | 0     | 0     | 0      | 0   | 0   | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0      | 0       | 0    | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R     | R     | R     | R      | R   | R   | R    | R    | R    | R    | R    | R    | R    | R      | R       | R    | R   | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | TCMP2 | TCMP1 | TCMP0 | TXIDLE | CCF | SSM | MPAF | FERR | PERR | TXUF | TXOF | RXUF | RXOF | RXFULL | RXDATAV | TXBL | TXC |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 31:17 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 16    | TCMP2           | 0   | R      | <b>Timer Comparator 2 Interrupt Flag</b><br>Set when the timer reaches the comparator 2 value, TCMP2.  |
| 15    | TCMP1           | 0   | R      | <b>Timer Comparator 1 Interrupt Flag</b><br>Set when the timer reaches the comparator 1 value, TCMP1.  |
| 14    | TCMP0           | 0   | R      | <b>Timer Comparator 0 Interrupt Flag</b><br>Set when the Timer reaches the comparator 0 value, TCMP0.  |
| 13    | TXIDLE          | 0   | R      | <b>TX Idle Interrupt Flag</b><br>Set when TX goes idle. At this point, transmission has ended  |
| 12    | CCF             | 0   | R      | <b>Collision Check Fail Interrupt Flag</b><br>Set when a collision check notices an error in the transmitted data.   |
| 11    | SSM             | 0   | R      | <b>Slave-Select in Master Mode Interrupt Flag</b><br>Set when the device is selected as a slave when in master mode.   |
| 10    | MPAF            | 0   | R      | <b>Multi-Processor Address Frame Interrupt Flag</b><br>Set when a multi-processor address frame is detected.   |
| 9     | FERR            | 0   | R      | <b>Framing Error Interrupt Flag</b><br>Set when a frame with a framing error is received while RXBLOCK is cleared.   |
| 8     | PERR            | 0   | R      | <b>Parity Error Interrupt Flag</b><br>Set when a frame with a parity error (asynchronous mode only) is received while RXBLOCK is cleared.  |
| 7     | TXUF            | 0   | R      | <b>TX Underflow Interrupt Flag</b><br>Set when operating as a synchronous slave, no data is available in the transmit buffer when the master starts transmission of a new frame. |
| 6     | TXOF            | 0   | R      | <b>TX Overflow Interrupt Flag</b><br>Set when a write is done to the transmit buffer while it is full. The data already in the transmit buffer is preserved.                     |
| 5     | RXUF            | 0   | R      | <b>RX Underflow Interrupt Flag</b><br>Set when trying to read from the receive buffer when it is empty.  |
| 4     | RXOF            | 0   | R      | <b>RX Overflow Interrupt Flag</b><br>Set when data is incoming while the receive shift register is full. The data previously in the shift register is lost.                      |

| Bit | Name    | Reset | Access | Description   |
|-----|---------|-------|--------|---|
| 3   | RXFULL  | 0     | R      | <b>RX Buffer Full Interrupt Flag</b><br>Set when the receive buffer becomes full.   |
| 2   | RXDATAV | 0     | R      | <b>RX Data Valid Interrupt Flag</b><br>Set when data becomes available in the receive buffer.   |
| 1   | TXBL    | 1     | R      | <b>TX Buffer Level Interrupt Flag</b><br>Set when buffer becomes empty if buffer level is set to 0x0, or when the number of empty TX buffer elements equals specified buffer level. |
| 0   | TXC     | 0     | R      | <b>TX Complete Interrupt Flag</b><br>This interrupt is set after a transmission when both the TX buffer and shift register are empty.   |

## 19.5.18 USARTn\_IFS - Interrupt Flag Set Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |       |       |       |        |     |     |      |      |      |      |      |      |      |        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |     |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|-------|-------|--------|-----|-----|------|------|------|------|------|------|------|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----|
| 0x044         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16    | 15    | 14    | 13     | 12  | 11  | 10   | 9    | 8    | 7    | 6    | 5    | 4    | 3      | 2  | 1  | 0  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |     |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0     | 0     | 0     | 0      | 0   | 0   | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |    |     |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W1    | W1    | W1    | W1     | W1  | W1  | W1   | W1   | W1   | W1   | W1   | W1   | W1   | W1     | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 |     |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | TCMP2 | TCMP1 | TCMP0 | TXIDLE | CCF | SSM | MPAF | FERR | PERR | TXUF | TXOF | RXUF | RXOF | RXFULL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | TXC |

| Bit   | Name     | Reset   | Access | Description  |
|-------|----------|---|--------|--|
| 31:17 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 16    | TCMP2    | 0   | W1     | <b>Set TCMP2 Interrupt Flag</b><br>Write 1 to set the TCMP2 interrupt flag   |
| 15    | TCMP1    | 0   | W1     | <b>Set TCMP1 Interrupt Flag</b><br>Write 1 to set the TCMP1 interrupt flag   |
| 14    | TCMP0    | 0   | W1     | <b>Set TCMP0 Interrupt Flag</b><br>Write 1 to set the TCMP0 interrupt flag   |
| 13    | TXIDLE   | 0   | W1     | <b>Set TXIDLE Interrupt Flag</b><br>Write 1 to set the TXIDLE interrupt flag |
| 12    | CCF      | 0   | W1     | <b>Set CCF Interrupt Flag</b><br>Write 1 to set the CCF interrupt flag       |
| 11    | SSM      | 0   | W1     | <b>Set SSM Interrupt Flag</b><br>Write 1 to set the SSM interrupt flag       |
| 10    | MPAF     | 0   | W1     | <b>Set MPAF Interrupt Flag</b><br>Write 1 to set the MPAF interrupt flag     |
| 9     | FERR     | 0   | W1     | <b>Set FERR Interrupt Flag</b><br>Write 1 to set the FERR interrupt flag     |
| 8     | PERR     | 0   | W1     | <b>Set PERR Interrupt Flag</b><br>Write 1 to set the PERR interrupt flag     |
| 7     | TXUF     | 0   | W1     | <b>Set TXUF Interrupt Flag</b><br>Write 1 to set the TXUF interrupt flag     |
| 6     | TXOF     | 0   | W1     | <b>Set TXOF Interrupt Flag</b><br>Write 1 to set the TXOF interrupt flag     |
| 5     | RXUF     | 0   | W1     | <b>Set RXUF Interrupt Flag</b><br>Write 1 to set the RXUF interrupt flag     |
| 4     | RXOF     | 0   | W1     | <b>Set RXOF Interrupt Flag</b><br>Write 1 to set the RXOF interrupt flag     |
| 3     | RXFULL   | 0   | W1     | <b>Set RXFULL Interrupt Flag</b><br>Write 1 to set the RXFULL interrupt flag |

| Bit | Name     | Reset  | Access | Description  |
|-----|----------|--|--------|--|
| 2:1 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 0   | TXC      | 0  | W1     | <b>Set TXC Interrupt Flag</b><br>Write 1 to set the TXC interrupt flag |

## 19.5.19 USARTn\_IFC - Interrupt Flag Clear Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |       |       |       |        |       |       |       |       |       |       |       |       |       |        |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |  |     |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|-------|-------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|--|-----|
| 0x048         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15    | 14    | 13    | 12     | 11    | 10    | 9     | 8     | 7     | 6     | 5     | 4     | 3     | 2      | 1     | 0     |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |  |     |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0     | 0     | 0     | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |       |  |     |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | (R)W1 | (R)W1 | (R)W1 | (R)W1  | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1  | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 |  |     |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | TCMP2 | TCMP1 | TCMP0 | TXIDLE | CCF   | SSM   | MPAF  | FERR  | PERR  | TXUF  | TXOF  | RXUF  | RXOF  | RXFULL |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |  | TXC |

| Bit   | Name     | Reset   | Access | Description   |
|-------|----------|---|--------|---|
| 31:17 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 16    | TCMP2    | 0   | (R)W1  | <b>Clear TCMP2 Interrupt Flag</b><br><br>Write 1 to clear the TCMP2 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |
| 15    | TCMP1    | 0   | (R)W1  | <b>Clear TCMP1 Interrupt Flag</b><br><br>Write 1 to clear the TCMP1 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |
| 14    | TCMP0    | 0   | (R)W1  | <b>Clear TCMP0 Interrupt Flag</b><br><br>Write 1 to clear the TCMP0 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |
| 13    | TXIDLE   | 0   | (R)W1  | <b>Clear TXIDLE Interrupt Flag</b><br><br>Write 1 to clear the TXIDLE interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 12    | CCF      | 0   | (R)W1  | <b>Clear CCF Interrupt Flag</b><br><br>Write 1 to clear the CCF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).       |
| 11    | SSM      | 0   | (R)W1  | <b>Clear SSM Interrupt Flag</b><br><br>Write 1 to clear the SSM interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).       |
| 10    | MPAF     | 0   | (R)W1  | <b>Clear MPAF Interrupt Flag</b><br><br>Write 1 to clear the MPAF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 9     | FERR     | 0   | (R)W1  | <b>Clear FERR Interrupt Flag</b><br><br>Write 1 to clear the FERR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 8     | PERR     | 0   | (R)W1  | <b>Clear PERR Interrupt Flag</b><br><br>Write 1 to clear the PERR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 7     | TXUF     | 0   | (R)W1  | <b>Clear TXUF Interrupt Flag</b><br><br>Write 1 to clear the TXUF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |

| Bit | Name            | Reset   | Access | Description   |
|-----|-----------------|---|--------|---|
| 6   | TXOF            | 0   | (R)W1  | <b>Clear TXOF Interrupt Flag</b><br><br>Write 1 to clear the TXOF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 5   | RXUF            | 0   | (R)W1  | <b>Clear RXUF Interrupt Flag</b><br><br>Write 1 to clear the RXUF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 4   | RXOF            | 0   | (R)W1  | <b>Clear RXOF Interrupt Flag</b><br><br>Write 1 to clear the RXOF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 3   | RXFULL          | 0   | (R)W1  | <b>Clear RXFULL Interrupt Flag</b><br><br>Write 1 to clear the RXFULL interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 2:1 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 0   | TXC             | 0   | (R)W1  | <b>Clear TXC Interrupt Flag</b><br><br>Write 1 to clear the TXC interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).       |

## 19.5.20 USARTn\_IEN - Interrupt Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |       |       |       |        |     |     |      |      |      |      |      |      |      |        |         |      |     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|-------|-------|--------|-----|-----|------|------|------|------|------|------|------|--------|---------|------|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0x04C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15    | 14    | 13    | 12     | 11  | 10  | 9    | 8    | 7    | 6    | 5    | 4    | 3    | 2      | 1       | 0    |     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0     | 0     | 0     | 0      | 0   | 0   | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0      | 0       | 0    | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |    |    |    |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW    | RW    | RW    | RW     | RW  | RW  | RW   | RW   | RW   | RW   | RW   | RW   | RW   | RW     | RW      | RW   | RW  | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | TCMP2 | TCMP1 | TCMP0 | TXIDLE | CCF | SSM | MPAF | FERR | PERR | TXUF | TXOF | RXUF | RXOF | RXFULL | RXDATAV | TXBL | TXC |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:17 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 16    | TCMP2           | 0   | RW     | <b>TCMP2 Interrupt Enable</b><br>Enable/disable the TCMP2 interrupt   |
| 15    | TCMP1           | 0   | RW     | <b>TCMP1 Interrupt Enable</b><br>Enable/disable the TCMP1 interrupt   |
| 14    | TCMP0           | 0   | RW     | <b>TCMP0 Interrupt Enable</b><br>Enable/disable the TCMP0 interrupt   |
| 13    | TXIDLE          | 0   | RW     | <b>TXIDLE Interrupt Enable</b><br>Enable/disable the TXIDLE interrupt |
| 12    | CCF             | 0   | RW     | <b>CCF Interrupt Enable</b><br>Enable/disable the CCF interrupt       |
| 11    | SSM             | 0   | RW     | <b>SSM Interrupt Enable</b><br>Enable/disable the SSM interrupt       |
| 10    | MPAF            | 0   | RW     | <b>MPAF Interrupt Enable</b><br>Enable/disable the MPAF interrupt     |
| 9     | FERR            | 0   | RW     | <b>FERR Interrupt Enable</b><br>Enable/disable the FERR interrupt     |
| 8     | PERR            | 0   | RW     | <b>PERR Interrupt Enable</b><br>Enable/disable the PERR interrupt     |
| 7     | TXUF            | 0   | RW     | <b>TXUF Interrupt Enable</b><br>Enable/disable the TXUF interrupt     |
| 6     | TXOF            | 0   | RW     | <b>TXOF Interrupt Enable</b><br>Enable/disable the TXOF interrupt     |
| 5     | RXUF            | 0   | RW     | <b>RXUF Interrupt Enable</b><br>Enable/disable the RXUF interrupt     |
| 4     | RXOF            | 0   | RW     | <b>RXOF Interrupt Enable</b><br>Enable/disable the RXOF interrupt     |

| Bit | Name    | Reset | Access | Description   |
|-----|---------|-------|--------|---|
| 3   | RXFULL  | 0     | RW     | <b>RXFULL Interrupt Enable</b><br>Enable/disable the RXFULL interrupt   |
| 2   | RXDATAV | 0     | RW     | <b>RXDATAV Interrupt Enable</b><br>Enable/disable the RXDATAV interrupt |
| 1   | TXBL    | 0     | RW     | <b>TXBL Interrupt Enable</b><br>Enable/disable the TXBL interrupt       |
| 0   | TXC     | 0     | RW     | <b>TXC Interrupt Enable</b><br>Enable/disable the TXC interrupt         |

## 19.5.21 USARTn\_IRCTRL - IrDA Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |          |    |    |    |         |    |    |    |    |    |    |   |        |   |      |   |      |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|---------|----|----|----|----|----|----|---|--------|---|------|---|------|---|---|---|---|
| 0x050         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20       | 19 | 18 | 17 | 16      | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8      | 7 | 6    | 5 | 4    | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    | 0x0      |    |    |    | 0       |    |    |    | 0  |    |    |   | 0x0    |   | 0    |   |      |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    | RW       |    |    |    | RW      |    |    |    |    |    |    |   | RW     |   | RW   |   | RW   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    | IRPRSSEL |    |    |    | IRPRSEN |    |    |    |    |    |    |   | IRFILT |   | IRPW |   | IREN |   |   |   |   |

| Bit   | Name            | Reset   | Access | Description |
|-------|-----------------|---|--------|-------------|
| 31:12 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |             |

|      |          |         |    |   |
|------|----------|---------|----|---|
| 11:8 | IRPRSSEL | 0x0     | RW | <b>IrDA PRS Channel Select</b><br>A PRS can be used as input to the pulse modulator instead of TX. This value selects the channel to use. |
|      | Value    | Mode    |    | Description   |
|      | 0        | PRSCH0  |    | PRS Channel 0 selected  |
|      | 1        | PRSCH1  |    | PRS Channel 1 selected  |
|      | 2        | PRSCH2  |    | PRS Channel 2 selected  |
|      | 3        | PRSCH3  |    | PRS Channel 3 selected  |
|      | 4        | PRSCH4  |    | PRS Channel 4 selected  |
|      | 5        | PRSCH5  |    | PRS Channel 5 selected  |
|      | 6        | PRSCH6  |    | PRS Channel 6 selected  |
|      | 7        | PRSCH7  |    | PRS Channel 7 selected  |
|      | 8        | PRSCH8  |    | PRS Channel 8 selected  |
|      | 9        | PRSCH9  |    | PRS Channel 9 selected  |
|      | 10       | PRSCH10 |    | PRS Channel 10 selected   |
|      | 11       | PRSCH11 |    | PRS Channel 11 selected   |

|     |                 |   |    |  |
|-----|-----------------|---|----|--|
| 7   | IRPRSEN         | 0   | RW | <b>IrDA PRS Channel Enable</b><br>Enable the PRS channel selected by IRPRSSEL as input to IrDA module instead of TX. |
| 6:4 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |    |  |

|   |        |   |    |  |
|---|--------|---|----|--|
| 3 | IRFILT | 0 | RW | <b>IrDA RX Filter</b><br>Set to enable filter on IrDA demodulator.                             |
|   | Value  |   |    | Description  |
|   | 0      |   |    | No filter enabled  |
|   | 1      |   |    | Filter enabled. IrDA pulse must be high for at least 4 consecutive clock cycles to be detected |

| Bit | Name  | Reset | Access | Description   |
|-----|-------|-------|--------|---|
| 2:1 | IRPW  | 0x0   | RW     | <b>IrDA TX Pulse Width</b><br>Configure the pulse width generated by the IrDA modulator as a fraction of the configured USART bit period. |
|     | Value | Mode  |        | Description   |
|     | 0     | ONE   |        | IrDA pulse width is 1/16 for OVS=0 and 1/8 for OVS=1  |
|     | 1     | TWO   |        | IrDA pulse width is 2/16 for OVS=0 and 2/8 for OVS=1  |
|     | 2     | THREE |        | IrDA pulse width is 3/16 for OVS=0 and 3/8 for OVS=1  |
|     | 3     | FOUR  |        | IrDA pulse width is 4/16 for OVS=0 and 4/8 for OVS=1  |
| 0   | IREN  | 0     | RW     | <b>Enable IrDA Module</b><br>Enable IrDA module and rout USART signals through it.  |

## 19.5.22 USARTn\_INPUT - USART Input Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |          |   |   |   |   |   |   |       |   |  |  |  |  |  |         |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|----------|---|---|---|---|---|---|-------|---|--|--|--|--|--|---------|
| 0x058         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8        | 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0 |  |  |  |  |  |         |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0      |    |    |    |    |    |   | 0x0      |   |   |   |   |   |   | 0     |   |  |  |  |  |  | 0x0     |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW     |    |    |    |    |    |   | RW       |   |   |   |   |   |   | RW    |   |  |  |  |  |  | RW      |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CLKPRS |    |    |    |    |    |   | CLKPRSEL |   |   |   |   |   |   | RXPRS |   |  |  |  |  |  | RXPRSEL |

| Bit   | Name            | Reset   | Access | Description  |       |      |             |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |
|-------|-----------------|---|--------|--|-------|------|-------------|---|--------|------------------------|---|--------|------------------------|---|--------|------------------------|---|--------|------------------------|---|--------|------------------------|---|--------|------------------------|---|--------|------------------------|---|--------|------------------------|---|--------|------------------------|---|--------|------------------------|----|---------|-------------------------|----|---------|-------------------------|
| 31:16 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |
| 15    | CLKPRS          | 0   | RW     | <b>PRS CLK Enable</b><br>When set, the PRS channel selected as input to CLK.   |       |      |             |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |
| 14:12 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |
| 11:8  | CLKPRSEL        | 0x0   | RW     | <b>CLK PRS Channel Select</b><br>Select PRS channel as input to CLK.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>0</td><td>PRSCH0</td><td>PRS Channel 0 selected</td></tr> <tr><td>1</td><td>PRSCH1</td><td>PRS Channel 1 selected</td></tr> <tr><td>2</td><td>PRSCH2</td><td>PRS Channel 2 selected</td></tr> <tr><td>3</td><td>PRSCH3</td><td>PRS Channel 3 selected</td></tr> <tr><td>4</td><td>PRSCH4</td><td>PRS Channel 4 selected</td></tr> <tr><td>5</td><td>PRSCH5</td><td>PRS Channel 5 selected</td></tr> <tr><td>6</td><td>PRSCH6</td><td>PRS Channel 6 selected</td></tr> <tr><td>7</td><td>PRSCH7</td><td>PRS Channel 7 selected</td></tr> <tr><td>8</td><td>PRSCH8</td><td>PRS Channel 8 selected</td></tr> <tr><td>9</td><td>PRSCH9</td><td>PRS Channel 9 selected</td></tr> <tr><td>10</td><td>PRSCH10</td><td>PRS Channel 10 selected</td></tr> <tr><td>11</td><td>PRSCH11</td><td>PRS Channel 11 selected</td></tr> </tbody> </table> | Value | Mode | Description | 0 | PRSCH0 | PRS Channel 0 selected | 1 | PRSCH1 | PRS Channel 1 selected | 2 | PRSCH2 | PRS Channel 2 selected | 3 | PRSCH3 | PRS Channel 3 selected | 4 | PRSCH4 | PRS Channel 4 selected | 5 | PRSCH5 | PRS Channel 5 selected | 6 | PRSCH6 | PRS Channel 6 selected | 7 | PRSCH7 | PRS Channel 7 selected | 8 | PRSCH8 | PRS Channel 8 selected | 9 | PRSCH9 | PRS Channel 9 selected | 10 | PRSCH10 | PRS Channel 10 selected | 11 | PRSCH11 | PRS Channel 11 selected |
| Value | Mode            | Description   |        |  |       |      |             |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |
| 0     | PRSCH0          | PRS Channel 0 selected  |        |  |       |      |             |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |
| 1     | PRSCH1          | PRS Channel 1 selected  |        |  |       |      |             |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |
| 2     | PRSCH2          | PRS Channel 2 selected  |        |  |       |      |             |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |
| 3     | PRSCH3          | PRS Channel 3 selected  |        |  |       |      |             |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |
| 4     | PRSCH4          | PRS Channel 4 selected  |        |  |       |      |             |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |
| 5     | PRSCH5          | PRS Channel 5 selected  |        |  |       |      |             |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |
| 6     | PRSCH6          | PRS Channel 6 selected  |        |  |       |      |             |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |
| 7     | PRSCH7          | PRS Channel 7 selected  |        |  |       |      |             |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |
| 8     | PRSCH8          | PRS Channel 8 selected  |        |  |       |      |             |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |
| 9     | PRSCH9          | PRS Channel 9 selected  |        |  |       |      |             |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |
| 10    | PRSCH10         | PRS Channel 10 selected   |        |  |       |      |             |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |
| 11    | PRSCH11         | PRS Channel 11 selected   |        |  |       |      |             |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |
| 7     | RXPRS           | 0   | RW     | <b>PRS RX Enable</b><br>When set, the PRS channel selected as input to RX.   |       |      |             |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |
| 6:4   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |
| 3:0   | RXPRSEL         | 0x0   | RW     | <b>RX PRS Channel Select</b><br>Select PRS channel as input to RX.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> </tbody> </table>   | Value | Mode | Description |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |
| Value | Mode            | Description   |        |  |       |      |             |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |   |        |                        |    |         |                         |    |         |                         |

| Bit | Name | Reset   | Access | Description             |
|-----|------|---------|--------|-------------------------|
| 0   |      | PRSCH0  |        | PRS Channel 0 selected  |
| 1   |      | PRSCH1  |        | PRS Channel 1 selected  |
| 2   |      | PRSCH2  |        | PRS Channel 2 selected  |
| 3   |      | PRSCH3  |        | PRS Channel 3 selected  |
| 4   |      | PRSCH4  |        | PRS Channel 4 selected  |
| 5   |      | PRSCH5  |        | PRS Channel 5 selected  |
| 6   |      | PRSCH6  |        | PRS Channel 6 selected  |
| 7   |      | PRSCH7  |        | PRS Channel 7 selected  |
| 8   |      | PRSCH8  |        | PRS Channel 8 selected  |
| 9   |      | PRSCH9  |        | PRS Channel 9 selected  |
| 10  |      | PRSCH10 |        | PRS Channel 10 selected |
| 11  |      | PRSCH11 |        | PRS Channel 11 selected |



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| Bit | Name | Reset | Access | Description  |
|-----|------|-------|--------|--|
| 0   | EN   | 0     | RW     | <b>Enable I2S Mode</b><br>Set the U(S)ART in I2S mode. |

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## 19.5.24 USARTn\_TIMING - Timing Register

| Offset        | Bit Position |    |        |    |    |    |     |    |    |    |         |    |    |    |         |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|---------------|--------------|----|--------|----|----|----|-----|----|----|----|---------|----|----|----|---------|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|
| 0x060         | 31           | 30 | 29     | 28 | 27 | 26 | 25  | 24 | 23 | 22 | 21      | 20 | 19 | 18 | 17      | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| <b>Reset</b>  |              |    | 0x0    |    |    |    | 0x0 |    |    |    | 0x0     |    |    |    | 0x0     |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| <b>Access</b> |              |    | RW     |    |    |    | RW  |    |    |    | RW      |    |    |    | RW      |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| <b>Name</b>   |              |    | CSHOLD |    |    |    | ICS |    |    |    | CSSETUP |    |    |    | TXDELAY |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |

| Bit | Name            | Reset   | Access | Description |
|-----|-----------------|---|--------|-------------|
| 31  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |             |

|       |        |     |    |                         |
|-------|--------|-----|----|-------------------------|
| 30:28 | CSHOLD | 0x0 | RW | <b>Chip Select Hold</b> |
|-------|--------|-----|----|-------------------------|

Chip Select will be asserted after the end of frame transmission. When using TCMPn, normally set TIMECMPn\_TSTART to DISABLE to stop general timer and to prevent unwanted interrupts.

| Value | Mode  | Description  |
|-------|-------|--|
| 0     | ZERO  | Disable CS being asserted after the end of transmission              |
| 1     | ONE   | CS is asserted for 1 baud-times after the end of transmission        |
| 2     | TWO   | CS is asserted for 2 baud-times after the end of transmission        |
| 3     | THREE | CS is asserted for 3 baud-times after the end of transmission        |
| 4     | SEVEN | CS is asserted for 7 baud-times after the end of transmission        |
| 5     | TCMP0 | CS is asserted after the end of transmission for TCMPVAL0 baud-times |
| 6     | TCMP1 | CS is asserted after the end of transmission for TCMPVAL1 baud-times |
| 7     | TCMP2 | CS is asserted after the end of transmission for TCMPVAL2 baud-times |

|    |                 |   |  |  |
|----|-----------------|---|--|--|
| 27 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |  |
|----|-----------------|---|--|--|

|       |     |     |    |                                |
|-------|-----|-----|----|--------------------------------|
| 26:24 | ICS | 0x0 | RW | <b>Inter-character Spacing</b> |
|-------|-----|-----|----|--------------------------------|

Inter-character spacing after each TX frame while the TX buffer is not empty. When using USART\_TIMECMPn, normally set TSTART to DISABLE to stop general timer and to prevent unwanted interrupts.

| Value | Mode  | Description  |
|-------|-------|--|
| 0     | ZERO  | There is no space between characters                                       |
| 1     | ONE   | Create a space of 1 baud-times before start of transmission                |
| 2     | TWO   | Create a space of 2 baud-times before start of transmission                |
| 3     | THREE | Create a space of 3 baud-times before start of transmission                |
| 4     | SEVEN | Create a space of 7 baud-times before start of transmission                |
| 5     | TCMP0 | Create a space of before the start of transmission for TCMPVAL0 baud-times |
| 6     | TCMP1 | Create a space of before the start of transmission for TCMPVAL1 baud-times |

| Bit  | Name            | Reset   | Access  | Description  |
|--|-----------------|---|---|--|
|  | 7               | TCMP2   |   | Create a space of before the start of transmission for TCMPVAL2 baud-times |
| 23   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 22:20  | CSSETUP         | 0x0   | RW  | <b>Chip Select Setup</b>   |
| Chip Select will be asserted before the start of frame transmission. When using USART_TIMECMPn, normally set TSTART to DISABLE to stop general timer and to prevent unwanted interrupts. |                 |   |   |  |
|  | Value           | Mode  | Description   |  |
|  | 0               | ZERO  | CS is not asserted before start of transmission                         |  |
|  | 1               | ONE   | CS is asserted for 1 baud-times before start of transmission            |  |
|  | 2               | TWO   | CS is asserted for 2 baud-times before start of transmission            |  |
|  | 3               | THREE   | CS is asserted for 3 baud-times before start of transmission            |  |
|  | 4               | SEVEN   | CS is asserted for 7 baud-times before start of transmission            |  |
|  | 5               | TCMP0   | CS is asserted before the start of transmission for TCMPVAL0 baud-times |  |
|  | 6               | TCMP1   | CS is asserted before the start of transmission for TCMPVAL1 baud-times |  |
|  | 7               | TCMP2   | CS is asserted before the start of transmission for TCMPVAL2 baud-times |  |
| 19   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 18:16  | TXDELAY         | 0x0   | RW  | <b>TX Frame Start Delay</b>  |
| Number of baud-times to delay the start of frame transmission. When using USART_TIMECMPn, normally set TSTART to DISABLE to stop general timer and to prevent unwanted interrupts.       |                 |   |   |  |
|  | Value           | Mode  | Description   |  |
|  | 0               | DISABLE   | Disable - TXDELAY in USARTn_CTRL can be used for legacy                 |  |
|  | 1               | ONE   | Start of transmission is delayed for 1 baud-times                       |  |
|  | 2               | TWO   | Start of transmission is delayed for 2 baud-times                       |  |
|  | 3               | THREE   | Start of transmission is delayed for 3 baud-times                       |  |
|  | 4               | SEVEN   | Start of transmission is delayed for 7 baud-times                       |  |
|  | 5               | TCMP0   | Start of transmission is delayed for TCMPVAL0 baud-times                |  |
|  | 6               | TCMP1   | Start of transmission is delayed for TCMPVAL1 baud-times                |  |
|  | 7               | TCMP2   | Start of transmission is delayed for TCMPVAL2 baud-times                |  |
| 15:0   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |



## 19.5.26 USARTn\_TIMECMP0 - Used to Generate Interrupts and Various Delays

| Offset        | Bit Position |    |    |    |    |    |    |           |    |       |    |    |    |        |    |    |    |    |    |    |    |    |   |         |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|-----------|----|-------|----|----|----|--------|----|----|----|----|----|----|----|----|---|---------|---|---|---|---|---|---|---|---|
| 0x068         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24        | 23 | 22    | 21 | 20 | 19 | 18     | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8       | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    | 0         |    | 0x0   |    |    |    | 0x0    |    |    |    |    |    |    |    |    |   | 0x00    |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    | RW        |    | RW    |    |    |    | RW     |    |    |    |    |    |    |    |    |   | RW      |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    | RESTARTEN |    | TSTOP |    |    |    | TSTART |    |    |    |    |    |    |    |    |   | TCMPVAL |   |   |   |   |   |   |   |   |

| Bit   | Name                                  | Reset  | Access | Description  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
|-------|---------------------------------------|--|--------|--|-------|-------------|-------------|---------------------------------------|---------|---|---|-------|---|---|-------|--|---|--------|--|---|-------|---|
| 31:25 | Reserved                              | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 24    | RESTARTEN                             | 0  | RW     | <b>Restart Timer on TCMP0</b><br>Each TCMP0 event will reset and restart the timer<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Disable the timer restarting on TCMP0</td> </tr> <tr> <td>1</td> <td>Enable the timer restarting on TCMP0</td> </tr> </tbody> </table>  | Value | Description | 0           | Disable the timer restarting on TCMP0 | 1       | Enable the timer restarting on TCMP0  |   |       |   |   |       |  |   |        |  |   |       |   |
| Value | Description                           |  |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 0     | Disable the timer restarting on TCMP0 |  |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 1     | Enable the timer restarting on TCMP0  |  |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 23    | Reserved                              | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 22:20 | TSTOP                                 | 0x0  | RW     | <b>Source Used to Disable Comparator 0</b><br>Select the source which disables comparator 0<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>TCMP0</td> <td>Comparator 0 is disabled when the counter equals TCMPVAL and triggers a TCMP0 event</td> </tr> <tr> <td>1</td> <td>TXST</td> <td>Comparator 0 is disabled at the start of transmission</td> </tr> <tr> <td>2</td> <td>RXACT</td> <td>Comparator 0 is disabled on RX going going Active (default: low)</td> </tr> <tr> <td>3</td> <td>RXACTN</td> <td>Comparator 0 is disabled on RX going Inactive</td> </tr> </tbody> </table>                               | Value | Mode        | Description | 0                                     | TCMP0   | Comparator 0 is disabled when the counter equals TCMPVAL and triggers a TCMP0 event | 1 | TXST  | Comparator 0 is disabled at the start of transmission | 2 | RXACT | Comparator 0 is disabled on RX going going Active (default: low) | 3 | RXACTN | Comparator 0 is disabled on RX going Inactive                        |   |       |   |
| Value | Mode                                  | Description  |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 0     | TCMP0                                 | Comparator 0 is disabled when the counter equals TCMPVAL and triggers a TCMP0 event                                      |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 1     | TXST                                  | Comparator 0 is disabled at the start of transmission  |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 2     | RXACT                                 | Comparator 0 is disabled on RX going going Active (default: low)   |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 3     | RXACTN                                | Comparator 0 is disabled on RX going Inactive  |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 19    | Reserved                              | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 18:16 | TSTART                                | 0x0  | RW     | <b>Timer Start Source</b><br>Source used to start comparator 0 and timer<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>DISABLE</td> <td>Comparator 0 is disabled</td> </tr> <tr> <td>1</td> <td>TXEOF</td> <td>Comparator 0 and timer are started at TX end of frame</td> </tr> <tr> <td>2</td> <td>TXC</td> <td>Comparator 0 and timer are started at TX Complete</td> </tr> <tr> <td>3</td> <td>RXACT</td> <td>Comparator 0 and timer are started at RX going Active (default: low)</td> </tr> <tr> <td>4</td> <td>RXEOF</td> <td>Comparator 0 and timer are started at RX end of frame</td> </tr> </tbody> </table> | Value | Mode        | Description | 0                                     | DISABLE | Comparator 0 is disabled  | 1 | TXEOF | Comparator 0 and timer are started at TX end of frame | 2 | TXC   | Comparator 0 and timer are started at TX Complete                | 3 | RXACT  | Comparator 0 and timer are started at RX going Active (default: low) | 4 | RXEOF | Comparator 0 and timer are started at RX end of frame |
| Value | Mode                                  | Description  |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 0     | DISABLE                               | Comparator 0 is disabled   |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 1     | TXEOF                                 | Comparator 0 and timer are started at TX end of frame  |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 2     | TXC                                   | Comparator 0 and timer are started at TX Complete  |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 3     | RXACT                                 | Comparator 0 and timer are started at RX going Active (default: low)   |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 4     | RXEOF                                 | Comparator 0 and timer are started at RX end of frame  |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |

| Bit  | Name     | Reset   | Access | Description   |
|------|----------|---|--------|---|
| 15:8 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 7:0  | TCMPVAL  | 0x00  | RW     | <b>Timer Comparator 0</b><br><br>When the timer equals TCMPVAL, this signals a TCMP0 event and sets the TCMP0 flag. This event can also be used to enable various USART functionality. A value of 0x00 represents 256 baud times. |

## 19.5.27 USARTn\_TIMECMP1 - Used to Generate Interrupts and Various Delays

| Offset        | Bit Position |    |    |    |    |    |    |           |    |       |    |    |    |        |    |    |    |    |    |    |    |    |   |         |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|-----------|----|-------|----|----|----|--------|----|----|----|----|----|----|----|----|---|---------|---|---|---|---|---|---|---|---|
| 0x06C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24        | 23 | 22    | 21 | 20 | 19 | 18     | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8       | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    | 0         |    | 0x0   |    |    |    | 0x0    |    |    |    |    |    |    |    |    |   | 0x00    |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    | RW        |    | RW    |    |    |    | RW     |    |    |    |    |    |    |    |    |   | RW      |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    | RESTARTEN |    | TSTOP |    |    |    | TSTART |    |    |    |    |    |    |    |    |   | TCMPVAL |   |   |   |   |   |   |   |   |

| Bit   | Name                                  | Reset   | Access | Description  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
|-------|---------------------------------------|---|--------|--|-------|-------------|-------------|---------------------------------------|---------|---|---|-------|---|---|-------|--|---|--------|--|---|-------|---|
| 31:25 | <i>Reserved</i>                       | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 24    | RESTARTEN                             | 0   | RW     | <b>Restart Timer on TCMP1</b><br>Each TCMP1 event will reset and restart the timer<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Disable the timer restarting on TCMP1</td> </tr> <tr> <td>1</td> <td>Enable the timer restarting on TCMP1</td> </tr> </tbody> </table>  | Value | Description | 0           | Disable the timer restarting on TCMP1 | 1       | Enable the timer restarting on TCMP1  |   |       |   |   |       |  |   |        |  |   |       |   |
| Value | Description                           |   |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 0     | Disable the timer restarting on TCMP1 |   |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 1     | Enable the timer restarting on TCMP1  |   |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 23    | <i>Reserved</i>                       | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 22:20 | TSTOP                                 | 0x0   | RW     | <b>Source Used to Disable Comparator 1</b><br>Select the source which disables comparator 1<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>TCMP1</td> <td>Comparator 1 is disabled when the counter equals TCMPVAL and triggers a TCMP1 event</td> </tr> <tr> <td>1</td> <td>TXST</td> <td>Comparator 1 is disabled at TX start TX Engine</td> </tr> <tr> <td>2</td> <td>RXACT</td> <td>Comparator 1 is disabled on RX going going Active (default: low)</td> </tr> <tr> <td>3</td> <td>RXACTN</td> <td>Comparator 1 is disabled on RX going Inactive</td> </tr> </tbody> </table>  | Value | Mode        | Description | 0                                     | TCMP1   | Comparator 1 is disabled when the counter equals TCMPVAL and triggers a TCMP1 event | 1 | TXST  | Comparator 1 is disabled at TX start TX Engine        | 2 | RXACT | Comparator 1 is disabled on RX going going Active (default: low) | 3 | RXACTN | Comparator 1 is disabled on RX going Inactive                              |   |       |   |
| Value | Mode                                  | Description   |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 0     | TCMP1                                 | Comparator 1 is disabled when the counter equals TCMPVAL and triggers a TCMP1 event   |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 1     | TXST                                  | Comparator 1 is disabled at TX start TX Engine  |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 2     | RXACT                                 | Comparator 1 is disabled on RX going going Active (default: low)  |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 3     | RXACTN                                | Comparator 1 is disabled on RX going Inactive   |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 19    | <i>Reserved</i>                       | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 18:16 | TSTART                                | 0x0   | RW     | <b>Timer Start Source</b><br>Source used to start comparator 1 and timer<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>DISABLE</td> <td>Comparator 1 is disabled</td> </tr> <tr> <td>1</td> <td>TXEOF</td> <td>Comparator 1 and timer are started at TX end of frame</td> </tr> <tr> <td>2</td> <td>TXC</td> <td>Comparator 1 and timer are started at TX Complete</td> </tr> <tr> <td>3</td> <td>RXACT</td> <td>Comparator 1 and timer are started at RX going going Active (default: low)</td> </tr> <tr> <td>4</td> <td>RXEOF</td> <td>Comparator 1 and timer are started at RX end of frame</td> </tr> </tbody> </table> | Value | Mode        | Description | 0                                     | DISABLE | Comparator 1 is disabled  | 1 | TXEOF | Comparator 1 and timer are started at TX end of frame | 2 | TXC   | Comparator 1 and timer are started at TX Complete                | 3 | RXACT  | Comparator 1 and timer are started at RX going going Active (default: low) | 4 | RXEOF | Comparator 1 and timer are started at RX end of frame |
| Value | Mode                                  | Description   |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 0     | DISABLE                               | Comparator 1 is disabled  |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 1     | TXEOF                                 | Comparator 1 and timer are started at TX end of frame   |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 2     | TXC                                   | Comparator 1 and timer are started at TX Complete   |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 3     | RXACT                                 | Comparator 1 and timer are started at RX going going Active (default: low)  |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |
| 4     | RXEOF                                 | Comparator 1 and timer are started at RX end of frame   |        |  |       |             |             |                                       |         |   |   |       |   |   |       |  |   |        |  |   |       |   |

| Bit  | Name     | Reset  | Access | Description   |
|------|----------|--|--------|---|
| 15:8 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 7:0  | TCMPVAL  | 0x00   | RW     | <b>Timer Comparator 1</b><br><br>When the timer equals TCMPVAL, this signals a TCMP1 event and sets the TCMP1 flag. This event can also be used to enable various USART functionality. A value of 0x00 represents 256 baud times. |

## 19.5.28 USARTn\_TIMECMP2 - Used to Generate Interrupts and Various Delays

| Offset        | Bit Position |    |    |    |    |    |    |           |    |       |    |    |    |        |    |    |    |    |    |    |    |    |   |         |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|-----------|----|-------|----|----|----|--------|----|----|----|----|----|----|----|----|---|---------|---|---|---|---|---|---|---|---|
| 0x070         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24        | 23 | 22    | 21 | 20 | 19 | 18     | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8       | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    | 0         |    | 0x0   |    |    |    | 0x0    |    |    |    |    |    |    |    |    |   | 0x00    |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    | RW        |    | RW    |    |    |    | RW     |    |    |    |    |    |    |    |    |   | RW      |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    | RESTARTEN |    | TSTOP |    |    |    | TSTART |    |    |    |    |    |    |    |    |   | TCMPVAL |   |   |   |   |   |   |   |   |

| Bit   | Name      | Reset  | Access  | Description   |
|-------|-----------|--|---|---|
| 31:25 | Reserved  | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |   |   |
| 24    | RESTARTEN | 0  | RW  | <b>Restart Timer on TCMP2</b><br>Each TCMP2 event will reset and restart the timer          |
|       | Value     | Description  |   |   |
|       | 0         | Disable the timer restarting on TCMP2  |   |   |
|       | 1         | Enable the timer restarting on TCMP2   |   |   |
| 23    | Reserved  | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |   |   |
| 22:20 | TSTOP     | 0x0  | RW  | <b>Source Used to Disable Comparator 2</b><br>Select the source which disables comparator 2 |
|       | Value     | Mode   | Description   |   |
|       | 0         | TCMP2  | Comparator 2 is disabled when the counter equals TCMPVAL and triggers a TCMP2 event |   |
|       | 1         | TXST   | Comparator 2 is disabled at TX start TX Engine                                      |   |
|       | 2         | RXACT  | Comparator 2 is disabled on RX going going Active (default: low)                    |   |
|       | 3         | RXACTN   | Comparator 2 is disabled on RX going Inactive                                       |   |
| 19    | Reserved  | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |   |   |
| 18:16 | TSTART    | 0x0  | RW  | <b>Timer Start Source</b><br>Source used to start comparator 2 and timer                    |
|       | Value     | Mode   | Description   |   |
|       | 0         | DISABLE  | Comparator 2 is disabled  |   |
|       | 1         | TXEOF  | Comparator 2 and timer are started at TX end of frame                               |   |
|       | 2         | TXC  | Comparator 2 and timer are started at TX Complete                                   |   |
|       | 3         | RXACT  | Comparator 2 and timer are started at RX going going Active (default: low)          |   |
|       | 4         | RXEOF  | Comparator 2 and timer are started at RX end of frame                               |   |

| Bit  | Name     | Reset  | Access | Description   |
|------|----------|--|--------|---|
| 15:8 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 7:0  | TCMPVAL  | 0x00   | RW     | <b>Timer Comparator 2</b><br>When the timer equals TCMPVAL, this signals a TCMP2 event and sets the TCMP2 flag. This event can also be used to enable various USART functionality. A value of 0x00 represents 256 baud times. |

## 19.5.29 USARTn\_ROUTEPEM - I/O Routing Pin Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |        |        |        |       |       |       |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|--------|--------|--------|-------|-------|-------|---|---|
| 0x074         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7      | 6      | 5      | 4     | 3     | 2     | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0      | 0      | 0      | 0     | 0     | 0     |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RW     | RW     | RW     | RW    | RW    | RW    |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RTSPEN | CTSPEN | CLKPEN | CSPEN | TXPEN | RXPEN |   |   |

| Bit   | Name                                | Reset   | Access | Description  |       |             |   |                                     |   |                                    |
|-------|-------------------------------------|---|--------|--|-------|-------------|---|-------------------------------------|---|------------------------------------|
| 31:6  | <i>Reserved</i>                     | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |             |   |                                     |   |                                    |
| 5     | RTSPEN                              | 0   | RW     | <b>RTS Pin Enable</b><br>When set, the RTS pin of the USART is enabled.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>The USn_RTS pin is disabled</td> </tr> <tr> <td>1</td> <td>The USn_RTS pin is enabled</td> </tr> </tbody> </table>                   | Value | Description | 0 | The USn_RTS pin is disabled         | 1 | The USn_RTS pin is enabled         |
| Value | Description                         |   |        |  |       |             |   |                                     |   |                                    |
| 0     | The USn_RTS pin is disabled         |   |        |  |       |             |   |                                     |   |                                    |
| 1     | The USn_RTS pin is enabled          |   |        |  |       |             |   |                                     |   |                                    |
| 4     | CTSPEN                              | 0   | RW     | <b>CTS Pin Enable</b><br>When set, the CTS pin of the USART is enabled.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>The USn_CTS pin is disabled</td> </tr> <tr> <td>1</td> <td>The USn_CTS pin is enabled</td> </tr> </tbody> </table>                   | Value | Description | 0 | The USn_CTS pin is disabled         | 1 | The USn_CTS pin is enabled         |
| Value | Description                         |   |        |  |       |             |   |                                     |   |                                    |
| 0     | The USn_CTS pin is disabled         |   |        |  |       |             |   |                                     |   |                                    |
| 1     | The USn_CTS pin is enabled          |   |        |  |       |             |   |                                     |   |                                    |
| 3     | CLKPEN                              | 0   | RW     | <b>CLK Pin Enable</b><br>When set, the CLK pin of the USART is enabled.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>The USn_CLK pin is disabled</td> </tr> <tr> <td>1</td> <td>The USn_CLK pin is enabled</td> </tr> </tbody> </table>                   | Value | Description | 0 | The USn_CLK pin is disabled         | 1 | The USn_CLK pin is enabled         |
| Value | Description                         |   |        |  |       |             |   |                                     |   |                                    |
| 0     | The USn_CLK pin is disabled         |   |        |  |       |             |   |                                     |   |                                    |
| 1     | The USn_CLK pin is enabled          |   |        |  |       |             |   |                                     |   |                                    |
| 2     | CSPEN                               | 0   | RW     | <b>CS Pin Enable</b><br>When set, the CS pin of the USART is enabled.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>The USn_CS pin is disabled</td> </tr> <tr> <td>1</td> <td>The USn_CS pin is enabled</td> </tr> </tbody> </table>                       | Value | Description | 0 | The USn_CS pin is disabled          | 1 | The USn_CS pin is enabled          |
| Value | Description                         |   |        |  |       |             |   |                                     |   |                                    |
| 0     | The USn_CS pin is disabled          |   |        |  |       |             |   |                                     |   |                                    |
| 1     | The USn_CS pin is enabled           |   |        |  |       |             |   |                                     |   |                                    |
| 1     | TXPEN                               | 0   | RW     | <b>TX Pin Enable</b><br>When set, the TX/MOSI pin of the USART is enabled<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>The U(S)n_TX (MOSI) pin is disabled</td> </tr> <tr> <td>1</td> <td>The U(S)n_TX (MOSI) pin is enabled</td> </tr> </tbody> </table> | Value | Description | 0 | The U(S)n_TX (MOSI) pin is disabled | 1 | The U(S)n_TX (MOSI) pin is enabled |
| Value | Description                         |   |        |  |       |             |   |                                     |   |                                    |
| 0     | The U(S)n_TX (MOSI) pin is disabled |   |        |  |       |             |   |                                     |   |                                    |
| 1     | The U(S)n_TX (MOSI) pin is enabled  |   |        |  |       |             |   |                                     |   |                                    |

| Bit   | Name  | Reset | Access | Description  |
|-------|-------|-------|--------|--|
| 0     | RXPEN | 0     | RW     | <b>RX Pin Enable</b><br>When set, the RX/MISO pin of the USART is enabled. |
| Value |       |       |        | Description  |
| 0     |       |       |        | The U(S)n_RX (MISO) pin is disabled  |
| 1     |       |       |        | The U(S)n_RX (MISO) pin is enabled   |

## 19.5.30 USARTn\_ROUTELOC0 - I/O Routing Location Register

| Offset        | Bit Position |    |    |    |        |    |    |    |    |    |    |    |       |    |    |    |    |    |    |    |       |    |   |   |   |   |   |   |   |       |   |   |  |  |
|---------------|--------------|----|----|----|--------|----|----|----|----|----|----|----|-------|----|----|----|----|----|----|----|-------|----|---|---|---|---|---|---|---|-------|---|---|--|--|
| 0x078         | 31           | 30 | 29 | 28 | 27     | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19    | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11    | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2     | 1 | 0 |  |  |
| <b>Reset</b>  |              |    |    |    | 0x00   |    |    |    |    |    |    |    | 0x00  |    |    |    |    |    |    |    | 0x00  |    |   |   |   |   |   |   |   | 0x00  |   |   |  |  |
| <b>Access</b> |              |    |    |    | RW     |    |    |    |    |    |    |    | RW    |    |    |    |    |    |    |    | RW    |    |   |   |   |   |   |   |   | RW    |   |   |  |  |
| <b>Name</b>   |              |    |    |    | CLKLOC |    |    |    |    |    |    |    | CSLOC |    |    |    |    |    |    |    | TXLOC |    |   |   |   |   |   |   |   | RXLOC |   |   |  |  |

| Bit   | Name            | Reset | Access | Description   |
|-------|-----------------|-------|--------|---|
| 31:30 | <i>Reserved</i> |       |        | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |

29:24 CLKLOC 0x00 RW **I/O Location**

Decides the location of the USART CLK pin.

| Value | Mode  | Description |
|-------|-------|-------------|
| 0     | LOC0  | Location 0  |
| 1     | LOC1  | Location 1  |
| 2     | LOC2  | Location 2  |
| 3     | LOC3  | Location 3  |
| 4     | LOC4  | Location 4  |
| 5     | LOC5  | Location 5  |
| 6     | LOC6  | Location 6  |
| 7     | LOC7  | Location 7  |
| 8     | LOC8  | Location 8  |
| 9     | LOC9  | Location 9  |
| 10    | LOC10 | Location 10 |
| 11    | LOC11 | Location 11 |
| 12    | LOC12 | Location 12 |
| 13    | LOC13 | Location 13 |
| 14    | LOC14 | Location 14 |
| 15    | LOC15 | Location 15 |
| 16    | LOC16 | Location 16 |
| 17    | LOC17 | Location 17 |
| 18    | LOC18 | Location 18 |
| 19    | LOC19 | Location 19 |
| 20    | LOC20 | Location 20 |
| 21    | LOC21 | Location 21 |
| 22    | LOC22 | Location 22 |
| 23    | LOC23 | Location 23 |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 24    |                 | LOC24   |        | Location 24  |
| 25    |                 | LOC25   |        | Location 25  |
| 26    |                 | LOC26   |        | Location 26  |
| 27    |                 | LOC27   |        | Location 27  |
| 28    |                 | LOC28   |        | Location 28  |
| 29    |                 | LOC29   |        | Location 29  |
| 30    |                 | LOC30   |        | Location 30  |
| 31    |                 | LOC31   |        | Location 31  |
| 23:22 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 21:16 | CSLOC           | 0x00  | RW     | <b>I/O Location</b><br>Decides the location of the USART CS pin. |
|       | Value           | Mode  |        | Description  |
|       | 0               | LOC0  |        | Location 0   |
|       | 1               | LOC1  |        | Location 1   |
|       | 2               | LOC2  |        | Location 2   |
|       | 3               | LOC3  |        | Location 3   |
|       | 4               | LOC4  |        | Location 4   |
|       | 5               | LOC5  |        | Location 5   |
|       | 6               | LOC6  |        | Location 6   |
|       | 7               | LOC7  |        | Location 7   |
|       | 8               | LOC8  |        | Location 8   |
|       | 9               | LOC9  |        | Location 9   |
|       | 10              | LOC10   |        | Location 10  |
|       | 11              | LOC11   |        | Location 11  |
|       | 12              | LOC12   |        | Location 12  |
|       | 13              | LOC13   |        | Location 13  |
|       | 14              | LOC14   |        | Location 14  |
|       | 15              | LOC15   |        | Location 15  |
|       | 16              | LOC16   |        | Location 16  |
|       | 17              | LOC17   |        | Location 17  |
|       | 18              | LOC18   |        | Location 18  |
|       | 19              | LOC19   |        | Location 19  |
|       | 20              | LOC20   |        | Location 20  |
|       | 21              | LOC21   |        | Location 21  |
|       | 22              | LOC22   |        | Location 22  |
|       | 23              | LOC23   |        | Location 23  |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
|       | 24              | LOC24   |        | Location 24  |
|       | 25              | LOC25   |        | Location 25  |
|       | 26              | LOC26   |        | Location 26  |
|       | 27              | LOC27   |        | Location 27  |
|       | 28              | LOC28   |        | Location 28  |
|       | 29              | LOC29   |        | Location 29  |
|       | 30              | LOC30   |        | Location 30  |
|       | 31              | LOC31   |        | Location 31  |
| 15:14 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 13:8  | TXLOC           | 0x00  | RW     | <b>I/O Location</b><br>Decides the location of the USART TX pin. |
|       | Value           | Mode  |        | Description  |
|       | 0               | LOC0  |        | Location 0   |
|       | 1               | LOC1  |        | Location 1   |
|       | 2               | LOC2  |        | Location 2   |
|       | 3               | LOC3  |        | Location 3   |
|       | 4               | LOC4  |        | Location 4   |
|       | 5               | LOC5  |        | Location 5   |
|       | 6               | LOC6  |        | Location 6   |
|       | 7               | LOC7  |        | Location 7   |
|       | 8               | LOC8  |        | Location 8   |
|       | 9               | LOC9  |        | Location 9   |
|       | 10              | LOC10   |        | Location 10  |
|       | 11              | LOC11   |        | Location 11  |
|       | 12              | LOC12   |        | Location 12  |
|       | 13              | LOC13   |        | Location 13  |
|       | 14              | LOC14   |        | Location 14  |
|       | 15              | LOC15   |        | Location 15  |
|       | 16              | LOC16   |        | Location 16  |
|       | 17              | LOC17   |        | Location 17  |
|       | 18              | LOC18   |        | Location 18  |
|       | 19              | LOC19   |        | Location 19  |
|       | 20              | LOC20   |        | Location 20  |
|       | 21              | LOC21   |        | Location 21  |
|       | 22              | LOC22   |        | Location 22  |
|       | 23              | LOC23   |        | Location 23  |

| Bit | Name            | Reset   | Access | Description  |
|-----|-----------------|---|--------|--|
| 24  |                 | LOC24   |        | Location 24  |
| 25  |                 | LOC25   |        | Location 25  |
| 26  |                 | LOC26   |        | Location 26  |
| 27  |                 | LOC27   |        | Location 27  |
| 28  |                 | LOC28   |        | Location 28  |
| 29  |                 | LOC29   |        | Location 29  |
| 30  |                 | LOC30   |        | Location 30  |
| 31  |                 | LOC31   |        | Location 31  |
| 7:6 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 5:0 | RXLOC           | 0x00  | RW     | <b>I/O Location</b><br>Decides the location of the USART RX pin. |
|     | Value           | Mode  |        | Description  |
|     | 0               | LOC0  |        | Location 0   |
|     | 1               | LOC1  |        | Location 1   |
|     | 2               | LOC2  |        | Location 2   |
|     | 3               | LOC3  |        | Location 3   |
|     | 4               | LOC4  |        | Location 4   |
|     | 5               | LOC5  |        | Location 5   |
|     | 6               | LOC6  |        | Location 6   |
|     | 7               | LOC7  |        | Location 7   |
|     | 8               | LOC8  |        | Location 8   |
|     | 9               | LOC9  |        | Location 9   |
|     | 10              | LOC10   |        | Location 10  |
|     | 11              | LOC11   |        | Location 11  |
|     | 12              | LOC12   |        | Location 12  |
|     | 13              | LOC13   |        | Location 13  |
|     | 14              | LOC14   |        | Location 14  |
|     | 15              | LOC15   |        | Location 15  |
|     | 16              | LOC16   |        | Location 16  |
|     | 17              | LOC17   |        | Location 17  |
|     | 18              | LOC18   |        | Location 18  |
|     | 19              | LOC19   |        | Location 19  |
|     | 20              | LOC20   |        | Location 20  |
|     | 21              | LOC21   |        | Location 21  |
|     | 22              | LOC22   |        | Location 22  |
|     | 23              | LOC23   |        | Location 23  |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
| 24  |      | LOC24 |        | Location 24 |
| 25  |      | LOC25 |        | Location 25 |
| 26  |      | LOC26 |        | Location 26 |
| 27  |      | LOC27 |        | Location 27 |
| 28  |      | LOC28 |        | Location 28 |
| 29  |      | LOC29 |        | Location 29 |
| 30  |      | LOC30 |        | Location 30 |
| 31  |      | LOC31 |        | Location 31 |

## 19.5.31 USARTn\_ROUTELOC1 - I/O Routing Location Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |        |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|--------|---|---|---|---|---|---|---|
| 0x07C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00   |    |    |    |    |    |   |   | 0x00   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW     |    |    |    |    |    |   |   | RW     |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RTSLOC |    |    |    |    |    |   |   | CTSLOC |   |   |   |   |   |   |   |

| Bit   | Name            | Reset   | Access | Description |
|-------|-----------------|---|--------|-------------|
| 31:14 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |             |

13:8    RTSLOC    0x00    RW    **I/O Location**

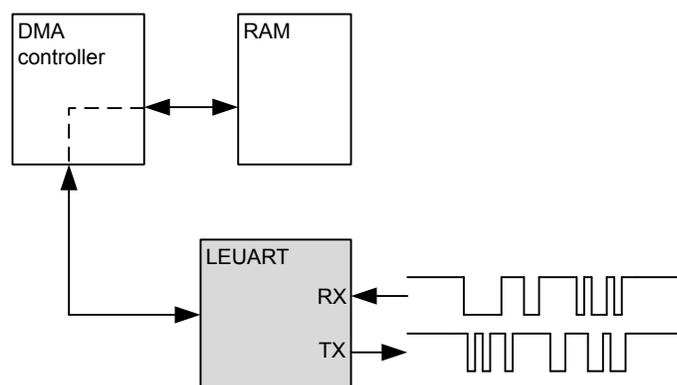
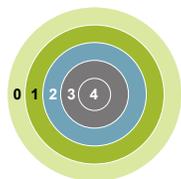
Decides the location of the USART RTS pin.

| Value | Mode  | Description |
|-------|-------|-------------|
| 0     | LOC0  | Location 0  |
| 1     | LOC1  | Location 1  |
| 2     | LOC2  | Location 2  |
| 3     | LOC3  | Location 3  |
| 4     | LOC4  | Location 4  |
| 5     | LOC5  | Location 5  |
| 6     | LOC6  | Location 6  |
| 7     | LOC7  | Location 7  |
| 8     | LOC8  | Location 8  |
| 9     | LOC9  | Location 9  |
| 10    | LOC10 | Location 10 |
| 11    | LOC11 | Location 11 |
| 12    | LOC12 | Location 12 |
| 13    | LOC13 | Location 13 |
| 14    | LOC14 | Location 14 |
| 15    | LOC15 | Location 15 |
| 16    | LOC16 | Location 16 |
| 17    | LOC17 | Location 17 |
| 18    | LOC18 | Location 18 |
| 19    | LOC19 | Location 19 |
| 20    | LOC20 | Location 20 |
| 21    | LOC21 | Location 21 |
| 22    | LOC22 | Location 22 |

| Bit | Name            | Reset   | Access | Description   |
|-----|-----------------|---|--------|---|
|     | 23              | LOC23   |        | Location 23   |
|     | 24              | LOC24   |        | Location 24   |
|     | 25              | LOC25   |        | Location 25   |
|     | 26              | LOC26   |        | Location 26   |
|     | 27              | LOC27   |        | Location 27   |
|     | 28              | LOC28   |        | Location 28   |
|     | 29              | LOC29   |        | Location 29   |
|     | 30              | LOC30   |        | Location 30   |
|     | 31              | LOC31   |        | Location 31   |
| 7:6 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 5:0 | CTSLOC          | 0x00  | RW     | <b>I/O Location</b><br>Decides the location of the USART CTS pin. |
|     | Value           | Mode  |        | Description   |
|     | 0               | LOC0  |        | Location 0  |
|     | 1               | LOC1  |        | Location 1  |
|     | 2               | LOC2  |        | Location 2  |
|     | 3               | LOC3  |        | Location 3  |
|     | 4               | LOC4  |        | Location 4  |
|     | 5               | LOC5  |        | Location 5  |
|     | 6               | LOC6  |        | Location 6  |
|     | 7               | LOC7  |        | Location 7  |
|     | 8               | LOC8  |        | Location 8  |
|     | 9               | LOC9  |        | Location 9  |
|     | 10              | LOC10   |        | Location 10   |
|     | 11              | LOC11   |        | Location 11   |
|     | 12              | LOC12   |        | Location 12   |
|     | 13              | LOC13   |        | Location 13   |
|     | 14              | LOC14   |        | Location 14   |
|     | 15              | LOC15   |        | Location 15   |
|     | 16              | LOC16   |        | Location 16   |
|     | 17              | LOC17   |        | Location 17   |
|     | 18              | LOC18   |        | Location 18   |
|     | 19              | LOC19   |        | Location 19   |
|     | 20              | LOC20   |        | Location 20   |
|     | 21              | LOC21   |        | Location 21   |
|     | 22              | LOC22   |        | Location 22   |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
| 23  |      | LOC23 |        | Location 23 |
| 24  |      | LOC24 |        | Location 24 |
| 25  |      | LOC25 |        | Location 25 |
| 26  |      | LOC26 |        | Location 26 |
| 27  |      | LOC27 |        | Location 27 |
| 28  |      | LOC28 |        | Location 28 |
| 29  |      | LOC29 |        | Location 29 |
| 30  |      | LOC30 |        | Location 30 |
| 31  |      | LOC31 |        | Location 31 |

## 20. LEUART - Low Energy Universal Asynchronous Receiver/Transmitter



### Quick Facts

#### What?

The LEUART provides full UART communication using a low frequency 32.768 kHz clock, and has special features for communication without CPU intervention.

#### Why?

It allows UART communication to be performed in low energy modes, using only a few  $\mu\text{A}$  during active communication and only 150 nA when waiting for incoming data.

#### How?

A low frequency clock signal allows communication with less energy. Using DMA, the LEUART can transmit and receive data with minimal CPU intervention. Special UART-frames can be configured to help control the data flow, further automating data transmission.

### 20.1 Introduction

The unique Low Energy UART (LEUART) is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud.

Even when the system is in low energy mode EM2 Deep Sleep (with most core functionality turned off), the LEUART can wait for an incoming UART frame while having an extremely low energy consumption. When a UART frame is completely received, the CPU can quickly be woken up. Alternatively, multiple frames can be transferred via the Direct Memory Access (DMA) module into RAM memory before waking up the CPU.

Received data can optionally be blocked until a configurable start frame is detected. A signal frame can be configured to generate an interrupt indicating the end of a data transmission. The start frame and signal frame can be used in combination to handle higher level communication protocols.

Similarly, data can be transmitted in EM2 Deep Sleep either on a frame-by-frame basis with data from the CPU or through use of the DMA.

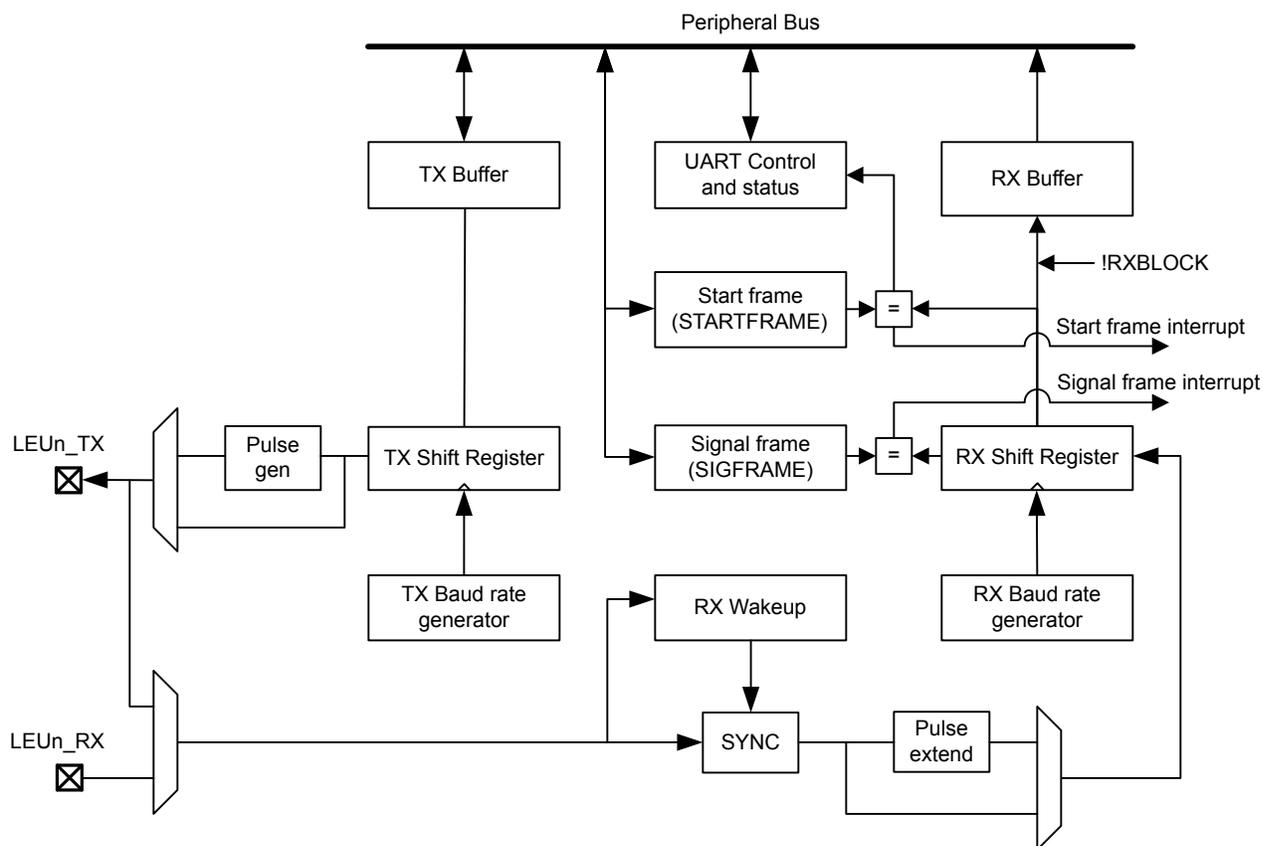
The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimal software overhead and low energy consumption.

## 20.2 Features

- Low energy asynchronous serial communications
- Full/half duplex communication
- Separate TX / RX enable
- Separate double buffered transmit buffer and receive buffer
- Programmable baud rate, generated as a fractional division of the LFBCLK
  - Supports baud rates from 300 baud to 9600 baud
- Can use a high frequency clock source for even higher baud rates
- Configurable number of data bits: 8 or 9 (plus parity bit, if enabled)
- Configurable parity: off, even or odd
  - HW parity bit generation and check
- Configurable number of stop bits, 1 or 2
- Capable of sleep-mode wake-up on received frame
  - Either wake-up on any received byte or
  - Wake up only on specified start and signal frames
- Supports transmission and reception in EM0 Active, EM1 Sleep and EM2 Deep Sleep with
  - Full DMA support
  - Specified start-frame can start reception automatically
- IrDA modulator (pulse generator, pulse extender)
- Multi-processor mode
- Loopback mode
  - Half duplex communication
  - Communication debugging
- PRS RX input

### 20.3 Functional Description

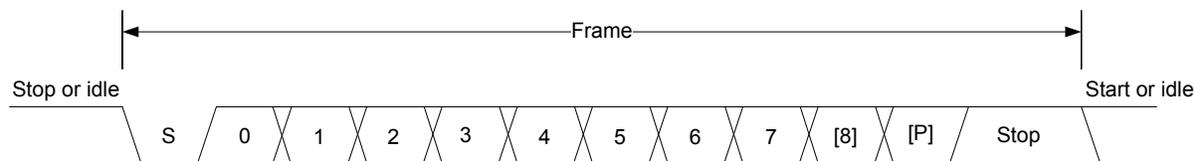
An overview of the LEUART module is shown in [Figure 20.1 LEUART Overview on page 658](#).



**Figure 20.1. LEUART Overview**

### 20.3.1 Frame Format

The frame format used by the LEUART consists of a set of data bits in addition to bits for synchronization and optionally a parity bit for error checking. A frame starts with one start-bit (S), where the line is driven low for one bit-period. This signals the start of a frame, and is used for synchronization. Following the start bit are 8 or 9 data bits and an optional parity bit. The data is transmitted with the least significant bit first. Finally, a number of stop-bits, where the line is driven high, end the frame. The frame format is shown in [Figure 20.2 LEUART Asynchronous Frame Format on page 659](#).



**Figure 20.2. LEUART Asynchronous Frame Format**

The number of data bits in a frame is set by DATABITS in LEUARTn\_CTRL, and the number of stop-bits is set by STOPBITS in LEUARTn\_CTRL. Whether or not a parity bit should be included, and whether it should be even or odd is defined by PARITY in LEUARTn\_CTRL. For communication to be possible, all parties of an asynchronous transfer must agree on the frame format being used.

The frame format used by the LEUART can be inverted by setting INV in LEUARTn\_CTRL. This affects the entire frame, resulting in a low idle state, a high start-bit, inverted data and parity bits, and low stop-bits. INV should only be changed while the receiver is disabled.

#### 20.3.1.1 Parity Bit Calculation and Handling

Hardware automatically inserts parity bits into outgoing frames and checks the parity bits of incoming frames. The possible parity modes are defined in [Table 20.1 LEUART Parity Bit on page 659](#). When even parity is chosen, a parity bit is inserted to make the number of high bits (data + parity) even. If odd parity is chosen, the parity bit makes the total number of high bits odd. When parity bits are disabled, which is the default configuration, the parity bit is omitted.

**Table 20.1. LEUART Parity Bit**

| PARITY [1:0] | Description         |
|--------------|---------------------|
| 00           | No parity (default) |
| 01           | Reserved            |
| 10           | Even parity         |
| 11           | Odd parity          |

See [20.3.5.4 Parity Error](#) for more information on parity bit handling.

### 20.3.2 Clock Source

The LEUART clock source is selected by the LFB bit field the CMU\_LFBCLKSEL register. The clock is prescaled by the LEUARTn bitfield in the CMU\_LFBPRESC0 register and enabled by the LEUARTn bit in the CMU\_LFBCLKEN0. See [Figure 12.2 CMU Overview - Low Frequency Portion on page 319](#) for a diagram of the clocking structure.

To use this module, the LE interface clock must be enabled in CMU\_HFBUSCLKEN0, in addition to the module clock.

### 20.3.3 Clock Generation

The LEUART clock defines the transmission and reception data rate. The clock generator employs a fractional clock divider to allow baud rates that are not attainable by integral division of the 32.768 kHz clock that drives the LEUART.

The clock divider used in the LEUART is a 14-bit value, with a 9-bit integral part and a 5-bit fractional part. The baud rate of the LEUART is given by :

$$br = f_{LEUARTn} / (1 + LEUARTn\_CLKDIV / 256)$$

**Figure 20.3. LEUART Baud Rate Equation**

where  $f_{LEUARTn}$  is the clock frequency supplied to the LEUART. The value of  $LEUARTn\_CLKDIV$  thus defines the baud rate of the LEUART. The integral part of the divider is right-aligned in the upper 24 bits of  $LEUARTn\_CLKDIV$  and the fractional part is left-aligned in the lower 8 bits. The divider is thus a 256th of  $LEUARTn\_CLKDIV$  as seen in the equation.

As an example let us assume  $f_{LEUART} = 22.5$  kHz and the value of  $DIV$  in  $LEUARTn\_CLKDIV$  is  $0x0028$  ( $LEUARTn\_CLKDIV = 0x00000140$ ). The baud rate =  $22.5$  kHz /  $(1 + 0x140 / 256) = 22.5$  kHz /  $2.25 = 10$  kHz.

For a desired baud rate  $br_{DESIRED}$ ,  $LEUARTn\_CLKDIV$  can be calculated by using:

$$LEUARTn\_CLKDIV = 256 \times (f_{LEUARTn} / br_{DESIRED} - 1)$$

**Figure 20.4. LEUART CLKDIV Equation**

It's important to note that this equation results in a 32bit value for the  $LEUARTn\_CLKDIV$  register but only bits [16:3] are valid and all others must be 0. For example if we have a 32 kHz clock and wish to achieve a baud rate of 10 kHz the equation above results in a  $LEUARTn\_CLKDIV$  value of  $0x233$ . However, the actual value of the register will be  $0x230$  since bits [2:0] cannot be set. This limits the best achievable accuracy. In this example the actual baud rate will be  $32$  kHz /  $(1 + 0x230 / 255) = 10.039$  kHz instead of  $32$  kHz /  $(1 + 0x233 / 255) = 10.002$  kHz.

[Table 20.2 LEUART Baud Rates on page 660](#) lists a set of desired baud rates and the closest baud rates reachable by the LEUART with a 32.768 kHz clock source. It also shows the average baud rate error.

**Table 20.2. LEUART Baud Rates**

| Desired baud rate | LEUARTn_CLKDIV | LEUARTn_CLKDIV/256 | Actual Baud Rate | Error [%] |
|-------------------|----------------|--------------------|------------------|-----------|
| 300               | 27704          | 108.21875          | 300.0217         | 0.01      |
| 600               | 13728          | 53.625             | 599.8719         | -0.02     |
| 1200              | 6736           | 26.3125            | 1199.744         | -0.02     |
| 2400              | 3240           | 12.65625           | 2399.487         | -0.02     |
| 4800              | 1488           | 5.8125             | 4809.982         | 0.21      |
| 9600              | 616            | 2.40625            | 9619.963         | 0.21      |

### 20.3.4 Data Transmission

Data transmission is initiated by writing data to the transmit buffer using one of the methods described in [20.3.4.1 Transmit Buffer Operation](#). When the transmit shift register is empty and ready for new data, a frame from the transmit buffer is loaded into the shift register, and if the transmitter is enabled, transmission begins. When the frame has been transmitted, a new frame is loaded into the shift register if available, and transmission continues. If the transmit buffer is empty, the transmitter goes to an idle state, waiting for a new frame to become available. Transmission is enabled through the command register  $LEUARTn\_CMD$  by setting  $TXEN$ , and disabled by setting  $TXDIS$ . When the transmitter is disabled using  $TXDIS$ , any ongoing transmission is aborted, and any frame currently being transmitted is discarded. When disabled, the TX output goes to an idle state, which by default is a high value. Whether or not the transmitter is enabled at a given time can be read from  $TXENS$  in  $LEUARTn\_STATUS$ . After a transmission, when there is no more data in the shift register or transmit buffer, the  $TXC$  flag in  $LEUARTn\_STATUS$  and the  $TXC$  interrupt flag in  $LEUARTn\_IF$  are set, signaling that the transmitter is idle. The  $TXC$  status flag is cleared when a new byte becomes available for transmission, but the  $TXC$  interrupt flag must be cleared by software.

### 20.3.4.1 Transmit Buffer Operation

A frame can be loaded into the transmit buffer by writing to LEUARTn\_TXDATA or LEUARTn\_TXDATAX. Using LEUARTn\_TXDATA allows 8 bits to be written to the buffer. If 9 bit frames are used, the 9th bit will in that case be set to the value of BIT8DV in LEUARTn\_CTRL. To set the 9th bit directly and/or use transmission control, LEUARTn\_TXDATAX must be used. When writing data to the transmit buffer using LEUARTn\_TXDATAX, the 9th bit written to LEUARTn\_TXDATAX overrides the value in BIT8DV, and alone defines the 9th bit that is transmitted if 9-bit frames are used.

If a write is attempted to the transmit buffer when it is not empty, the TXOF interrupt flag in LEUARTn\_IF is set, indicating the overflow. The data already in the buffer is in that case preserved, and no data is written.

In addition to the interrupt flag TXC in LEUARTn\_IF and the status flag TXC in LEUARTn\_STATUS which are set when the transmitter becomes idle, TXBL in LEUARTn\_STATUS and the TXBL interrupt flag in LEUARTn\_IF are used to indicate the level of the transmit buffer. Whenever the transmit buffer becomes empty, these flags are set high. Both the TXBL status flag and the TXBL interrupt flag are cleared automatically when data is written to the transmit buffer.

There is also TXIDLE status in LEUART\_STATUS which can be used to detect when the transmit state machine is in the idle state.

The transmit buffer, including the TX shift register can be cleared by setting command bit CLEARTX in LEUARTn\_CMD. This will prevent the LEUART from transmitting the data in the buffer and shift register, and will make them available for new data. Any frame currently being transmitted will not be aborted. Transmission of this frame will be completed. An overview of the operation of the transmitter is shown in [Figure 20.5 LEUART Transmitter Overview on page 661](#).

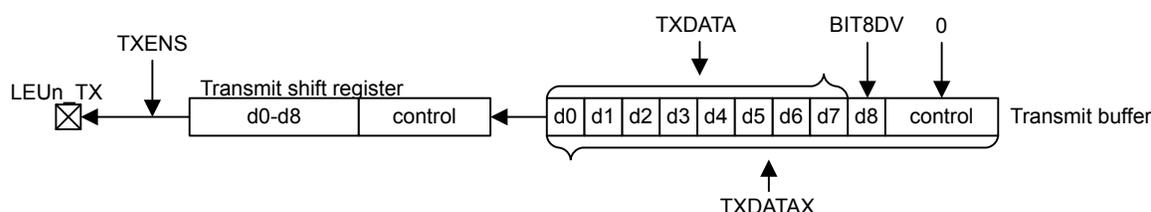


Figure 20.5. LEUART Transmitter Overview

### 20.3.4.2 Frame Transmission Control

The transmission control bits, which can be written using LEUARTn\_TXDATAX, affect the transmission of the written frame. The following options are available:

- **Generate break:** By setting TXBREAK, the output will be held low during the first stop-bit period to generate a framing error. A receiver that supports break detection detects this state, allowing it to be used e.g. for framing of larger data packets. The line is driven high for one bit period before the next frame is transmitted so the next start condition can be identified correctly by the recipient. Continuous breaks lasting longer than an UART frame are thus not supported by the LEUART. GPIO can be used for this. Note that when AUTOTRI in LEUARTn\_CTRL is used, the transmitter is not tristated before the high-bit after the break has been transmitted.
- **Disable transmitter after transmission:** If TXDISAT is set, the transmitter is disabled after the frame has been fully transmitted.
- **Enable receiver after transmission:** If RXENAT is set, the receiver is enabled after the frame has been fully transmitted. It is enabled in time to detect a start-bit directly after the last stop-bit has been transmitted.

The transmission control bits in the LEUART cannot tristate the transmitter. This is performed automatically by hardware if AUTOTRI in LEUARTn\_CTRL is set. See [20.3.7 Half Duplex Communication](#) for more information on half duplex operation.

### 20.3.5 Data Reception

Data reception is enabled by setting RXEN in LEUARTn\_CMD. When the receiver is enabled, it actively samples the input looking for a transition from high to low indicating the start bit of a new frame. When a start bit is found, reception of the new frame begins if the receive shift register is empty and ready for new data. When the frame has been received, it is pushed into the receive buffer, making the shift register ready for another frame of data, and the receiver starts looking for another start bit. If the receive buffer is full, the received frame remains in the shift register until more space in the receive buffer is available.

If an incoming frame is detected while both the receive buffer and the receive shift register are full, the data in the receive shift register is overwritten, and the RXOF interrupt flag in LEUARTn\_IF is set to indicate the buffer overflow.

The receiver can be disabled by setting the command bit RXDIS in LEUARTn\_CMD. Any frame currently being received when the receiver is disabled is discarded. Whether or not the receiver is enabled at a given time can be read out from RXENS in LEUARTn\_STATUS.

The receive buffer can be cleared by setting command bit CLEARRX in LEUARTn\_CMD. This will make it available for new data. Any frame currently being received will not be aborted and will become the first received frame when complete.

#### 20.3.5.1 Receive Buffer Operation

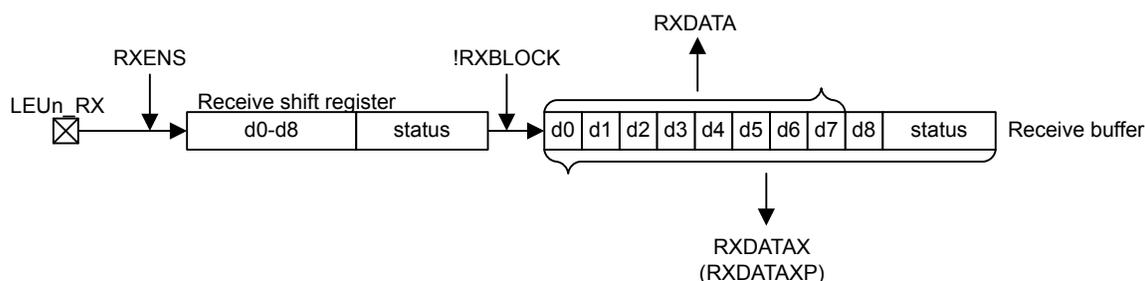
When data becomes available in the receive buffer, the RXDATAV flag in LEUARTn\_STATUS and the RXDATAV interrupt flag in LEUARTn\_IF are set. Both the RXDATAV status flag and the RXDATAV interrupt flag are cleared by hardware when data is no longer available, i.e. when data has been read out of the buffer.

Data can be read from receive buffer using either LEUARTn\_RXDATA or LEUARTn\_RXDATAx. LEUARTn\_RXDATA gives access to the 8 least significant bits of the received frame, while LEUARTn\_RXDATAx must be used to get access to the 9th, most significant bit. The LEUARTn\_RXDATAx register also contains status information regarding the frame.

When a frame is read from the receive buffer using LEUARTn\_RXDATA or LEUARTn\_RXDATAx, the frame is removed from the buffer, making room for a new one. If an attempt is done to read more frames from the buffer than what is available, the RXUF interrupt flag in LEUARTn\_IF is set to signal the underflow, and the data read from the buffer is undefined.

Frames can also be read from the receive buffer without removing the data by using LEUARTn\_RXDATAxp, which gives access to the frame in the buffer including control bits. Data read from this register when the receive buffer is empty is undefined. No underflow interrupt is generated by a read using LEUARTn\_RXDATAxp, i.e. the RXUF interrupt flag is never set as a result of reading from LEUARTn\_RXDATAxp.

An overview of the operation of the receiver is shown in [Figure 20.6 LEUART Receiver Overview on page 662](#).



**Figure 20.6. LEUART Receiver Overview**

### 20.3.5.2 Blocking Incoming Data

When using hardware frame recognition, as detailed in [20.3.5.6 Programmable Start Frame](#), [20.3.5.7 Programmable Signal Frame](#), and [20.3.5.8 Multi-Processor Mode](#), it is necessary to be able to let the receiver sample incoming frames without passing the frames to software by loading them into the receive buffer. This is accomplished by blocking incoming data.

Incoming data is blocked as long as RXBLOCK in LEUARTn\_STATUS is set. When blocked, frames received by the receiver will not be loaded into the receive buffer, and software is not notified by the RXDATAV bit in LEUARTn\_STATUS or the RXDATAV interrupt flag in LEUARTn\_IF at their arrival. For data to be loaded into the receive buffer, RXBLOCK must be cleared in the instant a frame is fully received by the receiver. RXBLOCK is set by setting RXBLOCKEN in LEUARTn\_CMD and disabled by setting RXBLOCKDIS also in LEUARTn\_CMD. There are two exceptions where data is loaded into the receive buffer even when RXBLOCK is set. The first is when an address frame is received when in operating in multi-processor mode as shown in [20.3.5.8 Multi-Processor Mode](#). The other case is when receiving a start-frame when SFUBRX in LEUARTn\_CTRL is set; see [20.3.5.6 Programmable Start Frame](#)

Frames received containing framing or parity errors will not result in the FERR and PERR interrupt flags in LEUARTn\_IF being set while RXBLOCK is set. Hardware recognition is not applied to these erroneous frames, and they are silently discarded.

#### Note:

- If a frame is received while RXBLOCK in LEUARTn\_STATUS is cleared, but stays in the receive shift register because the receive buffer is full, the received frame will be loaded into the receive buffer when space becomes available even if RXBLOCK is set at that time.
- The overflow interrupt flag RXOF in LEUARTn\_IF will be set if a frame in the receive shift register, waiting to be loaded into the receive buffer is overwritten by an incoming frame even though RXBLOCK is set.

### 20.3.5.3 Data Sampling

The receiver samples each incoming bit as close as possible to the middle of the bit-period. Except for the start-bit, only a single sample is taken of each of the incoming bits.

The length of a bit-period is given by  $1 + \text{LEUARTn\_CLKDIV}/256$ , as a number of 32.768 kHz clock periods. Let the clock cycle where a start-bit is first detected be given the index 0. The optimal sampling point for each bit in the UART frame is then given by the following equation:

$$S_{\text{opt}}(n) = n (1 + \text{LEUARTn\_CLKDIV}/256) + \text{LEUARTn\_CLKDIV}/512$$

**Figure 20.7. LEUART Optimal Sampling Point**

where n is the bit-index.

Since samples are only done on the positive edges of the 32.768 kHz clock, the actual samples are performed on the closest positive edge, i.e. the edge given by the following equation:

$$S(n) = \text{floor}(n \times (1 + \text{LEUARTn\_CLKDIV}/256) + \text{LEUARTn\_CLKDIV}/512)$$

**Figure 20.8. LEUART Actual Sampling Point**

The sampling location will thus have jitter according to difference between  $S_{\text{opt}}$  and S. The start-bit is found at  $n=0$ , then follows the data bits, any parity bit, and the stop bits.

If the value of the start-bit is found to be high, then the start-bit is discarded, and the receiver waits for a new start-bit.

### 20.3.5.4 Parity Error

When the parity bit is enabled, a parity check is automatically performed on incoming frames. When a parity error is detected in a frame, the data parity error bit PERR in the frame is set, as well as the interrupt flag PERR. Frames with parity errors are loaded into the receive buffer like regular frames.

PERR can be accessed by reading the frame from the receive buffer using the LEUARTn\_RXDATA register.

### 20.3.5.5 Framing Error and Break Detection

A framing error is the result of a received frame where the stop bit was sampled to a value of 0. This can be the result of noise and baud rate errors, but can also be the result of a break generated by the transmitter on purpose.

When a framing error is detected, the framing error bit FERR in the received frame is set. The interrupt flag FERR in LEUARTn\_IF is also set. Frames with framing errors are loaded into the receive buffer like regular frames.

FERR can be accessed by reading the frame from the receive buffer using the LEUARTn\_RXDATA or LEUARTn\_RXDATAEXP registers.

### 20.3.5.6 Programmable Start Frame

The LEUART can be configured to start receiving data when a special start frame is detected on the input. This can be useful when operating in low energy modes, allowing other devices to gain the attention of the LEUART by transmitting a given frame.

When SFUBRX in LEUARTn\_CTRL is set, an incoming frame matching the frame defined in LEUARTn\_STARTFRAME will result in RXBLOCK in LEUARTn\_STATUS being cleared. This can be used to enable reception when a specified start frame is detected. If the receiver is enabled and blocked, i.e. RXENS and RXBLOCK in LEUARTn\_STATUS are set, the receiver will receive all incoming frames, but unless an incoming frame is a start frame it will be discarded and not loaded into the receive buffer. When a start frame is detected, the block is cleared, and frames received from that point, including the start frame, are loaded into the receive buffer.

An incoming start frame results in the STARTF interrupt flag in LEUARTn\_IF being set, regardless of the value of SFUBRX in LEUARTn\_CTRL. This allows an interrupt to be made when the start frame is detected.

When 8 data-bit frame formats are used, only the 8 least significant bits of LEUARTn\_STARTFRAME are compared to incoming frames. The full length of LEUARTn\_STARTFRAME is used when operating with frames consisting of 9 data bits.

**Note:** The receiver must be enabled for start frames to be detected. In addition, a start frame with a parity error or framing error is not detected as a start frame.

### 20.3.5.7 Programmable Signal Frame

As well as the configurable start frame, a special signal frame can be specified. When a frame matching the frame defined in LEUARTn\_SIGFRAME is detected by the receiver, the SIGF interrupt flag in LEUARTn\_IF is set. As for start frame detection, the receiver must be enabled for signal frames to be detected.

One use of the programmable signal frame is to signal the end of a multi-frame message transmitted to the LEUART. An interrupt will then be triggered when the packet has been completely received, allowing software to process it. Used in conjunction with the programmable start frame and DMA, this makes it possible for the LEUART to automatically begin the reception of a packet on a specified start frame, load the entire packet into memory, and give an interrupt when reception of a packet has completed. The device can thus wait for data packets in EM2 Deep Sleep, and only be woken up when a packet has been completely received.

A signal frame with a parity error or framing error is not detected as a signal frame.

### 20.3.5.8 Multi-Processor Mode

To simplify communication between multiple processors and maintain compatibility with the USART, the LEUART supports a multi-processor mode. In this mode the 9th data bit in each frame is used to indicate whether the content of the remaining 8 bits is data or an address.

When multi-processor mode is enabled, an incoming 9-bit frame with the 9th bit equal to the value of MPAB in LEUARTn\_CTRL is identified as an address frame. When an address frame is detected, the MPAF interrupt flag in LEUARTn\_IF is set, and the address frame is loaded into the receive register. This happens regardless of the value of RXBLOCK in LEUARTn\_STATUS.

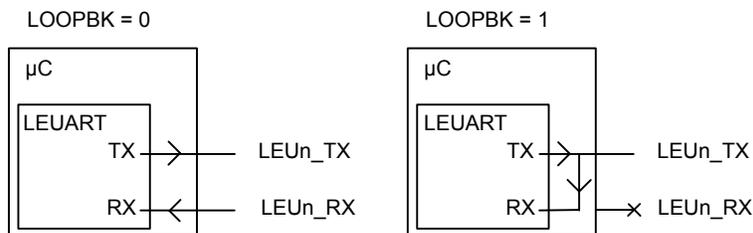
Multi-processor mode is enabled by setting MPM in LEUARTn\_CTRL. The mode can be used in buses with multiple slaves, allowing the slaves to be addressed using the special address frames. An addressed slave, which was previously blocking reception using RXBLOCK, would then unblock reception, receive a message from the bus master, and then block reception again, waiting for the next message. See the USART for a more detailed example.

**Note:** The programmable start frame functionality can be used for automatic address matching, enabling reception on a correctly configured incoming frame.

An address frame with a parity error or a framing error is not detected as an address frame. The Start, Signal, and address frames should not be set to match the same frame since each of these uses separate synchronization to the peripheral clock domain.

### 20.3.6 Loopback

The LEUART receiver samples LEUn\_RX by default, and the transmitter drives LEUn\_TX by default. This is not the only configuration however. When LOOPBK in LEUARTn\_CTRL is set, the receiver is connected to the LEUn\_TX pin as shown in [Figure 20.9 LEUART Local Loopback on page 665](#). This is useful for debugging, as the LEUART can receive the data it transmits, but it is also used to allow the LEUART to read and write to the same pin, which is required for some half duplex communication modes. In this mode, the LEUn\_TX pin must be enabled as an output in the GPIO.



**Figure 20.9. LEUART Local Loopback**

### 20.3.7 Half Duplex Communication

When doing full duplex communication, two data links are provided, making it possible for data to be sent and received at the same time. In half duplex mode, data is only sent in one direction at a time. There are several possible half duplex setups, as described in the following sections.

#### 20.3.7.1 Single Data-link

In this setup, the LEUART both receives and transmits data on the same pin. This is enabled by setting LOOPBK in LEUARTn\_CTRL, which connects the receiver to the transmitter output. Because they are both connected to the same line, it is important that the LEUART transmitter does not drive the line when receiving data, as this would corrupt the data on the line.

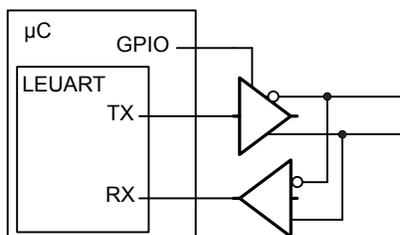
When communicating over a single data-link, the transmitter must thus be tristated whenever not transmitting data. If AUTOTRI in LEUARTn\_CTRL is set, the LEUART automatically tristates LEUn\_TX whenever the transmitter is inactive. It is then the responsibility of the software protocol to make sure the transmitter is not transmitting data whenever incoming data is expected.

The transmitter can also be tristated from software by configuring the GPIO pin as an input and disabling the LEUART output on LEUn\_TX.

**Note:** Another way to tristate the transmitter is to enable wired-and or wired-or mode in GPIO. For wired-and mode, outputting a 1 will be the same as tristating the output, and for wired-or mode, outputting a 0 will be the same as tristating the output. This can only be done on buses with a pull-up or pull-down resistor respectively.

### 20.3.7.2 Single Data-link With External Driver

Some communication schemes, such as RS-485 rely on an external driver. Here, the driver has an extra input which enables it, and instead of Tristating the transmitter when receiving data, the external driver must be disabled. The USART has hardware support for automatically turning the driver on and off. When using the LEUART in such a setup, the driver must be controlled by a GPIO. [Figure 20.10 LEUART Half Duplex Communication with External Driver](#) on page 666 shows an example configuration using an external driver.



**Figure 20.10. LEUART Half Duplex Communication with External Driver**

### 20.3.7.3 Two Data-links

Some limited devices only support half duplex communication even though two data links are available. In this case software is responsible for making sure data is not transmitted when incoming data is expected.

### 20.3.8 Transmission Delay

By configuring TXDELAY in LEUARTn\_CTRL, the transmitter can be forced to wait a number of bit-periods from when it is ready to transmit data, to when it actually transmits the data. This delay is only applied to the first frame transmitted after the transmitter has been idle. When transmitting frames back-to-back the delay is not introduced between the transmitted frames.

This is useful on half duplex buses, because the receiver always returns received frames to software during the first stop-bit. The bus may still be driven for up to 3 bit periods, depending on the current frame format. Using the transmission delay, a transmission can be started when a frame is received, and it is possible to make sure that the transmitter does not begin driving the output before the frame on the bus is completely transmitted.

To route the UART TX and RX signals to a pin first select the desired pins using the RXLOC and TXLOC fields in the LEUARTn\_ROUTELOC0 register. Then enable the connection using TXPEN and RXPEN in the LEUARTn\_ROUTEPEN register. See the device data sheet for mappings between UART locations (LOC0, LOC1, etc.) and device pins (PA0, PA1, etc.).

### 20.3.9 PRS RX Input

In addition to receiving data on an external pin the LEUART can be configured to receive data directly from a PRS channel by setting RX\_PRS in LEUARTn\_INPUT. The PRS channel used can be selected using RX\_PRS\_SEL in LEUARTn\_INPUT. See the PRS chapter for more details on the PRS block.

For example the output of a comparator could be routed to the LEUART through the PRS to allow for receiving a signal with low peak-to-peak voltage or a significant DC offset.

### 20.3.10 DMA Support

The LEUART has full DMA support in energy modes EM0 Active – EM2 Deep Sleep. The DMA controller can write to the transmit buffer using the registers LEUARTn\_TXDATA and LEUARTn\_TXDATAx, and it can read from receive buffer using the registers LEUARTn\_RXDATA and LEUARTn\_RXDATAx. This enables single byte transfers and 9 bit data + control/status bits transfers both to and from the LEUART. The DMA will start up the HFRCO and run from this when it is waken by the LEUART in EM2. The HFRCO is disabled once the transaction is done.

A request for the DMA controller to read from the receive buffer can come from one of the following sources:

- Receive buffer full

A write request can come from one of the following sources:

- Transmit buffer and shift register empty. No data to send.
- Transmit buffer empty

In some cases, it may be sensible to temporarily stop DMA access to the LEUART when a parity or framing error has occurred. This is enabled by setting ERRSDMA in LEUARTn\_CTRL. When this bit is set, the DMA controller will not get requests from the receive buffer if a framing error or parity error is detected in the received byte. The ERRSDMA bit applies only to the RX DMA.

When operating in EM2 Deep Sleep, the DMA controller must be powered up in order to perform the transfer. This is automatically performed for read operations if RXDMAWU in LEUARTn\_CTRL is set and for write operations if TXDMAWU in LEUARTn\_CTRL is set. To make sure the DMA controller still transfers bits to and from the LEUART in low energy modes, these bits must thus be configured accordingly.

**Note:** When RXDMAWU or TXDMAWU is set, the system will not be able to go to EM2 Deep Sleep/EM3 Stop before all related LEUART DMA requests have been processed. This means that if RXDMAWU is set and the LEUART receives a frame, the system will not be able to go to EM2 Deep Sleep/EM3 Stop before the frame has been read from the LEUART. In order for the system to go to EM2 during the last byte transmission, LEUARTn\_CTRL\_TXDMAWU must be cleared in the DMA interrupt service routine. This is because TXBL will be high during that last byte transfer.

### 20.3.11 Pulse Generator/ Pulse Extender

The LEUART has an optional pulse generator for the transmitter output, and a pulse extender on the receiver input. These are enabled by setting PULSEEN in LEUARTn\_PULSECTRL, and with INV in LEUARTn\_CTRL set, they will change the output/input format of the LEUART from NRZ to RZI as shown in [Figure 20.11 LEUART - NRZ vs. RZI on page 667](#).

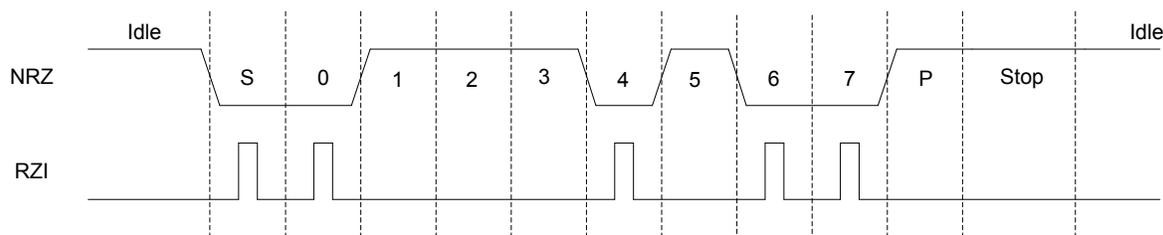


Figure 20.11. LEUART - NRZ vs. RZI

If PULSEEN in LEUARTn\_PULSECTRL is set while INV in LEUARTn\_CTRL is cleared, the output waveform will look like RZI shown in [Figure 20.11 LEUART - NRZ vs. RZI on page 667](#), only inverted.

The width of the pulses from the pulse generator can be configured using PULSEW in LEUARTn\_PULSECTRL. The generated pulse width is PULSEW + 1 cycles of the 32.768 kHz clock, which makes pulse width from 31.25µs to 500µs possible.

Since the incoming signal is only sampled on positive clock edges, the width of the incoming pulses must be at least two 32.768 kHz clock periods wide for reliable detection by the LEUART receiver. They must also be shorter than half a UART bit period.

At 2400 baud or lower, the pulse generator is able to generate RZI pulses compatible with the IrDA physical layer specification. The external IrDA device must generate pulses of sufficient length for successful two-way communication.

PULSEFILT in the LEUARTn\_PULSECTRL register can be used to extend the minimum receive pulse width from 2 clock periods to 3 clock periods.

### 20.3.11.1 Interrupts

The interrupts generated by the LEUART are combined into one interrupt vector. If LEUART interrupts are enabled, an interrupt will be made if one or more of the interrupt flags in LEUARTn\_IF and their corresponding bits in LEUART\_IEN are set.

### 20.3.12 Register Access

Since this module is a Low Energy Peripheral, and runs off a clock which is asynchronous to the HFCORECLK, special considerations must be taken when accessing registers. Refer to [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#) for a description on how to perform register accesses to Low Energy Peripherals.

The registers LEUARTn\_FREEZE and LEUARTn\_SYNCBUSY are used for synchronization of this peripheral.

## 20.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name               | Type  | Description                                |
|--------|--------------------|-------|--|
| 0x000  | LEUARTn_CTRL       | RW    | Control Register                           |
| 0x004  | LEUARTn_CMD        | W1    | Command Register                           |
| 0x008  | LEUARTn_STATUS     | R     | Status Register                            |
| 0x00C  | LEUARTn_CLKDIV     | RW    | Clock Control Register                     |
| 0x010  | LEUARTn_STARTFRAME | RW    | Start Frame Register                       |
| 0x014  | LEUARTn_SIGFRAME   | RW    | Signal Frame Register                      |
| 0x018  | LEUARTn_RXDATAx    | R(a)  | Receive Buffer Data Extended Register      |
| 0x01C  | LEUARTn_RXDATA     | R(a)  | Receive Buffer Data Register               |
| 0x020  | LEUARTn_RXDATAxP   | R     | Receive Buffer Data Extended Peek Register |
| 0x024  | LEUARTn_TXDATAx    | W     | Transmit Buffer Data Extended Register     |
| 0x028  | LEUARTn_TXDATA     | W     | Transmit Buffer Data Register              |
| 0x02C  | LEUARTn_IF         | R     | Interrupt Flag Register                    |
| 0x030  | LEUARTn_IFS        | W1    | Interrupt Flag Set Register                |
| 0x034  | LEUARTn_IFC        | (R)W1 | Interrupt Flag Clear Register              |
| 0x038  | LEUARTn_IEN        | RW    | Interrupt Enable Register                  |
| 0x03C  | LEUARTn_PULSECTRL  | RW    | Pulse Control Register                     |
| 0x040  | LEUARTn_FREEZE     | RW    | Freeze Register                            |
| 0x044  | LEUARTn_SYNCBUSY   | R     | Synchronization Busy Register              |
| 0x054  | LEUARTn_ROUTEPEEN  | RW    | I/O Routing Pin Enable Register            |
| 0x058  | LEUARTn_ROUTELOC0  | RW    | I/O Routing Location Register              |
| 0x064  | LEUARTn_INPUT      | RW    | LEUART Input Register                      |

## 20.5 Register Description

### 20.5.1 LEUARTn\_CTRL - Control Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |         |         |        |      |     |        |        |         |     |          |        |          |         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|---------|---------|--------|------|-----|--------|--------|---------|-----|----------|--------|----------|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0x000         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14      | 13      | 12     | 11   | 10  | 9      | 8      | 7       | 6   | 5        | 4      | 3        | 2       | 1  | 0  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0     | 0       | 0       | 0      | 0    | 0   | 0      | 0      | 0       | 0   | 0        | 0      | 0        | 0       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |    |    |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      | RW      | RW      | RW     | RW   | RW  | RW     | RW     | RW      | RW  | RW       | RW     | RW       | RW      | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | TXDELAY | TXDMAWU | RXDMAWU | BIT8DV | MPAB | MPM | SFUBRX | LOOPBK | ERRSDMA | INV | STOPBITS | PARITY | DATABITS | AUTOTRI |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

| Bit   | Name  | Reset   | Access | Description   |       |             |             |   |      |  |   |        |   |   |        |   |   |        |   |
|-------|---|---|--------|---|-------|-------------|-------------|---|------|--|---|--------|---|---|--------|---|---|--------|---|
| 31:16 | <i>Reserved</i>   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |             |             |   |      |  |   |        |   |   |        |   |   |        |   |
| 15:14 | TXDELAY   | 0x0   | RW     | <b>TX Delay Transmission</b><br>Configurable delay before new transfers. Frames sent back-to-back are not delayed.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>NONE</td> <td>Frames are transmitted immediately</td> </tr> <tr> <td>1</td> <td>SINGLE</td> <td>Transmission of new frames are delayed by a single bit period</td> </tr> <tr> <td>2</td> <td>DOUBLE</td> <td>Transmission of new frames are delayed by two bit periods</td> </tr> <tr> <td>3</td> <td>TRIPLE</td> <td>Transmission of new frames are delayed by three bit periods</td> </tr> </tbody> </table> | Value | Mode        | Description | 0   | NONE | Frames are transmitted immediately   | 1 | SINGLE | Transmission of new frames are delayed by a single bit period | 2 | DOUBLE | Transmission of new frames are delayed by two bit periods | 3 | TRIPLE | Transmission of new frames are delayed by three bit periods |
| Value | Mode  | Description   |        |   |       |             |             |   |      |  |   |        |   |   |        |   |   |        |   |
| 0     | NONE  | Frames are transmitted immediately  |        |   |       |             |             |   |      |  |   |        |   |   |        |   |   |        |   |
| 1     | SINGLE  | Transmission of new frames are delayed by a single bit period   |        |   |       |             |             |   |      |  |   |        |   |   |        |   |   |        |   |
| 2     | DOUBLE  | Transmission of new frames are delayed by two bit periods   |        |   |       |             |             |   |      |  |   |        |   |   |        |   |   |        |   |
| 3     | TRIPLE  | Transmission of new frames are delayed by three bit periods   |        |   |       |             |             |   |      |  |   |        |   |   |        |   |   |        |   |
| 13    | TXDMAWU   | 0   | RW     | <b>TX DMA Wakeup</b><br>Set to wake the DMA controller up when in EM2 and space is available in the transmit buffer.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>While in EM2, the DMA controller will not get requests about space being available in the transmit buffer</td> </tr> <tr> <td>1</td> <td>DMA is available in EM2 for the request about space available in the transmit buffer</td> </tr> </tbody> </table>   | Value | Description | 0           | While in EM2, the DMA controller will not get requests about space being available in the transmit buffer | 1    | DMA is available in EM2 for the request about space available in the transmit buffer |   |        |   |   |        |   |   |        |   |
| Value | Description   |   |        |   |       |             |             |   |      |  |   |        |   |   |        |   |   |        |   |
| 0     | While in EM2, the DMA controller will not get requests about space being available in the transmit buffer |   |        |   |       |             |             |   |      |  |   |        |   |   |        |   |   |        |   |
| 1     | DMA is available in EM2 for the request about space available in the transmit buffer                      |   |        |   |       |             |             |   |      |  |   |        |   |   |        |   |   |        |   |
| 12    | RXDMAWU   | 0   | RW     | <b>RX DMA Wakeup</b><br>Set to wake the DMA controller up when in EM2 and data is available in the receive buffer.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>While in EM2, the DMA controller will not get requests about data being available in the receive buffer</td> </tr> <tr> <td>1</td> <td>DMA is available in EM2 for the request about data in the receive buffer</td> </tr> </tbody> </table>   | Value | Description | 0           | While in EM2, the DMA controller will not get requests about data being available in the receive buffer   | 1    | DMA is available in EM2 for the request about data in the receive buffer             |   |        |   |   |        |   |   |        |   |
| Value | Description   |   |        |   |       |             |             |   |      |  |   |        |   |   |        |   |   |        |   |
| 0     | While in EM2, the DMA controller will not get requests about data being available in the receive buffer   |   |        |   |       |             |             |   |      |  |   |        |   |   |        |   |   |        |   |
| 1     | DMA is available in EM2 for the request about data in the receive buffer                                  |   |        |   |       |             |             |   |      |  |   |        |   |   |        |   |   |        |   |
| 11    | BIT8DV  | 0   | RW     | <b>Bit 8 Default Value</b><br>When 9-bit frames are transmitted, the default value of the 9th bit is given by BIT8DV. If TXDATA is used to write a frame, then the value of BIT8DV is assigned to the 9th bit of the outgoing frame. If a frame is written with TXDATA however, the default value is overridden by the written value.   |       |             |             |   |      |  |   |        |   |   |        |   |   |        |   |

| Bit | Name     | Reset | Access | Description   |
|-----|----------|-------|--------|---|
| 10  | MPAB     | 0     | RW     | <b>Multi-Processor Address-Bit</b><br>Defines the value of the multi-processor address bit. An incoming frame with its 9th bit equal to the value of this bit marks the frame as a multi-processor address frame. |
| 9   | MPM      | 0     | RW     | <b>Multi-Processor Mode</b><br>Set to enable multi-processor mode.  |
|     | Value    |       |        | Description   |
|     | 0        |       |        | The 9th bit of incoming frames have no special function   |
|     | 1        |       |        | An incoming frame with the 9th bit equal to MPAB will be loaded into the receive buffer regardless of RXBLOCK and will result in the MPAB interrupt flag being set  |
| 8   | SFUBRX   | 0     | RW     | <b>Start-Frame Unblock RX</b><br>Clears RXBLOCK when the start-frame is found in the incoming data. The start-frame is loaded into the receive buffer.  |
|     | Value    |       |        | Description   |
|     | 0        |       |        | Detected start-frames have no effect on RXBLOCK   |
|     | 1        |       |        | When a start-frame is detected, RXBLOCK is cleared and the start-frame is loaded into the receive buffer  |
| 7   | LOOPBK   | 0     | RW     | <b>Loopback Enable</b><br>Set to connect receiver to LEUn_TX instead of LEUn_RX.  |
|     | Value    |       |        | Description   |
|     | 0        |       |        | The receiver is connected to and receives data from LEUn_RX   |
|     | 1        |       |        | The receiver is connected to and receives data from LEUn_TX   |
| 6   | ERRSDMA  | 0     | RW     | <b>Clear RX DMA on Error</b><br>When set, RX DMA requests will be cleared on framing and parity errors.   |
|     | Value    |       |        | Description   |
|     | 0        |       |        | Framing and parity errors have no effect on DMA requests from the LEUART  |
|     | 1        |       |        | RX DMA requests from the LEUART are disabled if a framing error or parity error occurs.   |
| 5   | INV      | 0     | RW     | <b>Invert Input and Output</b><br>Set to invert the output on LEUn_TX and input on LEUn_RX.   |
|     | Value    |       |        | Description   |
|     | 0        |       |        | A high value on the input/output is 1, and a low value is 0.  |
|     | 1        |       |        | A low value on the input/output is 1, and a high value is 0.  |
| 4   | STOPBITS | 0     | RW     | <b>Stop-Bit Mode</b><br>Determines the number of stop-bits used. Only used when transmitting data. The receiver only verifies that one stop bit is present.   |
|     | Value    | Mode  |        | Description   |

| Bit | Name     | Reset | Access | Description  |
|-----|----------|-------|--------|--|
|     | 0        | ONE   |        | One stop-bit is transmitted with every frame   |
|     | 1        | TWO   |        | Two stop-bits are transmitted with every frame   |
| 3:2 | PARITY   | 0x0   | RW     | <b>Parity-Bit Mode</b><br>Determines whether parity bits are enabled, and whether even or odd parity should be used. |
|     | Value    | Mode  |        | Description  |
|     | 0        | NONE  |        | Parity bits are not used   |
|     | 2        | EVEN  |        | Even parity are used. Parity bits are automatically generated and checked by hardware.                               |
|     | 3        | ODD   |        | Odd parity is used. Parity bits are automatically generated and checked by hardware.                                 |
| 1   | DATABITS | 0     | RW     | <b>Data-Bit Mode</b><br>This register sets the number of data bits.  |
|     | Value    | Mode  |        | Description  |
|     | 0        | EIGHT |        | Each frame contains 8 data bits  |
|     | 1        | NINE  |        | Each frame contains 9 data bits  |
| 0   | AUTOTRI  | 0     | RW     | <b>Automatic Transmitter Tristate</b><br>When set, LEUn_TX is tristated whenever the transmitter is inactive.        |
|     | Value    |       |        | Description  |
|     | 0        |       |        | LEUn_TX is held high when the transmitter is inactive. INV inverts the inactive state.                               |
|     | 1        |       |        | LEUn_TX is tristated when the transmitter is inactive  |

## 20.5.2 LEUARTn\_CMD - Command Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |         |         |            |           |       |      |       |      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---------|---------|------------|-----------|-------|------|-------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8       | 7       | 6          | 5         | 4     | 3    | 2     | 1    | 0  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 0x004         |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |         |         |            |           |       |      |       |      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | 0       | 0       | 0          | 0         | 0     | 0    | 0     | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |    |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | W1      | W1      | W1         | W1        | W1    | W1   | W1    | W1   | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   | CLEARRX | CLEARTX | RXBLOCKDIS | RXBLOCKEN | TXDIS | TXEN | RXDIS | RXEN |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 31:8 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 7    | CLEARRX         | 0   | W1     | <b>Clear RX</b><br>Set to clear receive buffer and the RX shift register.   |
| 6    | CLEARTX         | 0   | W1     | <b>Clear TX</b><br>Set to clear transmit buffer and the TX shift register.  |
| 5    | RXBLOCKDIS      | 0   | W1     | <b>Receiver Block Disable</b><br>Set to clear RXBLOCK, resulting in all incoming frames being loaded into the receive buffer.                           |
| 4    | RXBLOCKEN       | 0   | W1     | <b>Receiver Block Enable</b><br>Set to set RXBLOCK, resulting in all incoming frames being discarded.   |
| 3    | TXDIS           | 0   | W1     | <b>Transmitter Disable</b><br>Set to disable transmission.  |
| 2    | TXEN            | 0   | W1     | <b>Transmitter Enable</b><br>Set to enable data transmission.   |
| 1    | RXDIS           | 0   | W1     | <b>Receiver Disable</b><br>Set to disable data reception. If a frame is under reception when the receiver is disabled, the incoming frame is discarded. |
| 0    | RXEN            | 0   | W1     | <b>Receiver Enable</b><br>Set to activate data reception on LEUn_RX.  |



### 20.5.4 LEUARTn\_CLKDIV - Clock Control Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x00C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DIV    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description   |
|-------|----------|--|--------|---|
| 31:17 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 16:3  | DIV      | 0x0000   | RW     | <b>Fractional Clock Divider</b><br><br>Specifies the fractional clock divider for the LEUART. Bits [7:3] are the fractional part and bits [16:8] are the integer part. The total divider is $([16:8] + [7:3]/32)$ . To make the math easier the total divider can also be calculated as $([16:8] + [7:0]/256)$ where bits [0:2] will always be 0. |
| 2:0   | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |

### 20.5.5 LEUARTn\_STARTFRAME - Start Frame Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x010         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x000      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | STARTFRAME |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name       | Reset  | Access | Description  |
|------|------------|--|--------|--|
| 31:9 | Reserved   | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 8:0  | STARTFRAME | 0x000  | RW     | <b>Start Frame</b><br><br>When a frame matching STARTFRAME is detected by the receiver, STARTF interrupt flag is set, and if SFUBRX is set, RXBLOCK is cleared. The start-frame is be loaded into the RX buffer. |

### 20.5.6 LEUARTn\_SIGFRAME - Signal Frame Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |          |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|----------|---|---|---|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3        | 2 | 1 | 0 |  |
| 0x014         |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |          |   |   |   |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0x000    |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | RW       |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | SIGFRAME |   |   |   |  |

| Bit  | Name     | Reset  | Access | Description  |
|------|----------|--|--------|--|
| 31:9 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 8:0  | SIGFRAME | 0x000  | RW     | <b>Signal Frame</b><br>When a frame matching SIGFRAME is detected by the receiver, SIGF interrupt flag is set. |

### 20.5.7 LEUARTn\_RXDATAx - Receive Buffer Data Extended Register (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |      |      |    |    |    |    |   |   |   |   |   |   |   |   |   |   |        |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------|------|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--------|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15   | 14   | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |        |  |
| 0x018         |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |      |      |    |    |    |    |   |   |   |   |   |   |   |   |   |   |        |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0    | 0    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | 0x000  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R    | R    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | R      |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | FERR | PERR |    |    |    |    |   |   |   |   |   |   |   |   |   |   | RXDATA |  |

| Bit   | Name     | Reset  | Access | Description   |
|-------|----------|--|--------|---|
| 31:16 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 15    | FERR     | 0  | R      | <b>Receive Data Framing Error</b><br>Set if data in buffer has a framing error. Can be the result of a break condition. |
| 14    | PERR     | 0  | R      | <b>Receive Data Parity Error</b><br>Set if data in buffer has a parity error.   |
| 13:9  | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 8:0   | RXDATA   | 0x000  | R      | <b>RX Data</b><br>Use this register to access data read from the LEUART. Buffer is cleared on read access.              |

### 20.5.8 LEUARTn\_RXDATA - Receive Buffer Data Register (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |        |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|--------|---|---|---|---|---|---|---|
| 0x01C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x00   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | R      |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RXDATA |   |   |   |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description    |
|------|----------|--|--------|----------------|
| 31:8 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |                |
| 7:0  | RXDATA   | 0x00   | R      | <b>RX Data</b> |

Use this register to access data read from LEUART. Buffer is cleared on read access. Only the 8 LSB can be read using this register.

### 20.5.9 LEUARTn\_RXDATAXP - Receive Buffer Data Extended Peek Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |       |       |    |    |    |    |    |    |   |   |   |   |   |   |   |   |         |   |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|-------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---------|---|--|--|
| 0x020         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17    | 16    | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1       | 0 |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    | 0     | 0     |    |    |    |    |    |    |   |   |   |   |   |   |   |   | 0x000   |   |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    | R     | R     |    |    |    |    |    |    |   |   |   |   |   |   |   |   | R       |   |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    | FERRP | PERRP |    |    |    |    |    |    |   |   |   |   |   |   |   |   | RXDATAP |   |  |  |

| Bit  | Name     | Reset  | Access | Description                            |
|--|----------|--|--------|--|
| 31:16  | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 15   | FERRP    | 0  | R      | <b>Receive Data Framing Error Peek</b> |
| Set if data in buffer has a framing error. Can be the result of a break condition. |          |  |        |  |
| 14   | PERRP    | 0  | R      | <b>Receive Data Parity Error Peek</b>  |
| Set if data in buffer has a parity error.  |          |  |        |  |
| 13:9   | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 8:0  | RXDATAP  | 0x000  | R      | <b>RX Data Peek</b>                    |
| Use this register to access data read from the LEUART.                             |          |  |        |  |

**20.5.10 LEUARTn\_TXDATAx - Transmit Buffer Data Extended Register (Async Reg)**

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |         |         |    |    |    |   |   |   |   |   |   |   |        |   |   |  |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|---------|---------|----|----|----|---|---|---|---|---|---|---|--------|---|---|--|--|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14      | 13      | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2      | 1 | 0 |  |  |  |
| 0x024         |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |         |         |    |    |    |   |   |   |   |   |   |   |        |   |   |  |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0      | 0       | 0       |    |    |    |   |   |   |   |   |   |   | 0x000  |   |   |  |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W      | W       | W       |    |    |    |   |   |   |   |   |   |   | W      |   |   |  |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RXENAT | TXDISAT | TXBREAK |    |    |    |   |   |   |   |   |   |   | TXDATA |   |   |  |  |  |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:16 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i>   |        |   |
| 15    | RXENAT          | 0   | W      | <b>Enable RX After Transmission</b><br>Set to enable reception after transmission.  |
|       | Value           | Description   |        |   |
|       | 0               | The receiver is not enabled after the frame has been transmitted  |        |   |
|       | 1               | The receiver is enabled (setting RXENS) after the frame has been transmitted  |        |   |
| 14    | TXDISAT         | 0   | W      | <b>Disable TX After Transmission</b><br>Set to disable transmitter directly after transmission has completed.   |
|       | Value           | Description   |        |   |
|       | 0               | The transmitter is not disabled after the frame has been transmitted  |        |   |
|       | 1               | The transmitter is disabled (clearing TXENS) after the frame has been transmitted   |        |   |
| 13    | TXBREAK         | 0   | W      | <b>Transmit Data as Break</b><br>Set to send data as a break. Recipient will see a framing error or a break condition depending on its configuration and the value of TXDATA. |
|       | Value           | Description   |        |   |
|       | 0               | The specified number of stop-bits are transmitted   |        |   |
|       | 1               | Instead of the ordinary stop-bits, 0 is transmitted to generate a break. A single stop-bit is generated after the break to allow the receiver to detect the start of the next frame |        |   |
| 12:9  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i>   |        |   |
| 8:0   | TXDATA          | 0x000   | W      | <b>TX Data</b><br>Use this register to write data to the LEUART. If the transmitter is enabled, a transfer will be initiated at the first opportunity.                        |

### 20.5.11 LEUARTn\_TXDATA - Transmit Buffer Data Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |        |   |   |   |   |   |   |   |  |  |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|--------|---|---|---|---|---|---|---|--|--|--|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| 0x028         |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |        |   |   |   |   |   |   |   |  |  |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x00   |   |   |   |   |   |   |   |  |  |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | W      |   |   |   |   |   |   |   |  |  |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | TXDATA |   |   |   |   |   |   |   |  |  |  |  |

| Bit   | Name     | Reset  | Access | Description    |
|---|----------|--|--------|----------------|
| 31:8  | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |                |
| 7:0   | TXDATA   | 0x00   | W      | <b>TX Data</b> |
| This frame will be added to the transmit buffer. Only 8 LSB can be written using this register. 9th bit and control bits will be cleared. |          |  |        |                |



## 20.5.13 LEUARTn\_IFS - Interrupt Flag Set Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |      |        |      |      |      |      |      |      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |     |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------|--------|------|------|------|------|------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----|
| 0x030         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11   | 10     | 9    | 8    | 7    | 6    | 5    | 4    | 3  | 2  | 1  | 0  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |     |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0    | 0      | 0    | 0    | 0    | 0    | 0    | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |     |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W1   | W1     | W1   | W1   | W1   | W1   | W1   | W1   | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1 | W1  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | SIGF | STARTF | MPAF | FERR | PERR | TXOF | RXUF | RXOF |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | TXC |

| Bit   | Name     | Reset   | Access | Description  |
|-------|----------|---|--------|--|
| 31:11 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 10    | SIGF     | 0   | W1     | <b>Set SIGF Interrupt Flag</b><br>Write 1 to set the SIGF interrupt flag     |
| 9     | STARTF   | 0   | W1     | <b>Set STARTF Interrupt Flag</b><br>Write 1 to set the STARTF interrupt flag |
| 8     | MPAF     | 0   | W1     | <b>Set MPAF Interrupt Flag</b><br>Write 1 to set the MPAF interrupt flag     |
| 7     | FERR     | 0   | W1     | <b>Set FERR Interrupt Flag</b><br>Write 1 to set the FERR interrupt flag     |
| 6     | PERR     | 0   | W1     | <b>Set PERR Interrupt Flag</b><br>Write 1 to set the PERR interrupt flag     |
| 5     | TXOF     | 0   | W1     | <b>Set TXOF Interrupt Flag</b><br>Write 1 to set the TXOF interrupt flag     |
| 4     | RXUF     | 0   | W1     | <b>Set RXUF Interrupt Flag</b><br>Write 1 to set the RXUF interrupt flag     |
| 3     | RXOF     | 0   | W1     | <b>Set RXOF Interrupt Flag</b><br>Write 1 to set the RXOF interrupt flag     |
| 2:1   | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 0     | TXC      | 0   | W1     | <b>Set TXC Interrupt Flag</b><br>Write 1 to set the TXC interrupt flag       |

## 20.5.14 LEUARTn\_IFC - Interrupt Flag Clear Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |       |        |        |       |       |       |       |       |       |       |       |       |       |       |       |       |  |  |  |  |       |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|--|--|--|--|-------|---|
| 0x034         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9     | 8      | 7      | 6     | 5     | 4     | 3     | 2     | 1     | 0     |       |       |       |       |       |       |  |  |  |  |       |   |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | SIGF  | 0      | STARTF | 0     | MPAF  | 0     | FERR  | 0     | PERR  | 0     | TXOF  | 0     | RXUF  | 0     | RXOF  | 0     |  |  |  |  | TXC   | 0 |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | (R)W1 | (R)W1  | (R)W1  | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 |  |  |  |  | (R)W1 |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | SIGF  | STARTF | MPAF   | FERR  | PERR  | TXOF  | RXUF  | RXOF  |       |       |       |       | TXC   |       |       |       |  |  |  |  |       |   |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:11 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 10    | SIGF            | 0   | (R)W1  | <b>Clear SIGF Interrupt Flag</b><br><br>Write 1 to clear the SIGF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 9     | STARTF          | 0   | (R)W1  | <b>Clear STARTF Interrupt Flag</b><br><br>Write 1 to clear the STARTF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 8     | MPAF            | 0   | (R)W1  | <b>Clear MPAF Interrupt Flag</b><br><br>Write 1 to clear the MPAF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 7     | FERR            | 0   | (R)W1  | <b>Clear FERR Interrupt Flag</b><br><br>Write 1 to clear the FERR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 6     | PERR            | 0   | (R)W1  | <b>Clear PERR Interrupt Flag</b><br><br>Write 1 to clear the PERR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 5     | TXOF            | 0   | (R)W1  | <b>Clear TXOF Interrupt Flag</b><br><br>Write 1 to clear the TXOF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 4     | RXUF            | 0   | (R)W1  | <b>Clear RXUF Interrupt Flag</b><br><br>Write 1 to clear the RXUF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 3     | RXOF            | 0   | (R)W1  | <b>Clear RXOF Interrupt Flag</b><br><br>Write 1 to clear the RXOF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 2:1   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 0     | TXC             | 0   | (R)W1  | <b>Clear TXC Interrupt Flag</b><br><br>Write 1 to clear the TXC interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).       |

## 20.5.15 LEUARTn\_IEN - Interrupt Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |      |        |      |      |      |      |      |      |         |      |     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------|--------|------|------|------|------|------|------|---------|------|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0x038         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11   | 10     | 9    | 8    | 7    | 6    | 5    | 4    | 3       | 2    | 1   | 0  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0    | 0      | 0    | 0    | 0    | 0    | 0    | 0    | 0       | 0    | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |    |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW   | RW     | RW   | RW   | RW   | RW   | RW   | RW   | RW      | RW   | RW  | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | SIGF | STARTF | MPAF | FERR | PERR | TXOF | RXUF | RXOF | RXDATAV | TXBL | TXC |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:11 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 10    | SIGF            | 0   | RW     | <b>SIGF Interrupt Enable</b><br>Enable/disable the SIGF interrupt       |
| 9     | STARTF          | 0   | RW     | <b>STARTF Interrupt Enable</b><br>Enable/disable the STARTF interrupt   |
| 8     | MPAF            | 0   | RW     | <b>MPAF Interrupt Enable</b><br>Enable/disable the MPAF interrupt       |
| 7     | FERR            | 0   | RW     | <b>FERR Interrupt Enable</b><br>Enable/disable the FERR interrupt       |
| 6     | PERR            | 0   | RW     | <b>PERR Interrupt Enable</b><br>Enable/disable the PERR interrupt       |
| 5     | TXOF            | 0   | RW     | <b>TXOF Interrupt Enable</b><br>Enable/disable the TXOF interrupt       |
| 4     | RXUF            | 0   | RW     | <b>RXUF Interrupt Enable</b><br>Enable/disable the RXUF interrupt       |
| 3     | RXOF            | 0   | RW     | <b>RXOF Interrupt Enable</b><br>Enable/disable the RXOF interrupt       |
| 2     | RXDATAV         | 0   | RW     | <b>RXDATAV Interrupt Enable</b><br>Enable/disable the RXDATAV interrupt |
| 1     | TXBL            | 0   | RW     | <b>TXBL Interrupt Enable</b><br>Enable/disable the TXBL interrupt       |
| 0     | TXC             | 0   | RW     | <b>TXC Interrupt Enable</b><br>Enable/disable the TXC interrupt         |

**20.5.16 LEUARTn\_PULSECTRL - Pulse Control Register (Async Reg)**

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |           |         |   |   |        |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|-----------|---------|---|---|--------|---|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5         | 4       | 3 | 2 | 1      | 0 |  |
| 0x03C         |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |           |         |   |   |        |   |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | 0         | 0       |   |   | 0x0    |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | RW        | RW      |   |   | RW     |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | PULSEFILT | PULSEEN |   |   | PULSEW |   |  |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 31:6 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 5    | PULSEFILT       | 0   | RW     | <b>Pulse Filter</b><br>Enable a one-cycle pulse filter for pulse extender   |
|      | Value           |   |        | Description   |
|      | 0               |   |        | Filter is disabled. Pulses must be at least 2 cycles long for reliable detection.   |
|      | 1               |   |        | Filter is enabled. Pulses must be at least 3 cycles long for reliable detection.  |
| 4    | PULSEEN         | 0   | RW     | <b>Pulse Generator/Extender Enable</b><br>Filter LEUART output through pulse generator and the LEUART input through the pulse extender. |
| 3:0  | PULSEW          | 0x0   | RW     | <b>Pulse Width</b><br>Configure the pulse width of the pulse generator as a number of 32.768 kHz clock cycles.                          |

## 20.5.17 LEUARTn\_FREEZE - Freeze Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |           |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-----------|
| 0x040         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0         |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0         |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | RW        |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | REGFREEZE |

| Bit  | Name      | Reset  | Access   | Description   |
|------|-----------|--|--|---|
| 31:1 | Reserved  | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |  |   |
| 0    | REGFREEZE | 0  | RW   | <b>Register Update Freeze</b><br>When set, the update of the LEUART logic from registers is postponed until this bit is cleared. Use this bit to update several registers simultaneously. |
|      | Value     | Mode   | Description  |   |
|      | 0         | UPDATE   | Each write access to a LEUART register is updated into the Low Frequency domain as soon as possible. |   |
|      | 1         | FREEZE   | The LEUART is not updated with the new written value.  |   |

## 20.5.18 LEUARTn\_SYNCBUSY - Synchronization Busy Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |           |    |        |   |         |   |          |   |            |   |        |   |     |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------|----|--------|---|---------|---|----------|---|------------|---|--------|---|-----|---|------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|
| 0x044         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11        | 10 | 9      | 8 | 7       | 6 | 5        | 4 | 3          | 2 | 1      | 0 |     |   |      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R         | 0  | R      | 0 | R       | 0 | R        | 0 | R          | 0 | R      | 0 | R   | 0 | R    | 0 | R | 0 | R | 0 | R | 0 | R | 0 | R | 0 | R | 0 | R | 0 |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R         |    | R      |   | R       |   | R        |   | R          |   | R      |   | R   |   | R    |   | R |   | R |   | R |   | R |   | R |   | R |   | R |   | R |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PULSECTRL |    | TXDATA |   | TXDATAX |   | SIGFRAME |   | STARTFRAME |   | CLKDIV |   | CMD |   | CTRL |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |

| Bit  | Name       | Reset  | Access | Description  |
|------|------------|--|--------|--|
| 31:8 | Reserved   | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 7    | PULSECTRL  | 0  | R      | <b>PULSECTRL Register Busy</b><br>Set when the value written to PULSECTRL is being synchronized.   |
| 6    | TXDATA     | 0  | R      | <b>TXDATA Register Busy</b><br>Set when the value written to TXDATA is being synchronized.         |
| 5    | TXDATAX    | 0  | R      | <b>TXDATAX Register Busy</b><br>Set when the value written to TXDATAX is being synchronized.       |
| 4    | SIGFRAME   | 0  | R      | <b>SIGFRAME Register Busy</b><br>Set when the value written to SIGFRAME is being synchronized.     |
| 3    | STARTFRAME | 0  | R      | <b>STARTFRAME Register Busy</b><br>Set when the value written to STARTFRAME is being synchronized. |
| 2    | CLKDIV     | 0  | R      | <b>CLKDIV Register Busy</b><br>Set when the value written to CLKDIV is being synchronized.         |
| 1    | CMD        | 0  | R      | <b>CMD Register Busy</b><br>Set when the value written to CMD is being synchronized.               |
| 0    | CTRL       | 0  | R      | <b>CTRL Register Busy</b><br>Set when the value written to CTRL is being synchronized.             |

## 20.5.19 LEUARTn\_ROUTE PEN - I/O Routing Pin Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |       |       |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|-------|-------|---|---|
| 0x054         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3     | 2     | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0     | 0     |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | RW    | RW    |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | TXPEN | RXPEN |   |   |

| Bit  | Name            | Reset   | Access | Description  |
|------|-----------------|---|--------|--|
| 31:2 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 1    | TXPEN           | 0   | RW     | <b>TX Pin Enable</b><br>When set, the TX pin of the LEUART is enabled. |
|      | Value           |   |        | Description  |
|      | 0               |   |        | The LEUn_TX pin is disabled  |
|      | 1               |   |        | The LEUn_TX pin is enabled   |
| 0    | RXPEN           | 0   | RW     | <b>RX Pin Enable</b><br>When set, the RX pin of the LEUART is enabled. |
|      | Value           |   |        | Description  |
|      | 0               |   |        | The LEUn_RX pin is disabled  |
|      | 1               |   |        | The LEUn_RX pin is enabled   |

## 20.5.20 LEUARTn\_ROUTELOC0 - I/O Routing Location Register

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |       |    |    |    |    |    |   |   |   |   |   |   |       |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|----|----|----|----|----|---|---|---|---|---|---|-------|---|---|---|
| 0x058  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15    | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3     | 2 | 1 | 0 |
| Reset  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00  |    |    |    |    |    |   |   |   |   |   |   | 0x00  |   |   |   |
| Access |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW    |    |    |    |    |    |   |   |   |   |   |   | RW    |   |   |   |
| Name   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | TXLOC |    |    |    |    |    |   |   |   |   |   |   | RXLOC |   |   |   |

| Bit   | Name     | Reset   | Access | Description         |
|-------|----------|---|--------|---------------------|
| 31:14 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |                     |
| 13:8  | TXLOC    | 0x00  | RW     | <b>I/O Location</b> |

Decides the location of the LEUART TX pin. See the device data sheet for the mapping between location and physical pins.

| Value | Mode  | Description |
|-------|-------|-------------|
| 0     | LOC0  | Location 0  |
| 1     | LOC1  | Location 1  |
| 2     | LOC2  | Location 2  |
| 3     | LOC3  | Location 3  |
| 4     | LOC4  | Location 4  |
| 5     | LOC5  | Location 5  |
| 6     | LOC6  | Location 6  |
| 7     | LOC7  | Location 7  |
| 8     | LOC8  | Location 8  |
| 9     | LOC9  | Location 9  |
| 10    | LOC10 | Location 10 |
| 11    | LOC11 | Location 11 |
| 12    | LOC12 | Location 12 |
| 13    | LOC13 | Location 13 |
| 14    | LOC14 | Location 14 |
| 15    | LOC15 | Location 15 |
| 16    | LOC16 | Location 16 |
| 17    | LOC17 | Location 17 |
| 18    | LOC18 | Location 18 |
| 19    | LOC19 | Location 19 |
| 20    | LOC20 | Location 20 |
| 21    | LOC21 | Location 21 |
| 22    | LOC22 | Location 22 |
| 23    | LOC23 | Location 23 |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
| 24  |      | LOC24 |        | Location 24 |
| 25  |      | LOC25 |        | Location 25 |
| 26  |      | LOC26 |        | Location 26 |
| 27  |      | LOC27 |        | Location 27 |
| 28  |      | LOC28 |        | Location 28 |
| 29  |      | LOC29 |        | Location 29 |
| 30  |      | LOC30 |        | Location 30 |
| 31  |      | LOC31 |        | Location 31 |

**7:6** *Reserved* *To ensure compatibility with future devices, always write bits to 0. More information in [1.2 Conventions](#)*

**5:0** RXLOC 0x00 RW **I/O Location**

Decides the location of the LEUART RX pin. See the device data sheet for the mapping between location and physical pins.

| Value | Mode  | Description |
|-------|-------|-------------|
| 0     | LOC0  | Location 0  |
| 1     | LOC1  | Location 1  |
| 2     | LOC2  | Location 2  |
| 3     | LOC3  | Location 3  |
| 4     | LOC4  | Location 4  |
| 5     | LOC5  | Location 5  |
| 6     | LOC6  | Location 6  |
| 7     | LOC7  | Location 7  |
| 8     | LOC8  | Location 8  |
| 9     | LOC9  | Location 9  |
| 10    | LOC10 | Location 10 |
| 11    | LOC11 | Location 11 |
| 12    | LOC12 | Location 12 |
| 13    | LOC13 | Location 13 |
| 14    | LOC14 | Location 14 |
| 15    | LOC15 | Location 15 |
| 16    | LOC16 | Location 16 |
| 17    | LOC17 | Location 17 |
| 18    | LOC18 | Location 18 |
| 19    | LOC19 | Location 19 |
| 20    | LOC20 | Location 20 |
| 21    | LOC21 | Location 21 |
| 22    | LOC22 | Location 22 |
| 23    | LOC23 | Location 23 |

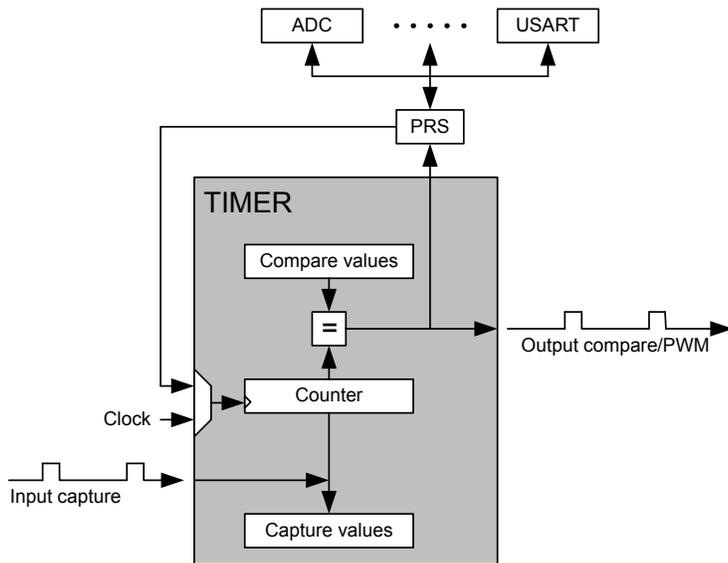
| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
| 24  |      | LOC24 |        | Location 24 |
| 25  |      | LOC25 |        | Location 25 |
| 26  |      | LOC26 |        | Location 26 |
| 27  |      | LOC27 |        | Location 27 |
| 28  |      | LOC28 |        | Location 28 |
| 29  |      | LOC29 |        | Location 29 |
| 30  |      | LOC30 |        | Location 30 |
| 31  |      | LOC31 |        | Location 31 |

## 20.5.21 LEUARTn\_INPUT - LEUART Input Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |       |   |   |         |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|-------|---|---|---------|---|---|
| 0x064         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5     | 4 | 3 | 2       | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | 0     |   |   | 0x0     |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | RW    |   |   | RW      |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | RXPRS |   |   | RXPRSEL |   |   |

| Bit  | Name            | Reset   | Access                  | Description  |
|------|-----------------|---|-------------------------|--|
| 31:6 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                         |  |
| 5    | RXPRS           | 0   | RW                      | <b>PRS RX Enable</b><br>When set, the PRS channel selected as input to RX. |
| 4    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                         |  |
| 3:0  | RXPRSEL         | 0x0   | RW                      | <b>RX PRS Channel Select</b><br>Select PRS channel as input to RX.         |
|      | Value           | Mode  | Description             |  |
|      | 0               | PRSCH0  | PRS Channel 0 selected  |  |
|      | 1               | PRSCH1  | PRS Channel 1 selected  |  |
|      | 2               | PRSCH2  | PRS Channel 2 selected  |  |
|      | 3               | PRSCH3  | PRS Channel 3 selected  |  |
|      | 4               | PRSCH4  | PRS Channel 4 selected  |  |
|      | 5               | PRSCH5  | PRS Channel 5 selected  |  |
|      | 6               | PRSCH6  | PRS Channel 6 selected  |  |
|      | 7               | PRSCH7  | PRS Channel 7 selected  |  |
|      | 8               | PRSCH8  | PRS Channel 8 selected  |  |
|      | 9               | PRSCH9  | PRS Channel 9 selected  |  |
|      | 10              | PRSCH10   | PRS Channel 10 selected |  |
|      | 11              | PRSCH11   | PRS Channel 11 selected |  |

## 21. TIMER/WTIMER - Timer/Counter



### Quick Facts

#### What?

The TIMER (Timer/Counter) keeps track of timing and counts events, generates output waveforms, and triggers timed actions in other peripherals.

#### Why?

Most applications have activities that need to be timed accurately with as little CPU intervention and energy consumption as possible.

#### How?

The flexible 16/32-bit timer can be configured to provide PWM waveforms with optional dead-time insertion (e.g. motor control) or work as a frequency generator. The timer can also count events and control other peripherals through the PRS, which offloads the CPU and reduces energy consumption.

### 21.1 Introduction

The general purpose timer has 3 or 4 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output.

The TIMER and WTIMER peripherals are identical except for the timer width. A TIMER is 16-bits wide and a WTIMER is 32-bits wide. Some timers also include a Dead-Time Insertion module suitable for motor control applications.

Refer to the device data sheet to determine the capabilities (capture/compare channel count and DTI) of each timer instance.

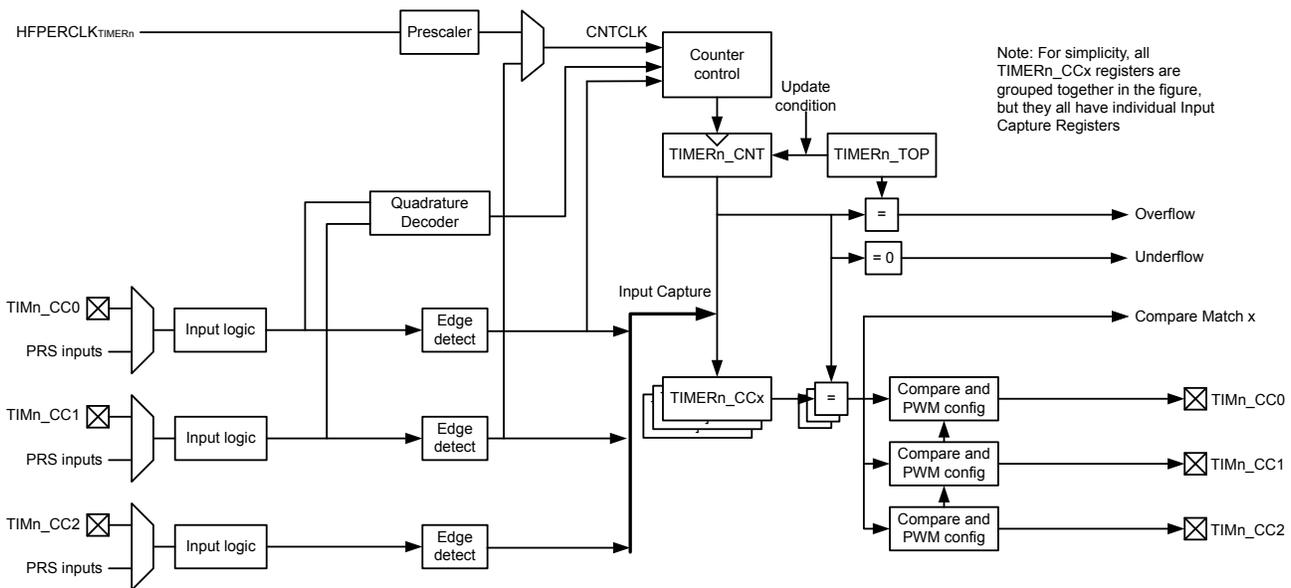
## 21.2 Features

- 16/32-bit auto reload up/down counter
  - Dedicated 16/32-bit reload register which serves as counter maximum
- 3 or 4 Compare/Capture channels
  - Individually configurable as either input capture or output compare/PWM
- Multiple Counter modes
  - Count up
  - Count down
  - Count up/down
  - Quadrature Decoder
  - Direction and count from external pins
- 2x Count Mode
- Counter control from PRS or external pin
  - Start
  - Stop
  - Reload and start
- Inter-Timer connection
  - Allows 32-bit counter mode
  - Start/stop synchronization between several timers
- Input Capture
  - Period measurement
  - Pulse width measurement
  - Two capture registers for each capture channel
    - Capture on either positive or negative edge
    - Capture on both edges
  - Optional digital noise filtering on capture inputs
- Output Compare
  - Compare output toggle/pulse on compare match
  - Immediate update of compare registers
- PWM
  - Up-count PWM
  - Up/down-count PWM
  - Predictable initial PWM output state (configured by SW)
  - Buffered compare register to ensure glitch-free update of compare values
- Clock sources
  - HFPERCLK<sub>TIMERn</sub>
    - 10-bit Prescaler
  - External pin
  - Peripheral Reflex System
- Debug mode
  - Configurable to either run or stop when processor is stopped (halt/breakpoint)
- Interrupts, PRS output and/or DMA request on:
  - Underflow
  - Overflow
  - Compare/Capture event
- Dead-Time Insertion Unit
  - Complementary PWM outputs with programmable dead-time
    - Dead-time is specified independently for rising and falling edge
      - 10-bit prescaler
      - 6-bit time value
  - Outputs have configurable polarity
  - Outputs can be set inactive individually by software.

- Configurable action on fault
  - Set outputs inactive
  - Clear output
  - Tristate output
- Individual fault sources
  - One or two PRS signals
  - Debugger
    - Support for automatic restart
  - Core lockup
- Configuration lock

### 21.3 Functional Description

An overview of the TIMER/WTIMER module is shown in [Figure 21.1 TIMER/WTIMER Block Overview on page 693](#) and it consists of a 16/32 bit up/down counter with 3 Compare/Capture channels connected to pins TIMn\_CC0, TIMn\_CC1, and TIMn\_CC2.



**Figure 21.1. TIMER/WTIMER Block Overview**

WTIMERS (Wide TIMERS) are 32-bit variants of the TIMER/WTIMER module.

#### 21.3.1 Counter Modes

The timer consists of a counter that can be configured to the following modes:

1. Up-count: Counter counts up until it reaches the value in TIMERn\_TOP, where it is reset to 0 before counting up again.
2. Down-count: The counter starts at the value in TIMERn\_TOP and counts down. When it reaches 0, it is reloaded with the value in TIMERn\_TOP.
3. Up/Down-count: The counter starts at 0 and counts up. When it reaches the value in TIMERn\_TOP, it counts down until it reaches 0 and starts counting up again.
4. Quadrature Decoder: Two input channels where one determines the count direction, while the other pin triggers a clock event.

In addition, to the TIMER/WTIMER modes listed above, the TIMER/WTIMER also supports a 2x Count Mode. In this mode the counter increments/decrements by 2. The 2x Count Mode intended use is to generate 2x PWM frequency when the Compare/Capture channel is put in PWM mode. The 2x Count Mode can be enabled by setting the X2CNT bitfield in the TIMERn\_CTRL register.

The counter value can be read or written by software at any time by accessing the CNT field in TIMERn\_CNT.

### 21.3.1.1 Events

Overflow is set when the counter value shifts from `TIMERN_TOP` to the next value when counting up. In up-count mode and Quadrature Decoder mode the next value is 0. In up/down-count mode, the next value is `TIMERN_TOP-1`.

Underflow is set when the counter value shifts from 0 to the next value when counting down. In down-count mode and Quadrature Decoder mode, the next value is `TIMERN_TOP`. In up/down-count mode the next value is 1.

An update event occurs on overflow in up-count mode and on underflow in down-count or up/down count mode. Additionally, an update event also occurs on overflow and underflow in Quadrature Decoder Mode. This event is used to time updates of buffered values.

### 21.3.1.2 Operation

Figure 21.2 **TIMER/WTIMER Hardware Timer/Counter Control** on page 694 shows the hardware Timer/Counter control. Software can start or stop the counter by setting the `START` or `STOP` bits in `TIMERN_CMD`. The counter value (`CNT` in `TIMERN_CNT`) can always be written by software to any 16/32-bit value.

It is also possible to control the counter through either an external pin or PRS input. This is done through the input logic for the Compare/Capture Channel 0. The Timer/Counter allows individual actions (start, stop, reload) to be taken for rising and falling input edges. This is configured in the `RISEA` and `FALLA` fields in `TIMERN_CTRL`. The reload value is 0 in up-count and up/down-count mode and `TOP` in down-count mode.

The `RUNNING` bit in `TIMERN_STATUS` indicates if the timer is running or not. If the `SYNC` bit in `TIMERN_CTRL` is set, the timer is started/stopped/reloaded (external pin or PRS) when any of the other timers are started/stopped/reloaded.

The `DIR` bit in `TIMERN_STATUS` indicates the counting direction of the timer at any given time. The counter value can be read or written by software through the `CNT` field in `TIMERN_CNT`. In Up/Down-Count mode the count direction will be set to up if the `CNT` value is written by software.

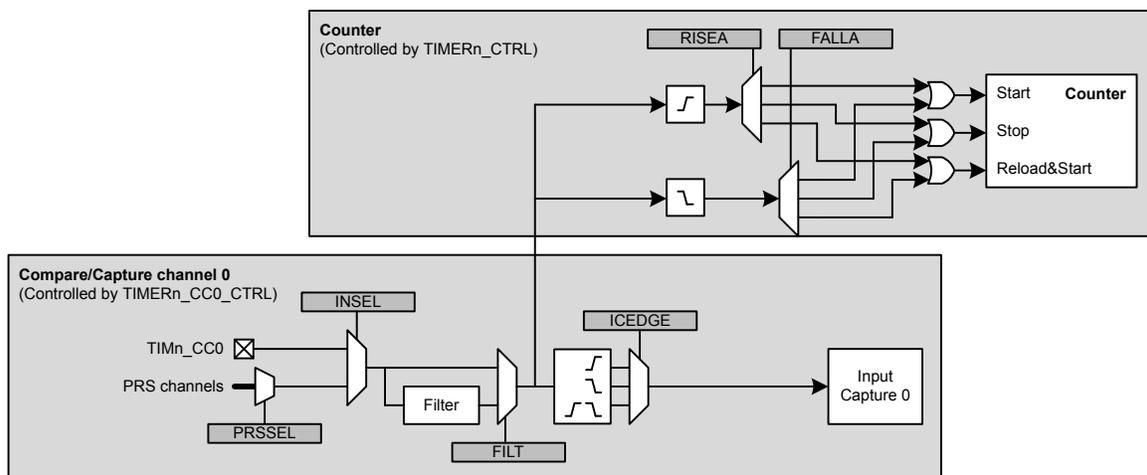


Figure 21.2. TIMER/WTIMER Hardware Timer/Counter Control

### 21.3.1.3 Clock Source

The counter can be clocked from several sources, which are all synchronized with the peripheral clock (HFPERCLK). See [Figure 21.3 TIMER/WTIMER Clock Selection on page 695](#).

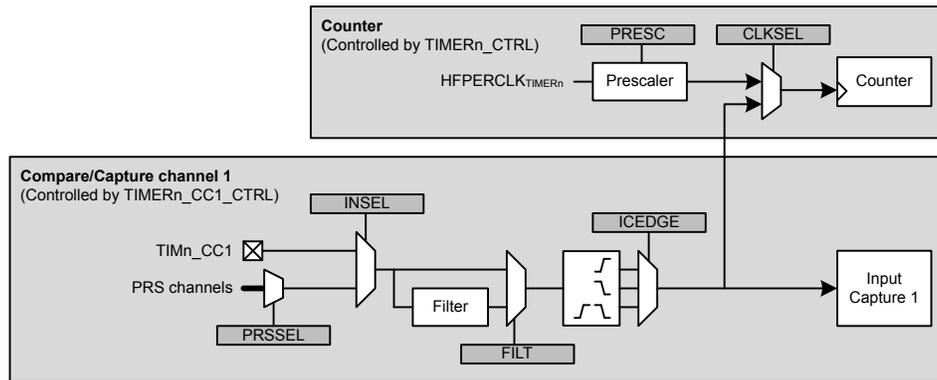


Figure 21.3. TIMER/WTIMER Clock Selection

### 21.3.1.4 Peripheral Clock (HFPERCLK)

The peripheral clock (HFPERCLK) can be used as a source with a configurable prescale factor of  $2^{\text{PRESC}}$ , where PRESC is an integer between 0 and 10, which is set in PRESC in `TIMERn_CTRL`. However, if 2x Count Mode is enabled and the Compare/Capture channels are put in PWM mode, the CC output is updated on both clock edges so prescaling the peripheral clock will produce an incorrect result. The prescaler is stopped and reset when the timer is stopped.

### 21.3.1.5 Compare/ Capture Channel 1 Input

The timer can also be clocked by positive and/or negative edges on the Compare/Capture channel 1 input. This input can either come from the `TIMn_CC1` pin or one of the PRS channels. The input signal must not have a higher frequency than  $f_{\text{HFPERCLK}}/3$  when running from a pin input or a PRS input with `FILT` enabled in `TIMERn_CCx_CTRL`. When running from PRS without `FILT`, the frequency can be as high as  $f_{\text{HFPERCLK}}$ . Note that when clocking the timer from the same pulse that triggers a start (through `RISEA/FALLA` in `TIMERn_CTRL`), the starting pulse will not update the Counter Value.

### 21.3.1.6 Underflow/Overflow From Neighboring Timer

All timers are linked together (see [Figure 21.4 TIMER/WTIMER Connections on page 695](#)), allowing timers to count on overflow/underflow from the lower numbered neighbouring timers to form a 32-bit or 48-bit timer. Note that all timers must be set to same count direction and less significant timer(s) can only be set to count up or down.

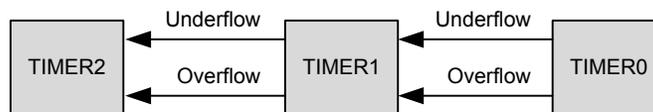


Figure 21.4. TIMER/WTIMER Connections

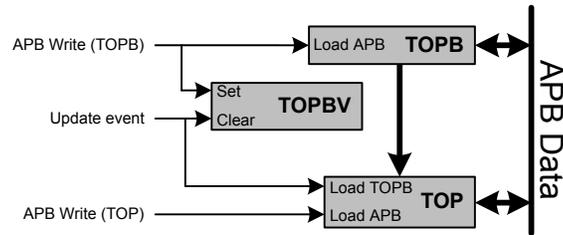
### 21.3.1.7 One-Shot Mode

By default, the counter counts continuously until it is stopped. If the `OSMEN` bit is set in the `TIMERn_CTRL` register, however, the counter is disabled by hardware on the first *update event* (see [21.3.1.1 Events](#)). Note that when the counter is running with `CC1` as clock source (`0b01` in `CLKSEL` in `TIMERn_CTRL`) and `OSMEN` is set, a `CC1` capture event will not take place on the *update event* (`CC1` rising edge) that stops the timer.

### 21.3.1.8 Top Value Buffer

The TIMERN\_TOP register can be altered either by writing it directly or by writing to the TIMER\_TOPB (buffer) register. When writing to the buffer register the TIMERN\_TOPB register will be written to TIMERN\_TOP on the next *update event*. Buffering ensures that the TOP value is not set below the actual count value. The TOPBV flag in TIMERN\_STATUS indicates whether the TIMERN\_TOPB register contains data that has not yet been written to the TIMERN\_TOP register (see [Figure 21.5 TIMER/WTIMER TOP Value Update Functionality on page 696](#)).

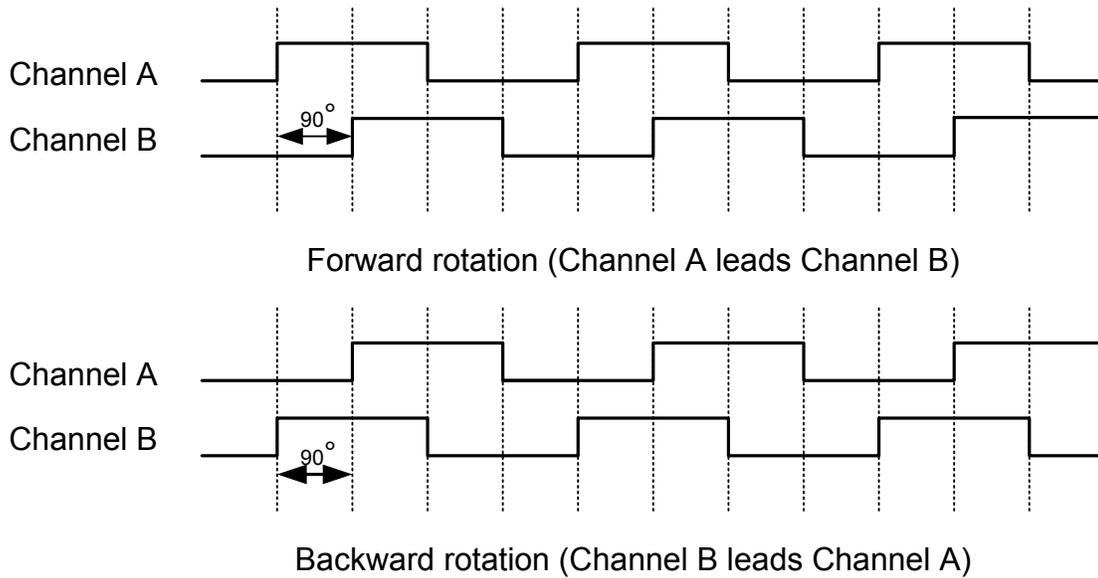
**Note:** When writing to TIMERN\_TOP register directly, the TIMERN\_TOPB register value will be invalidated and the TOPBV flag will be cleared. This prevents TIMERN\_TOP register from being immediately updated by an existing valid TIMERN\_TOPB value during the next *update event*.



**Figure 21.5. TIMER/WTIMER TOP Value Update Functionality**

### 21.3.1.9 Quadrature Decoder

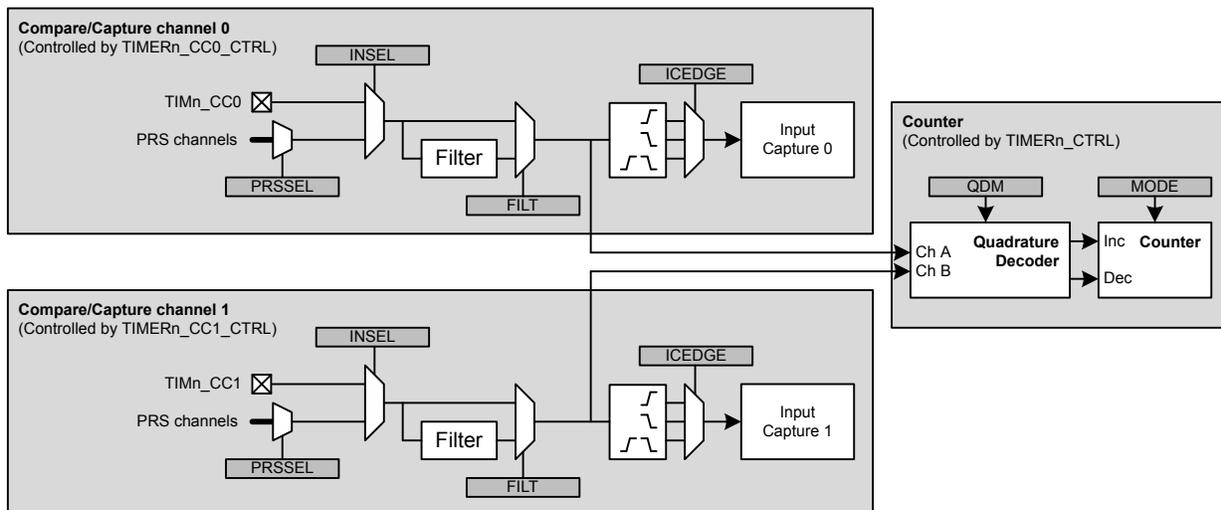
Quadrature Decoding mode is used to track motion and determine both rotation direction and position. The Quadrature Decoder uses two input channels that are 90 degrees out of phase (see [Figure 21.6 TIMER/WTIMER Quadrature Encoded Inputs on page 697](#)).



**Figure 21.6. TIMER/WTIMER Quadrature Encoded Inputs**

In the timer these inputs are tapped from the Compare/Capture channel 0 (Channel A) and 1 (Channel B) inputs before edge detection. The Timer/Counter then increments or decrements the counter, based on the phase relation between the two inputs. The Quadrature Decoder Mode supports two channels, but if a third channel (Z-terminal) is available, this can be connected to an external interrupt and trigger a counter reset from the interrupt service routine. By connecting a periodic signal from another timer as input capture on Compare/Capture Channel 2, it is also possible to calculate speed and acceleration.

**Note:** In Quadrature Decoder mode, overflow and underflow triggers an *update event*.



**Figure 21.7. TIMER/WTIMER Quadrature Decoder Configuration**

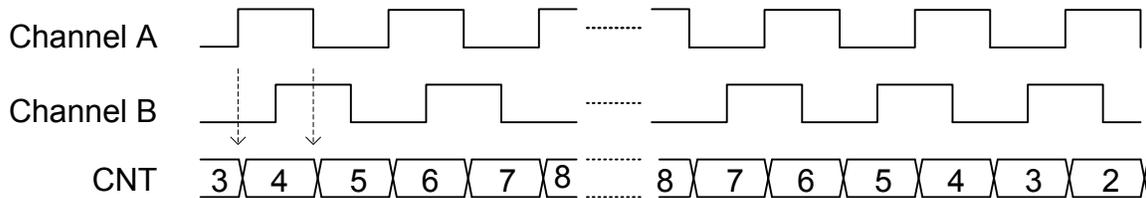
The Quadrature Decoder can be set in either X2 or X4 mode, which is configured in the QDM bit in TIMn\_CTRL. See [Figure 21.7 TIMER/WTIMER Quadrature Decoder Configuration on page 697](#)

### 21.3.1.10 X2 Decoding Mode

In X2 Decoding mode, the counter increments or decrements on every edge of Channel A, see [Table 21.1 TIMER/WTIMER Counter Response in X2 Decoding Mode on page 698](#) and [Figure 21.8 TIMER/WTIMER X2 Decoding Mode on page 698](#).

**Table 21.1. TIMER/WTIMER Counter Response in X2 Decoding Mode**

| Channel B | Channel A |           |
|-----------|-----------|-----------|
|           | Rising    | Falling   |
| 0         | Increment | Decrement |
| 1         | Decrement | Increment |



**Figure 21.8. TIMER/WTIMER X2 Decoding Mode**

### 21.3.1.11 X4 Decoding Mode

In X4 Decoding mode, the counter increments or decrements on every edge of Channel A and Channel B, see [Figure 21.9 TIMER/WTIMER X4 Decoding Mode on page 698](#) and [Table 21.2 TIMER/WTIMER Counter Response in X4 Decoding Mode on page 698](#).

**Table 21.2. TIMER/WTIMER Counter Response in X4 Decoding Mode**

| Opposite Channel | Channel A |           | Channel B |           |
|------------------|-----------|-----------|-----------|-----------|
|                  | Rising    | Falling   | Rising    | Falling   |
| Channel A = 0    |           |           | Decrement | Increment |
| Channel A = 1    |           |           | Increment | Decrement |
| Channel B = 0    | Increment | Decrement |           |           |
| Channel B = 1    | Decrement | Increment |           |           |



**Figure 21.9. TIMER/WTIMER X4 Decoding Mode**

### 21.3.1.12 TIMER/WTIMER Rotational Position

To calculate a position [Figure 21.10 TIMER/WTIMER Rotational Position Equation on page 699](#) can be used.

$$\text{pos}^\circ = (\text{CNT}/X \times N) \times 360^\circ$$

**Figure 21.10. TIMER/WTIMER Rotational Position Equation**

where X = Encoding type and N = Number of pulses per revolution.

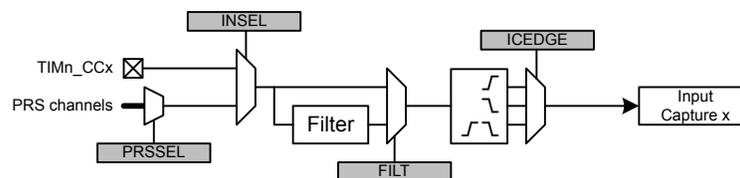
### 21.3.2 Compare/Capture Channels

The timer contains 3 Compare/Capture channels, which can be configured in the following modes:

1. Input Capture
2. Output Compare
3. PWM

#### 21.3.2.1 Input Pin Logic

Each Compare/Capture channel can be configured as an input source for the Capture Unit or as external clock source for the timer (see [Figure 21.11 TIMER/WTIMER Input Pin Logic on page 699](#)). Compare/Capture channels 0 and 1 are the inputs for the Quadrature Decoder Mode. The input channel can be filtered before it is used, which requires the input to remain stable for 5 cycles in a row before the input is propagated to the output.



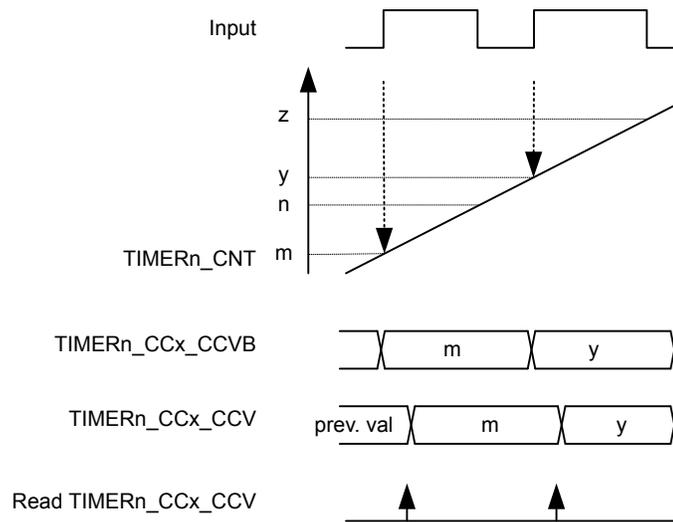
**Figure 21.11. TIMER/WTIMER Input Pin Logic**

#### 21.3.2.2 Compare/Capture Registers

The Compare/Capture channel registers are prefixed with `TIMERn_CCx_`, where the x stands for the channel number. Since the Compare/Capture channels serve three functions (input capture, compare, PWM), the behavior of the Compare/Capture registers (`TIMERn_CCx_CCV`) and buffer registers (`TIMERn_CCx_CCVB`) change depending on the mode the channel is set in.

### 21.3.2.3 Input Capture

In Input Capture Mode, the counter value (TIMERN\_CNT) can be captured in the Compare/Capture Register (TIMERN\_CCx\_CCV) (see [Figure 21.12 TIMER/WTIMER Input Capture on page 700](#)). The CCPOL bits in TIMERN\_STATUS indicate the polarity of the edge that triggered the capture in TIMERN\_CCx\_CCV.



**Figure 21.12. TIMER/WTIMER Input Capture**

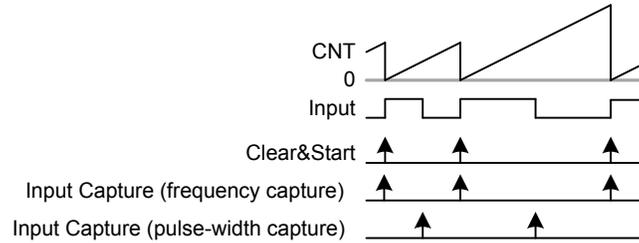
The Compare/Capture Buffer Register (TIMERN\_CCx\_CCVB) and the TIMERN\_CCx\_CCV register form double-buffered capture registers allowing two subsequent capture events to take place before a read-out is required. The first capture can always be read from TIMERN\_CCx\_CCV, and reading this address will load the next capture value into TIMERN\_CCx\_CCV from TIMERN\_CCx\_CCVB if it contains valid data. The CC value can be read without altering the FIFO contents by reading TIMERN\_CCx\_CCV. TIMERN\_CCx\_CCVB can also be read without altering the FIFO contents. The ICV flag in TIMERN\_STATUS indicates if there is a valid unread capture in TIMERN\_CCx\_CCV. In this mode, TIMERN\_CCx\_CCV is read-only.

In the case where a capture is triggered while both TIMERN\_CCx\_CCV and TIMERN\_CCx\_CCVB contain unread capture values, the buffer overflow interrupt flag (ICBOF in TIMERN\_IF) will be set. On overflow new capture values will overwrite the value in TIMERN\_CCx\_CCVB and the value of TIMERN\_CCx\_CCV will remain unchanged. TIMERN\_CCx\_CCV will always contain the oldest unread value and TIMERN\_CCx\_CCVB will always contain the newest value.

**Note:** In input capture mode, the timer will only trigger interrupts when it is running.

### 21.3.2.4 Period/Pulse-Width Capture

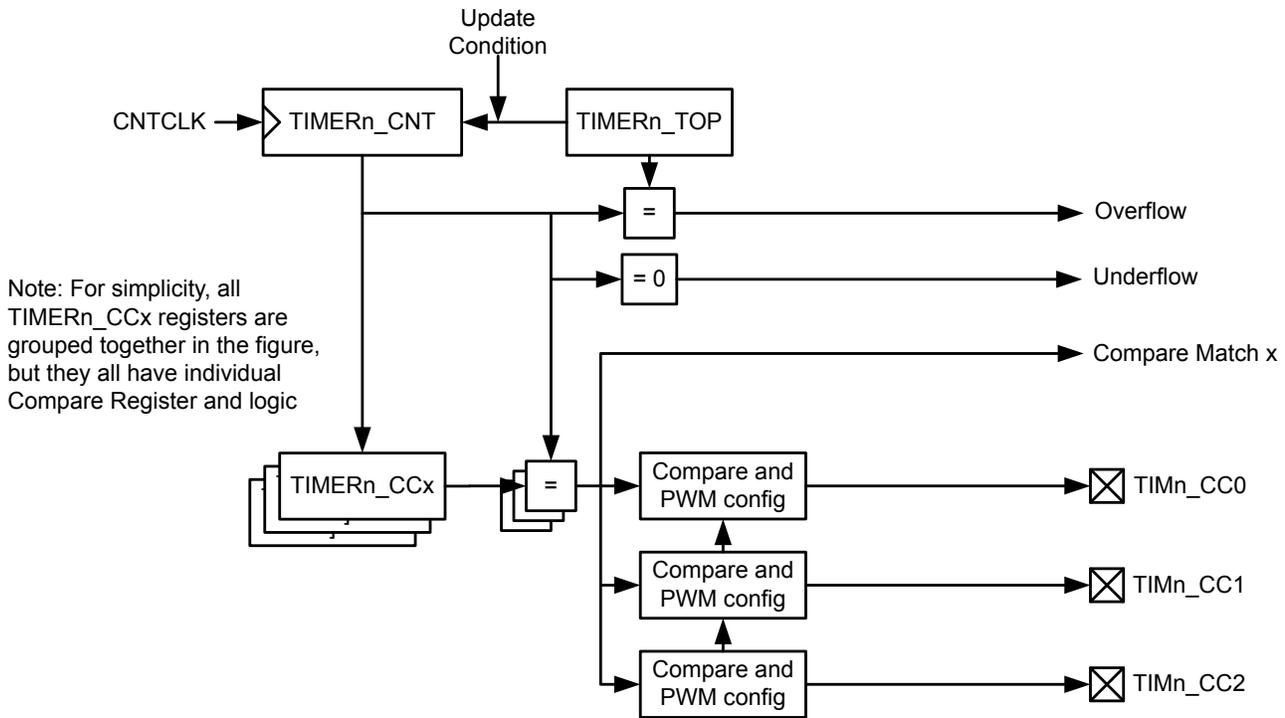
Period and/or pulse-width capture can only be possible with Channel 0 (CC0), because this is the only channel that can start and stop the timer. This can be done by setting the RISEA field in `TIMERn_CTRL` to `Clear&Start`, and select the wanted input from either external pin or PRS, see [Figure 21.13 TIMER/WTIMER Period and/or Pulse width Capture on page 701](#). For period capture, the Compare/Capture Channel should then be set to input capture on a rising edge of the same input signal. To capture the width of a high pulse, the Compare/Capture Channel should be set to capture on a falling edge of the input signal. To measure the low pulse-width of a signal, opposite polarities should be chosen.



**Figure 21.13. TIMER/WTIMER Period and/or Pulse width Capture**

### 21.3.2.5 Compare

Each Compare/Capture channel contains a comparator which outputs a compare match if the contents of `TIMERn_CCx_CCV` matches the counter value, see [Figure 21.14 TIMER/WTIMER Block Diagram Showing Comparison Functionality on page 702](#). In compare mode, each compare channel can be configured to either set, clear or toggle the output on an event (compare match, overflow or underflow). The output from each channel is represented as an alternative function on the port it is connected to, which needs to be enabled for the CC outputs to propagate to the pins.

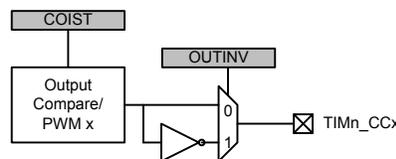


**Figure 21.14. TIMER/WTIMER Block Diagram Showing Comparison Functionality**

The compare output is delayed by one cycle to allow for full 0% to 100% PWM generation. If occurring in the same cycle, match action will have priority over overflow or underflow action.

The input selected (through `PRSEL`, `INSEL` and `FILTSEL` in `TIMERn_CCx_CTRL`) for the CC channel will also be sampled on compare match and the result is found in the `CCPOL` bits in `TIMERn_STATUS`. It is also possible to configure the `CCPOL` to always track the inputs by setting `ATI` in `TIMERn_CTRL`.

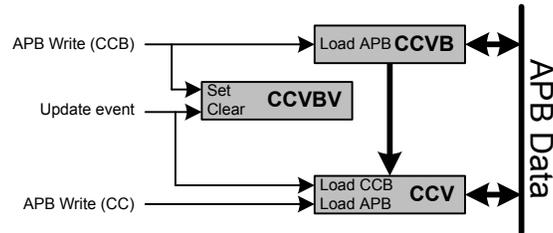
The `COIST` bit in `TIMERn_CCx_CTRL` is the initial state of the compare/PWM output. The `COIST` bit can also be used as an initial value to the compare outputs on a reload-start when `RSSCOIST` is set in `TIMERn_CTRL`. Also the resulting output can be inverted by setting `OUTINV` in `TIMERn_CCx_CTRL`. It is recommended to turn off the CC channel before configuring the output state to avoid any pulses on the output. The CC channel can be turned off by setting `MODE` to `OFF` in `TIMERn_CCx_CTRL`. The following figure shows the output logic for the TIMER/WTIMER module.



**Figure 21.15. TIMER/WTIMER Output Logic**

### 21.3.2.6 Compare Mode Registers

When running in Output Compare or PWM mode, the value in `TIMERN_CCx_CCv` will be compared against the count value. In Compare mode the output can be configured to toggle, clear or set on compare match, overflow, and underflow through the `CMOA`, `COFOA` and `CUFOA` fields in `TIMERN_CCx_CTRL`. `TIMERN_CCx_CCv` can be accessed directly or through the buffer register `TIMERN_CCx_CCvB`, see [Figure 21.16 TIMER/WTIMER Output Compare/PWM Buffer Functionality Detail on page 703](#). When writing to the buffer register, the value in `TIMERN_CCx_CCvB` will be written to `TIMERN_CCx_CCv` on the next *update event*. This functionality ensures glitch free PWM outputs. The `CCVBV` flag in `TIMERN_STATUS` indicates whether the `TIMERN_CCx_CCvB` register contains data that has not yet been written to the `TIMERN_CCx_CCv` register. Note that when writing 0 to `TIMERN_CCx_CCvB` in up-down count mode the `CCv` value is updated when the timer counts from 0 to 1. Thus, the compare match for the next period will not happen until the timer reaches 0 again on the way down.

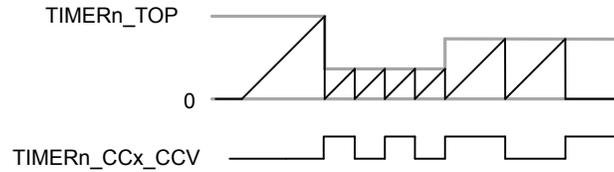


**Figure 21.16. TIMER/WTIMER Output Compare/PWM Buffer Functionality Detail**

### 21.3.2.7 Frequency Generation (FRG)

Frequency generation (see [Figure 21.17 TIMER/WTIMER Up-count Frequency Generation on page 704](#)) can be achieved in compare mode by:

- Setting the counter in up-count mode
- Enabling buffering of the TOP value.
- Setting the CC channels overflow action to toggle



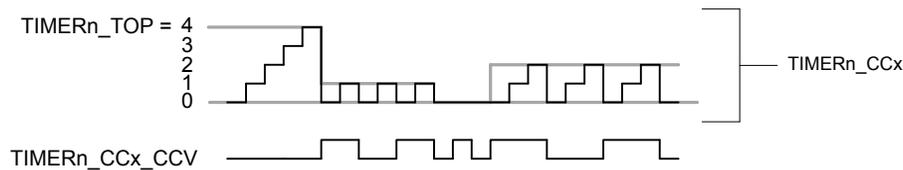
**Figure 21.17. TIMER/WTIMER Up-count Frequency Generation**

The output frequency is given by [Figure 21.18 TIMER/WTIMER Up-count Frequency Generation Equation on page 704](#)

$$f_{FRG} = f_{HFPERCLK} / (2^{(PRESC + 1)} \times (TOP + 1) \times 2)$$

**Figure 21.18. TIMER/WTIMER Up-count Frequency Generation Equation**

The figure below provides cycle accurate timing and event generation information for frequency generation.



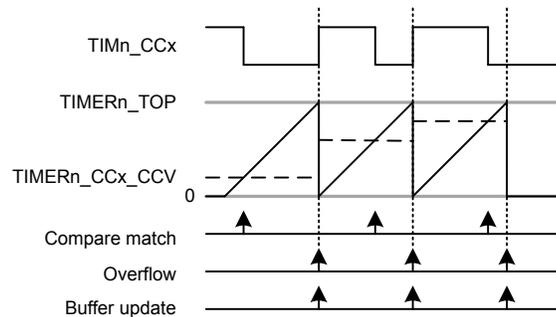
**Figure 21.19. TIMER/WTIMER Up-count Frequency Generation Detail**

### 21.3.2.8 Pulse-Width Modulation (PWM)

In PWM mode, `TIMERn_CCx_CCV` is buffered to avoid glitches in the output. The settings in the Compare Output Action configuration bits are ignored in PWM mode and PWM generation is only supported for up-count and up/down-count mode.

### 21.3.2.9 Up-count (Single-slope) PWM

If the counter is set to up-count and the Compare/Capture channel is put in PWM mode, single slope PWM output will be generated (see [Figure 21.20 TIMER/WTIMER Up-count PWM Generation on page 705](#)). In up-count mode the PWM period is TOP+1 cycles and the PWM output will be high for a number of cycles equal to TIMERn\_CCx\_CCV. This means that a constant high output is achieved by setting TIMERn\_CCx\_CCV to TOP+1 or higher. The PWM resolution (in bits) is then given by [Figure 21.21 TIMER/WTIMER Up-count PWM Resolution Equation on page 705](#).



**Figure 21.20. TIMER/WTIMER Up-count PWM Generation**

$$R_{PWM_{up}} = \log(TOP+1)/\log(2)$$

**Figure 21.21. TIMER/WTIMER Up-count PWM Resolution Equation**

The PWM frequency is given by [Figure 21.22 TIMER/WTIMER Up-count PWM Frequency Equation on page 705](#):

$$f_{PWM_{up/down}} = f_{HFPERCLK} / (2^{PRESC} \times (TOP + 1))$$

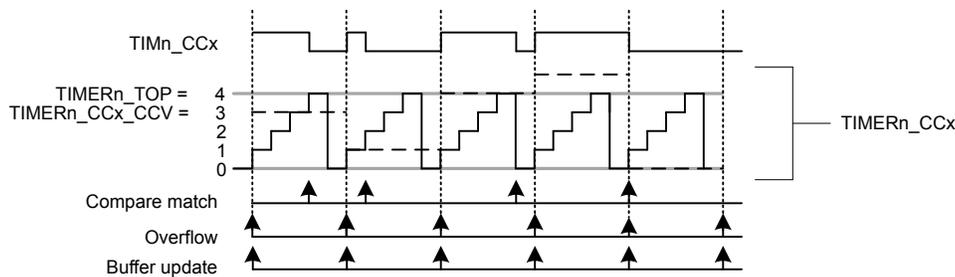
**Figure 21.22. TIMER/WTIMER Up-count PWM Frequency Equation**

The high duty cycle is given by [Figure 21.23 TIMER/WTIMER Up-count Duty Cycle Equation on page 705](#)

$$DS_{up} = CCVx/(TOP+1)$$

**Figure 21.23. TIMER/WTIMER Up-count Duty Cycle Equation**

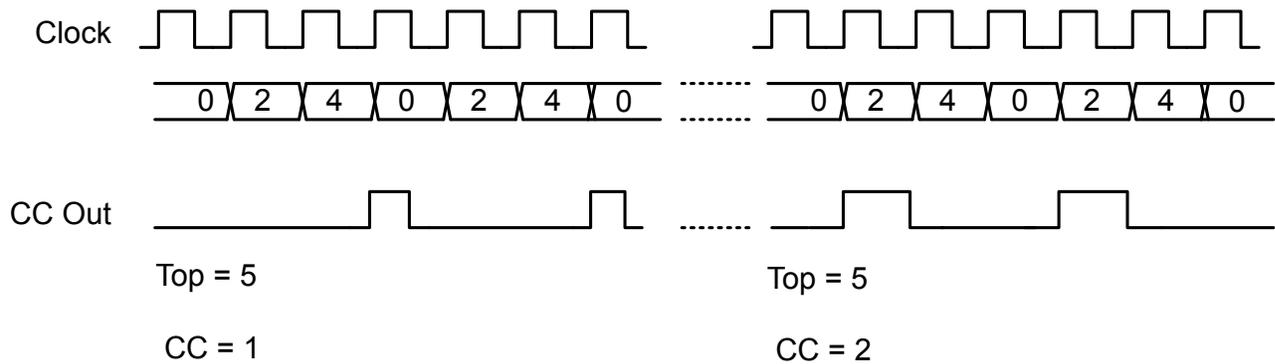
The figure below provides cycle accurate timing and event generation information for up-count mode.



**Figure 21.24. TIMER/WTIMER Up-count PWM Generation Detail**

### 21.3.2.10 2x Count Mode (Up-count)

When the timer is set in 2x mode, the TIMER/WTIMER will count up by two. This will in effect make any odd Top value be rounded down to the closest even number. Similarly, any odd CC value will generate a match on the closest lower even value as shown in [Figure 21.25 TIMER/WTIMER CC out in 2x mode on page 706](#)



**Figure 21.25. TIMER/WTIMER CC out in 2x mode**

The PWM resolution is given by [Figure 21.26 TIMER/WTIMER 2x PWM Resolution Equation on page 706](#).

$$R_{\text{PWM}_{2\text{xmode}}} = \log(\text{TOP}/2+1)/\log(2)$$

**Figure 21.26. TIMER/WTIMER 2x PWM Resolution Equation**

The PWM frequency is given by [Figure 21.27 TIMER/WTIMER 2x Mode PWM Frequency Equation\( Up-count\) on page 706](#):

$$f_{\text{PWM}_{2\text{xmode}}} = f_{\text{HFPERCLK}} / \text{floor}(\text{TOP}/2)+1$$

**Figure 21.27. TIMER/WTIMER 2x Mode PWM Frequency Equation( Up-count)**

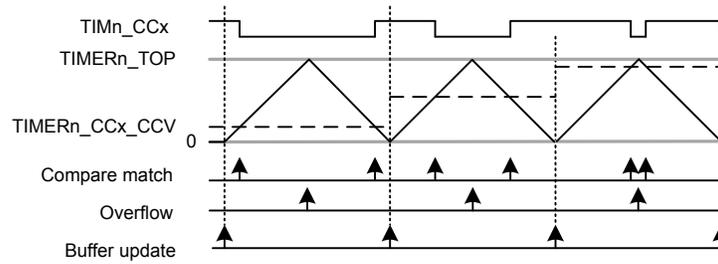
The high duty cycle is given by [Figure 21.28 TIMER/WTIMER 2x Mode Duty Cycle Equation on page 706](#)

$$DS_{2\text{xmode}} = \text{CCVx} / ((\text{floor}(\text{TOP}/2)+1)*2)$$

**Figure 21.28. TIMER/WTIMER 2x Mode Duty Cycle Equation**

### 21.3.2.11 Up/Down-count (Dual-slope) PWM

If the counter is set to up-down count and the Compare/Capture channel is put in PWM mode, dual slope PWM output will be generated by [Figure 21.29 TIMER/WTIMER Up/Down-count PWM Generation on page 707](#). The resolution (in bits) is given by [Figure 21.30 TIMER/WTIMER Up/Down-count PWM Resolution Equation on page 707](#).



**Figure 21.29. TIMER/WTIMER Up/Down-count PWM Generation**

$$R_{PWM_{up/down}} = \log(TOP+1)/\log(2)$$

**Figure 21.30. TIMER/WTIMER Up/Down-count PWM Resolution Equation**

The PWM frequency is given by [Figure 21.31 TIMER/WTIMER Up/Down-count PWM Frequency Equation on page 707](#):

$$f_{PWM_{up/down}} = f_{HFPERCLK} / (2^{(PRESC+1)} \times TOP)$$

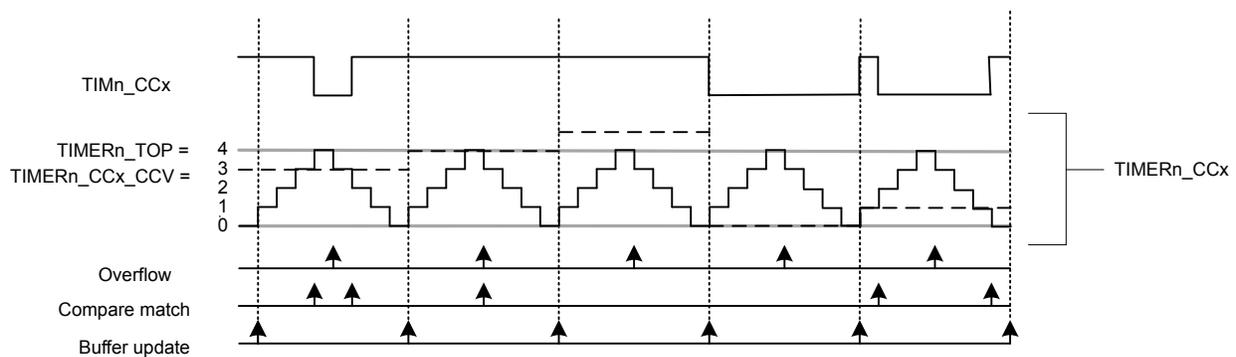
**Figure 21.31. TIMER/WTIMER Up/Down-count PWM Frequency Equation**

The high duty cycle is given by [Figure 21.32 TIMER/WTIMER Up/Down-count Duty Cycle Equation on page 707](#)

$$DS_{up/down} = CCVx/TOP$$

**Figure 21.32. TIMER/WTIMER Up/Down-count Duty Cycle Equation**

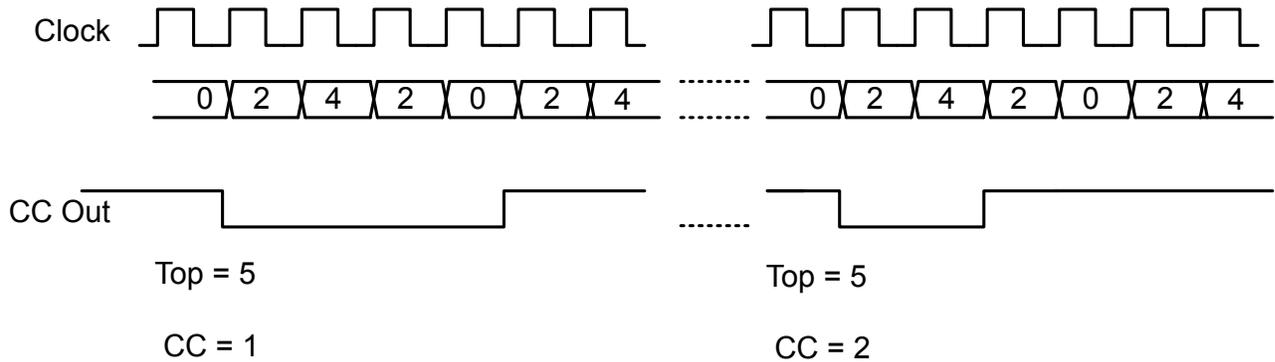
The figure below provides cycle accurate timing and event generation information for up-count mode.



**Figure 21.33. TIMER/WTIMER Up/Down-count PWM Generation**

### 21.3.2.12 2x Count Mode (Up/Down-count)

When the timer is set in 2x mode, the TIMER/WTIMER will count up/down by two. This will in effect make any odd Top value be rounded down to the closest even number. Similarly, any odd CC value will generate a match on the closest lower even value as shown in Figure 21.34 TIMER/WTIMER CC out in 2x mode on page 708



**Figure 21.34. TIMER/WTIMER CC out in 2x mode**

Figure 21.35 TIMER/WTIMER 2x PWM Resolution Equation on page 708.

$$R_{PWM_{2xmode}} = \log(TOP/2+1)/\log(2)$$

**Figure 21.35. TIMER/WTIMER 2x PWM Resolution Equation**

The PWM frequency is given by Figure 21.36 TIMER/WTIMER 2x Mode PWM Frequency Equation( Up/Down-count) on page 708:

$$f_{PWM_{2xmode}} = f_{HFPERCLK} / (\text{floor}(TOP/2)*2)$$

**Figure 21.36. TIMER/WTIMER 2x Mode PWM Frequency Equation( Up/Down-count)**

The high duty cycle is given by two equations based on the CCVx values. Figure 21.37 TIMER/WTIMER 2x Mode Duty Cycle Equation for CCVx = 1 or CCVx = even on page 708 and Figure 21.38 TIMER/WTIMER 2x Mode Duty Cycle Equation for all other CCVx = odd values on page 708

$$DS_{2xmode} = (CCVx*2)/(\text{floor}(TOP/2)*4)$$

**Figure 21.37. TIMER/WTIMER 2x Mode Duty Cycle Equation for CCVx = 1 or CCVx = even**

$$DS_{2xmode} = (CCVx*2 - CCVx)/(\text{floor}(TOP/2)*4)$$

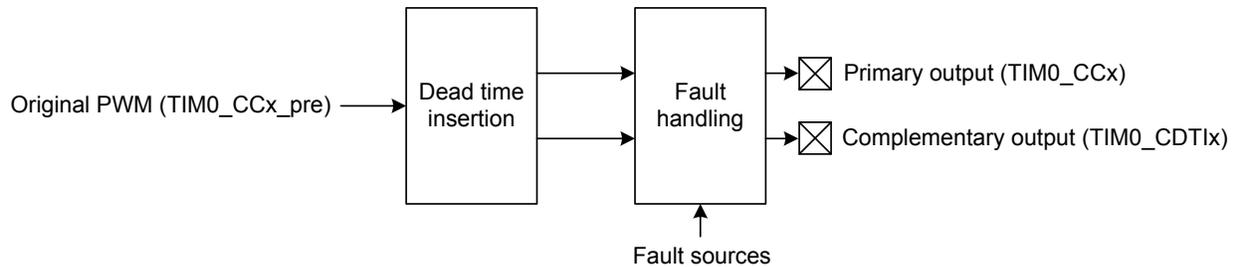
**Figure 21.38. TIMER/WTIMER 2x Mode Duty Cycle Equation for all other CCVx = odd values**

### 21.3.2.13 Timer Configuration Lock

To prevent software errors from making changes to the timer configuration, a configuration lock is available similar to DTI configuration Lock. Writing any value but 0xCE80 to LOCKKEY in TIMERN\_LOCK results in TIMERN\_CTRL, TIMERN\_CMD, TIMERN\_TOP, TIMERN\_CNT, TIMERN\_CCx\_CTRL and TIMERN\_CCx\_CCv being locked from writing. To unlock the registers, write 0xCE80 to LOCKKEY in TIMERN\_LOCK. The value of TIMERN\_LOCK is 1 when the lock is active, and 0 when the registers are unlocked.

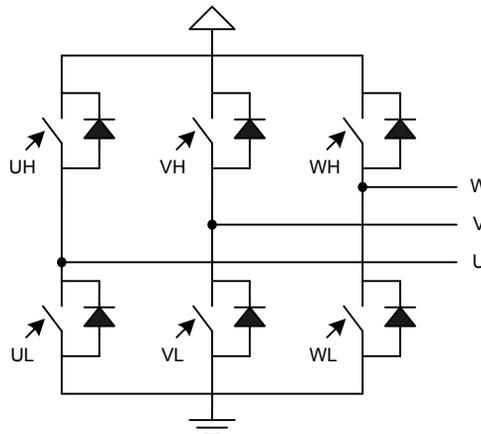
### 21.3.3 Dead-Time Insertion Unit

Some of the timers include a Dead-Time Insertion module suitable for motor control applications. Refer to the device data sheet to check if a timer has this feature. The example settings in this section are for TIMER0, but identical settings can be used for other timers with DTI as well. The Dead-Time Insertion Unit aims to make control of brushless DC (BLDC) motors safer and more efficient by introducing complementary PWM outputs with dead-time insertion and fault handling, see [Figure 21.39 TIMER/WTIMER Dead-Time Insertion Unit Overview on page 709](#).



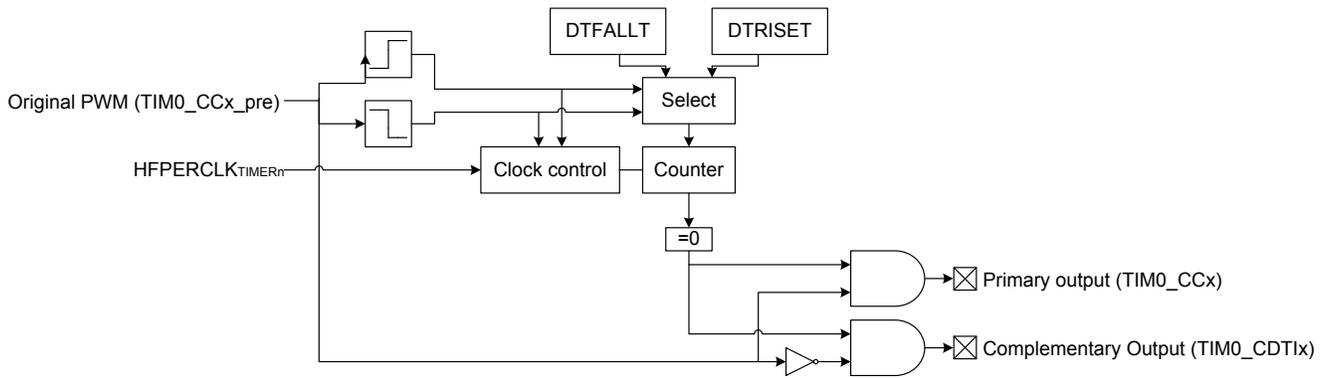
**Figure 21.39. TIMER/WTIMER Dead-Time Insertion Unit Overview**

When used for motor control, the PWM outputs TIM0\_CC0, TIM0\_CC1 and TIM0\_CC2 are often connected to the high-side transistors of a triple half-bridge setup (UH, VH and WH), and the complementary outputs connected to the respective low-side transistors (UL, VL, WL shown in [Figure 21.40 TIMER/WTIMER Triple Half-Bridge on page 709](#)). Transistors used in such a bridge often do not open/close instantaneously, and using the exact complementary inputs for the high and low side of a half-bridge may result in situations where both gates are open. This can give unnecessary current-draw and short circuit the power supply. The DTI unit provides dead-time insertion to deal with this problem.



**Figure 21.40. TIMER/WTIMER Triple Half-Bridge**

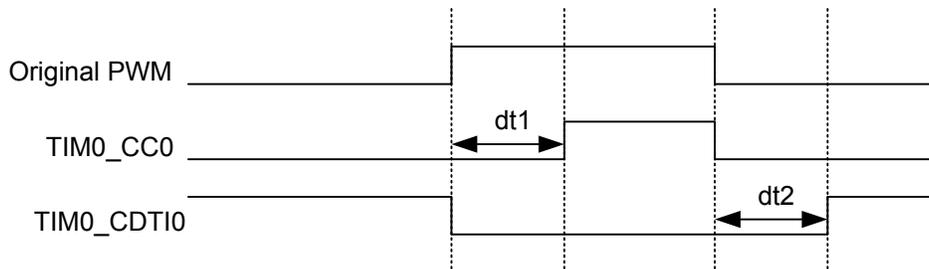
For each of the 3 compare-match outputs of TIMER0, an additional complementary output is provided by the DTI unit. These outputs, named TIM0\_CDTI0, TIM0\_CDTI1 and TIM0\_CDTI2 are provided to make control of e.g. 3-channel BLDC or permanent magnet AC (PMA) motors possible using only a single timer, see [Figure 21.41 TIMER/WTIMER Overview of Dead-Time Insertion Block for a Single PWM channel on page 710](#).



**Figure 21.41. TIMER/WTIMER Overview of Dead-Time Insertion Block for a Single PWM channel**

The DTI unit is enabled by setting DTEN in TIMERO\_DTCTRL. In addition to providing the complementary outputs, the DTI unit then also overrides the compare match outputs from the timer.

The DTI unit gives the rising edges of the PWM outputs and the rising edges of the complementary PWM outputs a configurable time delay. By doing this, the DTI unit introduces a dead-time where both the primary and complementary outputs in a pair are inactive as seen in Figure 21.42 TIMER/WTIMER Polarity of Both Signals are Set as Active-High on page 710.



**Figure 21.42. TIMER/WTIMER Polarity of Both Signals are Set as Active-High**

Dead-time is specified individually for the rising and falling edge of the original PWM. These values are shared across all the three PWM channels of the DTI unit. A single prescaler value is provided for the DTI unit, meaning that both the rising and falling edge dead-times share prescaler value. The prescaler divides the HFPERCLK<sub>TIMERn</sub> by a configurable factor between 1 and 1024, which is set in the DTPRESC field in TIMERO\_DTTIME. The rising and falling edge dead-times are configured in DTRISSET and DTFALLT in TIMERO\_DTTIME to any number between 1-64 HFPERCLK<sub>TIMER0</sub> cycles.

The DTAR and DTFATS bits in TIMERO\_DTCTRL control the DTI output behavior when the timer stops. By default the DTI block stops when the timer is stopped. Setting the DTAR bit will cause the DTI to output on channel 0 to continue when the timer is stopped. DTAR effects only channel 0. See 21.3.3.2 PRS Channel as a Source for an example of when this can be used. While in this mode the undivided HFPERCLK<sub>TIMER0</sub> (DTPRESC=0) is always used regardless of programmed DTPRESC value in TIMERO\_DTTIME. This means that rise and fall dead times are calculated assuming DTPRESC = 0.

When the timer stops DTI outputs are frozen by default, preserving their last state. To allow the outputs to go to a safe state as programmed in the DTFA field of TIMERO\_DTFC register and set the DTFATS bitfield in the TIMERO\_DTCTRL reg. Note that when DTAR is also set, DTAR has priority over DTFATS for DTI channel 0 output.

The following table shows the DTI output when the timer is halted.

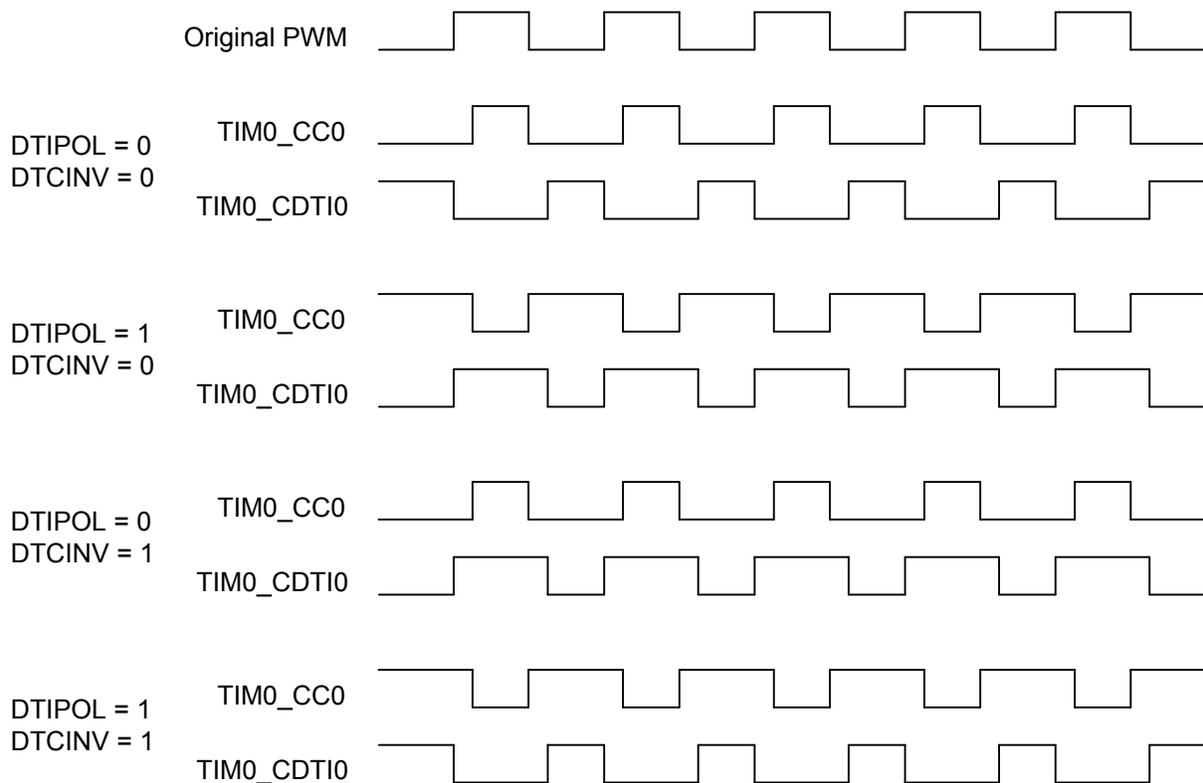
**Table 21.3. DTI Output When Timer Halted**

| DTAR | DTFATS | State   |
|------|--------|---------|
| 0    | 0      | frozen  |
| 0    | 1      | safe    |
| 1    | 0      | running |
| 1    | 1      | running |

**21.3.3.1 Output Polarity**

The value of the primary and complementary outputs in a pair will never be set active at the same time by the DTI unit. The polarity of the outputs can be changed if this is required by the application. The active values of the primary and complementary outputs are set by the DTIPOL and DTCINV bits in the TIMERO\_DTCTRL register. The DTIPOL bit of this register specifies the base polarity. If DTIPOL = 0, then the outputs are active-high, and if DTIPOL = 1 they are active-low. The relative phase of the primary and complementary outputs is not changed by DTIPOL, as the polarity of both outputs is changed, see [Figure 21.43 TIMER/WTIMER Output Polarities on page 711](#).

In some applications, it may be required that the primary outputs are active-high, while the complementary outputs are active-low. This can be accomplished by manipulating the DTCINV bit of the TIMERO\_DTCTRL register, which inverts the polarity of the complementary outputs relative to the primary outputs. As an example, DTIPOL = 0 and DTCINV = 0 results in outputs with opposite phase and active-high states. Similarly, DTIPOL = 1 and DTCINV = 1 results in outputs with equal phase and the primary output will be active-high while the complementary will be active-low.



**Figure 21.43. TIMER/WTIMER Output Polarities**

Output generation on the individual DTI outputs can be disabled by configuring TIMERO\_DTOGEN. When output generation on an output is disabled that output will go to and stay in its inactive state.

### 21.3.3.2 PRS Channel as a Source

A PRS channel can be used as input to the DTI module instead of the PWM output from the timer for DTI channel 0. Setting DTPRSEN in `TIMER0_DTCTRL` will override the source of the first DTI channel, driving `TIM0_CC0` and `TIM0_CDTI0`, with the value on the PRS channel. The rest of the DTI channels will continue to be driven by the PWM output from the timer. The input PRS channel is chosen by configuring `DTPRSSEL` in `TIMER0_DTCTRL`. Note that the timer must be running even when PRS is used as DTI source. However, if it is required to keep the DTI channel 0 running even when the timer is stopped, set `DTAR` in `TIMER0_DTCTRL`. When this bit is set, it uses `DTPRESC=0` regardless of the value programmed in `DTPRESC` in `TIMER0_DTTIME`.

The DTI prescaler, set by `DTPRESC` in `TIMER0_DTTIME` determines the accuracy with which the DTI can insert dead-time into a PRS signal. The maximum dead-time error equals  $2^{DTPRESC}$  clock cycles. With zero prescaling, the inserted dead-times are therefore accurate, but they may be inaccurate for larger prescaler settings.

### 21.3.3.3 Fault Handling

The fault handling system of the DTI unit allows the outputs of the DTI unit to be put in a well-defined state in case of a fault. This hardware fault handling system enables a fast reaction to faults, reducing the possibility of damage to the system.

The fault sources which trigger a fault in the DTI module are determined by the bitfields of `TIMER0_DTFC` register. Any combination of the available error sources can be selected:

- PRS source 0, determined by `DTPRS0FSEL` in `TIMER0_DTFC`
- PRS source 1, determined by `DTPRS1FSEL` in `TIMER0_DTFC`
- Debugger
- Core Lockup

One or two PRS channels can be used as an error source. When PRS source 0 is selected as an error source, `DTPRS0FSEL` determines which PRS channel is used for this source. `DTPRS1FSEL` determines which PRS channel is selected as PRS source 1. Note that for Core Lockup, the `LOCKUPRDIS` in `RMU_CTRL` must be set. Otherwise this will generate a full reset of the chip.

### 21.3.3.4 Action on Fault

When a fault occurs, the bit representing the fault source is set in `TIMER0_DTFAULT` register, and the outputs from the DTI unit are set to a well-defined state. The following options are available, and can be enabled by configuring `DTFACT` in `TIMER0_DTFC`:

- Set outputs to inactive level
- Clear outputs
- Tristate outputs

With the first option enabled, the output state in case of a fault depends on the polarity settings for the individual outputs. An output set to be active high will be set low if a fault is detected, while an output set to be active low will be driven high.

When a fault occurs, the fault source(s) can be read out from `TIMER0_DTFAULT` register.

Additionally a fault action can also be triggered when the timer stops if `DTFATS` in `TIMER0_DTCTRL` is set. This allows the DTI output to go to safe state programmed in `DTFACT` in `TIMER0_DTFC` when timer stops. When `DTAR` and `DTFATS` in `TIMER0_DTCTRL` are both set, DTI channel 0 keeps running even when the timer stops. This is useful when DTI channel 0 has an input coming from PRS.

### 21.3.3.5 Exiting Fault State

When a fault is triggered by the PRS system, software intervention is required to re-enable the outputs of the DTI unit. This is done by manually clearing bits in `TIMER0_DTFAULT` register. If the fault source as determined by checking `TIMER0_DEFAULT` is the debugger alone, the outputs can be automatically restarted when the debugger exits. To enable automatic restart set `DTDAS` in `TIMER0_DCTRL`. When an automatic restart occurs the `DTDBGF` bit in `TIMER0_DTFAULT` will be automatically cleared by hardware. If any other bits in the `TIMER0_DTFAULT` register are set when the hardware clears `DTDBGF` the DTI module will not exit the fault state.

### 21.3.3.6 DTI Configuration Lock

To prevent software errors from making changes to the DTI configuration, a configuration lock is available. Writing any value but `0xCE80` to `LOCKKEY` in `TIMER0_DTLOCK` results in `TIMER0_DTFC`, `TIMER0_DTCTRL`, `TIMER0_DTTIME` and `TIMER0_ROUTE` being locked from writing. To unlock the registers, write `0xCE80` to `LOCKKEY` in `TIMER0_DTLOCK`. The value of `TIMER0_DTLOCK` is 1 when the lock is active, and 0 when the registers are unlocked.

### 21.3.4 Debug Mode

When the CPU is halted in debug mode, the timer can be configured to either continue to run or to be frozen. This is configured in `DEBUGRUN` in `TIMERn_CTRL`.

### 21.3.5 Interrupts, DMA and PRS Output

The timer has 3 different types of output events:

- Counter Underflow
- Counter Overflow
- Compare match or input capture (one per Compare/Capture channel)

Each of the events has its own interrupt flag. Also, there is one interrupt flag for each Compare/Capture channel which is set on buffer overflow in capture mode. Buffer overflow happens when a new capture pushes an old unread capture out of the `TIMERn_CCx_CCV/TIMERn_CCx_CCVB` register pair.

If the interrupt flags are set and the corresponding interrupt enable bits in `TIMERn_IEN` are set high, the timer will send out an interrupt request. Each of the events will also lead to a one `HPPERCLKTIMERn` cycle high pulse on individual PRS outputs. Setting `PRSOCNF` to `LEVEL` in `TIMERn_CCx_CTRL` will make the compare match PRS output follow the compare match output, instead of outputting one `HPPERCLKTIMERn` cycle high pulse. Interrupts are cleared by setting the corresponding bit in the `TIMERn_IFC` register.

Each of the events will also set a DMA request when they occur. The different DMA requests are cleared when certain acknowledge conditions are met, see [Table 21.4 TIMER/WTIMER DMA Events on page 713](#). Events which clear the DMA requests do not clear interrupt flags. Software must still manually clear the interrupt flag if interrupts are in use.

If `DMACLRACT` is set in `TIMERn_CTRL`, the DMA request is cleared when the triggered DMA channel is active, without having to access any timer registers. This is useful in cases where a timer event is used to trigger a DMA transfer that does not target the `CCV` or `CCVB` register.

**Table 21.4. TIMER/WTIMER DMA Events**

| Event              | Acknowledge/Clear  |
|--------------------|--|
| Underflow/Overflow | Read or write to <code>TIMERn_CNT</code> or <code>TIMERn_TOPB</code>         |
| CC 0               | Read or write to <code>TIMERn_CC0_CCV</code> or <code>TIMERn_CC0_CCVB</code> |
| CC 1               | Read or write to <code>TIMERn_CC1_CCV</code> or <code>TIMERn_CC1_CCVB</code> |
| CC 2               | Read or write to <code>TIMERn_CC2_CCV</code> or <code>TIMERn_CC2_CCVB</code> |

### 21.3.6 GPIO Input/Output

The `TIMn_CCx` inputs/outputs and `TIM0_CDTIx` outputs are accessible as alternate functions through GPIO. Each pin connection can be enabled/disabled separately by setting the corresponding `CCxPEN` or `CDTIxPEN` bits in `TIMERn_ROUTE`. The `LOCATION` bits in the same register can be used to move all enabled pins to alternate pins. See the device data sheet for the mapping between block locations (`LOC0`, `LOC1`, etc.) and actual device pins (`PA0`, `PA1`, etc.).

## 21.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name             | Type   | Description                           |
|--------|------------------|--------|---------------------------------------|
| 0x000  | TIMERn_CTRL      | RW     | Control Register                      |
| 0x004  | TIMERn_CMD       | W1     | Command Register                      |
| 0x008  | TIMERn_STATUS    | R      | Status Register                       |
| 0x00C  | TIMERn_IF        | R      | Interrupt Flag Register               |
| 0x010  | TIMERn_IFS       | W1     | Interrupt Flag Set Register           |
| 0x014  | TIMERn_IFC       | (R)W1  | Interrupt Flag Clear Register         |
| 0x018  | TIMERn_IEN       | RW     | Interrupt Enable Register             |
| 0x01C  | TIMERn_TOP       | RWH    | Counter Top Value Register            |
| 0x020  | TIMERn_TOPB      | RW     | Counter Top Value Buffer Register     |
| 0x024  | TIMERn_CNT       | RWH    | Counter Value Register                |
| 0x02C  | TIMERn_LOCK      | RWH    | TIMER Configuration Lock Register     |
| 0x030  | TIMERn_ROUTEPEN  | RW     | I/O Routing Pin Enable Register       |
| 0x034  | TIMERn_ROUTELOC0 | RW     | I/O Routing Location Register         |
| 0x03C  | TIMERn_ROUTELOC2 | RW     | I/O Routing Location Register         |
| 0x060  | TIMERn_CC0_CTRL  | RW     | CC Channel Control Register           |
| 0x064  | TIMERn_CC0_CCV   | RWH(a) | CC Channel Value Register             |
| 0x068  | TIMERn_CC0_CCVP  | R      | CC Channel Value Peek Register        |
| 0x06C  | TIMERn_CC0_CCVB  | RWH    | CC Channel Buffer Register            |
| ...    | TIMERn_CCx_CTRL  | RW     | CC Channel Control Register           |
| ...    | TIMERn_CCx_CCV   | RWH(a) | CC Channel Value Register             |
| ...    | TIMERn_CCx_CCVP  | R      | CC Channel Value Peek Register        |
| ...    | TIMERn_CCx_CCVB  | RWH    | CC Channel Buffer Register            |
| 0x090  | TIMERn_CC3_CTRL  | RW     | CC Channel Control Register           |
| 0x094  | TIMERn_CC3_CCV   | RWH(a) | CC Channel Value Register             |
| 0x098  | TIMERn_CC3_CCVP  | R      | CC Channel Value Peek Register        |
| 0x09C  | TIMERn_CC3_CCVB  | RWH    | CC Channel Buffer Register            |
| 0x0A0  | TIMERn_DTCTRL    | RW     | DTI Control Register                  |
| 0x0A4  | TIMERn_DTTIME    | RW     | DTI Time Control Register             |
| 0x0A8  | TIMERn_DTFC      | RW     | DTI Fault Configuration Register      |
| 0x0AC  | TIMERn_DTOGEN    | RW     | DTI Output Generation Enable Register |
| 0x0B0  | TIMERn_DTFAULT   | R      | DTI Fault Register                    |
| 0x0B4  | TIMERn_DTFAULTC  | W1     | DTI Fault Clear Register              |
| 0x0B8  | TIMERn_DTLOCK    | RWH    | DTI Configuration Lock Register       |

## 21.5 Register Description

### 21.5.1 TIMERN\_CTRL - Control Register

| Offset        | Bit Position |    |          |     |    |    |    |    |    |    |    |    |    |    |        |    |    |            |       |    |    |       |   |   |       |           |          |     |       |      |   |    |      |
|---------------|--------------|----|----------|-----|----|----|----|----|----|----|----|----|----|----|--------|----|----|------------|-------|----|----|-------|---|---|-------|-----------|----------|-----|-------|------|---|----|------|
| 0x000         | 31           | 30 | 29       | 28  | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17     | 16 | 15 | 14         | 13    | 12 | 11 | 10    | 9 | 8 | 7     | 6         | 5        | 4   | 3     | 2    | 1 | 0  |      |
| <b>Reset</b>  |              |    | 0        | 0   |    |    |    |    |    |    |    |    |    |    | 0x0    |    |    | 0          | 0     |    |    | 0x0   |   |   | 0x0   | 0         | 0        | 0   | 0     | 0    |   |    | 0x0  |
| <b>Access</b> |              |    | RW       | RW  |    |    |    |    |    |    |    |    |    |    | RW     |    |    | RW         | RW    |    |    | RW    |   |   | RW    | RW        | RW       | RW  | RW    |      |   | RW |      |
| <b>Name</b>   |              |    | RSSCOIST | ATI |    |    |    |    |    |    |    |    |    |    | CLKSEL |    |    | DISSYNCOUT | X2CNT |    |    | FALLA |   |   | RISEA | DMACLRACT | DEBUGRUN | QDM | OSMEN | SYNC |   |    | MODE |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:30 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 29    | RSSCOIST        | 0   | RW     | <b>Reload-Start Sets Compare Output Initial State</b><br>When set, compare output is set to COIST value at Reload-Start event |
| 28    | ATI             | 0   | RW     | <b>Always Track Inputs</b><br>when set, makes CCPOL always track the polarity of the inputs                                   |
| 27:24 | PRESC           | 0x0   | RW     | <b>Prescaler Setting</b><br>These bits select the prescaling factor.  |
|       | Value           | Mode  |        | Description   |
|       | 0               | DIV1  |        | The HFPERCLK is undivided   |
|       | 1               | DIV2  |        | The HFPERCLK is divided by 2  |
|       | 2               | DIV4  |        | The HFPERCLK is divided by 4  |
|       | 3               | DIV8  |        | The HFPERCLK is divided by 8  |
|       | 4               | DIV16   |        | The HFPERCLK is divided by 16   |
|       | 5               | DIV32   |        | The HFPERCLK is divided by 32   |
|       | 6               | DIV64   |        | The HFPERCLK is divided by 64   |
|       | 7               | DIV128  |        | The HFPERCLK is divided by 128  |
|       | 8               | DIV256  |        | The HFPERCLK is divided by 256  |
|       | 9               | DIV512  |        | The HFPERCLK is divided by 512  |
|       | 10              | DIV1024   |        | The HFPERCLK is divided by 1024   |
| 23:18 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 17:16 | CLKSEL          | 0x0   | RW     | <b>Clock Source Select</b><br>These bits select the clock source for the timer.   |
|       | Value           | Mode  |        | Description   |
|       | 0               | PRESCHFPERCLK   |        | Prescaled HFPERCLK  |

| Bit   | Name            | Reset   | Access                       | Description   |
|-------|-----------------|---|------------------------------|---|
|       | 1               | CC1   |                              | Compare/Capture Channel 1 Input   |
|       | 2               | TIMEROUF  |                              | Timer is clocked by underflow(down-count) or overflow(up-count) in the lower numbered neighbor Timer  |
| 15    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                              |   |
| 14    | DISSYNCOU       | 0   | RW                           | <b>Disable Timer From Start/Stop/Reload Other Synchronized Timers</b><br>When this bit is set, the Timer does not start/stop/reload other timer with SYNC bit set   |
|       | Value           | Description   |                              |   |
|       | 0               | Timer can start/stop/reload other timers with SYNC bit set  |                              |   |
|       | 1               | Timer cannot start/stop/reload other timers with SYNC bit set   |                              |   |
| 13    | X2CNT           | 0   | RW                           | <b>2x Count Mode</b><br>Enable 2x count mode  |
| 12    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                              |   |
| 11:10 | FALLA           | 0x0   | RW                           | <b>Timer Falling Input Edge Action</b><br>These bits select the action taken in the counter when a falling edge occurs on the input.  |
|       | Value           | Mode  | Description                  |   |
|       | 0               | NONE  | No action                    |   |
|       | 1               | START   | Start counter without reload |   |
|       | 2               | STOP  | Stop counter without reload  |   |
|       | 3               | RELOADSTART   | Reload and start counter     |   |
| 9:8   | RISEA           | 0x0   | RW                           | <b>Timer Rising Input Edge Action</b><br>These bits select the action taken in the counter when a rising edge occurs on the input.  |
|       | Value           | Mode  | Description                  |   |
|       | 0               | NONE  | No action                    |   |
|       | 1               | START   | Start counter without reload |   |
|       | 2               | STOP  | Stop counter without reload  |   |
|       | 3               | RELOADSTART   | Reload and start counter     |   |
| 7     | DMACLRACT       | 0   | RW                           | <b>DMA Request Clear on Active</b><br>When this bit is set, the DMA requests are cleared when the corresponding DMA channel is active. This enables the timer DMA requests to be cleared without accessing the timer. |
| 6     | DEBUGRUN        | 0   | RW                           | <b>Debug Mode Run Enable</b><br>Set this bit to enable timer to run in debug mode.  |
|       | Value           | Description   |                              |   |
|       | 0               | Timer is frozen in debug mode   |                              |   |
|       | 1               | Timer is running in debug mode  |                              |   |

| Bit | Name            | Reset   | Access | Description   |
|-----|-----------------|---|--------|---|
| 5   | QDM             | 0   | RW     | <b>Quadrature Decoder Mode Selection</b><br>This bit sets the mode for the quadrature decoder.  |
|     | Value           | Mode  |        | Description   |
|     | 0               | X2  |        | X2 mode selected  |
|     | 1               | X4  |        | X4 mode selected  |
| 4   | OSMEN           | 0   | RW     | <b>One-shot Mode Enable</b><br>Enable/disable one shot mode.  |
| 3   | SYNC            | 0   | RW     | <b>Timer Start/Stop/Reload Synchronization</b><br>When this bit is set, the Timer is started/stopped/reloaded by start/stop/reload commands in the other timers   |
|     | Value           |   |        | Description   |
|     | 0               |   |        | Timer is not started/stopped/reloaded by other timers   |
|     | 1               |   |        | Timer is started/stopped/reloaded by other timers   |
| 2   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 1:0 | MODE            | 0x0   | RW     | <b>Timer Mode</b><br>These bits set the counting mode for the Timer. Note, when Quadrature Decoder Mode is selected (MODE = 'b11), the CLKSEL is don't care. The Timer is clocked by the Decoder Mode clock output. |
|     | Value           | Mode  |        | Description   |
|     | 0               | UP  |        | Up-count mode   |
|     | 1               | DOWN  |        | Down-count mode   |
|     | 2               | UPDOWN  |        | Up/down-count mode  |
|     | 3               | QDEC  |        | Quadrature decoder mode   |

## 21.5.2 TIMERN\_CMD - Command Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |      |       |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|------|-------|---|---|---|---|
| 0x004         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5    | 4     | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | 0    | 0     |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | W1   | W1    |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | STOP | START |   |   |   |   |

| Bit  | Name                                 | Reset   | Access | Description        |
|------|--------------------------------------|---|--------|--------------------|
| 31:2 | Reserved                             | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |                    |
| 1    | STOP<br>Set this bit to stop timer   | 0   | W1     | <b>Stop Timer</b>  |
| 0    | START<br>Set this bit to start timer | 0   | W1     | <b>Start Timer</b> |

## 21.5.3 TIMERN\_STATUS - Status Register

| Offset        | Bit Position |    |    |    |        |        |        |        |    |    |    |    |      |      |      |      |    |    |    |    |        |        |        |        |   |   |   |   |   |       |     |         |   |
|---------------|--------------|----|----|----|--------|--------|--------|--------|----|----|----|----|------|------|------|------|----|----|----|----|--------|--------|--------|--------|---|---|---|---|---|-------|-----|---------|---|
| 0x008         | 31           | 30 | 29 | 28 | 27     | 26     | 25     | 24     | 23 | 22 | 21 | 20 | 19   | 18   | 17   | 16   | 15 | 14 | 13 | 12 | 11     | 10     | 9      | 8      | 7 | 6 | 5 | 4 | 3 | 2     | 1   | 0       |   |
| <b>Reset</b>  |              |    |    |    | 0      | 0      | 0      | 0      |    |    |    |    | 0    | 0    | 0    | 0    |    |    |    |    | 0      | 0      | 0      | 0      |   |   |   |   |   |       | 0   | 0       | 0 |
| <b>Access</b> |              |    |    |    | R      | R      | R      | R      |    |    |    |    | R    | R    | R    | R    |    |    |    |    | R      | R      | R      | R      |   |   |   |   |   |       | R   | R       | R |
| <b>Name</b>   |              |    |    |    | CCPOL3 | CCPOL2 | CCPOL1 | CCPOL0 |    |    |    |    | ICV3 | ICV2 | ICV1 | ICV0 |    |    |    |    | CCVBV3 | CCVBV2 | CCVBV1 | CCVBV0 |   |   |   |   |   | TOPBV | DIR | RUNNING |   |

| Bit   | Name     | Reset  | Access | Description  |       |      |             |   |         |                                    |   |          |                                      |
|-------|----------|--|--------|--|-------|------|-------------|---|---------|------------------------------------|---|----------|--------------------------------------|
| 31:28 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |       |      |             |   |         |                                    |   |          |                                      |
| 27    | CCPOL3   | 0  | R      | <b>CC3 Polarity</b><br><br>In Input Capture mode, this bit indicates the polarity of the edge that triggered capture in TIMERN_CC3_CC3V. In Compare/PWM mode, this bit indicates the polarity of the selected input to CC channel 3. These bits are cleared when CCMODE is written to 0b00 (Off).<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>LOWRISE</td> <td>CC3 polarity low level/rising edge</td> </tr> <tr> <td>1</td> <td>HIGHFALL</td> <td>CC3 polarity high level/falling edge</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | LOWRISE | CC3 polarity low level/rising edge | 1 | HIGHFALL | CC3 polarity high level/falling edge |
| Value | Mode     | Description  |        |  |       |      |             |   |         |                                    |   |          |                                      |
| 0     | LOWRISE  | CC3 polarity low level/rising edge   |        |  |       |      |             |   |         |                                    |   |          |                                      |
| 1     | HIGHFALL | CC3 polarity high level/falling edge   |        |  |       |      |             |   |         |                                    |   |          |                                      |
| 26    | CCPOL2   | 0  | R      | <b>CC2 Polarity</b><br><br>In Input Capture mode, this bit indicates the polarity of the edge that triggered capture in TIMERN_CC2_CC2V. In Compare/PWM mode, this bit indicates the polarity of the selected input to CC channel 2. These bits are cleared when CCMODE is written to 0b00 (Off).<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>LOWRISE</td> <td>CC2 polarity low level/rising edge</td> </tr> <tr> <td>1</td> <td>HIGHFALL</td> <td>CC2 polarity high level/falling edge</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | LOWRISE | CC2 polarity low level/rising edge | 1 | HIGHFALL | CC2 polarity high level/falling edge |
| Value | Mode     | Description  |        |  |       |      |             |   |         |                                    |   |          |                                      |
| 0     | LOWRISE  | CC2 polarity low level/rising edge   |        |  |       |      |             |   |         |                                    |   |          |                                      |
| 1     | HIGHFALL | CC2 polarity high level/falling edge   |        |  |       |      |             |   |         |                                    |   |          |                                      |
| 25    | CCPOL1   | 0  | R      | <b>CC1 Polarity</b><br><br>In Input Capture mode, this bit indicates the polarity of the edge that triggered capture in TIMERN_CC1_CC1V. In Compare/PWM mode, this bit indicates the polarity of the selected input to CC channel 1. These bits are cleared when CCMODE is written to 0b00 (Off).<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>LOWRISE</td> <td>CC1 polarity low level/rising edge</td> </tr> <tr> <td>1</td> <td>HIGHFALL</td> <td>CC1 polarity high level/falling edge</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | LOWRISE | CC1 polarity low level/rising edge | 1 | HIGHFALL | CC1 polarity high level/falling edge |
| Value | Mode     | Description  |        |  |       |      |             |   |         |                                    |   |          |                                      |
| 0     | LOWRISE  | CC1 polarity low level/rising edge   |        |  |       |      |             |   |         |                                    |   |          |                                      |
| 1     | HIGHFALL | CC1 polarity high level/falling edge   |        |  |       |      |             |   |         |                                    |   |          |                                      |
| 24    | CCPOL0   | 0  | R      | <b>CC0 Polarity</b><br><br>In Input Capture mode, this bit indicates the polarity of the edge that triggered capture in TIMERN_CC0_CC0V. In Compare/PWM mode, this bit indicates the polarity of the selected input to CC channel 0. These bits are cleared when CCMODE is written to 0b00 (Off).<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>LOWRISE</td> <td>CC0 polarity low level/rising edge</td> </tr> <tr> <td>1</td> <td>HIGHFALL</td> <td>CC0 polarity high level/falling edge</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | LOWRISE | CC0 polarity low level/rising edge | 1 | HIGHFALL | CC0 polarity high level/falling edge |
| Value | Mode     | Description  |        |  |       |      |             |   |         |                                    |   |          |                                      |
| 0     | LOWRISE  | CC0 polarity low level/rising edge   |        |  |       |      |             |   |         |                                    |   |          |                                      |
| 1     | HIGHFALL | CC0 polarity high level/falling edge   |        |  |       |      |             |   |         |                                    |   |          |                                      |

| Bit   | Name   | Reset   | Access | Description   |       |             |   |   |   |  |
|-------|--|---|--------|---|-------|-------------|---|---|---|--|
| 23:20 | <i>Reserved</i>  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |             |   |   |   |  |
| 19    | ICV3   | 0   | R      | <b>CC3 Input Capture Valid</b><br><br>This bit indicates that TIMERN_CC3_CCV contains a valid capture value. These bits are only used in input capture mode and are cleared when CCMODE is written to 0b00 (Off).<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>TIMERN_CC3_CCV does not contain a valid capture value(FIFO empty)</td> </tr> <tr> <td>1</td> <td>TIMERN_CC3_CCV contains a valid capture value(FIFO not empty)</td> </tr> </tbody> </table>   | Value | Description | 0 | TIMERN_CC3_CCV does not contain a valid capture value(FIFO empty) | 1 | TIMERN_CC3_CCV contains a valid capture value(FIFO not empty)  |
| Value | Description  |   |        |   |       |             |   |   |   |  |
| 0     | TIMERN_CC3_CCV does not contain a valid capture value(FIFO empty)                                    |   |        |   |       |             |   |   |   |  |
| 1     | TIMERN_CC3_CCV contains a valid capture value(FIFO not empty)  |   |        |   |       |             |   |   |   |  |
| 18    | ICV2   | 0   | R      | <b>CC2 Input Capture Valid</b><br><br>This bit indicates that TIMERN_CC2_CCV contains a valid capture value. These bits are only used in input capture mode and are cleared when CCMODE is written to 0b00 (Off).<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>TIMERN_CC2_CCV does not contain a valid capture value(FIFO empty)</td> </tr> <tr> <td>1</td> <td>TIMERN_CC2_CCV contains a valid capture value(FIFO not empty)</td> </tr> </tbody> </table>   | Value | Description | 0 | TIMERN_CC2_CCV does not contain a valid capture value(FIFO empty) | 1 | TIMERN_CC2_CCV contains a valid capture value(FIFO not empty)  |
| Value | Description  |   |        |   |       |             |   |   |   |  |
| 0     | TIMERN_CC2_CCV does not contain a valid capture value(FIFO empty)                                    |   |        |   |       |             |   |   |   |  |
| 1     | TIMERN_CC2_CCV contains a valid capture value(FIFO not empty)  |   |        |   |       |             |   |   |   |  |
| 17    | ICV1   | 0   | R      | <b>CC1 Input Capture Valid</b><br><br>This bit indicates that TIMERN_CC1_CCV contains a valid capture value. These bits are only used in input capture mode and are cleared when CCMODE is written to 0b00 (Off).<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>TIMERN_CC1_CCV does not contain a valid capture value(FIFO empty)</td> </tr> <tr> <td>1</td> <td>TIMERN_CC1_CCV contains a valid capture value(FIFO not empty)</td> </tr> </tbody> </table>   | Value | Description | 0 | TIMERN_CC1_CCV does not contain a valid capture value(FIFO empty) | 1 | TIMERN_CC1_CCV contains a valid capture value(FIFO not empty)  |
| Value | Description  |   |        |   |       |             |   |   |   |  |
| 0     | TIMERN_CC1_CCV does not contain a valid capture value(FIFO empty)                                    |   |        |   |       |             |   |   |   |  |
| 1     | TIMERN_CC1_CCV contains a valid capture value(FIFO not empty)  |   |        |   |       |             |   |   |   |  |
| 16    | ICV0   | 0   | R      | <b>CC0 Input Capture Valid</b><br><br>This bit indicates that TIMERN_CC0_CCV contains a valid capture value. These bits are only used in input capture mode and are cleared when CCMODE is written to 0b00 (Off).<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>TIMERN_CC0_CCV does not contain a valid capture value(FIFO empty)</td> </tr> <tr> <td>1</td> <td>TIMERN_CC0_CCV contains a valid capture value(FIFO not empty)</td> </tr> </tbody> </table>   | Value | Description | 0 | TIMERN_CC0_CCV does not contain a valid capture value(FIFO empty) | 1 | TIMERN_CC0_CCV contains a valid capture value(FIFO not empty)  |
| Value | Description  |   |        |   |       |             |   |   |   |  |
| 0     | TIMERN_CC0_CCV does not contain a valid capture value(FIFO empty)                                    |   |        |   |       |             |   |   |   |  |
| 1     | TIMERN_CC0_CCV contains a valid capture value(FIFO not empty)  |   |        |   |       |             |   |   |   |  |
| 15:12 | <i>Reserved</i>  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |             |   |   |   |  |
| 11    | CCVBV3   | 0   | R      | <b>CC3 CCVB Valid</b><br><br>This field indicates that the TIMERN_CC3_CCVB registers contain data which have not been written to TIMERN_CC3_CCV. These bits are only used in output compare/PWM mode and are cleared when CCMODE is written to 0b00 (Off).<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>TIMERN_CC3_CCVB does not contain valid data</td> </tr> <tr> <td>1</td> <td>TIMERN_CC3_CCVB contains valid data which will be written to TIMERN_CC3_CCV on the next update event</td> </tr> </tbody> </table> | Value | Description | 0 | TIMERN_CC3_CCVB does not contain valid data                       | 1 | TIMERN_CC3_CCVB contains valid data which will be written to TIMERN_CC3_CCV on the next update event |
| Value | Description  |   |        |   |       |             |   |   |   |  |
| 0     | TIMERN_CC3_CCVB does not contain valid data  |   |        |   |       |             |   |   |   |  |
| 1     | TIMERN_CC3_CCVB contains valid data which will be written to TIMERN_CC3_CCV on the next update event |   |        |   |       |             |   |   |   |  |

| Bit   | Name   | Reset   | Access | Description   |       |             |             |   |    |  |   |      |               |
|-------|--|---|--------|---|-------|-------------|-------------|---|----|--|---|------|---------------|
| 10    | CCVBV2   | 0   | R      | <b>CC2 CCVB Valid</b><br><br>This field indicates that the TIMERN_CC2_CCVB registers contain data which have not been written to TIMERN_CC2_CCV. These bits are only used in output compare/PWM mode and are cleared when CCMODE is written to 0b00 (Off).<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>TIMERN_CC2_CCVB does not contain valid data</td> </tr> <tr> <td>1</td> <td>TIMERN_CC2_CCVB contains valid data which will be written to TIMERN_CC2_CCV on the next update event</td> </tr> </tbody> </table> | Value | Description | 0           | TIMERN_CC2_CCVB does not contain valid data | 1  | TIMERN_CC2_CCVB contains valid data which will be written to TIMERN_CC2_CCV on the next update event |   |      |               |
| Value | Description  |   |        |   |       |             |             |   |    |  |   |      |               |
| 0     | TIMERN_CC2_CCVB does not contain valid data  |   |        |   |       |             |             |   |    |  |   |      |               |
| 1     | TIMERN_CC2_CCVB contains valid data which will be written to TIMERN_CC2_CCV on the next update event |   |        |   |       |             |             |   |    |  |   |      |               |
| 9     | CCVBV1   | 0   | R      | <b>CC1 CCVB Valid</b><br><br>This field indicates that the TIMERN_CC1_CCVB registers contain data which have not been written to TIMERN_CC1_CCV. These bits are only used in output compare/PWM mode and are cleared when CCMODE is written to 0b00 (Off).<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>TIMERN_CC1_CCVB does not contain valid data</td> </tr> <tr> <td>1</td> <td>TIMERN_CC1_CCVB contains valid data which will be written to TIMERN_CC1_CCV on the next update event</td> </tr> </tbody> </table> | Value | Description | 0           | TIMERN_CC1_CCVB does not contain valid data | 1  | TIMERN_CC1_CCVB contains valid data which will be written to TIMERN_CC1_CCV on the next update event |   |      |               |
| Value | Description  |   |        |   |       |             |             |   |    |  |   |      |               |
| 0     | TIMERN_CC1_CCVB does not contain valid data  |   |        |   |       |             |             |   |    |  |   |      |               |
| 1     | TIMERN_CC1_CCVB contains valid data which will be written to TIMERN_CC1_CCV on the next update event |   |        |   |       |             |             |   |    |  |   |      |               |
| 8     | CCVBV0   | 0   | R      | <b>CC0 CCVB Valid</b><br><br>This field indicates that the TIMERN_CC0_CCVB registers contain data which have not been written to TIMERN_CC0_CCV. These bits are only used in output compare/PWM mode and are cleared when CCMODE is written to 0b00 (Off).<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>TIMERN_CC0_CCVB does not contain valid data</td> </tr> <tr> <td>1</td> <td>TIMERN_CC0_CCVB contains valid data which will be written to TIMERN_CC0_CCV on the next update event</td> </tr> </tbody> </table> | Value | Description | 0           | TIMERN_CC0_CCVB does not contain valid data | 1  | TIMERN_CC0_CCVB contains valid data which will be written to TIMERN_CC0_CCV on the next update event |   |      |               |
| Value | Description  |   |        |   |       |             |             |   |    |  |   |      |               |
| 0     | TIMERN_CC0_CCVB does not contain valid data  |   |        |   |       |             |             |   |    |  |   |      |               |
| 1     | TIMERN_CC0_CCVB contains valid data which will be written to TIMERN_CC0_CCV on the next update event |   |        |   |       |             |             |   |    |  |   |      |               |
| 7:3   | <i>Reserved</i>  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |             |             |   |    |  |   |      |               |
| 2     | TOPBV  | 0   | R      | <b>TOPB Valid</b><br><br>This indicates that TIMERN_TOPB contains valid data that has not been written to TIMERN_TOP. This bit is also cleared when TIMERN_TOP is written.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>TIMERN_TOPB does not contain valid data</td> </tr> <tr> <td>1</td> <td>TIMERN_TOPB contains valid data which will be written to TIMERN_TOP on the next update event</td> </tr> </tbody> </table>   | Value | Description | 0           | TIMERN_TOPB does not contain valid data     | 1  | TIMERN_TOPB contains valid data which will be written to TIMERN_TOP on the next update event         |   |      |               |
| Value | Description  |   |        |   |       |             |             |   |    |  |   |      |               |
| 0     | TIMERN_TOPB does not contain valid data  |   |        |   |       |             |             |   |    |  |   |      |               |
| 1     | TIMERN_TOPB contains valid data which will be written to TIMERN_TOP on the next update event         |   |        |   |       |             |             |   |    |  |   |      |               |
| 1     | DIR  | 0   | R      | <b>Direction</b><br><br>Indicates count direction.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>UP</td> <td>Counting up</td> </tr> <tr> <td>1</td> <td>DOWN</td> <td>Counting down</td> </tr> </tbody> </table>  | Value | Mode        | Description | 0   | UP | Counting up  | 1 | DOWN | Counting down |
| Value | Mode   | Description   |        |   |       |             |             |   |    |  |   |      |               |
| 0     | UP   | Counting up   |        |   |       |             |             |   |    |  |   |      |               |
| 1     | DOWN   | Counting down   |        |   |       |             |             |   |    |  |   |      |               |

| Bit | Name    | Reset | Access | Description   |
|-----|---------|-------|--------|---|
| 0   | RUNNING | 0     | R      | <b>Running</b><br>Indicates if timer is running or not. |

#### 21.5.4 TIMERN\_IF - Interrupt Flag Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |        |        |        |     |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |        |    |    |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|--------|--------|--------|-----|-----|-----|-----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------|----|----|---|
| 0x00C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11     | 10     | 9      | 8      | 7   | 6   | 5   | 4   | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |        |    |    |   |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R      | 0      | R      | 0      | R   | 0   | R   | 0   | R | 0 | R | 0 | R | 0 | R | 0 | R | 0 | R | 0 | R | 0 | R | 0 | R | 0 | R      | 0  | R  | 0 |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R      |        | R      |        | R   |     | R   |     | R |   | R |   | R |   | R |   | R |   | R |   | R |   | R |   | R |   | R      |    | R  |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | ICBOF3 | ICBOF2 | ICBOF1 | ICBOF0 | CC3 | CC2 | CC1 | CC0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | DIRCHG | UF | OF |   |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 31:12 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 11    | ICBOF3          | 0   | R      | <b>CC Channel 3 Input Capture Buffer Overflow Interrupt Flag</b><br>This bit indicates that a new capture value has pushed an unread value out of TIMERN_CC3_CCVB. |
| 10    | ICBOF2          | 0   | R      | <b>CC Channel 2 Input Capture Buffer Overflow Interrupt Flag</b><br>This bit indicates that a new capture value has pushed an unread value out of TIMERN_CC2_CCVB. |
| 9     | ICBOF1          | 0   | R      | <b>CC Channel 1 Input Capture Buffer Overflow Interrupt Flag</b><br>This bit indicates that a new capture value has pushed an unread value out of TIMERN_CC1_CCVB. |
| 8     | ICBOF0          | 0   | R      | <b>CC Channel 0 Input Capture Buffer Overflow Interrupt Flag</b><br>This bit indicates that a new capture value has pushed an unread value out of TIMERN_CC0_CCVB. |
| 7     | CC3             | 0   | R      | <b>CC Channel 3 Interrupt Flag</b><br>This bit indicates that there has been an interrupt event on Compare/Capture channel 3.                                      |
| 6     | CC2             | 0   | R      | <b>CC Channel 2 Interrupt Flag</b><br>This bit indicates that there has been an interrupt event on Compare/Capture channel 2.                                      |
| 5     | CC1             | 0   | R      | <b>CC Channel 1 Interrupt Flag</b><br>This bit indicates that there has been an interrupt event on Compare/Capture channel 1.                                      |
| 4     | CC0             | 0   | R      | <b>CC Channel 0 Interrupt Flag</b><br>This bit indicates that there has been an interrupt event on Compare/Capture channel 0.                                      |
| 3     | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 2     | DIRCHG          | 0   | R      | <b>Direction Change Detect Interrupt Flag</b><br>This bit is set when count direction changes. Set only in Quadrature Decoder mode                                 |
| 1     | UF              | 0   | R      | <b>Underflow Interrupt Flag</b><br>This bit indicates that there has been an underflow.  |
| 0     | OF              | 0   | R      | <b>Overflow Interrupt Flag</b><br>This bit indicates that there has been an overflow.  |



## 21.5.6 TIMERN\_IFC - Interrupt Flag Clear Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |        |        |        |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |        |       |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|--------|-------|----|
| 0x014         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14     | 13     | 12     | 11    | 10    | 9     | 8     | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |        |       |    |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0      | 0      | 0      | 0      | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0      |       |    |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | (R)W1  | (R)W1  | (R)W1  | (R)W1  | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1  | (R)W1 |    |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | ICBOF3 | ICBOF2 | ICBOF1 | ICBOF0 | CC3   | CC2   | CC1   | CC0   |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       | DIRCHG | UF    | OF |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:12 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in 1.2 Conventions</i> |        |   |
| 11    | ICBOF3          | 0   | (R)W1  | <b>Clear ICBOF3 Interrupt Flag</b><br><br>Write 1 to clear the ICBOF3 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 10    | ICBOF2          | 0   | (R)W1  | <b>Clear ICBOF2 Interrupt Flag</b><br><br>Write 1 to clear the ICBOF2 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 9     | ICBOF1          | 0   | (R)W1  | <b>Clear ICBOF1 Interrupt Flag</b><br><br>Write 1 to clear the ICBOF1 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 8     | ICBOF0          | 0   | (R)W1  | <b>Clear ICBOF0 Interrupt Flag</b><br><br>Write 1 to clear the ICBOF0 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 7     | CC3             | 0   | (R)W1  | <b>Clear CC3 Interrupt Flag</b><br><br>Write 1 to clear the CC3 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).       |
| 6     | CC2             | 0   | (R)W1  | <b>Clear CC2 Interrupt Flag</b><br><br>Write 1 to clear the CC2 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).       |
| 5     | CC1             | 0   | (R)W1  | <b>Clear CC1 Interrupt Flag</b><br><br>Write 1 to clear the CC1 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).       |
| 4     | CC0             | 0   | (R)W1  | <b>Clear CC0 Interrupt Flag</b><br><br>Write 1 to clear the CC0 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).       |
| 3     | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in 1.2 Conventions</i> |        |   |
| 2     | DIRCHG          | 0   | (R)W1  | <b>Clear DIRCHG Interrupt Flag</b><br><br>Write 1 to clear the DIRCHG interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |

| Bit | Name | Reset | Access | Description   |
|-----|------|-------|--------|---|
| 1   | UF   | 0     | (R)W1  | <b>Clear UF Interrupt Flag</b><br><br>Write 1 to clear the UF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 0   | OF   | 0     | (R)W1  | <b>Clear OF Interrupt Flag</b><br><br>Write 1 to clear the OF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |

## 21.5.7 TIMERN\_IEN - Interrupt Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |        |        |        |     |     |     |     |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |    |    |    |    |    |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|--------|--------|--------|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|----|----|----|--|
| 0x018         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11     | 10     | 9      | 8      | 7   | 6   | 5   | 4   | 3  | 2  | 1  | 0  |    |    |    |    |    |    |    |    |        |    |    |    |    |    |    |    |    |    |    |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0      | 0      | 0      | 0      | 0   | 0   | 0   | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW     | RW     | RW     | RW     | RW  | RW  | RW  | RW  | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW     | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | ICBOF3 | ICBOF2 | ICBOF1 | ICBOF0 | CC3 | CC2 | CC1 | CC0 |    |    |    |    |    |    |    |    |    |    |    |    | DIRCHG | UF | OF |    |    |    |    |    |    |    |    |  |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:12 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 11    | ICBOF3          | 0   | RW     | <b>ICBOF3 Interrupt Enable</b><br>Enable/disable the ICBOF3 interrupt |
| 10    | ICBOF2          | 0   | RW     | <b>ICBOF2 Interrupt Enable</b><br>Enable/disable the ICBOF2 interrupt |
| 9     | ICBOF1          | 0   | RW     | <b>ICBOF1 Interrupt Enable</b><br>Enable/disable the ICBOF1 interrupt |
| 8     | ICBOF0          | 0   | RW     | <b>ICBOF0 Interrupt Enable</b><br>Enable/disable the ICBOF0 interrupt |
| 7     | CC3             | 0   | RW     | <b>CC3 Interrupt Enable</b><br>Enable/disable the CC3 interrupt       |
| 6     | CC2             | 0   | RW     | <b>CC2 Interrupt Enable</b><br>Enable/disable the CC2 interrupt       |
| 5     | CC1             | 0   | RW     | <b>CC1 Interrupt Enable</b><br>Enable/disable the CC1 interrupt       |
| 4     | CC0             | 0   | RW     | <b>CC0 Interrupt Enable</b><br>Enable/disable the CC0 interrupt       |
| 3     | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 2     | DIRCHG          | 0   | RW     | <b>DIRCHG Interrupt Enable</b><br>Enable/disable the DIRCHG interrupt |
| 1     | UF              | 0   | RW     | <b>UF Interrupt Enable</b><br>Enable/disable the UF interrupt         |
| 0     | OF              | 0   | RW     | <b>OF Interrupt Enable</b><br>Enable/disable the OF interrupt         |

**21.5.8 TIMERN\_TOP - Counter Top Value Register**

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x01C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000FFFF |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | TOP        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name | Reset      | Access | Description              |
|--|------|------------|--------|--------------------------|
| 31:0   | TOP  | 0x0000FFFF | RWH    | <b>Counter Top Value</b> |
| These bits hold the TOP value for the counter. |      |            |        |                          |

**21.5.9 TIMERN\_TOPB - Counter Top Value Buffer Register**

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x020         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | TOPB       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit                                   | Name | Reset      | Access | Description                     |
|---------------------------------------|------|------------|--------|---------------------------------|
| 31:0                                  | TOPB | 0x00000000 | RW     | <b>Counter Top Value Buffer</b> |
| These bits hold the TOP buffer value. |      |            |        |                                 |

### 21.5.10 TIMERN\_CNT - Counter Value Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x024         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CNT        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit                                | Name | Reset      | Access | Description          |
|------------------------------------|------|------------|--------|----------------------|
| 31:0                               | CNT  | 0x00000000 | RWH    | <b>Counter Value</b> |
| These bits hold the counter value. |      |            |        |                      |

### 21.5.11 TIMERN\_LOCK - TIMER Configuration Lock Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |              |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x02C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15           | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | TIMERLOCKKEY |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name            | Reset   | Access | Description           |
|---|-----------------|---|--------|-----------------------|
| 31:16   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |                       |
| 15:0  | TIMERLOCKKEY    | 0x0000  | RWH    | <b>Timer Lock Key</b> |
| Write any other value than the unlock code to lock TIMERN_CTRL, TIMERN_CMD, TIMERN_TOP, TIMERN_CNT, TIMERN_CCx_CTRL and TIMERN_CCx_CCV from editing. Write the unlock code to unlock. When reading the register, bit 0 is set when the lock is enabled. |                 |   |        |                       |

| Mode            | Value  | Description                  |
|-----------------|--------|------------------------------|
| Read Operation  |        |                              |
| UNLOCKED        | 0      | TIMER registers are unlocked |
| LOCKED          | 1      | TIMER registers are locked   |
| Write Operation |        |                              |
| LOCK            | 0      | Lock TIMER registers         |
| UNLOCK          | 0xCE80 | Unlock TIMER registers       |

## 21.5.12 TIMERN\_ROUTE PEN - I/O Routing Pin Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |          |          |   |   |   |   |   |   |   |   |   |  |  |  |  |        |        |        |        |  |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|----------|----------|---|---|---|---|---|---|---|---|---|--|--|--|--|--------|--------|--------|--------|--|--|--|
| 0x030         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11       | 10       | 9        | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |        |        |        |        |  |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0        | 0        | 0        |   |   |   |   |   |   |   |   |   |  |  |  |  | 0      | 0      | 0      |        |  |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW       | RW       | RW       |   |   |   |   |   |   |   |   |   |  |  |  |  | RW     | RW     | RW     |        |  |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CDTI2PEN | CDTI1PEN | CDTI0PEN |   |   |   |   |   |   |   |   |   |  |  |  |  | CC3PEN | CC2PEN | CC1PEN | CC0PEN |  |  |  |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:11 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 10    | CDTI2PEN        | 0   | RW     | <b>CC Channel 2 Complementary Dead-Time Insertion Pin Enable</b><br>Enable/disable CC channel 2 complementary dead-time insertion output connection to pin. |
| 9     | CDTI1PEN        | 0   | RW     | <b>CC Channel 1 Complementary Dead-Time Insertion Pin Enable</b><br>Enable/disable CC channel 1 complementary dead-time insertion output connection to pin. |
| 8     | CDTI0PEN        | 0   | RW     | <b>CC Channel 0 Complementary Dead-Time Insertion Pin Enable</b><br>Enable/disable CC channel 0 complementary dead-time insertion output connection to pin. |
| 7:4   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 3     | CC3PEN          | 0   | RW     | <b>CC Channel 3 Pin Enable</b><br>Enable/disable CC channel 3 output/input connection to pin.   |
| 2     | CC2PEN          | 0   | RW     | <b>CC Channel 2 Pin Enable</b><br>Enable/disable CC channel 2 output/input connection to pin.   |
| 1     | CC1PEN          | 0   | RW     | <b>CC Channel 1 Pin Enable</b><br>Enable/disable CC channel 1 output/input connection to pin.   |
| 0     | CC0PEN          | 0   | RW     | <b>CC Channel 0 Pin Enable</b><br>Enable/disable CC Channel 0 output/input connection to pin.   |

21.5.13 TIMERN\_ROUTELOC0 - I/O Routing Location Register

| Offset        | Bit Position |    |    |    |        |    |    |    |    |    |    |    |        |    |    |    |    |    |    |    |        |    |   |   |   |   |   |   |   |   |        |   |  |
|---------------|--------------|----|----|----|--------|----|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|--------|----|---|---|---|---|---|---|---|---|--------|---|--|
| 0x034         | 31           | 30 | 29 | 28 | 27     | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19     | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11     | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1      | 0 |  |
| <b>Reset</b>  |              |    |    |    | 0x00   |    |    |    |    |    |    |    | 0x00   |    |    |    |    |    |    |    | 0x00   |    |   |   |   |   |   |   |   |   | 0x00   |   |  |
| <b>Access</b> |              |    |    |    | RW     |    |    |    |    |    |    |    | RW     |    |    |    |    |    |    |    | RW     |    |   |   |   |   |   |   |   |   | RW     |   |  |
| <b>Name</b>   |              |    |    |    | CC3LOC |    |    |    |    |    |    |    | CC2LOC |    |    |    |    |    |    |    | CC1LOC |    |   |   |   |   |   |   |   |   | CC0LOC |   |  |

| Bit   | Name     | Reset  | Access | Description |
|-------|----------|--|--------|-------------|
| 31:30 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |             |

|       |        |      |    |   |
|-------|--------|------|----|---|
| 29:24 | CC3LOC | 0x00 | RW | <b>I/O Location</b><br>Decides the location of the CC3 pin. |
|-------|--------|------|----|---|

| Value | Mode  | Description |
|-------|-------|-------------|
| 0     | LOC0  | Location 0  |
| 1     | LOC1  | Location 1  |
| 2     | LOC2  | Location 2  |
| 3     | LOC3  | Location 3  |
| 4     | LOC4  | Location 4  |
| 5     | LOC5  | Location 5  |
| 6     | LOC6  | Location 6  |
| 7     | LOC7  | Location 7  |
| 8     | LOC8  | Location 8  |
| 9     | LOC9  | Location 9  |
| 10    | LOC10 | Location 10 |
| 11    | LOC11 | Location 11 |
| 12    | LOC12 | Location 12 |
| 13    | LOC13 | Location 13 |
| 14    | LOC14 | Location 14 |
| 15    | LOC15 | Location 15 |
| 16    | LOC16 | Location 16 |
| 17    | LOC17 | Location 17 |
| 18    | LOC18 | Location 18 |
| 19    | LOC19 | Location 19 |
| 20    | LOC20 | Location 20 |
| 21    | LOC21 | Location 21 |
| 22    | LOC22 | Location 22 |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
|       | 23              | LOC23   |        | Location 23   |
|       | 24              | LOC24   |        | Location 24   |
|       | 25              | LOC25   |        | Location 25   |
|       | 26              | LOC26   |        | Location 26   |
|       | 27              | LOC27   |        | Location 27   |
|       | 28              | LOC28   |        | Location 28   |
|       | 29              | LOC29   |        | Location 29   |
|       | 30              | LOC30   |        | Location 30   |
|       | 31              | LOC31   |        | Location 31   |
| 23:22 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 21:16 | CC2LOC          | 0x00  | RW     | <b>I/O Location</b><br>Decides the location of the CC2 pin. |
|       | Value           | Mode  |        | Description   |
|       | 0               | LOC0  |        | Location 0  |
|       | 1               | LOC1  |        | Location 1  |
|       | 2               | LOC2  |        | Location 2  |
|       | 3               | LOC3  |        | Location 3  |
|       | 4               | LOC4  |        | Location 4  |
|       | 5               | LOC5  |        | Location 5  |
|       | 6               | LOC6  |        | Location 6  |
|       | 7               | LOC7  |        | Location 7  |
|       | 8               | LOC8  |        | Location 8  |
|       | 9               | LOC9  |        | Location 9  |
|       | 10              | LOC10   |        | Location 10   |
|       | 11              | LOC11   |        | Location 11   |
|       | 12              | LOC12   |        | Location 12   |
|       | 13              | LOC13   |        | Location 13   |
|       | 14              | LOC14   |        | Location 14   |
|       | 15              | LOC15   |        | Location 15   |
|       | 16              | LOC16   |        | Location 16   |
|       | 17              | LOC17   |        | Location 17   |
|       | 18              | LOC18   |        | Location 18   |
|       | 19              | LOC19   |        | Location 19   |
|       | 20              | LOC20   |        | Location 20   |
|       | 21              | LOC21   |        | Location 21   |
|       | 22              | LOC22   |        | Location 22   |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
|       | 23              | LOC23   |        | Location 23   |
|       | 24              | LOC24   |        | Location 24   |
|       | 25              | LOC25   |        | Location 25   |
|       | 26              | LOC26   |        | Location 26   |
|       | 27              | LOC27   |        | Location 27   |
|       | 28              | LOC28   |        | Location 28   |
|       | 29              | LOC29   |        | Location 29   |
|       | 30              | LOC30   |        | Location 30   |
|       | 31              | LOC31   |        | Location 31   |
| 15:14 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 13:8  | CC1LOC          | 0x00  | RW     | <b>I/O Location</b><br>Decides the location of the CC1 pin. |
|       | Value           | Mode  |        | Description   |
|       | 0               | LOC0  |        | Location 0  |
|       | 1               | LOC1  |        | Location 1  |
|       | 2               | LOC2  |        | Location 2  |
|       | 3               | LOC3  |        | Location 3  |
|       | 4               | LOC4  |        | Location 4  |
|       | 5               | LOC5  |        | Location 5  |
|       | 6               | LOC6  |        | Location 6  |
|       | 7               | LOC7  |        | Location 7  |
|       | 8               | LOC8  |        | Location 8  |
|       | 9               | LOC9  |        | Location 9  |
|       | 10              | LOC10   |        | Location 10   |
|       | 11              | LOC11   |        | Location 11   |
|       | 12              | LOC12   |        | Location 12   |
|       | 13              | LOC13   |        | Location 13   |
|       | 14              | LOC14   |        | Location 14   |
|       | 15              | LOC15   |        | Location 15   |
|       | 16              | LOC16   |        | Location 16   |
|       | 17              | LOC17   |        | Location 17   |
|       | 18              | LOC18   |        | Location 18   |
|       | 19              | LOC19   |        | Location 19   |
|       | 20              | LOC20   |        | Location 20   |
|       | 21              | LOC21   |        | Location 21   |
|       | 22              | LOC22   |        | Location 22   |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
|     | 23   | LOC23 |        | Location 23 |
|     | 24   | LOC24 |        | Location 24 |
|     | 25   | LOC25 |        | Location 25 |
|     | 26   | LOC26 |        | Location 26 |
|     | 27   | LOC27 |        | Location 27 |
|     | 28   | LOC28 |        | Location 28 |
|     | 29   | LOC29 |        | Location 29 |
|     | 30   | LOC30 |        | Location 30 |
|     | 31   | LOC31 |        | Location 31 |

7:6 *Reserved* *To ensure compatibility with future devices, always write bits to 0. More information in [1.2 Conventions](#)*

5:0 CC0LOC 0x00 RW **I/O Location**

Decides the location of the CC0 pin.

| Value | Mode  | Description |
|-------|-------|-------------|
| 0     | LOC0  | Location 0  |
| 1     | LOC1  | Location 1  |
| 2     | LOC2  | Location 2  |
| 3     | LOC3  | Location 3  |
| 4     | LOC4  | Location 4  |
| 5     | LOC5  | Location 5  |
| 6     | LOC6  | Location 6  |
| 7     | LOC7  | Location 7  |
| 8     | LOC8  | Location 8  |
| 9     | LOC9  | Location 9  |
| 10    | LOC10 | Location 10 |
| 11    | LOC11 | Location 11 |
| 12    | LOC12 | Location 12 |
| 13    | LOC13 | Location 13 |
| 14    | LOC14 | Location 14 |
| 15    | LOC15 | Location 15 |
| 16    | LOC16 | Location 16 |
| 17    | LOC17 | Location 17 |
| 18    | LOC18 | Location 18 |
| 19    | LOC19 | Location 19 |
| 20    | LOC20 | Location 20 |
| 21    | LOC21 | Location 21 |
| 22    | LOC22 | Location 22 |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
| 23  |      | LOC23 |        | Location 23 |
| 24  |      | LOC24 |        | Location 24 |
| 25  |      | LOC25 |        | Location 25 |
| 26  |      | LOC26 |        | Location 26 |
| 27  |      | LOC27 |        | Location 27 |
| 28  |      | LOC28 |        | Location 28 |
| 29  |      | LOC29 |        | Location 29 |
| 30  |      | LOC30 |        | Location 30 |
| 31  |      | LOC31 |        | Location 31 |

## 21.5.14 TIMERN\_ROUTELOC2 - I/O Routing Location Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |          |    |    |    |    |    |    |    |          |    |    |   |          |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|----|----|----|----|----------|----|----|---|----------|---|---|---|---|---|---|---|---|
| 0x03C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20       | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12       | 11 | 10 | 9 | 8        | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    | 0x00     |    |    |    |    |    |    |    | 0x00     |    |    |   | 0x00     |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    | RW       |    |    |    |    |    |    |    | RW       |    |    |   | RW       |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    | CDT12LOC |    |    |    |    |    |    |    | CDT11LOC |    |    |   | CDT10LOC |   |   |   |   |   |   |   |   |

| Bit   | Name            | Reset   | Access | Description |
|-------|-----------------|---|--------|-------------|
| 31:22 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |             |

21:16 CDT12LOC 0x00 RW **I/O Location**

Decides the location of the CDT12 pin.

| Value | Mode  | Description |
|-------|-------|-------------|
| 0     | LOC0  | Location 0  |
| 1     | LOC1  | Location 1  |
| 2     | LOC2  | Location 2  |
| 3     | LOC3  | Location 3  |
| 4     | LOC4  | Location 4  |
| 5     | LOC5  | Location 5  |
| 6     | LOC6  | Location 6  |
| 7     | LOC7  | Location 7  |
| 8     | LOC8  | Location 8  |
| 9     | LOC9  | Location 9  |
| 10    | LOC10 | Location 10 |
| 11    | LOC11 | Location 11 |
| 12    | LOC12 | Location 12 |
| 13    | LOC13 | Location 13 |
| 14    | LOC14 | Location 14 |
| 15    | LOC15 | Location 15 |
| 16    | LOC16 | Location 16 |
| 17    | LOC17 | Location 17 |
| 18    | LOC18 | Location 18 |
| 19    | LOC19 | Location 19 |
| 20    | LOC20 | Location 20 |
| 21    | LOC21 | Location 21 |
| 22    | LOC22 | Location 22 |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
|       | 23              | LOC23   |        | Location 23   |
|       | 24              | LOC24   |        | Location 24   |
|       | 25              | LOC25   |        | Location 25   |
|       | 26              | LOC26   |        | Location 26   |
|       | 27              | LOC27   |        | Location 27   |
|       | 28              | LOC28   |        | Location 28   |
|       | 29              | LOC29   |        | Location 29   |
|       | 30              | LOC30   |        | Location 30   |
|       | 31              | LOC31   |        | Location 31   |
| 15:14 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 13:8  | CDTI1LOC        | 0x00  | RW     | <b>I/O Location</b><br>Decides the location of the CDTI1 pin. |
|       | Value           | Mode  |        | Description   |
|       | 0               | LOC0  |        | Location 0  |
|       | 1               | LOC1  |        | Location 1  |
|       | 2               | LOC2  |        | Location 2  |
|       | 3               | LOC3  |        | Location 3  |
|       | 4               | LOC4  |        | Location 4  |
|       | 5               | LOC5  |        | Location 5  |
|       | 6               | LOC6  |        | Location 6  |
|       | 7               | LOC7  |        | Location 7  |
|       | 8               | LOC8  |        | Location 8  |
|       | 9               | LOC9  |        | Location 9  |
|       | 10              | LOC10   |        | Location 10   |
|       | 11              | LOC11   |        | Location 11   |
|       | 12              | LOC12   |        | Location 12   |
|       | 13              | LOC13   |        | Location 13   |
|       | 14              | LOC14   |        | Location 14   |
|       | 15              | LOC15   |        | Location 15   |
|       | 16              | LOC16   |        | Location 16   |
|       | 17              | LOC17   |        | Location 17   |
|       | 18              | LOC18   |        | Location 18   |
|       | 19              | LOC19   |        | Location 19   |
|       | 20              | LOC20   |        | Location 20   |
|       | 21              | LOC21   |        | Location 21   |
|       | 22              | LOC22   |        | Location 22   |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
|     | 23   | LOC23 |        | Location 23 |
|     | 24   | LOC24 |        | Location 24 |
|     | 25   | LOC25 |        | Location 25 |
|     | 26   | LOC26 |        | Location 26 |
|     | 27   | LOC27 |        | Location 27 |
|     | 28   | LOC28 |        | Location 28 |
|     | 29   | LOC29 |        | Location 29 |
|     | 30   | LOC30 |        | Location 30 |
|     | 31   | LOC31 |        | Location 31 |

7:6 *Reserved* *To ensure compatibility with future devices, always write bits to 0. More information in [1.2 Conventions](#)*

5:0 CDTI0LOC 0x00 RW **I/O Location**

Decides the location of the CDTI0 pin.

| Value | Mode  | Description |
|-------|-------|-------------|
| 0     | LOC0  | Location 0  |
| 1     | LOC1  | Location 1  |
| 2     | LOC2  | Location 2  |
| 3     | LOC3  | Location 3  |
| 4     | LOC4  | Location 4  |
| 5     | LOC5  | Location 5  |
| 6     | LOC6  | Location 6  |
| 7     | LOC7  | Location 7  |
| 8     | LOC8  | Location 8  |
| 9     | LOC9  | Location 9  |
| 10    | LOC10 | Location 10 |
| 11    | LOC11 | Location 11 |
| 12    | LOC12 | Location 12 |
| 13    | LOC13 | Location 13 |
| 14    | LOC14 | Location 14 |
| 15    | LOC15 | Location 15 |
| 16    | LOC16 | Location 16 |
| 17    | LOC17 | Location 17 |
| 18    | LOC18 | Location 18 |
| 19    | LOC19 | Location 19 |
| 20    | LOC20 | Location 20 |
| 21    | LOC21 | Location 21 |
| 22    | LOC22 | Location 22 |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
| 23  |      | LOC23 |        | Location 23 |
| 24  |      | LOC24 |        | Location 24 |
| 25  |      | LOC25 |        | Location 25 |
| 26  |      | LOC26 |        | Location 26 |
| 27  |      | LOC27 |        | Location 27 |
| 28  |      | LOC28 |        | Location 28 |
| 29  |      | LOC29 |        | Location 29 |
| 30  |      | LOC30 |        | Location 30 |
| 31  |      | LOC31 |        | Location 31 |

## 21.5.15 TIMERN\_CCx\_CTRL - CC Channel Control Register

| Offset        | Bit Position |      |       |         |          |    |        |    |    |    |    |    |    |        |    |    |    |    |       |    |       |    |      |   |   |   |   |       |   |        |      |   |
|---------------|--------------|------|-------|---------|----------|----|--------|----|----|----|----|----|----|--------|----|----|----|----|-------|----|-------|----|------|---|---|---|---|-------|---|--------|------|---|
| 0x060         | 31           | 30   | 29    | 28      | 27       | 26 | 25     | 24 | 23 | 22 | 21 | 20 | 19 | 18     | 17 | 16 | 15 | 14 | 13    | 12 | 11    | 10 | 9    | 8 | 7 | 6 | 5 | 4     | 3 | 2      | 1    | 0 |
| <b>Reset</b>  |              | 0    | 0     | 0       | 0x0      |    | 0x0    |    |    |    |    |    |    | 0x0    |    |    |    |    | 0x0   |    | 0x0   |    | 0x0  |   |   |   |   | 0     |   | 0      | 0x0  |   |
| <b>Access</b> |              | RW   | RW    | RW      | RW       |    | RW     |    |    |    |    |    |    | RW     |    |    |    |    | RW    |    | RW    |    | RW   |   |   |   |   | RW    |   | RW     | RW   |   |
| <b>Name</b>   |              | FILT | INSEL | PRSCONF | ICEVCTRL |    | ICEDGE |    |    |    |    |    |    | PRSSEL |    |    |    |    | CUFOA |    | COFOA |    | CMOA |   |   |   |   | COIST |   | OUTINV | MODE |   |

| Bit   | Name            | Reset   | Access  | Description  |
|-------|-----------------|---|---|--|
| 31    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 30    | FILT            | 0   | RW  | <b>Digital Filter</b><br>Enable digital filter.  |
|       | Value           | Mode  | Description   |  |
|       | 0               | DISABLE   | Digital filter disabled   |  |
|       | 1               | ENABLE  | Digital filter enabled  |  |
| 29    | INSEL           | 0   | RW  | <b>Input Selection</b><br>Select Compare/Capture channel input.  |
|       | Value           | Mode  | Description   |  |
|       | 0               | PIN   | TIMERNCCx pin is selected   |  |
|       | 1               | PRS   | PRS input (selected by PRSSEL) is selected                                      |  |
| 28    | PRSCONF         | 0   | RW  | <b>PRS Configuration</b><br>Select PRS pulse or level.   |
|       | Value           | Mode  | Description   |  |
|       | 0               | PULSE   | Each CC event will generate a one HFPERCLK cycle high pulse                     |  |
|       | 1               | LEVEL   | The PRS channel will follow CC out  |  |
| 27:26 | ICEVCTRL        | 0x0   | RW  | <b>Input Capture Event Control</b><br>These bits control when a Compare/Capture PRS output pulse and interrupt flag is set. DMA request however is set on every capture. |
|       | Value           | Mode  | Description   |  |
|       | 0               | EVERYEDGE   | PRS output pulse and interrupt flag set on every capture                        |  |
|       | 1               | EVERYSECONDEDGE   | PRS output pulse and interrupt flag set on every second capture                 |  |
|       | 2               | RISING  | PRS output pulse and interrupt flag set on rising edge only (if ICEDGE = BOTH)  |  |
|       | 3               | FALLING   | PRS output pulse and interrupt flag set on falling edge only (if ICEDGE = BOTH) |  |

| Bit  | Name            | Reset   | Access | Description  |
|--|-----------------|---|--------|--|
| 25:24  | ICEDGE          | 0x0   | RW     | <b>Input Capture Edge Select</b>                           |
| These bits control which edges the edge detector triggers on. The output is used for input capture and external clock input. |                 |   |        |  |
|  | Value           | Mode  |        | Description  |
|  | 0               | RISING  |        | Rising edges detected                                      |
|  | 1               | FALLING   |        | Falling edges detected                                     |
|  | 2               | BOTH  |        | Both edges detected  |
|  | 3               | NONE  |        | No edge detection, signal is left as it is                 |
| 23:20  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 19:16  | PRSEL           | 0x0   | RW     | <b>Compare/Capture Channel PRS Input Channel Selection</b> |
| Select PRS input channel for Compare/Capture channel.  |                 |   |        |  |
|  | Value           | Mode  |        | Description  |
|  | 0               | PRSCH0  |        | PRS Channel 0 selected as input                            |
|  | 1               | PRSCH1  |        | PRS Channel 1 selected as input                            |
|  | 2               | PRSCH2  |        | PRS Channel 2 selected as input                            |
|  | 3               | PRSCH3  |        | PRS Channel 3 selected as input                            |
|  | 4               | PRSCH4  |        | PRS Channel 4 selected as input                            |
|  | 5               | PRSCH5  |        | PRS Channel 5 selected as input                            |
|  | 6               | PRSCH6  |        | PRS Channel 6 selected as input                            |
|  | 7               | PRSCH7  |        | PRS Channel 7 selected as input                            |
|  | 8               | PRSCH8  |        | PRS Channel 8 selected as input                            |
|  | 9               | PRSCH9  |        | PRS Channel 9 selected as input                            |
|  | 10              | PRSCH10   |        | PRS Channel 10 selected as input                           |
|  | 11              | PRSCH11   |        | PRS Channel 11 selected as input                           |
| 15:14  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 13:12  | CUFOA           | 0x0   | RW     | <b>Counter Underflow Output Action</b>                     |
| Select output action on counter underflow.   |                 |   |        |  |
|  | Value           | Mode  |        | Description  |
|  | 0               | NONE  |        | No action on counter underflow                             |
|  | 1               | TOGGLE  |        | Toggle output on counter underflow                         |
|  | 2               | CLEAR   |        | Clear output on counter underflow                          |
|  | 3               | SET   |        | Set output on counter underflow                            |
| 11:10  | COFOA           | 0x0   | RW     | <b>Counter Overflow Output Action</b>                      |
| Select output action on counter overflow.  |                 |   |        |  |
|  | Value           | Mode  |        | Description  |

| Bit | Name            | Reset   | Access | Description   |
|-----|-----------------|---|--------|---|
|     | 0               | NONE  |        | No action on counter overflow   |
|     | 1               | TOGGLE  |        | Toggle output on counter overflow   |
|     | 2               | CLEAR   |        | Clear output on counter overflow  |
|     | 3               | SET   |        | Set output on counter overflow  |
| 9:8 | CMOA            | 0x0   | RW     | <b>Compare Match Output Action</b><br>Select output action on compare match.  |
|     | Value           | Mode  |        | Description   |
|     | 0               | NONE  |        | No action on compare match  |
|     | 1               | TOGGLE  |        | Toggle output on compare match  |
|     | 2               | CLEAR   |        | Clear output on compare match   |
|     | 3               | SET   |        | Set output on compare match   |
| 7:5 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 4   | COIST           | 0   | RW     | <b>Compare Output Initial State</b><br>This bit is only used in Output Compare and PWM mode. When this bit is set in Compare or PWM mode, the output is set high when the counter is disabled. When counting resumes, this value will represent the initial value for the output. If the bit is cleared, the output will be cleared when the counter is disabled. |
| 3   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 2   | OUTINV          | 0   | RW     | <b>Output Invert</b><br>Setting this bit inverts the output from the CC channel (Output compare,PWM).   |
| 1:0 | MODE            | 0x0   | RW     | <b>CC Channel Mode</b><br>These bits select the mode for Compare/Capture channel.   |
|     | Value           | Mode  |        | Description   |
|     | 0               | OFF   |        | Compare/Capture channel turned off  |
|     | 1               | INPUTCAPTURE  |        | Input capture   |
|     | 2               | OUTPUTCOMPARE   |        | Output compare  |
|     | 3               | PWM   |        | Pulse-Width Modulation  |

**21.5.16 TIMERN\_CCx\_CCV - CC Channel Value Register (Actionable Reads)**

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x064         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CCV        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name | Reset      | Access | Description             |
|--|------|------------|--------|-------------------------|
| 31:0   | CCV  | 0x00000000 | RWH    | <b>CC Channel Value</b> |
| <p>In input capture mode, this field holds the first unread capture value. When reading this register in input capture mode, the contents of the TIMERN_CCx_CCVB register will be written to TIMERN_CCx_CCV in the next cycle. In compare mode, this fields holds the compare value.</p> |      |            |        |                         |

**21.5.17 TIMERN\_CCx\_CCVP - CC Channel Value Peek Register**

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x068         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CCVP       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name | Reset      | Access | Description                  |
|---|------|------------|--------|------------------------------|
| 31:0  | CCVP | 0x00000000 | R      | <b>CC Channel Value Peek</b> |
| <p>This field is used to read the CC value without pulling data through the FIFO in capture mode.</p> |      |            |        |                              |

21.5.18 TIMERN\_CCx\_CCVB - CC Channel Buffer Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x06C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CCVB       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit   | Name | Reset      | Access | Description                    |
|---|------|------------|--------|--------------------------------|
| 31:0  | CCVB | 0x00000000 | RWH    | <b>CC Channel Value Buffer</b> |
| <p>In Input Capture mode, this field holds the last capture value if the TIMERN_CCx_CCV register already contains an earlier unread capture value. In Output Compare or PWM mode, this field holds the CC buffer value which will be written to TIMERN_CCx_CCV on an update event if TIMERN_CCx_CCVB contains valid data.</p> |      |            |        |                                |

## 21.5.19 TIMERN\_DTCTRL - DTI Control Register

| Offset        | Bit Position |    |    |    |    |    |    |         |    |    |    |    |    |    |    |    |    |    |    |    |    |        |      |   |          |   |   |        |        |       |      |   |
|---------------|--------------|----|----|----|----|----|----|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|------|---|----------|---|---|--------|--------|-------|------|---|
| 0x0A0         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24      | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10     | 9    | 8 | 7        | 6 | 5 | 4      | 3      | 2     | 1    | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    | 0       |    |    |    |    |    |    |    |    |    |    |    |    |    | 0      | 0    |   | 0x0      |   |   | 0      | 0      | 0     | 0    |   |
| <b>Access</b> |              |    |    |    |    |    |    | RW      |    |    |    |    |    |    |    |    |    |    |    |    |    | RW     | RW   |   | RW       |   |   | RW     | RW     | RW    | RW   |   |
| <b>Name</b>   |              |    |    |    |    |    |    | DTPRSEN |    |    |    |    |    |    |    |    |    |    |    |    |    | DTFATS | DTAR |   | DTPRSSEL |   |   | DTCINV | DTIPOL | DTDAS | DTEN |   |

| Bit   | Name     | Reset   | Access                           | Description   |
|-------|----------|---|----------------------------------|---|
| 31:25 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                  |   |
| 24    | DTPRSEN  | 0   | RW                               | <b>DTI PRS Source Enable</b><br>Enable/disable PRS as DTI input.  |
| 23:11 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                  |   |
| 10    | DTFATS   | 0   | RW                               | <b>DTI Fault Action on Timer Stop</b><br>When Timer stops, DTI block outputs go to safe state as programmed in DTFA field of TIMERN_DTFC register. However, when DTAR is also set, DTAR having higher priority allows channel 0 to output the incoming PRS input while the other channels go to safe state. |
| 9     | DTAR     | 0   | RW                               | <b>DTI Always Run</b><br>This is used only for DTI channel 0. It Allows DTI channel 0 to keep running even when timer is stopped. This is useful when its input source is PRS. However, here the undivided HFPERCLK is always used regardless of the programmed value in DTPRESC.                           |
| 8     | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                  |   |
| 7:4   | DTPRSSEL | 0x0   | RW                               | <b>DTI PRS Source Channel Select</b><br>Selects which PRS channel compare channel 0 will listen to.   |
|       | Value    | Mode  | Description                      |   |
|       | 0        | PRSCH0  | PRS Channel 0 selected as input  |   |
|       | 1        | PRSCH1  | PRS Channel 1 selected as input  |   |
|       | 2        | PRSCH2  | PRS Channel 2 selected as input  |   |
|       | 3        | PRSCH3  | PRS Channel 3 selected as input  |   |
|       | 4        | PRSCH4  | PRS Channel 4 selected as input  |   |
|       | 5        | PRSCH5  | PRS Channel 5 selected as input  |   |
|       | 6        | PRSCH6  | PRS Channel 6 selected as input  |   |
|       | 7        | PRSCH7  | PRS Channel 7 selected as input  |   |
|       | 8        | PRSCH8  | PRS Channel 8 selected as input  |   |
|       | 9        | PRSCH9  | PRS Channel 9 selected as input  |   |
|       | 10       | PRSCH10   | PRS Channel 10 selected as input |   |
|       | 11       | PRSCH11   | PRS Channel 11 selected as input |   |

| Bit | Name   | Reset     | Access | Description  |
|-----|--------|-----------|--------|--|
| 3   | DTCINV | 0         | RW     | <b>DTI Complementary Output Invert</b><br>Set to invert complementary outputs.         |
| 2   | DTIPOL | 0         | RW     | <b>DTI Inactive Polarity</b><br>Set inactive polarity for outputs.                     |
| 1   | DTDAS  | 0         | RW     | <b>DTI Automatic Start-up Functionality</b><br>Configure DTI restart on debugger exit. |
|     | Value  | Mode      |        | Description  |
|     | 0      | NORESTART |        | No DTI restart on debugger exit  |
|     | 1      | RESTART   |        | DTI restart on debugger exit   |
| 0   | DTEN   | 0         | RW     | <b>DTI Enable</b><br>Enable/disable DTI.   |

## 21.5.20 TIMERN\_DTIME - DTI Time Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |    |    |          |    |    |   |         |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|----|----|----------|----|----|---|---------|---|---|---|---|---|---|---|---|
| 0x0A4         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20      | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12       | 11 | 10 | 9 | 8       | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    | 0x00    |    |    |    |    |    |    |    | 0x00     |    |    |   | 0x0     |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    | RW      |    |    |    |    |    |    |    | RW       |    |    |   | RW      |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    | DTFALLT |    |    |    |    |    |    |    | DTRISSET |    |    |   | DTPRESC |   |   |   |   |   |   |   |   |

| Bit   | Name            | Reset   | Access                          | Description   |
|-------|-----------------|---|---------------------------------|---|
| 31:22 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                 |   |
| 21:16 | DTFALLT         | 0x00  | RW                              | <b>DTI Fall-time</b><br>Set time span for the falling edge. |
|       | Value           | Description   |                                 |   |
|       | DTFALLT         | Fall time of DTFALLT+1 prescaled HFPERCLK cycles  |                                 |   |
| 15:14 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                 |   |
| 13:8  | DTRISSET        | 0x00  | RW                              | <b>DTI Rise-time</b><br>Set time span for the rising edge.  |
|       | Value           | Description   |                                 |   |
|       | DTRISSET        | Rise time of DTRISSET+1 prescaled HFPERCLK cycles   |                                 |   |
| 7:4   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                 |   |
| 3:0   | DTPRESC         | 0x0   | RW                              | <b>DTI Prescaler Setting</b><br>Select prescaler for DTI.   |
|       | Value           | Mode  | Description                     |   |
|       | 0               | DIV1  | The HFPERCLK is undivided       |   |
|       | 1               | DIV2  | The HFPERCLK is divided by 2    |   |
|       | 2               | DIV4  | The HFPERCLK is divided by 4    |   |
|       | 3               | DIV8  | The HFPERCLK is divided by 8    |   |
|       | 4               | DIV16   | The HFPERCLK is divided by 16   |   |
|       | 5               | DIV32   | The HFPERCLK is divided by 32   |   |
|       | 6               | DIV64   | The HFPERCLK is divided by 64   |   |
|       | 7               | DIV128  | The HFPERCLK is divided by 128  |   |
|       | 8               | DIV256  | The HFPERCLK is divided by 256  |   |
|       | 9               | DIV512  | The HFPERCLK is divided by 512  |   |
|       | 10              | DIV1024   | The HFPERCLK is divided by 1024 |   |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
|-----|------|-------|--------|-------------|

## 21.5.21 TIMERN\_DTFC - DTI Fault Configuration Register

| Offset        | Bit Position |    |    |    |             |          |           |           |    |    |    |    |    |    |    |    |      |    |    |    |    |    |   |   |   |            |   |   |   |   |            |   |
|---------------|--------------|----|----|----|-------------|----------|-----------|-----------|----|----|----|----|----|----|----|----|------|----|----|----|----|----|---|---|---|------------|---|---|---|---|------------|---|
| 0x0A8         | 31           | 30 | 29 | 28 | 27          | 26       | 25        | 24        | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15   | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6          | 5 | 4 | 3 | 2 | 1          | 0 |
| <b>Reset</b>  |              |    |    |    | 0           | 0        | 0         | 0         |    |    |    |    |    |    |    |    | 0x0  |    |    |    |    |    |   |   |   | 0x0        |   |   |   |   | 0x0        |   |
| <b>Access</b> |              |    |    |    | RW          | RW       | RW        | RW        |    |    |    |    |    |    |    |    | RW   |    |    |    |    |    |   |   |   | RW         |   |   |   |   | RW         |   |
| <b>Name</b>   |              |    |    |    | DTLOCKUPFEN | DTDBGFEN | DTPRS1FEN | DTPRS0FEN |    |    |    |    |    |    |    |    | DTFA |    |    |    |    |    |   |   |   | DTPRS1FSEL |   |   |   |   | DTPRS0FSEL |   |

| Bit   | Name        | Reset   | Access | Description  |       |      |             |   |        |  |   |          |  |   |        |  |   |          |                  |
|-------|-------------|---|--------|--|-------|------|-------------|---|--------|--|---|----------|--|---|--------|--|---|----------|------------------|
| 31:28 | Reserved    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |        |  |   |          |  |   |        |  |   |          |                  |
| 27    | DTLOCKUPFEN | 0   | RW     | <b>DTI Lockup Fault Enable</b><br>Set this bit to 1 to enable core lockup as a fault source  |       |      |             |   |        |  |   |          |  |   |        |  |   |          |                  |
| 26    | DTDBGFEN    | 0   | RW     | <b>DTI Debugger Fault Enable</b><br>Set this bit to 1 to enable debugger as a fault source   |       |      |             |   |        |  |   |          |  |   |        |  |   |          |                  |
| 25    | DTPRS1FEN   | 0   | RW     | <b>DTI PRS 1 Fault Enable</b><br>Set this bit to 1 to enable PRS source 1(PRS channel determined by DTPRS1FSEL) as a fault source  |       |      |             |   |        |  |   |          |  |   |        |  |   |          |                  |
| 24    | DTPRS0FEN   | 0   | RW     | <b>DTI PRS 0 Fault Enable</b><br>Set this bit to 1 to enable PRS source 0(PRS channel determined by DTPRS0FSEL) as a fault source  |       |      |             |   |        |  |   |          |  |   |        |  |   |          |                  |
| 23:18 | Reserved    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |        |  |   |          |  |   |        |  |   |          |                  |
| 17:16 | DTFA        | 0x0   | RW     | <b>DTI Fault Action</b><br>Select fault action.<br><table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>NONE</td> <td>No action on fault</td> </tr> <tr> <td>1</td> <td>INACTIVE</td> <td>Set outputs inactive</td> </tr> <tr> <td>2</td> <td>CLEAR</td> <td>Clear outputs</td> </tr> <tr> <td>3</td> <td>TRISTATE</td> <td>Tristate outputs</td> </tr> </tbody> </table>                                    | Value | Mode | Description | 0 | NONE   | No action on fault                       | 1 | INACTIVE | Set outputs inactive                     | 2 | CLEAR  | Clear outputs                            | 3 | TRISTATE | Tristate outputs |
| Value | Mode        | Description   |        |  |       |      |             |   |        |  |   |          |  |   |        |  |   |          |                  |
| 0     | NONE        | No action on fault  |        |  |       |      |             |   |        |  |   |          |  |   |        |  |   |          |                  |
| 1     | INACTIVE    | Set outputs inactive  |        |  |       |      |             |   |        |  |   |          |  |   |        |  |   |          |                  |
| 2     | CLEAR       | Clear outputs   |        |  |       |      |             |   |        |  |   |          |  |   |        |  |   |          |                  |
| 3     | TRISTATE    | Tristate outputs  |        |  |       |      |             |   |        |  |   |          |  |   |        |  |   |          |                  |
| 15:12 | Reserved    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |        |  |   |          |  |   |        |  |   |          |                  |
| 11:8  | DTPRS1FSEL  | 0x0   | RW     | <b>DTI PRS Fault Source 1 Select</b><br>Select PRS channel for fault source 1.<br><table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>PRSCH0</td> <td>PRS Channel 0 selected as fault source 1</td> </tr> <tr> <td>1</td> <td>PRSCH1</td> <td>PRS Channel 1 selected as fault source 1</td> </tr> <tr> <td>2</td> <td>PRSCH2</td> <td>PRS Channel 2 selected as fault source 1</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | PRSCH0 | PRS Channel 0 selected as fault source 1 | 1 | PRSCH1   | PRS Channel 1 selected as fault source 1 | 2 | PRSCH2 | PRS Channel 2 selected as fault source 1 |   |          |                  |
| Value | Mode        | Description   |        |  |       |      |             |   |        |  |   |          |  |   |        |  |   |          |                  |
| 0     | PRSCH0      | PRS Channel 0 selected as fault source 1  |        |  |       |      |             |   |        |  |   |          |  |   |        |  |   |          |                  |
| 1     | PRSCH1      | PRS Channel 1 selected as fault source 1  |        |  |       |      |             |   |        |  |   |          |  |   |        |  |   |          |                  |
| 2     | PRSCH2      | PRS Channel 2 selected as fault source 1  |        |  |       |      |             |   |        |  |   |          |  |   |        |  |   |          |                  |

| Bit | Name            | Reset   | Access | Description  |
|-----|-----------------|---|--------|--|
| 3   |                 | PRSCH3  |        | PRS Channel 3 selected as fault source 1                                       |
| 4   |                 | PRSCH4  |        | PRS Channel 4 selected as fault source 1                                       |
| 5   |                 | PRSCH5  |        | PRS Channel 5 selected as fault source 1                                       |
| 6   |                 | PRSCH6  |        | PRS Channel 6 selected as fault source 1                                       |
| 7   |                 | PRSCH7  |        | PRS Channel 7 selected as fault source 1                                       |
| 8   |                 | PRSCH8  |        | PRS Channel 8 selected as fault source 1                                       |
| 9   |                 | PRSCH9  |        | PRS Channel 9 selected as fault source 1                                       |
| 10  |                 | PRSCH10   |        | PRS Channel 10 selected as fault source 1                                      |
| 11  |                 | PRSCH11   |        | PRS Channel 11 selected as fault source 1                                      |
| 7:4 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 3:0 | DTPRS0FSEL      | 0x0   | RW     | <b>DTI PRS Fault Source 0 Select</b><br>Select PRS channel for fault source 0. |
|     | Value           | Mode  |        | Description  |
|     | 0               | PRSCH0  |        | PRS Channel 0 selected as fault source 0                                       |
|     | 1               | PRSCH1  |        | PRS Channel 1 selected as fault source 1                                       |
|     | 2               | PRSCH2  |        | PRS Channel 2 selected as fault source 2                                       |
|     | 3               | PRSCH3  |        | PRS Channel 3 selected as fault source 3                                       |
|     | 4               | PRSCH4  |        | PRS Channel 4 selected as fault source 4                                       |
|     | 5               | PRSCH5  |        | PRS Channel 5 selected as fault source 5                                       |
|     | 6               | PRSCH6  |        | PRS Channel 6 selected as fault source 6                                       |
|     | 7               | PRSCH7  |        | PRS Channel 7 selected as fault source 7                                       |
|     | 8               | PRSCH8  |        | PRS Channel 8 selected as fault source 8                                       |
|     | 9               | PRSCH9  |        | PRS Channel 9 selected as fault source 9                                       |
|     | 10              | PRSCH10   |        | PRS Channel 10 selected as fault source 10                                     |
|     | 11              | PRSCH11   |        | PRS Channel 11 selected as fault source 11                                     |







21.5.25 TIMERN\_DTLOCK - DTI Configuration Lock Register

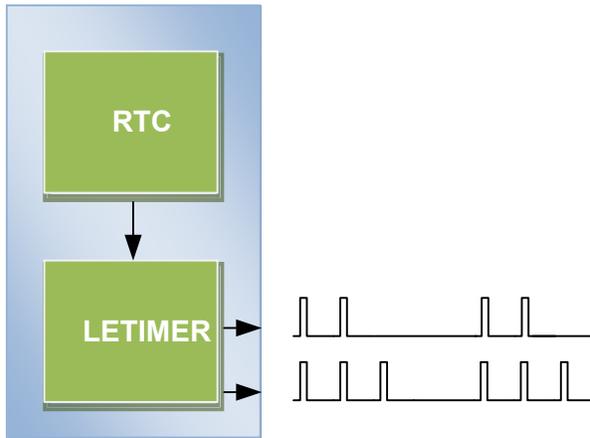
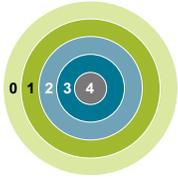
| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x0B8         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LOCKKEY |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description |
|-------|----------|--|--------|-------------|
| 31:16 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |             |

|      |         |        |     |   |
|------|---------|--------|-----|---|
| 15:0 | LOCKKEY | 0x0000 | RWH | <b>DTI Lock Key</b><br><br>Write any other value than the unlock code to lock TIMERN_ROUTE, TIMERN_DTCTRL, TIMERN_DTTIME and TIMERN_DTFC from editing. Write the unlock code to unlock. When reading the register, bit 0 is set when the lock is enabled. |
|------|---------|--------|-----|---|

| Mode            | Value  | Description                      |
|-----------------|--------|----------------------------------|
| Read Operation  |        |                                  |
| UNLOCKED        | 0      | TIMER DTI registers are unlocked |
| LOCKED          | 1      | TIMER DTI registers are locked   |
| Write Operation |        |                                  |
| LOCK            | 0      | Lock TIMER DTI registers         |
| UNLOCK          | 0xCE80 | Unlock TIMER DTI registers       |

## 22. LETIMER - Low Energy Timer



### Quick Facts

#### What?

The LETIMER is a down-counter that can keep track of time and output configurable waveforms. Running on a 32768 Hz clock, the LETIMER is available in EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

#### Why?

The LETIMER can be used to provide repeatable waveforms to external components while remaining in EM2 Deep Sleep. It is well suited for applications such as metering systems or to provide more compare values than available in the RTC.

#### How?

With buffered repeat and top value registers, the LETIMER can provide glitch-free waveforms at frequencies up to 16 kHz. It can be coupled with RTC using PRS, allowing advanced time-keeping and wake-up functions in EM2 Deep Sleep and EM3 Stop.

### 22.1 Introduction

The unique LETIMER™, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum.

The LETIMER can be used to output a variety of waveforms with minimal software intervention. It can also be connected to the Real Time Counter (RTC) using PRS, and can be configured to start counting on compare matches from the RTC.

### 22.2 Features

- 16-bit down count timer
- 2 Compare match registers
- Compare register 0 can be top timer top value
- Compare registers can be double buffered
- Double buffered 8-bit Repeat Register
- Same clock source as the Real Time Counter
- LETIMER can be triggered (started) by an RTC event via PRS or by software
- LETIMER can be started, stopped, and/or cleared by PRS
- 2 output pins can optionally be configured to provide different waveforms on timer underflow:
  - Toggle output pin
  - Apply a positive pulse (pulse width of one  $LFACLK_{LETIMER}$  period)
  - PWM
- Interrupt on:
  - Compare matches
  - Timer underflow
  - Repeat done
- Optionally runs during debug
- PRS Output

### 22.3 Functional Description

An overview of the LETIMER module is shown in [Figure 22.1 LETIMER Overview on page 755](#). The LETIMER is a 16-bit down-counter with two compare registers, LETIMERn\_COMP0 and LETIMERn\_COMP1. The LETIMERn\_COMP0 register can optionally act as a top value for the counter. The repeat counter LETIMERn\_REP0 allows the timer to count a specified number of times before it stops. Both the LETIMERn\_COMP0 and LETIMERn\_REP0 registers can be double buffered by the LETIMERn\_COMP1 and LETIMERn\_REP1 registers to allow continuous operation. The timer can generate a single pin output, or two linked outputs.

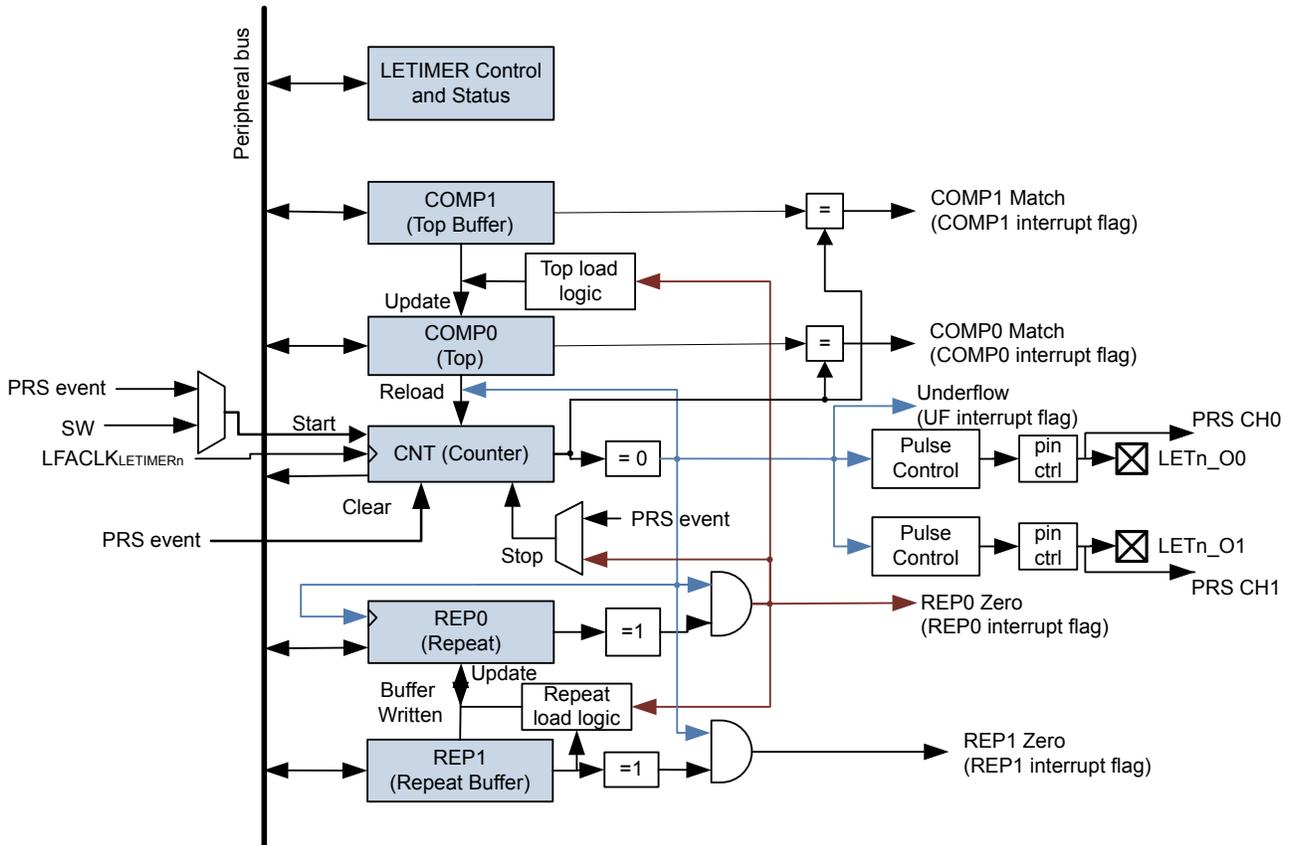


Figure 22.1. LETIMER Overview

#### 22.3.1 Timer

The timer is started by setting command bit START in LETIMERn\_CMD, and stopped by setting the STOP command bit in the same register. RUNNING in LETIMERn\_STATUS is set as long as the timer is running. The timer can also be started on external signals, such as a compare match from the Real Time Counter. If START and STOP are set at the same time, STOP has priority, and the timer will be stopped.

The timer value can be read using the LETIMERn\_CNT register. The value can be written, and it can also be cleared by setting the CLEAR command bit in LETIMERn\_CMD. If the CLEAR and START commands are issued at the same time, the timer will be cleared, then start counting at the top value.

#### 22.3.2 Compare Registers

The LETIMER has two compare match registers, LETIMERn\_COMP0 and LETIMERn\_COMP1. Each of these compare registers are capable of generating an interrupt when the counter value LETIMERn\_CNT becomes equal to their value. When LETIMERn\_CNT becomes equal to the value of LETIMERn\_COMP0, the interrupt flag COMP0 in LETIMERn\_IF is set, and when LETIMERn\_CNT becomes equal to the value of LETIMERn\_COMP1, the interrupt flag COMP1 in LETIMERn\_IF is set.

### 22.3.3 Top Value

If COMP0TOP in LETIMERn\_CTRL is set, the value of LETIMERn\_COMP0 acts as the top value of the timer, and LETIMERn\_COMP0 is loaded into LETIMERn\_CNT on timer underflow. If COMP0TOP is cleared to 0, the timer wraps around to 0xFFFF. The underflow interrupt flag UF in LETIMERn\_IF is set when the timer reaches zero.

#### 22.3.3.1 Buffered Top Value

If BUFTOP in LETIMERn\_CTRL is set, the value of LETIMERn\_COMP0 is buffered by LETIMERn\_COMP1. In this mode, the value of LETIMERn\_COMP1 is loaded into LETIMERn\_COMP0 every time LETIMERn\_REP0 is about to decrement to 0. This can for instance be used in conjunction with the buffered repeat mode to generate continually changing output waveforms.

Write operations to LETIMERn\_COMP0 have priority over buffer loads.

#### 22.3.3.2 Repeat Modes

By default, the timer wraps around to the top value or 0xFFFF on each underflow, and continues counting. The repeat counters can be used to get more control of the operation of the timer, including defining the number of times the counter should wrap around. Four different repeat modes are available, see [Table 22.1 LETIMER Repeat Modes on page 756](#).

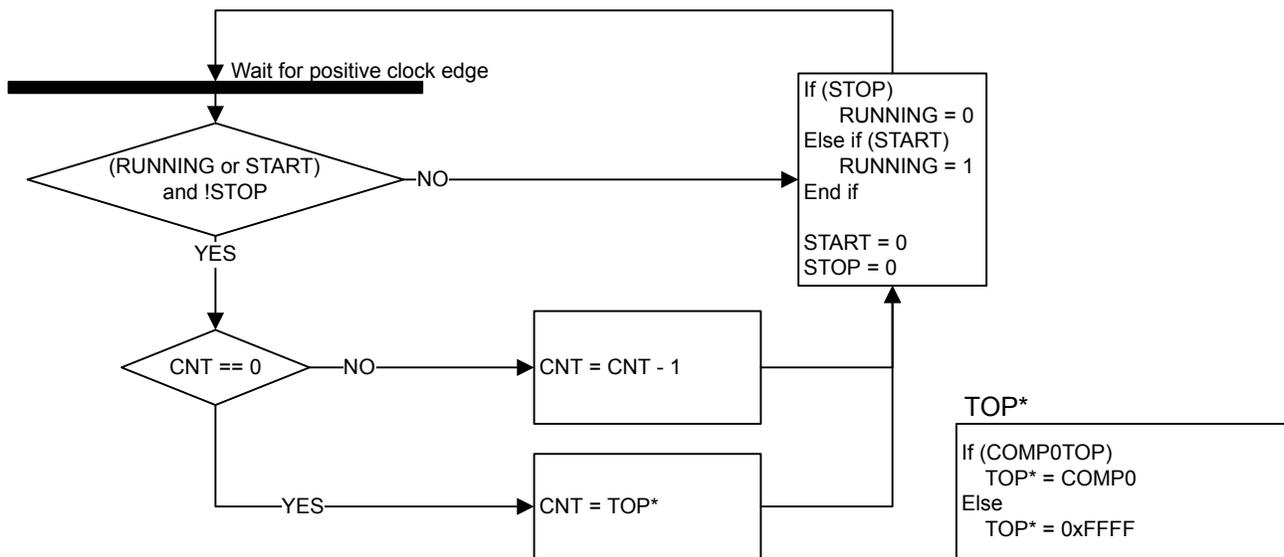
**Table 22.1. LETIMER Repeat Modes**

| REPMODE | Mode         | Description  |
|---------|--------------|--|
| 0b00    | Free-running | The timer runs until it is stopped.  |
| 0b01    | One-shot     | The timer runs as long as LETIMERn_REP0 != 0. LETIMERn_REP0 is decremented at each timer underflow.  |
| 0b10    | Buffered     | The timer runs as long as LETIMERn_REP0 != 0. LETIMERn_REP0 is decremented on each timer underflow. If LETIMERn_REP1 has been written, it is loaded into LETIMERn_REP0 when LETIMERn_REP0 is about to be decremented to 0. |
| 0b11    | Double       | The timer runs as long as LETIMERn_REP0 != 0 or LETIMERn_REP1 != 0. Both LETIMERn_REP0 and LETIMERn_REP1 are decremented at each timer underflow.  |

The interrupt flags REP0 and REP1 in LETIMERn\_IF are set whenever LETIMERn\_REP0 or LETIMERn\_REP1 are decremented to 0 respectively. REP0 is also set when the value of LETIMERn\_REP1 is loaded into LETIMERn\_REP0 in buffered mode.

### 22.3.3.3 Free-Running Mode

In free-running mode, the LETIMER acts as a regular timer and the repeat counter is disabled. When started, the timer runs until it is stopped using the STOP command bit in LETIMERn\_CMD. A state machine for this mode is shown in [Figure 22.2 LETIMER State Machine for Free-running Mode on page 757](#).



**Figure 22.2. LETIMER State Machine for Free-running Mode**

Note that the CLEAR command bit in LETIMERn\_CMD always has priority over other changes to LETIMERn\_CNT. When the clear command is used, LETIMERn\_CNT is set to 0 and an underflow event will not be generated when LETIMERn\_CNT wraps around to the top value or 0xFFFF. Since no underflow event is generated, no output action is performed. LETIMERn\_REP0, LETIMERn\_REP1, LETIMERn\_COMP0 and LETIMERn\_COMP1 are also left untouched.





### 22.3.3.6 Double Mode

The Double repeat mode works much like the one-shot repeat mode. The difference is that, where the one-shot mode counts as long as LETIMERn\_REP0 is larger than 0, the double mode counts as long as either LETIMERn\_REP0 or LETIMERn\_REP1 is larger than 0. As an example, say LETIMERn\_REP0 is 3 and LETIMERn\_REP1 is 10 when the timer is started. If no further interaction is done with the timer, LETIMERn\_REP0 will now be decremented 3 times, and LETIMERn\_REP1 will be decremented 10 times. The timer counts a total of 10 times, and LETIMERn\_REP0 is 0 after the first three timer underflows and stays at 0. LETIMERn\_REP0 and LETIMERn\_REP1 can be written at any time. After a write to either of these, the timer is guaranteed to underflow at least the written number of times if the timer is running. Use the Double repeat mode to generate output on both the LETIMER outputs at the same time. The state machine for this repeat mode can be seen in [Figure 22.5 LETIMER Double Repeat State Machine on page 760](#).

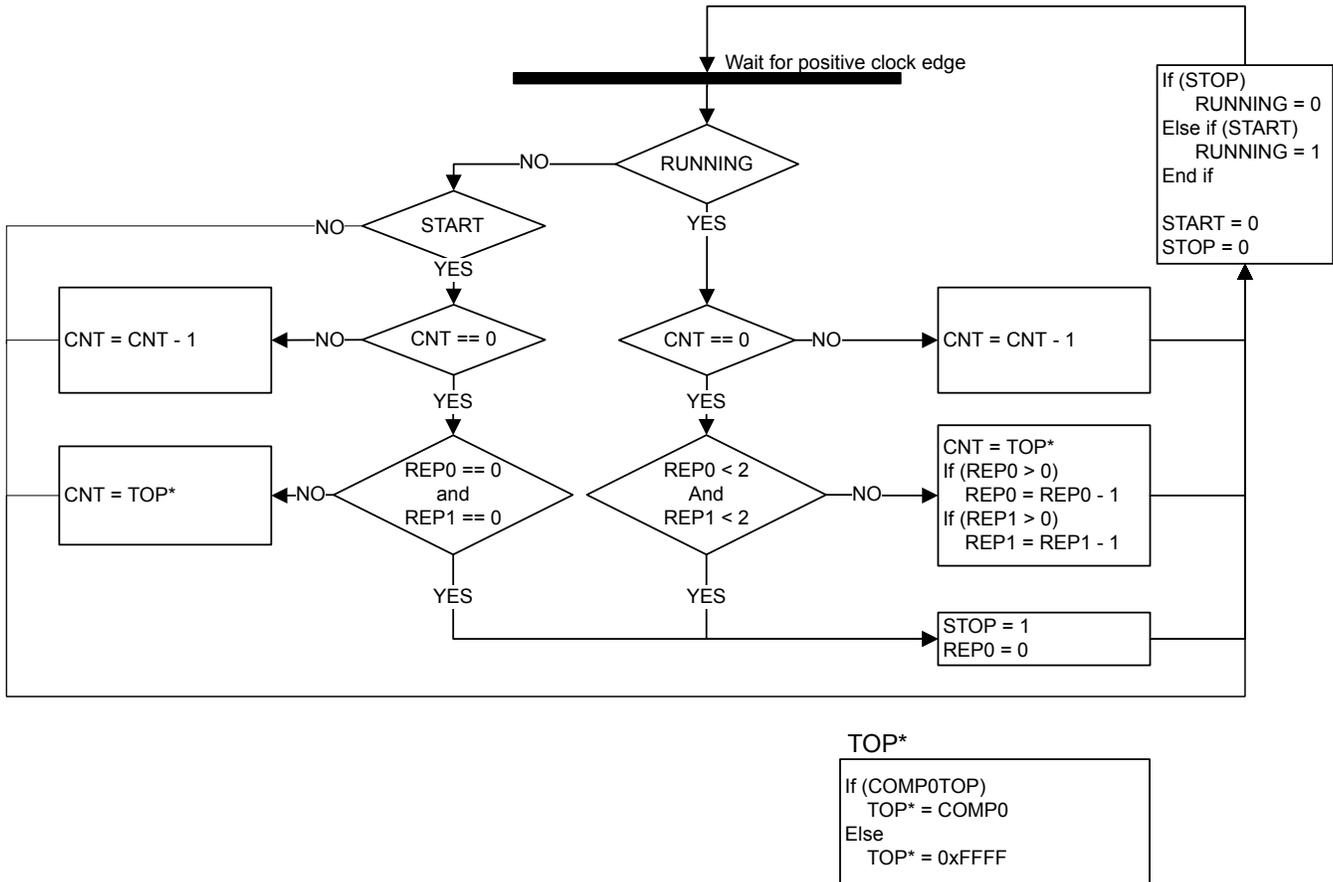


Figure 22.5. LETIMER Double Repeat State Machine

### 22.3.3.7 Clock Source

The LETIMER clock source and its prescaler value are defined in the Clock Management Unit (CMU). The LFACTL<sub>LETIMERn</sub> has a frequency given by [Figure 22.6 LETIMER Clock Frequency on page 760](#).

$$f_{LFACTL\_LETIMERn} = 32768/2^{LETIMERn}$$

Figure 22.6. LETIMER Clock Frequency

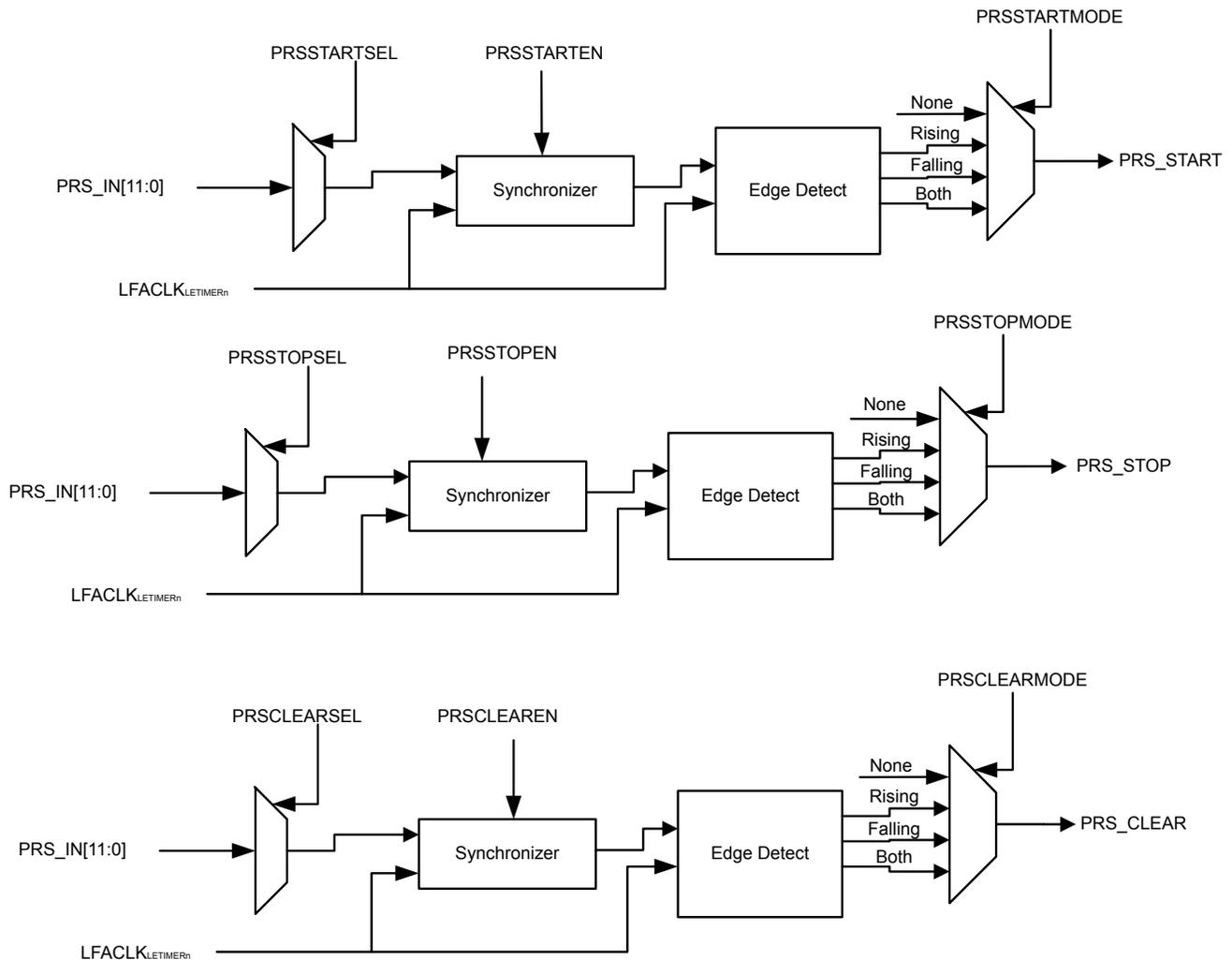
where the exponent LETIMERn is a 4 bit value in the CMU\_LFAPRESC0 register.

To use this module, the LE interface clock must be enabled in CMU\_HFBUSCLKEN0, in addition to the module clock.

### 22.3.3.8 PRS Input Triggers

The LETIMER can be configured to start, stop, and/or clear based on PRS inputs. The diagram showing the functions of the PRS input triggers is shown in [Figure 22.7 LETIMER PRS Input Triggers on page 761](#).

There are 12 PRS inputs to the LETIMER. PRSSTARTSEL, PRSSTOPSEL, and PRSCLEARSEL select which PRS inputs are used to start, stop, and/or clear the LETIMER. PRSSTARTMODE, PRSSTOPMODE, and PRSCLEARMODE select which edge or edge(s) can trigger the start, stop, and/or clear action. The PRSSTARTEN, PRSSTOPEN, and PRSCLEAREN signals shown in the diagram are derived from the PRSSTARTMODE, PRSSTOPMODE, and PRSCLEARMODE fields; if the corresponding bit field is set to NONE, the feature is disabled.



**Figure 22.7. LETIMER PRS Input Triggers**

### 22.3.3.9 Debug

If DEBUGRUN in LETIMERn\_CTRL is cleared, the LETIMER automatically stops counting when the CPU is halted during a debug session, and resumes operation when the CPU continues. Because of synchronization, the LETIMER is halted two clock cycles after the CPU is halted, and continues running two clock cycles after the CPU continues. RUNNING in LETIMERn\_STATUS is not cleared when the LETIMER stops because of a debug-session.

Set DEBUGRUN in LETIMERn\_CTRL to allow the LETIMER to continue counting even when the CPU is halted in debug mode.

### 22.3.4 Underflow Output Action

For each of the repeat registers, an underflow output action can be set. The configured output action is performed every time the counter underflows while the respective repeat register is nonzero. In PWM mode, the output is similarly only changed on COMP1 match if the repeat register is nonzero. As an example, the timer will perform 7 output actions if LETIMERN\_REP0 is set to 7 when starting the timer in one-shot mode and leaving it untouched.

The output actions can be set by configuring UFOA0 and UFOA1 in LETIMERN\_CTRL. UFOA0 defines the action on output 0, and is connected to LETIMERN\_REP0, while UFOA1 defines the action on output 1 and is connected to LETIMERN\_REP1. The possible actions are defined in [Table 22.2 LETIMER Underflow Output Actions on page 762](#).

**Table 22.2. LETIMER Underflow Output Actions**

| UF0A0/UF0A1 | Mode   | Description  |
|-------------|--------|--|
| 0b00        | Idle   | The output is held at its idle value   |
| 0b01        | Toggle | The output is toggled on LETIMERN_CNT underflow if LETIMERN_REPx is nonzero  |
| 0b10        | Pulse  | The output is held active for one clock cycle on LETIMERN_CNT underflow if LETIMERN_REPx is nonzero. It then returns to its idle value |
| 0b11        | PWM    | The output is set idle on LETIMERN_CNT underflow and active on compare match with LETIMERN_COMP1 if LETIMERN_REPx is nonzero.          |

**Note:**

- For the Pulse and PWM modes, the outputs will return to their idle states regardless of the state of the corresponding LETIMERN\_REPx registers. They will only be set active if the LETIMERN\_REPx registers are nonzero however.
- For free-running mode, LETIMERN\_REP0 != 0 for output generation to be enabled.

The polarity of the outputs can be set individually by configuring OPOL0 and OPOL1 in LETIMERN\_CTRL. When these are cleared, their respective outputs have a low idle value and a high active value. When they are set, the idle value is high, and the active value is low.

When using the toggle action, the outputs can be driven to their idle values by setting their respective CTO0/CTO1 command bits in LETIMERN\_CTRL. This can be used to put the output in a well-defined state before beginning to generate toggle output, which may be important in some applications. The command bit can also be used while the timer is running.

Some simple waveforms generated with the different output modes are shown in [Figure 22.8 LETIMER Simple Waveforms Output on page 763](#). For the example, REPMODE in LETIMERN\_CTRL has been cleared, COMP0TOP also in LETIMERN\_CTRL has been set and LETIMERN\_COMP0 has been written to 3. As seen in the figure, LETIMERN\_COMP0 now decides the length of the signal periods. For the toggle mode, the period of the output signal is  $2(\text{LETIMERN\_COMP0} + 1)$ , and for the pulse modes, the periods of the output signals are  $\text{LETIMERN\_COMP0} + 1$ . Note that the pulse outputs are delayed by one period relative to the toggle output. The pulses come at the end of their periods.

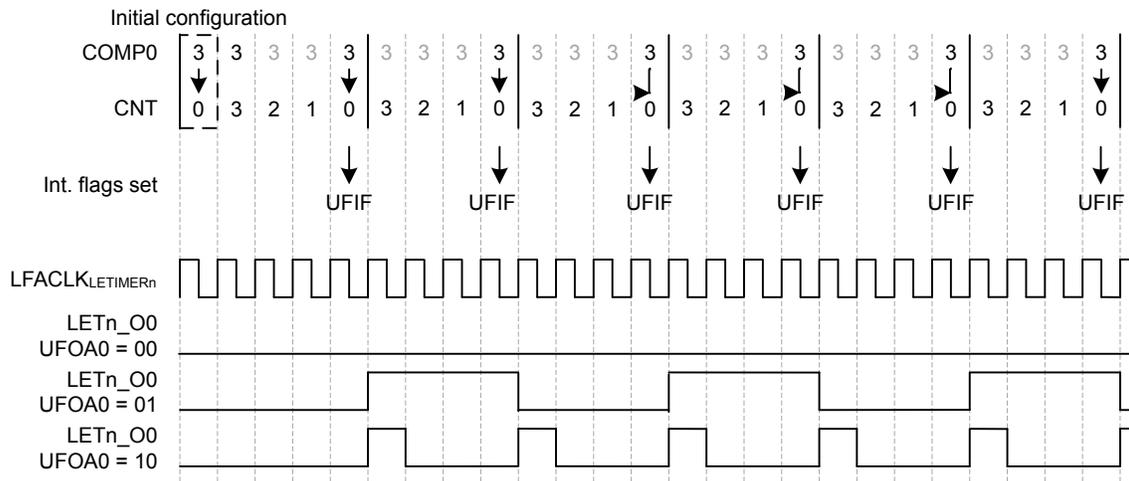


Figure 22.8. LETIMER Simple Waveforms Output

For the example in [Figure 22.9 LETIMER Repeated Counting on page 763](#), the One-shot repeat mode has been selected, and LETIMER<sub>n</sub>\_REP0 has been written to 3. The resulting behavior is pretty similar to that shown in Figure 6, but in this case, the timer stops after counting to zero LETIMER<sub>n</sub>\_REP0 times. By using LETIMER<sub>n</sub>\_REP0 the user has full control of the number of pulses/toggles generated on the output.

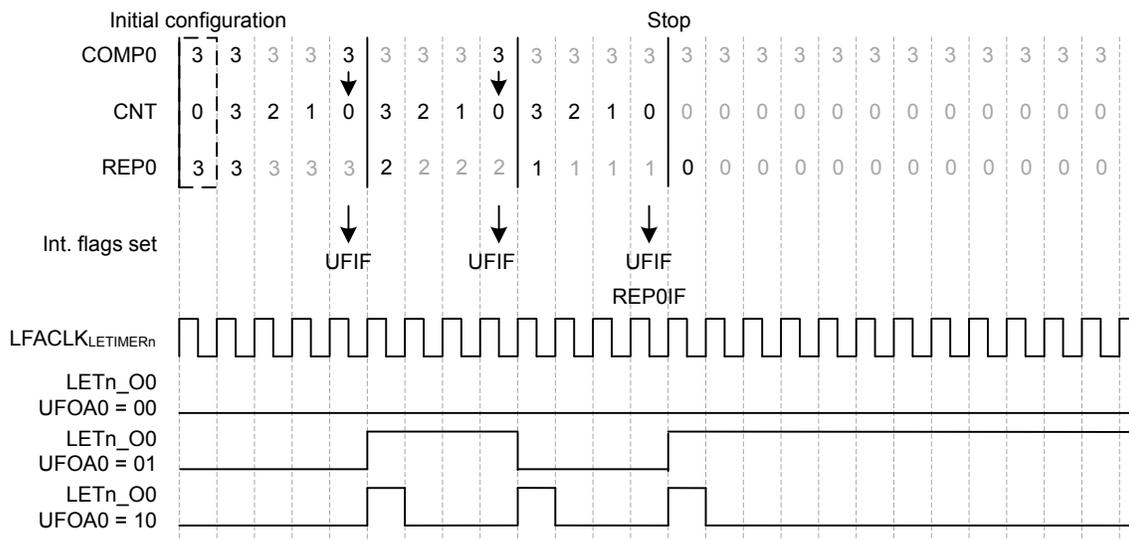
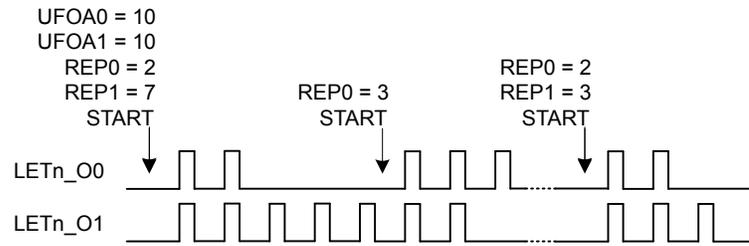


Figure 22.9. LETIMER Repeated Counting

Using the Double repeat mode, output can be generated on both the LETIMER outputs. [Figure 22.10 LETIMER Dual Output on page 764](#) shows an example of this. UFOA0 and UFOA1 in LETIMER<sub>n</sub>\_CTRL are configured for pulse output and the outputs are configured for low idle polarity. As seen in the figure, the number written to the repeat registers determine the number of pulses generated on each of the outputs.



**Figure 22.10. LETIMER Dual Output**

### 22.3.5 PRS Output

The LETIMER outputs can be routed out onto the PRS system. Enabling the PRS connection can be done by setting SOURCESEL to LETIMERx and SIGSEL to LETIMERxCHn in PRS\_CHx\_CTRL. The PRS register description can be found in [16.5 Register Description](#)

### 22.3.6 Examples

This section presents a couple of usage examples for the LETIMER.

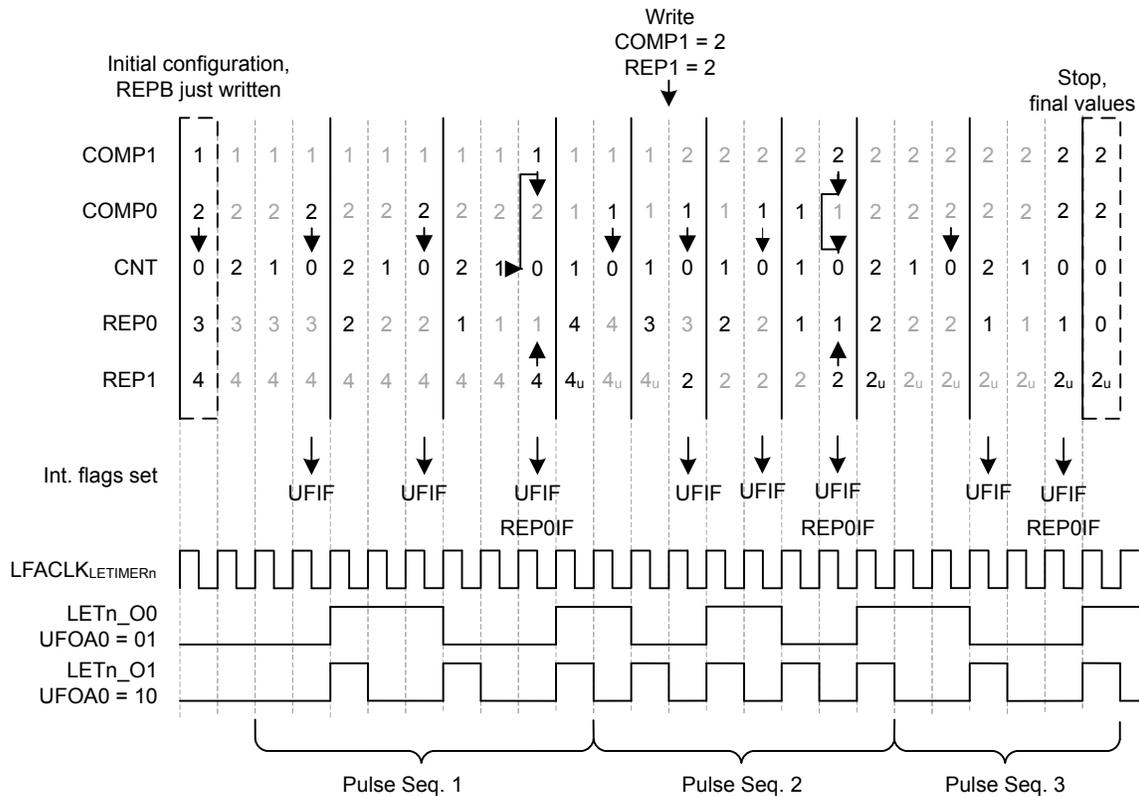


### 22.3.6.2 Continuous Output Generation

In some scenarios, it might be desired to make LETIMER generate a continuous waveform. Very simple constant waveforms can be generated without the repeat counter as shown in [Figure 22.8 LETIMER Simple Waveforms Output on page 763](#), but to generate changing waveforms, using the repeat counter and buffer registers can prove advantageous.

For the example in [Figure 22.12 LETIMER Continuous Operation on page 766](#), the goal is to produce a pulse train consisting of 3 sequences with the following properties:

- 3 pulses with periods of 3 cycles
- 4 pulses with periods of 2 cycles
- 2 pulses with periods of 3 cycles



**Figure 22.12. LETIMER Continuous Operation**

The first two sequences are loaded into the LETIMER before the timer is started.

LETIMERn\_COMP0 is set to 2 (cycles – 1), and LETIMERn\_REP0 is set to 3 for the first sequence, and the second sequence is loaded into the buffer registers, i.e. COMP1 is set to 1 and LETIMERn\_REP1 is set to 4.

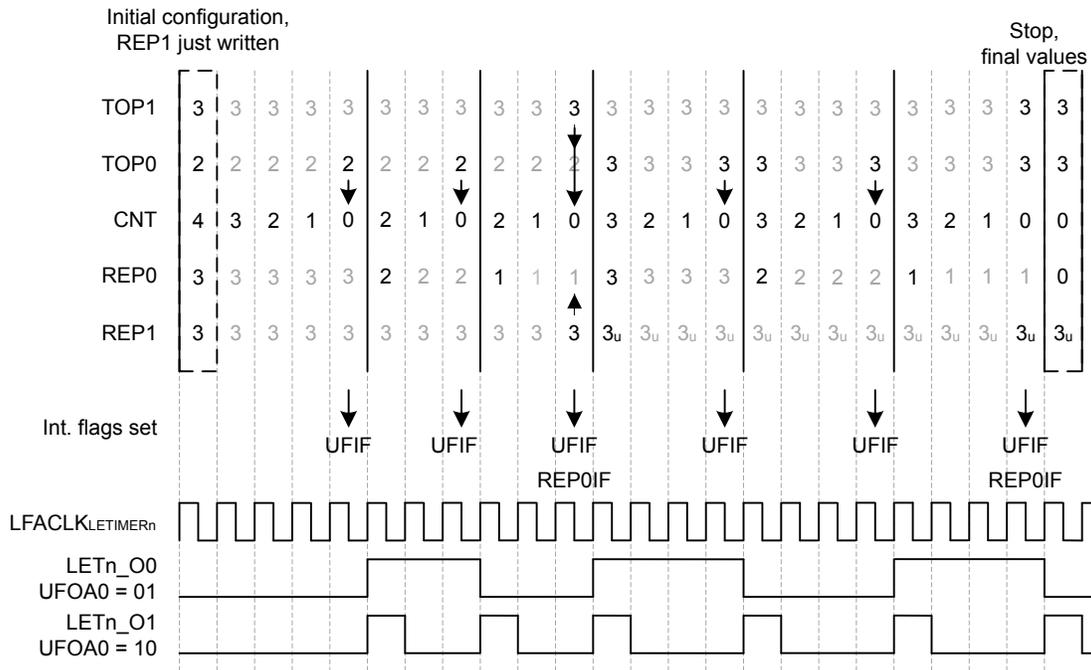
The LETIMER is set to trigger an interrupt when LETIMERn\_REP0 is done by setting REP0 in LETIMERn\_IEN. This interrupt is a good place to update the values of the buffers. Last but not least REPMODE in LETIMERn\_CTRL is set to buffered mode, and the timer is started.

In the interrupt routine the buffers are updated with the values for the third sequence. If this had not been done, the timer would have stopped after the second sequence.

The final result is shown in [Figure 22.12 LETIMER Continuous Operation on page 766](#). The pulse output is grouped to show which sequence generated which output. Toggle output is also shown in the figure. Note that the toggle output is not aligned with the pulse outputs.

**Note:** Multiple LETIMER cycles are required to write a value to the LETIMER registers. The example in [Figure 22.12 LETIMER Continuous Operation on page 766](#) assumes that writes are done in advance so they arrive in the LETIMER as described in the figure.

[Figure 22.13 LETIMER LETIMERn\\_CNT Not Initialized to 0 on page 767](#) shows an example where the LETIMER is started while LETIMERn\_CNT is nonzero. In this case the length of the first repetition is given by the value in LETIMERn\_CNT.



**Figure 22.13. LETIMER LETIMERn\_CNT Not Initialized to 0**

### 22.3.6.3 PWM Output

There are several ways of generating PWM output with the LETIMER, but the most straight-forward way is using the PWM output mode. This mode is enabled by setting UFOA0 or UFOA1 in LETIMERn\_CTRL to 3. In PWM mode, the output is set idle on timer underflow, and active on LETIMERn\_COMP1 match, so if for instance COMP0TOP = 1 and OPOL0 = 0 in LETIMERn\_CTRL, LETIMERn\_COMP0 determines the PWM period, and LETIMERn\_COMP1 determines the active period.

The PWM period in PWM mode is LETIMERn\_COMP0 + 1. There is no special handling of the case where LETIMERn\_COMP1 > LETIMERn\_COMP0, so if LETIMERn\_COMP1 > LETIMERn\_COMP0, the PWM output is given by the idle output value. This means that for OPOLx = 0 in LETIMERn\_CTRL, the PWM output will always be 0 for at least one clock cycle, and for OPOLx = 1 in LETIMERn\_CTRL, the PWM output will always be 1 for at least one clock cycle.

To generate a PWM signal using the full PWM range, invert OPOLx when LETIMERn\_COMP1 is set to a value larger than LETIMERn\_COMP0.

### 22.3.6.4 Interrupts

The interrupts generated by the LETIMER are combined into one interrupt vector. If the interrupt for the LETIMER is enabled, an interrupt will be made if one or more of the interrupt flags in LETIMERn\_IF and their corresponding bits in LETIMER\_IEN are set.

### 22.3.7 Register Access

This module is a Low Energy Peripheral, and supports immediate synchronization. For description regarding immediate synchronization, the reader is referred to [4.3.1 Writing](#).

## 22.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name               | Type  | Description                     |
|--------|--------------------|-------|---------------------------------|
| 0x000  | LETIMERn_CTRL      | RW    | Control Register                |
| 0x004  | LETIMERn_CMD       | W1    | Command Register                |
| 0x008  | LETIMERn_STATUS    | R     | Status Register                 |
| 0x00C  | LETIMERn_CNT       | RWH   | Counter Value Register          |
| 0x010  | LETIMERn_COMP0     | RWH   | Compare Value Register 0        |
| 0x014  | LETIMERn_COMP1     | RW    | Compare Value Register 1        |
| 0x018  | LETIMERn_REP0      | RWH   | Repeat Counter Register 0       |
| 0x01C  | LETIMERn_REP1      | RWH   | Repeat Counter Register 1       |
| 0x020  | LETIMERn_IF        | R     | Interrupt Flag Register         |
| 0x024  | LETIMERn_IFS       | W1    | Interrupt Flag Set Register     |
| 0x028  | LETIMERn_IFC       | (R)W1 | Interrupt Flag Clear Register   |
| 0x02C  | LETIMERn_IEN       | RW    | Interrupt Enable Register       |
| 0x034  | LETIMERn_SYNCBUSY  | R     | Synchronization Busy Register   |
| 0x040  | LETIMERn_ROUTEPEN  | RW    | I/O Routing Pin Enable Register |
| 0x044  | LETIMERn_ROUTELOC0 | RW    | I/O Routing Location Register   |
| 0x050  | LETIMERn_PRSEL     | RW    | PRS Input Select Register       |



| Bit | Name    | Reset    | Access | Description   |
|-----|---------|----------|--------|---|
| 5:4 | UFOA1   | 0x0      | RW     | <b>Underflow Output Action 1</b><br>Defines the action on LETn_O1 on a LETIMER underflow.   |
|     | Value   | Mode     |        | Description   |
|     | 0       | NONE     |        | LETn_O1 is held at its idle value as defined by OPOL1   |
|     | 1       | TOGGLE   |        | LETn_O1 is toggled on CNT underflow   |
|     | 2       | PULSE    |        | LETn_O1 is held active for one LFACLK <sub>LETIMER0</sub> clock cycle on CNT underflow. The output then returns to its idle value as defined by OPOL1 |
|     | 3       | PWM      |        | LETn_O1 is set idle on CNT underflow, and active on compare match with COMP1  |
| 3:2 | UFOA0   | 0x0      | RW     | <b>Underflow Output Action 0</b><br>Defines the action on LETn_O0 on a LETIMER underflow.   |
|     | Value   | Mode     |        | Description   |
|     | 0       | NONE     |        | LETn_O0 is held at its idle value as defined by OPOLO   |
|     | 1       | TOGGLE   |        | LETn_O0 is toggled on CNT underflow   |
|     | 2       | PULSE    |        | LETn_O0 is held active for one LFACLK <sub>LETIMER0</sub> clock cycle on CNT underflow. The output then returns to its idle value as defined by OPOLO |
|     | 3       | PWM      |        | LETn_O0 is set idle on CNT underflow, and active on compare match with COMP1  |
| 1:0 | REPMODE | 0x0      | RW     | <b>Repeat Mode</b><br>Allows the repeat counter to be enabled and disabled.   |
|     | Value   | Mode     |        | Description   |
|     | 0       | FREE     |        | When started, the LETIMER counts down until it is stopped by software   |
|     | 1       | ONESHOT  |        | The counter counts REP0 times. When REP0 reaches zero, the counter stops  |
|     | 2       | BUFFERED |        | The counter counts REP0 times. If REP1 has been written, it is loaded into REP0 when REP0 reaches zero, otherwise the counter stops                   |
|     | 3       | DOUBLE   |        | Both REP0 and REP1 are decremented when the LETIMER wraps around. The LETIMER counts until both REP0 and REP1 are zero                                |

## 22.5.2 LETIMERn\_CMD - Command Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |      |      |       |      |       |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------|------|-------|------|-------|---|---|---|---|---|---|---|
| 0x004         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11   | 10   | 9     | 8    | 7     | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0    | 0    | 0     | 0    | 0     |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W1   | W1   | W1    | W1   | W1    |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CTO1 | CTO0 | CLEAR | STOP | START |   |   |   |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description  |
|------|----------|--|--------|--|
| 31:5 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 4    | CTO1     | 0  | W1     | <b>Clear Toggle Output 1</b><br>Set to drive toggle output 1 to its idle value |
| 3    | CTO0     | 0  | W1     | <b>Clear Toggle Output 0</b><br>Set to drive toggle output 0 to its idle value |
| 2    | CLEAR    | 0  | W1     | <b>Clear LETIMER</b><br>Set to clear LETIMER                                   |
| 1    | STOP     | 0  | W1     | <b>Stop LETIMER</b><br>Set to stop LETIMER                                     |
| 0    | START    | 0  | W1     | <b>Start LETIMER</b><br>Set to start LETIMER                                   |

## 22.5.3 LETIMERn\_STATUS - Status Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|---|---|---|---|---|---|---|---|---|---|
| 0x008         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11      | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0       | 0  |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R       | R  |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RUNNING |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description  |
|------|----------|--|--------|--|
| 31:1 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 0    | RUNNING  | 0  | R      | <b>LETIMER Running</b><br>Set when LETIMER is running. |

## 22.5.4 LETIMERn\_CNT - Counter Value Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x00C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CNT    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description   |
|-------|----------|--|--------|---|
| 31:16 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 15:0  | CNT      | 0x0000   | RWH    | <b>Counter Value</b><br>Use to read the current value of the LETIMER. |

## 22.5.5 LETIMERn\_COMP0 - Compare Value Register 0 (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x010         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | COMP0  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description   |
|-------|----------|--|--------|---|
| 31:16 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 15:0  | COMP0    | 0x0000   | RWH    | <b>Compare Value 0</b><br>Compare and optionally top value for LETIMER. |

### 22.5.6 LETIMERn\_COMP1 - Compare Value Register 1 (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x014         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | COMP1  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description  |
|-------|----------|--|--------|--|
| 31:16 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 15:0  | COMP1    | 0x0000   | RW     | <b>Compare Value 1</b><br>Compare and optionally buffered top value for LETIMER. |

### 22.5.7 LETIMERn\_REP0 - Repeat Counter Register 0 (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x018         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15   | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | REP0 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description   |
|------|----------|--|--------|---|
| 31:8 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 7:0  | REP0     | 0x00   | RWH    | <b>Repeat Counter 0</b><br>Optional repeat counter. |

### 22.5.8 LETIMERn\_REP1 - Repeat Counter Register 1 (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |      |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|------|---|---|---|---|---|---|---|
| 0x01C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x00 |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RWH  |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | REP1 |   |   |   |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description  |
|------|----------|--|--------|--|
| 31:8 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 7:0  | REP1     | 0x00   | RWH    | <b>Repeat Counter 1</b><br>Optional repeat counter or buffer for REP0. |

### 22.5.9 LETIMERn\_IF - Interrupt Flag Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |      |      |    |       |       |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|------|------|----|-------|-------|---|---|---|
| 0x020         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7    | 6    | 5  | 4     | 3     | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0    | 0    | 0  | 0     | 0     |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | R    | R    | R  | R     | R     |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | REP1 | REP0 | UF | COMP1 | COMP0 |   |   |   |

| Bit  | Name     | Reset  | Access | Description  |
|------|----------|--|--------|--|
| 31:5 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 4    | REP1     | 0  | R      | <b>Repeat Counter 1 Interrupt Flag</b><br>Set when repeat counter 1 reaches zero.  |
| 3    | REP0     | 0  | R      | <b>Repeat Counter 0 Interrupt Flag</b><br>Set when repeat counter 0 reaches zero or when the REP1 interrupt flag is loaded into the REP0 interrupt flag. |
| 2    | UF       | 0  | R      | <b>Underflow Interrupt Flag</b><br>Set on LETIMER underflow.   |
| 1    | COMP1    | 0  | R      | <b>Compare Match 1 Interrupt Flag</b><br>Set when LETIMER reaches the value of COMP1.  |
| 0    | COMP0    | 0  | R      | <b>Compare Match 0 Interrupt Flag</b><br>Set when LETIMER reaches the value of COMP0.  |







22.5.14 LETIMERn\_ROUTE PEN - I/O Routing Pin Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |         |         |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---------|---------|---|---|
| 0x040         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3       | 2       | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0       | 0       |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | RW      | RW      |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | OUT1PEN | OUT0PEN |   |   |

| Bit  | Name     | Reset   | Access | Description   |
|------|----------|---|--------|---|
| 31:2 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 1    | OUT1PEN  | 0   | RW     | <b>Output 1 Pin Enable</b><br>When set, output 1 of the LETIMER is enabled. |
|      | Value    | Description   |        |   |
|      | 0        | The LETn_O1 pin is disabled   |        |   |
|      | 1        | The LETn_O1 pin is enabled  |        |   |
| 0    | OUT0PEN  | 0   | RW     | <b>Output 0 Pin Enable</b><br>When set, output 0 of the LETIMER is enabled. |
|      | Value    | Description   |        |   |
|      | 0        | The LETn_O0 pin is disabled   |        |   |
|      | 1        | The LETn_O0 pin is enabled  |        |   |

22.5.15 LETIMERn\_ROUTELOC0 - I/O Routing Location Register

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x044  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Access |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Name   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | OUT1LOC |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description |
|-------|----------|--|--------|-------------|
| 31:14 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |             |

13:8    OUT1LOC    0x00    RW    **I/O Location**

Decides the location of the LETIMER OUT1 pin.

| Value | Mode  | Description |
|-------|-------|-------------|
| 0     | LOC0  | Location 0  |
| 1     | LOC1  | Location 1  |
| 2     | LOC2  | Location 2  |
| 3     | LOC3  | Location 3  |
| 4     | LOC4  | Location 4  |
| 5     | LOC5  | Location 5  |
| 6     | LOC6  | Location 6  |
| 7     | LOC7  | Location 7  |
| 8     | LOC8  | Location 8  |
| 9     | LOC9  | Location 9  |
| 10    | LOC10 | Location 10 |
| 11    | LOC11 | Location 11 |
| 12    | LOC12 | Location 12 |
| 13    | LOC13 | Location 13 |
| 14    | LOC14 | Location 14 |
| 15    | LOC15 | Location 15 |
| 16    | LOC16 | Location 16 |
| 17    | LOC17 | Location 17 |
| 18    | LOC18 | Location 18 |
| 19    | LOC19 | Location 19 |
| 20    | LOC20 | Location 20 |
| 21    | LOC21 | Location 21 |
| 22    | LOC22 | Location 22 |

| Bit | Name            | Reset   | Access | Description  |
|-----|-----------------|---|--------|--|
|     | 23              | LOC23   |        | Location 23  |
|     | 24              | LOC24   |        | Location 24  |
|     | 25              | LOC25   |        | Location 25  |
|     | 26              | LOC26   |        | Location 26  |
|     | 27              | LOC27   |        | Location 27  |
|     | 28              | LOC28   |        | Location 28  |
|     | 29              | LOC29   |        | Location 29  |
|     | 30              | LOC30   |        | Location 30  |
|     | 31              | LOC31   |        | Location 31  |
| 7:6 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 5:0 | OUT0LOC         | 0x00  | RW     | <b>I/O Location</b><br>Decides the location of the LETIMER OUT0 pin. |
|     | Value           | Mode  |        | Description  |
|     | 0               | LOC0  |        | Location 0   |
|     | 1               | LOC1  |        | Location 1   |
|     | 2               | LOC2  |        | Location 2   |
|     | 3               | LOC3  |        | Location 3   |
|     | 4               | LOC4  |        | Location 4   |
|     | 5               | LOC5  |        | Location 5   |
|     | 6               | LOC6  |        | Location 6   |
|     | 7               | LOC7  |        | Location 7   |
|     | 8               | LOC8  |        | Location 8   |
|     | 9               | LOC9  |        | Location 9   |
|     | 10              | LOC10   |        | Location 10  |
|     | 11              | LOC11   |        | Location 11  |
|     | 12              | LOC12   |        | Location 12  |
|     | 13              | LOC13   |        | Location 13  |
|     | 14              | LOC14   |        | Location 14  |
|     | 15              | LOC15   |        | Location 15  |
|     | 16              | LOC16   |        | Location 16  |
|     | 17              | LOC17   |        | Location 17  |
|     | 18              | LOC18   |        | Location 18  |
|     | 19              | LOC19   |        | Location 19  |
|     | 20              | LOC20   |        | Location 20  |
|     | 21              | LOC21   |        | Location 21  |
|     | 22              | LOC22   |        | Location 22  |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
| 23  |      | LOC23 |        | Location 23 |
| 24  |      | LOC24 |        | Location 24 |
| 25  |      | LOC25 |        | Location 25 |
| 26  |      | LOC26 |        | Location 26 |
| 27  |      | LOC27 |        | Location 27 |
| 28  |      | LOC28 |        | Location 28 |
| 29  |      | LOC29 |        | Location 29 |
| 30  |      | LOC30 |        | Location 30 |
| 31  |      | LOC31 |        | Location 31 |

## 22.5.16 LETIMERn\_PRSEL - PRS Input Select Register

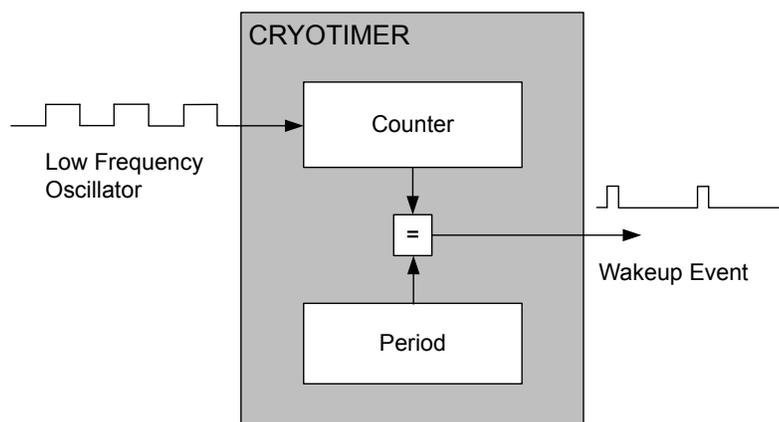
| Offset        | Bit Position |    |    |    |              |    |    |    |    |             |    |    |    |    |               |    |    |    |    |             |    |    |   |   |             |   |   |   |   |              |   |   |
|---------------|--------------|----|----|----|--------------|----|----|----|----|-------------|----|----|----|----|---------------|----|----|----|----|-------------|----|----|---|---|-------------|---|---|---|---|--------------|---|---|
| 0x050         | 31           | 30 | 29 | 28 | 27           | 26 | 25 | 24 | 23 | 22          | 21 | 20 | 19 | 18 | 17            | 16 | 15 | 14 | 13 | 12          | 11 | 10 | 9 | 8 | 7           | 6 | 5 | 4 | 3 | 2            | 1 | 0 |
| <b>Reset</b>  |              |    |    |    | 0x0          |    |    |    |    | 0x0         |    |    |    |    | 0x0           |    |    |    |    | 0x0         |    |    |   |   | 0x0         |   |   |   |   | 0x0          |   |   |
| <b>Access</b> |              |    |    |    | RW           |    |    |    |    | RW          |    |    |    |    | RW            |    |    |    |    | RW          |    |    |   |   | RW          |   |   |   |   | RW           |   |   |
| <b>Name</b>   |              |    |    |    | PRSCLEARMODE |    |    |    |    | PRSSTOPMODE |    |    |    |    | PRSSSTARTMODE |    |    |    |    | PRSCLEARSEL |    |    |   |   | PRSSSTOPSEL |   |   |   |   | PRSSSTARTSEL |   |   |

| Bit   | Name            | Reset   | Access | Description  |       |      |             |   |      |                              |   |        |   |   |         |  |   |      |   |
|-------|-----------------|---|--------|--|-------|------|-------------|---|------|------------------------------|---|--------|---|---|---------|--|---|------|---|
| 31:28 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |      |                              |   |        |   |   |         |  |   |      |   |
| 27:26 | PRSCLEARMODE    | 0x0   | RW     | <b>PRS Clear Mode</b><br>Determines mode for PRS input clear.<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>NONE</td> <td>PRS cannot clear the LETIMER</td> </tr> <tr> <td>1</td> <td>RISING</td> <td>Rising edge of selected PRS input can clear the LETIMER</td> </tr> <tr> <td>2</td> <td>FALLING</td> <td>Falling edge of selected PRS input can clear the LETIMER</td> </tr> <tr> <td>3</td> <td>BOTH</td> <td>Both the rising or falling edge of the selected PRS input can clear the LETIMER</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | NONE | PRS cannot clear the LETIMER | 1 | RISING | Rising edge of selected PRS input can clear the LETIMER | 2 | FALLING | Falling edge of selected PRS input can clear the LETIMER | 3 | BOTH | Both the rising or falling edge of the selected PRS input can clear the LETIMER |
| Value | Mode            | Description   |        |  |       |      |             |   |      |                              |   |        |   |   |         |  |   |      |   |
| 0     | NONE            | PRS cannot clear the LETIMER  |        |  |       |      |             |   |      |                              |   |        |   |   |         |  |   |      |   |
| 1     | RISING          | Rising edge of selected PRS input can clear the LETIMER   |        |  |       |      |             |   |      |                              |   |        |   |   |         |  |   |      |   |
| 2     | FALLING         | Falling edge of selected PRS input can clear the LETIMER  |        |  |       |      |             |   |      |                              |   |        |   |   |         |  |   |      |   |
| 3     | BOTH            | Both the rising or falling edge of the selected PRS input can clear the LETIMER   |        |  |       |      |             |   |      |                              |   |        |   |   |         |  |   |      |   |
| 25:24 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |      |                              |   |        |   |   |         |  |   |      |   |
| 23:22 | PRSSTOPMODE     | 0x0   | RW     | <b>PRS Stop Mode</b><br>Determines mode for PRS input stop.<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>NONE</td> <td>PRS cannot stop the LETIMER</td> </tr> <tr> <td>1</td> <td>RISING</td> <td>Rising edge of selected PRS input can stop the LETIMER</td> </tr> <tr> <td>2</td> <td>FALLING</td> <td>Falling edge of selected PRS input can stop the LETIMER</td> </tr> <tr> <td>3</td> <td>BOTH</td> <td>Both the rising or falling edge of the selected PRS input can stop the LETIMER</td> </tr> </tbody> </table>       | Value | Mode | Description | 0 | NONE | PRS cannot stop the LETIMER  | 1 | RISING | Rising edge of selected PRS input can stop the LETIMER  | 2 | FALLING | Falling edge of selected PRS input can stop the LETIMER  | 3 | BOTH | Both the rising or falling edge of the selected PRS input can stop the LETIMER  |
| Value | Mode            | Description   |        |  |       |      |             |   |      |                              |   |        |   |   |         |  |   |      |   |
| 0     | NONE            | PRS cannot stop the LETIMER   |        |  |       |      |             |   |      |                              |   |        |   |   |         |  |   |      |   |
| 1     | RISING          | Rising edge of selected PRS input can stop the LETIMER  |        |  |       |      |             |   |      |                              |   |        |   |   |         |  |   |      |   |
| 2     | FALLING         | Falling edge of selected PRS input can stop the LETIMER   |        |  |       |      |             |   |      |                              |   |        |   |   |         |  |   |      |   |
| 3     | BOTH            | Both the rising or falling edge of the selected PRS input can stop the LETIMER  |        |  |       |      |             |   |      |                              |   |        |   |   |         |  |   |      |   |
| 21:20 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |      |                              |   |        |   |   |         |  |   |      |   |
| 19:18 | PRSSSTARTMODE   | 0x0   | RW     | <b>PRS Start Mode</b><br>Determines mode for PRS input start.<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>NONE</td> <td>PRS cannot start the LETIMER</td> </tr> <tr> <td>1</td> <td>RISING</td> <td>Rising edge of selected PRS input can start the LETIMER</td> </tr> </tbody> </table>   | Value | Mode | Description | 0 | NONE | PRS cannot start the LETIMER | 1 | RISING | Rising edge of selected PRS input can start the LETIMER |   |         |  |   |      |   |
| Value | Mode            | Description   |        |  |       |      |             |   |      |                              |   |        |   |   |         |  |   |      |   |
| 0     | NONE            | PRS cannot start the LETIMER  |        |  |       |      |             |   |      |                              |   |        |   |   |         |  |   |      |   |
| 1     | RISING          | Rising edge of selected PRS input can start the LETIMER   |        |  |       |      |             |   |      |                              |   |        |   |   |         |  |   |      |   |

| Bit   | Name            | Reset   | Access                           | Description   |
|-------|-----------------|---|----------------------------------|---|
|       | 2               | FALLING   |                                  | Falling edge of selected PRS input can start the LETIMER                        |
|       | 3               | BOTH  |                                  | Both the rising or falling edge of the selected PRS input can start the LETIMER |
| 17:16 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                  |   |
| 15:12 | PRSCLEARSEL     | 0x0   | RW                               | <b>PRS Clear Select</b><br>Determines which PRS input can clear the LETIMER.    |
|       | Value           | Mode  | Description                      |   |
|       | 0               | PRSCH0  | PRS Channel 0 selected as input  |   |
|       | 1               | PRSCH1  | PRS Channel 1 selected as input  |   |
|       | 2               | PRSCH2  | PRS Channel 2 selected as input  |   |
|       | 3               | PRSCH3  | PRS Channel 3 selected as input  |   |
|       | 4               | PRSCH4  | PRS Channel 4 selected as input  |   |
|       | 5               | PRSCH5  | PRS Channel 5 selected as input  |   |
|       | 6               | PRSCH6  | PRS Channel 6 selected as input  |   |
|       | 7               | PRSCH7  | PRS Channel 7 selected as input  |   |
|       | 8               | PRSCH8  | PRS Channel 8 selected as input  |   |
|       | 9               | PRSCH9  | PRS Channel 9 selected as input  |   |
|       | 10              | PRSCH10   | PRS Channel 10 selected as input |   |
|       | 11              | PRSCH11   | PRS Channel 11 selected as input |   |
| 11:10 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                  |   |
| 9:6   | PRSTOPSEL       | 0x0   | RW                               | <b>PRS Stop Select</b><br>Determines which PRS input can stop the LETIMER.      |
|       | Value           | Mode  | Description                      |   |
|       | 0               | PRSCH0  | PRS Channel 0 selected as input  |   |
|       | 1               | PRSCH1  | PRS Channel 1 selected as input  |   |
|       | 2               | PRSCH2  | PRS Channel 2 selected as input  |   |
|       | 3               | PRSCH3  | PRS Channel 3 selected as input  |   |
|       | 4               | PRSCH4  | PRS Channel 4 selected as input  |   |
|       | 5               | PRSCH5  | PRS Channel 5 selected as input  |   |
|       | 6               | PRSCH6  | PRS Channel 6 selected as input  |   |
|       | 7               | PRSCH7  | PRS Channel 7 selected as input  |   |
|       | 8               | PRSCH8  | PRS Channel 8 selected as input  |   |
|       | 9               | PRSCH9  | PRS Channel 9 selected as input  |   |
|       | 10              | PRSCH10   | PRS Channel 10 selected as input |   |
|       | 11              | PRSCH11   | PRS Channel 11 selected as input |   |

| Bit | Name       | Reset   | Access                           | Description  |
|-----|------------|---|----------------------------------|--|
| 5:4 | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                  |  |
| 3:0 | PRSTARTSEL | 0x0   | RW                               | <b>PRS Start Select</b><br>Determines which PRS input can start the LETIMER. |
|     | Value      | Mode  | Description                      |  |
|     | 0          | PRSCH0  | PRS Channel 0 selected as input  |  |
|     | 1          | PRSCH1  | PRS Channel 1 selected as input  |  |
|     | 2          | PRSCH2  | PRS Channel 2 selected as input  |  |
|     | 3          | PRSCH3  | PRS Channel 3 selected as input  |  |
|     | 4          | PRSCH4  | PRS Channel 4 selected as input  |  |
|     | 5          | PRSCH5  | PRS Channel 5 selected as input  |  |
|     | 6          | PRSCH6  | PRS Channel 6 selected as input  |  |
|     | 7          | PRSCH7  | PRS Channel 7 selected as input  |  |
|     | 8          | PRSCH8  | PRS Channel 8 selected as input  |  |
|     | 9          | PRSCH9  | PRS Channel 9 selected as input  |  |
|     | 10         | PRSCH10   | PRS Channel 10 selected as input |  |
|     | 11         | PRSCH11   | PRS Channel 11 selected as input |  |

## 23. CRYOTIMER - Ultra Low Energy Timer/Counter



### Quick Facts

#### What?

The CRYOTIMER is a timer capable of providing wakeup events/interrupts after deterministic intervals in all energy modes, including EM4.

#### Why?

The CRYOTIMER enables the chip to remain in the lowest energy modes for long durations, while keeping track of time and being able to wake up at regular intervals, all with an absolute minimum current consumption.

#### How?

Using a counter running on a prescaled Low Frequency Oscillator, the CRYOTIMER can provide periodic wakeup events with a very wide period range.

### 23.1 Introduction

The CRYOTIMER is a 32 bit counter which operates on a low frequency oscillator, and is capable of running in all energy modes. It can provide periodic wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a very wide range of periods for the interrupts facilitating flexible ultra-low energy operation.

Because of its simplicity, the CRYOTIMER is a lower energy solution for periodically waking up the MCU compared to the RTCC.

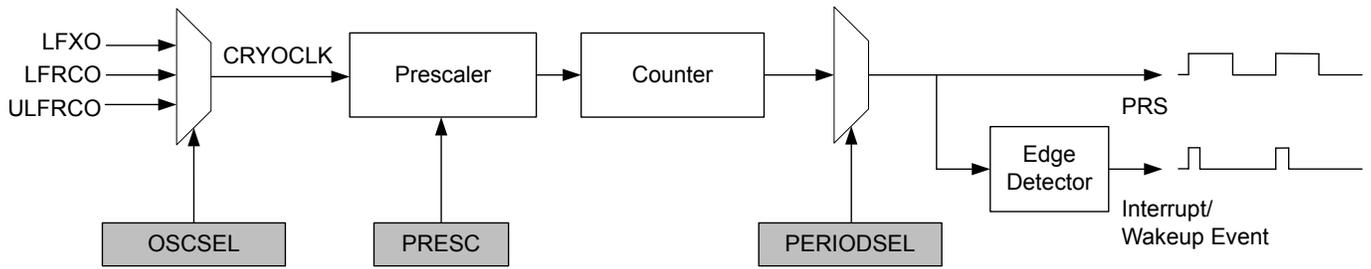
### 23.2 Features

- 32 bit Counter
- Works in all the energy modes
- Only External and Power-On resets reset the CRYOTIMER
- Interrupt/wake up event after deterministic intervals
- PRS Output
- Debug mode
  - Configurable to either run or stop when processor is stopped (break)

### 23.3 Functional Description

### 23.3.1 Block Diagram

An overview of the CRYOTIMER is shown in [Figure 23.1 CRYOTIMER Block Overview on page 786](#).



**Figure 23.1. CRYOTIMER Block Overview**

### 23.3.2 Operation

The desired low frequency oscillator for the CRYOTIMER operation can be selected by using OSCSEL in CRYOTIMER\_CTRL. The selection must be made before enabling the CRYOTIMER, and it must be ensured that the selected oscillator is ready. This can be checked by observing LFXORDY or LFRCORDY (depending upon the oscillator selection) in CMU\_STATUS. Note that the ULFRCO is always ready.

By default the CRYOTIMER is held in reset. It can be started by setting EN in CRYOTIMER\_CTRL. The CRYOTIMER, when running, is reset by clearing EN.

The timer counts at a frequency determined by PRESC in CRYOTIMER\_CTRL. This value should be set before the CRYOTIMER is enabled. Setting PRESC to 0 gives the maximum resolution, while higher values allow longer periods, see [Table 23.1 CRYOTIMER Resolution vs Maximum Wakeup Event/Interrupt Period](#),  $F_{CRYOCLK} = 32768$  Hz on page 787.

The 32-bit Counter provides 32 different options for selecting the duration between the Wakeup events. The selected duration is specified by CRYOTIMER\_PERIODSEL. It should be configured before the CRYOTIMER is enabled.

$$T_{WU} = (2^{PRESC} \times 2^{PERIODSEL})/f_{CRYOCLK}$$

**Figure 23.2. Duration Between the CRYOTIMER Wakeup Events in Seconds**

**Table 23.1. CRYOTIMER Resolution vs Maximum Wakeup Event/Interrupt Period,  $F_{CRYOCLK} = 32768$  Hz**

| CRYOTIMER_CTRL_PRESC | Resolution, $2^{PRESC}/f_{CRYOCLK}$ | Maximum Wakeup event/Interrupt Period |
|----------------------|-------------------------------------|---------------------------------------|
| DIV1                 | 30.5 $\mu$ s                        | 36.4 hours                            |
| DIV2                 | 61 $\mu$ s                          | 72.8 hours                            |
| DIV4                 | 122 $\mu$ s                         | 145.6 hours                           |
| DIV8                 | 244 $\mu$ s                         | 12 days                               |
| DIV16                | 488 $\mu$ s                         | 24 days                               |
| DIV32                | 977 $\mu$ s                         | 48 days                               |
| DIV64                | 1.95 ms                             | 97 days                               |
| DIV128               | 3.91 ms                             | 194 days                              |

The 32-bit counter value of the CRYOTIMER can be read using the CRYOTIMER\_CNT register.

The PRS output pulses of the CRYOTIMER are 1 CRYOCLK clock cycle wide. However, if the PRESC and PERIODSEL are both set to 0, the width of these pulses will be half CRYOCLK time period.

The CRYOTIMER wakeup events set the flag in the CRYOTIMER\_IF. Interrupt on this event can be enabled by using the CRYOTIMER\_IEN register.

The CRYOTIMER is always reset by the External Pin and Power-On resets. Additionally, by using EMU\_CTRL, it can also be configured to reset by Watchdog, lockup, and system request resets.

**Note:** The CRYOTIMER configuration bits/registers should only be changed when EN in CRYOTIMER\_CTRL is cleared.

### 23.3.3 Debug Mode

When the CPU is halted in debug mode, the CRYOTIMER can be configured to either continue to run or to be frozen. This is configured using DEBUGRUN in CRYOTIMER\_CTRL.

### 23.3.4 Energy Mode Availability

The CRYOTIMER is available in all energy modes. Wakeup from EM2 Deep Sleep and EM3 Stop to EM0 Active can be performed using the regular interrupt as discussed in [23.3.2 Operation](#). To generate wakeup events during EM4 Hibernate/Shutoff, EM4WU in CRYOTIMER\_EM4WUEN must be set to 1. Since the interrupt flag serves as the wakeup source, it must be cleared by software after exiting a low energy mode. Refer to [11. EMU - Energy Management Unit](#) for details on how to configure the EMU.

## 23.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name                | Type  | Description                   |
|--------|---------------------|-------|-------------------------------|
| 0x000  | CRYOTIMER_CTRL      | RW    | Control Register              |
| 0x004  | CRYOTIMER_PERIODSEL | RW    | Interrupt Duration            |
| 0x008  | CRYOTIMER_CNT       | R     | Counter Value                 |
| 0x00C  | CRYOTIMER_EM4WUEN   | RW    | Wake Up Enable                |
| 0x010  | CRYOTIMER_IF        | R     | Interrupt Flag Register       |
| 0x014  | CRYOTIMER_IFS       | W1    | Interrupt Flag Set Register   |
| 0x018  | CRYOTIMER_IFC       | (R)W1 | Interrupt Flag Clear Register |
| 0x01C  | CRYOTIMER_IEN       | RW    | Interrupt Enable Register     |

## 23.5 Register Description

### 23.5.1 CRYOTIMER\_CTRL - Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |       |   |        |   |          |   |    |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|-------|---|--------|---|----------|---|----|---|
| 0x000         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7     | 6 | 5      | 4 | 3        | 2 | 1  | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x0   |   | 0x0    |   | 0        |   | 0  |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RW    |   | RW     |   | RW       |   | RW |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | PRESC |   | OSCSEL |   | DEBUGRUN |   | EN |   |

| Bit  | Name            | Reset   | Access | Description  |
|------|-----------------|---|--------|--|
| 31:8 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 7:5  | PRESC           | 0x0   | RW     | <b>Prescaler Setting</b><br>These bits select the prescaling factor.   |
|      | Value           | Mode  |        | Description  |
|      | 0               | DIV1  |        | LF Oscillator frequency undivided  |
|      | 1               | DIV2  |        | LF Oscillator frequency divided by 2   |
|      | 2               | DIV4  |        | LF Oscillator frequency divided by 4   |
|      | 3               | DIV8  |        | LF Oscillator frequency divided by 8   |
|      | 4               | DIV16   |        | LF Oscillator frequency divided by 16  |
|      | 5               | DIV32   |        | LF Oscillator frequency divided by 32  |
|      | 6               | DIV64   |        | LF Oscillator frequency divided by 64  |
|      | 7               | DIV128  |        | LF Oscillator frequency divided by 128   |
| 4:2  | OSCSEL          | 0x0   | RW     | <b>Select Low Frequency Oscillator</b><br>These bits select the low frequency oscillator for the CRYOTIMER operation. This field should be set after the oscillator to be selected is ready. |
|      | Value           | Mode  |        | Description  |
|      | 0               | DISABLED  |        | Output is driven low   |
|      | 1               | LFRCO   |        | Select Low Frequency RC Oscillator   |
|      | 2               | LFXO  |        | Select Low Frequency Crystal Oscillator  |
|      | 3               | ULFRCO  |        | Select Ultra Low Frequency RC Oscillator   |
| 1    | DEBUGRUN        | 0   | RW     | <b>Debug Mode Run Enable</b><br>Set this bit to enable CRYOTIMER to run in debug mode.   |
| 0    | EN              | 0   | RW     | <b>Enable CRYOTIMER</b><br>Set this bit to start the CRYOTIMER. Clear this bit to reset the CRYOTIMER. This bit should be set after the oscillator to be selected is ready.                  |

### 23.5.2 CRYOTIMER\_PERIODSEL - Interrupt Duration

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x004         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | PERIODSEL    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name     | Reset  | Access | Description |
|------|----------|--|--------|-------------|
| 31:6 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |             |

| Bit   | Name      | Reset  | Access | Description  |
|-------|-----------|--|--------|--|
| 5:0   | PERIODSEL | 0x20   | RW     | <b>Interrupts/Wakeup Events Period Setting</b><br>Defines the duration between the Interrupts/Wakeup events based on the pre-scaled clock. |
| Value |           | Description                                      |        |  |
| 0     |           | Wakeup event after every Pre-scaled clock cycle. |        |  |
| 1     |           | Wakeup event after 2 Pre-scaled clock cycles.    |        |  |
| 2     |           | Wakeup event after 4 Pre-scaled clock cycles.    |        |  |
| 3     |           | Wakeup event after 8 Pre-scaled clock cycles.    |        |  |
| 4     |           | Wakeup event after 16 Pre-scaled clock cycles.   |        |  |
| 5     |           | Wakeup event after 32 Pre-scaled clock cycles.   |        |  |
| 6     |           | Wakeup event after 64 Pre-scaled clock cycles.   |        |  |
| 7     |           | Wakeup event after 128 Pre-scaled clock cycles.  |        |  |
| 8     |           | Wakeup event after 256 Pre-scaled clock cycles.  |        |  |
| 9     |           | Wakeup event after 512 Pre-scaled clock cycles.  |        |  |
| 10    |           | Wakeup event after 1k Pre-scaled clock cycles.   |        |  |
| 11    |           | Wakeup event after 2k Pre-scaled clock cycles.   |        |  |
| 12    |           | Wakeup event after 4k Pre-scaled clock cycles.   |        |  |
| 13    |           | Wakeup event after 8k Pre-scaled clock cycles.   |        |  |
| 14    |           | Wakeup event after 16k Pre-scaled clock cycles.  |        |  |
| 15    |           | Wakeup event after 32k Pre-scaled clock cycles.  |        |  |
| 16    |           | Wakeup event after 64k Pre-scaled clock cycles.  |        |  |
| 17    |           | Wakeup event after 128k Pre-scaled clock cycles. |        |  |
| 18    |           | Wakeup event after 256k Pre-scaled clock cycles. |        |  |
| 19    |           | Wakeup event after 512k Pre-scaled clock cycles. |        |  |
| 20    |           | Wakeup event after 1M Pre-scaled clock cycles.   |        |  |
| 21    |           | Wakeup event after 2M Pre-scaled clock cycles.   |        |  |
| 22    |           | Wakeup event after 4M Pre-scaled clock cycles.   |        |  |

| Bit | Name | Reset | Access | Description                                       |
|-----|------|-------|--------|---|
| 23  |      |       |        | Wakeup event after 8M Pre-scaled clock cycles.    |
| 24  |      |       |        | Wakeup event after 16M Pre-scaled clock cycles.   |
| 25  |      |       |        | Wakeup event after 32M Pre-scaled clock cycles.   |
| 26  |      |       |        | Wakeup event after 64M Pre-scaled clock cycles.   |
| 27  |      |       |        | Wakeup event after 128M Pre-scaled clock cycles.  |
| 28  |      |       |        | Wakeup event after 256M Pre-scaled clock cycles.  |
| 29  |      |       |        | Wakeup event after 512M Pre-scaled clock cycles.  |
| 30  |      |       |        | Wakeup event after 1024M Pre-scaled clock cycles. |
| 31  |      |       |        | Wakeup event after 2048M Pre-scaled clock cycles. |
| 32  |      |       |        | Wakeup event after 4096M Pre-scaled clock cycles. |

### 23.5.3 CRYOTIMER\_CNT - Counter Value

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x008         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0x00000000   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> | R            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | CNT          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit                                | Name | Reset      | Access | Description          |
|------------------------------------|------|------------|--------|----------------------|
| 31:0                               | CNT  | 0x00000000 | R      | <b>Counter Value</b> |
| These bits hold the Counter value. |      |            |        |                      |

### 23.5.4 CRYOTIMER\_EM4WUEN - Wake Up Enable

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x00C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | EM4WU        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name            | Reset   | Access | Description               |
|--|-----------------|---|--------|---------------------------|
| 31:1   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |                           |
| 0  | EM4WU           | 0   | RW     | <b>EM4 Wake-up Enable</b> |
| Write 1 to enable wake-up request, write 0 to disable wake-up request. |                 |   |        |                           |

### 23.5.5 CRYOTIMER\_IF - Interrupt Flag Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |        |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|--------|
| 0x010         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0      |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0      |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | R      |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | PERIOD |

| Bit  | Name     | Reset   | Access | Description  |
|------|----------|---|--------|--|
| 31:1 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 0    | PERIOD   | 0   | R      | <b>Wakeup Event/Interrupt</b><br>Set when the Wakeup event/Interrupt occurs. |

### 23.5.6 CRYOTIMER\_IFS - Interrupt Flag Set Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |        |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|--------|
| 0x014         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0      |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0      |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | W1     |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | PERIOD |

| Bit  | Name     | Reset   | Access | Description  |
|------|----------|---|--------|--|
| 31:1 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 0    | PERIOD   | 0   | W1     | <b>Set PERIOD Interrupt Flag</b><br>Write 1 to set the PERIOD interrupt flag |

## 23.5.7 CRYOTIMER\_IFC - Interrupt Flag Clear Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |        |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|--------|
| 0x018         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0      |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |        |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |        |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |        |
|               |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | PERIOD |
|               |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0      |
|               |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | (R)W1  |
|               |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0      |

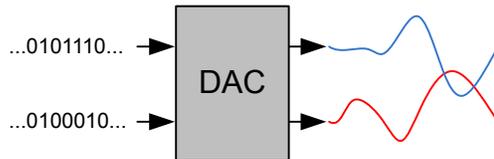
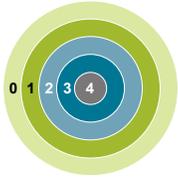
| Bit  | Name  | Reset  | Access | Description                        |
|------|---|--|--------|------------------------------------|
| 31:1 | Reserved  | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |                                    |
| 0    | PERIOD  | 0  | (R)W1  | <b>Clear PERIOD Interrupt Flag</b> |
|      | Write 1 to clear the PERIOD interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |  |        |                                    |

## 23.5.8 CRYOTIMER\_IEN - Interrupt Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |        |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|--------|
| 0x01C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0      |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |        |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |        |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |        |
|               |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | PERIOD |
|               |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0      |
|               |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | RW     |
|               |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0      |

| Bit  | Name                                | Reset  | Access | Description                    |
|------|-------------------------------------|--|--------|--------------------------------|
| 31:1 | Reserved                            | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |                                |
| 0    | PERIOD                              | 0  | RW     | <b>PERIOD Interrupt Enable</b> |
|      | Enable/disable the PERIOD interrupt |  |        |                                |

## 24. VDAC - Digital to Analog Converter



### Quick Facts

#### What?

The VDAC is designed for low energy consumption, but can also provide very good performance. It can convert digital values to analog signals at up to 500 kilo samples/second with 12-bit accuracy.

#### Why?

The VDAC can be used to generate accurate analog signals for sound, sensors and other applications, using only a limited amount of energy.

#### How?

The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available down to Energy Mode 3.

### 24.1 Introduction

The Voltage Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is fully differential rail-to-rail, with 12-bit resolution. It has two single ended output buffers which can be combined into one differential output. The VDAC may be used for a number of different applications such as sensor interfaces or sound output.

## 24.2 Features

- 500 ksamples/s operation
- Two single ended output channels
  - Can be combined into one differential output
- Integrated prescaler with division factor selectable between 1-128
- Selectable voltage reference
  - Internal low noise 2.5 V
  - Internal low noise 1.25 V
  - Internal low power 2.5 V
  - Internal low power 1.25 V
  - AVDD
  - External Pin Reference
- Conversion triggers
  - Data write
  - PRS input
  - Refresh timer
  - LESENSE
- Automatic refresh timer
  - Selection from 16-64 DAC\_CLK cycles
  - Individual refresh enable for each channel
- Interrupt generation on buffer empty or finished conversion
  - Separate interrupt flags for each channel
- PRS output pulse on finished conversion
  - Separate line for each channel
- DMA request on buffer empty
  - Separate request for each channel
- Support for offset and gain calibration
- Output to dedicated pins or APORT bus
- Internal connections to ADC and ACMP
- Sine generation mode
- Asynchronous clocking mode

## 24.3 Functional Description

An overview of the VDAC module is shown in the figure below.

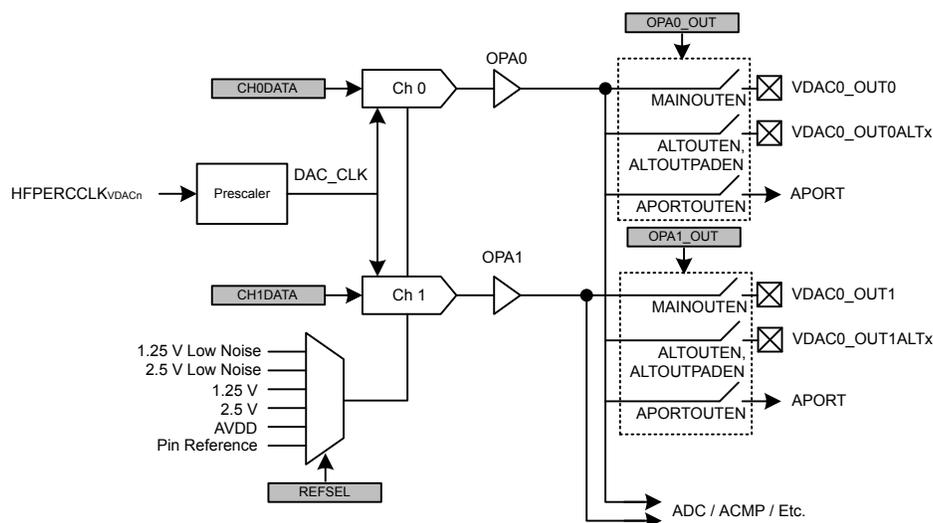


Figure 24.1. VDAC Overview

### 24.3.1 Power Supply

The VDAC module power ( $V_{OPA}$ ) is derived from the AVDD supply pin.

### 24.3.2 I/O Pin Considerations

The maximum usable analog signal that can be seen on external VDAC outputs depends on several factors: whether the signal is routed through the APORT, whether overvoltage is enabled, and on the IOVDD/AVDD supply voltages, as shown in the [Table 24.1 Maximum Usable IO Voltage on page 796](#) table.

Table 24.1. Maximum Usable IO Voltage

| VDAC Pin                  | Maximum IO Voltage (APORT USED and OVT Enabled/ Disabled) | Maximum IO Voltage (APORT UNUSED, OVT Enabled) | Maximum IO Voltage (APORT UN-USED, OVT Disabled) |
|---------------------------|---|--|--|
| VDAC External VREF Inputs | N/A   | MIN(AVDD, IOVDD)                               | MIN(AVDD, IOVDD)                                 |
| VDAC Outputs              | MIN(AVDD, IOVDD)  | MIN(AVDD, IOVDD + 2 V)                         | MIN(AVDD, IOVDD)                                 |

### 24.3.3 Enabling and Disabling a Channel

A VDAC channel is enabled by writing 1 to the CHxEN and disabled by writing 1 to CHxDIS in VDACCn\_CMD. The channel enabled status can be read by polling the CHxENS bit in VDACCn\_STATUS. This bit will go high immediately following a write to CHxEN. After disabling a channel the CHxENS bit will stay high until the VDAC channel is completely disabled.

Software should configure the VDAC before enabling a channel. Software *must not* write to any of the following registers while *either* CH0ENS or CH1ENS are set:

- VDACCn\_CTRL
- VDACCn\_CHxCTRL
- VDACCn\_OPAXTIMER

A VDAC channel will not begin driving its output before it is enabled *and* has received a conversion trigger, see [24.3.4.3 Conversion Trigger](#). After a channel is enabled it will listen for trigger sources specified in TRIGMODE in VDACCn\_CHxCTRL. If TRIGMODE is set to SW, SWPRS or SWREFRESH and a value was written to CHxDATA or COMBDATA before enabling the channel a conversion will start immediately when the channel is enabled. When disabling a channel any pending triggers are flushed.

### 24.3.4 Conversions

The VDAC consists of two channels (channel 0 and 1) with separate 12-bit data registers (VDACn\_CH0DATA and VDACn\_CH1DATA). These can be used to produce two independent single ended outputs or the channel 0 register can be used to drive both outputs in differential mode. The VDAC supports two conversion modes: continuous and sample/off.

#### 24.3.4.1 Continuous Mode

In continuous mode the VDAC channels will drive their outputs continuously with the data in the VDACn\_CHxDATA registers. A channel is configured in continuous mode by programming the CONVMODE bitfield in VDACn\_CHxCTRL to CONTINUOUS. This mode will maintain the output voltage and no manual refresh is needed.

In continuous mode the SETTLETIME field in VDACn\_OPAXTIMER should be programmed to zero to achieve the maximum update rate.

#### 24.3.4.2 Sample/Off Mode

In sample/off mode the VDAC will only drive the output for a limited time per conversion. A channel is configured in sample/off mode by programming the CONVMODE bitfield in VDACn\_CHxCTRL to SAMPLEOFF. How long the channel should drive the output can be controlled by programming the SETTLETIME field in the VDACn\_OPAXTIMER register. The VDAC will drive the output for SETTLETIME  $f_{DAC\_CLK}$  cycles before tristating the output again (and therefore if SETTLETIME is set to zero, the output will never be driven when using sample/off mode).

#### 24.3.4.3 Conversion Trigger

Conversions can only be done while a channel is enabled, see [24.3.3 Enabling and Disabling a Channel](#).

If TRIGMODE is programmed to SW, SWPRS or SWREFRESH a conversion can be started by writing to the VDACn\_CHxDATA register. The data registers are also mapped to a combined data register, VDACn\_COMBDATA, where the data values for both channels can be written simultaneously. Writing to this register will trigger all enabled channels.

If TRIGMODE is programmed to PRS or SWPRS, a conversion can be started by an incoming pulse on the PRS channel selected in PRSSEL in VDACn\_CHxCTRL. The PRSASYNC bit in VDACn\_CHxCTRL determines if the VDAC expects a PRS pulse coming from a synchronous or asynchronous PRS producer.

If TRIGMODE is programmed to REFRESH or SWREFRESH a conversion will start on an overflow of the internal refresh timer. See [24.3.10 Refresh Timer](#).

If TRIGMODE is programmed to LESENSE a conversion will start when the LESENSE block sends a request. This setting needs to be selected whenever the channel is under LESENE control.

#### 24.3.4.4 PRS Triggers

PRS triggers can be used to set a constant sample frequency, for instance by using a TIMER. In order to get a jitter-free sample rate, set DACCLKMODE to SYNC, set the CH0PRESCRST bit and clear the PRSASYNC bit. Note that this is only possible for channel 0.

The PRSASYNC bit tells whether the VDAC expects a synchronous PRS producer or not. When this bit is cleared, the PRS pulse must come from a synchronous producer and HPPERCLK must be running (this clock is turned off in EM2 and below). When PRSASYNC is set, the corresponding PRS channels should also be configured as asynchronous (see the PRS chapter).

When either DACCLKMODE is set to ASYNC or the PRSASYNC bit is set, the sample frequency cannot be guaranteed to be jitter-free with respect to the PRS pulses.

The PRS frequency should never be higher than 0.5 MHz (the fastest possible sample rate). In addition the PRS frequency should not be higher than  $f_{HPPERCLK}/12$  (in synchronous mode). If the PRS frequency is set too high, some PRS pulses will be dropped and the output can jitter.

### 24.3.5 Reference Selection

These voltage references are available and are selected by programming the REFSEL field in VDACn\_CTRL.

- Internal 1.25 V Low Noise Bandgap Reference
- Internal 2.5 V Low Noise Bandgap Reference
- Internal 1.25 V Low Power Bandgap Reference
- Internal 2.5 V Low Power Bandgap Reference
- AVDD

- External Pin

### 24.3.6 Warmup Time and Initial Conversion

When a channel is first enabled it needs to warm up. This is performed automatically during the first conversion. The time required to warm up depends on the programmed DRIVESTRENGTH field in VDACn\_OPAX\_CTRL. In [Table 24.2 VDAC Warmup Time on page 798](#) the minimum WARMUPTIME field for each drive strength is specified. Software is responsible for programming the correct value to WARMUPTIME before enabling a channel. If the time is programmed too short, an undefined voltage may be output until the VDAC settles.

The CHxWARM bits in VDACn\_STATUS are set when the warmup period has completed.

A consequence of the warmup period is that in continuous mode, the first conversion might take longer than the following conversions. In order to make sure all samples have the same timing, perform a dummy conversion to make the VDAC settle to a known voltage first.

**Table 24.2. VDAC Warmup Time**

| DRIVESTRENGTH | WARMUPTIME  |
|---------------|-------------|
| 0             | 100 $\mu$ s |
| 1             | 85 $\mu$ s  |
| 2             | 8 $\mu$ s   |
| 3             | 8 $\mu$ s   |

### 24.3.7 Analog Output

The output selection for each VDAC channel is configured in the VDACn\_OPAX\_OUT registers. Each VDAC channel has its own main output pin, VDACn\_OUTx, that can be enabled with MAINOUTEN. In addition, several alternate outputs can be selected. These are enabled by first setting ALTOUTEN and then setting the corresponding bit(s) in ALTOUTPADEN. The VDAC output can also be routed to APORT by setting APORTOUTEN and configuring the APORTOUTSEL field to select the desired APORT.

The VDAC outputs also have direct internal connections to ADCs and ACMPs. These outputs are always enabled and can be selected by configuring the input selection for the ADC/ACMP.

In sample/off mode the VDAC will only drive the output for the duration programmed in SETTLETIME (in VDACn\_OPAX\_TIMER register) for each incoming conversion trigger. In continuous mode the VDAC will continue to drive the output until the channel is disabled. However, note that also in this mode a conversion trigger is needed before the output is enabled. See [24.3.3 Enabling and Disabling a Channel](#) and [24.3.4.3 Conversion Trigger](#).

### 24.3.8 Output Mode

The two VDAC channels can act as two separate single ended channels or be combined into one differential channel. This is selected through the DIFF bit in VDACn\_CTRL.

#### 24.3.8.1 Single Ended Output

When operating in single ended mode, the channel 0 output is on VDACn\_OUT0 and the channel 1 output is on VDACn\_OUT1. The output voltage can be calculated using [Figure 24.2 VDAC Single Ended Output Voltage on page 798](#)

$$V_{OUT} = V_{VDACn\_OUTx} - V_{SS} = V_{ref} \times CHxDATA/4095$$

**Figure 24.2. VDAC Single Ended Output Voltage**

where CHxDATA is a 12-bit unsigned integer.

#### 24.3.8.2 Differential Output

When operating in differential mode, both VDAC outputs are used. The differential conversion uses VDACn\_CH0DATA as source. The positive output is on VDACn\_OUT1 and the negative output is on VDACn\_OUT0. Since the output can be negative, it is expected that

the data is written in 2's complement form with the MSB of the 12-bit value being the signed bit. The output voltage can be calculated using [Figure 24.3 VDAC Differential Output Voltage on page 799](#):

$$V_{OUT} = V_{VDACn\_OUT1} - V_{VDACn\_OUT0} = V_{ref} \times CH0DATA/2047$$

**Figure 24.3. VDAC Differential Output Voltage**

where CH0DATA is a 12-bit signed integer. The common mode voltage is  $V_{ref}/2$ .

When using differential mode, the user must make sure that both channels are set up identically. I.e. VDACn\_CH0CTRL and VDACn\_CH1CTRL must be programmed to identical values (with the exception that the PRSSEL bitfield is allowed to be programmed differently for usage together with the OUTENPRS feature). Similarly the user must program VDACn\_OPA0TIMER and VDACn\_OPA1TIMER to identical values.

### 24.3.9 Async Mode

The VDAC is default clocked from HFPERCLK, which is automatically turned off in EM2/3. In order to allow VDAC operation in EM2/3 an internal oscillator can be selected for the VDAC by setting the DACCLKMODE bitfield in VDACn\_CTRL to ASYNC. Before entering EM2/3 software must make sure the channel is enabled first by polling CHxENS in VDACn\_STATUS. Entering EM2/3 with an enabled VDAC channel while DACCLKMODE is set to SYNC is a programming error and will lead to EM23ERRIF getting set to 1.

In asynchronous mode both VDAC channels are not necessarily triggered synchronous to each other and therefore the user should not assume that e.g. PRS, refresh or VDACn\_COMBDATA based conversion triggers are observed by both channels at the same time. In differential mode both channels will operate in lock step, even while using the asynchronous clocking mode.

### 24.3.10 Refresh Timer

The VDAC includes an internal refresh timer. The refresh timer is automatically started if a channel selects either REFRESH or SWREFRESH for TRIGMODE and the channel is enabled. The refresh timer will count the number of  $f_{DAC\_CLK}$  cycles programmed in REFRESHPERIOD before wrapping and generating a conversion trigger.

### 24.3.11 Clock Prescaling

The VDAC has an internal clock prescaler, which can divide the input clock by any factor between 1 and 128, by setting the PRESC field in VDACn\_CTRL. The resulting DAC\_CLK is used by the converter core and the frequency is given by [Figure 24.4 VDAC Clock Prescaling on page 799](#) :

$$f_{DAC\_CLK} = f_{IN\_CLK} / (PRESC + 1)$$

**Figure 24.4. VDAC Clock Prescaling**

where  $f_{IN\_CLK}$  is the input clock frequency. The  $f_{DAC\_CLK}$  must be programmed to be at most 1 MHz. When the DACCLKMODE is set to SYNC, the input clock frequency is  $f_{HFPERCLK}$ . When DACCLKMODE is set to ASYNC, an internal 12Mhz oscillator is used. In this mode it is required that the PRESC field be program to 11 or higher.

The prescaler runs continuously when either of the channels are enabled. When running with a prescaler setting higher than 0, there will be an unpredictable delay from the time the conversion was triggered to the time the actual conversion takes place. This is because the conversions are controlled by the prescaled clock and the conversion can arrive at any time during a prescaled clock (DAC\_CLK) period. A second reason for unpredictable delay between a trigger and the associated conversion is that the activity on one channel can impact whether the VDAC reference is warm or not and therefore it can impact whether warmup is required when using the other channel. The uncertainty related to the clock prescaler can be addressed by using CHOPRESCRST. If the CHOPRESCRST bit in VDACn\_CTRL is set, the prescaler will be reset every time a conversion is triggered on channel 0. This leads to a predictable latency between channel 0 trigger and conversion (assuming the warmup sequence is deterministic as well). If channel 0 is used in continuous mode, the warmup sequence will only apply to its first conversion and software can use the CH0WARM status bit to determine if the VDAC has warmed up.

### 24.3.12 High Speed

The VDAC is able to do conversions up to 400 ksamples/s. In order to reach the maximum conversion rate it is recommended to configure the VDAC in the following way:

1. Make  $f_{DAC\_CLK}$  1 Mhz
2. Set TRIGMODE to SW
3. Program SETTLETIME in OPAx\_TIMER to 0

4. Set up a DMA transfer from a buffer in RAM to CHxDATA
5. Set CONVMODE to CONTINUOUS

### 24.3.13 Sine Generation Mode

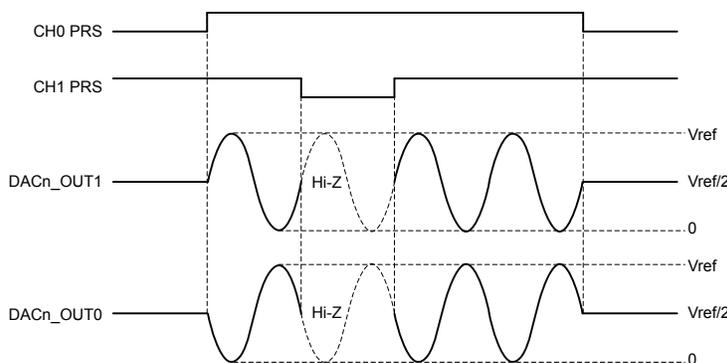
The VDAC contains an automatic sine-generation mode, which is enabled by setting the SINEMODE bit in VDACn\_CTRL. In this mode, the VDAC data is overridden with a conversion data taken from a sine lookup table. The sine signal is controlled by the PRS line selected by CH0PRSEL in VDACn\_CH0CTRL. When the line is high, a sine wave will be produced. Each period, starting at 0 degrees, is made up of 16 samples and the frequency is given by [Figure 24.5 VDAC Sine Generation on page 800](#). In case OUTENPRS equals 1, lowering the PRS line selected by CH0PRSEL will reset the sine output to 0 degrees resulting in a voltage of  $V_{ref}/2$  on the output channel. In case OUTENPRS equals 0, lowering the PRS line selected by CH0PRSEL will stop progress of the sine wave at the sample currently being output (and the sine will therefore not be reset to 0 degrees when raising the PRS line again).

$$f_{\text{sine}} = f_{\text{HFPERCLK}} / 32 \times (\text{PRESC} + 1)$$

**Figure 24.5. VDAC Sine Generation**

Sine mode is supported only for the fastest configuration of the VDAC in continuous mode. Therefore the CONVMODE bitfield needs to be set to CONTINUOUS and the SETTLETIME bitfield in VDACn\_OPAXTIMER need to be programmed to zero for the used channel(s) in order to use sine generation mode. The TRIGMODE bitfield needs to be programmed to PRS for any channel used for sine generation mode. The other trigger modes are not supported.

The SINE wave will be output on channel 0 and therefore requires that this channel is enabled by writing 1 to CH0EN in the VDACn\_CMD register. If DIFF is set in VDACn\_CTRL, the sine wave will be output on both channels, but inverted. Note that when OUTENPRS in VDACn\_CTRL is set, the sine output will be reset to 0 degrees when the PRS line selected by CH1PRSEL is low.



**Figure 24.6. VDAC Sine Mode**

### 24.3.14 Interrupt Flags

The VDAC has several interrupt flags, indicating state transitions and error conditions.

In addition to the VDAC interrupt flags the VDAC registers contain interrupt flags for the OPAMP modules. See The OPAMP chapter for more information on these flags.

#### 24.3.14.1 Conversion Done

The Conversion Done (CHxCD) interrupt flags are set when a conversion is complete. The flags are set after a channel has driven the output with the new code for the time programmed in SETTLETIME in VDACn\_OPAXTIMER.

#### 24.3.14.2 Buffer Level

The Buffer Level (CHxBL) interrupt flags are set when there is space available in CHxDATA. These flags are initially set, get cleared when CHxDATA is written and set again when the value is used for a conversion.

### 24.3.14.3 Overflow/Underflow

If CHxDATA is written to while CHxBL is cleared, the channel overflow flag (CHxOF) will be set. If a new conversion is triggered (e.g. via PRS) before data is written to CHxDATA (CHxDATA is empty) the channel underflow flag (CHxUF) will be set.

### 24.3.14.4 EM2/3 Sleep Error

The VDAC can only operate in EM2/3 when DACCLKMODE is set to ASYNC. If EM2 or EM3 is entered while a channel is enabled and DACCLKMODE is set to SYNC the EM23ERRIF flag will be set.

### 24.3.15 PRS Outputs

The VDAC has two PRS outputs which will carry a one cycle (HFPERCLK) high pulse when the corresponding channel has finished a conversion. Only available when DACCLKMODE is set to SYNC.

### 24.3.16 DMA Request

Each channel sends a DMA request when there is space in the channel's data register (VDACn\_CHxDATA). These registers are initially empty and also become empty every time a conversion is triggered. The request is cleared when VDACn\_CHxDATA is written.

### 24.3.17 LESENSE Trigger Mode

The VDAC can be controlled by LESENSE by programming the TRIGMODE field in VDACn\_CHxCTRL to LESENSE. In LESENSE mode the conversion data can come from either VDACn\_CHxDATA registers or LESENSE registers, depending on the LESENSE configuration. The trigger events are also controlled by the LESENSE state machine. See the LESENSE chapter for more information.

### 24.3.18 Opamps

The VDAC includes a set of highly configurable opamps that can be accessed with the VDAC registers. OPA0 and OPA1 is used for the output stages of the two VDAC channels, but can be used as standalone opamps if the VDAC channels are not in use. Opamps with higher numbers are completely standalone. For a detailed description see the OPAMP chapter.

### 24.3.19 Calibration

The VDAC contains a calibration register, VDACn\_CAL, where calibration values for both offset and gain correction can be written. The required (gain) calibration values depend on the chosen reference and on whether the main or alternative VDAC output is used. The Device Information page provides the required trim values depending on reference choice and output selection in the DEVINFO\_VDACnMAINCAL, DEVINFO\_VDACnALTCAL, and DEVINFO\_VDACnCH1CAL locations.

The OPAMPs contain a calibration register, VDACn\_OPAx\_CAL, where calibration values for both offset and gain correction can be written. The required calibration settings depend on the chosen DRIVESTRENGTH. The required calibration values can be found in the Device Information pages. For a given OPAMP x, the calibration settings for DRIVESTRENGTH n can be found in DEVINFO\_OPAX-CALn.

#### 24.3.19.1 Channel 1 Calibration

For channel 1, the factory calibration values are only accurate for the main output. When using the alternative outputs or APORT, the error on the output may be larger than the data sheet values (even when loading values from DEVINFO\_VDACn\_ALTCAL). To get accurate output from channel 1, either use the main output or perform manual calibration.

#### 24.3.19.2 Manual Calibration

To manually calibrate the VDAC:

1. Enable CH0 and CH1 in their desired modes
2. Set both channel outputs to 80% of full-scale by setting VDACn\_CHxDATA = 0xCCC
3. Measure CH0 output and sweep VDACn\_CAL.GAINERRTRIM until the smallest calibration error is found
4. Measure CH1 output and sweep VDACn\_CAL.GAINERRTRIMCH1 until the smallest calibration error is found

The calibration error is given by

$$e = \text{abs}(V_{\text{out}}/(V_{\text{REF}} * 0.8) - 1)$$

**Figure 24.7. Calibration Error**

where  $V_{\text{out}}$  is the measured voltage at the pin and  $V_{\text{REF}}$  is the reference voltage.

Note that even if only CH1 is going to be used, the full calibration procedure should be followed. It is permissible to skip CH1 calibration if only CH0 is used. The following parameters influence the calibration. A change in any of these might require a re-calibration:

- VDACn\_CTRL.REFSEL
- VDACn\_OPAX\_OUT.MAINOUTEN
- VDACn\_OPAX\_OUT.ALTOUTEN
- VDACn\_OPAX\_CTRL.DRIVESTRENGTH

#### **24.3.20 Warmup Mode**

If the WARMUPMODE field in VDACn\_CTRL is set to KEEPINSTANDBY, the VDAC keeps internal bias currents running between conversions. It does not reduce the startup time, but it can help reduce noise from the VDAC to other analog peripherals, like the ADC or ACMP.

## 24.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name                     | Type  | Description  |
|--------|--------------------------|-------|--|
| 0x000  | VDACn_CTRL               | RW    | Control Register                                     |
| 0x004  | VDACn_STATUS             | R     | Status Register                                      |
| 0x008  | VDACn_CH0CTRL            | RW    | Channel 0 Control Register                           |
| 0x00C  | VDACn_CH1CTRL            | RW    | Channel 1 Control Register                           |
| 0x010  | VDACn_CMD                | W1    | Command Register                                     |
| 0x014  | VDACn_IF                 | R     | Interrupt Flag Register                              |
| 0x018  | VDACn_IFS                | W1    | Interrupt Flag Set Register                          |
| 0x01C  | VDACn_IFC                | (R)W1 | Interrupt Flag Clear Register                        |
| 0x020  | VDACn_IEN                | RW    | Interrupt Enable Register                            |
| 0x024  | VDACn_CH0DATA            | RWH   | Channel 0 Data Register                              |
| 0x028  | VDACn_CH1DATA            | RWH   | Channel 1 Data Register                              |
| 0x02C  | VDACn_COMBDATA           | W     | Combined Data Register                               |
| 0x030  | VDACn_CAL                | RW    | Calibration Register                                 |
| 0x0A0  | VDACn_OPA0_APORTREQ      | R     | Operational Amplifier APORT Request Status Register  |
| 0x0A4  | VDACn_OPA0_APORTCONFLICT | R     | Operational Amplifier APORT Conflict Status Register |
| 0x0A8  | VDACn_OPA0_CTRL          | RW    | Operational Amplifier Control Register               |
| 0x0AC  | VDACn_OPA0_TIMER         | RW    | Operational Amplifier Timer Control Register         |
| 0x0B0  | VDACn_OPA0_MUX           | RW    | Operational Amplifier Mux Configuration Register     |
| 0x0B4  | VDACn_OPA0_OUT           | RW    | Operational Amplifier Output Configuration Register  |
| 0x0B8  | VDACn_OPA0_CAL           | RW    | Operational Amplifier Calibration Register           |
| 0x0C0  | VDACn_OPA1_APORTREQ      | R     | Operational Amplifier APORT Request Status Register  |
| 0x0C4  | VDACn_OPA1_APORTCONFLICT | R     | Operational Amplifier APORT Conflict Status Register |
| 0x0C8  | VDACn_OPA1_CTRL          | RW    | Operational Amplifier Control Register               |
| 0x0CC  | VDACn_OPA1_TIMER         | RW    | Operational Amplifier Timer Control Register         |
| 0x0D0  | VDACn_OPA1_MUX           | RW    | Operational Amplifier Mux Configuration Register     |
| 0x0D4  | VDACn_OPA1_OUT           | RW    | Operational Amplifier Output Configuration Register  |
| 0x0D8  | VDACn_OPA1_CAL           | RW    | Operational Amplifier Calibration Register           |
| 0x0E0  | VDACn_OPA2_APORTREQ      | R     | Operational Amplifier APORT Request Status Register  |
| 0x0E4  | VDACn_OPA2_APORTCONFLICT | R     | Operational Amplifier APORT Conflict Status Register |
| 0x0E8  | VDACn_OPA2_CTRL          | RW    | Operational Amplifier Control Register               |
| 0x0EC  | VDACn_OPA2_TIMER         | RW    | Operational Amplifier Timer Control Register         |
| 0x0F0  | VDACn_OPA2_MUX           | RW    | Operational Amplifier Mux Configuration Register     |
| 0x0F4  | VDACn_OPA2_OUT           | RW    | Operational Amplifier Output Configuration Register  |
| 0x0F8  | VDACn_OPA2_CAL           | RW    | Operational Amplifier Calibration Register           |

## 24.5 Register Description

### 24.5.1 VDACn\_CTRL - Control Register

| Offset        | Bit Position |    |    |            |    |    |               |    |    |    |    |    |       |    |    |    |    |    |    |    |    |    |     |        |   |   |             |          |          |    |   |   |      |    |
|---------------|--------------|----|----|------------|----|----|---------------|----|----|----|----|----|-------|----|----|----|----|----|----|----|----|----|-----|--------|---|---|-------------|----------|----------|----|---|---|------|----|
| 0x000         | 31           | 30 | 29 | 28         | 27 | 26 | 25            | 24 | 23 | 22 | 21 | 20 | 19    | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9   | 8      | 7 | 6 | 5           | 4        | 3        | 2  | 1 | 0 |      |    |
| <b>Reset</b>  | 0            |    |    | 0          |    |    | 0x0           |    |    |    |    |    | 0x00  |    |    |    |    |    |    |    |    |    | 0x0 |        |   |   | 0           | 0        | 0        |    |   |   | 0    |    |
| <b>Access</b> | RW           |    |    | RW         |    |    | RW            |    |    |    |    |    | RW    |    |    |    |    |    |    |    |    |    |     | RW     |   |   |             | RW       | RW       | RW |   |   |      | RW |
| <b>Name</b>   | DACCLKMODE   |    |    | WARMUPMODE |    |    | REFRESHPERIOD |    |    |    |    |    | PRESC |    |    |    |    |    |    |    |    |    |     | REFSEL |   |   | CH0PRESCRST | OUTENPRS | SINEMODE |    |   |   | DIFF |    |

| Bit   | Name            | Reset   | Access | Description   |       |      |             |   |         |  |   |               |   |   |          |   |
|-------|-----------------|---|--------|---|-------|------|-------------|---|---------|--|---|---------------|---|---|----------|---|
| 31    | DACCLKMODE      | 0   | RW     | <b>Clock Mode</b><br>Selects DAC clock source from synchronous or asynchronous - with respect to Peripheral Clock - clock source<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>SYNC</td> <td>Uses HPPERCLK to generate DAC_CLK, DAC will run with static settings in EM2 in this mode</td> </tr> <tr> <td>1</td> <td>ASYNC</td> <td>Uses internal VDAC oscillator to generate DAC_CLK. DAC will be available in EM2</td> </tr> </tbody> </table>  | Value | Mode | Description | 0 | SYNC    | Uses HPPERCLK to generate DAC_CLK, DAC will run with static settings in EM2 in this mode | 1 | ASYNC         | Uses internal VDAC oscillator to generate DAC_CLK. DAC will be available in EM2 |   |          |   |
| Value | Mode            | Description   |        |   |       |      |             |   |         |  |   |               |   |   |          |   |
| 0     | SYNC            | Uses HPPERCLK to generate DAC_CLK, DAC will run with static settings in EM2 in this mode  |        |   |       |      |             |   |         |  |   |               |   |   |          |   |
| 1     | ASYNC           | Uses internal VDAC oscillator to generate DAC_CLK. DAC will be available in EM2   |        |   |       |      |             |   |         |  |   |               |   |   |          |   |
| 30:29 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |      |             |   |         |  |   |               |   |   |          |   |
| 28    | WARMUPMODE      | 0   | RW     | <b>Warm-up Mode</b><br>Select Warm-up Mode for DAC<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>NORMAL</td> <td>DAC is shut off after each sample off conversion</td> </tr> <tr> <td>1</td> <td>KEEPINSTANDBY</td> <td>DAC is kept in standby mode between sample off conversions</td> </tr> </tbody> </table>   | Value | Mode | Description | 0 | NORMAL  | DAC is shut off after each sample off conversion   | 1 | KEEPINSTANDBY | DAC is kept in standby mode between sample off conversions                      |   |          |   |
| Value | Mode            | Description   |        |   |       |      |             |   |         |  |   |               |   |   |          |   |
| 0     | NORMAL          | DAC is shut off after each sample off conversion  |        |   |       |      |             |   |         |  |   |               |   |   |          |   |
| 1     | KEEPINSTANDBY   | DAC is kept in standby mode between sample off conversions  |        |   |       |      |             |   |         |  |   |               |   |   |          |   |
| 27:26 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |      |             |   |         |  |   |               |   |   |          |   |
| 25:24 | REFRESHPERIOD   | 0x0   | RW     | <b>Refresh Period</b><br>Select refresh counter period. A channel x will be refreshed with the period set in REFRESHPERIOD if the channel in VDACn_CHxCTRL has its TRIGMODE set to REFRESH or SWREFRESH.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>8CYCLES</td> <td>All channels with enabled refresh are refreshed every 8 DAC_CLK cycles</td> </tr> <tr> <td>1</td> <td>16CYCLES</td> <td>All channels with enabled refresh are refreshed every 16 DAC_CLK cycles</td> </tr> <tr> <td>2</td> <td>32CYCLES</td> <td>All channels with enabled refresh are refreshed every 32 DAC_CLK cycles</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | 8CYCLES | All channels with enabled refresh are refreshed every 8 DAC_CLK cycles                   | 1 | 16CYCLES      | All channels with enabled refresh are refreshed every 16 DAC_CLK cycles         | 2 | 32CYCLES | All channels with enabled refresh are refreshed every 32 DAC_CLK cycles |
| Value | Mode            | Description   |        |   |       |      |             |   |         |  |   |               |   |   |          |   |
| 0     | 8CYCLES         | All channels with enabled refresh are refreshed every 8 DAC_CLK cycles  |        |   |       |      |             |   |         |  |   |               |   |   |          |   |
| 1     | 16CYCLES        | All channels with enabled refresh are refreshed every 16 DAC_CLK cycles   |        |   |       |      |             |   |         |  |   |               |   |   |          |   |
| 2     | 32CYCLES        | All channels with enabled refresh are refreshed every 32 DAC_CLK cycles   |        |   |       |      |             |   |         |  |   |               |   |   |          |   |

| Bit   | Name            | Reset   | Access                                      | Description  |
|-------|-----------------|---|---|--|
|       | 3               | 64CYCLES  |   | All channels with enabled refresh are refreshed every 64 DAC_CLK cycles  |
| 23    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 22:16 | PRESC           | 0x00  | RW  | <b>Prescaler Setting for DAC Clock</b><br>Selected DAC clock source (as selected by DACCLKMODE) is prescaled by PRESC+1 to generated DAC clock (DAC_CLK) |
|       | Value           | Description   |   |  |
|       | PRESC           | Clock division factor of PRESC+1.   |   |  |
| 15:11 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 10:8  | REFSEL          | 0x0   | RW  | <b>Reference Selection</b><br>Select reference   |
|       | Value           | Mode  | Description                                 |  |
|       | 0               | 1V25LN  | Internal low noise 1.25 V bandgap reference |  |
|       | 1               | 2V5LN   | Internal low noise 2.5 V bandgap reference  |  |
|       | 2               | 1V25  | Internal 1.25 V bandgap reference           |  |
|       | 3               | 2V5   | Internal 2.5 V bandgap reference            |  |
|       | 4               | VDD   | AVDD reference                              |  |
|       | 6               | EXT   | External pin reference                      |  |
| 7     | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 6     | CH0PRESCRST     | 0   | RW  | <b>Channel 0 Start Reset Prescaler</b><br>Select if prescaler (determining DAC_CLK rate) is reset on channel 0 start.                                    |
|       | Value           | Description   |   |  |
|       | 0               | Prescaler not reset on channel 0 start  |   |  |
|       | 1               | Prescaler reset on channel 0 start  |   |  |
| 5     | OUTENPRS        | 0   | RW  | <b>PRS Controlled Output Enable</b><br>Enable PRS Control of DAC output enable.  |
|       | Value           | Description   |   |  |
|       | 0               | DAC output enable always on   |   |  |
|       | 1               | DAC output enable controlled by PRS signal selected for CH1   |   |  |
| 4     | SINEMODE        | 0   | RW  | <b>Sine Mode</b><br>Enable/disable sine mode.  |
|       | Value           | Description   |   |  |

| Bit | Name            | Reset   | Access | Description   |
|-----|-----------------|---|--------|---|
|     | 0               |   |        | Sine mode disabled. Sine reset to 0 degrees                           |
|     | 1               |   |        | Sine mode enabled   |
| 3:1 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 0   | DIFF            | 0   | RW     | <b>Differential Mode</b><br>Select single ended or differential mode. |
|     | Value           |   |        | Description   |
|     | 0               |   |        | Single ended output   |
|     | 1               |   |        | Differential output   |

## 24.5.2 VDACn\_STATUS - Status Register

| Offset | Bit Position |              |              |              |    |          |          |          |    |         |         |         |    |                   |                   |                   |    |    |    |    |    |    |   |   |   |   |         |         |       |       |        |        |
|--------|--------------|--------------|--------------|--------------|----|----------|----------|----------|----|---------|---------|---------|----|-------------------|-------------------|-------------------|----|----|----|----|----|----|---|---|---|---|---------|---------|-------|-------|--------|--------|
| 0x004  | 31           | 30           | 29           | 28           | 27 | 26       | 25       | 24       | 23 | 22      | 21      | 20      | 19 | 18                | 17                | 16                | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5       | 4       | 3     | 2     | 1      | 0      |
| Reset  |              | 0            | 0            | 0            |    | 0        | 0        | 0        |    | 0       | 0       | 0       |    | 0                 | 0                 | 0                 |    |    |    |    |    |    |   |   |   |   | 0       | 0       | 1     | 1     | 0      | 0      |
| Access |              | R            | R            | R            |    | R        | R        | R        |    | R       | R       | R       |    | R                 | R                 | R                 |    |    |    |    |    |    |   |   |   |   | R       | R       | R     | R     | R      | R      |
| Name   |              | OPA2OUTVALID | OPA1OUTVALID | OPA0OUTVALID |    | OPA2WARM | OPA1WARM | OPA0WARM |    | OPA2ENS | OPA1ENS | OPA0ENS |    | OPA2APORTCONFLICT | OPA1APORTCONFLICT | OPA0APORTCONFLICT |    |    |    |    |    |    |   |   |   |   | CH1WARM | CH0WARM | CH1BL | CH0BL | CH1ENS | CH0ENS |

| Bit | Name         | Reset  | Access | Description   |
|-----|--------------|--|--------|---|
| 31  | Reserved     | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 30  | OPA2OUTVALID | 0  | R      | <b>OPA2 Output Valid Status</b><br>OPA2 output is settled externally at the load. In PRS triggered mode this status flag is not used (and remains 0). |
| 29  | OPA1OUTVALID | 0  | R      | <b>OPA1 Output Valid Status</b><br>OPA1 output is settled externally at the load. In PRS triggered mode this status flag is not used (and remains 0). |
| 28  | OPA0OUTVALID | 0  | R      | <b>OPA0 Output Valid Status</b><br>OPA0 output is settled externally at the load. In PRS triggered mode this status flag is not used (and remains 0). |
| 27  | Reserved     | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 26  | OPA2WARM     | 0  | R      | <b>OPA2 Warm Status</b><br>OPA2 is warm and output is enabled. In PRS triggered mode this status flag is not used (and remains 0).                    |
| 25  | OPA1WARM     | 0  | R      | <b>OPA1 Warm Status</b><br>OPA1 is warm and output is enabled. In PRS triggered mode this status flag is not used (and remains 0).                    |
| 24  | OPA0WARM     | 0  | R      | <b>OPA0 Warm Status</b><br>OPA0 is warm and output is enabled. In PRS triggered mode this status flag is not used (and remains 0).                    |
| 23  | Reserved     | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 22  | OPA2ENS      | 0  | R      | <b>OPA2 Enabled Status</b><br>This bit is set when OPA2 is enabled  |
| 21  | OPA1ENS      | 0  | R      | <b>OPA1 Enabled Status</b><br>This bit is set when OPA1 is enabled  |
| 20  | OPA0ENS      | 0  | R      | <b>OPA0 Enabled Status</b><br>This bit is set when OPA0 is enabled  |
| 19  | Reserved     | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |

| Bit  | Name                   | Reset   | Access | Description   |
|------|------------------------|---|--------|---|
| 18   | OPA2APORTCON-<br>FLICT | 0   | R      | <b>OPA2 Bus Conflict Output</b><br><br>1 if any of the APORTs being requested by the OPA2 are also being requested by another peripheral. |
| 17   | OPA1APORTCON-<br>FLICT | 0   | R      | <b>OPA1 Bus Conflict Output</b><br><br>1 if any of the APORTs being requested by the OPA1 are also being requested by another peripheral. |
| 16   | OPA0APORTCON-<br>FLICT | 0   | R      | <b>OPA0 Bus Conflict Output</b><br><br>1 if any of the APORTs being requested by the OPA0 are also being requested by another peripheral. |
| 15:6 | <i>Reserved</i>        | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 5    | CH1WARM                | 0   | R      | <b>Channel 1 Warm</b><br><br>This bit is set when channel 1 is warm.  |
| 4    | CH0WARM                | 0   | R      | <b>Channel 0 Warm</b><br><br>This bit is set when channel 0 is warm.  |
| 3    | CH1BL                  | 1   | R      | <b>Channel 1 Buffer Level</b><br><br>This bit is set when there is space for new data in CH1DATA.   |
| 2    | CH0BL                  | 1   | R      | <b>Channel 0 Buffer Level</b><br><br>This bit is set when there is space for new data in CH0DATA.   |
| 1    | CH1ENS                 | 0   | R      | <b>Channel 1 Enabled Status</b><br><br>This bit is set when channel 1 is enabled.   |
| 0    | CH0ENS                 | 0   | R      | <b>Channel 0 Enabled Status</b><br><br>This bit is set when channel 0 is enabled.   |

### 24.5.3 VDACn\_CH0CTRL - Channel 0 Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |       |    |    |    |        |    |     |   |          |   |   |   |   |   |          |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|----|----|----|--------|----|-----|---|----------|---|---|---|---|---|----------|---|
| 0x008         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15    | 14 | 13 | 12 | 11     | 10 | 9   | 8 | 7        | 6 | 5 | 4 | 3 | 2 | 1        | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0   |    |    |    | 0      |    | 0x0 |   |          |   |   |   |   |   | 0        |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW    |    |    |    | RW     |    |     |   | RW       |   |   |   |   |   | RW       |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PRSEL |    |    |    | PRASYN |    |     |   | TRIGMODE |   |   |   |   |   | CONVMODE |   |

| Bit   | Name            | Reset   | Access  | Description  |
|-------|-----------------|---|---|--|
| 31:16 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 15:12 | PRSEL           | 0x0   | RW  | <b>Channel 0 PRS Trigger Select</b><br>Select Channel 0 PRS input channel.                         |
|       | Value           | Mode  | Description   |  |
|       | 0               | PRSCH0  | PRS ch 0 triggers a conversion.                     |  |
|       | 1               | PRSCH1  | PRS ch 1 triggers a conversion.                     |  |
|       | 2               | PRSCH2  | PRS ch 2 triggers a conversion.                     |  |
|       | 3               | PRSCH3  | PRS ch 3 triggers a conversion.                     |  |
|       | 4               | PRSCH4  | PRS ch 4 triggers a conversion.                     |  |
|       | 5               | PRSCH5  | PRS ch 5 triggers a conversion.                     |  |
|       | 6               | PRSCH6  | PRS ch 6 triggers a conversion.                     |  |
|       | 7               | PRSCH7  | PRS ch 7 triggers a conversion.                     |  |
|       | 8               | PRSCH8  | PRS ch 8 triggers a conversion.                     |  |
|       | 9               | PRSCH9  | PRS ch 9 triggers a conversion.                     |  |
|       | 10              | PRSCH10   | PRS ch 10 triggers a conversion.                    |  |
|       | 11              | PRSCH11   | PRS ch 11 triggers a conversion.                    |  |
| 11:9  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 8     | PRASYN          | 0   | RW  | <b>Channel 0 PRS Asynchronous Enable</b><br>Set this bit to 1 to treat PRS channel as asynchronous |
| 7     | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 6:4   | TRIGMODE        | 0x0   | RW  | <b>Channel 0 Trigger Mode</b><br>Select Channel 0 conversion trigger.                              |
|       | Value           | Mode  | Description   |  |
|       | 0               | SW  | Channel 0 is triggered by CH0DATA or COMBDATA write |  |
|       | 1               | PRS   | Channel 0 is triggered by PRS input                 |  |

| Bit | Name            | Reset   | Access                                  | Description   |
|-----|-----------------|---|---|---|
|     | 2               | REFRESH   |   | Channel 0 is triggered by Refresh timer                           |
|     | 3               | SWPRS   |   | Channel 0 is triggered by CH0DATA/COMBDATA write or PRS input     |
|     | 4               | SWREFRESH   |   | Channel 0 is triggered by CH0DATA/COMBDATA write or Refresh timer |
|     | 5               | LESENSE   |   | Channel 0 is triggered by LESENSE                                 |
| 3:1 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |
| 0   | CONVMODE        | 0   | RW                                      | <b>Conversion Mode</b><br>Configure conversion mode.              |
|     | Value           | Mode  | Description                             |   |
|     | 0               | CONTINUOUS  | DAC channel 0 is set in continuous mode |   |
|     | 1               | SAMPLEOFF   | DAC channel 0 is set in sample/off mode |   |

### 24.5.4 VDACn\_CH1CTRL - Channel 1 Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |       |    |    |    |        |    |     |   |          |   |   |   |   |   |          |   |    |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|----|----|----|--------|----|-----|---|----------|---|---|---|---|---|----------|---|----|--|
| 0x00C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15    | 14 | 13 | 12 | 11     | 10 | 9   | 8 | 7        | 6 | 5 | 4 | 3 | 2 | 1        | 0 |    |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0   |    |    |    | 0      |    | 0x0 |   |          |   |   |   |   |   |          |   | 0  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW    |    |    |    | RW     |    |     |   | RW       |   |   |   |   |   |          |   | RW |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PRSEL |    |    |    | PRASYN |    |     |   | TRIGMODE |   |   |   |   |   | CONVMODE |   |    |  |

| Bit   | Name     | Reset   | Access  | Description  |
|-------|----------|---|---|--|
| 31:16 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 15:12 | PRSEL    | 0x0   | RW  | <b>Channel 1 PRS Trigger Select</b><br>Select Channel 1 PRS input channel.                         |
|       | Value    | Mode  | Description   |  |
|       | 0        | PRSCH0  | PRS ch 0 triggers a conversion.                     |  |
|       | 1        | PRSCH1  | PRS ch 1 triggers a conversion.                     |  |
|       | 2        | PRSCH2  | PRS ch 2 triggers a conversion.                     |  |
|       | 3        | PRSCH3  | PRS ch 3 triggers a conversion.                     |  |
|       | 4        | PRSCH4  | PRS ch 4 triggers a conversion.                     |  |
|       | 5        | PRSCH5  | PRS ch 5 triggers a conversion.                     |  |
|       | 6        | PRSCH6  | PRS ch 6 triggers a conversion.                     |  |
|       | 7        | PRSCH7  | PRS ch 7 triggers a conversion.                     |  |
|       | 8        | PRSCH8  | PRS ch 8 triggers a conversion.                     |  |
|       | 9        | PRSCH9  | PRS ch 9 triggers a conversion.                     |  |
|       | 10       | PRSCH10   | PRS ch 10 triggers a conversion.                    |  |
|       | 11       | PRSCH11   | PRS ch 11 triggers a conversion.                    |  |
| 11:9  | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 8     | PRASYN   | 0   | RW  | <b>Channel 1 PRS Asynchronous Enable</b><br>Set this bit to 1 to treat PRS channel as asynchronous |
| 7     | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 6:4   | TRIGMODE | 0x0   | RW  | <b>Channel 1 Trigger Mode</b><br>Select Channel 1 conversion trigger.                              |
|       | Value    | Mode  | Description   |  |
|       | 0        | SW  | Channel 1 is triggered by CH1DATA or COMBDATA write |  |
|       | 1        | PRS   | Channel 1 is triggered by PRS input                 |  |

| Bit | Name            | Reset   | Access                                  | Description   |
|-----|-----------------|---|---|---|
|     | 2               | REFRESH   |   | Channel 1 is triggered by Refresh timer                           |
|     | 3               | SWPRS   |   | Channel 1 is triggered by CH1DATA/COMBDATA write or PRS input     |
|     | 4               | SWREFRESH   |   | Channel 1 is triggered by CH1DATA/COMBDATA write or Refresh timer |
|     | 5               | LESENSE   |   | Channel 1 is triggered by LESENSE                                 |
| 3:1 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |
| 0   | CONVMODE        | 0   | RW                                      | <b>Conversion Mode</b><br>Configure conversion mode.              |
|     | Value           | Mode  | Description                             |   |
|     | 0               | CONTINUOUS  | DAC channel 1 is set in continuous mode |   |
|     | 1               | SAMPLEOFF   | DAC channel 1 is set in sample/off mode |   |

## 24.5.5 VDACn\_CMD - Command Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |         |        |         |        |         |        |    |    |    |    |    |   |   |   |   |   |   |        |       |        |       |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|---------|--------|---------|--------|---------|--------|----|----|----|----|----|---|---|---|---|---|---|--------|-------|--------|-------|----|
| 0x010         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20      | 19     | 18      | 17     | 16      | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3      | 2     | 1      | 0     |    |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    | 0       | 0      | 0       | 0      | 0       | 0      |    |    |    |    |    |   |   |   |   |   |   | 0      | 0     | 0      | 0     |    |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    | W1      | W1     | W1      | W1     | W1      | W1     | W1 |    |    |    |    |   |   |   |   |   |   |        | W1    | W1     | W1    | W1 |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    | OPA2DIS | OPA2EN | OPA1DIS | OPA1EN | OPA0DIS | OPA0EN |    |    |    |    |    |   |   |   |   |   |   | CH1DIS | CH1EN | CH0DIS | CH0EN |    |

| Bit   | Name                              | Reset   | Access | Description                  |
|-------|-----------------------------------|---|--------|------------------------------|
| 31:22 | <i>Reserved</i>                   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |                              |
| 21    | OPA2DIS<br>Disables OPA2.         | 0   | W1     | <b>OPA2 Disable</b>          |
| 20    | OPA2EN<br>Enables OPA2            | 0   | W1     | <b>OPA2 Enable</b>           |
| 19    | OPA1DIS<br>Disables OPA1.         | 0   | W1     | <b>OPA1 Disable</b>          |
| 18    | OPA1EN<br>Enables OPA1            | 0   | W1     | <b>OPA1 Enable</b>           |
| 17    | OPA0DIS<br>Disables OPA0.         | 0   | W1     | <b>OPA0 Disable</b>          |
| 16    | OPA0EN<br>Enables OPA0            | 0   | W1     | <b>OPA0 Enable</b>           |
| 15:4  | <i>Reserved</i>                   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |                              |
| 3     | CH1DIS<br>Disables DAC Channel 1  | 0   | W1     | <b>DAC Channel 1 Disable</b> |
| 2     | CH1EN<br>Enables DAC Channel 1.   | 0   | W1     | <b>DAC Channel 1 Enable</b>  |
| 1     | CH0DIS<br>Disables DAC Channel 0. | 0   | W1     | <b>DAC Channel 0 Disable</b> |
| 0     | CH0EN<br>Enables DAC Channel 0    | 0   | W1     | <b>DAC Channel 0 Enable</b>  |

### 24.5.6 VDACn\_IF - Interrupt Flag Register

| Offset        | Bit Position |              |              |              |    |    |    |    |    |                |                |                |    |                   |                   |                   |         |    |    |    |    |    |   |   |       |       |       |       |       |       |       |       |   |
|---------------|--------------|--------------|--------------|--------------|----|----|----|----|----|----------------|----------------|----------------|----|-------------------|-------------------|-------------------|---------|----|----|----|----|----|---|---|-------|-------|-------|-------|-------|-------|-------|-------|---|
| 0x014         | 31           | 30           | 29           | 28           | 27 | 26 | 25 | 24 | 23 | 22             | 21             | 20             | 19 | 18                | 17                | 16                | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |   |
| <b>Reset</b>  |              | 0            | 0            | 0            |    |    |    |    |    | 0              | 0              | 0              |    | 0                 | 0                 | 0                 | 0       |    |    |    |    |    |   |   |       | 1     | 1     | 0     | 0     | 0     | 0     | 0     | 0 |
| <b>Access</b> |              | R            | R            | R            |    |    |    |    |    | R              | R              | R              |    | R                 | R                 | R                 | R       |    |    |    |    |    |   |   |       | R     | R     | R     | R     | R     | R     | R     | R |
| <b>Name</b>   |              | OPA2OUTVALID | OPA1OUTVALID | OPA0OUTVALID |    |    |    |    |    | OPA2PRSTIMEERR | OPA1PRSTIMEERR | OPA0PRSTIMEERR |    | OPA2APORTCONFLICT | OPA1APORTCONFLICT | OPA0APORTCONFLICT | EM23ERR |    |    |    |    |    |   |   | CH1BL | CH0BL | CH1UF | CH0UF | CH1OF | CH0OF | CH1CD | CH0CD |   |

| Bit   | Name              | Reset   | Access | Description   |
|-------|-------------------|---|--------|---|
| 31    | <i>Reserved</i>   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 30    | OPA2OUTVALID      | 0   | R      | <b>OPA3 Output Valid Interrupt Flag</b><br>OPA2 output is settled externally at the load  |
| 29    | OPA1OUTVALID      | 0   | R      | <b>OPA1 Output Valid Interrupt Flag</b><br>OPA1 output is settled externally at the load  |
| 28    | OPA0OUTVALID      | 0   | R      | <b>OPA0 Output Valid Interrupt Flag</b><br>OPA0 output is settled externally at the load  |
| 27:23 | <i>Reserved</i>   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 22    | OPA2PRSTIME-DERR  | 0   | R      | <b>OPA2 PRS Trigger Mode Error Interrupt Flag</b><br>Indicates that in TIMED PRS triggered mode, the negative edge of the PRS pulse came before the OPA output was valid. |
| 21    | OPA1PRSTIME-DERR  | 0   | R      | <b>OPA1 PRS Trigger Mode Error Interrupt Flag</b><br>Indicates that in TIMED PRS triggered mode, the negative edge of the PRS pulse came before the OPA output was valid. |
| 20    | OPA0PRSTIME-DERR  | 0   | R      | <b>OPA0 PRS Trigger Mode Error Interrupt Flag</b><br>Indicates that in TIMED PRS triggered mode, the negative edge of the PRS pulse came before the OPA output was valid. |
| 19    | <i>Reserved</i>   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 18    | OPA2APORTCONFLICT | 0   | R      | <b>OPA2 Bus Conflict Output Interrupt Flag</b><br>1 if any of the APORTs being requested by the OPA0 are also being requested by another peripheral.                      |
| 17    | OPA1APORTCONFLICT | 0   | R      | <b>OPA1 Bus Conflict Output Interrupt Flag</b><br>1 if any of the APORTs being requested by the OPA1 are also being requested by another peripheral.                      |
| 16    | OPA0APORTCONFLICT | 0   | R      | <b>OPA0 Bus Conflict Output Interrupt Flag</b><br>1 if any of the APORTs being requested by the OPA0 are also being requested by another peripheral.                      |

| Bit  | Name            | Reset   | Access | Description  |
|------|-----------------|---|--------|--|
| 15   | EM23ERR         | 0   | R      | <b>EM2/3 Entry Error Flag</b><br>Set when going to EM2/3 while DACCLKMODE equals SYNC and a channel is enabled |
| 14:8 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 7    | CH1BL           | 1   | R      | <b>Channel 1 Buffer Level Interrupt Flag</b><br>Indicates space available in CH1DATA.                          |
| 6    | CH0BL           | 1   | R      | <b>Channel 0 Buffer Level Interrupt Flag</b><br>Indicates space available in CH0DATA.                          |
| 5    | CH1UF           | 0   | R      | <b>Channel 1 Data Underflow Interrupt Flag</b><br>Indicates channel 1 data underflow.                          |
| 4    | CH0UF           | 0   | R      | <b>Channel 0 Data Underflow Interrupt Flag</b><br>Indicates channel 0 data underflow.                          |
| 3    | CH1OF           | 0   | R      | <b>Channel 1 Data Overflow Interrupt Flag</b><br>Indicates channel 1 data overflow.                            |
| 2    | CH0OF           | 0   | R      | <b>Channel 0 Data Overflow Interrupt Flag</b><br>Indicates channel 0 data overflow.                            |
| 1    | CH1CD           | 0   | R      | <b>Channel 1 Conversion Done Interrupt Flag</b><br>Indicates channel 1 conversion complete.                    |
| 0    | CH0CD           | 0   | R      | <b>Channel 0 Conversion Done Interrupt Flag</b><br>Indicates channel 0 conversion complete.                    |

### 24.5.7 VDACn\_IFS - Interrupt Flag Set Register

| Offset        | Bit Position |              |              |              |    |    |    |    |    |                 |                 |                 |    |                   |                   |                   |         |    |    |    |    |    |   |   |   |   |       |       |       |       |       |       |    |
|---------------|--------------|--------------|--------------|--------------|----|----|----|----|----|-----------------|-----------------|-----------------|----|-------------------|-------------------|-------------------|---------|----|----|----|----|----|---|---|---|---|-------|-------|-------|-------|-------|-------|----|
| 0x018         | 31           | 30           | 29           | 28           | 27 | 26 | 25 | 24 | 23 | 22              | 21              | 20              | 19 | 18                | 17                | 16                | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5     | 4     | 3     | 2     | 1     | 0     |    |
| <b>Reset</b>  |              | 0            | 0            | 0            |    |    |    |    |    | 0               | 0               | 0               |    | 0                 | 0                 | 0                 | 0       |    |    |    |    |    |   |   |   |   |       | 0     | 0     | 0     | 0     | 0     | 0  |
| <b>Access</b> |              | W1           | W1           | W1           |    |    |    |    |    | W1              | W1              | W1              |    | W1                | W1                | W1                | W1      |    |    |    |    |    |   |   |   |   |       | W1    | W1    | W1    | W1    | W1    | W1 |
| <b>Name</b>   |              | OPA2OUTVALID | OPA1OUTVALID | OPA0OUTVALID |    |    |    |    |    | OPA2PRSTIMEDERR | OPA1PRSTIMEDERR | OPA0PRSTIMEDERR |    | OPA2APORTCONFLICT | OPA1APORTCONFLICT | OPA0APORTCONFLICT | EM23ERR |    |    |    |    |    |   |   |   |   | CH1UF | CH0UF | CH1OF | CH0OF | CH1CD | CH0CD |    |

| Bit   | Name              | Reset   | Access | Description  |
|-------|-------------------|---|--------|--|
| 31    | <i>Reserved</i>   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 30    | OPA2OUTVALID      | 0   | W1     | <b>Set OPA2OUTVALID Interrupt Flag</b><br>Write 1 to set the OPA2OUTVALID interrupt flag           |
| 29    | OPA1OUTVALID      | 0   | W1     | <b>Set OPA1OUTVALID Interrupt Flag</b><br>Write 1 to set the OPA1OUTVALID interrupt flag           |
| 28    | OPA0OUTVALID      | 0   | W1     | <b>Set OPA0OUTVALID Interrupt Flag</b><br>Write 1 to set the OPA0OUTVALID interrupt flag           |
| 27:23 | <i>Reserved</i>   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 22    | OPA2PRSTIME-DERR  | 0   | W1     | <b>Set OPA2PRSTIMEDERR Interrupt Flag</b><br>Write 1 to set the OPA2PRSTIMEDERR interrupt flag     |
| 21    | OPA1PRSTIME-DERR  | 0   | W1     | <b>Set OPA1PRSTIMEDERR Interrupt Flag</b><br>Write 1 to set the OPA1PRSTIMEDERR interrupt flag     |
| 20    | OPA0PRSTIME-DERR  | 0   | W1     | <b>Set OPA0PRSTIMEDERR Interrupt Flag</b><br>Write 1 to set the OPA0PRSTIMEDERR interrupt flag     |
| 19    | <i>Reserved</i>   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 18    | OPA2APORTCONFLICT | 0   | W1     | <b>Set OPA2APORTCONFLICT Interrupt Flag</b><br>Write 1 to set the OPA2APORTCONFLICT interrupt flag |
| 17    | OPA1APORTCONFLICT | 0   | W1     | <b>Set OPA1APORTCONFLICT Interrupt Flag</b><br>Write 1 to set the OPA1APORTCONFLICT interrupt flag |

| Bit  | Name                   | Reset   | Access | Description  |
|------|------------------------|---|--------|--|
| 16   | OPA0APORTCON-<br>FLICT | 0   | W1     | <b>Set OPA0APORTCONFLICT Interrupt Flag</b><br><br>Write 1 to set the OPA0APORTCONFLICT interrupt flag |
| 15   | EM23ERR                | 0   | W1     | <b>Set EM23ERR Interrupt Flag</b><br><br>Write 1 to set the EM23ERR interrupt flag                     |
| 14:6 | <i>Reserved</i>        | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 5    | CH1UF                  | 0   | W1     | <b>Set CH1UF Interrupt Flag</b><br><br>Write 1 to set the CH1UF interrupt flag                         |
| 4    | CH0UF                  | 0   | W1     | <b>Set CH0UF Interrupt Flag</b><br><br>Write 1 to set the CH0UF interrupt flag                         |
| 3    | CH1OF                  | 0   | W1     | <b>Set CH1OF Interrupt Flag</b><br><br>Write 1 to set the CH1OF interrupt flag                         |
| 2    | CH0OF                  | 0   | W1     | <b>Set CH0OF Interrupt Flag</b><br><br>Write 1 to set the CH0OF interrupt flag                         |
| 1    | CH1CD                  | 0   | W1     | <b>Set CH1CD Interrupt Flag</b><br><br>Write 1 to set the CH1CD interrupt flag                         |
| 0    | CH0CD                  | 0   | W1     | <b>Set CH0CD Interrupt Flag</b><br><br>Write 1 to set the CH0CD interrupt flag                         |

## 24.5.8 VDACn\_IFC - Interrupt Flag Clear Register

| Offset | Bit Position |              |              |              |    |    |    |    |    |                 |                 |                 |    |                   |                   |                   |         |    |    |    |    |    |   |   |   |   |       |       |       |       |       |       |       |
|--------|--------------|--------------|--------------|--------------|----|----|----|----|----|-----------------|-----------------|-----------------|----|-------------------|-------------------|-------------------|---------|----|----|----|----|----|---|---|---|---|-------|-------|-------|-------|-------|-------|-------|
| 0x01C  | 31           | 30           | 29           | 28           | 27 | 26 | 25 | 24 | 23 | 22              | 21              | 20              | 19 | 18                | 17                | 16                | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5     | 4     | 3     | 2     | 1     | 0     |       |
| Reset  |              | 0            | 0            | 0            |    |    |    |    |    | 0               | 0               | 0               |    | 0                 | 0                 | 0                 | 0       |    |    |    |    |    |   |   |   |   |       | 0     | 0     | 0     | 0     | 0     | 0     |
| Access |              | (R)W1        | (R)W1        | (R)W1        |    |    |    |    |    | (R)W1           | (R)W1           | (R)W1           |    | (R)W1             | (R)W1             | (R)W1             | (R)W1   |    |    |    |    |    |   |   |   |   |       | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 |
| Name   |              | OPA2OUTVALID | OPA1OUTVALID | OPA0OUTVALID |    |    |    |    |    | OPA2PRSTIMEDERR | OPA1PRSTIMEDERR | OPA0PRSTIMEDERR |    | OPA2APORTCONFLICT | OPA1APORTCONFLICT | OPA0APORTCONFLICT | EM23ERR |    |    |    |    |    |   |   |   |   | CH1UF | CH0UF | CH1OF | CH0OF | CH1CD | CH0CD |       |

| Bit   | Name              | Reset  | Access | Description   |
|-------|-------------------|--|--------|---|
| 31    | Reserved          | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 30    | OPA2OUTVALID      | 0  | (R)W1  | <b>Clear OPA2OUTVALID Interrupt Flag</b><br>Write 1 to clear the OPA2OUTVALID interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).           |
| 29    | OPA1OUTVALID      | 0  | (R)W1  | <b>Clear OPA1OUTVALID Interrupt Flag</b><br>Write 1 to clear the OPA1OUTVALID interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).           |
| 28    | OPA0OUTVALID      | 0  | (R)W1  | <b>Clear OPA0OUTVALID Interrupt Flag</b><br>Write 1 to clear the OPA0OUTVALID interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).           |
| 27:23 | Reserved          | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 22    | OPA2PRSTIME-DERR  | 0  | (R)W1  | <b>Clear OPA2PRSTIMEDERR Interrupt Flag</b><br>Write 1 to clear the OPA2PRSTIMEDERR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 21    | OPA1PRSTIME-DERR  | 0  | (R)W1  | <b>Clear OPA1PRSTIMEDERR Interrupt Flag</b><br>Write 1 to clear the OPA1PRSTIMEDERR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 20    | OPA0PRSTIME-DERR  | 0  | (R)W1  | <b>Clear OPA0PRSTIMEDERR Interrupt Flag</b><br>Write 1 to clear the OPA0PRSTIMEDERR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 19    | Reserved          | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 18    | OPA2APORTCONFLICT | 0  | (R)W1  | <b>Clear OPA2APORTCONFLICT Interrupt Flag</b><br>Write 1 to clear the OPA2APORTCONFLICT interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |

| Bit  | Name                   | Reset   | Access | Description   |
|------|------------------------|---|--------|---|
| 17   | OPA1APORTCON-<br>FLICT | 0   | (R)W1  | <b>Clear OPA1APORTCONFLICT Interrupt Flag</b><br><br>Write 1 to clear the OPA1APORTCONFLICT interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 16   | OPA0APORTCON-<br>FLICT | 0   | (R)W1  | <b>Clear OPA0APORTCONFLICT Interrupt Flag</b><br><br>Write 1 to clear the OPA0APORTCONFLICT interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 15   | EM23ERR                | 0   | (R)W1  | <b>Clear EM23ERR Interrupt Flag</b><br><br>Write 1 to clear the EM23ERR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                     |
| 14:6 | <i>Reserved</i>        | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 5    | CH1UF                  | 0   | (R)W1  | <b>Clear CH1UF Interrupt Flag</b><br><br>Write 1 to clear the CH1UF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                         |
| 4    | CH0UF                  | 0   | (R)W1  | <b>Clear CH0UF Interrupt Flag</b><br><br>Write 1 to clear the CH0UF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                         |
| 3    | CH1OF                  | 0   | (R)W1  | <b>Clear CH1OF Interrupt Flag</b><br><br>Write 1 to clear the CH1OF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                         |
| 2    | CH0OF                  | 0   | (R)W1  | <b>Clear CH0OF Interrupt Flag</b><br><br>Write 1 to clear the CH0OF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                         |
| 1    | CH1CD                  | 0   | (R)W1  | <b>Clear CH1CD Interrupt Flag</b><br><br>Write 1 to clear the CH1CD interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                         |
| 0    | CH0CD                  | 0   | (R)W1  | <b>Clear CH0CD Interrupt Flag</b><br><br>Write 1 to clear the CH0CD interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                         |

### 24.5.9 VDACn\_IEN - Interrupt Enable Register

| Offset        | Bit Position |              |              |              |    |    |    |    |    |                 |                 |                 |    |                   |                   |                   |         |    |    |    |    |    |   |   |       |       |       |       |       |       |       |       |    |
|---------------|--------------|--------------|--------------|--------------|----|----|----|----|----|-----------------|-----------------|-----------------|----|-------------------|-------------------|-------------------|---------|----|----|----|----|----|---|---|-------|-------|-------|-------|-------|-------|-------|-------|----|
| 0x020         | 31           | 30           | 29           | 28           | 27 | 26 | 25 | 24 | 23 | 22              | 21              | 20              | 19 | 18                | 17                | 16                | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |    |
| <b>Reset</b>  |              | 0            | 0            | 0            |    |    |    |    |    | 0               | 0               | 0               |    | 0                 | 0                 | 0                 | 0       |    |    |    |    |    |   |   |       | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0  |
| <b>Access</b> |              | RW           | RW           | RW           |    |    |    |    |    | RW              | RW              | RW              |    | RW                | RW                | RW                | RW      |    |    |    |    |    |   |   |       | RW    | RW |
| <b>Name</b>   |              | OPA2OUTVALID | OPA1OUTVALID | OPA0OUTVALID |    |    |    |    |    | OPA2PRSTIMEDERR | OPA1PRSTIMEDERR | OPA0PRSTIMEDERR |    | OPA2APORTCONFLICT | OPA1APORTCONFLICT | OPA0APORTCONFLICT | EM23ERR |    |    |    |    |    |   |   | CH1BL | CH0BL | CH1UF | CH0UF | CH1OF | CH0OF | CH1CD | CH0CD |    |

| Bit   | Name              | Reset   | Access | Description   |
|-------|-------------------|---|--------|---|
| 31    | <i>Reserved</i>   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 30    | OPA2OUTVALID      | 0   | RW     | <b>OPA2OUTVALID Interrupt Enable</b><br>Enable/disable the OPA2OUTVALID interrupt           |
| 29    | OPA1OUTVALID      | 0   | RW     | <b>OPA1OUTVALID Interrupt Enable</b><br>Enable/disable the OPA1OUTVALID interrupt           |
| 28    | OPA0OUTVALID      | 0   | RW     | <b>OPA0OUTVALID Interrupt Enable</b><br>Enable/disable the OPA0OUTVALID interrupt           |
| 27:23 | <i>Reserved</i>   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 22    | OPA2PRSTIME-DERR  | 0   | RW     | <b>OPA2PRSTIMEDERR Interrupt Enable</b><br>Enable/disable the OPA2PRSTIMEDERR interrupt     |
| 21    | OPA1PRSTIME-DERR  | 0   | RW     | <b>OPA1PRSTIMEDERR Interrupt Enable</b><br>Enable/disable the OPA1PRSTIMEDERR interrupt     |
| 20    | OPA0PRSTIME-DERR  | 0   | RW     | <b>OPA0PRSTIMEDERR Interrupt Enable</b><br>Enable/disable the OPA0PRSTIMEDERR interrupt     |
| 19    | <i>Reserved</i>   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 18    | OPA2APORTCONFLICT | 0   | RW     | <b>OPA2APORTCONFLICT Interrupt Enable</b><br>Enable/disable the OPA2APORTCONFLICT interrupt |
| 17    | OPA1APORTCONFLICT | 0   | RW     | <b>OPA1APORTCONFLICT Interrupt Enable</b><br>Enable/disable the OPA1APORTCONFLICT interrupt |

| Bit  | Name              | Reset   | Access | Description   |
|------|-------------------|---|--------|---|
| 16   | OPA0APORTCONFLICT | 0   | RW     | <b>OPA0APORTCONFLICT Interrupt Enable</b><br>Enable/disable the OPA0APORTCONFLICT interrupt |
| 15   | EM23ERR           | 0   | RW     | <b>EM23ERR Interrupt Enable</b><br>Enable/disable the EM23ERR interrupt                     |
| 14:8 | <i>Reserved</i>   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 7    | CH1BL             | 0   | RW     | <b>CH1BL Interrupt Enable</b><br>Enable/disable the CH1BL interrupt                         |
| 6    | CH0BL             | 0   | RW     | <b>CH0BL Interrupt Enable</b><br>Enable/disable the CH0BL interrupt                         |
| 5    | CH1UF             | 0   | RW     | <b>CH1UF Interrupt Enable</b><br>Enable/disable the CH1UF interrupt                         |
| 4    | CH0UF             | 0   | RW     | <b>CH0UF Interrupt Enable</b><br>Enable/disable the CH0UF interrupt                         |
| 3    | CH1OF             | 0   | RW     | <b>CH1OF Interrupt Enable</b><br>Enable/disable the CH1OF interrupt                         |
| 2    | CH0OF             | 0   | RW     | <b>CH0OF Interrupt Enable</b><br>Enable/disable the CH0OF interrupt                         |
| 1    | CH1CD             | 0   | RW     | <b>CH1CD Interrupt Enable</b><br>Enable/disable the CH1CD interrupt                         |
| 0    | CH0CD             | 0   | RW     | <b>CH0CD Interrupt Enable</b><br>Enable/disable the CH0CD interrupt                         |

#### 24.5.10 VDACn\_CH0DATA - Channel 0 Data Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |       |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|-------|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x024         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20    | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    | 0x800 |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    | RWH   |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    | DATA  |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:12 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 11:0  | DATA            | 0x800   | RWH    | <b>Channel 0 Data</b><br>This register contains the value which will be converted by DAC channel 0. |

## 24.5.11 VDACn\_CH1DATA - Channel 1 Data Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |       |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|-------|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x028         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20    | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    | 0x800 |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    | RWH   |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    | DATA  |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description   |
|-------|----------|--|--------|---|
| 31:12 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 11:0  | DATA     | 0x800  | RWH    | <b>Channel 1 Data</b><br>This register contains the value which will be converted by DAC channel 1. |

## 24.5.12 VDACn\_COMBDATA - Combined Data Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |    |    |    |    |    |         |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|----|----|----|----|----|---------|---|---|---|---|---|---|---|---|---|
| 0x02C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20      | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9       | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    | 0x800   |    |    |    |    |    |    |    |    |    |    | 0x800   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    | W       |    |    |    |    |    |    |    |    |    |    | W       |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    | CH1DATA |    |    |    |    |    |    |    |    |    |    | CH0DATA |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description  |
|-------|----------|--|--------|--|
| 31:28 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 27:16 | CH1DATA  | 0x800  | W      | <b>Channel 1 Data</b><br>Data written to this register will be written to DATA in VDACn_CH1DATA. |
| 15:12 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 11:0  | CH0DATA  | 0x800  | W      | <b>Channel 0 Data</b><br>Data written to this register will be written to DATA in VDACn_CH0DATA. |

### 24.5.13 VDACn\_CAL - Calibration Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |                |    |    |    |    |    |    |    |             |    |   |   |   |   |   |   |   |   |   |   |            |  |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|-------------|----|---|---|---|---|---|---|---|---|---|---|------------|--|--|--|
| 0x030         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19             | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11          | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |            |  |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    | 0x8            |    |    |    |    |    |    |    | 0x20        |    |   |   |   |   |   |   |   |   |   |   | 0x4        |  |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    | RW          |    |   |   |   |   |   |   |   |   |   |   | RW         |  |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    | GAINERRTRIMCH1 |    |    |    |    |    |    |    | GAINERRTRIM |    |   |   |   |   |   |   |   |   |   |   | OFFSETTRIM |  |  |  |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 31:20 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 19:16 | GAINERRTRIMCH1  | 0x8   | RW     | <b>Gain Error Trim Value for CH1</b><br><br>This register contains the fine gain error trim for CH1. Program with Device Information value found in DEVINFO_VDACnCH1CAL depending on chosen reference.   |
| 15:14 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 13:8  | GAINERRTRIM     | 0x20  | RW     | <b>Gain Error Trim Value</b><br><br>This register contains the fine gain error trim for CH0 and coarse gain error trim for CH1. Program with Device Information value found in DEVINFO_VDACnMAINCAL or DEVINFO_VDACnALTCAL depending on chosen reference and choice of main versus alternative output usage. |
| 7:3   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 2:0   | OFFSETTRIM      | 0x4   | RW     | <b>Input Buffer Offset Calibration Value</b><br><br>This register contains the DAC input buffer offset calibration value. Program with Device Information value found in DEVINFO_VDACnCH1CAL.  |

24.5.14 VDACn\_OPAx\_APORREQ - Operational Amplifier APOR Request Status Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |            |            |            |            |            |            |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|------------|------------|------------|------------|------------|------------|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x0A0         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9          | 8          | 7          | 6          | 5          | 4          | 3          | 2          | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R          | R          | R          | R          | R          | R          | R          | R          | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | APORT4YREQ | APORT4XREQ | APORT3YREQ | APORT3XREQ | APORT2YREQ | APORT2XREQ | APORT1YREQ | APORT1XREQ |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name       | Reset   | Access | Description  |
|-------|------------|---|--------|--|
| 31:10 | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 9     | APORT4YREQ | 0   | R      | <b>1 If the Bus Connected to APORT4Y is Requested</b><br>Reports if the bus connected to APORT4Y is being requested from the APORT |
| 8     | APORT4XREQ | 0   | R      | <b>1 If the Bus Connected to APORT4X is Requested</b><br>Reports if the bus connected to APORT4X is being requested from the APORT |
| 7     | APORT3YREQ | 0   | R      | <b>1 If the Bus Connected to APORT3Y is Requested</b><br>Reports if the bus connected to APORT3Y is being requested from the APORT |
| 6     | APORT3XREQ | 0   | R      | <b>1 If the Bus Connected to APORT3X is Requested</b><br>Reports if the bus connected to APORT3X is being requested from the APORT |
| 5     | APORT2YREQ | 0   | R      | <b>1 If the Bus Connected to APORT2Y is Requested</b><br>Reports if the bus connected to APORT2Y is being requested from the APORT |
| 4     | APORT2XREQ | 0   | R      | <b>1 If the Bus Connected to APORT2X is Requested</b><br>Reports if the bus connected to APORT2X is being requested from the APORT |
| 3     | APORT1YREQ | 0   | R      | <b>1 If the Bus Connected to APORT1X is Requested</b><br>Reports if the bus connected to APORT1X is being requested from the APORT |
| 2     | APORT1XREQ | 0   | R      | <b>1 If the Bus Connected to APORT2X is Requested</b><br>Reports if the bus connected to APORT2X is being requested from the APORT |
| 1:0   | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |

24.5.15 VDACn\_OPAn\_APORCONFLICT - Operational Amplifier APOR Conflict Status Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                 |                 |                 |                 |                 |                 |                 |                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|
| 0x0A4         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15              | 14              | 13              | 12              | 11              | 10              | 9               | 8               | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R               | R               | R               | R               | R               | R               | R               | R               | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | APORT4YCONFLICT | APORT4XCONFLICT | APORT3YCONFLICT | APORT3XCONFLICT | APORT2YCONFLICT | APORT2XCONFLICT | APORT1YCONFLICT | APORT1XCONFLICT |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |

| Bit   | Name            | Reset  | Access | Description   |
|-------|-----------------|--|--------|---|
| 31:10 | Reserved        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 9     | APORT4YCONFLICT | 0  | R      | <b>1 If the Bus Connected to APORT4Y is in Conflict With Another Peripheral</b><br><br>Reports if the bus connected to APORT4Y is is also being requested by another peripheral |
| 8     | APORT4XCONFLICT | 0  | R      | <b>1 If the Bus Connected to APORT4X is in Conflict With Another Peripheral</b><br><br>Reports if the bus connected to APORT4X is is also being requested by another peripheral |
| 7     | APORT3YCONFLICT | 0  | R      | <b>1 If the Bus Connected to APORT3Y is in Conflict With Another Peripheral</b><br><br>Reports if the bus connected to APORT3Y is is also being requested by another peripheral |
| 6     | APORT3XCONFLICT | 0  | R      | <b>1 If the Bus Connected to APORT3X is in Conflict With Another Peripheral</b><br><br>Reports if the bus connected to APORT3X is is also being requested by another peripheral |
| 5     | APORT2YCONFLICT | 0  | R      | <b>1 If the Bus Connected to APORT2Y is in Conflict With Another Peripheral</b><br><br>Reports if the bus connected to APORT2Y is is also being requested by another peripheral |
| 4     | APORT2XCONFLICT | 0  | R      | <b>1 If the Bus Connected to APORT2X is in Conflict With Another Peripheral</b><br><br>Reports if the bus connected to APORT2X is is also being requested by another peripheral |
| 3     | APORT1YCONFLICT | 0  | R      | <b>1 If the Bus Connected to APORT1X is in Conflict With Another Peripheral</b><br><br>Reports if the bus connected to APORT1X is is also being requested by another peripheral |
| 2     | APORT1XCONFLICT | 0  | R      | <b>1 If the Bus Connected to APORT1X is in Conflict With Another Peripheral</b><br><br>Reports if the bus connected to APORT1X is is also being requested by another peripheral |
| 1:0   | Reserved        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |

24.5.16 VDACn\_OPAX\_CTRL - Operational Amplifier Control Register

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |                 |                 |    |    |    |    |    |    |             |    |    |   |   |   |   |        |         |       |   |   |   |  |  |    |          |        |       |               |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|-----------------|-----------------|----|----|----|----|----|----|-------------|----|----|---|---|---|---|--------|---------|-------|---|---|---|--|--|----|----------|--------|-------|---------------|
| 0x0A8  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20              | 19              | 18 | 17 | 16 | 15 | 14 | 13 | 12          | 11 | 10 | 9 | 8 | 7 | 6 | 5      | 4       | 3     | 2 | 1 | 0 |  |  |    |          |        |       |               |
| Reset  |              |    |    |    |    |    |    |    |    |    |    | 0               | 0               |    |    |    |    |    |    | 0           |    |    |   |   |   |   | 0      | 0       |       |   |   |   |  |  | 0  | 1        | 1      | 0x2   |               |
| Access |              |    |    |    |    |    |    |    |    |    |    | RW              | RW              |    |    |    |    |    |    | RW          |    |    |   |   |   |   | RW     | RW      |       |   |   |   |  |  | RW | RW       | RW     | RW    |               |
| Name   |              |    |    |    |    |    |    |    |    |    |    | APORTYMASTERDIS | APORTXMASTERDIS |    |    |    |    |    |    | PRSOOUTMODE |    |    |   |   |   |   | PRRSEL | PRRMODE | PRSEN |   |   |   |  |  |    | OUTSCALE | HCMDIS | INCBW | DRIVESTRENGTH |

| Bit   | Name                   | Reset   | Access | Description  |       |             |             |                       |      |   |
|-------|------------------------|---|--------|--|-------|-------------|-------------|-----------------------|------|---|
| 31:22 | Reserved               | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |             |             |                       |      |   |
| 21    | APORTYMASTER-DIS       | 0   | RW     | <b>APORT Bus Master Disable</b><br><br>Determines if the OPAX will request the APORT bus Y with POSSEL, NEGSEL or APORTOUTSEL. This bit allows multiple APORT connected devices to monitor the same APORT bus simultaneously by allowing the OPAX to not master the selected bus. When 1, the determination is expected to be from another peripheral, and the OPAX only passively looks at the bus. When 1, the selection of channel for a selected bus is ignored (the bus is not), and is whatever selection the external device mastering the bus has configured for the APORT bus.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Bus mastering enabled</td> </tr> <tr> <td>1</td> <td>Bus mastering disabled</td> </tr> </tbody> </table> | Value | Description | 0           | Bus mastering enabled | 1    | Bus mastering disabled  |
| Value | Description            |   |        |  |       |             |             |                       |      |   |
| 0     | Bus mastering enabled  |   |        |  |       |             |             |                       |      |   |
| 1     | Bus mastering disabled |   |        |  |       |             |             |                       |      |   |
| 20    | APORTXMASTER-DIS       | 0   | RW     | <b>APORT Bus Master Disable</b><br><br>Determines if the OPAX will request the APORT bus X with POSSEL, NEGSEL or APORTOUTSEL. This bit allows multiple APORT connected devices to monitor the same APORT bus simultaneously by allowing the OPAX to not master the selected bus. When 1, the determination is expected to be from another peripheral, and the OPAX only passively looks at the bus. When 1, the selection of channel for a selected bus is ignored (the bus is not), and is whatever selection the external device mastering the bus has configured for the APORT bus.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Bus mastering enabled</td> </tr> <tr> <td>1</td> <td>Bus mastering disabled</td> </tr> </tbody> </table> | Value | Description | 0           | Bus mastering enabled | 1    | Bus mastering disabled  |
| Value | Description            |   |        |  |       |             |             |                       |      |   |
| 0     | Bus mastering enabled  |   |        |  |       |             |             |                       |      |   |
| 1     | Bus mastering disabled |   |        |  |       |             |             |                       |      |   |
| 19:17 | Reserved               | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |             |             |                       |      |   |
| 16    | PRSOOUTMODE            | 0   | RW     | <b>OPAx PRS Output Select</b><br><br>Selects OPAX Output to PRS.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>WARM</td> <td>Warm status available on PRS. Warm status indicates that opamp is warm and output is enabled.</td> </tr> </tbody> </table>  | Value | Mode        | Description | 0                     | WARM | Warm status available on PRS. Warm status indicates that opamp is warm and output is enabled. |
| Value | Mode                   | Description   |        |  |       |             |             |                       |      |   |
| 0     | WARM                   | Warm status available on PRS. Warm status indicates that opamp is warm and output is enabled.                                   |        |  |       |             |             |                       |      |   |

| Bit   | Name            | Reset   | Access  | Description  |
|-------|-----------------|---|---|--|
|       | 1               | OUTVALID  |   | Outvalid status available on PRS. Outvalid status indicates that opamp output is settled externally at the load. |
| 15:14 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 13:10 | PRSEL           | 0x0   | RW  | <b>OPAx PRS Trigger Select</b><br>Select Channel 0 PRS input channel.  |
|       | Value           | Mode  | Description   |  |
|       | 0               | PRSCH0  | PRS ch 0 triggers OPA.  |  |
|       | 1               | PRSCH1  | PRS ch 1 triggers OPA.  |  |
|       | 2               | PRSCH2  | PRS ch 2 triggers OPA.  |  |
|       | 3               | PRSCH3  | PRS ch 3 triggers OPA.  |  |
|       | 4               | PRSCH4  | PRS ch 4 triggers OPA.  |  |
|       | 5               | PRSCH5  | PRS ch 5 triggers OPA.  |  |
|       | 6               | PRSCH6  | PRS ch 6 triggers OPA.  |  |
|       | 7               | PRSCH7  | PRS ch 7 triggers OPA.  |  |
|       | 8               | PRSCH8  | PRS ch 8 triggers OPA.  |  |
|       | 9               | PRSCH9  | PRS ch 9 triggers OPA.  |  |
|       | 10              | PRSCH10   | PRS ch 10 triggers OPA.   |  |
|       | 11              | PRSCH11   | PRS ch 11 triggers OPA.   |  |
| 9     | PRSMODE         | 0   | RW  | <b>OPAx PRS Trigger Mode</b><br>PRS trigger mode of OPA.   |
|       | Value           | Mode  | Description   |  |
|       | 0               | PULSED  | PULSED trigger is considered a regular asynchronous pulse that starts OPA warmup sequence. The end of warmup sequence is controlled by timeout settings in OPAXTIMER. |  |
|       | 1               | TIMED   | TIMED trigger is considered a pulse long enough to provide OPA warmup sequence. The end of warmup sequence is controlled by negative edge of the pulse.               |  |
| 8     | PRSEN           | 0   | RW  | <b>OPAx PRS Trigger Enable</b><br>Select OPAx conversion trigger.  |
|       | Value           | Description   |   |  |
|       | 0               | OPAx is triggered by OPAXEN   |   |  |
|       | 1               | OPAx is triggered by PRS input  |   |  |
| 7:5   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 4     | OUTSCALE        | 0   | RW  | <b>Scale OPAx Output Driving Strength</b><br>Use this to scale OPAx output driving strength.                     |

| Bit | Name          | Reset | Access | Description   |
|-----|---------------|-------|--------|---|
|     | Value         | Mode  |        | Description   |
|     | 0             | FULL  |        | Select this for full output driving strength.   |
|     | 1             | HALF  |        | Select this for half output driving strength.   |
| 3   | HCMDIS        | 1     | RW     | <b>High Common Mode Disable</b><br><br>Set to disable high common mode. Disables rail-to-rail on input, while output still remains rail-to-rail. The input voltage to the opamp while HCM is disabled is restricted between VSS and VDD-1.2V. Setting this bit improves output linearity when input is low. |
| 2   | INCBW         | 1     | RW     | <b>OPAx Unity Gain Bandwidth Scale</b><br><br>Unity gain bandwidth scale.   |
|     | Value         |       |        | Description   |
|     | 0             |       |        | No scaling  |
|     | 1             |       |        | When set the unity gain bandwidth will be scaled by factor of 2.5. useful to make OPA operate faster for closed-loop gain setting greater than 3x.  |
| 1:0 | DRIVESTRENGTH | 0x2   | RW     | <b>OPAx Operation Mode</b><br><br>Selects OPAX operation mode.  |
|     | Value         |       |        | Description   |
|     | 0             |       |        | Lower accuracy with Low drive strength.   |
|     | 1             |       |        | Low accuracy with Low drive strength.   |
|     | 2             |       |        | High accuracy with High drive strength.   |
|     | 3             |       |        | Higher accuracy with High drive strength.   |

24.5.17 VDACn\_OPAX\_TIMER - Operational Amplifier Timer Control Register

| Offset        | Bit Position |    |    |    |    |    |            |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |   |   |   |   |   |   |   |   |            |   |  |  |  |  |
|---------------|--------------|----|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|---|---|---|---|---|---|---|---|------------|---|--|--|--|--|
| 0x0AC         | 31           | 30 | 29 | 28 | 27 | 26 | 25         | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13         | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1          | 0 |  |  |  |  |
| <b>Reset</b>  |              |    |    |    |    |    | 0x001      |    |    |    |    |    |    |    |    |    |    |    | 0x07       |    |    |    |   |   |   |   |   |   |   |   | 0x00       |   |  |  |  |  |
| <b>Access</b> |              |    |    |    |    |    | RW         |    |    |    |    |    |    |    |    |    |    |    | RW         |    |    |    |   |   |   |   |   |   |   |   | RW         |   |  |  |  |  |
| <b>Name</b>   |              |    |    |    |    |    | SETTLETIME |    |    |    |    |    |    |    |    |    |    |    | WARMUPTIME |    |    |    |   |   |   |   |   |   |   |   | STARTUPDLY |   |  |  |  |  |

| Bit   | Name       | Reset   | Access | Description  |
|-------|------------|---|--------|--|
| 31:26 | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 25:16 | SETTLETIME | 0x001   | RW     | <b>OPAx Output Settling Timeout Value</b><br>Number of clock cycles to drive the output                                  |
| 15    | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 14:8  | WARMUPTIME | 0x07  | RW     | <b>OPAx Warmup Time Count Value</b><br>OPAx warmup timeout value   |
| 7:6   | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 5:0   | STARTUPDLY | 0x00  | RW     | <b>OPAx Startup Delay Count Value</b><br>OPAx startup delay in us. Used only in PRS sample of mode of stand alone opamp. |

24.5.18 VDACn\_OPAX\_MUX - Operational Amplifier Mux Configuration Register

| Offset        | Bit Position |    |    |    |    |        |    |    |    |    |    |    |        |    |    |    |    |    |          |    |    |    |   |   |   |        |   |   |   |   |   |   |        |  |
|---------------|--------------|----|----|----|----|--------|----|----|----|----|----|----|--------|----|----|----|----|----|----------|----|----|----|---|---|---|--------|---|---|---|---|---|---|--------|--|
| 0x0B0         | 31           | 30 | 29 | 28 | 27 | 26     | 25 | 24 | 23 | 22 | 21 | 20 | 19     | 18 | 17 | 16 | 15 | 14 | 13       | 12 | 11 | 10 | 9 | 8 | 7 | 6      | 5 | 4 | 3 | 2 | 1 | 0 |        |  |
| <b>Reset</b>  |              |    |    |    |    | 0x0    |    |    |    |    |    |    | 1      |    |    |    |    |    | 0x6      |    |    |    |   |   |   | 0xF2   |   |   |   |   |   |   | 0xF1   |  |
| <b>Access</b> |              |    |    |    |    | RW     |    |    |    |    |    |    | RW     |    |    |    |    |    | RW       |    |    |    |   |   |   | RW     |   |   |   |   |   |   | RW     |  |
| <b>Name</b>   |              |    |    |    |    | RESSEL |    |    |    |    |    |    | GAIN3X |    |    |    |    |    | RESINMUX |    |    |    |   |   |   | NEGSEL |   |   |   |   |   |   | POSSEL |  |

| Bit   | Name     | Reset  | Access             | Description   |
|-------|----------|--|--------------------|---|
| 31:27 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i>  |                    |   |
| 26:24 | RESSEL   | 0x0  | RW                 | <b>OPAx Resistor Ladder Select</b><br>Configures the resistor ladder tap for OPAX.                              |
|       | Value    | Mode   | Resistor Value     |   |
|       | 0        | RES0   | R2 = 1/3 x R1      |   |
|       | 1        | RES1   | R2 = R1            |   |
|       | 2        | RES2   | R2 = 1 2/3 x R1    |   |
|       | 3        | RES3   | R2 = 2 1/5 x R1    |   |
|       | 4        | RES4   | R2 = 3 x R1        |   |
|       | 5        | RES5   | R2 = 4 1/3 x R1    |   |
|       | 6        | RES6   | R2 = 7 x R1        |   |
|       | 7        | RES7   | R2 = 15 x R1       |   |
| 23:21 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i>  |                    |   |
| 20    | GAIN3X   | 1  | RW                 | <b>OPAx Dedicated 3x Gain Resistor Ladder</b><br>Selects gain of 3x.  |
|       | Value    | Description  |                    |   |
|       | 0        | Disables 3x gain ladder.   |                    |   |
|       | 1        | Enables and sets the gain to 3x. If this is set to 1, RESSEL will only be used externally by other opamps. By default this is set to 1 for dac to work properly. For stand alone opamp and to configure gain based on RESSEL value, users need to configure this to 0. |                    |   |
| 19    | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i>  |                    |   |
| 18:16 | RESINMUX | 0x6  | RW                 | <b>OPAx Resistor Ladder Input Mux</b><br>These bits selects the source for the input mux to the resistor ladder |
|       | Value    | Mode   | Description        |   |
|       | 0        | DISABLE  | Set for Unity Gain |   |

| Bit | Name | Reset   | Access | Description  |
|-----|------|---------|--------|--|
| 1   |      | OPANEXT |        | Set for NEXTOUT(x-1) input   |
| 2   |      | NEGPAD  |        | NEG pad connected  |
| 3   |      | POSPAD  |        | POS pad connected  |
| 4   |      | COMPAD  |        | Neg pad of OPA0 connected. Direct input to support common reference.                 |
| 5   |      | CENTER  |        | OPA0 and OPA1 Resmux connected to form fully differential instrumentation amplifier. |
| 6   |      | VSS     |        | VSS connected  |

15:8 NEGSEL 0xF2 RW **OPAx Inverting Input Mux**

These bits selects the source for the inverting input on OPAx

| Mode        | Value | Description              |
|-------------|-------|--------------------------|
| APORT1YCH1  | 48    | Select APORT1YCH1        |
| APORT1YCH3  | 49    | Select APORT1YCH3        |
| APORT1YCH5  | 50    | Select APORT1YCH5        |
| ...         | ...   | .....                    |
| APORT1YCH31 | 63    | Select APORT1YCH31       |
| APORT2YCH0  | 80    | Select APORT2YCH0        |
| APORT2YCH2  | 81    | Select APORT2YCH2        |
| APORT2YCH4  | 82    | Select APORT2YCH3        |
| ...         | ...   | .....                    |
| APORT2YCH30 | 95    | Select APORT2YCH30       |
| APORT3YCH1  | 112   | Select APORT3YCH1        |
| APORT3YCH3  | 113   | Select APORT3YCH3        |
| APORT3YCH5  | 114   | Select APORT3YCH5        |
| ...         | ...   | .....                    |
| APORT3YCH31 | 127   | Select APORT3YCH31       |
| APORT4YCH0  | 144   | Select APORT4YCH0        |
| APORT4YCH2  | 145   | Select APORT4YCH2        |
| APORT4YCH4  | 146   | Select APORT4YCH4        |
| ...         | ...   | .....                    |
| APORT4YCH30 | 159   | Select APORT4YCH30       |
| DISABLE     | 240   | Input disabled           |
| UG          | 241   | Unity Gain feedback path |
| OPATAP      | 242   | OPAxTAP as input         |
| NEGPAD      | 243   | Input from NEG PAD       |

7:0 POSSEL 0xF1 RW **OPAx Non-inverting Input Mux**

These bits selects the source for the non-inverting input on OPAx

| Bit | Name         | Reset | Access | Description                                     |
|-----|--------------|-------|--------|---|
|     | Mode         | Value |        | Description                                     |
|     | APOINT1XCH0  | 32    |        | Select APOINT1XCH0                              |
|     | APOINT1XCH2  | 33    |        | Select APOINT1XCH2                              |
|     | APOINT1XCH4  | 34    |        | Select APOINT1XCH4                              |
|     | ...          | ...   |        | .....   |
|     | APOINT1XCH30 | 47    |        | Select APOINT1XCH30                             |
|     | APOINT2XCH1  | 64    |        | Select APOINT2XCH1                              |
|     | APOINT2XCH3  | 65    |        | Select APOINT2XCH3                              |
|     | APOINT2XCH5  | 66    |        | Select APOINT2XCH5                              |
|     | ...          | ...   |        | .....   |
|     | APOINT2XCH31 | 79    |        | Select APOINT2XCH30                             |
|     | APOINT3XCH0  | 96    |        | Select APOINT3XCH0                              |
|     | APOINT3XCH2  | 97    |        | Select APOINT3XCH2                              |
|     | APOINT3XCH4  | 98    |        | Select APOINT3XCH4                              |
|     | ...          | ...   |        | .....   |
|     | APOINT3XCH30 | 111   |        | Select APOINT3XCH30                             |
|     | APOINT4XCH1  | 128   |        | Select APOINT4XCH1                              |
|     | APOINT4XCH3  | 129   |        | Select APOINT4XCH3                              |
|     | APOINT4XCH5  | 130   |        | Select APOINT4XCH5                              |
|     | ...          | ...   |        | .....   |
|     | APOINT4XCH31 | 143   |        | Select APOINT4XCH31                             |
|     | DISABLE      | 240   |        | Input disabled                                  |
|     | DAC          | 241   |        | DAC as input                                    |
|     | POSPAD       | 242   |        | POS PAD as input                                |
|     | OPANEXT      | 243   |        | NEXTOUT(x-1) as input. For OPA0 not applicable. |
|     | OPATAP       | 244   |        | OPAxTAP as input. For OPA2 OPA0TAP.             |

24.5.19 VDACn\_OPAX\_OUT - Operational Amplifier Output Configuration Register

| Offset | Bit Position |    |    |    |    |    |    |    |             |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |           |   |   |   |   |   |   |   |       |            |          |           |
|--------|--------------|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|-----------|---|---|---|---|---|---|---|-------|------------|----------|-----------|
| 0x0B4  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |            |          |           |
| Reset  |              |    |    |    |    |    |    |    | 0x00        |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x00      |   |   |   |   |   |   |   | 0     | 0          | 0        | 1         |
| Access |              |    |    |    |    |    |    |    | RW          |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RW        |   |   |   |   |   |   |   | RW    | RW         | RW       | RW        |
| Name   |              |    |    |    |    |    |    |    | APORTOUTSEL |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | ALTOPADEN |   |   |   |   |   |   |   | SHORT | APORTOUTEN | ALTOUTEN | MAINOUTEN |

| Bit   | Name        | Reset  | Access | Description                                      |
|-------|-------------|--|--------|--|
| 31:24 | Reserved    | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 23:16 | APORTOUTSEL | 0x00   | RW     | <b>OPAx APORt Output</b><br>Select APORt output. |
|       | Mode        | Value  |        | Description                                      |
|       | APORT1YCH1  | 48   |        | Select APORt1YCH1                                |
|       | APORT1YCH3  | 49   |        | Select APORt1YCH3                                |
|       | APORT1YCH5  | 50   |        | Select APORt1YCH5                                |
|       | ...         | ...  |        | .....  |
|       | APORT1YCH31 | 63   |        | Select APORt1YCH31                               |
|       | APORT2YCH0  | 80   |        | Select APORt2YCH0                                |
|       | APORT2YCH2  | 81   |        | Select APORt2YCH2                                |
|       | APORT2YCH4  | 82   |        | Select APORt2YCH3                                |
|       | ...         | ...  |        | .....  |
|       | APORT2YCH30 | 95   |        | Select APORt2YCH30                               |
|       | APORT3YCH1  | 112  |        | Select APORt3YCH1                                |
|       | APORT3YCH3  | 113  |        | Select APORt3YCH3                                |
|       | APORT3YCH5  | 114  |        | Select APORt3YCH5                                |
|       | ...         | ...  |        | .....  |
|       | APORT3YCH31 | 127  |        | Select APORt3YCH31                               |
|       | APORT4YCH0  | 144  |        | Select APORt4YCH0                                |
|       | APORT4YCH2  | 145  |        | Select APORt4YCH2                                |
|       | APORT4YCH4  | 146  |        | Select APORt4YCH4                                |
|       | ...         | ...  |        | .....  |
|       | APORT4YCH30 | 159  |        | Select APORt4YCH30                               |
| 15:9  | Reserved    | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |

| Bit | Name        | Reset | Access | Description   |
|-----|-------------|-------|--------|---|
| 8:4 | ALTOUTPADEN | 0x00  | RW     | <b>OPAx Output Enable Value</b><br>Set to enable output, clear to disable output  |
|     | OUT ENABLE  | VALUE |        | Description   |
|     | OUT0        | xxxx1 |        | Alternate Output 0  |
|     | OUT1        | xxx1x |        | Alternate Output 1  |
|     | OUT2        | xx1xx |        | Alternate Output 2  |
|     | OUT3        | x1xxx |        | Alternate Output 3  |
|     | OUT4        | 1xxxx |        | Alternate Output 4  |
| 3   | SHORT       | 0     | RW     | <b>OPAx Main and Alternative Output Short</b><br>Set this to short circuit main and alternative outputs. This will keep the outputs shorted even when the VDAC is disabled. |
| 2   | APORTOUTEN  | 0     | RW     | <b>OPAx Aport Output Enable</b><br>Set this to enable aport output of OPAx.   |
| 1   | ALTOUTEN    | 0     | RW     | <b>OPAx Alternative Output Enable</b><br>Set this to enable alternative output of OPAx.   |
| 0   | MAINOUTEN   | 1     | RW     | <b>OPAx Main Output Enable</b><br>Set this to enable main output of OPAx.   |

### 24.5.20 VDACn\_OPAX\_CAL - Operational Amplifier Calibration Register

| Offset        | Bit Position |    |    |         |    |    |    |    |    |         |    |    |    |     |    |    |    |     |    |    |     |    |   |   |   |     |     |   |   |   |   |     |
|---------------|--------------|----|----|---------|----|----|----|----|----|---------|----|----|----|-----|----|----|----|-----|----|----|-----|----|---|---|---|-----|-----|---|---|---|---|-----|
| 0x0B8         | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22      | 21 | 20 | 19 | 18  | 17 | 16 | 15 | 14  | 13 | 12 | 11  | 10 | 9 | 8 | 7 | 6   | 5   | 4 | 3 | 2 | 1 | 0   |
| <b>Reset</b>  |              |    |    | 0x00    |    |    |    |    |    | 0x00    |    |    |    | 0x0 |    |    |    | 0x4 |    |    | 0x0 |    |   |   |   | 0x7 |     |   |   |   |   | 0x7 |
| <b>Access</b> |              |    |    | RW      |    |    |    |    |    | RW      |    |    |    | RW  |    |    |    | RW  |    |    | RW  |    |   |   |   | RW  |     |   |   |   |   | RW  |
| <b>Name</b>   |              |    |    | OFFSETN |    |    |    |    |    | OFFSETP |    |    |    | GM3 |    |    |    | GM  |    |    |     |    |   |   |   |     | CM2 |   |   |   |   | CM1 |

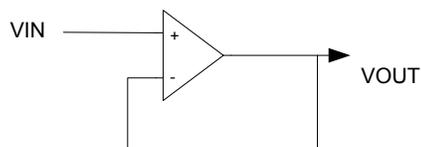
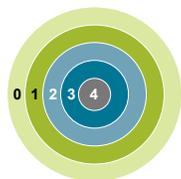
| Bit   | Name     | Reset   | Access | Description   |
|-------|----------|---|--------|---|
| 31    | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 30:26 | OFFSETN  | 0x00  | RW     | <b>OPAx Inverting Input Offset Configuration Value</b><br><br>This register contains the offset calibration value for inverting input. Program with value obtained from Device Information page (DEVINFO_OPAXCALn) depending on OPAMP number and chosen DRIVESTRENGTH.                |
| 25    | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 24:20 | OFFSETP  | 0x00  | RW     | <b>OPAx Non-Inverting Input Offset Configuration Value</b><br><br>This register contains the offset calibration value for Non-inverting input offset. Program with value obtained from Device Information page (DEVINFO_OPAXCALn) depending on OPAMP number and chosen DRIVESTRENGTH. |
| 19    | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 18:17 | GM3      | 0x0   | RW     | <b>Gm3 Trim Value</b><br><br>Gm trim code of OPAMP stage 3. Additional trim for OPAMP stage 3. Program with value obtained from Device Information page (DEVINFO_OPAXCALn) depending on OPAMP number and chosen DRIVESTRENGTH.  |
| 16    | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 15:13 | GM       | 0x4   | RW     | <b>Gm Trim Value</b><br><br>Gm trim value common to all OPAMP stages to keep the bandwidth insensitive to process variation. Program with value obtained from Device Information page (DEVINFO_OPAXCALn) depending on OPAMP number and chosen DRIVESTRENGTH.                          |
| 12    | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 11:10 | CM3      | 0x0   | RW     | <b>Compensation Cap Cm3 Trim Value</b><br><br>Program with value obtained from Device Information page (DEVINFO_OPAXCALn) depending on OPAMP number and chosen DRIVESTRENGTH.   |
| 9     | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 8:5   | CM2      | 0x7   | RW     | <b>Compensation Cap Cm2 Trim Value</b><br><br>Program with value obtained from Device Information page (DEVINFO_OPAXCALn) depending on OPAMP number and chosen DRIVESTRENGTH.   |
| 4     | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |

---

| Bit | Name | Reset | Access | Description   |
|-----|------|-------|--------|---|
| 3:0 | CM1  | 0x7   | RW     | <b>Compensation Cap Cm1 Trim Value</b><br><br>Program with value obtained from Device Information page (DEVINFO_OPAXCALn) depending on OPAMP number and chosen DRIVESTRENGTH. |

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## 25. OPAMP - Operational Amplifier



### Quick Facts

#### What?

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas. With flexible gain and interconnection built-in, they can be configured to support multiple common opamp functions. All pins are available externally for filter configurations. Each opamp has a rail-to-rail input and a rail-to-rail output.

#### Why?

The opamps are included not only to save energy on a PCB compared to standalone opamps but also to reduce system cost by replacing external opamps.

#### How?

Two of the opamps are made available as part of the VDAC, while the other opamps are standalone. In addition to popular differential-to-single ended and differential-to-differential driver modes, an ADC unity gain buffer mode configuration makes it possible to isolate kickback noise. The opamps can also be configured as a multi-step cascaded PGA, and for all of the built-in modes no external components are necessary.

### 25.1 Introduction

The opamps are highly configurable general purpose opamps, suitable for simple filters and buffer applications. The 3 opamps can be configured to support various operational amplifier functions through a network of muxes with possibilities of selecting ranges of on-chip non-inverting and inverting gain configurations and selecting between outputs to various destinations. The opamps can also be configured with external feedback in addition to supporting cascade connections between two or three opamps. The opamps are rail-to-rail in and out. A user selectable mode has been added to optimize linearity, in which case the input voltage to the opamp is restricted to a range between VSS and AVDD-1.2V.

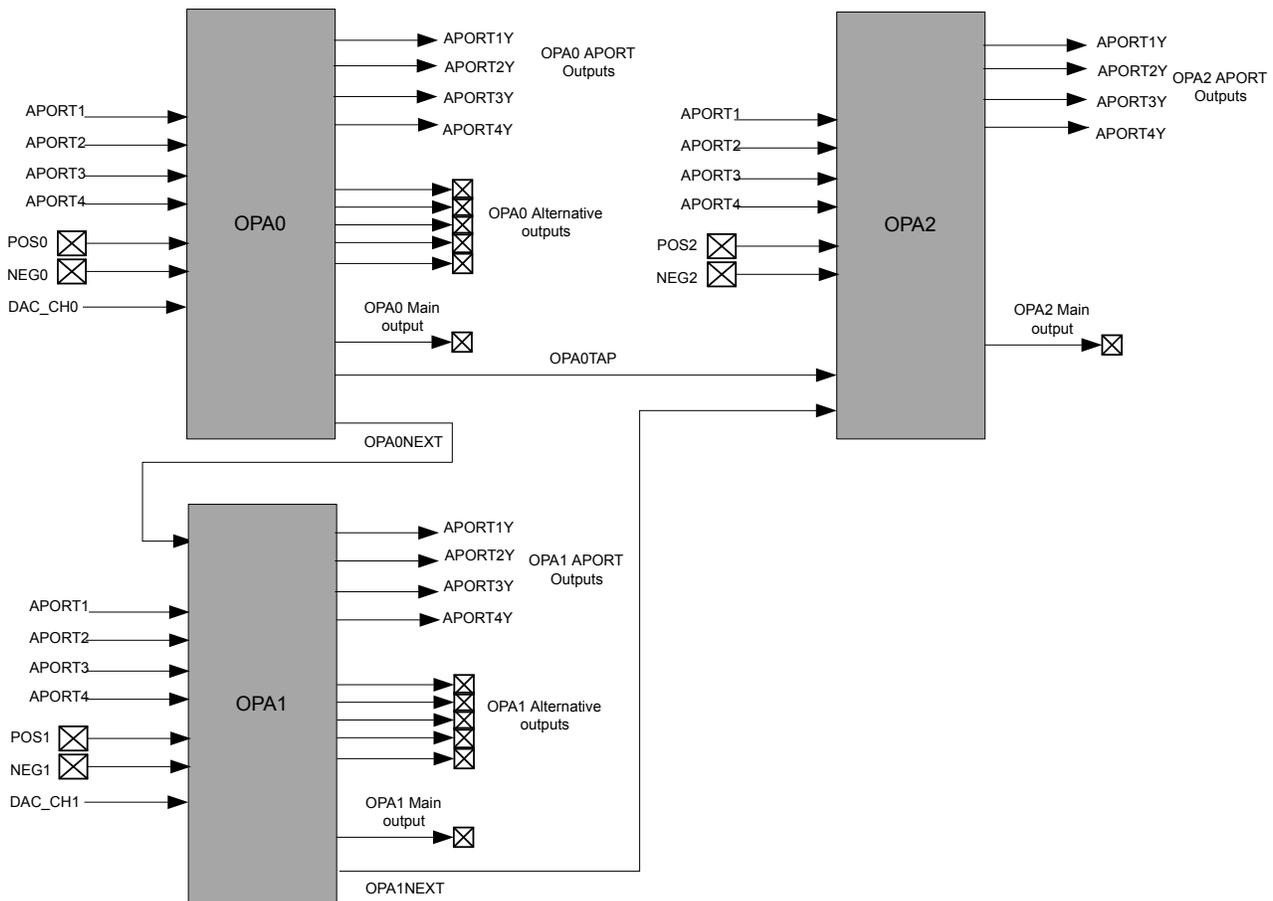
### 25.2 Features

- 3 individually configurable opamps
- Opamps support rail-to-rail inputs and outputs
- Supports the following functions
  - General opamp mode
  - Voltage follower unity gain
  - Inverting input PGA
  - Non-inverting PGA
  - Cascaded inverting PGA
  - Cascaded non-inverting PGA
  - Two opamp differential amplifier
  - Three opamp differential amplifier
  - Dual buffer ADC driver
- Programmable gain
- Programmable drive strength
- Programmable start delay, warmup and settle time
- Connection to APORT
- Enable / Disable via PRS

- Output status to PRS

### 25.3 Functional Description

The 3 opamps can be configured to perform various opamp functions through a network of muxes. An overview of the opamps are shown in [Figure 25.1 OPAMP System Overview on page 838](#). Two of the 3 opamps are part of the VDAC, while the others are stand-alone. The outputs of the opamps can be routed to the ADC and ACMP. All 3 opamps can also take input from pins. Since OPA0 and OPA1 are part of the VDAC, special considerations needs to be taken when both VDAC channel 0/channel 1 and OPA0/OPA1 are used. For detailed explanation, refer to [25.3.5 Opamp VDAC Combination](#).



**Figure 25.1. OPAMP System Overview**

There is a set of input muxes for each opamp, making it possible to select various input sources. A more detailed view of the 3 opamps, including the mux network is shown in [Figure 25.2 OPAMP Overview on page 839](#). The POSSEL mux connected to the positive input makes it possible to select a pin, another opamp output, or tap from the resistor network. Similarly, the NEGSEL mux on the negative input makes it possible to select a pin or a feedback path as its source. The feedback path can be unity gain, 3x gain, or selected from the resistor network for programmable gain. Each opamp has several outputs, a main output, an alternative output network, APORT output and a next output. These outputs make it possible to route the output to a pin, another opamp input, the ADC, the ACMP, or into the feedback path. For details regarding configuring the outputs, see [25.3.1.8 Output Configuration](#). In addition, there is also a mux to configure the resistor ladder for connection to VSS, a pin, or another opamp output.

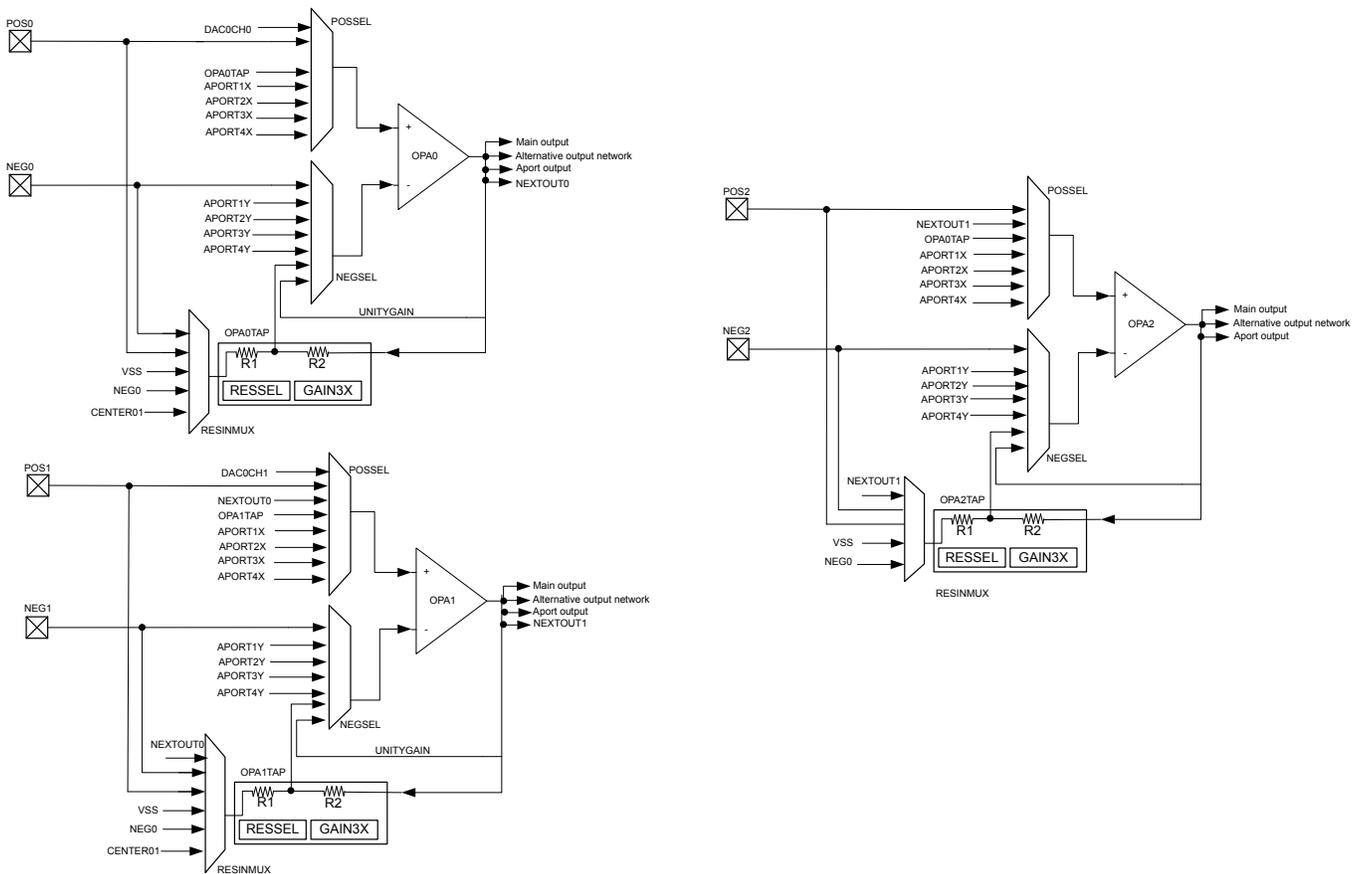


Figure 25.2. OPAMP Overview

### 25.3.1 Opamp Configuration

Since two of the 3 OPAMPs (OPA0, OPA1) are part of the VDACC, the opamp configuration registers are located in the VDACC.

Each OPAMP can be enabled by setting OPAXEN in VDACCn\_CMD and can be disabled by setting OPAXDIS in VDACCn\_CMD. The enabled status of each OPAMP can be read by polling the OPAXENS bit in VDACCn\_STATUS. OPAXENS goes high immediately after an OPAXEN is written and goes low when OPAXDIS is written and after OPAMP is completely disabled.

Software *must not* write to the following registers while OPAXENS set.

- VDACCn\_OPAX\_CTRL
- VDACCn\_OPAX\_TIMER
- VDACCn\_OPAX\_MUX

#### 25.3.1.1 Enable Sources

Opamp can be enabled either with software or PRS. The default source is software. Setting PRSEN to 1 in VDACCn\_OPAX\_CTRL enables PRS mode. In PRS mode, opamp has two options, which are selectable with PRSMODE in VDACCn\_OPAX\_CTRL. If PRSMODE is configured to TIMED, opamp is turned on on the positive edge of PRS and stays on until PRS goes low. If PRSMODE is configured to PULSED, opamp is turned on on the positive edge of PRS and stays on based on the timer configurations in VDACCn\_OPAX\_TIMER. The PRS channel is selected by PRSSEL in VDACCn\_OPAX\_CTRL.

#### 25.3.1.2 Warmup Time

When an opamp is enabled some initialization time is required. The warm up period is programmable with WARMUPTIME in VDACCn\_OPAX\_TIME. The OPAXWARM bit in VDACCn\_STATUS are set when the warmup period has completed.

The warm up period depends on the selected DRIVESTRENGTH in VDACCn\_OPAX\_CTRL.

**Table 25.1. OPAMP Warmup Time**

| DRIVESTRENGTH | WARMUPTIME ( $\mu$ s) |
|---------------|-----------------------|
| 0             | 100                   |
| 1             | 85                    |
| 2             | 8                     |
| 3             | 6                     |

**25.3.1.3 Settle Time**

After an opamp is enabled and the warmed-up time has elapsed the output settles externally. The settle period is programmable with SETTLETIME in VDACCn\_OPAX\_TIME. The OPAXOUTVALID bit in VDACCn\_STATUS is set when the settle period has completed. When in use by the VDACC the default settling time is used.

The settling period depends on the load at opamp output and DRIVESTRENGTH of the opamp. [Table 25.2 OPAMP Settling Time on page 840](#) specifies SETTLETIME settings for a load of 1KOhm and 75pF.

**Table 25.2. OPAMP Settling Time**

| DRIVESTRENGTH | SETTLETIME ( $\mu$ s) |
|---------------|-----------------------|
| 0             | 60                    |
| 1             | 25                    |
| 2             | 3                     |
| 3             | 1                     |

**25.3.1.4 Startup Delay**

Each opamp has an option to delay the warm up period. The startup delay is programmable with STARTDLY in VDACCn\_OPAX\_TIME. If STARTDLY is programmed to a non-zero value, the opamp is warmed up after STARTDLY+WARMUPTIME, and the output settles after STARTDLY+WARMUPTIME+SETTLETIME.

**25.3.1.5 Power Supply**

The opamp module power ( $V_{OPA}$ ) is derived from the AVDD supply pin.

**25.3.1.6 I/O Pin Considerations**

The maximum usable analog signal that can be applied to external opamp inputs (or seen on external opamp outputs) depends on several factors: whether the signal is routed through the APORT, whether High Linearity mode is used, whether overvoltage is enabled, and on the IOVDD/AVDD supply voltages, as shown in the [Table 25.3 Maximum Usable IO Voltage on page 840](#) table.

**Table 25.3. Maximum Usable IO Voltage**

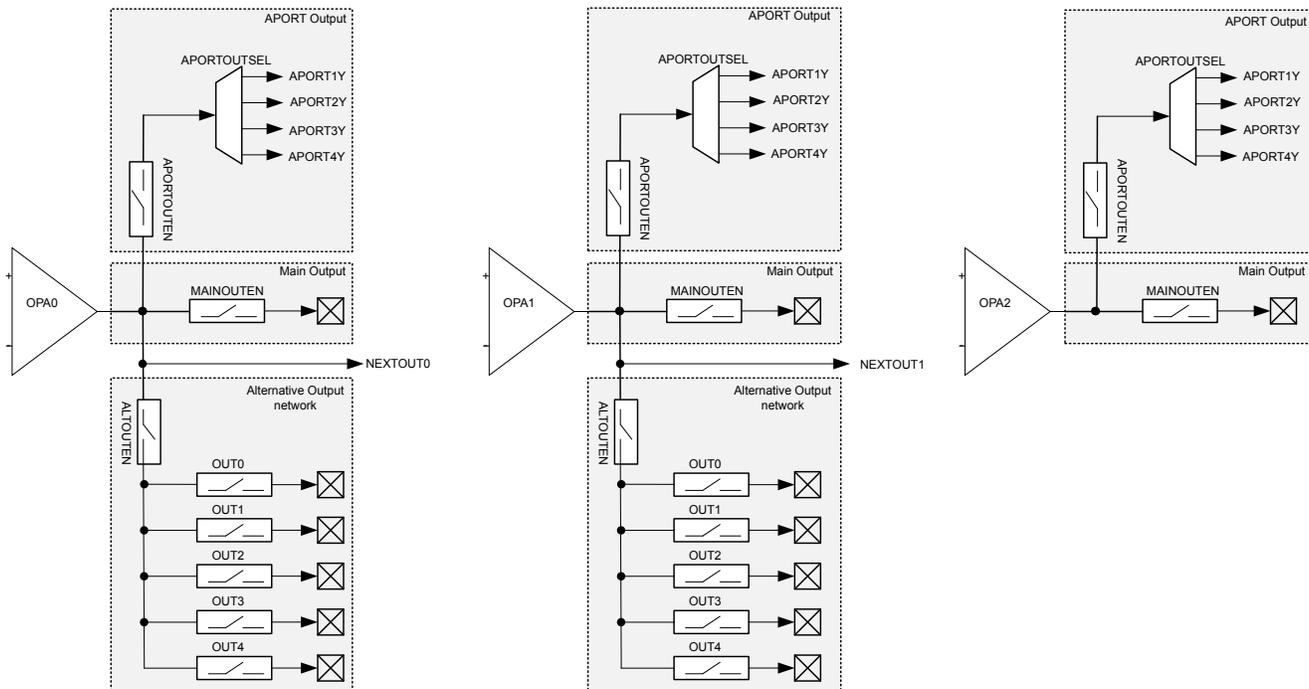
| Opamp Pin                  | Maximum IO Voltage (APORT USED and OVT Enabled/ Disabled) | Maximum IO Voltage (APORT UNUSED, OVT Enabled) | Maximum IO Voltage (APORT UNUSED, OVT Disabled) |
|----------------------------|---|--|---|
| Opamp Inputs - Normal Mode | MIN(AVDD, IOVDD)  | MIN(AVDD, IOVDD)                               | MIN(AVDD, IOVDD)                                |
| Opamp Outputs              | MIN(AVDD, IOVDD)  | MIN(AVDD, IOVDD + 2 V)                         | MIN(AVDD, IOVDD)                                |

### 25.3.1.7 Input Configuration

The inputs to the opamps are controlled through a set of input muxes. The mux connected to the positive input is configured by the POSSEL bit-field in the VDACn\_OPAX\_MUX register. Similarly, the mux connected to the negative input is configured by setting the NEGSEL bit-field in VDACn\_OPAX\_MUX. The input into the resistor ladder can be configured by setting the RESINMUX bit-field in VDACn\_OPAX\_MUX.

### 25.3.1.8 Output Configuration

Each opamp has three outputs: the main output, an alternative output network with lower drive strength, and an APORT output with low drive strength. These three outputs can be configured as shown in [Figure 25.3 Opamp Output Stage Overview on page 841](#). The main output can be used to drive the main output by setting MAINOUTEN in VDACn\_OPAX\_OUT. The alternative output can drive the alternative output network by setting ALTOUTEN in VDACn\_OPAX\_OUT. The APORT output can drive the APORT selection mux by setting APORTOUTSEL in VDACn\_OPAX\_OUT.



**Figure 25.3. Opamp Output Stage Overview**

The alternative output network consists of connections to pins and a connection to the next opamp. The connections to pins can be individually enabled by configuring ALTOUTPADEN in the VDACn\_OPAX\_OUT register. For cascaded opamp configurations, each opamp has a NEXTOUT connection.

The opamp outputs can also be routed to APORT1Y, APORT2Y, APORT3Y, and APORT4Y. The APORT channel can be selected by configuring APORTOUTSEL in VDACn\_OPAX\_OUT.

The opamps are also routed internally to the ADC. OPA0 and OPA1 are routed through the POSMUX of the ADC, and OPA2 routed through the NEGMUX of the ADC. See [27.3.7 Input Selection](#) in the ADC chapter for information on how to configure the ADC input mux.

In addition, OPA0 and OPA1 are internally routed to both the POSMUX and NEGMUX of ACMP. See [26.3.6 Input Selection](#) in the ACMP chapter for information on how to configure the ACMP input mux.

The main and alternate outputs of each opamp can be shorted together by setting the SHORT bit-field in VDACn\_OPAX\_OUT.

### 25.3.1.9 Gain Programming

The feedback path of each mux includes a resistor ladder that can be used to select a set of gain values. Gain is configured by the RESSEL bit-field located in the VDACn\_OPAX\_MUX register. Gain values are determined by the resistor ladder based on ratio of R2/R1. It is also possible to bypass the resistor ladder in unity gain mode. In addition, there is also a preconfigured resistor ladder with

3X gain. The 3x gain resistor ladder is enabled by setting GAIN3X in VDACn\_OPAX\_MUX. By default all opamps are configured in 3x gain mode. When using RESSEL, GAIN3X should be set to zero.

#### 25.3.1.10 Offset Calibration

Each opamp has a calibration register, VDACn\_OPAX\_CAL, where calibration values for both offset and gain correction can be written. The required calibration settings depend on the chosen DRIVESTRENGTH. The default calibration settings stored in VDACn\_OPAX\_CAL are for DRIVESTRENGTH=2. If an opamp is being reconfigured, the required calibration settings for DRIVESTRENGTH=n can be found in DEVINFO\_OPAXCALn. Offsets can be programmed through the OFFSETP and OFFSETN bitfields of VDACn\_OPAX\_CAL.

#### 25.3.1.11 Disabling of Rail-to-Rail Operation

Each opamp can have its input rail-to-rail stage disabled by setting the HCMDIS in VDACn\_OPAX\_CTRL. Disabling the rail-to-rail input stage improves linearity of the opamp, thus improving the total harmonic distortion (THD) at the cost of reduced input signal swing.

#### 25.3.1.12 Unity Gain Bandwidth Scaling

Unity gain bandwidth of an opamp can be scaled setting the INCBW bit in VDACn\_OPAX\_CTRL. Note that this setting is used only when closed loop gain is greater than 3X. With this setting is enabled, the opamp is not unity gain stable.

#### 25.3.1.13 Opamp Output Scaling

Opamp output drive strength is scaled by one half when the OUTSCALE bit in VDACn\_OPAX\_CTRL is set.

### 25.3.2 Interrupts and PRS Output

Each opamp has an interrupt flag OPAXOUTVALID in VDACn\_IF that is set when the output is settled externally at the load. An interrupt will be requested if the OPAXOUTVALID interrupt flag in VDACn\_IF is set and enabled by the OPAXOUTVALID bit in VDACn\_IEN.

The OPAXERRPRSMODE interrupt flag in VDACn\_IF indicates a protocol error when the opamp is triggered in PRS TIMED mode. This flag is set if the negative edge of the PRS pulse came before the output to opamp is valid. The interrupt flag is enabled by the OPAXERRPRSMODE bit in VDACn\_IEN.

An interrupt can also be requested when an APORT bus conflict occurs if the OPAXAPORTCONFLICT interrupt flag in VDACn\_IF is set and enabled through by the OPAXAPORTCONFLICT bit in VDACn\_IEN.

One of two asynchronous PRS outputs can be enabled for each opamp by setting PRSOUTMODE in VDACn\_OPAX\_CTRL. If PRSOUTMODE is WARM, opamp warm-up status is available. If PRSOUTMODE is OUTVALID, opamp output valid status is available.

### 25.3.3 APORT Request and Conflict Status

The opamps are connected to pins through the APORT system. To help debug over-utilization of APORT resources, the opamps provide request and conflict status information. The request status of APORT buses is visible through the DACn\_OPAX\_APORTREQ register.

If an APORT bus conflict occurs, it is reported in the DACn\_OPAX\_APORTCONFLICT register. An APORT conflict occurs if an opamp requests the same bus at the same time as another analog peripheral. In addition an APORT conflict is reported if any two of NEGSEL, POSSEL or APORTOUTSEL are configured to request the same APORT bus.

It is possible for the opamps to passively monitor APORT buses without controlling the switches and creating bus conflicts. This can be done by setting APORTXMASTERDIS or APORTYMASTERDIS in the DACn\_OPAX\_CTRL register.

### 25.3.4 Opamp Modes

The opamps can perform several different functions by configuring the internal signal routing between the opamps. The modes available are described in the following sections.

#### 25.3.4.1 General Opamp Mode

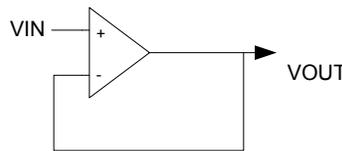
In this mode, the resistor ladder is isolated from the feedback path, and the input signal routing is defined by POSSEL and NEGSEL in VDACn\_OPAX\_MUX. The output signal routing is defined by the setting of VDACn\_OPAX\_OUT.

**Table 25.4. General Opamp Mode Configuration**

| OPA Bitfields | OPA Configuration                |
|---------------|----------------------------------|
| OPAx POSSEL   | POSPADx, APORT[1-4]X             |
| OPAx NEGSEL   | OPATAP, UG, NEGPADx, APORT[1-4]Y |
| OPAx RESINMUX | NEXTOUT, POSPADx, NEGPADx, VSS   |

**25.3.4.2 Voltage Follower Unity Gain**

In this mode, the unity gain feedback path is selected for the negative input by setting the NEGSEL bit-field to UG in the VDACn\_OPAX\_MUX register as shown in [Figure 25.4 Voltage Follower Unity Gain Overview on page 843](#). The positive input is selected by the POSSEL bit-field in VDACn\_OPAX\_MUX, and the output is configured by VDACn\_OPAX\_OUT register.



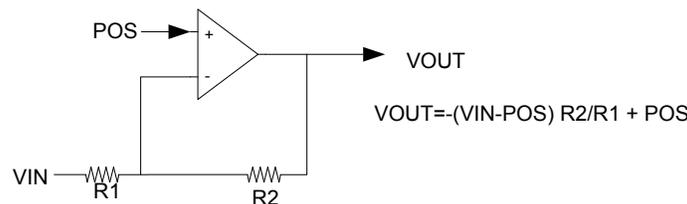
**Figure 25.4. Voltage Follower Unity Gain Overview**

**Table 25.5. Voltage Follower Unity Gain Configuration**

| OPA Bitfields | OPA Configuration                     |
|---------------|---------------------------------------|
| OPAx POSSEL   | OPATAP, NEXTOUT, POSPADx, APORT[1-4]X |
| OPAx NEGSEL   | UG                                    |
| OPAx RESINMUX | DISABLE                               |

**25.3.4.3 Inverting Input PGA**

[Figure 25.5 Inverting Input PGA Overview on page 843](#) shows the inverting input PGA configuration. In this mode, the negative input is connected to the resistor ladder by setting the NEGSEL bit-field to OPATAP in the VDACn\_OPAX\_MUX register. This setting provides a programmable gain on the negative input, which is set by the RESSEL bit-field in VDACn\_OPAX\_MUX. Signal ground for the positive input can come from off-chip by setting the POSSEL bit-field to PAD or APORT in VDACn\_OPAX\_MUX. In addition, the output is configured by VDACn\_OPAX\_OUT register.



**Figure 25.5. Inverting Input PGA Overview**

Table 25.6. Inverting Input PGA Configuration

| OPA Bitfields | OPA Configuration         |
|---------------|---------------------------|
| OPAx POSSEL   | POSPADx, APORT[1-4]X      |
| OPAx NEGSEL   | OPATAP                    |
| OPAx RESINMUX | NEXTOUT, NEGPADx, POSPADx |

#### 25.3.4.4 Non-inverting PGA

Figure 25.6 Non-inverting PGA Overview on page 844 shows the non-inverting input configuration. In this mode, the negative input is connected to the resistor ladder by setting the NEGSEL bit-field to OPATAP in VDACCn\_OPAX\_MUX. This setting provides a programmable gain on the negative input, which is set by the RESSEL bit-field in VDACCn\_OPAX\_MUX. In addition, the RESINMUX bit-field must be set to VSS or NEGPAD in VDACCn\_OPAX\_MUX. The positive input is selected by the POSSEL bit-field, and the output is configured by VDACCn\_OPAX\_OUT register.

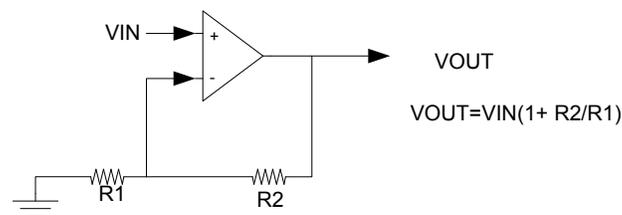


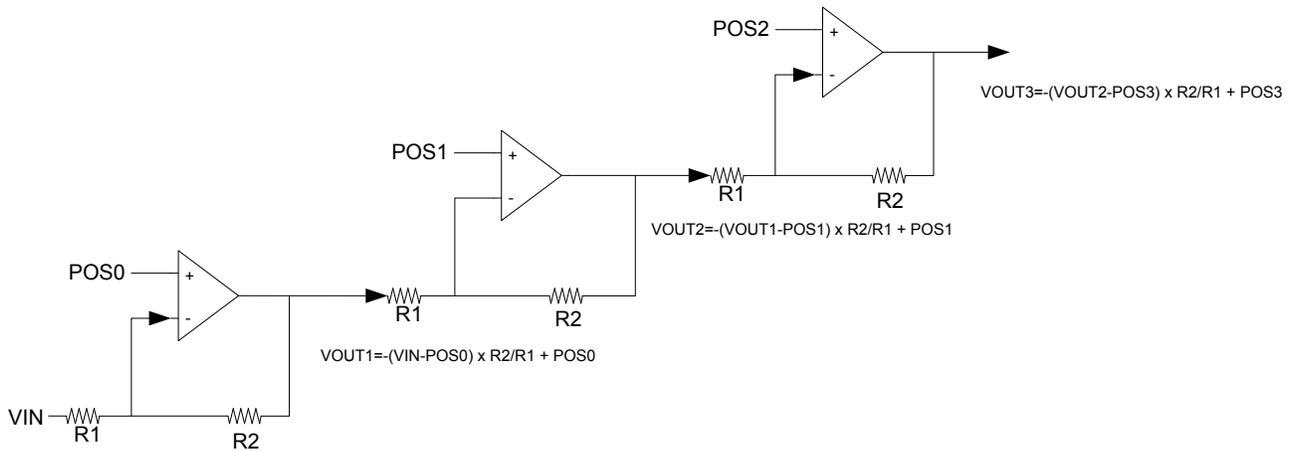
Figure 25.6. Non-inverting PGA Overview

Table 25.7. Non-inverting PGA Configuration

| OPA Bitfields | OPA Configuration             |
|---------------|-------------------------------|
| OPAx POSSEL   | NEXTOUT, POSPADx, APORT[1-4]X |
| OPAx NEGSEL   | OPATAP                        |
| OPAx RESINMUX | VSS, NEGPAD                   |

#### 25.3.4.5 Cascaded Inverting PGA

This mode enables the opamp signals to be internally configured to cascade two or more opamps in inverting mode as shown in Figure 25.7 Cascaded Inverting PGA Overview on page 845. In both cases, the positive input is connected to signal ground by setting the POSSEL bit-field to PAD or APORT in VDACCn\_OPAX\_MUX. When cascaded, the negative input is connected to the resistor ladder by setting the NEGSEL bit-field to OPATAP in VDACCn\_OPAX\_MUX. The input to the resistor ladder is configured by the RESINMUX bit-field in VDACCn\_OPAX\_MUX.



**Figure 25.7. Cascaded Inverting PGA Overview**

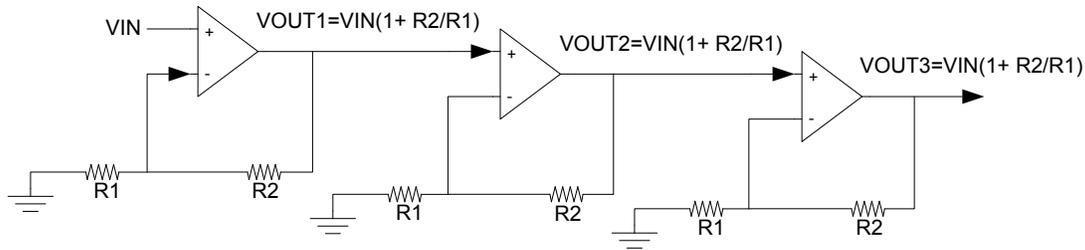
Table 25.8 Cascaded Inverting PGA Configuration on page 845 shows cascaded non-inverting PGA with OPA0, OPA1 and OPA2. The output from OPA0 is connected to OPA1 to create the second stage by setting the RESINMUX field to OPANEXT in VDACn\_OPA1\_MUX. The last stage is created by setting the RESINMUX bit-field to OPANEXT in VDACn\_OPA2\_MUX.

**Table 25.8. Cascaded Inverting PGA Configuration**

| OPA  | OPA Bitfields | OPA Configuration    |
|------|---------------|----------------------|
| OPA0 | POSSEL        | POSPAD0, APORT[1-4]X |
| OPA0 | NEGSEL        | OPATAP               |
| OPA0 | RESINMUX      | NEGPAD0              |
| OPA1 | POSSEL        | POSPAD1, APORT[1-4]X |
| OPA1 | NEGSEL        | OPATAP               |
| OPA1 | RESINMUX      | OPANEXT              |
| OPA2 | POSSEL        | POSPAD2, APORT[1-4]X |
| OPA2 | NEGSEL        | OPATAP               |
| OPA2 | RESINMUX      | OPANEXT              |

#### 25.3.4.6 Cascaded Non-inverting PGA

This mode enables the opamp signals to be internally configured to cascade two or more opamps in non-inverting mode as shown in Figure 25.8 Cascaded Non-inverting PGA Overview on page 846. The negative input for all opamps will be connected to the resistor ladder by setting the NEGSEL bit-field to OPATAP. In addition the resistor ladder input must be set to VSS or NEGPADx by configuring the RESINMUX bit-field in VDACn\_OPAx\_MUX.



**Figure 25.8. Cascaded Non-inverting PGA Overview**

Table 25.9 Cascaded Non-inverting PGA Configuration on page 846 shows cascaded non-inverting PGA with OPA0, OPA1 and OPA2. When cascaded, the positive input on OPA0 is configured by the POSSEL bit-field in VDACn\_OPA0\_MUX. The output from OPA0 is connected to OPA1 to create the second stage by setting the POSSEL field to OPANEXT in VDACn\_OPA1\_MUX. The last stage is created by setting the POSSEL bit-field to OPANEXT in VDACn\_OPA2\_MUX.

**Table 25.9. Cascaded Non-inverting PGA Configuration**

| OPA  | OPA Bitfields | OPA Configuration    |
|------|---------------|----------------------|
| OPA0 | POSSEL        | POSPAD0, APORT[1-4]X |
| OPA0 | NEGSEL        | OPATAP               |
| OPA0 | RESINMUX      | VSS, NEGPAD0         |
| OPA1 | POSSEL        | OPANEXT              |
| OPA1 | NEGSEL        | OPATAP               |
| OPA1 | RESINMUX      | VSS, NEGPAD1         |
| OPA2 | POSSEL        | OPANEXT              |
| OPA2 | NEGSEL        | OPATAP               |
| OPA2 | RESINMUX      | VSS, NEGPAD2         |

### 25.3.4.7 Two Opamp Differential Amplifier

This mode allows OPA0 and OPA1 or OPA1 and OPA2 to be internally connected to form a two opamp differential amplifier as shown in Figure 25.9 Two Op-amp Differential Amplifier Overview on page 847. When using OPA0 and OPA1, the positive input of OPA0 can be connected to any input by setting the POSSEL bit-field in VDACn\_OPA0\_MUX. The OPA0 feedback path must be configured for unity gain by setting the NEGSEL bit-field to UG in VDACn\_OPA0\_MUX. In addition, the OPA0 RESINMUX bit-field must be set to DISABLED. The OPA0 NEXTOUT output must be connected to OPA1 by setting the RESINMUX bit-field to OPANEXT in VDACn\_OPA1\_MUX. The positive input of OPA1 is selected by the POSSEL bit-field in VDACn\_OPA1\_MUX. The OPA1 output is configured by DACn\_OPA1\_OUT.

When using OPA1 and OPA2, the positive input of OPA1 can be connected to any input by setting the POSSEL bit-field in VDACn\_OPA1\_MUX. The OPA1 feedback path must be configured for unity gain by setting the NEGSEL bit-field to UG in VDACn\_OPA1\_MUX. In addition, the OPA1 RESINMUX bit-field must be set to DISABLED. The OPA1 NEXTOUT output must be connected to OPA2 by setting the RESINMUX bit-field to OPANEXT in VDACn\_OPA2\_MUX. The positive input of OPA2 is selected by the POSSEL bit-field in VDACn\_OPA2\_MUX. The OPA2 output is configured by DACn\_OPA2\_OUT.

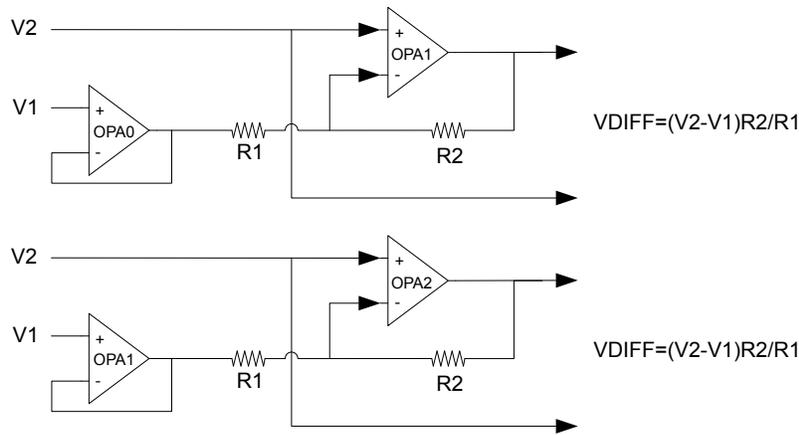


Figure 25.9. Two Op-amp Differential Amplifier Overview

Table 25.10. OPA0/OPA1 Differential Amplifier Configuration

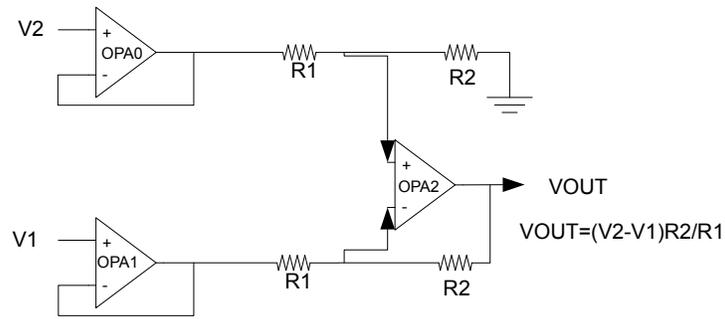
| OPA  | OPA Bitfields | OPA Configuration    |
|------|---------------|----------------------|
| OPA0 | POSSEL        | POSPAD0, APORT[1-4]X |
| OPA0 | NEGSEL        | UG                   |
| OPA0 | RESINMUX      | DISABLE              |
| OPA1 | POSSEL        | POSPAD1, APORT[1-4]X |
| OPA1 | NEGSEL        | OPATAP               |
| OPA1 | RESINMUX      | OPANEXT              |

Table 25.11. OPA1/OPA2 Differential Amplifier Configuration

| OPA  | OPA Bitfields | OPA Configuration    |
|------|---------------|----------------------|
| OPA1 | POSSEL        | POSPAD1, APORT[1-4]X |
| OPA1 | NEGSEL        | UG                   |
| OPA1 | RESINMUX      | DISABLE              |
| OPA2 | POSSEL        | POSPAD2, APORT[1-4]X |
| OPA2 | NEGSEL        | OPATAP               |
| OPA2 | RESINMUX      | OPANEXT              |

### 25.3.4.8 Three Opamp Differential Amplifier

This mode allows the three opamps to be internally configured to form a three opamp differential amplifier as shown in [Figure 25.10 Three Op-amp Differential Amplifier Overview on page 848](#). For both OPA0 and OPA1, the positive input can be connected to any input by configuring the OPA0 POSSEL and OPA1 POSSEL bitfields in VDACn\_OPA0\_MUX and VDACn\_OPA1\_MUX, respectively. The OPA0 and OPA1 feedback paths must be configured for unity gain by setting the OPA0 NEGSEL and OPA1 NEGSEL bitfields to UG in VDACn\_OPA0\_MUX and VDACn\_OPA1\_MUX respectively. In addition the OPA0 RESINMUX and OPA1 RESINMUX bitfields must be set to DISABLED. The OPA1 output must be connected to OPA2 by setting RESINMUX to OPANEXT in VDACn\_OPA2\_MUX and the OPA2 POSSEL must be set to OPATAP. The OPA2 output is configured by the DACn\_OPA2\_OUT register.



**Figure 25.10. Three Op-amp Differential Amplifier Overview**

The gain for the Three Opamp Differential Amplifier is determined by the combination of the gain settings of OPA0 and OPA2. Gain values of 1/3, 1 and 3, are available and programmed as shown in the table below.

**Table 25.12. Three Opamp Differential Amplifier Gain Programming**

| Gain | OPA0 RESSEL | OPA2 RESSEL |
|------|-------------|-------------|
| 1/3  | 4           | 0           |
| 1    | 1           | 1           |
| 3    | 0           | 4           |

**Table 25.13. Three Opamp Differential Amplifier Configuration**

| OPA  | OPA Bitfields | OPA Configuration    |
|------|---------------|----------------------|
| OPA0 | POSSEL        | POSPAD0, APORT[1-4]X |
| OPA0 | NEGSEL        | UG                   |
| OPA0 | RESINMUX      | DISABLE              |
| OPA1 | POSSEL        | POSPAD1, APORT[1-4]X |
| OPA1 | NEGSEL        | UG                   |
| OPA1 | RESINMUX      | DISABLE              |
| OPA2 | POSSEL        | OPATAP               |
| OPA2 | NEGSEL        | OPATAP               |
| OPA2 | RESINMUX      | OPANEXT              |

### 25.3.4.9 Instrumentation Amplifier

OPA0 and OPA1 can form a fully differential instrumentation amplifier by setting RESINMUX to CENTER for both opamps in VDACn\_OPA0\_MUX and VDACn\_OPA1\_MUX. Configuring RESINMUX to CENTER makes a connection between resistor ladder of the opamps as shown in [Figure 25.11 Instrumentaion Amplifier Overview on page 849](#).

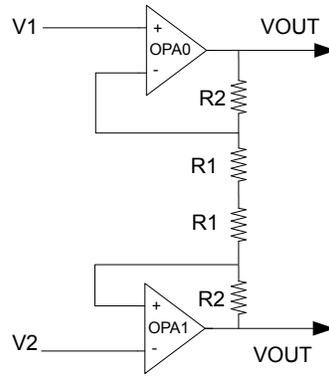


Figure 25.11. Instrumentation Amplifier Overview

### 25.3.4.10 Common Reference

It is possible to configure all opamps to have a common reference by setting the RESINMUX to COMPAD in VDACCn\_OPAX\_MUX. When RESINMUX of all opamps is set to COMPAD mode, the NEGPAID input of OPA0 is used.

### 25.3.4.11 Dual Buffer ADC Driver

It is possible to use any two of the opamps to form a Dual Buffer ADC driver as shown in [Figure 25.12 Dual Buffer ADC Driver Overview on page 849](#). Both opamps used must be configured in the same way. The positive input is configured by setting the OPAX POSSEL to PAD, and the negative input is connected to the resistor ladder by setting NEGSEL to OPATAP in VDACCn\_OPAX\_MUX. The output from the opamps can be configured to drive pins through the alternative output network or the APORT. The ADC can sample pins that the opamps are driving through the APORT.

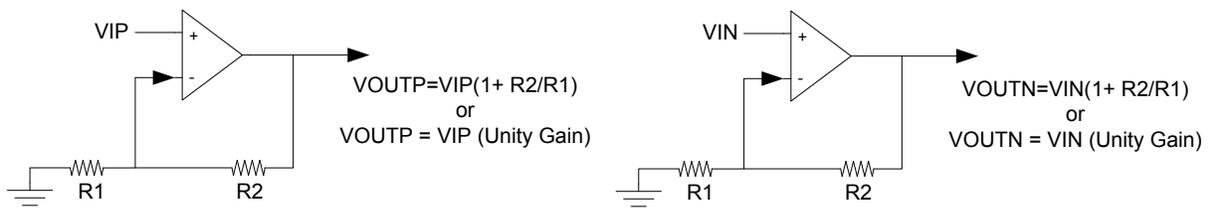


Figure 25.12. Dual Buffer ADC Driver Overview

Table 25.14. Dual Buffer ADC Driver Configuration

| OPA  | OPA Bitfields | OPA Configuration    |
|------|---------------|----------------------|
| OPAx | POSSEL        | POSPADx, APORT[1-4]X |
| OPAx | NEGSEL        | OPATAP               |
| OPAx | RESINMUX      | VSS                  |

### 25.3.5 Opamp VDACC Combination

Since two of the OPAMPs are part of the VDACC, it is not possible to use both VDACC channels and all 3 OPAMPs at the same time. If both VDACC channels are used, OPA0 and OPA1 can not be used as stand-alone opamp. However, it is possible to use one of the VDACC channels in combination with OPA0 or OPA1. OPA1 is available when VDACC channel 0 is in use, and OPA0 is available when VDACC channel 1 is used.

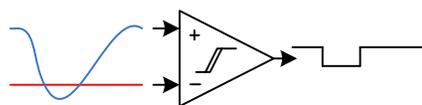
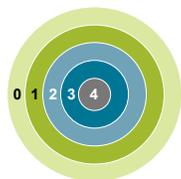
## 25.4 Register Map

The register map of the opamp can be found in [24.4 Register Map](#) in the VDAC chapter.

## 25.5 Register Description

The register description of the opamp can be found in [24.5 Register Description](#) in the VDAC chapter.

## 26. ACMP - Analog Comparator



### Quick Facts

#### What?

The Analog Comparator (ACMP) compares two analog signals and returns a digital value telling which is greater.

#### Why?

Applications often do not need to know the exact value of an analog signal, only if it has passed a certain threshold. Often the voltage must be monitored continuously, which requires extremely low power consumption.

#### How?

Available down to Energy Mode 3 and using as little as 100 nA, the ACMP can wake up the system when input signals pass the threshold. The analog comparator can compare two analog signals or one analog signal and a highly configurable internal reference.

### 26.1 Introduction

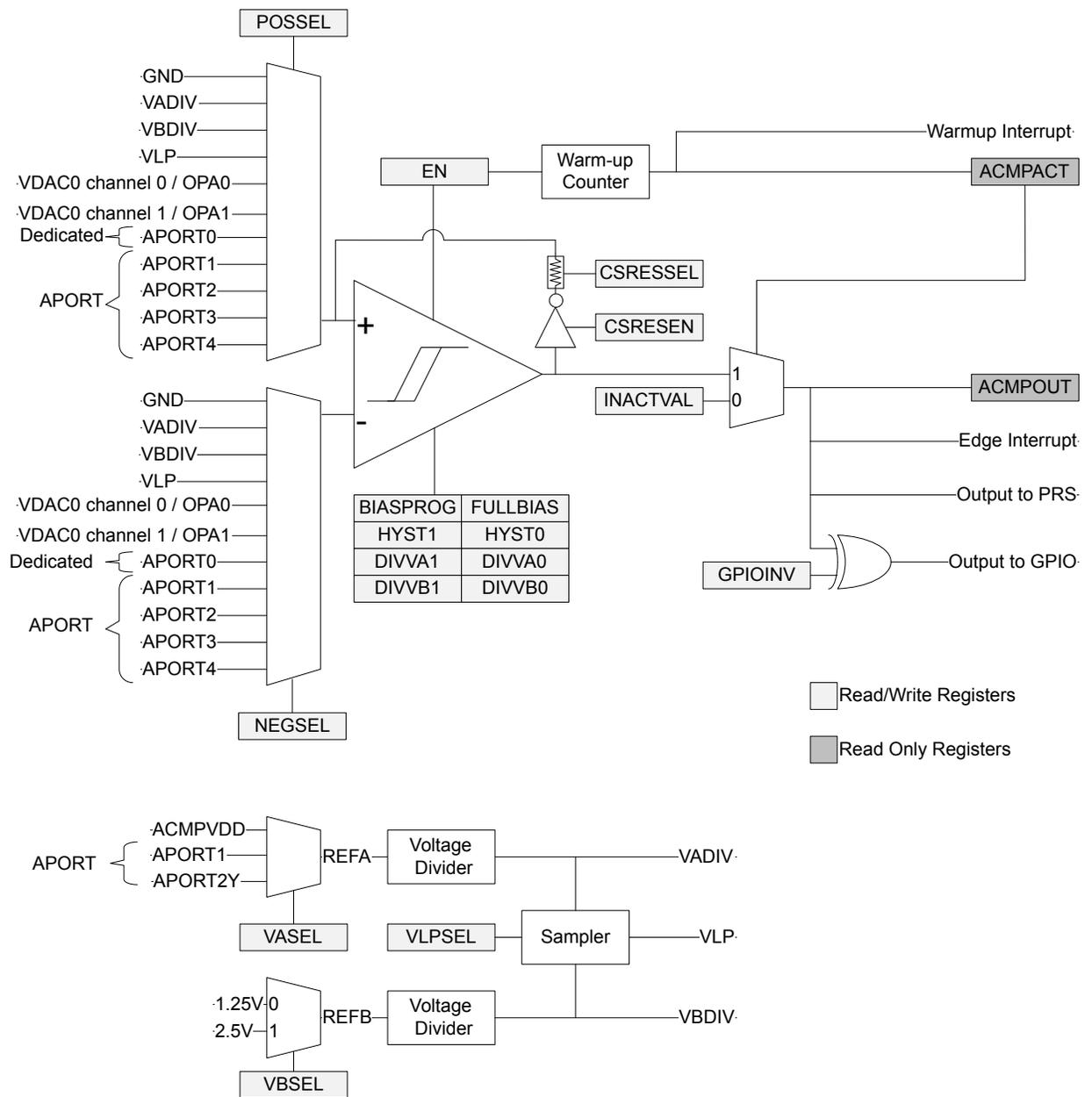
The Analog Comparator compares the voltage of two analog inputs and outputs a digital signal indicating which input voltage is higher. Inputs can either be from internal references or from external pins. Response time, and thereby the current consumption, can be configured by altering the current supply to the comparator.

## 26.2 Features

- Up to 160 selectable external I/O inputs for both positive and negative inputs
  - Up to 48 I/O can be used as a dividable reference
- 5 selectable internal inputs
  - VDAC channel 0 voltage as a reference
  - VDAC channel 1 voltage as a reference
  - Dividable Internal 1.25 V bandgap reference voltage
  - Dividable Internal 2.5 V bandgap reference voltage
  - Dividable  $V_{ACMPVDD}$  reference voltage
- Voltage supply monitoring
- Low power mode for internal  $V_{DD}$  and bandgap references
- Selectable hysteresis
  - 8 values
  - Values can be positive or negative
  - Dividable references have scale for both both output values, allowing for even larger hysteresis
- Selectable response time
- Asynchronous interrupt generation on selectable edges
  - Rising edge
  - Falling edge
  - Both edges
- Operational in EM0 Active down to EM3 Stop
- Dedicated capacitive sense mode with up to 8 inputs
  - Adjustable internal resistor
- Configurable output when inactive
- Comparator output direct on PRS
- Comparator output on GPIO through alternate functionality
  - Output inversion available

### 26.3 Functional Description

An overview of the ACMP is shown in [Figure 26.1 ACMP Overview on page 853](#).



**Figure 26.1. ACMP Overview**

The comparator has two analog inputs: one positive and one negative. When the comparator is active, the output indicates which of the two input voltages is higher. When the voltage on the positive input is higher than the voltage on the negative input, the digital output is high and vice versa.

The output of the comparator can be read in the ACMPOUT bit in ACMPn\_STATUS. It is possible to switch inputs while the comparator is enabled, but all other configuration should only be changed while the comparator is disabled.

#### 26.3.1 Power Supply

The comparator power supply ( $V_{ACMPVDD}$ ) can be configured to be AVDD, DVDD, or IOVDD using the PWRSEL bitfield in ACMPn\_CTRL. By default,  $V_{ACMPVDD}$  is set to AVDD.

### 26.3.2 Warm-up Time

The analog comparator is enabled by setting the EN bit in ACMPn\_CTRL. The comparator requires some time to stabilize after it is enabled. This time period is called the warm-up time. The warm-up period is self-timed and will complete within 5 $\mu$ s after EN is set.

During warm-up and when the comparator is disabled, the output level of the comparator is set to the value of the INACTVAL bit in ACMPn\_CTRL. When the warm-up time is over, the ACMPACT bit in ACMPn\_STATUS is set to 1 to indicate that the comparator is active.

An edge interrupt will be generated if the edge interrupt is enabled and the value set in INACTVAL differs from ACMPOUT when the comparator transitions from warm-up to active.

Software should wait until the warm-up period is over before entering EM2 or EM3, otherwise no comparator interrupts will be detected. EM1 can still be entered during warm-up. After the warm-up period is completed, interrupts will be detected in EM2 and EM3.

### 26.3.3 Response Time

There is a delay from when the input voltage changes polarity to when the output toggles. This delay is called the response time and can be altered by increasing or decreasing the bias current to the comparator through the BIASPROG and FULLBIAS fields in the ACMPn\_CTRL register. The current and speed of the circuit increase as the values of FULLBIAS and BIASPROG are increased from their minimum setting of FULLBIAS=0 BIASPROG=0b00000 to the maximum setting FULLBIAS=1 BIASPROG=0b11111 (maximum). The setting of FULLBIAS has a greater affect on current and speed than the setting of BIASPROG. See the part data sheet for specific current and response times related to the setting of these fields.

If FULLBIAS is set, to avoid glitches the highest hysteresis level should be used.

### 26.3.4 Hysteresis

When the hysteresis level is set to a non-zero value, the digital output will not toggle until the positive input voltage is at a voltage equal to the hysteresis level above or below the negative input voltage (see [Figure 26.3 Hysteresis on page 855](#) ). This feature can be used to avoid continual comparator output changes due to noise when the positive and negative inputs are nearly equal by requiring the input difference to exceed the hysteresis threshold.

In the analog comparator, hysteresis can be configured to 8 different levels. Level 0 is no hysteresis. Hysteresis is configured through the HYST field in ACMPn\_HYSTERESIS0 and ACMPn\_HYSTERESIS1 registers. The hysteresis value can be positive or negative. The comparator will output a 1 if:

$$POSSEL - NEGSEL > HYST$$

There are two hysteresis registers, ACMPn\_HYSTERESIS0 and ACMPn\_HYSTERESIS1, as the ACMP supports asymmetric hysteresis. ACMPn\_HYSTERESIS0 are the hysteresis values used when the comparator output is 0; ACMPn\_HYSTERESIS1 are the values used when the comparator output is 1. The user must set both registers to the same values if symmetric hysteresis is desired.

Along with the HYST field, the ACMPn\_HYSTERESIS0/1 registers include the DIVVA and DIVVB fields. This allows the user to implement even larger hysteresis when comparing against VADIV or VBDIV, as the reference voltage can vary with the comparator output, also.

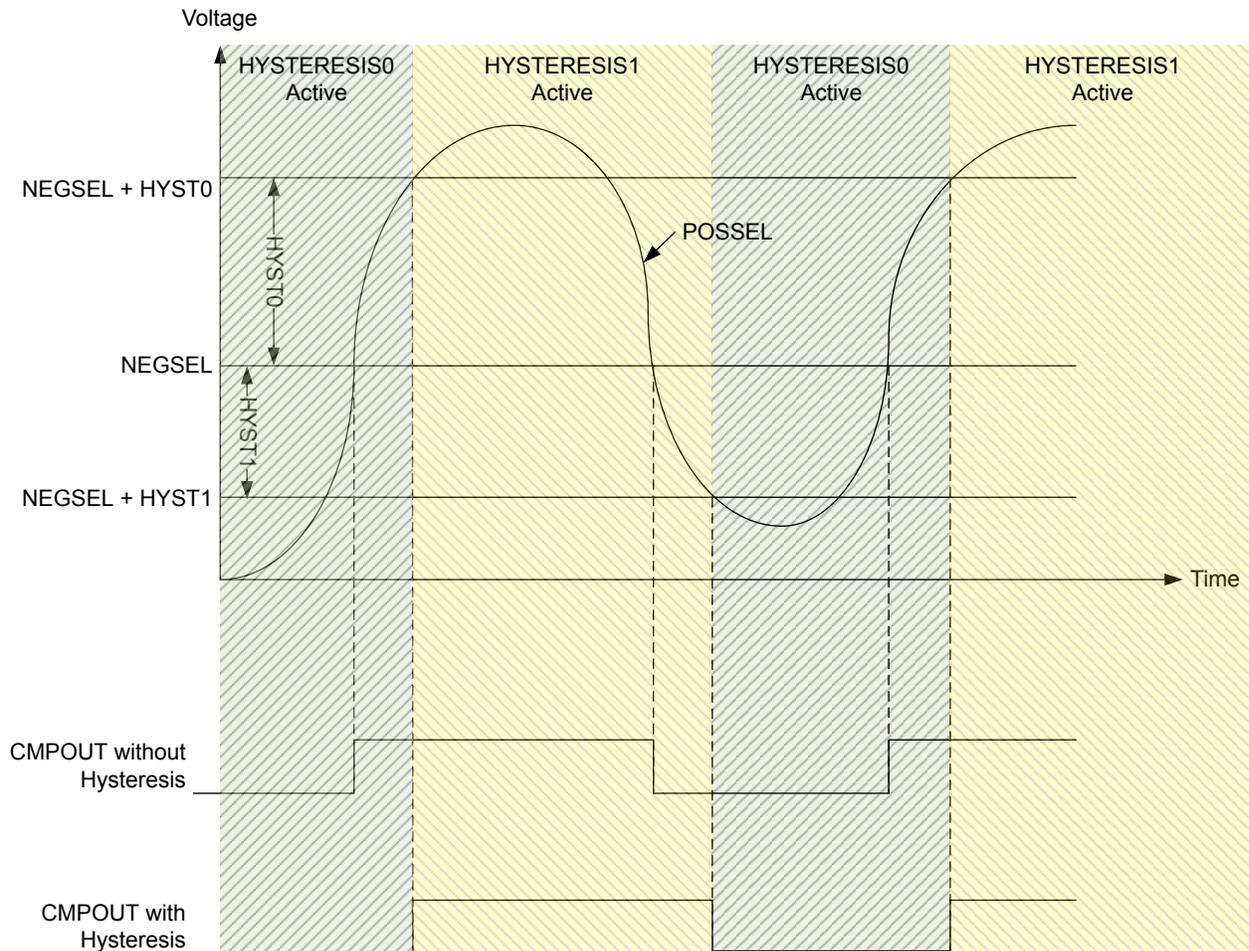


Figure 26.3. Hysteresis

### 26.3.5 Input Pin Considerations

For external ACMP inputs routed through the APORT, the maximum supported analog input voltage will be limited to the  $\text{MIN}(V_{\text{ACMPVDD}}, \text{IOVDD})$  (where  $V_{\text{ACMPVDD}}$  is selected by the PWRSEL bitfield in ACMPn\_CTRL). Note that pins configured as ACMP inputs should disable OVT (by setting the corresponding GPIO\_Px\_OVTDIS bit) to reduce any potential distortion introduced by the OVT circuitry.

### 26.3.6 Input Selection

The POSSEL and NEGSEL fields in ACMPn\_INPUTSEL control the input connections to the positive and negative inputs of the comparator. The user can select external GPIO pins on the chip, or select a number of internal chip voltages. Pins are selected by configuring channels on APORT buses. Not all selectable channels are available on a given device, as different devices within a family may not implement or bring out all of the I/O defined for that family. Refer to the data sheet for channel availability and pin mapping.

There are limitations on the POSSEL and NEGSEL connections that can be made. The user cannot select an X-bus for both POSSEL and NEGSEL simultaneously, nor a Y-bus for both POSSEL and NEGSEL simultaneously. The second limitation is that when using the feedback resistor only X-bus selections can be made for POSSEL. (The resistor only physically exists on the positive input of the comparator).

The user may also select from a number of internal voltages. VADIV and VBDIV are two dividable voltages. VADIV can be  $V_{\text{ACMPVDD}}$  divided, or the user can choose to select inputs from a number of APORT buses. VBDIV consists of two dividable band-gap references of either 1.25V or 2.5V. Each of these voltages have dividers in the ACMPn\_HYSTERESIS0/1 registers. The formula for the division of these voltages is:

$$\text{VADIV} = \text{VA} \cdot ((\text{DIVVA}+1) / 64)$$

**Figure 26.3. VA Voltage Division**

$$\text{VBDIV} = \text{VB} \cdot ((\text{DIVVB}+1) / 64)$$

**Figure 26.4. VB Voltage Division**

Either VADIV and VBDIV can also be used as an input to a lower power reference: VLP. Which of the two is used is configured via the VLPSEL field in ACMPn\_INPUTSEL. If the user selects VLP as an input source, then VADIV or VBDIV cannot be used as the source for the other input.

The POSSEL and NEGSEL fields also allow input from the on-chip VDAC channel 0 or VDAC channel 1.

ACMP can be configured to operate with a selected level of accuracy depending on the setting of ACCURACY in ACMPn\_CTRL. The default is low-accuracy mode where ACMP operates with lower accuracy but consumes less current. When higher accuracy is needed the user can set ACCURACY=1 at the cost of higher current consumption.

### 26.3.7 Capacitive Sense Mode

The analog comparator includes specialized hardware for capacitive sensing of passive push buttons. Such buttons are traces on the PCB laid out in a way that creates a parasitic capacitor between the button and the ground node. Because a human finger will have a small intrinsic capacitance to ground, the capacitance of the button will increase when the button is touched. The capacitance is measured by including the capacitor in a free-running RC oscillator (see [Figure 26.5 Capacitive Sensing Setup on page 858](#) ). The frequency produced will decrease when the button is touched compared to when it is not touched. By measuring the output frequency with a timer (via the PRS), the change in capacitance can be detected.

The analog comparator contains a feedback loop including an optional internal resistor. This resistor is enabled by setting the CSRESEN bit in ACMPn\_INPUTSEL. The resistance can be set to any of 8 values by configuring the CSRESSEL bits in ACMPn\_INPUTSEL. The source for VADIV is set to  $V_{ACMPVDD}$  by setting field VASEL=0 in ACMPn\_INPUTSEL. The oscillation rails are defined by the VADIV fields in registers ACMPn\_HYSTERESIS0/1. The user should select VADIV as the source for NEGSEL, and APORTXCHc for POSSEL in ACMPn\_INPUTSEL. When enabled, the comparator output will oscillate between the rails defined by VADIV in ACMPn\_HYSTERESIS0/1.

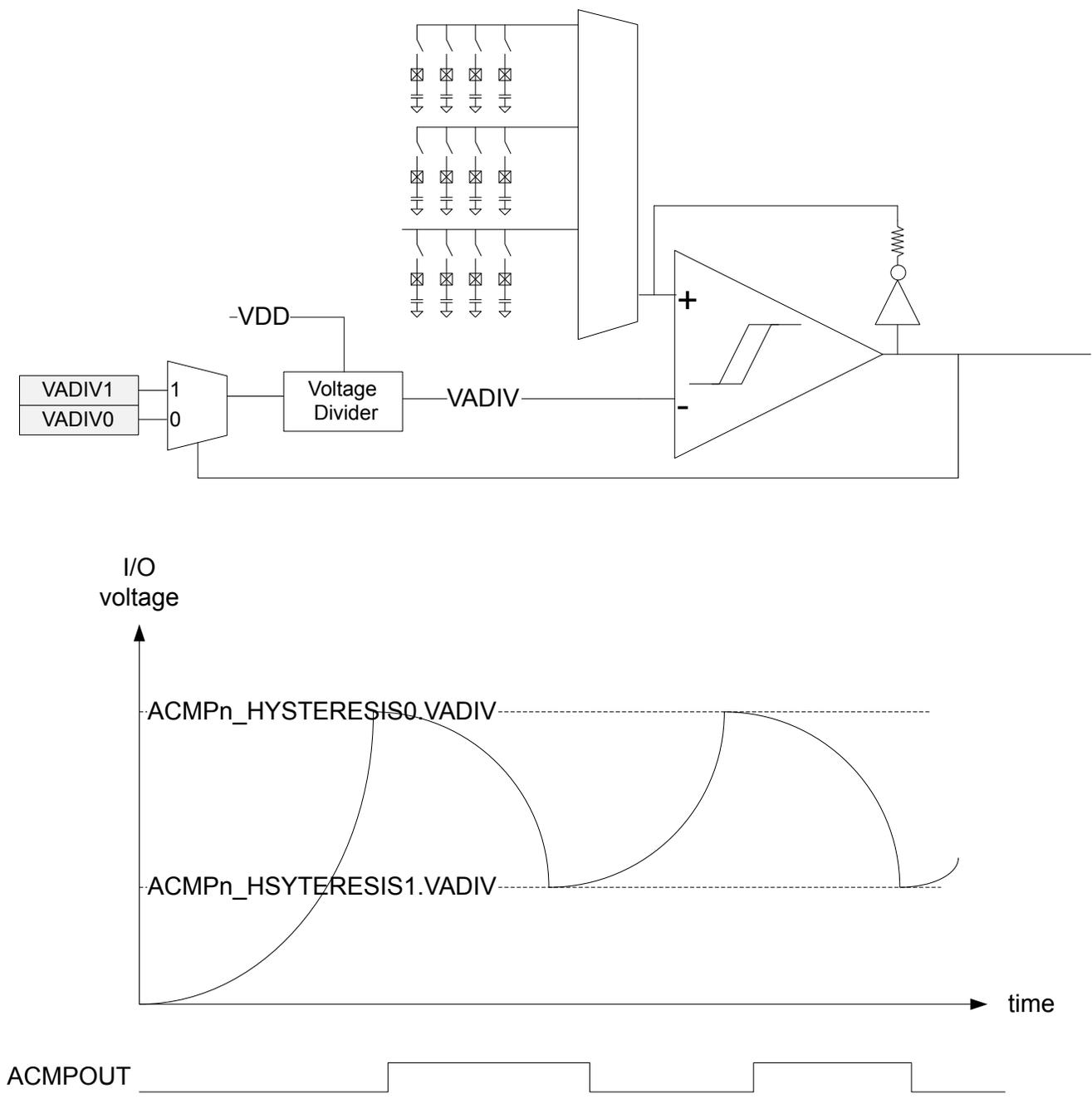


Figure 26.5. Capacitive Sensing Setup

### 26.3.8 Interrupts and PRS Output

The analog comparator includes an edge triggered interrupt flag (EDGE in ACMPn\_IF). If either IRISE and/or IFALL in ACMPn\_CTRL is set, the EDGE interrupt flag will be set on rising and/or falling edge of the comparator output respectively. An interrupt request will be sent if the EDGE interrupt flag in ACMPn\_IF is set and enabled through the EDGE bit in ACMPn\_IEN. The edge interrupt can also be used to wake up the device from EM3 Stop-EM1 Sleep.

The analog comparator includes the interrupt flag WARMUP in ACMPn\_IF which is set when a warm-up sequence has finished. An interrupt request will be sent if the WARMUP interrupt flag in ACMPn\_IF is set and enabled through the WARMUP bit in ACMPn\_IEN.

The analog comparator can also generate an interrupt if a bus conflict occurs. An interrupt request will be sent if the APORTCONFLICT interrupt flag in ACMPn\_IF is set and enabled through the APORTCONFLICT bit in ACMPn\_IEN.

The synchronized comparator output is also available as a PRS output signal.

### 26.3.9 Output to GPIO

The output from the comparator and the capacitive sense output are available as alternate functions to the GPIO pins. Set the ACMP-PEN bit in ACMPn\_ROUTE to enable the output to a pin and the LOCATION bits to select the output location. The GPIO-pin must also be set as output. The output to the GPIO can be inverted by setting the GPIOINV bit in ACMPn\_CTRL.

### 26.3.10 APORT Conflicts

The analog comparator connects to chip pins through APORT buses. It is possible that another APORT client is using a given APORT bus. To help debugging over-utilization of APORT resources the ACMP provides a number of status registers. The ACMPn\_APOR-TREQ gives the user visibility into what APORT buses the ACMP is requesting given the setting of registers ACMPn\_INPUTSEL and ACMPn\_CTRL. ACMPn\_APORTCONFLICT indicates if any of the selections are in conflict, internally or externally.

For example, if the user selects APORT1XCH0 for POSSEL and APORT3XCH1 for NEGSEL, then bits APORT1XCONFLICT and APORT3XCONFLICT would be 1 in register ACMPn\_APORTCONFLICT, as it is illegal for POSSEL and NEGSEL to both select an X-bus simultaneously.

If the user wishes the ACMP to monitor the same pin as another APORT client within the system, the ACMP can be configured to not attempt to control the switches on an APORT bus via the fields APORTXMASTERDIS, APOR TYMASTERDIS, and APORTVMAS-TERDIS in ACMPn\_CTRL. APORTXMASTERDIS and APOR TYMASTERDIS control if the X or Y bus selected via POSSEL or NEGSEL is mastered or not. APORTVMAS-TERDIS controls if either the X or Y bus selection of VASEL is mastered or not. When bus mastering is disabled, it is the other APORT client that determines which pin is connected to the APORT bus.

### 26.3.11 Supply Voltage Monitoring

The ACMP can be used to monitor supply voltages. The ACMP can select which voltage it uses via PWRSEL in ACMPn\_CTRL. This voltage can be selected for VADIV using VASEL=0 in ACMPn\_INPUTSEL and divided to a voltage with the band-gap reference range using DIVVA in registers ACMPn\_HYSTERESIS0/1. The band-gap reference voltage can also be scaled via DIVVB in registers ACMPn\_HYSTERESIS0/1 to provide a voltage higher or lower than the scaled VA voltage for comparison.

### 26.3.12 External Override Interface

The ACMP can be controlled by an external module, for instance LESENSE. In this mode, the external module will take control of the positive input mux control signal, which is normally controlled by ACMP\_INPUTSEL\_POSSEL. Only the APORTs are selectable for the positive input mux in this mode. Which APORT(s) used is configured in ACMP\_EXTIFCTRL\_APORTSEL.

ACMP\_EXTIFCTRL\_APORTSEL also controls the base value for the positive input mux control signal. The external module will be able to add an offset to this base. The resulting mux configuration can be calculated using [Figure 26.6 POSSEL in External Override Mode on page 860](#). The external module controls EXT\_OFFSET, while EXT\_BASE is controlled by ACMP. See register description of ACMP\_EXTIFCTRL\_APORTSEL to see values of EXT\_BASE.

$$\text{POSSEL} = \text{EXT\_BASE} + \text{EXT\_OFFSET}$$

**Figure 26.6. POSSEL in External Override Mode**

**Note:** If only one APORT in a pair is used, the external module needs to be programmed to only use the channels that the ACMP has control of.

The external module is also able to override DIVVA and DIVVB in ACMP\_HYSTERESIS0/HYSTERESIS1. This needs to be enabled in the external module. If the external module does not override DIVVA/DIVVB, the configuration in ACMP\_HYSTERESIS0/HYSTERESIS1 will be used.

To enable the external override interface these steps must be performed:

- Configure the parts of the ACMP that will not be overridden, i.e. everything except ACMP\_INPUTSEL\_POSSEL and possibly ACMP\_HYSTERESIS0/HYSTERESIS1. Make sure ACMP\_CTRL\_EN is set.
- Configure and enable the external override interface in ACMP\_EXTIFCTRL.
- Check for APORT conflicts in ACMP\_APORTCONFLICT.
- Wait for ACMP\_STATUS\_EXTIFACT to go high, indicating that the interface is ready to use.

## 26.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name                | Type  | Description                         |
|--------|---------------------|-------|-------------------------------------|
| 0x000  | ACMPn_CTRL          | RW    | Control Register                    |
| 0x004  | ACMPn_INPUTSEL      | RW    | Input Selection Register            |
| 0x008  | ACMPn_STATUS        | R     | Status Register                     |
| 0x00C  | ACMPn_IF            | R     | Interrupt Flag Register             |
| 0x010  | ACMPn_IFS           | W1    | Interrupt Flag Set Register         |
| 0x014  | ACMPn_IFC           | (R)W1 | Interrupt Flag Clear Register       |
| 0x018  | ACMPn_IEN           | RW    | Interrupt Enable Register           |
| 0x020  | ACMPn_APORTREQ      | R     | APORT Request Status Register       |
| 0x024  | ACMPn_APORTCONFLICT | R     | APORT Conflict Status Register      |
| 0x028  | ACMPn_HYSTERESIS0   | RW    | Hysteresis 0 Register               |
| 0x02C  | ACMPn_HYSTERESIS1   | RW    | Hysteresis 1 Register               |
| 0x040  | ACMPn_ROUTEPEN      | RW    | I/O Routing Pine Enable Register    |
| 0x044  | ACMPn_ROUTELOC0     | RW    | I/O Routing Location Register       |
| 0x048  | ACMPn_EXTIFCTRL     | RW    | External Override Interface Control |

## 26.5 Register Description

### 26.5.1 ACMPn\_CTRL - Control Register

| Offset        | Bit Position |    |    |    |          |    |    |    |    |    |       |       |            |    |    |    |          |    |    |        |    |    |    |                  |                  |                  |   |   |   |         |          |   |    |
|---------------|--------------|----|----|----|----------|----|----|----|----|----|-------|-------|------------|----|----|----|----------|----|----|--------|----|----|----|------------------|------------------|------------------|---|---|---|---------|----------|---|----|
| 0x000         | 31           | 30 | 29 | 28 | 27       | 26 | 25 | 24 | 23 | 22 | 21    | 20    | 19         | 18 | 17 | 16 | 15       | 14 | 13 | 12     | 11 | 10 | 9  | 8                | 7                | 6                | 5 | 4 | 3 | 2       | 1        | 0 |    |
| <b>Reset</b>  | 0            |    |    |    | 0x07     |    |    |    |    |    | 0     | 0     | 0x0        |    |    |    | 0        |    |    | 0x0    |    |    | 0  | 0                | 0                |                  |   |   |   | 0       | 0        |   | 0  |
| <b>Access</b> | RW           |    |    |    | RW       |    |    |    |    |    | RW    | RW    | RW         |    |    |    | RW       |    |    | RW     |    |    | RW | RW               | RW               |                  |   |   |   | RW      | RW       |   | RW |
| <b>Name</b>   | FULLBIAS     |    |    |    | BIASPROG |    |    |    |    |    | IFALL | IRISE | INPUTRANGE |    |    |    | ACCURACY |    |    | PWRSEL |    |    |    | APORTVMASSTERDIS | APORTYMASSTERDIS | APORTXMASSTERDIS |   |   |   | GPIOINV | INACTVAL |   | EN |

| Bit   | Name            | Reset   | Access | Description   |       |      |             |   |          |  |   |           |   |
|-------|-----------------|---|--------|---|-------|------|-------------|---|----------|--|---|-----------|---|
| 31    | FULLBIAS        | 0   | RW     | <b>Full Bias Current</b><br>Set this bit to 1 for full bias current. See the data sheet for details.  |       |      |             |   |          |  |   |           |   |
| 30    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |      |             |   |          |  |   |           |   |
| 29:24 | BIASPROG        | 0x07  | RW     | <b>Bias Configuration</b><br>These bits control the bias current level. See the data sheet for details.   |       |      |             |   |          |  |   |           |   |
| 23:22 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |      |             |   |          |  |   |           |   |
| 21    | IFALL           | 0   | RW     | <b>Falling Edge Interrupt Sense</b><br>Set this bit to 1 to set the EDGE interrupt flag on falling edges of comparator output.<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>DISABLED</td> <td>Interrupt flag is not set on falling edges</td> </tr> <tr> <td>1</td> <td>ENABLED</td> <td>Interrupt flag is set on falling edges</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | DISABLED | Interrupt flag is not set on falling edges       | 1 | ENABLED   | Interrupt flag is set on falling edges                        |
| Value | Mode            | Description   |        |   |       |      |             |   |          |  |   |           |   |
| 0     | DISABLED        | Interrupt flag is not set on falling edges  |        |   |       |      |             |   |          |  |   |           |   |
| 1     | ENABLED         | Interrupt flag is set on falling edges  |        |   |       |      |             |   |          |  |   |           |   |
| 20    | IRISE           | 0   | RW     | <b>Rising Edge Interrupt Sense</b><br>Set this bit to 1 to set the EDGE interrupt flag on rising edges of comparator output.<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>DISABLED</td> <td>Interrupt flag is not set on rising edges</td> </tr> <tr> <td>1</td> <td>ENABLED</td> <td>Interrupt flag is set on rising edges</td> </tr> </tbody> </table>     | Value | Mode | Description | 0 | DISABLED | Interrupt flag is not set on rising edges        | 1 | ENABLED   | Interrupt flag is set on rising edges                         |
| Value | Mode            | Description   |        |   |       |      |             |   |          |  |   |           |   |
| 0     | DISABLED        | Interrupt flag is not set on rising edges   |        |   |       |      |             |   |          |  |   |           |   |
| 1     | ENABLED         | Interrupt flag is set on rising edges   |        |   |       |      |             |   |          |  |   |           |   |
| 19:18 | INPUTRANGE      | 0x0   | RW     | <b>Input Range</b><br>Adjust performance of the comparator for a given input voltage range.<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>FULL</td> <td>Setting when the input can be from 0 to ACMPVDD.</td> </tr> <tr> <td>1</td> <td>GTVDDDIV2</td> <td>Setting when the input will always be greater than ACMPVDD/2.</td> </tr> </tbody> </table>         | Value | Mode | Description | 0 | FULL     | Setting when the input can be from 0 to ACMPVDD. | 1 | GTVDDDIV2 | Setting when the input will always be greater than ACMPVDD/2. |
| Value | Mode            | Description   |        |   |       |      |             |   |          |  |   |           |   |
| 0     | FULL            | Setting when the input can be from 0 to ACMPVDD.  |        |   |       |      |             |   |          |  |   |           |   |
| 1     | GTVDDDIV2       | Setting when the input will always be greater than ACMPVDD/2.   |        |   |       |      |             |   |          |  |   |           |   |

| Bit   | Name                  | Reset   | Access   | Description   |
|-------|-----------------------|---|--|---|
|       | 2                     | LTVDDDIV2   |  | Setting when the input will always be less than ACMPVDD/2.  |
| 17:16 | <i>Reserved</i>       | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |   |
| 15    | ACCURACY              | 0   | RW   | <b>ACMP Accuracy Mode</b><br>Select between low and high accuracy mode of the comparator. Note, high frequency changes can cause the ACMP performance to degrade. For such uses, such as quickly scanning through multiple channels or setting the ACMP to oscillate for capacitive sense, this bit should be set to 1.   |
|       | Value                 | Mode  | Description  |   |
|       | 0                     | LOW   | ACMP operates in low-accuracy mode but consumes less current.  |   |
|       | 1                     | HIGH  | ACMP operates in high-accuracy mode but consumes more current. |   |
| 14:12 | PWRSEL                | 0x0   | RW   | <b>Power Select</b><br>Selects the power source for the ACMP(ACMPVDD). NOTE, this field should only be changed when the block is disabled (EN=0).   |
|       | Value                 | Mode  | Description  |   |
|       | 0                     | AVDD  | AVDD supply  |   |
|       | 1                     | DVDD  | DVDD supply  |   |
|       | 2                     | IOVDD0  | IOVDD/IOVDD0 supply  |   |
|       | 4                     | IOVDD1  | IOVDD1 supply (if part has two I/O voltages)                   |   |
| 11    | <i>Reserved</i>       | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |   |
| 10    | APORTVMAS-<br>TER-DIS | 0   | RW   | <b>APORT Bus Master Disable for Bus Selected By VASEL</b><br>Determines if the ACMP will request the X or Y APORT bus selected by VASEL. This bit allows multiple APORT connected devices to monitor the same APORT bus simultaneously by allowing the ACMP to not master the selected bus. When 1, the determination is expected to be from another peripheral, and the ACMP only passively looks at the bus. When 1, the selection of channel for a selected bus is ignored (the bus is not), and is whatever selection the external device mastering the bus has configured for the APORT bus. |
|       | Value                 | Description   |  |   |
|       | 0                     | Bus mastering enabled   |  |   |
|       | 1                     | Bus mastering disabled  |  |   |
| 9     | APORTYMAS-<br>TER-DIS | 0   | RW   | <b>APORT Bus Y Master Disable</b><br>Determines if the ACMP will request the APORT Y bus selected by POSSEL or NEGSEL. This bit allows multiple APORT connected devices to monitor the same APORT bus simultaneously by allowing the ACMP to not master the selected bus. When 1, the determination is expected to be from another peripheral, and the ACMP only passively looks at the bus. When 1, the selection of channel for a selected bus is ignored (the bus is not), and is whatever selection the external device mastering the bus has configured for the APORT bus.                   |
|       | Value                 | Description   |  |   |
|       | 0                     | Bus mastering enabled   |  |   |
|       | 1                     | Bus mastering disabled  |  |   |

| Bit   | Name             | Reset   | Access  | Description   |
|-------|------------------|---|---|---|
| 8     | APORTXMASTER-DIS | 0   | RW  | <b>APORT Bus X Master Disable</b><br><br>Determines if the ACMP will request the APORT X bus selected by POSSEL or NEGSEL. This bit allows multiple APORT connected devices to monitor the same APORT bus simultaneously by allowing the ACMP to not master the selected bus. When 1, the determination is expected to be from another peripheral, and the ACMP only passively looks at the bus. When 1, the selection of channel for a selected bus is ignored (the bus is not), and is whatever selection the external device mastering the bus has configured for the APORT bus. |
| Value |                  | Description   |   |   |
| 0     |                  | Bus mastering enabled   |   |   |
| 1     |                  | Bus mastering disabled  |   |   |
| 7:4   | <i>Reserved</i>  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |
| 3     | GPIOINV          | 0   | RW  | <b>Comparator GPIO Output Invert</b><br><br>Set this bit to 1 to invert the comparator alternate function output to GPIO.   |
| Value |                  | Mode  | Description                                   |   |
| 0     |                  | NOTINV  | The comparator output to GPIO is not inverted |   |
| 1     |                  | INV   | The comparator output to GPIO is inverted     |   |
| 2     | INACTVAL         | 0   | RW  | <b>Inactive Value</b><br><br>The value of this bit is used as the comparator output when the comparator is inactive.  |
| Value |                  | Mode  | Description                                   |   |
| 0     |                  | LOW   | The inactive value is 0                       |   |
| 1     |                  | HIGH  | The inactive state is 1                       |   |
| 1     | <i>Reserved</i>  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |
| 0     | EN               | 0   | RW  | <b>Analog Comparator Enable</b><br><br>Enable/disable analog comparator.  |

### 26.5.2 ACMPn\_INPUTSEL - Input Selection Register

| Offset        | Bit Position |    |          |    |    |         |    |        |    |       |    |    |       |    |    |    |    |    |    |        |    |    |   |   |   |   |   |   |        |   |   |   |  |
|---------------|--------------|----|----------|----|----|---------|----|--------|----|-------|----|----|-------|----|----|----|----|----|----|--------|----|----|---|---|---|---|---|---|--------|---|---|---|--|
| 0x004         | 31           | 30 | 29       | 28 | 27 | 26      | 25 | 24     | 23 | 22    | 21 | 20 | 19    | 18 | 17 | 16 | 15 | 14 | 13 | 12     | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3      | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    | 0x0      |    |    | 0       |    | 0      |    | 0     |    |    | 0x00  |    |    |    |    |    |    | 0x00   |    |    |   |   |   |   |   |   | 0x00   |   |   |   |  |
| <b>Access</b> |              |    | RW       |    |    | RW      |    | RW     |    | RW    |    |    | RW    |    |    |    |    |    |    | RW     |    |    |   |   |   |   |   |   | RW     |   |   |   |  |
| <b>Name</b>   |              |    | CSRESSEL |    |    | CSRESEN |    | VLPSEL |    | VBSEL |    |    | VASEL |    |    |    |    |    |    | NEGSEL |    |    |   |   |   |   |   |   | POSSEL |   |   |   |  |

| Bit   | Name            | Reset   | Access | Description   |       |      |             |   |       |  |   |       |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |
|-------|-----------------|---|--------|---|-------|------|-------------|---|-------|--|---|-------|--|---|------|--|---|------|--|---|------|--|---|------|--|---|------|--|---|------|--|
| 31    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |      |             |   |       |  |   |       |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |
| 30:28 | CSRESSEL        | 0x0   | RW     | <b>Capacitive Sense Mode Internal Resistor Select</b><br>These bits select the resistance value for the internal capacitive sense resistor. Resulting actual resistor values are given in the device data sheets.<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>0</td><td>RES0</td><td>Internal capacitive sense resistor value 0</td></tr> <tr><td>1</td><td>RES1</td><td>Internal capacitive sense resistor value 1</td></tr> <tr><td>2</td><td>RES2</td><td>Internal capacitive sense resistor value 2</td></tr> <tr><td>3</td><td>RES3</td><td>Internal capacitive sense resistor value 3</td></tr> <tr><td>4</td><td>RES4</td><td>Internal capacitive sense resistor value 4</td></tr> <tr><td>5</td><td>RES5</td><td>Internal capacitive sense resistor value 5</td></tr> <tr><td>6</td><td>RES6</td><td>Internal capacitive sense resistor value 6</td></tr> <tr><td>7</td><td>RES7</td><td>Internal capacitive sense resistor value 7</td></tr> </tbody> </table> | Value | Mode | Description | 0 | RES0  | Internal capacitive sense resistor value 0 | 1 | RES1  | Internal capacitive sense resistor value 1 | 2 | RES2 | Internal capacitive sense resistor value 2 | 3 | RES3 | Internal capacitive sense resistor value 3 | 4 | RES4 | Internal capacitive sense resistor value 4 | 5 | RES5 | Internal capacitive sense resistor value 5 | 6 | RES6 | Internal capacitive sense resistor value 6 | 7 | RES7 | Internal capacitive sense resistor value 7 |
| Value | Mode            | Description   |        |   |       |      |             |   |       |  |   |       |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |
| 0     | RES0            | Internal capacitive sense resistor value 0  |        |   |       |      |             |   |       |  |   |       |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |
| 1     | RES1            | Internal capacitive sense resistor value 1  |        |   |       |      |             |   |       |  |   |       |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |
| 2     | RES2            | Internal capacitive sense resistor value 2  |        |   |       |      |             |   |       |  |   |       |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |
| 3     | RES3            | Internal capacitive sense resistor value 3  |        |   |       |      |             |   |       |  |   |       |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |
| 4     | RES4            | Internal capacitive sense resistor value 4  |        |   |       |      |             |   |       |  |   |       |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |
| 5     | RES5            | Internal capacitive sense resistor value 5  |        |   |       |      |             |   |       |  |   |       |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |
| 6     | RES6            | Internal capacitive sense resistor value 6  |        |   |       |      |             |   |       |  |   |       |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |
| 7     | RES7            | Internal capacitive sense resistor value 7  |        |   |       |      |             |   |       |  |   |       |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |
| 27    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |      |             |   |       |  |   |       |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |
| 26    | CSRESEN         | 0   | RW     | <b>Capacitive Sense Mode Internal Resistor Enable</b><br>Enable/disable the internal capacitive sense resistor.   |       |      |             |   |       |  |   |       |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |
| 25    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |      |             |   |       |  |   |       |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |
| 24    | VLPSEL          | 0   | RW     | <b>Low-Power Sampled Voltage Selection</b><br>Select the input to the sampled voltage VLP<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>0</td><td>VADIV</td><td>VADIV</td></tr> <tr><td>1</td><td>VBDIV</td><td>VBDIV</td></tr> </tbody> </table>   | Value | Mode | Description | 0 | VADIV | VADIV                                      | 1 | VBDIV | VBDIV                                      |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |
| Value | Mode            | Description   |        |   |       |      |             |   |       |  |   |       |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |
| 0     | VADIV           | VADIV   |        |   |       |      |             |   |       |  |   |       |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |
| 1     | VBDIV           | VBDIV   |        |   |       |      |             |   |       |  |   |       |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |
| 23    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |      |             |   |       |  |   |       |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |   |      |  |

| Bit   | Name         | Reset | Access | Description  |
|-------|--------------|-------|--------|--|
| 22    | VBSEL        | 0     | RW     | <b>VB Selection</b><br>Select the input for the VB Divider |
|       | Value        | Mode  |        | Description  |
|       | 0            | 1V25  |        | 1.25V  |
|       | 1            | 2V5   |        | 2.50V  |
| 21:16 | VASEL        | 0x00  | RW     | <b>VA Selection</b><br>Select the input for the VA Divider |
|       | Mode         | Value |        | Description  |
|       | VDD          | 0x0   |        | ACMPVDD  |
|       | APOINT2YCH0  | 0x1   |        | APOINT2Y Channel 0   |
|       | APOINT2YCH2  | 0x3   |        | APOINT2Y Channel 2   |
|       | APOINT2YCH4  | 0x5   |        | APOINT2Y Channel 4   |
|       | ...          | ...   |        | ...  |
|       | APOINT2YCH30 | 0x1f  |        | APOINT2Y Channel 30  |
|       | APOINT1XCH0  | 0x20  |        | APOINT1X Channel 0   |
|       | APOINT1YCH1  | 0x21  |        | APOINT1Y Channel 1   |
|       | APOINT1XCH2  | 0x22  |        | APOINT1X Channel 2   |
|       | APOINT1YCH3  | 0x23  |        | APOINT1Y Channel 3   |
|       | APOINT1XCH4  | 0x24  |        | APOINT1X Channel 4   |
|       | APOINT1YCH5  | 0x25  |        | APOINT1Y Channel 5   |
|       | ...          | ...   |        | ...  |
|       | APOINT1XCH30 | 0x3e  |        | APOINT1X Channel 30  |
|       | APOINT1YCH31 | 0x3f  |        | APOINT1Y Channel 31  |
| 15:8  | NEGSEL       | 0x00  | RW     | <b>Negative Input Select</b><br>Select negative input.     |
|       | APOINT0XCH0  | 0x00  |        | Dedicated APOINT0X Channel 0                               |
|       | APOINT0XCH1  | 0x01  |        | Dedicated APOINT0X Channel 1                               |
|       | APOINT0XCH2  | 0x02  |        | Dedicated APOINT0X Channel 2                               |
|       | ...          | ...   |        | ...  |
|       | APOINT0XCH15 | 0x0f  |        | Dedicated APOINT0X Channel 15                              |
|       | APOINT0YCH0  | 0x10  |        | Dedicated APOINT0Y Channel 0                               |
|       | APOINT0YCH1  | 0x11  |        | Dedicated APOINT0Y Channel 1                               |
|       | APOINT0YCH2  | 0x12  |        | Dedicated APOINT0Y Channel 2                               |
|       | ...          | ...   |        | ...  |
|       | APOINT0YCH15 | 0x1f  |        | Dedicated APOINT0Y Channel 15                              |

| Bit | Name        | Reset | Access | Description          |
|-----|-------------|-------|--------|----------------------|
|     | APORT1XCH0  | 0x20  |        | APORT1X Channel 0    |
|     | APORT1YCH1  | 0x21  |        | APORT1Y Channel 1    |
|     | APORT1XCH2  | 0x22  |        | APORT1X Channel 2    |
|     | APORT1YCH3  | 0x23  |        | APORT1Y Channel 3    |
|     | APORT1XCH4  | 0x24  |        | APORT1X Channel 4    |
|     | APORT1YCH5  | 0x25  |        | APORT1Y Channel 5    |
|     | ...         | ...   |        | ...                  |
|     | APORT1XCH30 | 0x3e  |        | APORT1X Channel 30   |
|     | APORT1YCH31 | 0x3f  |        | APORT1Y Channel 31   |
|     | APORT2YCH0  | 0x40  |        | APORT2Y Channel 0    |
|     | APORT2XCH1  | 0x41  |        | APORT2X Channel 1    |
|     | APORT2YCH2  | 0x42  |        | APORT2Y Channel 2    |
|     | APORT2XCH3  | 0x43  |        | APORT2X Channel 3    |
|     | APORT2YCH4  | 0x44  |        | APORT2Y Channel 4    |
|     | APORT2XCH5  | 0x45  |        | APORT2X Channel 5    |
|     | ...         | ...   |        | ...                  |
|     | APORT2YCH30 | 0x5e  |        | APORT2Y Channel 30   |
|     | APORT2XCH31 | 0x5f  |        | APORT2X Channel 31   |
|     | APORT3XCH0  | 0x60  |        | APORT3X Channel 0    |
|     | APORT3YCH1  | 0x61  |        | APORT3Y Channel 1    |
|     | APORT3XCH2  | 0x62  |        | APORT3X Channel 2    |
|     | APORT3YCH3  | 0x63  |        | APORT3Y Channel 3    |
|     | APORT3XCH4  | 0x64  |        | APORT3X Channel 4    |
|     | APORT3YCH5  | 0x65  |        | APORT3Y Channel 5    |
|     | ...         | ...   |        | ...                  |
|     | APORT3XCH30 | 0x7e  |        | APORT3X Channel 30   |
|     | APORT3YCH31 | 0x7f  |        | APORT3Y Channel 31   |
|     | APORT4YCH0  | 0x80  |        | APORT4Y Channel 0    |
|     | APORT4XCH1  | 0x81  |        | APORT4X Channel 1    |
|     | APORT4YCH2  | 0x82  |        | APORT4Y Channel 2    |
|     | APORT4XCH3  | 0x83  |        | APORT4X Channel 3    |
|     | APORT4YCH4  | 0x84  |        | APORT4Y Channel 4    |
|     | APORT4XCH5  | 0x85  |        | APORT4X Channel 5    |
|     | ...         | ...   |        | ...                  |
|     | APORT4YCH30 | 0x9e  |        | APORT4Y Channel 30   |
|     | APORT4XCH31 | 0x9f  |        | APORT4X Channel 31   |
|     | DACOUT0     | 0xf2  |        | DAC Channel 0 Output |

| Bit | Name         | Reset | Access | Description  |
|-----|--------------|-------|--------|--|
|     | DACOUT1      | 0xf3  |        | DAC Channel 1 Output                                   |
|     | VLP          | 0xfb  |        | Low-Power Sampled Voltage                              |
|     | VBDIV        | 0xfc  |        | Divided VB Voltage                                     |
|     | VADIV        | 0xfd  |        | Divided VA Voltage                                     |
|     | VDD          | 0xfe  |        | ACMPVDD as selected via PWRSEL                         |
|     | VSS          | 0xff  |        | VSS  |
| 7:0 | POSSEL       | 0x00  | RW     | <b>Positive Input Select</b><br>Select positive input. |
|     | APOINT0XCH0  | 0x00  |        | Dedicated APOINT0X Channel 0                           |
|     | APOINT0XCH1  | 0x01  |        | Dedicated APOINT0X Channel 1                           |
|     | APOINT0XCH2  | 0x02  |        | Dedicated APOINT0X Channel 2                           |
|     | ...          | ...   |        | ...  |
|     | APOINT0XCH15 | 0x0f  |        | Dedicated APOINT0X Channel 15                          |
|     | APOINT0YCH0  | 0x10  |        | Dedicated APOINT0Y Channel 0                           |
|     | APOINT0YCH1  | 0x11  |        | Dedicated APOINT0Y Channel 1                           |
|     | APOINT0YCH2  | 0x12  |        | Dedicated APOINT0Y Channel 2                           |
|     | ...          | ...   |        | ...  |
|     | APOINT0YCH15 | 0x1f  |        | Dedicated APOINT0Y Channel 15                          |
|     | APOINT1XCH0  | 0x20  |        | APOINT1X Channel 0                                     |
|     | APOINT1YCH1  | 0x21  |        | APOINT1Y Channel 1                                     |
|     | APOINT1XCH2  | 0x22  |        | APOINT1X Channel 2                                     |
|     | APOINT1YCH3  | 0x23  |        | APOINT1Y Channel 3                                     |
|     | APOINT1XCH4  | 0x24  |        | APOINT1X Channel 4                                     |
|     | APOINT1YCH5  | 0x25  |        | APOINT1Y Channel 5                                     |
|     | ...          | ...   |        | ...  |
|     | APOINT1XCH30 | 0x3e  |        | APOINT1X Channel 30                                    |
|     | APOINT1YCH31 | 0x3f  |        | APOINT1Y Channel 31                                    |
|     | APOINT2YCH0  | 0x40  |        | APOINT2Y Channel 0                                     |
|     | APOINT2XCH1  | 0x41  |        | APOINT2X Channel 1                                     |
|     | APOINT2YCH2  | 0x42  |        | APOINT2Y Channel 2                                     |
|     | APOINT2XCH3  | 0x43  |        | APOINT2X Channel 3                                     |
|     | APOINT2YCH4  | 0x44  |        | APOINT2Y Channel 4                                     |
|     | APOINT2XCH5  | 0x45  |        | APOINT2X Channel 5                                     |
|     | ...          | ...   |        | ...  |
|     | APOINT2YCH30 | 0x5e  |        | APOINT2Y Channel 30                                    |
|     | APOINT2XCH31 | 0x5f  |        | APOINT2X Channel 31                                    |

| Bit | Name        | Reset | Access | Description                    |
|-----|-------------|-------|--------|--------------------------------|
|     | APORT3XCH0  | 0x60  |        | APORT3X Channel 0              |
|     | APORT3YCH1  | 0x61  |        | APORT3Y Channel 1              |
|     | APORT3XCH2  | 0x62  |        | APORT3X Channel 2              |
|     | APORT3YCH3  | 0x63  |        | APORT3Y Channel 3              |
|     | APORT3XCH4  | 0x64  |        | APORT3X Channel 4              |
|     | APORT3YCH5  | 0x65  |        | APORT3Y Channel 5              |
|     | ...         | ...   |        | ...                            |
|     | APORT3XCH30 | 0x7e  |        | APORT3X Channel 30             |
|     | APORT3YCH31 | 0x7f  |        | APORT3Y Channel 31             |
|     | APORT4YCH0  | 0x80  |        | APORT4Y Channel 0              |
|     | APORT4XCH1  | 0x81  |        | APORT4X Channel 1              |
|     | APORT4YCH2  | 0x82  |        | APORT4Y Channel 2              |
|     | APORT4XCH3  | 0x83  |        | APORT4X Channel 3              |
|     | APORT4YCH4  | 0x84  |        | APORT4Y Channel 4              |
|     | APORT4XCH5  | 0x85  |        | APORT4X Channel 5              |
|     | ...         | ...   |        | ...                            |
|     | APORT4YCH30 | 0x9e  |        | APORT4Y Channel 30             |
|     | APORT4XCH31 | 0x9f  |        | APORT4X Channel 31             |
|     | DACOUT0     | 0xf2  |        | DAC Channel 0 Output           |
|     | DACOUT1     | 0xf3  |        | DAC Channel 1 Output           |
|     | VLP         | 0xfb  |        | Low-Power Sampled Voltage      |
|     | VBDIV       | 0xfc  |        | Divided VB Voltage             |
|     | VADIV       | 0xfd  |        | Divided VA Voltage             |
|     | VDD         | 0xfe  |        | ACMPVDD as selected via PWRSEL |
|     | VSS         | 0xff  |        | VSS                            |



### 26.5.4 ACMPn\_IF - Interrupt Flag Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |        |    |    |      |   |   |   |   |   |   |   |   |   |  |  |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|----|--------|----|----|------|---|---|---|---|---|---|---|---|---|--|--|--|--|
| 0x00C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15            | 14 | 13 | 12     | 11 | 10 | 9    | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R             | 0  | 2  | R      | 0  | 1  | R    | 0 | 0 |   |   |   |   |   |   |   |  |  |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R             | 0  | 2  | R      | 0  | 1  | R    | 0 | 0 |   |   |   |   |   |   |   |  |  |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | APORTCONFLICT |    |    | WARMUP |    |    | EDGE |   |   |   |   |   |   |   |   |   |  |  |  |  |

| Bit  | Name          | Reset   | Access | Description   |
|------|---------------|---|--------|---|
| 31:3 | Reserved      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 2    | APORTCONFLICT | 0   | R      | <b>APORT Conflict Interrupt Flag</b><br>1 if any of the APORT BUSes being requested by the ACMPn are also being requested by another peripheral |
| 1    | WARMUP        | 0   | R      | <b>Warm-up Interrupt Flag</b><br>Indicates that the analog comparator warm-up period is finished.   |
| 0    | EDGE          | 0   | R      | <b>Edge Triggered Interrupt Flag</b><br>Indicates that there has been a rising or falling edge on the analog comparator output.                 |

### 26.5.5 ACMPn\_IFS - Interrupt Flag Set Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |        |    |    |      |   |   |   |   |   |   |   |   |   |  |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|----|--------|----|----|------|---|---|---|---|---|---|---|---|---|--|--|--|
| 0x010         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15            | 14 | 13 | 12     | 11 | 10 | 9    | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W1            | 0  | 2  | W1     | 0  | 1  | W1   | 0 | 0 |   |   |   |   |   |   |   |  |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W1            | 0  | 2  | W1     | 0  | 1  | W1   | 0 | 0 |   |   |   |   |   |   |   |  |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | APORTCONFLICT |    |    | WARMUP |    |    | EDGE |   |   |   |   |   |   |   |   |   |  |  |  |

| Bit  | Name          | Reset   | Access | Description  |
|------|---------------|---|--------|--|
| 31:3 | Reserved      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 2    | APORTCONFLICT | 0   | W1     | <b>Set APORTCONFLICT Interrupt Flag</b><br>Write 1 to set the APORTCONFLICT interrupt flag |
| 1    | WARMUP        | 0   | W1     | <b>Set WARMUP Interrupt Flag</b><br>Write 1 to set the WARMUP interrupt flag               |
| 0    | EDGE          | 0   | W1     | <b>Set EDGE Interrupt Flag</b><br>Write 1 to set the EDGE interrupt flag                   |

### 26.5.6 ACMPn\_IFC - Interrupt Flag Clear Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |               |        |       |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---------------|--------|-------|---|---|---|
| 0x014         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5             | 4      | 3     | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | 0             | 0      | 0     |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | (R)W1         | (R)W1  | (R)W1 |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | APORTCONFLICT | WARMUP | EDGE  |   |   |   |

| Bit  | Name          | Reset   | Access | Description   |
|------|---------------|---|--------|---|
| 31:3 | Reserved      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 2    | APORTCONFLICT | 0   | (R)W1  | <b>Clear APORTCONFLICT Interrupt Flag</b><br><br>Write 1 to clear the APORTCONFLICT interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 1    | WARMUP        | 0   | (R)W1  | <b>Clear WARMUP Interrupt Flag</b><br><br>Write 1 to clear the WARMUP interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).               |
| 0    | EDGE          | 0   | (R)W1  | <b>Clear EDGE Interrupt Flag</b><br><br>Write 1 to clear the EDGE interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                   |

### 26.5.7 ACMPn\_IEN - Interrupt Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |               |        |      |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---------------|--------|------|---|---|---|
| 0x018         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5             | 4      | 3    | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | 0             | 0      | 0    |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | RW            | RW     | RW   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | APORTCONFLICT | WARMUP | EDGE |   |   |   |

| Bit  | Name          | Reset   | Access | Description   |
|------|---------------|---|--------|---|
| 31:3 | Reserved      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 2    | APORTCONFLICT | 0   | RW     | <b>APORTCONFLICT Interrupt Enable</b><br>Enable/disable the APORTCONFLICT interrupt |
| 1    | WARMUP        | 0   | RW     | <b>WARMUP Interrupt Enable</b><br>Enable/disable the WARMUP interrupt               |
| 0    | EDGE          | 0   | RW     | <b>EDGE Interrupt Enable</b><br>Enable/disable the EDGE interrupt                   |

## 26.5.8 ACMPn\_APORTREQ - APORT Request Status Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |            |            |            |            |            |            |            |            |            |   |   |   |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x020         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13         | 12         | 11         | 10         | 9          | 8          | 7          | 6          | 5          | 4          | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R          | R          | R          | R          | R          | R          | R          | R          | R          | R          | R | R | R | R | R | R | R | R | R | R | R | R | R |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | APORT4YREQ | APORT4XREQ | APORT3YREQ | APORT3XREQ | APORT2YREQ | APORT2XREQ | APORT1YREQ | APORT1XREQ | APORT0YREQ | APORT0XREQ |   |   |   |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name       | Reset   | Access | Description  |
|-------|------------|---|--------|--|
| 31:10 | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 9     | APORT4YREQ | 0   | R      | <b>1 If the Bus Connected to APORT4Y is Requested</b><br>Reports if the bus connected to APORT4Y is being requested from the APORT |
| 8     | APORT4XREQ | 0   | R      | <b>1 If the Bus Connected to APORT4X is Requested</b><br>Reports if the bus connected to APORT4X is being requested from the APORT |
| 7     | APORT3YREQ | 0   | R      | <b>1 If the Bus Connected to APORT3Y is Requested</b><br>Reports if the bus connected to APORT3Y is being requested from the APORT |
| 6     | APORT3XREQ | 0   | R      | <b>1 If the Bus Connected to APORT3X is Requested</b><br>Reports if the bus connected to APORT3X is being requested from the APORT |
| 5     | APORT2YREQ | 0   | R      | <b>1 If the Bus Connected to APORT2Y is Requested</b><br>Reports if the bus connected to APORT2Y is being requested from the APORT |
| 4     | APORT2XREQ | 0   | R      | <b>1 If the Bus Connected to APORT2X is Requested</b><br>Reports if the bus connected to APORT2X is being requested from the APORT |
| 3     | APORT1YREQ | 0   | R      | <b>1 If the Bus Connected to APORT1X is Requested</b><br>Reports if the bus connected to APORT1X is being requested from the APORT |
| 2     | APORT1XREQ | 0   | R      | <b>1 If the Bus Connected to APORT2X is Requested</b><br>Reports if the bus connected to APORT2X is being requested from the APORT |
| 1     | APORT0YREQ | 0   | R      | <b>1 If the Bus Connected to APORT0Y is Requested</b><br>Reports if the bus connected to APORT0Y is being requested from the APORT |
| 0     | APORT0XREQ | 0   | R      | <b>1 If the Bus Connected to APORT0X is Requested</b><br>Reports if the bus connected to APORT0X is being requested from the APORT |

### 26.5.9 ACMPn\_APORTCONFLICT - APORT Conflict Status Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x024         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9               | 8               | 7               | 6               | 5               | 4               | 3               | 2               | 1               | 0               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R               | R               | R               | R               | R               | R               | R               | R               | R               | R               | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | APORT4YCONFLICT | APORT4XCONFLICT | APORT3YCONFLICT | APORT3XCONFLICT | APORT2YCONFLICT | APORT2XCONFLICT | APORT1YCONFLICT | APORT1XCONFLICT | APORT0YCONFLICT | APORT0XCONFLICT |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name            | Reset  | Access | Description  |
|-------|-----------------|--|--------|--|
| 31:10 | Reserved        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 9     | APORT4YCONFLICT | 0  | R      | <p><b>1 If the Bus Connected to APORT4Y is in Conflict With Another Peripheral</b></p> <p>Reports if the bus connected to APORT4Y is is also being requested by another peripheral</p> |
| 8     | APORT4XCONFLICT | 0  | R      | <p><b>1 If the Bus Connected to APORT4X is in Conflict With Another Peripheral</b></p> <p>Reports if the bus connected to APORT4X is is also being requested by another peripheral</p> |
| 7     | APORT3YCONFLICT | 0  | R      | <p><b>1 If the Bus Connected to APORT3Y is in Conflict With Another Peripheral</b></p> <p>Reports if the bus connected to APORT3Y is is also being requested by another peripheral</p> |
| 6     | APORT3XCONFLICT | 0  | R      | <p><b>1 If the Bus Connected to APORT3X is in Conflict With Another Peripheral</b></p> <p>Reports if the bus connected to APORT3X is is also being requested by another peripheral</p> |
| 5     | APORT2YCONFLICT | 0  | R      | <p><b>1 If the Bus Connected to APORT2Y is in Conflict With Another Peripheral</b></p> <p>Reports if the bus connected to APORT2Y is is also being requested by another peripheral</p> |
| 4     | APORT2XCONFLICT | 0  | R      | <p><b>1 If the Bus Connected to APORT2X is in Conflict With Another Peripheral</b></p> <p>Reports if the bus connected to APORT2X is is also being requested by another peripheral</p> |
| 3     | APORT1YCONFLICT | 0  | R      | <p><b>1 If the Bus Connected to APORT1X is in Conflict With Another Peripheral</b></p> <p>Reports if the bus connected to APORT1X is is also being requested by another peripheral</p> |
| 2     | APORT1XCONFLICT | 0  | R      | <p><b>1 If the Bus Connected to APORT1X is in Conflict With Another Peripheral</b></p> <p>Reports if the bus connected to APORT1X is is also being requested by another peripheral</p> |
| 1     | APORT0YCONFLICT | 0  | R      | <p><b>1 If the Bus Connected to APORT0Y is in Conflict With Another Peripheral</b></p> <p>Reports if the bus connected to APORT0Y is is also being requested by another peripheral</p> |

---

| Bit | Name            | Reset | Access | Description   |
|-----|-----------------|-------|--------|---|
| 0   | APORT0XCONFLICT | 0     | R      | <b>1 If the Bus Connected to APORT0X is in Conflict With Another Peripheral</b><br><br>Reports if the bus connected to APORT0X is is also being requested by another peripheral |

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### 26.5.10 ACMPn\_HYSTERESIS0 - Hysteresis 0 Register

| Offset        | Bit Position |    |    |    |    |       |    |    |    |    |    |    |    |    |    |       |    |    |    |    |     |    |   |   |   |      |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|-------|----|----|----|----|----|----|----|----|----|-------|----|----|----|----|-----|----|---|---|---|------|---|---|---|---|---|---|
| 0x028         | 31           | 30 | 29 | 28 | 27 | 26    | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16    | 15 | 14 | 13 | 12 | 11  | 10 | 9 | 8 | 7 | 6    | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    | 0x00  |    |    |    |    |    |    |    |    |    |       |    |    |    |    | 0x0 |    |   |   |   |      |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    | RW    |    |    |    |    |    |    |    |    |    |       |    |    |    |    | RW  |    |   |   |   |      |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    | DIVVB |    |    |    |    |    |    |    |    |    | DIVVA |    |    |    |    |     |    |   |   |   | HYST |   |   |   |   |   |   |

| Bit   | Name     | Reset   | Access | Description   |
|-------|----------|---|--------|---|
| 31:30 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 29:24 | DIVVB    | 0x00  | RW     | <b>Divider for VB Voltage When ACMPOUT=0</b><br>Divider to scale VB when ACMPOUT=0. $VBDIV = VB * (DIVVB+1)/64$ . |
| 23:22 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 21:16 | DIVVA    | 0x00  | RW     | <b>Divider for VA Voltage When ACMPOUT=0</b><br>Divider to scale VA when ACMPOUT=0. $VADIV = VA * (DIVVA+1)/64$ . |
| 15:4  | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 3:0   | HYST     | 0x0   | RW     | <b>Hysteresis Select When ACMPOUT=0</b>   |

Select hysteresis level when comparator output is 0. The hysteresis levels can vary, please see the electrical characteristics for the device for more information.

| Value | Mode   | Description       |
|-------|--------|-------------------|
| 0     | HYST0  | No hysteresis     |
| 1     | HYST1  | 14 mV hysteresis  |
| 2     | HYST2  | 25 mV hysteresis  |
| 3     | HYST3  | 30 mV hysteresis  |
| 4     | HYST4  | 35 mV hysteresis  |
| 5     | HYST5  | 39 mV hysteresis  |
| 6     | HYST6  | 42 mV hysteresis  |
| 7     | HYST7  | 45 mV hysteresis  |
| 8     | HYST8  | No hysteresis     |
| 9     | HYST9  | -14 mV hysteresis |
| 10    | HYST10 | -25 mV hysteresis |
| 11    | HYST11 | -30 mV hysteresis |
| 12    | HYST12 | -35 mV hysteresis |
| 13    | HYST13 | -39 mV hysteresis |
| 14    | HYST14 | -42 mV hysteresis |
| 15    | HYST15 | -45 mV hysteresis |

### 26.5.11 ACMPn\_HYSTERESIS1 - Hysteresis 1 Register

| Offset        | Bit Position |    |    |    |       |    |    |    |    |    |    |    |      |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |      |   |
|---------------|--------------|----|----|----|-------|----|----|----|----|----|----|----|------|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|------|---|
| 0x02C         | 31           | 30 | 29 | 28 | 27    | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19   | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1    | 0 |
| <b>Reset</b>  |              |    |    |    | 0x00  |    |    |    |    |    |    |    | 0x00 |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | 0x0  |   |
| <b>Access</b> |              |    |    |    | RW    |    |    |    |    |    |    |    | RW   |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | RW   |   |
| <b>Name</b>   |              |    |    |    | DIVVB |    |    |    |    |    |    |    | DIWA |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | HYST |   |

| Bit   | Name     | Reset  | Access | Description   |
|-------|----------|--|--------|---|
| 31:30 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 29:24 | DIVVB    | 0x00   | RW     | <b>Divider for VB Voltage When ACMPOUT=1</b><br>Divider to scale VB when ACMPOUT=1. $VBDIV = VB * (DIVVB+1)/64$ . |
| 23:22 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 21:16 | DIWA     | 0x00   | RW     | <b>Divider for VA Voltage When ACMPOUT=1</b><br>Divider to scale VA when ACMPOUT=1. $VADIV = VA * (DIWA+1)/64$ .  |
| 15:4  | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 3:0   | HYST     | 0x0  | RW     | <b>Hysteresis Select When ACMPOUT=1</b>   |

Select hysteresis level when comparator output is 1. The hysteresis levels can vary, please see the electrical characteristics for the device for more information.

| Value | Mode   | Description       |
|-------|--------|-------------------|
| 0     | HYST0  | No hysteresis     |
| 1     | HYST1  | 14 mV hysteresis  |
| 2     | HYST2  | 25 mV hysteresis  |
| 3     | HYST3  | 30 mV hysteresis  |
| 4     | HYST4  | 35 mV hysteresis  |
| 5     | HYST5  | 39 mV hysteresis  |
| 6     | HYST6  | 42 mV hysteresis  |
| 7     | HYST7  | 45 mV hysteresis  |
| 8     | HYST8  | No hysteresis     |
| 9     | HYST9  | -14 mV hysteresis |
| 10    | HYST10 | -25 mV hysteresis |
| 11    | HYST11 | -30 mV hysteresis |
| 12    | HYST12 | -35 mV hysteresis |
| 13    | HYST13 | -39 mV hysteresis |
| 14    | HYST14 | -42 mV hysteresis |
| 15    | HYST15 | -45 mV hysteresis |

26.5.12 ACMPn\_ROUTEPEM - I/O Routing Pine Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |        |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|--------|
| 0x040         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0      |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0      |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | RW     |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | OUTPEN |

| Bit  | Name     | Reset   | Access | Description  |
|------|----------|---|--------|--|
| 31:1 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 0    | OUTPEN   | 0   | RW     | <b>ACMP Output Pin Enable</b><br>Enable/disable analog comparator output to pin. |

## 26.5.13 ACMPn\_ROUTELOC0 - I/O Routing Location Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|---|---|---|---|---|---|---|---|---|---|
| 0x044         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11     | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00   |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW     |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | OUTLOC |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name            | Reset   | Access | Description |
|------|-----------------|---|--------|-------------|
| 31:6 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |             |

5:0    OUTLOC    0x00    RW    **I/O Location**

Decides the location of the OUT pin.

| Value | Mode  | Description |
|-------|-------|-------------|
| 0     | LOC0  | Location 0  |
| 1     | LOC1  | Location 1  |
| 2     | LOC2  | Location 2  |
| 3     | LOC3  | Location 3  |
| 4     | LOC4  | Location 4  |
| 5     | LOC5  | Location 5  |
| 6     | LOC6  | Location 6  |
| 7     | LOC7  | Location 7  |
| 8     | LOC8  | Location 8  |
| 9     | LOC9  | Location 9  |
| 10    | LOC10 | Location 10 |
| 11    | LOC11 | Location 11 |
| 12    | LOC12 | Location 12 |
| 13    | LOC13 | Location 13 |
| 14    | LOC14 | Location 14 |
| 15    | LOC15 | Location 15 |
| 16    | LOC16 | Location 16 |
| 17    | LOC17 | Location 17 |
| 18    | LOC18 | Location 18 |
| 19    | LOC19 | Location 19 |
| 20    | LOC20 | Location 20 |
| 21    | LOC21 | Location 21 |
| 22    | LOC22 | Location 22 |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
| 23  |      | LOC23 |        | Location 23 |
| 24  |      | LOC24 |        | Location 24 |
| 25  |      | LOC25 |        | Location 25 |
| 26  |      | LOC26 |        | Location 26 |
| 27  |      | LOC27 |        | Location 27 |
| 28  |      | LOC28 |        | Location 28 |
| 29  |      | LOC29 |        | Location 29 |
| 30  |      | LOC30 |        | Location 30 |
| 31  |      | LOC31 |        | Location 31 |

### 26.5.14 ACMPn\_EXTIFCTRL - External Override Interface Control

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |          |   |   |   |   |   |    |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|----------|---|---|---|---|---|----|---|
| 0x048         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7        | 6 | 5 | 4 | 3 | 2 | 1  | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x0      |   |   |   |   |   | 0  |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RW       |   |   |   |   |   | RW |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | APORTSEL |   |   |   |   |   | EN |   |

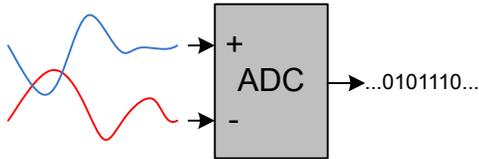
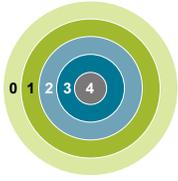
| Bit  | Name     | Reset  | Access | Description |
|------|----------|--|--------|-------------|
| 31:8 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |             |

7:4 APORTSEL      0x0      RW      **APORT Selection for External Interface**  
 Decides which APORT(s) the ACMP will use when controlled by an external module.

| Value | Mode     | Description   |
|-------|----------|---|
| 0     | APORT0X  | APORT0X used. EXT_BASE = ACMP_INPUTSEL_POSSEL_APORT0XCH0.   |
| 1     | APORT0Y  | APORT0Y used. EXT_BASE = ACMP_INPUTSEL_POSSEL_APORT0YCH0.   |
| 2     | APORT1X  | APORT1X used. EXT_BASE = ACMP_INPUTSEL_POSSEL_APORT1XCH0.   |
| 3     | APORT1Y  | APORT1Y used. EXT_BASE = ACMP_INPUTSEL_POSSEL_APORT1YCH0.   |
| 4     | APORT1XY | APORT1X/Y used. EXT_BASE = ACMP_INPUTSEL_POSSEL_APORT1XCH0. |
| 5     | APORT2X  | APORT2X used. EXT_BASE = ACMP_INPUTSEL_POSSEL_APORT2YCH0.   |
| 6     | APORT2Y  | APORT2Y used. EXT_BASE = ACMP_INPUTSEL_POSSEL_APORT2YCH0.   |
| 7     | APORT2YX | APORT2Y/X used. EXT_BASE = ACMP_INPUTSEL_POSSEL_APORT2YCH0. |
| 8     | APORT3X  | APORT3X used. EXT_BASE = ACMP_INPUTSEL_POSSEL_APORT3XCH0.   |
| 9     | APORT3Y  | APORT3Y used. EXT_BASE = ACMP_INPUTSEL_POSSEL_APORT3XCH0.   |
| 10    | APORT3XY | APORT3X/Y used. EXT_BASE = ACMP_INPUTSEL_POSSEL_APORT3XCH0. |
| 11    | APORT4X  | APORT4X used. EXT_BASE = ACMP_INPUTSEL_POSSEL_APORT4YCH0.   |
| 12    | APORT4Y  | APORT4Y used. EXT_BASE = ACMP_INPUTSEL_POSSEL_APORT4YCH0.   |
| 13    | APORT4YX | APORT4Y/X used. EXT_BASE = ACMP_INPUTSEL_POSSEL_APORT4YCH0. |

| Bit | Name     | Reset   | Access | Description   |
|-----|----------|---|--------|---|
| 3:1 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 0   | EN       | 0   | RW     | <b>Enable External Interface</b><br>Set to enable an external module, like LESENSE, to control the ACMP |

## 27. ADC - Analog to Digital Converter



### Quick Facts

#### What?

The ADC is used to convert analog signals into a digital representation and features low-power, autonomous operation.

#### Why?

In many applications there is a need to measure analog signals and record them in a digital representation, without exhausting the energy source.

#### How?

A low power ADC samples up to 32 input channels in a programmable sequence. With the help of PRS and DMA, the ADC can operate without CPU intervention in EM2 Deep Sleep and EM3 Stop, minimizing the number of powered up resources. The ADC can further be duty-cycled to reduce the energy consumption.

### 27.1 Introduction

The ADC uses a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second (1 Msp/s). The integrated input multiplexer can select from external I/Os and several internal signals.

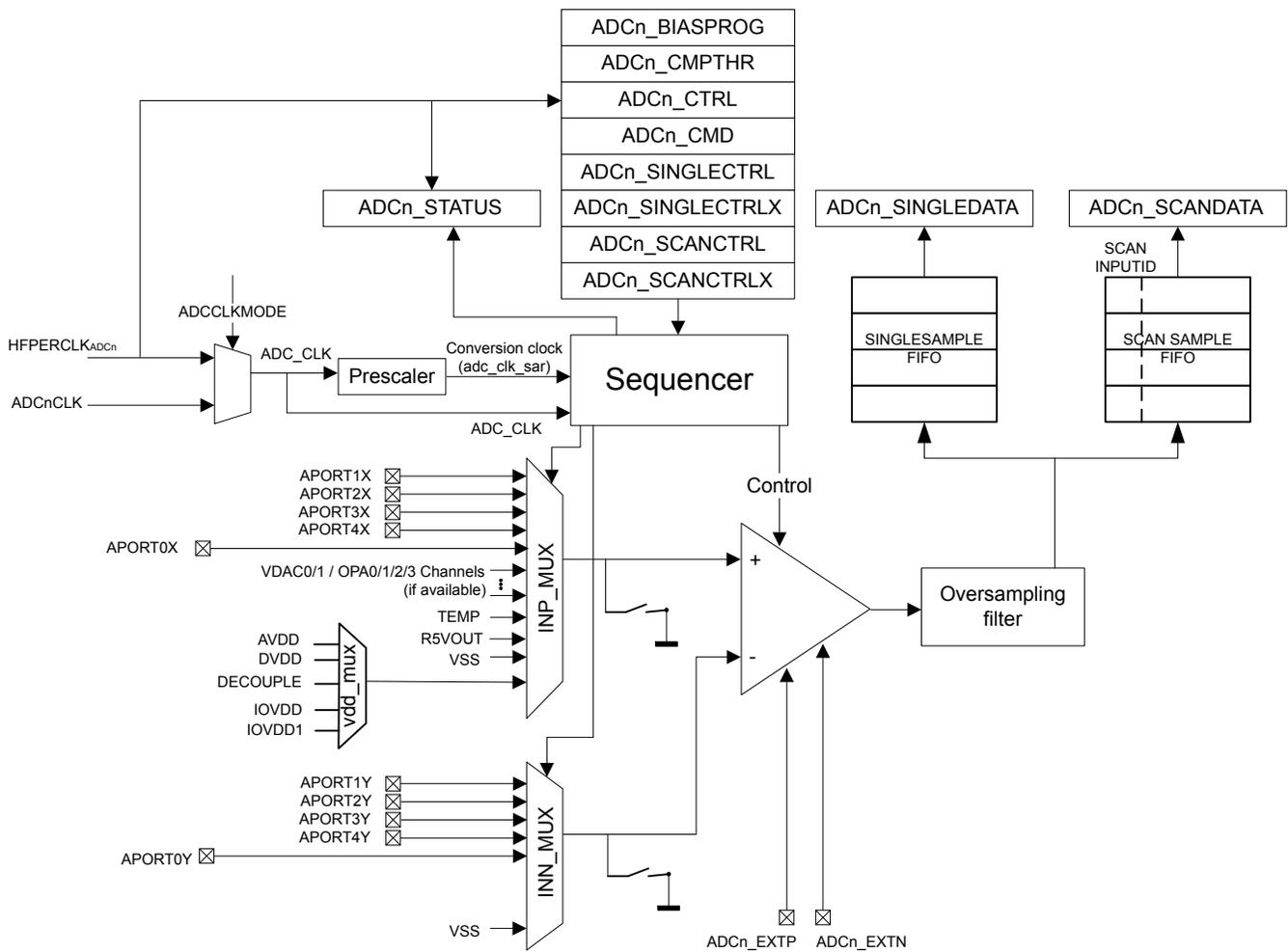
## 27.2 Features

- Programmable resolution (6/8/12-bit)
  - 13 conversion clock cycles for a 12-bit conversion
  - Maximum 1 Msps @ 12-bit
  - Maximum 1.6 Msps @ 6-bit
- Configurable acquisition time
- Externally controllable conversion start time using PRS in TIMED mode
- Integrated prescaler for conversion clock generation
  - Selectable clock division factor from 1 to 128
- Wide conversion clock range: 32 kHz to 16 MHz
- Can be run during EM2 Deep Sleep and EM3 Stop, waking up the system upon various enabled interrupts
- Can be run during EM2 Deep Sleep and EM3 Stop with DMA enabled to pull data from the FIFOs without waking up the system
- Supports up to 144 external input channels and several internal inputs
  - Includes temperature sensor and random number generator function
- Left or right adjusted results
  - Results in 2's complement representation
  - Differential results sign extended to 32-bits results
- Programmable scan sequence
  - Up to 32 configurable samples in scan sequence
  - Mask to select which pins are included in the sequence
  - Triggered by software or PRS input
  - One shot or repetitive mode
  - Oversampling available
  - Four deep FIFO to store conversion data along with channel ID and option to overwrite old data when full
  - Programmable watermark (DVL) to generate SCAN interrupt
  - Supports overflow and underflow interrupt generation
  - Supports window compare function
  - Conversion tailgating support for predictable periodic scans
- Programmable single channel conversion
  - Triggered by software or PRS input
  - Can be interleaved between two scan sequences
  - One shot or repetitive mode
  - Oversampling available
  - Four deep FIFO to store conversion data with option to overwrite old data when full
  - programmable watermark (DVL) to generate SINGLE interrupt
  - Supports overflow and underflow interrupt generation
  - Supports window compare function
- Hardware oversampling support
  - 1st order accumulate and dump filter
  - From 2 to 4096 oversampling ratio (OSR)
  - Results in 16-bit representation
  - Enabled individually for scan sequence and single channel mode
  - Common OSR select
- Programmable and preset input full scale (peak-to-peak) range (VFS) with selectable reference sources
  - VFS=1.25 V using internal VBGR reference
  - VFS=2.5 V using internal VBGR reference
  - VFS=AVDD with AVDD as reference source
  - VFS=5 V with internal VBGR reference
  - Single ended external reference
  - Differential external reference
  - VFS=2xAVDD with AVDD as reference source
  - User-programmable dividers for flexible VFS options from internal, external or supply voltage reference sources

- Support for offset and gain calibration
- Interrupt generation and/or DMA request when
  - Programmable number of converted data available in the single FIFO (also generates DMA request)
  - Programmable number of converted data available in the scan FIFO (also generates DMA request)
  - Single FIFO overflow or underflow
  - Scan FIFO overflow or underflow
  - Latest Single conversion tripped compare logic
  - Latest Scan conversion tripped compare logic
  - Analog over-voltage interrupt
  - Programming Error interrupt due to APORT Bus Request conflict or NEGSEL programming error

### 27.3 Functional Description

An overview of the ADC is shown in [Figure 27.1 ADC Overview on page 885](#).



**Figure 27.1. ADC Overview**

### 27.3.1 Clock Selection

The ADC logic is partitioned into two clock domains: HFPERCLK and ADC\_CLK. The HFPERCLK domain contains the register interface logic, APORT request logic and portions of FIFO read logic. The HFPERCLK is the default clock for the ADC peripheral. The rest of the ADC is clocked by the ADC\_CLK domain. The ADC\_CLK is chosen by ADCCLKMODE bit in the ADCn\_CTRL register.

The ADC\_CLK is the main clock for the ADC engine. If the ADCCLKMODE is set to SYNC, the ADC\_CLK is equal to the HFPERCLK and the ADC operates in synchronous mode. If the ADCCLKMODE is set to ASYNC, the ADC\_CLK is ASYNCCLK and the ADC operates in asynchronous mode. This distinction is important to understand as there are additional system restrictions and benefits to running the ADC in asynchronous mode detailed in [27.3.15 ASYNC ADC\\_CLK Usage Restrictions and Benefits](#).

**Note:** Whenever ADC is being used in asynchronous mode, then HFPERCLK must be at least 1.5 times higher than the ADC\_CLK.

The ADC has an internal clock prescaler, controlled by PRESC bits in ADCn\_CTRL, which can divide the ADC\_CLK by any factor between 1 and 128 to generate the conversion clock (adc\_clk\_sar) for the ADC. This adc\_clk\_sar is also used to generate acquisition timing. Note that the maximum clock frequency for adc\_clk\_sar is 16 MHz. The ADC warmup time is determined by ADC\_CLK and not by adc\_clk\_sar.

ASYNCCLK is a clock source from the CMU which is considered asynchronous to HFPERCLK. The CMU\_ADCCTRL register can be programmed to request and use ASYNCCLK. It has multiple choices for its source, including AUXHFRCO, HFXO and HFSRCCLK, and can optionally be inverted. If the chosen source for ASYNCCLK is not active at the time of request, the CMU enables the source oscillator upon receiving the request, and shuts down the oscillator when the ADC stops requesting the clock. Consult the CMU chapter for details of how to program the clock sources for the ASYNCCLK and oscillator start-up time details.

Software may choose a clock request generation scheme by programming the ASYNCCLKEN and WARMMODE of the ADCn\_CTRL register. If the ASYNCCLKEN is set to ASNEEDED with WARMMODE set to NORMAL, the ADC requests ASYNCCLK only when a conversion trigger is activated. The ASYNCCLK request is withdrawn after the conversion is complete. All other options keep the ASYNCCLK request "ON" until software programs these fields otherwise or changes the ADCCLKMODE to SYNC.

For EM2 Deep Sleep or EM3 Stop operation of the ADC, the ADC\_CLK must be configured for AUXHFRCO as this is the only available option during EM2 Deep Sleep or EM3 Stop. The ADC\_CLK source should not be changed as the system enters or exits various energy modes, otherwise measurement inaccuracies will result.

### 27.3.2 Conversions

A conversion consists of two phases: acquisition and approximation. The input is sampled in the acquisition phase before it is converted to digital representation during the approximation phase. The acquisition time can be configured independently for scan sequence and single channel conversions (see [27.3.3 ADC Modes](#)) by setting AT in ADCn\_SINGLECTRL/ADCn\_SCANCTRL. The acquisition times can be set to 1, 2, 3 or any integer power of 2 from 4 to 256 adc\_clk\_sar cycles.

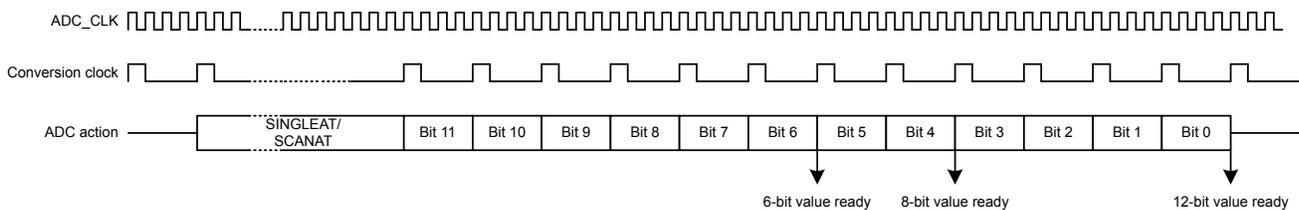
**Note:** For high impedance sources the acquisition time should be adjusted to allow enough time for the internal sample capacitor to fully charge. The minimum acquisition time for sampling at 1 Msps and typical input loading is 187.5 ns.

The ADC uses one adc\_clk\_sar cycle per output bit in the approximation phase plus 1 extra adc\_clk\_sar cycle.

$$T_{conv} = (T_{acq} + (N + 1) \times T_{adc\_clk\_sar}) \times OVSRSEL$$

Where  $T_{acq}$  is the acquisition time set by the AT bit field, N is the resolution (in bits), and OVSRSEL is the oversampling ratio according to the OVSRSEL field in ADCn\_CTRL when oversampling is enabled (see [27.3.10.6 Oversampling](#)).

**Figure 27.2. ADC Total Conversion Time Per Output**



**Figure 27.3. ADC Conversion Timing**

### 27.3.3 ADC Modes

The ADC contains two programmable modes: single channel mode and scan mode. Both modes have separate configuration registers and a four-deep FIFO for conversion results. Both modes may be set up to run only once per trigger or to automatically repeat after each operation. The scan mode has priority over the single channel mode. However by default, if scan sequence is running, a triggered single channel conversion will be interleaved between two scan samples.

#### 27.3.3.1 Single Channel Mode

Single channel mode can be used to convert a single channel either once per trigger or repetitively. The configuration of single channel mode is done using the `ADCn_SINGLECTRL` and `ADCn_SINGLECTRLX` registers and the result FIFO can be read through the `ADCn_SINGLEDATA` register. The `DVL` field of the `ADCn_SINGLECTRLX` controls the FIFO watermark crossing which sets the `SINGLEEDV` bit in `ADCn_STATUS` high and is cleared when the data is read and the number of unread data samples falls below the `DVL` threshold. The user can choose to throw out new samples or overwrite the old samples when the FIFO becomes full by programming the `FIFOFACT` field of the `ADCn_SINGLECTRLX` register. Single channel results can also be read through `ADCn_SINGLEDATAP` without popping the FIFO, returning its latest element. The `DIFF` field in `ADCn_SINGLECTRL` selects whether differential or single ended inputs are used and `POSSEL` and `NEGSEL` selects the input signal(s). The `CMPEN` bit in the `ADCn_SINGLECTRL` register enables the window compare function, and the latest converted data is compared against values programmed into the `ADGT` and `ADLT` fields of the `ADCn_CMPTHR` register and generates `SINGLECMP` interrupts if enabled. The window compare function allows for compare triggering both within (if `ADGT` less than `ADLT`) or out of (if `ADGT` greater than `ADLT`) window.

#### 27.3.3.2 Scan Mode

Scan mode is used to perform conversions across multiple channels, sweeping a set of selected inputs in a sequence. The configuration of scan mode is done in the `ADCn_SCANCTRL` and `ADCn_SCANCTRLX` registers. It has similar controls and data read mechanisms to single channel mode. There are two key differences between single channel mode and scan mode: the input sequence is programmed differently, and it has additional information in the result to indicate the channel on which the conversion was acquired. [27.3.7 Input Selection](#) explains how the input sequence is chosen. When the scan sequence is triggered, the ADC samples all inputs that are included in the mask (`ADCn_SCANMASK`), starting at the lowest pin number. `DIFF` in `ADCn_SCANCTRL` selects whether single ended or differential inputs are used. The FIFO data is tagged with `SCANINPUTID` and can be read along with the scan data using `ADCn_SCANDATAAX` register. The `ADCn_SCANDATAXP` can be used to read the latest valid entry from the scan FIFO without popping it. There is also a `ADCn_SCANDATA` register that contains results without the `SCANINPUTID` appended.

**Note:** If using scan mode with `ADCn_SCANCTRL_REP = 1` and `ADCn_SCANCTRLX_REPDELAY = NODELAY`, the last channel in the scan will report a `SCANINPUTID` of 0. Using `ADCn_SCANCTRLX_REPDELAY` with any value other than `NODELAY` will report the correct `SCANINPUTID`.

### 27.3.4 Warm-up Time

After power-on, the ADC requires some time for internal bias currents and references to settle prior to starting a conversion. This time period is called the warm-up time. Warm-up timing is performed by hardware. Software must program the number of ADC\_CLK cycles required to count at least 1  $\mu$ s in the TIMEBASE field of the ADCn\_CTRL register. TIMEBASE only affects the timing of the warm-up sequence and is not dependent on adc\_clk\_sar. When enabling the ADC or changing references between samples, the ADC is automatically warmed up for 5  $\mu$ s (5 times the period indicated by TIMEBASE).

Normally, the ADC will be warmed up only when samples are requested and is shut off when there are no more samples waiting. However, if lower latency is needed, configuring the WARMUPMODE field in ADCn\_CTRL allows the ADC and/or reference to stay warm between samples, reducing the warm-up time or eliminating it altogether. [Figure 27.4 ADC Analog Power Consumption With Different WARMUPMODE Settings on page 889](#) shows the effects on analog power consumption in scenarios using different WARMUPMODE settings.

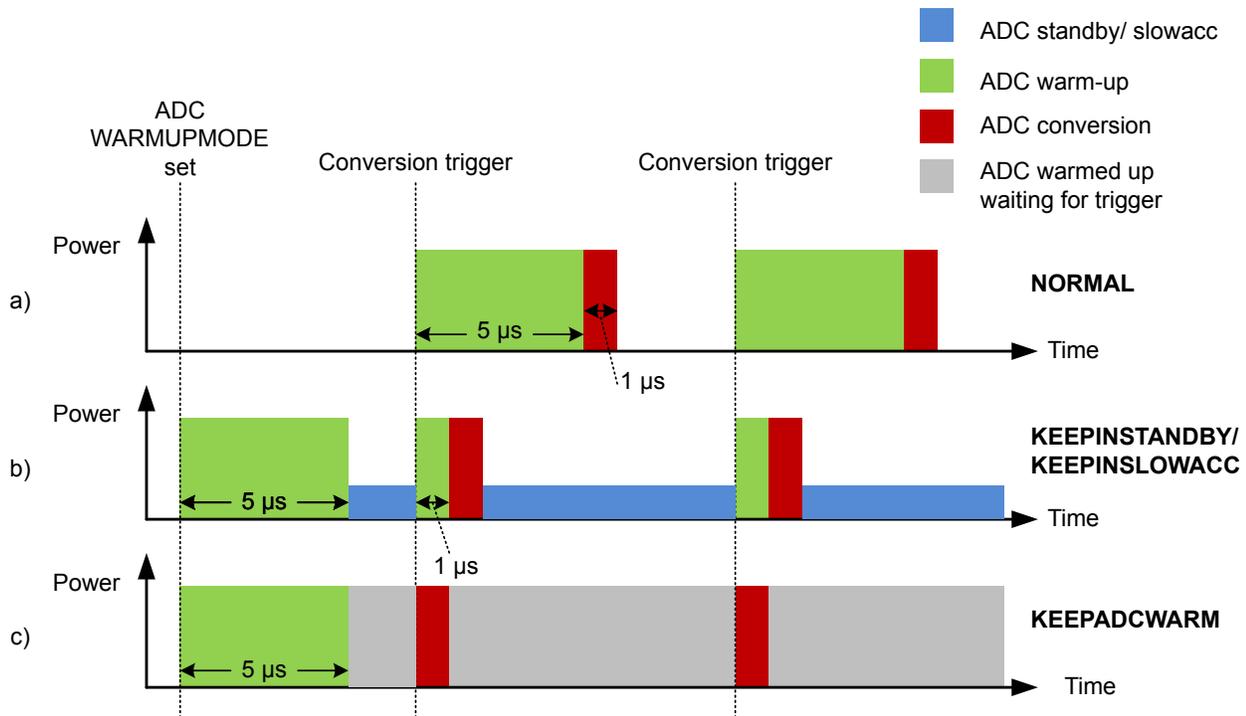
The user can program which reference should be kept warm in the CHCONREFWARMIDLE bitfield in the ADCn\_CTRL register. By default the scan mode reference is kept warm. The user can also choose to keep the single channel mode reference warm or to keep the last used reference warm. If the default setting is kept (scan mode reference is to be kept warm) and if the single-mode reference setting is different than scan-mode, then single mode conversions will first warmup its reference for 5  $\mu$ s before a conversion can begin.

Various warmup modes are described here:

- **NORMAL:** This is the lowest power option for general-purpose use and low sampling rates (below 35 ksps). The ADC and references are shut off when there are no samples waiting. The ADC does not consume any power when it is shut down. A 5  $\mu$ s warmup time will be initiated prior to every conversion. Figure a in [Figure 27.4 ADC Analog Power Consumption With Different WARMUPMODE Settings on page 889](#) shows this mode.
- **KEEPINSTANDBY:** This mode is suitable for infrequent sampling of lower impedance inputs, and is the lowest power option for sampling rates between about 35 and 125 ksps. It may also be useful for lower sampling rates where latency is important. The reference selected for scan mode is kept warm, but the ADC is powered down. The ADC will initiate a 1  $\mu$ s warmup period before a conversion begins. Because the reference is kept warm, the ADC will consume a small amount of standby current when it is not converting. Figure b in [Figure 27.4 ADC Analog Power Consumption With Different WARMUPMODE Settings on page 889](#) shows this mode.
- **KEEPINSLOWACC:** This mode is useful for high-impedance inputs which are sampled infrequently. It is similar to KEEPINSTANDBY, but continuously tracks the input, keeping the input multiplexer connected to the APORT bus. This mode consumes little more power than KEEPINSTANDBY mode (about 2  $\mu$ A extra) when a conversion is not in progress. This allows the user to avoid programming long acquisition time that would otherwise be necessary for high-impedance inputs when ADC wakes up to full power mode, thereby reducing the total current consumption per conversion.
- **KEEPADCWARM:** This mode provides the lowest latency and allows for maximum sampling rates. The ADC and reference circuitry remain powered on even when conversions are not in progress. Figure c in [Figure 27.4 ADC Analog Power Consumption With Different WARMUPMODE Settings on page 889](#) shows this mode. This mode consumes the most power, but as soon as a trigger event occurs, the acquisition and conversion begin with no warm-up time. Note that if KEEPADCWARM mode is set and HFXO is selected as the ADC clock source, the HFXO will remain on in EM2.

When KEEPADCWARM is chosen, ADC is termed as being in continuous operation. When any other warmup mode is chosen, ADC is termed to be in duty-cycled operation.

When entering EM2 Deep Sleep or EM3 Stop, if the ADC is not going to be used, it should be returned to an idle state and WARMUPMODE in ADCn\_CTRL written to 0. Refer to [27.3.17 ADC Programming Model](#) for more information on placing the ADC in an idle state. If the ADC is going to be used in these low energy modes, the user can use any of the WARMUPMODE settings, but should be mindful of the power consumption that comes along with the different mode settings. For EM2 Deep Sleep or EM3 Stop operation, the ADC clock source must be configured to use AUXHFRCO.



**Figure 27.4. ADC Analog Power Consumption With Different WARMUPMODE Settings**

**Note:** When using any warm-up mode other than NORMAL, always switch back to the NORMAL mode before switching to another warm-up mode.

### 27.3.5 Power Supply

The ADC block power ( $V_{ADC}$ ) is derived from the VDDX\_ANA supply rail. VDDX\_ANA can be selected from the AVDD or DVDD supply pins using the EMU\_PWRCTRL\_ANASW bit field.

### 27.3.6 Input Pin Considerations

For external ADC inputs routed through the APORT, the maximum supported analog input voltage will be limited to the  $\text{MIN}(V_{ADC}, \text{IOVDD})$  (where  $V_{ADC}$  is VDDX\_ANA, as described in 27.3.5 Power Supply). Note that pins configured as ADC inputs should disable OVT (by setting the corresponding GPIO\_Px\_OVTDIS bit) to reduce any potential distortion introduced by the OVT circuitry.

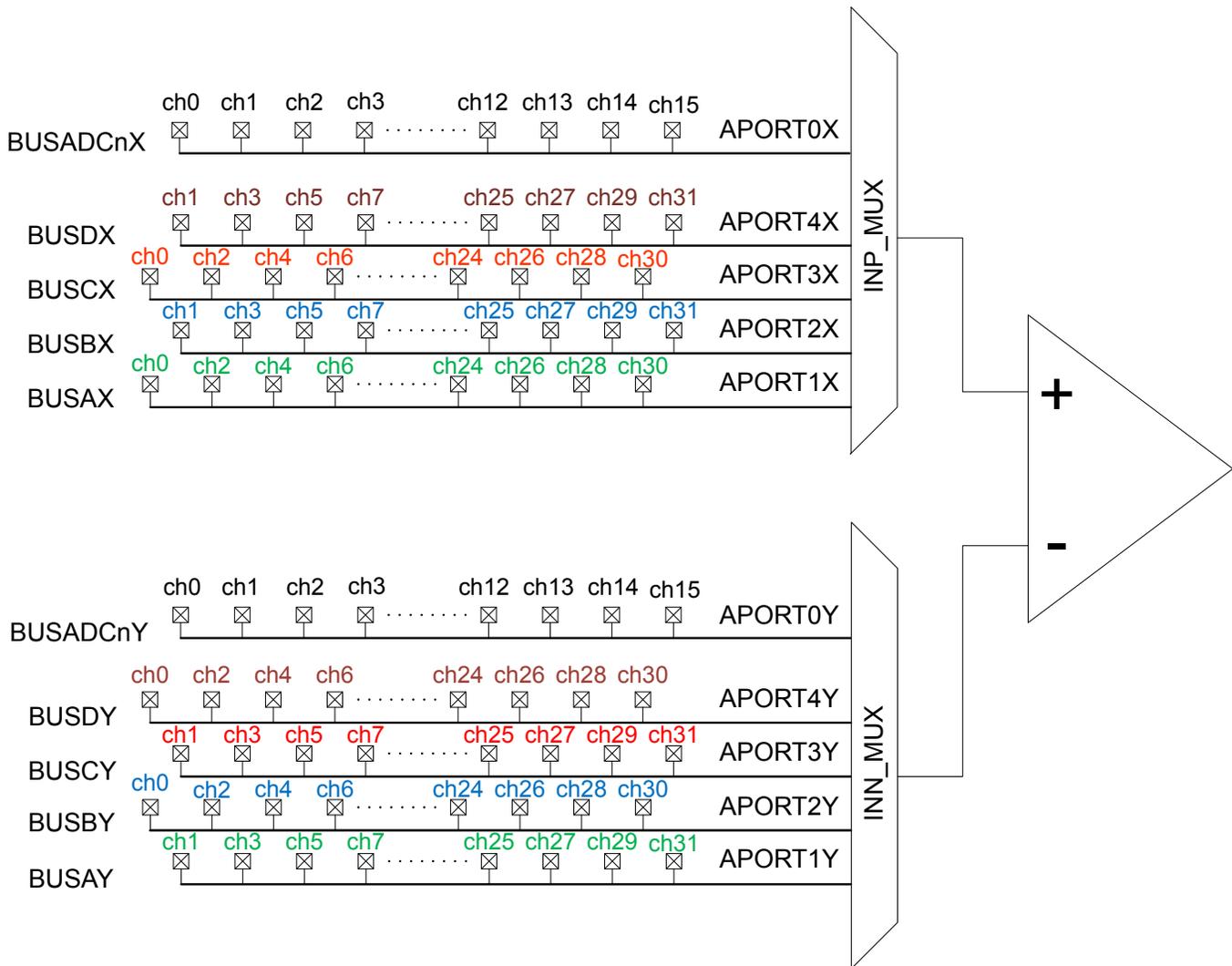
ADC external reference inputs are not routed through the APORT, and the maximum supported analog input voltage for an external reference will also be limited to the  $\text{MIN}(V_{ADC}, \text{IOVDD})$ .

### 27.3.7 Input Selection

The ADC samples and converts the analog voltage differential at its positive and negative voltage inputs. The input multiplexers of the ADC can connect these inputs to one of several internal nodes (e.g., temperature sensor) or to external signals via analog ports (APORT0, APORT1, APORT2, APORT3 or APORT4).

The analog ports APORT1, APORT2, APORT3, and APORT4 connect to external pins via analog buses (BUSAX, BUSAY, BUSBX, etc.) which are shared among other analog peripherals on the device. APORT1 through APORT4 are each 32 channels wide with connections to two sub-buses: a 16-channel X bus and a 16-channel Y bus. In the ADC module, all X buses connect to the INP\_MUX and all Y buses connect to the INN\_MUX as shown in [Figure 27.5 APORT Connection to the ADC on page 890](#). Connections to the X and Y sub-buses alternate channels on the APORT. On APORT1 and APORT3, even-numbered channels connect to the X bus, and odd-numbered channels connect to the Y bus. On APORT2 and APORT4, even-numbered channels connect to the Y bus and odd-numbered channels connect to the X bus. The APORT to BUS mappings may vary from device to device, Refer to the APORT Client Map in the device data sheet for exact mappings.

Unlike APORT1 through APORT4, APORT0 is not a shared resource. It consists of a 16-channel X bus and a 16-channel Y bus, each with dedicated I/O pin connections. Note that APORT0 is not available on all device families.



**Figure 27.5. APORT Connection to the ADC**

For differential measurements, one input must be chosen from an X bus and the other from a Y bus. Choosing both inputs from an X bus or both from a Y bus will generate a PROGERR interrupt (if enabled) of NEGSELCONF type. The PROGERR type can be checked in the ADCn\_STATUS register.

The mapping and availability for external I/O connections to ADC0 inputs is shown in device data sheet.

Multiple peripherals may request the same shared system bus (BUSAX, BUSAY, BUSBX, etc.). When this happens, a conflict status is generated and that bus is kept floating. If this happens with the ADC, the PROGERR field in ADCn\_STATUS is set to BUSCONF, and an interrupt may be generated (if enabled). When connecting dedicated I/Os through APORT0, all inputs are available to APORT0X and APORT0Y and no bus conflict is possible. Refer to [27.3.7.3 APORT Conflicts](#) for more information on identifying and resolving bus conflicts.

**Note:** The internal inputs can only be sampled in single channel, single-ended mode. NEGSEL should be fixed to VSS for these conversions.

### 27.3.7.1 Configuring ADC Inputs in Single Channel Mode

In single channel mode, the ADCn\_SINGLECTRL register provides the POSSEL and NEGSEL selection for positive and negative channel selection of the ADC. The APORT Client Map provides external pin to internal bus channel mapping enumeration for a particular device. Software can also choose internal nodes for POSSEL.

For single-ended conversions on external (APORT-connected) signals, POSSEL and NEGSEL are fully configurable. However, when performing conversions on internal signals, NEGSEL must be set to VSS. This NEGSEL reconfigurability feature in single-ended mode may not be available in all devices. If compatibility with devices that do not support this feature is desired, NEGSEL should be set to VSS for all single channel single-ended conversions.

Note that in both the POSSEL and NEGSEL fields, it is possible to choose inputs from both X and Y buses, even though X channels are physically connected to the positive mux (INP\_MUX) and Y channels are physically connected to the negative mux (INN\_MUX). For single-ended operation (DIFF = 0), if the positive input is chosen from a Y channel the ADC performs a negative single ended conversion and automatically inverts the result at the end, producing a positive result. For differential conversions (DIFF = 1), if a Y channel is chosen for the positive input and an X channel is chosen for the negative input, the ADC result will be inverted to produce the correct polarity.

Refer to device-specific data sheet for specific pin connection options. Note that the same I/O pin may appear in multiple locations.

### 27.3.7.2 Configuring ADC Inputs in Scan Mode

In scan mode, the ADC can sample and convert up to 32 external channels on each conversion trigger. Internal channels are not available in scan mode. The ADC's scanner logic automatically changes the input mux settings between conversions, eliminating the need for firmware intervention.

The ADC scanner logic is controlled by a set of 32 logical channels called SCANINPUTIDs. The 32 SCANINPUTIDs are arranged in four groups of 8 channels each. Each channel group can point to a predefined series of 8 sequential channels on any of the available APORTs. The ADCn\_SCANINPUTSEL register is used to configure which group of physical APORT channels each of the SCANINPUTID channel groups map to. For example, selecting APORT1CH16TOCH23 in the INPUT7TO0SEL field selects APORT1CH16 for SCANINPUTID0, APORT1CH17 for SCANINPUTID1, APORT1CH18 for SCANINPUTID2, and so on.

The four SCANINPUTID groups are fully independent and may be selected from any APORT in any combination. It is possible also to repeat the same selection in multiple groups. For example, the user may select APORT2CH0TOCH7 for all four of the SCANINPUTID groups.

In many cases, the user application will not require all 32 channels of the scanner to be converted. Each of the scanner channels may be individually enabled according to the needs of the system. The ADCn\_SCANMASK register is used to enable and disable individual SCANINPUTIDs. The bits in the ADCn\_SCANMASK register correspond one-to-one with the SCANINPUTID channel numbers. During a scan operation, the ADC scanner logic will convert only the enabled SCANINPUTIDs, in order from lowest to highest.

In single-ended mode, all conversions performed by the ADC will be relative to VSS. For any enabled SCANINPUTID, the selected APORT channel will be connected to the ADC with the opposite ADC input terminal connected to VSS. Note that the channel groups selected in ADCn\_SCANINPUTSEL point to a block of 8 channels on an APORT, which includes both X and Y channels. Depending on the channels enabled by ADCn\_SCANMASK, the ADC may perform conversions on the X or the Y bus associated with that APORT.

Figure 27.6 ADC Single-ended Scan Mode Example on page 892 shows an example of a single-ended scan configuration. In this example, ADCn\_SCANINPUTSEL has been configured to place APORT1CH16TO23 in the first, third, and fourth channel groups. APORT4CH8TO15 has been placed in the second channel group. ADCn\_SCANMASK selects six of these channels for inclusion in the scan. When an ADC scan is initiated with this configuration, the ADC begins at SCANINPUTID0 and converts each enabled channel in turn. This scan configuration results in a set of six single-ended ADC conversions: PF0, PF3, PA5, PA5, PF7, and PF4.

|               |                |      |      |      |      |      |      |      |                |      |      |      |      |      |      |      |               |      |      |      |      |      |     |     |                |      |      |      |      |      |      |      |   |  |  |  |  |  |  |  |
|---------------|----------------|------|------|------|------|------|------|------|----------------|------|------|------|------|------|------|------|---------------|------|------|------|------|------|-----|-----|----------------|------|------|------|------|------|------|------|---|--|--|--|--|--|--|--|
| SCANINPUTSEL  | APORT1CH16TO23 |      |      |      |      |      |      |      | APORT1CH16TO23 |      |      |      |      |      |      |      | APORT4CH8TO15 |      |      |      |      |      |     |     | APORT1CH16TO23 |      |      |      |      |      |      |      |   |  |  |  |  |  |  |  |
| APORT-Channel | 1-23           | 1-22 | 1-21 | 1-20 | 1-19 | 1-18 | 1-17 | 1-16 | 1-23           | 1-22 | 1-21 | 1-20 | 1-19 | 1-18 | 1-17 | 1-16 | 4-15          | 4-14 | 4-13 | 4-12 | 4-11 | 4-10 | 4-9 | 4-8 | 1-23           | 1-22 | 1-21 | 1-20 | 1-19 | 1-18 | 1-17 | 1-16 |   |  |  |  |  |  |  |  |
| I/O Pin       | PF7            | PF6  | PF5  | PF4  | PF3  | PF2  | PF1  | PF0  | PF7            | PF6  | PF5  | PF4  | PF3  | PF2  | PF1  | PF0  | none          | none | PA5  | PA4  | PA3  | PA2  | PA1 | PA0 | PF7            | PF6  | PF5  | PF4  | PF3  | PF2  | PF1  | PF0  |   |  |  |  |  |  |  |  |
| SCANMASK      | 0              | 0    | 0    | 1    | 0    | 0    | 0    | 0    | 1              | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0             | 0    | 1    | 1    | 0    | 0    | 0   | 0   | 0              | 0    | 0    | 0    | 1    | 0    | 0    | 0    |   |  |  |  |  |  |  |  |
| SCANINPUTID   | 31             |      |      |      |      |      |      |      | 24 23          |      |      |      |      |      |      |      | 16 15         |      |      |      |      |      |     |     | 8 7            |      |      |      |      |      |      |      | 0 |  |  |  |  |  |  |  |

Figure 27.6. ADC Single-ended Scan Mode Example

In differential mode, the default operation of the ADC scanner is to perform a differential measurement between the selected APORT channel and the next channel on that APORT. For example, if the enabled SCANINPUTID points to APORT1CH6, the ADC will perform a differential conversion between APORT1CH6 and APORT1CH7.

There are two exceptions to this rule, listed in order of precedence:

1. When converting SCANINPUTID15, the differential conversion will be performed between the channel selected by SCANINPUTID15 and the channel selected by SCANINPUTID8.
2. When APORTnCH31 is the selected input, the differential conversion will be performed between APORTnCH31 and APORTnCH0.

Figure 27.7 ADC Differential Scan Mode Example on page 893 shows an example of a differential scan configuration. In this example, ADCn\_SCANINPUTSEL has been configured to place APORT1CH16TO23 in the first, third, and fourth channel groups. APORT4CH8TO15 has been placed in the second channel group. ADCn\_SCANMASK selects three channels pairs for inclusion in the scan. When an ADC scan is initiated with this configuration, the ADC begins at SCANINPUTID0 and converts each enabled channel in turn. This scan configuration results in a set of three differential ADC conversions: PF0-PF1, PF2-PF3, and PA4-PA5.

|                          |                |         |         |         |         |         |         |         |                |         |         |         |         |         |         |         |               |      |          |         |         |         |         |         |                |         |         |         |         |         |         |         |   |  |  |  |  |  |  |  |
|--------------------------|----------------|---------|---------|---------|---------|---------|---------|---------|----------------|---------|---------|---------|---------|---------|---------|---------|---------------|------|----------|---------|---------|---------|---------|---------|----------------|---------|---------|---------|---------|---------|---------|---------|---|--|--|--|--|--|--|--|
| SCANINPUTSEL             | APORT1CH16TO23 |         |         |         |         |         |         |         | APORT1CH16TO23 |         |         |         |         |         |         |         | APORT4CH8TO15 |      |          |         |         |         |         |         | APORT1CH16TO23 |         |         |         |         |         |         |         |   |  |  |  |  |  |  |  |
| APORT-Channel (Positive) | 1-23           | 1-22    | 1-21    | 1-20    | 1-19    | 1-18    | 1-17    | 1-16    | 1-23           | 1-22    | 1-21    | 1-20    | 1-19    | 1-18    | 1-17    | 1-16    | 4-15          | 4-14 | 4-13     | 4-12    | 4-11    | 4-10    | 4-9     | 4-8     | 1-23           | 1-22    | 1-21    | 1-20    | 1-19    | 1-18    | 1-17    | 1-16    |   |  |  |  |  |  |  |  |
| APORT-Channel (Negative) | 1-24           | 1-23    | 1-22    | 1-21    | 1-20    | 1-19    | 1-18    | 1-17    | 1-24           | 1-23    | 1-22    | 1-21    | 1-20    | 1-19    | 1-18    | 1-17    | 4-8           | 4-15 | 4-14     | 4-13    | 4-12    | 4-11    | 4-10    | 4-9     | 1-24           | 1-23    | 1-22    | 1-21    | 1-20    | 1-19    | 1-18    | 1-17    |   |  |  |  |  |  |  |  |
| I/O Differential         | PF7-none       | PF6-FP7 | PF5-PF6 | PF4-PF5 | PF3-PF4 | PF2-PF3 | PF1-PF2 | PF0-PF1 | PF7-none       | PF6-FP7 | PF5-PF6 | PF4-PF5 | PF3-PF4 | PF2-PF3 | PF1-PF2 | PF0-PF1 | none          | none | PA5-none | PA4-PA5 | PA3-PA4 | PA2-PA3 | PA1-PA2 | PA0-PA1 | PF7-none       | PF6-FP7 | PF5-PF6 | PF4-PF5 | PF3-PF4 | PF2-PF3 | PF1-PF2 | PF0-PF1 |   |  |  |  |  |  |  |  |
| SCANMASK                 | 0              | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0              | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0             | 0    | 0        | 1       | 0       | 0       | 0       | 0       | 0              | 0       | 0       | 0       | 0       | 1       | 0       | 1       |   |  |  |  |  |  |  |  |
| SCANINPUTID              | 31             |         |         |         |         |         |         |         | 24 23          |         |         |         |         |         |         |         | 16 15         |      |          |         |         |         |         |         | 8 7            |         |         |         |         |         |         |         | 0 |  |  |  |  |  |  |  |

Figure 27.7. ADC Differential Scan Mode Example

In certain applications it may be desirable to perform differential conversions on several channels against a common voltage. The ADCn\_SCANNEGSEL register allows eight of the SCANINPUTIDs to re-map the negative terminal of a differential conversion to a common channel. In the first ADCn\_SCANINPUTSEL group, the negative input for SCANINPUT 0, 2, 4, and 6 may be re-mapped to any of the odd-numbered channels in that group (SCANINPUT 1, 3, 5, or 7). Likewise, in the second ADCn\_SCANINPUTSEL group, the negative input for SCANINPUT 9, 11, 13, and 15 may be re-mapped to any of the even-numbered channels in that group (SCANINPUT 8, 10, 12, or 14).

Figure 27.8 ADC Differential Scan Mode Re-mapping Negative Input Selections on page 893 shows the effects of the ADCn\_SCANNEGSEL register on the re-mappable inputs. The left side of the figure shows the default channel mapping, and the right side of the figure shows how ADCn\_SCANNEGSEL can be programmed to map the same negative input on up to four channels.

|                          | Default SCANNEGSEL Selections |         |         |         |         |         |         |         |                |         |         |         |         |         |         |         | Re-mapped using SCANNEGSEL |         |         |         |         |         |         |         |                |         |         |         |         |         |         |         |   |  |  |  |  |  |  |  |
|--------------------------|-------------------------------|---------|---------|---------|---------|---------|---------|---------|----------------|---------|---------|---------|---------|---------|---------|---------|----------------------------|---------|---------|---------|---------|---------|---------|---------|----------------|---------|---------|---------|---------|---------|---------|---------|---|--|--|--|--|--|--|--|
| SCANINPUTSEL             | APORT1CH16TO23                |         |         |         |         |         |         |         | APORT1CH16TO23 |         |         |         |         |         |         |         | APORT1CH16TO23             |         |         |         |         |         |         |         | APORT1CH16TO23 |         |         |         |         |         |         |         |   |  |  |  |  |  |  |  |
| APORT-Channel (Positive) | 1-23                          | 1-22    | 1-21    | 1-20    | 1-19    | 1-18    | 1-17    | 1-16    | 1-23           | 1-22    | 1-21    | 1-20    | 1-19    | 1-18    | 1-17    | 1-16    | 1-23                       | 1-22    | 1-21    | 1-20    | 1-19    | 1-18    | 1-17    | 1-16    | 1-23           | 1-22    | 1-21    | 1-20    | 1-19    | 1-18    | 1-17    | 1-16    |   |  |  |  |  |  |  |  |
| APORT-Channel (Negative) | 1-16                          | 1-23    | 1-22    | 1-21    | 1-20    | 1-19    | 1-18    | 1-17    | 1-24           | 1-22    | 1-22    | 1-21    | 1-20    | 1-19    | 1-18    | 1-17    | 1-24                       | 1-17    | 1-18    | 1-17    | 1-16    | 1-23    | 1-17    | 1-16    | 1-24           | 1-17    | 1-17    | 1-22    | 1-21    | 1-20    | 1-19    | 1-18    |   |  |  |  |  |  |  |  |
| SCANNEGSEL               | 0                             | 3       | 2       | 1       | 3       | 2       | 1       | 0       | 3              | 2       | 1       | 0       | 3       | 2       | 1       | 0       | 3                          | 3       | 1       | 1       | 0       | 0       | 0       | 0       | 3              | 3       | 1       | 1       | 0       | 0       | 0       | 0       |   |  |  |  |  |  |  |  |
| I/O Differential         | PF7-PF0                       | PF6-PF7 | PF5-PF6 | PF4-PF5 | PF3-PF4 | PF2-PF3 | PF1-PF2 | PF0-PF1 | PF7-none       | PF6-PF1 | PF5-PF6 | PF4-PF1 | PF3-PF4 | PF2-PF1 | PF1-PF2 | PF0-PF1 | PF7-PF6                    | PF6-PF7 | PF5-PF6 | PF4-PF5 | PF3-PF2 | PF2-PF3 | PF1-PF2 | PF0-PF1 | PF7-none       | PF6-PF1 | PF5-PF6 | PF4-PF1 | PF3-PF4 | PF2-PF1 | PF1-PF2 | PF0-PF1 |   |  |  |  |  |  |  |  |
| SCANINPUTID              | 15                            |         |         |         |         |         |         |         | 8 7            |         |         |         |         |         |         |         | 15                         |         |         |         |         |         |         |         | 8 7            |         |         |         |         |         |         |         | 0 |  |  |  |  |  |  |  |

Figure 27.8. ADC Differential Scan Mode Re-mapping Negative Input Selections

### 27.3.7.3 APORT Conflicts

The ADC shares common analog buses connected to its APORTs (1-4) with other analog peripherals (see device-specific data sheet). As the ADC performs single or scan conversions, it requests the shared buses and sends selections for the control switches to connect the desired I/O pins. If another analog peripheral requests the same shared bus at the same time, there will be a collision and none of the peripherals will be granted control of that bus.

To help debug over-utilization of APORT resources, the ADC hardware provides status information in local registers. The ADCn\_APOR-TREQ register gives the user visibility into which APORT(s) the ADC is requesting given the setting of the input selection registers. ADCn\_APORTCONFLICT reports any conflicts that occur. If PROGERR in ADCn\_IEN is set, any conflict generates an interrupt. The PROGERR field in the ADCn\_STATUS register indicates whether the programming error happened as a result of an APORT bus conflict (BUSCONF) or from a negative-input selection conflict (NEGSELCONF). If the PROGERR interrupt occurred due to a negative selection conflict, then the interrupt can be cleared by software only after correcting the conflict. If a software clear is attempted without correcting the configuration, the interrupt will be cleared for one clock cycle but then it will trigger again as the invalid configuration still persists.

**Note:** The ADC requests shared bus connections as soon as that bus is selected in the input select registers, even if the ADC is not performing any conversions. This means that by using the APORT request, the ADC will acquire the associated shared analog bus, preventing other peripherals from using it. The bus will be released only when the input select registers are changed.

It is possible for the ADC to passively monitor shared bus signals without controlling the switches and creating bus conflicts. This can be done by setting the ADCn\_APORTMASTERDIS register. When ADCn\_APORTMASTERDIS is used, channel selection defers to the peripheral acting as the bus master for that shared bus, and no bus conflict will occur. The ADC will connect its input to the shared bus, but the specific channel will be controlled by the peripheral designated as the bus master.

### 27.3.8 Reference Selection and Input Range Definition

The full scale voltage (VFS) of the ADC is defined as the full input range, from the lowest possible input voltage to the highest. For single-ended conversions, the input range on the selected positive input is from 0 to VFS. For differential conversions, the input to the converter is the difference between the positive and negative input selections. This can range from  $-VFS/2$  to  $+VFS/2$ .

VFS for the converter is determined by a combination of the selected voltage reference (VREF) and programmable divider circuits on the ADC input and voltage reference paths. Users have full control over the VREF and divider selections, offering a very flexible and wide selection of VFS values. In most applications however, it is not necessary to adjust VFS beyond a set of common pre-defined choices. For the simplest VFS configuration, refer to [27.3.8.1 Basic Full-Scale Voltage Configuration](#). If the application requires a VFS configuration not available in the pre-defined choices, [27.3.8.2 Advanced Full-Scale Voltage Configuration](#) covers additional configuration options.

### 27.3.8.1 Basic Full-Scale Voltage Configuration

Basic configuration of the VFS (full scale voltage) for the converter is done by programming the REF bitfield in ADCn\_SINGLECTRL (for single channel mode) or ADCn\_SCANCTRL (for scan mode) to any of the pre-defined options. The list of available pre-defined VFS options is:

- VFS = 1.25 V using internal VBGR as the reference source
- VFS = 2.5 V using internal VBGR as the reference source
- VFS = AVDD using AVDD as the reference source ( $AVDD \leq 3.6$  V)
- VFS = 5 V using internal VBGR as the reference source
- VFS = ADCn\_EXTP external pin as a single-ended reference source (1.2 V - 3.6 V)
- VFS = ADCn\_EXTP - ADCn\_EXTN external pins as a differential reference source. ( 1.2 V - 3.6 V difference)
- VFS = 2 x AVDD using AVDD as the reference source ( $AVDD \leq 3.6$  V)

The maximum and minimum input voltage which the ADC can recognize at any external pin is limited to the minimum of the  $V_{ADC}$  and IOVDD supply voltages (where  $V_{ADC}$  is VDDX\_ANA, as described in [27.3.5 Power Supply](#)). If VFS is configured to be larger than the supply range, the full ADC range will not be available. For example, with a 3.3 V supply and VFS configured to 5 V, the input voltage for single-ended conversions will be limited to 0 to 3.3 V, though the effective VFS is still 5 V.

The ADC uses a chip-level bias circuit to provide bias current for its operation. For highest accuracy when using a VBGR-derived internal bandgap reference source, GPBIASACC in ADCn\_BIASPROG should be cleared to 0 (HIGHACC). This will allow the ADC to enable high-accuracy mode from the bias circuitry during conversions. When AVDD or an external pin reference option is used, software may set GPBIASACC in ADCn\_BIASPROG to 1 (LOWACC) to conserve energy. Note that VDAC and DC-DC usage may also switch the chip-level bias to high- accuracy mode (even if GPBIASACC is set to LOWACC), potentially impacting ADC results. For example, if ADC is doing a conversion with GPBIASACC set to LOWACC and VDAC also starts a conversion using the internal low noise reference, then the chip-level bias circuit will be automatically switched to high-accuracy mode (potentially corrupting results of the on-going ADC conversion). Similarly, DC-DC startup automatically switches the chip-level bias circuit to high-accuracy mode for a short time, i.e., if DC-DC startup happens when ADC is doing a conversion (with GPBIASACC set to LOWACC), ADC results may get corrupted. DC-DC startup automatically switches the bias circuit to high-accuracy mode for 25  $\mu$ s. It is during this time that ADC conversions with the GPBIASACC set to LOWACC should be avoided.

If the pre-defined VFS options do not suit the particular application, refer to [27.3.8.2 Advanced Full-Scale Voltage Configuration](#) for more advanced VFS options.

### 27.3.8.2 Advanced Full-Scale Voltage Configuration

For most applications, the pre-defined VFS options described in [27.3.8.1 Basic Full-Scale Voltage Configuration](#) are suitable. Advanced VFS configurations are also possible by programming the REF bitfield in ADCn\_SINGLECTRL or ADCn\_SCANCTRL to the CONF option. Programming the REF bitfield to CONF allows the user to select the specific VREF source and adjust the programmable input and reference divider options directly.

The general procedure for programming an advanced VFS configuration is as follows:

1. Select the voltage reference source using VREFSEL.
2. Configure VREFATTFIX and VREFATT so that the reference voltage at the ADC is between 0.7 and 1.05 V.
3. Configure VINATT to achieve the desired full-scale voltage.

The VREFSEL field in ADCn\_SINGLECTRLX or ADCn\_SCANCTRLX selects the voltage reference source. The ADC can choose from the following voltage reference (VREF) sources:

- VBGR: An internal 0.83 V bandgap reference voltage. This is the most precise internal reference source available.
- VDDXWATT: An attenuated version of the AVDD supply voltage. The attenuation factor is determined by the VREFATTFIX and/or VREFATT bit fields.
- VREFPWATT: An external reference source applied to the ADCn\_EXTP pin, and attenuated by the attenuation factor (determined by the VREFATTFIX and/or VREFATT bit fields). This is the appropriate choice for external reference inputs greater than 1.05 V.
- VREFP: An external reference source applied to the ADCn\_EXTP pin, without any attenuation. This is the appropriate choice for external reference inputs between 0.7 V and 1.05 V.
- VENTROPY: A very low internal reference voltage (approx. 0.1 V). This option is intended to be used only with the ADC inputs tied internally to VSS, for generating random noise at the ADC output.
- VREFPNWATT: A differential version of VREFPWATT, with the reference source applied to the ADCn\_EXTP and ADCn\_EXTN pins and attenuated. This is the appropriate choice where a differential reference of greater than 1.05 V is required.
- VREFPN: A differential version of VREFP, with the reference source applied to the ADCn\_EXTP and ADCn\_EXTN pins and no attenuation. This is the appropriate choice where a differential reference of between 0.7 V and 1.05 V is required.
- VBGRLOW: An internal 0.78 V bandgap reference voltage.

The ADC reference voltage should be attenuated to a lower voltage when using AVDD or the external reference source. A simple method for a wide range of reference sources is to set VREFATTFIX to 1. The VREF attenuation factor ( $ATT_{VREF}$ ) can then be selected between 1/3 (when VREFATT is greater than 0), and 1/4 (when VREFATT is equal to 0). For reference sources between 1.2 V and 3.6 V,  $ATT_{VREF} = 1/3$  is the best choice.  $ATT_{VREF} = 1/4$  can be used with references from 1.6 V to 3.8 V, with slight performance degradation.

Finer granularity on  $ATT_{VREF}$  is possible as well, by clearing VREFATTFIX to 0, and setting the VREFATT field. For optimal performance with VREFATTFIX = 0, the attenuated ADC reference input should be limited to between 0.7 V and 1.05 V. When VREFATTFIX is cleared to 0,  $ATT_{VREF}$  is set according to the equation:

$$ATT_{VREF} = (VREFATT + 6) / 24 \text{ for } VREFATT < 13, \text{ and } (VREFATT - 3) / 12 \text{ for } VREFATT \geq 13$$

**Figure 27.9.  $ATT_{VREF}$ : VREF Attenuation Factor**

The ADC input also includes a programmable attenuator. The VIN attenuator is used to widen the available input range of the ADC beyond the reference source. The VIN attenuation factor ( $ATT_{VIN}$ ) is determined by the VINATT field according to the equation:

$$ATT_{VIN} = VINATT / 12 \text{ for } VINATT \geq 3 \text{ (settings 0, 1, and 2 are not allowable values for VINATT)}$$

**Figure 27.10.  $ATT_{VIN}$ : VIN Attenuation Factor**

VFS can be calculated by the formula given below for any given VREF source, VREF attenuation, and VIN attenuation:

$$VFS = 2 \cdot VREF \cdot ATT_{VREF} / ATT_{VIN}$$

VREF is selected in the VREFSEL bitfield, and

$ATT_{VREF}$  is the VREF attenuation factor, determined by VREFATT or VREFATTFIX

$ATT_{VIN}$  is the VIN attenuation factor, determined by VINATT

**Figure 27.11. VFS: Full-Scale Input Range**

The maximum and minimum input voltage which the ADC can recognize at any external pin is limited to the minimum of the  $V_{ADC}$  and IOVDD supply voltages (where  $V_{ADC}$  is VDDX\_ANA, as described in [27.3.5 Power Supply](#)). If VFS is configured to be larger than the supply range, the full ADC range will not be available. For example, with a 3.3 V supply and VFS configured to 5 V, the input voltage for single-ended conversions will be limited to 0 to 3.3 V, though the effective VFS is still 5 V.

The ADC uses a chip-level bias circuit to provide bias current for its operation. For highest accuracy when using a VBGR-derived internal bandgap reference source, GPBIASACC in ADCn\_BIASPROG should be cleared to 0 (HIGHACC). This will allow the ADC to enable high-accuracy mode from the bias circuitry during conversions. When AVDD or an external pin reference option is used, software may set GPBIASACC in ADCn\_BIASPROG to 1 (LOWACC) to conserve energy. Note that VDAC and DC-DC usage may also switch the chip-level bias to high-accuracy mode (even if GPBIASACC is set to LOWACC), potentially impacting ADC results. For example, if ADC is doing a conversion with GPBIASACC set to LOWACC and VDAC also starts a conversion using the internal low noise reference, then the chip-level bias circuit will be automatically switched to high-accuracy mode (potentially corrupting results of the on-going ADC conversion). Similarly, DC-DC startup automatically switches the chip-level bias circuit to high-accuracy mode for a short time, i.e., if DC-DC startup happens when ADC is doing a conversion (with GPBIASACC set to LOWACC), ADC results may get corrupted. DC-DC startup automatically switches the bias circuit to high-accuracy mode for 25  $\mu$ s. It is during this time that ADC conversions with the GPBIASACC set to LOWACC should be avoided.

The combination of VREF,  $ATT_{VREF}$  and  $ATT_{VIN}$  can produce a wide range of full-scale voltage options for the converter. [Table 27.1 Advanced VFS Configuration: VREF = AVDD on page 897](#) shows some example VFS configurations using AVDD as a reference source.

**Table 27.1. Advanced VFS Configuration: VREF = AVDD**

| AVDD Voltage | VREF Attenuation Settings   | Reference Voltage at ADC | VIN Attenuation Settings                          | VFS                                 |
|--------------|---|--------------------------|---|-------------------------------------|
| 1.85 V       | VREFATTFIX = 0<br>VREFATT = 6<br><b><math>ATT_{VREF} = 1/2</math></b> | 0.925 V                  | VINATT = 12<br><b><math>ATT_{VIN} = 1</math></b>  | 1.85 V<br>(+/-0.925 V differential) |
| 3.0 V        | VREFATTFIX = 0<br>VREFATT = 2<br><b><math>ATT_{VREF} = 1/3</math></b> | 1.0 V                    | VINATT = 8<br><b><math>ATT_{VIN} = 2/3</math></b> | 3.0 V<br>(+/-1.5 V differential)    |
| 3.0 V        | VREFATTFIX = 0<br>VREFATT = 2<br><b><math>ATT_{VREF} = 1/3</math></b> | 1.0 V                    | VINATT = 4<br><b><math>ATT_{VIN} = 1/3</math></b> | 6.0 V<br>(+/-3.0 V differential)    |
| 3.6 V        | VREFATTFIX = 1<br>VREFATT = 0<br><b><math>ATT_{VREF} = 1/4</math></b> | 0.9 V                    | VINATT = 6<br><b><math>ATT_{VIN} = 1/2</math></b> | 3.6 V<br>(+/-1.8 V differential)    |

### 27.3.9 Programming of Bias Current

The ADC uses a chip-level bias generator to provide bias current for its operation. The ADC's internal bias can be scaled by ADCBIASPROG field of the ADCn\_BIASPROG register. At lower conversion speeds, the ADCBIASPROG can be used to lower active power. Some commonly used settings are given in the ADCBIASPROG register description. For proper operation, the ADC conversion speed must be scaled accordingly. The scale factor is calculated as:

$$\text{Bias scale factor} = (1 - \text{ADCBIASPROG}[2:0]/8) / (1 + 3 \cdot \text{ADCBIASPROG}[3])$$

**Figure 27.12. Bias Scale Factor**

The bias programming register also includes the VFAULTCLR bit field. If VREFOF interrupt is enabled and it is triggered, then the user needs to set this bit in the ISR before clearing the interrupt flag. This bit then needs to be reset after the interrupt flag is cleared in order to enable the VREFOV flag to trigger on the next VREFOV condition.

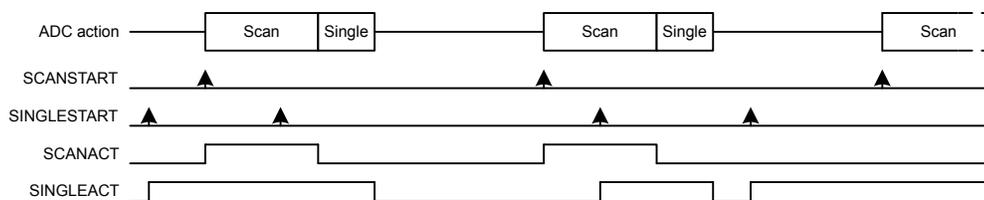
The bias current settings should only be changed while the ADC is disabled (i.e. in NORMAL warm-up mode and no conversion in progress).

### 27.3.10 Feature Set

The following sections explain different ADC features.

#### 27.3.10.1 Conversion Tailgating

Scan conversions have priority over single channel conversions. This means that if scan and single triggers are received simultaneously, or even if the scan is received later when ADC is being warmed up for performing a single conversion, the scan conversion will have priority and will be done before the single conversion. However, a scan trigger will not interrupt in the middle of a single conversion, i.e., if the single conversion is in the acquisition or approximation phase, then the scan will have to wait for the single conversion to complete. If a scan sequence is triggered by a timer on a periodic basis, single channel conversion that started just before a scan trigger can delay the start of the scan sequence, thus causing jitter in sample rate. To solve this, conversion tailgating can be chosen by setting TAILGATE in ADCn\_CTRL. When this bit is set, any triggered single channels will wait for the next scan sequence to finish before activating (see [Figure 27.13 ADC Conversion Tailgating on page 898](#)). The single channel will then follow immediately after the scan sequence. In this way, the scan sequence will always start immediately when triggered, provided that the period between the scan triggers is big enough to allow the single sample conversion that was triggered to finish before the next scan trigger arrives. Note that if tailgating is set and a single channel conversion is triggered, it will indefinitely wait for a scan conversion before starting the single channel conversion.



**Figure 27.13. ADC Conversion Tailgating**

### 27.3.10.2 Repetitive Mode

Both single channel and scan mode can be run as a one shot conversion or in repetitive mode. The REP bitfield in ADCn\_SINGLECTRL/ADCn\_SCANCTRL registers can be used to activate the repetitive mode for single and scan respectively. In order to achieve the maximum sampling rate of 1 Msps, repetitive mode should be used.

It is also possible to have a programmable delay between these repetitive conversions. The REPDELAY bitfield in the ADCn\_SINGLECTRLX and ADCn\_SCANCTRLX registers can be used to set the delay between two repeated conversions in single channel and scan mode respectively. For single channel mode when a single conversion in repetitive mode ends, the user programmed REPDELAY is inserted and then the next single conversion is re-triggered after the delay period is over. For scan mode the REPDELAY is inserted after the entire scan sequence ends. Once the delay period is over, scan mode is internally re-triggered. Note that when the ADC is in SYNC mode and REPDELAY is set to generate a delay, it takes an additional 5 HPPERCLK cycles after the trigger before the next conversion begins. If REPDELAY is set to NODELAY, the next conversion begins immediately, without any delay or additional HPPERCLKs. The [27.3.10.1 Conversion Tailgating](#) explains how the single channel and scan mode conversions can push each other out of phase. Conversion tailgating can be chosen in repetitive mode as well in order to ensure that the scan sequence will always start immediately when triggered, provided the scan REPDELAY chosen is big enough for the single conversion to finish. The status flags SINGLEACT and SCANACT stay high throughout the repeat mode, i.e., even during the delay period. The flags show that the conversions are either active or pending. Whether the ADC turns off or stays warmed up between these repeated conversions depends on the WARMUPMODE chosen in the ADCn\_CTRL register. When using single channel mode with repeat mode and REPDELAY enabled, then once the ADC has started operation (i.e., singleact status flag has gone high) then no new single conversion triggers (software START/ PRS triggers) should be sent to the ADC until the ADC has stopped converting (i.e., singleact status flag has gone low). The same applies to scan sequence conversions.

### 27.3.10.3 Conversion Trigger

The conversion modes can be activated by writing a 1 to the SINGLESTART or SCANSTART bit in the ADCn\_CMD register. The conversions can be stopped by writing a 1 to the SINGLESTOP or SCANSTOP bit in the ADCn\_CMD register. A START command will have priority over a STOP command. When the ADC is stopped in the middle of a conversion, the result buffer is cleared (the FIFO contents for any prior conversions are still intact). Every time a STOP command is issued, the user should wait for the corresponding status flag (SINGLEACT/SCANACT) to go low and then either read all the data in the FIFO or send the corresponding FIFOCLEAR command. The SINGLEACT and SCANACT bits in ADCn\_STATUS are set high when the modes are actively converting or have pending conversions.

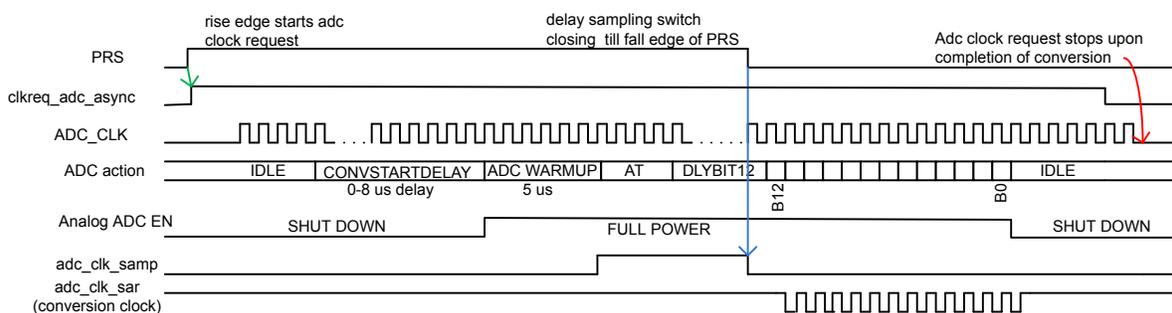
It is also possible to trigger conversions from PRS signals. The PRS is treated as an asynchronous trigger. Setting PRSEN in ADCn\_SINGLECTRL/ADCn\_SCANCTRL enables triggering from PRS input. Which PRS channel to listen to is defined by PRSSEL in ADCn\_SINGLECTRLX/ADCn\_SCANCTRLX. When PRS trigger is selected, it is still possible to trigger a conversion from software. Refer to the PRS chapter for more information on how to set up the PRS channels. When the conversions are triggered using the ADCn\_CMD register, then the SINGLEACT and SCANACT bits in the ADCn\_STATUS are set as soon as the START command is written to the register. When the conversion is triggered using PRS, it takes some cycles from the time PRS trigger is received until the SINGLEACT and SCANACT bits are set due to the synchronization requirement. If SINGLEACT is already high then sending a new START command or a new PRS trigger for a single conversion will not have any impact as ADC already has a single conversion ongoing or a single conversion pending (single conversion can be pending if ADC is busy running a scan sequence). The same rules apply for SCANACT and SCAN START and PRS triggers. When software issues a SINGLE/SCAN STOP command, it must wait until SINGLEACT/ SCANACT flag goes low before issuing a new START.

The PRS may trigger the ADC in two possible ways, configured by PRSMODE in ADCn\_SINGLECTRLX/ADCn\_SCANCTRLX. In PULSED mode, a PRS pulse triggers the ADC to start the ADC\_CLK (if not already enabled), warm up (if not already warm), start the acquisition period, and perform the conversion. This is identical to issuing a START command from software. In this mode, the input sampling finishes at the end of the acquisition period (AT).

If the ADC\_CLK and the source of the trigger (START command or PRS pulse) are not synchronous, the frequency of the input sampling (FS), will experience a  $1\frac{1}{2}$  to  $2\frac{1}{2}$  ADC\_CLK cycle jitter due to synchronization requirements.

To precisely control the sample frequency, the PRSMODE can be set to TIMED mode. In this mode, a long PRS pulse is expected to trigger the ADC and its negative edge directly finishes input sampling and starts the approximation phase, giving precise sampling frequency management. The restriction is that the PRS pulse has to be long enough to start the ADC\_CLK (if not already enabled), and finish the acquisition period based on the AT field in ADCn\_SINGLECTRL/ADCn\_SCANCTRL. The PRS pulse needs to be high when AT event finishes. If it is not high when AT finishes, then it is ignored and input sampling finishes after AT event has ended (a two cycle latency is added to the conversion in this scenario). In this case, the ADC sets the PRSTIMEDERR interrupt flag.

If the PRS pulse is too long (e.g., FS = 32kHz), the analog ADC start can be delayed to save power. The CONVSTARTDELAY along with its EN in the ADCn\_SINGLECTRLX or ADCn\_SCANCTRLx can be programmed to implement a 0 to 8 microseconds delay. The microsecond tick is counted by TIMEBASE with ADC\_CLK similar to warmup case. This saves power as the ADC is not enabled until the last possible microsecond before the fall edge of the PRS arrives to open the sampling switch and to start the approximation phase. [Figure 27.14 ADC PRS Timed Mode with ASNEEDED ADC\\_CLK Request on page 900](#)) shows PRS Timed mode triggering with CONVSTARTDELAY and ASNEEDED ADC\_CLK request. See that power is saved by both delaying the ADC EN and by requesting the ADC\_CLK only during ADC operation. This is especially useful in saving power when running the ADC in EM2 Deep Sleep or EM3 Stop power mode with low sampling frequency.



**Figure 27.14. ADC PRS Timed Mode with ASNEEDED ADC\_CLK Request**

When a PRS pulse is received, if the ADC\_CLK is not running (ASNEEDED mode), then the ADC requests the clock by setting clkreq\_adc\_async high. If the chosen clock source (HFXO/ HFSRCCLK/ AUXHFRCO) is already running, then it takes 5 ADC\_CLK cycles after the clock request is asserted for the ADC\_CLK to start. HFXO and HFSRCCLK (if chosen as ADC clock source) need to be already running before ADC sends out the clock request. If AUXHFRCO is chosen as the ADC clock source, and it is not already

running, then the CMU automatically turns it on when the ADC sends a clock request. In such a case, it takes (7 ADC\_CLK cycles + the oscillator startup time) for the ADC\_CLK to start. The oscillator startup time can be found in the device data sheet.

When triggering repeat mode using PRS and then stopping the triggered mode using STOP command, ensure that the PRS pulse used to generate the repeat mode has gone low by the time the STOP command is issued. If the PRS pulse continues to stay high after ADC has stopped the ongoing conversion, then it will be picked as a new trigger to start a new conversion.

**Note:**

- The conversion settings should not be changed while the ADC is running. Doing so may lead to unpredictable behavior.
- The `adc_clk_sar` phase is always reset by a conversion trigger as long as a conversion is not in progress. This gives predictable latency from the time of the trigger to the time the conversion starts, regardless of when in the trigger occurs.
- Software and LESENSE should not trigger conversions if PRS Timed mode is selected and PRSEN is set to 1 in the ADCn\_SINGLECTRL/ADCn\_SCANCTRL register.
- If the PRS Timed mode is being used, the acquisition time (AT) must be set greater than 0.

Scan conversions can be triggered using LESENSE as well. LESENSE only triggers one input conversion at a time (not the whole sequence of 32 possible inputs). The input to be converted using LESENSE must be configured by the user in the ADCn\_SCANINPUTSEL register before triggering the conversion, i.e., one of the 32 inputs chosen in the ADCn\_SCANINPUTSEL register must be the one that is to be converted using LESENSE. The ADCn\_SCANMASK is not used for LESENSE triggered conversions. Instead, the user can select which input should be converted through LESENSE inside the LESENSE settings (LESENSE\_CHX). The results of LESENSE triggered conversions are not loaded in the FIFO/ DATA registers but are instead available in the LESENSE register. Similarly, the SCAN interrupt flag is not set on completion of a LESENSE triggered conversion (because that flag is set only when the data is written to the Scan FIFO). When there is a LESENSE triggered conversion going on or pending, the SCANACT status flag is set. The SCANPEND interrupt flag is set when a software/PRS triggered scan goes pending because a LESENSE triggered scan is running (software/PRS triggered scan will start after the currently running LESENSE scan conversion completes). Similarly, SCANEXTPEND interrupt flag is set when the LESENSE triggered scan conversion goes pending because a software/PRS triggered scan is running. LESENSE triggered conversions can be stopped at any time using the SCANSTOP command in the ADCn\_CMD register. Note that the LESENSE triggered conversion cannot trigger the Scan repeat mode.

The DBGHALT bit-field in the ADCn\_CTRL register can be used to choose the ADC behavior in debug mode. If this bit is set to 1, then in debug mode ADC completes the current conversions and then halts. This means that all conversion triggers that were received before the debug halt occurred will be serviced before the ADC halts. All conversion triggers received after the ADC was halted, will be serviced when the debug mode is not halted any more. If the repetitive mode is running (in repetitive mode ADC keeps doing conversions until the user sends a software STOP) and a debug mode halt occurs, then the ADC will gracefully complete the current on-going conversion and then halt. The repetitive mode conversions will restart as soon as the debug mode is not halted any more.

### 27.3.10.4 Output Results

ADC output results are presented in 2's complement form and the format for single ended and differential conversions are given in [Table 27.2 ADC Single Ended Conversion on page 902](#) and [Table 27.3 ADC Differential Conversion on page 902](#), respectively. If differential mode is selected, the results are sign extended up to 32-bits (shown in [Table 27.5 ADC Results Representation on page 903](#)).

**Table 27.2. ADC Single Ended Conversion**

| Input Voltage         | Output Results |           |
|-----------------------|----------------|-----------|
|                       | Binary         | Hex value |
| $4095/4096 \cdot VFS$ | 111111111111   | FFF       |
| $0.5 \cdot VFS$       | 100000000000   | 800       |
| $1/4096 \cdot VFS$    | 000000000001   | 001       |
| 0                     | 000000000000   | 000       |

**Table 27.3. ADC Differential Conversion**

| Input                 | Output Results |           |
|-----------------------|----------------|-----------|
|                       | Binary         | Hex value |
| $2047/4096 \cdot VFS$ | 011111111111   | 7FF       |
| $0.25 \cdot VFS$      | 010000000000   | 400       |
| $1/4096 \cdot VFS$    | 000000000001   | 001       |
| 0                     | 000000000000   | 000       |
| $-1/4096 \cdot VFS$   | 111111111111   | FFF       |
| $-0.25 \cdot VFS$     | 110000000000   | C00       |
| $-0.5 \cdot VFS$      | 100000000000   | 800       |

### 27.3.10.5 Resolution

The ADC performs 12-bit conversions by default. However, if full 12-bit resolution is not needed, it is possible to speed up the conversion by selecting a lower resolution (6 or 8 bits). For more information on the accuracy of the ADC, the reader is referred to the electrical characteristics section for the device.

### 27.3.10.6 Oversampling

To achieve higher accuracy, hardware oversampling can be enabled individually for each mode (Set RES in ADCn\_SINGLECTRL/ADCn\_SCANCTRL to 0x3). The oversampling rate (OVSSEL in ADCn\_CTRL) can be set to any integer power of 2 from 2 to 4096 and the configuration is shared between the scan and single channel mode (OVSSEL field in ADCn\_CTRL).

With oversampling, each input is sampled at 12-bits of resolution a number of times (given by OVSSEL), and the results are filtered by a first order accumulate and dump filter to form the end result. The data presented in the ADCn\_SINGLEDATA and ADCn\_SCANDATA registers are the direct contents of the accumulation register (sum of samples). However, if the oversampling ratio is set higher than 16x, the accumulated results are shifted to fit the MSB in bit 15 as shown in [Table 27.4 Oversampling Result Shifting and Resolution on page 903](#).

**Table 27.4. Oversampling Result Shifting and Resolution**

| Oversampling setting | # right shifts | Result Resolution # bits |
|----------------------|----------------|--------------------------|
| 2x                   | 0              | 13                       |
| 4x                   | 0              | 14                       |
| 8x                   | 0              | 15                       |
| 16x                  | 0              | 16                       |
| 32x                  | 1              | 16                       |
| 64x                  | 2              | 16                       |
| 128x                 | 3              | 16                       |
| 256x                 | 4              | 16                       |
| 512x                 | 5              | 16                       |
| 1024x                | 6              | 16                       |
| 2048x                | 7              | 16                       |
| 4096x                | 8              | 16                       |

### 27.3.10.7 Adjustment

By default, all results are right adjusted, with the LSB of the result in bit position 0 (zero). In differential mode the signed bit is extended up to bit 31, but in single ended mode the bits above the result are read as 0. By setting ADJ in ADCn\_SINGLECTRL/ADCn\_SCANCTRL, the results are left adjusted as shown in [Table 27.5 ADC Results Representation on page 903](#). When left adjusted, the MSB is always placed on bit 15 and sign extended to bit 31. All bits below the conversion result are read as 0 (zero).

**Table 27.5. ADC Results Representation**

| Adjustment | Resolution | Bits      |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------|------------|-----------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
|            |            | 31 ... 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Right      | 12         | 11 ... 11 | 11 | 11 | 11 | 11 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|            | 8          | 7 ... 7   | 7  | 7  | 7  | 7  | 7  | 7  | 7 | 7 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|            | 6          | 5 ... 5   | 5  | 5  | 5  | 5  | 5  | 5  | 5 | 5 | 5 | 5 | 5 | 4 | 3 | 2 | 1 | 0 |
|            | OVS        | 15 ... 15 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Left       | 12         | 11 ... 11 | 11 | 10 | 9  | 8  | 7  | 6  | 5 | 4 | 3 | 2 | 1 | 0 | - | - | - | - |
|            | 8          | 7 ... 7   | 7  | 6  | 5  | 4  | 3  | 2  | 1 | 0 | - | - | - | - | - | - | - | - |
|            | 6          | 5 ... 5   | 5  | 4  | 3  | 2  | 1  | 0  | - | - | - | - | - | - | - | - | - | - |
|            | OVS        | 15 ... 15 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

### 27.3.10.8 Channel Connection

The inputs are connected to the analog ADC at the beginning of the acquisition phase and are disconnected at the end of the acquisition phase. The time when the APORT switches are closed (for the next input to be converted) can be controlled by the CHCONMODE bitfield in the ADCn\_CTRL register. By default, this field is set to the MAXSETTLE option. For MAXSETTLE, APORT switches are closed on the next input as soon as the acquisition phase for the current conversion is complete. This means that the APORT switches are closed approximately 12 adc\_clk\_sar cycles (assuming 12 bit resolution) before the acquisition phase of the current conversion starts, giving APORT switches maximum time to settle. The time for which APORT switches should be closed before the acquisition phase starts, should be the same for all inputs in order to get consistent results. This means that if the ADC is warmed up with CHCONREFWARMIDLE set to 0 (scan reference warmed up and the APORT switches for the first scan channel closed) and a single trigger comes in, the single conversion will have to wait 12 adc\_clk\_sar cycles before it can start (even if single is using the same reference as scan). In this case, it might be more suitable to switch to the MAXRESP option in the CHCONMODE bitfield. In MAXRESP, the APORT switches for the upcoming conversion are closed just before the acquisition phase starts. This gives less settling time to the APORT switches but removes the extra waiting time before a conversion can start (which could be the case with MAXSETTLE as discussed above).

### 27.3.10.9 Temperature Measurement

The ADC includes an internal temperature sensor. This sensor is measured during production test and the temperature readout from the ADC at production temperature, ADC0CAL3\_TEMPREAD1V25, is given in the Device Information (DI) page. The production temperature, CAL\_TEMP, is also given in this page. The temperature sensor slope, V\_TS\_SLOPE (mV/degree Celsius), for the sensor is found in the data sheet for the device. Using the 1.25 V VFS option and 12-bit resolution, the temperature can be calculated according to the following formula (VFS in the formula is 1250 mV) :

$$T_{\text{CELSIUS}} = \text{CAL\_TEMP} - (\text{ADC0CAL3\_TEMPREAD1V25} - \text{ADC\_result}) \cdot \text{VFS} / (4096 \cdot \text{V\_TS\_SLOPE})$$

**Figure 27.15. ADC Temperature Measurement**

#### Note:

- The minimum acquisition time for the temperature reference is found in the electrical characteristics for the device. If using the 1.25 V reference, extra acquisition time is required. In this case the AT field of ADCn\_SINGLECTRL or ADCn\_SCANCTRL should be set to a value of 9 or higher.
- For the most accurate temperature sensor results, GPBIASACC in ADCn\_BIASPROG should be set to 0 to keep the bias in HIGH-ACC mode.
- If the device has more than one ADC, all ADCs may not be equipped with the temperature sensor. See the device data sheet.

### 27.3.10.10 ADC as a Random Number Generator

The ADC can be used as a random number generator. This is done by:

1. Choose the REF in the ADCn\_SINGLECTRL as CONF, setting the VREFSEL in the ADCn\_SINGLECTRLX as VENTROPY and VINATT in the same register to its maximum value of 15.
2. Set DIFF to 1 and RES to 0 in the ADCn\_SINGLECTRL register.
3. Trigger a single channel conversion and then read ADCn\_SINGLEDATA register when the conversion finishes.

The LSB[2:0] of each sample will be a random number. In this mode, the POSSEL or NEGSEL in ADCn\_SINGLECTRL can be connected to VSS or any other noisy input.

### 27.3.11 Interrupts, PRS Output

The single and scan modes have separate SINGLE and SCAN interrupt flags indicating whether corresponding FIFO contains DVL # of valid conversion data. Corresponding interrupt enable bit has to be set in ADCn\_IEN in order to generate interrupts. For these interrupts, there is no software clear mechanism by writing to ADCn\_IFC. The user needs to read enough data from the interrupted FIFO to ensure it contains less than DVL # of elements. The ADCn\_SINGLEFIFOCOUNT/ADCn\_SCANFIFOCOUNT can provide number of valid elements remaining in corresponding FIFO. The FIFO can also be cleared by ADCn\_SINGLEFIFOCLEAR/ADCn\_SCANFIFOCLEAR, but any existing data will be lost by this operation.

In addition to the SINGLE and SCAN interrupt flags, there is separate scan and single channel result overflow interrupt flag which signals that a result from a scan or single channel FIFO has been overwritten before being read. There is also separate scan and single channel result underflow interrupt flag which signals that a FIFO read was issued when the FIFO was empty.

There is separate scan and single compare interrupt flag which signals a compare match with latest sample if the CMPEN in ADCn\_SINGLECTRL/ADCn\_SCANCTRL is enabled.

ADC has two separate PRS outputs, one for single channel and one for scan sequence. A finished conversion results in a one ADC\_CLK cycle pulse, which is output to the Peripheral Reflex System (PRS). Note that the PRS pulse for scan is generated once after every channel conversion in the scan sequence.

### 27.3.12 DMA Request

The ADC has two DMA request lines, SINGLEREQ and SCANREQ, which are set when a single or scan FIFO receives DVL# of samples. The requests are cleared when the corresponding single or scan result register is read and corresponding FIFO count reaches lower than DVL. It also has two additional DMA Single request lines, SINGLESREQ and SCANSREQ, that are set when the corresponding FIFO is not empty.

### 27.3.13 Calibration

The ADC supports offset and gain calibration to correct errors due to process and temperature variations. This must be done individually for each reference used. For each reference, it needs to be repeated for single-ended, negative single-ended (see [27.3.7 Input Selection](#) for details) and differential measurement. The ADC calibration (ADCn\_CAL) register contains register fields for calibrating offset and gain for both single and scan mode. The gain and offset calibration are done in single channel mode, but the resulting calibration values can be used for both single and scan mode.

Gain and offset for various references and modes are calibrated during production and the calibration values for these can be found in the Device Information page. During reset, the gain and offset calibration registers are loaded with the production calibration values for the 1V25 reference. Others can be loaded as needed or the user can perform calibration on the fly using the particular reference and mode to be used and write the result in the ADCn\_CAL before starting the ADC conversion with them.

#### 27.3.13.1 Offset Calibration

Offset calibration must be performed prior to gain calibration. Follow these steps for the offset calibration in single mode:

1. Select the desired full scale configuration by setting the REF bit field of the ADCn\_SINGLECTRL register.
2. Set the AT bit field of the ADCn\_SINGLECTRL register to 16CYCLES.
3. Set the POSSEL and NEGSEL of the ADCn\_SINGLECTRL register to VSS, and set the DIFF to 1 for enabling differential input if calibrating for DIFF measurement. During calibration, the ADC samples represent the code coming out of the analog. Thus, since the input voltage is 0, the expected ADC output is 0b100000000000 in differential mode, 0b000000000000 in single-ended mode and 0b111111111111 in negative single-ended mode.
4. A binary search is used to find the offset calibration value. Set the CALEN to 1, and OFFSETINVMODE to 1 (if calibrating for negative single-ended conversion) in the ADCn\_CAL register. If user is performing negative single-ended calibration, the SINGLEOFFSETINV provides the offset else SINGLEOFFSET bit provides the offset (for both single-ended and differential offset calibration). Start with 0b0000 (or 0b1111 if doing calibration for differential mode) in SINGLEOFFSET or with 0b1000 in SINGLEOFFSETINV (if calibrating for negative single-ended conversion). Set the SINGLESTART bit in the ADCn\_CMD register to perform a 12-bit conversion and read the ADCn\_SINGLEDATA register. The offset is (ADCn\_SINGLEDATA - expected ADC output). Calculate this and write [3:0] of the result into SINGLEOFFSET or SCANOFFSETINV (if doing negative single-ended conversion). The user repeats till ADCn\_SINGLEDATA matches expected ADC output. The ADC has a 8LSB built in negative offset to allow for negative offset correction. So, with default offset value, which corrects for the negative offset, the converted ADCn\_SINGLEDATA would match expected ADC output if there were no offset. To get better noise immunity, the sampling phase can be repeated with Oversampling enabled. The result of the binary search is written to the SINGLEOFFSET (or SINGLEOFFSETINV) field of the ADCn\_CAL register.

### 27.3.13.2 Gain Calibration

Offset calibration must be performed prior to gain calibration. The Gain Calibration is done in the following manner:

1. Select an external ADC channel for single channel conversion (a differential channel can also be used).
2. Apply an external voltage on the selected ADC input channel. This voltage should correspond to the top of the ADC input range for the selected reference.
3. Set SINGLEGAIN[6:0] to 64 in the ADCn\_CAL and measure gain, repeat gain calibration walking the 1 in SINGLEGAIN[6] to SINGLEGAIN[0] till sampled ADCn\_SINGLEDATA matches expected value. This is done by setting CALEN in ADCn\_CAL set to 1 and performing single channel, reading in the raw ADC code from the ADCn\_SINGLEDATA and comparing it with expected code, i.e. 0b111111111111 for single-ended or differential conversion, and 0b000000000000 for negative single-ended conversion. The target value is ideally the top of the ADC input range, but it is recommended to use a value a couple of LSBs below in order to avoid overshooting. The result of the binary search is written to the SINGLEGAIN field of the ADCn\_CAL register.

For the VDD reference and external reference, there is no hardware gain calibration. Calibration can be done by software after taking a sample.

### 27.3.14 EM2 Deep Sleep or EM3 Stop Operation

The ADC can operate in EM2 Deep Sleep or EM3 Stop mode. For EM2 Deep Sleep or EM3 Stop operation the ADC\_CLK must be selected as AUXHFRCO. The section [27.3.1 Clock Selection](#) describes how to choose AUXHFRCO as the ADC\_CLK. The AUXHFRCO can be kept on for as long as sample conversion is needed or it can be requested by trigger event and after the conversion is done, the AUXHFRCO can be shut down. The second option saves power at the expense of the delay to start the AUXHFRCO oscillator. All the trigger modes are available in EM2 Deep Sleep or EM3 Stop as well.

While in EM2 Deep Sleep or EM3 Stop, the ADC can wake the system to EM0 Active on enabled interrupts. Following interrupts can wake up the system to EM0 Active:

- SINGLE or SCAN interrupt indicating that the corresponding FIFO has reached the DVL watermark.
- Overflow interrupt (SINGLEOF or SCANOF)
- Underflow interrupt (SINGLEUF or SCANUF), triggered if DMA pops more data than present in the FIFO while the system is asleep
- Compare interrupt (SINGLECMP or SCANCMP)
- Over voltage interrupt (VREFOV)

The ADC can also work with the DMA so that the system does not have to wake up to consume data. This can happen if the SCAN or SINGLE interrupt is disabled and the SINGLEDMAWU or SCANDMAWU in the ADCn\_CTRL is set. The DMA will be triggered by the ADC when DVL samples become available in the corresponding FIFO. The DMA will then pop all the elements of the corresponding FIFO and put the system back into the low power state. A system-level wake up will occur upon the DMA done interrupt. Note that other enabled ADC interrupts can still wake up the system when operating with the DMA. For example, the user can configure the window compare function to trip when the result reaches a certain threshold while gathering ADC data in EM2 Deep Sleep or EM3 Stop.

The ADC works with the EMU to wake up the system or the DMA. It takes 2  $\mu$ s from the time the ADC request a wakeup to start of the peripheral clocks. In this ASYNC mode of ADC\_CLK, it takes 6 HFPERCLK cycles to read a single entry from the single or scan FIFO. So, with a 20MHz HFPERCLK, it takes about 4  $\mu$ s per DMA wakeup to empty a full FIFO (4 entries). This restricts the sampling rate in EM2 Deep Sleep or EM3 Stop in order to avoid FIFO overflows.

The AUXHFRCO power can be reduced by reducing the clock speed, and the user may adjust the ADCBIASPROG field in the ADCn\_BIASPROG register to reduce active power of the ADC during the conversions, thus reducing power even more in EM2 Deep Sleep/EM3 Stop. Refer to the data sheet for relevant power consumption numbers.

If the ADC is not to be used in EM2 Deep Sleep or EM3 Stop, then the user should ensure that the ADC is not busy before going to the low power mode. [27.3.17 ADC Programming Model](#) explains how to ensure the ADC is not busy. If the chip enters EM2 Deep Sleep or EM3 Stop when ADC is busy without using AUXHFRCO, then the ADC clock will stop but the ADC will stay on, resulting in higher supply current. If this occurs, the EM23ERR interrupt flag will be set. Software will see this interrupt flag only when the chip wakes up.

### 27.3.15 ASYNC ADC\_CLK Usage Restrictions and Benefits

When the ADC\_CLK is chosen to come from ASYNCCLK, (ADCCLKMODE is set to ASYNC), the ADC\_CLK and the ADC peripheral clock are considered asynchronous and this adds some restrictions:

- Due to a synchronization delay, accessing the following registers takes extra time (up to additional 7 HPPERCLK cycles): ADCn\_SINGLEDATA, ADCn\_SCANDATA, ADCn\_SINGLEDATAP, ADCn\_SCANDATAP, ADCn\_SCANDATAX, ADCn\_SCANDATAXP, ADCn\_SINGLEFIFOCOUNT, ADCn\_SCANFIFOCOUNT, ADCn\_SINGLEFIFOCLEAR, ADCn\_SCANFIFOCLEAR.
- The safe time to change the ADCn\_SINGLECTRL, ADCn\_SINGLECTRLX, ADCn\_SCANCTRL, ADCn\_SCANCTRLx, ADCn\_SCANINPUTSEL, ADCn\_SCANNEGSEL or ADCn\_SCANMASK register is when SINGLEACT/SCANACT in the ADCn\_STATUS is 0 with no pending trigger event. The user can enforce this by writing the SINGLESTOP or SCANSTOP in the ADCn\_CMD register and ensuring no trigger event can come before modifying the registers.
- When the ADC needs to run in EM2 Deep Sleep or EM3 Stop, only AUXHFRCO can provide the ADC\_CLK to the ADC. Thus the user needs to set ASYNC mode of ADCCLKMODE and setup the CMU to provide the AUXHFRCO clock as ASYNCCLK.
- If the ADC needs to run on a particular adc\_clk\_sar frequency to achieve a sample rate and the HPPERCLK is not a proper multiple for such clock frequency, a higher frequency system clock, HFRCO, can be chosen to be ADC\_CLK using ASYNC mode. This allows HPPERCLK to be set to an optimum value from a system view point.
- ASYNC mode can also help with digital noise mitigation as this clock is asynchronous (not balanced) with the system clock. Moreover, the user can use the invert option to invert the source of ASYNCCLK helping in noise mitigation further.
- Whenever ADC is being used in asynchronous mode, then HPPERCLK must be at least 1.5 times higher than the ADC\_CLK.
- With ASNEEDED setting for ASYNCCLK request, the ADC\_CLK power can be reduced.

### 27.3.16 Window Compare Function

The ADC supports a window compare function on both the latest single and scan outputs. The compare thresholds, ADGT and ADLT, are defined in the ADCn\_CMPTHR register. These are 16-bit values and their format must match the type of conversion (single-ended or differential) the user is trying to compare with. For example, a 12-bit differential conversion is sign extended to 16 bits while a 12-bit single-ended conversion result would get zero padded to 16-bit result before comparing with ADGT and ADLT. If over-sampling is enabled, the conversion result could grow to 16-bits. There is a single set of ADLT and ADGT threshold for both single and scan compare. The user can however enable single or scan compare logic individually by enabling CMPEN in ADCn\_SINGLECTRL or ADCn\_SCANCTRL register.

The user can perform comparison both within or outside of the window defined by the ADGT and ADLT. If the ADLT is greater than ADGT, the ADC compares if the current sample is within the window. Otherwise, the ADC compares if the current sample is outside of the window.

### 27.3.17 ADC Programming Model

The ADC configuration registers are considered static and can only be updated when (1) ADC is in SYNC mode and (2) ADC is idle. ADC is considered busy when it is doing conversions (either the SINGLEACT or SCANACT status flag is high) or when it is warmed up (one of the following status flags is high: WARM, SINGLEREFWARM, SCANREFWARM). The following registers are considered ADC configuration registers: CMU\_ADCCTRL, ADCn\_CTRL, ADCn\_SINGLECTRL, ADCn\_SINGLECTRLX, ADCn\_SCANCTRL, ADCn\_SCANCTRLX, ADCn\_SCANINPUTSEL, ADCn\_SCANNEGSEL, ADCn\_IEN, ADCn\_BIASPROG, ADCn\_SCANMASK, ADCn\_CAL and ADCn\_CMPTHR.

From reset, the ADC is in SYNC mode by default. The user can program the configuration registers as needed. If PRS is to be used, PRSEN in ADCn\_SINGLECTRL/ADCn\_SCANCTRL should be set after all other configuration is complete. Once configuration is complete, the ADC is ready to receive triggers. The user must ensure that no LESENSE triggers come in during the time the ADC configuration registers are being updated.

After the ADC has been used to perform conversions, the user must ensure that the ADC is idle before updating the configuration registers. The first step is to ensure that no new triggers (PRS, LESENSE) are being issued. It can take a few cycles from when a trigger is received to when SINGLEACT/SCANACT flags go high due to synchronization requirement. If it is unclear when the triggers were issued and if those are under synchronization or not, the user should add a small delay before checking the status flags. If the SINGLEACT/SCANACT status flags are high, the corresponding STOP command should be issued and the user should wait until the SINGLEACT/SCANACT flags go low. If the ADC was warmed up, then the WARMUPMODE should be changed to NORMAL and then the user should wait on WARM, SINGLEREFWARM and SCANREFWARM flags until those go low. Now the ADC is idle.

If both LESENSE scan and PRS/software scan conversions are taking place, then since there are two scans occurring, the SCAN STOP command needs to be issued twice. The user can check the SCANPENDING status flag. If the flag is set then the user needs to send out 2 SCAN STOP commands. After sending out the first SCAN STOP, the user needs to wait until the SCANPENDING flag goes low. Then the second SCAN STOP command should be issued and the user should wait on the SCANACT status flag to go low.

#### Note:

When switching ADCCLKMODE in the ADCn\_CTRL register, use the appropriate sequence below:

- SYNC to ASYNC:
  1. Disable ADC interrupts
  2. Clear the FIFOs
  3. Switch the ADCCLKMODE

If the ADC is to be used in ASYNC clock mode with WARMUPMODE set to KEEPADCWARM, then both ADCCLKMODE and WARMUPMODE fields in the ADCn\_CTRL register should be set to the desired values in the same register write. This will ensure that the ADC power-on sequence is valid.

- ASYNC TO SYNC:
  1. Disable ADC interrupts
  2. Switch the ADCCLKMODE
  3. Clear the FIFOs

The FIFOs are cleared by writing 1 to the ADCn\_SCANFIFOCLEAR and ADCn\_SINGLEFIFOCLEAR registers.

When switching from ASYNC to SYNC, ensure that the ASYNC clock is turned off before doing the switch.

## 27.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name                 | Type  | Description   |
|--------|----------------------|-------|---|
| 0x000  | ADCn_CTRL            | RW    | Control Register  |
| 0x008  | ADCn_CMD             | W1    | Command Register  |
| 0x00C  | ADCn_STATUS          | R     | Status Register   |
| 0x010  | ADCn_SINGLECTRL      | RW    | Single Channel Control Register   |
| 0x014  | ADCn_SINGLECTRLX     | RW    | Single Channel Control Register Continued                                 |
| 0x018  | ADCn_SCANCTRL        | RW    | Scan Control Register   |
| 0x01C  | ADCn_SCANCTRLX       | RW    | Scan Control Register Continued   |
| 0x020  | ADCn_SCANMASK        | RW    | Scan Sequence Input Mask Register   |
| 0x024  | ADCn_SCANINPUTSEL    | RW    | Input Selection Register for Scan Mode                                    |
| 0x028  | ADCn_SCANNEGSEL      | RW    | Negative Input Select Register for Scan                                   |
| 0x02C  | ADCn_CMPTHR          | RW    | Compare Threshold Register  |
| 0x030  | ADCn_BIASPROG        | RW    | Bias Programming Register for Various Analog Blocks Used in ADC Operation |
| 0x034  | ADCn_CAL             | RW    | Calibration Register  |
| 0x038  | ADCn_IF              | R     | Interrupt Flag Register   |
| 0x03C  | ADCn_IFS             | W1    | Interrupt Flag Set Register   |
| 0x040  | ADCn_IFC             | (R)W1 | Interrupt Flag Clear Register   |
| 0x044  | ADCn_IEN             | RW    | Interrupt Enable Register   |
| 0x048  | ADCn_SINGLEDATA      | R(a)  | Single Conversion Result Data   |
| 0x04C  | ADCn_SCANDATA        | R(a)  | Scan Conversion Result Data   |
| 0x050  | ADCn_SINGLEDATAP     | R     | Single Conversion Result Data Peek Register                               |
| 0x054  | ADCn_SCANDATAP       | R     | Scan Sequence Result Data Peek Register                                   |
| 0x068  | ADCn_SCANDATAAX      | R(a)  | Scan Sequence Result Data + Data Source Register                          |
| 0x06C  | ADCn_SCANDATAAXP     | R     | Scan Sequence Result Data + Data Source Peek Register                     |
| 0x07C  | ADCn_APORTREQ        | R     | APOINT Request Status Register  |
| 0x080  | ADCn_APORTCONFLICT   | R     | APOINT Conflict Status Register   |
| 0x084  | ADCn_SINGLEFIFOCOUNT | R     | Single FIFO Count Register  |
| 0x088  | ADCn_SCANFIFOCOUNT   | R     | Scan FIFO Count Register  |
| 0x08C  | ADCn_SINGLEFIFOCLEAR | W1    | Single FIFO Clear Register  |
| 0x090  | ADCn_SCANFIFOCLEAR   | W1    | Scan FIFO Clear Register  |
| 0x094  | ADCn_APORTMASTERDIS  | RW    | APOINT Bus Master Disable Register  |

## 27.5 Register Description

### 27.5.1 ADCn\_CTRL - Control Register

| Offset        | Bit Position     |    |           |         |          |    |    |    |          |    |    |    |    |    |    |    |       |    |    |    |            |            |          |   |           |             |            |    |     |    |    |   |
|---------------|------------------|----|-----------|---------|----------|----|----|----|----------|----|----|----|----|----|----|----|-------|----|----|----|------------|------------|----------|---|-----------|-------------|------------|----|-----|----|----|---|
| 0x000         | 31               | 30 | 29        | 28      | 27       | 26 | 25 | 24 | 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15    | 14 | 13 | 12 | 11         | 10         | 9        | 8 | 7         | 6           | 5          | 4  | 3   | 2  | 1  | 0 |
| <b>Reset</b>  | 0x0              |    | 0         | 0       | 0x0      |    |    |    | 0x1F     |    |    |    |    |    |    |    | 0x00  |    |    |    | 0          | 0          | 0        |   | 0         | 0           | 0          | 0  | 0x0 |    |    |   |
| <b>Access</b> | RW               |    | RW        | RW      | RW       |    |    |    | RW       |    |    |    |    |    |    |    | RW    |    |    |    | RW         | RW         | RW       |   | RW        | RW          | RW         | RW | RW  | RW | RW |   |
| <b>Name</b>   | CHCONREFWARMIDLE |    | CHCONMODE | DBGHALT | OVSRSSEL |    |    |    | TIMEBASE |    |    |    |    |    |    |    | PRESC |    |    |    | ADCCLKMODE | ASYNCCLKEN | TAILGATE |   | SCANDMAWU | SINGLEDMAWU | WARMUPMODE |    |     |    |    |   |

| Bit   | Name   | Reset  | Access | Description  |       |             |             |   |           |   |   |            |  |   |          |  |
|-------|--|--|--------|--|-------|-------------|-------------|---|-----------|---|---|------------|--|---|----------|--|
| 31:30 | CHCONREFWARMIDLE   | 0x0  | RW     | <b>Channel Connect and Reference Warm Sel When ADC is IDLE</b><br>Channel connect and reference warm preference<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>PREFSCAN</td> <td>Keep scan reference warm and APORT switches for first scan channel closed if WARMUPMODE is not NORMAL</td> </tr> <tr> <td>1</td> <td>PREFSINGLE</td> <td>Keep single reference warm and keep APORT switches for single channel closed if WARMUPMODE is not NORMAL</td> </tr> <tr> <td>2</td> <td>KEEPPREV</td> <td>Keep last used reference warm and keep APORT switches for corresponding channel closed if WARMUPMODE is not NORMAL</td> </tr> </tbody> </table> | Value | Mode        | Description | 0   | PREFSCAN  | Keep scan reference warm and APORT switches for first scan channel closed if WARMUPMODE is not NORMAL | 1 | PREFSINGLE | Keep single reference warm and keep APORT switches for single channel closed if WARMUPMODE is not NORMAL | 2 | KEEPPREV | Keep last used reference warm and keep APORT switches for corresponding channel closed if WARMUPMODE is not NORMAL |
| Value | Mode   | Description  |        |  |       |             |             |   |           |   |   |            |  |   |          |  |
| 0     | PREFSCAN   | Keep scan reference warm and APORT switches for first scan channel closed if WARMUPMODE is not NORMAL              |        |  |       |             |             |   |           |   |   |            |  |   |          |  |
| 1     | PREFSINGLE   | Keep single reference warm and keep APORT switches for single channel closed if WARMUPMODE is not NORMAL           |        |  |       |             |             |   |           |   |   |            |  |   |          |  |
| 2     | KEEPPREV   | Keep last used reference warm and keep APORT switches for corresponding channel closed if WARMUPMODE is not NORMAL |        |  |       |             |             |   |           |   |   |            |  |   |          |  |
| 29    | CHCONMODE  | 0  | RW     | <b>Channel Connect</b><br>Selects Channel Connect Mode<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>MAXSETTLE</td> <td>Connect APORT switches for the next input as soon as possible. This optimizes settling time.</td> </tr> <tr> <td>1</td> <td>MAXRESP</td> <td>Connect APORT switches for the next input at the end of the conversion.</td> </tr> </tbody> </table>  | Value | Mode        | Description | 0   | MAXSETTLE | Connect APORT switches for the next input as soon as possible. This optimizes settling time.          | 1 | MAXRESP    | Connect APORT switches for the next input at the end of the conversion.                                  |   |          |  |
| Value | Mode   | Description  |        |  |       |             |             |   |           |   |   |            |  |   |          |  |
| 0     | MAXSETTLE  | Connect APORT switches for the next input as soon as possible. This optimizes settling time.                       |        |  |       |             |             |   |           |   |   |            |  |   |          |  |
| 1     | MAXRESP  | Connect APORT switches for the next input at the end of the conversion.  |        |  |       |             |             |   |           |   |   |            |  |   |          |  |
| 28    | DBGHALT  | 0  | RW     | <b>Debug Mode Halt Enable</b><br>Selects ADC behavior during debug mode.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Continue operation as normal during debug mode.</td> </tr> <tr> <td>1</td> <td>Complete the current conversion and then halt during debug mode.</td> </tr> </tbody> </table>  | Value | Description | 0           | Continue operation as normal during debug mode. | 1         | Complete the current conversion and then halt during debug mode.                                      |   |            |  |   |          |  |
| Value | Description  |  |        |  |       |             |             |   |           |   |   |            |  |   |          |  |
| 0     | Continue operation as normal during debug mode.                  |  |        |  |       |             |             |   |           |   |   |            |  |   |          |  |
| 1     | Complete the current conversion and then halt during debug mode. |  |        |  |       |             |             |   |           |   |   |            |  |   |          |  |
| 27:24 | OVSRSSEL   | 0x0  | RW     | <b>Oversample Rate Select</b><br>Select oversampling rate. Oversampling must be enabled for this setting to take effect.   |       |             |             |   |           |   |   |            |  |   |          |  |

| Bit   | Name   | Reset   | Access   | Description  |
|-------|--|---|--|--|
|       | Value  | Mode  |  | Description  |
|       | 0  | X2  |  | 2 samples for each conversion result                         |
|       | 1  | X4  |  | 4 samples for each conversion result                         |
|       | 2  | X8  |  | 8 samples for each conversion result                         |
|       | 3  | X16   |  | 16 samples for each conversion result                        |
|       | 4  | X32   |  | 32 samples for each conversion result                        |
|       | 5  | X64   |  | 64 samples for each conversion result                        |
|       | 6  | X128  |  | 128 samples for each conversion result                       |
|       | 7  | X256  |  | 256 samples for each conversion result                       |
|       | 8  | X512  |  | 512 samples for each conversion result                       |
|       | 9  | X1024   |  | 1024 samples for each conversion result                      |
|       | 10   | X2048   |  | 2048 samples for each conversion result                      |
|       | 11   | X4096   |  | 4096 samples for each conversion result                      |
| 23    | <i>Reserved</i>  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i>                   |  |  |
| 22:16 | TIMEBASE   | 0x1F  | RW   | <b>1us Time Base</b>   |
|       | Sets the time base used for the ADC warm up sequence based on ADC_CLK. The TIMEBASE field should be set equal to produce timing of 1us or greater. |   |  |  |
|       | Value  | Description   |  |  |
|       | TIMEBASE   | ADC STANDBY/SLOWACC mode warm-up is set to 1 x (TIMEBASE + 1) ADC_CLK cycles and NORMAL mode warm-up is set to 5 x (TIMEBASE + 1) ADC_CLK cycles. |  |  |
| 15    | <i>Reserved</i>  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i>                   |  |  |
| 14:8  | PRESC  | 0x00  | RW   | <b>Prescaler Setting for ADC Sample and Conversion Clock</b> |
|       | Sets the prescale factor to generate the ADC conversion clock (adc_sar_clk) from ADC_CLK.  |   |  |  |
|       | Value  | Description   |  |  |
|       | PRESC  | Clock prescale factor. ADC_CLK is divided by (PRESC+1) to produce adc_clk_sar.  |  |  |
| 7     | ADCCLKMODE   | 0   | RW   | <b>ADC Clock Mode</b>  |
|       | Selects ADC_CLK source as synchronous or asynchronous - with respect to the Peripheral Clock (HFPERCLK).   |   |  |  |
|       | Value  | Mode  | Description  |  |
|       | 0  | SYNC  | Synchronous clocking. Uses HFPERCLK to generate ADC_CLK, ADC will not be available in EM2 in this mode.  |  |
|       | 1  | ASYNC   | Asynchronous clocking. Uses clk_adc_async coming from CMU to generate ADC_CLK. ADC might be available in EM2 in this mode if the CLK_ADC_ASYNC is available in EM2 |  |

| Bit | Name            | Reset   | Access | Description  |
|-----|-----------------|---|--------|--|
| 6   | ASYNCCLKEN      | 0   | RW     | <b>Selects ASYNC CLK Enable Mode When ADCCLKMODE=1</b><br>Write a 1 to keep ASYNC CLK always enabled.  |
|     | Value           | Mode  |        | Description  |
|     | 0               | ASNEEDED  |        | ASYNC CLK is enabled only during ADC Conversion.   |
|     | 1               | ALWAYSON  |        | ASYNC CLK is always enabled.   |
| 5   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 4   | TAILGATE        | 0   | RW     | <b>Conversion Tailgating</b><br>Enable/disable conversion tailgating. Single channel conversions wait for a scan sequence to finish before starting. |
|     | Value           |   |        | Description  |
|     | 0               |   |        | Scan sequence has priority, but can be delayed by ongoing single channels.   |
|     | 1               |   |        | Scan sequence has priority and single channels will only start immediately after completion of a scan sequence.                                      |
| 3   | SCANDMAWU       | 0   | RW     | <b>SCANFIFO DMA Wakeup</b><br>Selects whether to wakeup the DMA controller when in EM2 and DVL is reached in SCANFIFO                                |
|     | Value           |   |        | Description  |
|     | 0               |   |        | While in EM2, the DMA controller will not get requests about DVL reached in SCANFIFO   |
|     | 1               |   |        | DMA is available in EM2 for processing SCANFIFO DVL request  |
| 2   | SINGLEDMAWU     | 0   | RW     | <b>SINGLEFIFO DMA Wakeup</b><br>Selects whether to wakeup the DMA controller when in EM2 and DVL is reached in SINGLEFIFO                            |
|     | Value           |   |        | Description  |
|     | 0               |   |        | While in EM2, the DMA controller will not get requests about Data Valid Level (DVL) reached in SINGLEFIFO  |
|     | 1               |   |        | DMA is available in EM2 for processing SINGLEFIFO DVL request  |
| 1:0 | WARMUPMODE      | 0x0   | RW     | <b>Warm-up Mode</b><br>Select Warm-up Mode for ADC   |
|     | Value           | Mode  |        | Description  |
|     | 0               | NORMAL  |        | ADC is shut down after each conversion. 5us warmup time is used before each conversion.  |
|     | 1               | KEEPINSTANDBY   |        | ADC is kept in standby mode between conversions. 1us warmup time is used before each conversion.   |
|     | 2               | KEEPINSLOWACC   |        | ADC is kept in slow acquisition mode between conversions. 1us warm-up time is used before each conversion.   |
|     | 3               | KEEPADCWARM   |        | ADC is kept on after conversions, allowing for continuous conversion.  |



### 27.5.3 ADCn\_STATUS - Status Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |          |    |    |    |    |    |   |      |         |             |               |   |   |   |   |   |   |             |         |           |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----------|----|----|----|----|----|---|------|---------|-------------|---------------|---|---|---|---|---|---|-------------|---------|-----------|
| 0x00C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16     | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8    | 7       | 6           | 5             | 4 | 3 | 2 | 1 | 0 |   |             |         |           |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0      | 0        |    |    |    |    |    |   | 0    | 0x0     |             |               |   |   |   |   | 0 | 0 | 0           | 0       |           |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R      | R        |    |    |    |    |    |   | R    | R       |             |               |   |   |   |   | R | R | R           | R       |           |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | SCANDV | SINGLEDV |    |    |    |    |    |   | WARM | PROGERR | SCANREFWARM | SINGLEREFWARM |   |   |   |   |   |   | SCANPENDING | SCANACT | SINGLEACT |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 31:18 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 17    | SCANDV          | 0   | R      | <b>Scan Data Valid</b><br>SCANCTRLX_DVL # of scan conversion data results are available in Scan FIFO.  |
| 16    | SINGLEDV        | 0   | R      | <b>Single Channel Data Valid</b><br>SINGLECTRLX_DVL # of single channel conversion results are available in Single FIFO.   |
| 15:13 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 12    | WARM            | 0   | R      | <b>ADC Warmed Up</b><br>ADC is warmed up.  |
| 11:10 | PROGERR         | 0x0   | R      | <b>Programming Error Status</b><br>Programming Error Status  |
|       | Mode            | Value   |        | Description  |
|       | BUSCONF         | x1  |        | APOINT reported a BUS Conflict.  |
|       | NEGSELCONF      | 1x  |        | SINGLECTRL's NEGSEL choice is invalid with respect to POSSEL choice. Occurs when two X channels or two Y channels are selected.  |
| 9     | SCANREFWARM     | 0   | R      | <b>Scan Reference Warmed Up</b><br>Reference selected for scan mode is warmed up.  |
| 8     | SINGLEREFWARM   | 0   | R      | <b>Single Channel Reference Warmed Up</b><br>Reference selected for single channel mode is warmed up.  |
| 7:3   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 2     | SCANPENDING     | 0   | R      | <b>Scan Conversion Pending</b><br>Indicates that either an external scan (e.g., lesense triggered) or a PRS/software triggered scan has gone pending. SCANPENDIF and SCANEXTPENDIF show which one of two went pending. |
| 1     | SCANACT         | 0   | R      | <b>Scan Conversion Active</b><br>Scan sequence is active or has pending conversions.   |

---

| Bit | Name      | Reset | Access | Description  |
|-----|-----------|-------|--------|--|
| 0   | SINGLEACT | 0     | R      | <b>Single Channel Conversion Active</b><br>Single channel conversion is active or has pending conversions. |

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### 27.5.4 ADCn\_SINGLECTRL - Single Channel Control Register

| Offset        | Bit Position |    |       |    |    |     |    |    |    |    |    |        |    |    |    |    |    |    |    |        |    |    |   |   |   |     |   |   |     |   |   |     |      |     |
|---------------|--------------|----|-------|----|----|-----|----|----|----|----|----|--------|----|----|----|----|----|----|----|--------|----|----|---|---|---|-----|---|---|-----|---|---|-----|------|-----|
| 0x010         | 31           | 30 | 29    | 28 | 27 | 26  | 25 | 24 | 23 | 22 | 21 | 20     | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12     | 11 | 10 | 9 | 8 | 7 | 6   | 5 | 4 | 3   | 2 | 1 | 0   |      |     |
| <b>Reset</b>  | 0            |    | 0     |    |    | 0x0 |    |    |    |    |    | 0xFF   |    |    |    |    |    |    |    | 0xFF   |    |    |   |   |   | 0x0 |   |   | 0x0 |   |   |     |      |     |
| <b>Access</b> | RW           |    | RW    |    |    | RW  |    |    |    |    |    | RW     |    |    |    |    |    |    |    | RW     |    |    |   |   |   | RW  |   |   | RW  |   |   |     |      |     |
| <b>Name</b>   | CMPEN        |    | PRSEN |    |    | AT  |    |    |    |    |    | NEGSEL |    |    |    |    |    |    |    | POSSEL |    |    |   |   |   | REF |   |   | RES |   |   | ADJ | DIFF | REP |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 31    | CMPEN           | 0   | RW     | <b>Compare Logic Enable for Single Channel</b><br>Enable/disable Compare Logic             |
|       | Value           |   |        | Description  |
|       | 0               |   |        | Disable Compare Logic.   |
|       | 1               |   |        | Enable Compare Logic.  |
| 30    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 29    | PRSEN           | 0   | RW     | <b>Single Channel PRS Trigger Enable</b><br>Enabled/disable PRS trigger of single channel. |
|       | Value           |   |        | Description  |
|       | 0               |   |        | Single channel is not triggered by PRS input.  |
|       | 1               |   |        | Single channel is triggered by PRS input selected by PRSSEL.                               |
| 28    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 27:24 | AT              | 0x0   | RW     | <b>Single Channel Acquisition Time</b><br>Select the acquisition time for single channel.  |
|       | Value           | Mode  |        | Description  |
|       | 0               | 1CYCLE  |        | 1 conversion clock cycle acquisition time for single channel                               |
|       | 1               | 2CYCLES   |        | 2 conversion clock cycles acquisition time for single channel                              |
|       | 2               | 3CYCLES   |        | 3 conversion clock cycles acquisition time for single channel                              |
|       | 3               | 4CYCLES   |        | 4 conversion clock cycles acquisition time for single channel                              |
|       | 4               | 8CYCLES   |        | 8 conversion clock cycles acquisition time for single channel                              |
|       | 5               | 16CYCLES  |        | 16 conversion clock cycles acquisition time for single channel                             |
|       | 6               | 32CYCLES  |        | 32 conversion clock cycles acquisition time for single channel                             |
|       | 7               | 64CYCLES  |        | 64 conversion clock cycles acquisition time for single channel                             |
|       | 8               | 128CYCLES   |        | 128 conversion clock cycles acquisition time for single channel                            |
|       | 9               | 256CYCLES   |        | 256 conversion clock cycles acquisition time for single channel                            |

| Bit  | Name   | Reset                         | Access | Description                                    |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
|--|--------|-------------------------------|--------|--|------|-------|-------------|------------|---|-------------------|------------|---|-------------------|-----|-----|-------|-------------|----|--------------------|------------|----|-------------------|------------|----|-------------------|-------------|----|--------------------|------------|----|-------------------|------------|----|-------------------|-----|-----|-------|-------------|----|--------------------|------------|----|-------------------|------------|----|-------------------|-----|-----|-------|-------------|----|--------------------|------------|----|-------------------|------------|----|-------------------|-----|-----|-------|-------------|-----|--------------------|------------|-----|-------------------|------------|-----|-------------------|-----|-----|-------|-------------|-----|--------------------|-------|-----|-------------------------------|-----|-----|-----|
| 23:16  | NEGSEL | 0xFF                          | RW     | <b>Single Channel Negative Input Selection</b> |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| <p>Selects the negative input to the ADC for Single Channel Differential mode (in case of singled ended mode, the negative input is grounded). The user can choose any of the 32 channels of any of the 5 BUSES but must ensure that POSSEL and NEGSEL are chosen from different resources (X or Y) BUS. In case of an invalid configuration, the ADC will perform a single-ended sampling and issue a BUSCONFLICT IRQ.</p>  |        |                               |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| <table border="1"> <thead> <tr> <th>Mode</th> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>APORT0XCH0</td> <td>0</td> <td>Select APORT0XCH0</td> </tr> <tr> <td>APORT0XCH1</td> <td>1</td> <td>Select APORT0XCH1</td> </tr> <tr> <td>...</td> <td>...</td> <td>.....</td> </tr> <tr> <td>APORT0XCH15</td> <td>15</td> <td>Select APORT0XCH15</td> </tr> <tr> <td>APORT0YCH0</td> <td>16</td> <td>Select APORT0YCH0</td> </tr> <tr> <td>APORT0YCH1</td> <td>17</td> <td>Select APORT0YCH1</td> </tr> <tr> <td>APORT0YCH15</td> <td>31</td> <td>Select APORT0YCH15</td> </tr> <tr> <td>APORT1XCH0</td> <td>32</td> <td>Select APORT1XCH0</td> </tr> <tr> <td>APORT1YCH1</td> <td>33</td> <td>Select APORT1YCH1</td> </tr> <tr> <td>...</td> <td>...</td> <td>.....</td> </tr> <tr> <td>APORT1YCH31</td> <td>63</td> <td>Select APORT1YCH31</td> </tr> <tr> <td>APORT2YCH0</td> <td>64</td> <td>Select APORT2YCH0</td> </tr> <tr> <td>APORT2XCH1</td> <td>65</td> <td>Select APORT2XCH1</td> </tr> <tr> <td>...</td> <td>...</td> <td>.....</td> </tr> <tr> <td>APORT2XCH31</td> <td>95</td> <td>Select APORT2XCH31</td> </tr> <tr> <td>APORT3XCH0</td> <td>96</td> <td>Select APORT3XCH0</td> </tr> <tr> <td>APORT3YCH1</td> <td>97</td> <td>Select APORT3YCH1</td> </tr> <tr> <td>...</td> <td>...</td> <td>.....</td> </tr> <tr> <td>APORT3YCH31</td> <td>127</td> <td>Select APORT3YCH31</td> </tr> <tr> <td>APORT4YCH0</td> <td>128</td> <td>Select APORT4YCH0</td> </tr> <tr> <td>APORT4XCH1</td> <td>129</td> <td>Select APORT4XCH1</td> </tr> <tr> <td>...</td> <td>...</td> <td>.....</td> </tr> <tr> <td>APORT4XCH31</td> <td>159</td> <td>Select APORT4XCH31</td> </tr> <tr> <td>TESTN</td> <td>245</td> <td>Reserved for future expansion</td> </tr> <tr> <td>VSS</td> <td>255</td> <td>VSS</td> </tr> </tbody> </table> |        |                               |        |  | Mode | Value | Description | APORT0XCH0 | 0 | Select APORT0XCH0 | APORT0XCH1 | 1 | Select APORT0XCH1 | ... | ... | ..... | APORT0XCH15 | 15 | Select APORT0XCH15 | APORT0YCH0 | 16 | Select APORT0YCH0 | APORT0YCH1 | 17 | Select APORT0YCH1 | APORT0YCH15 | 31 | Select APORT0YCH15 | APORT1XCH0 | 32 | Select APORT1XCH0 | APORT1YCH1 | 33 | Select APORT1YCH1 | ... | ... | ..... | APORT1YCH31 | 63 | Select APORT1YCH31 | APORT2YCH0 | 64 | Select APORT2YCH0 | APORT2XCH1 | 65 | Select APORT2XCH1 | ... | ... | ..... | APORT2XCH31 | 95 | Select APORT2XCH31 | APORT3XCH0 | 96 | Select APORT3XCH0 | APORT3YCH1 | 97 | Select APORT3YCH1 | ... | ... | ..... | APORT3YCH31 | 127 | Select APORT3YCH31 | APORT4YCH0 | 128 | Select APORT4YCH0 | APORT4XCH1 | 129 | Select APORT4XCH1 | ... | ... | ..... | APORT4XCH31 | 159 | Select APORT4XCH31 | TESTN | 245 | Reserved for future expansion | VSS | 255 | VSS |
| Mode   | Value  | Description                   |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| APORT0XCH0   | 0      | Select APORT0XCH0             |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| APORT0XCH1   | 1      | Select APORT0XCH1             |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| ...  | ...    | .....                         |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| APORT0XCH15  | 15     | Select APORT0XCH15            |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| APORT0YCH0   | 16     | Select APORT0YCH0             |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| APORT0YCH1   | 17     | Select APORT0YCH1             |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| APORT0YCH15  | 31     | Select APORT0YCH15            |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| APORT1XCH0   | 32     | Select APORT1XCH0             |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| APORT1YCH1   | 33     | Select APORT1YCH1             |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| ...  | ...    | .....                         |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| APORT1YCH31  | 63     | Select APORT1YCH31            |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| APORT2YCH0   | 64     | Select APORT2YCH0             |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| APORT2XCH1   | 65     | Select APORT2XCH1             |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| ...  | ...    | .....                         |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| APORT2XCH31  | 95     | Select APORT2XCH31            |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| APORT3XCH0   | 96     | Select APORT3XCH0             |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| APORT3YCH1   | 97     | Select APORT3YCH1             |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| ...  | ...    | .....                         |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| APORT3YCH31  | 127    | Select APORT3YCH31            |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| APORT4YCH0   | 128    | Select APORT4YCH0             |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| APORT4XCH1   | 129    | Select APORT4XCH1             |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| ...  | ...    | .....                         |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| APORT4XCH31  | 159    | Select APORT4XCH31            |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| TESTN  | 245    | Reserved for future expansion |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |
| VSS  | 255    | VSS                           |        |  |      |       |             |            |   |                   |            |   |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |    |                    |            |    |                   |            |    |                   |     |     |       |             |     |                    |            |     |                   |            |     |                   |     |     |       |             |     |                    |       |     |                               |     |     |     |

|      |        |      |    |  |
|------|--------|------|----|--|
| 15:8 | POSSEL | 0xFF | RW | <b>Single Channel Positive Input Selection</b> |
|------|--------|------|----|--|

Selects the positive input to the ADC for single channel operation. Software can choose any of the 32 channels of any BUS as positive input. In DIFF mode POSSEL and NEGSEL need to be chosen from different resources (X or Y). If an X BUS is connected to POSSEL, only a Y BUS can connect to NEGSEL, and vice-versa. The user can also select some internal nodes as positive input for single-ended sampling. These internal nodes cannot be sampled differentially.

| Mode       | Value | Description       |
|------------|-------|-------------------|
| APORT0XCH0 | 0     | Select APORT0XCH0 |
| APORT0XCH1 | 1     | Select APORT0XCH1 |

| Bit | Name        | Reset | Access | Description  |
|-----|-------------|-------|--------|--|
| ... |             | ...   |        | .....  |
|     | APORT0XCH15 | 15    |        | Select APORT0XCH15   |
|     | APORT0YCH0  | 16    |        | Select APORT0YCH0  |
|     | APORT0YCH1  | 17    |        | Select APORT0YCH1  |
|     | APORT0YCH15 | 31    |        | Select APORT0YCH15   |
|     | APORT1XCH0  | 32    |        | Select APORT1XCH0  |
|     | APORT1YCH1  | 33    |        | Select APORT1YCH1  |
| ... |             | ...   |        | .....  |
|     | APORT1YCH31 | 63    |        | Select APORT1YCH31   |
|     | APORT2YCH0  | 64    |        | Select APORT2YCH0  |
|     | APORT2XCH1  | 65    |        | Select APORT2XCH1  |
| ... |             | ...   |        | .....  |
|     | APORT2XCH31 | 95    |        | Select APORT2XCH31   |
|     | APORT3XCH0  | 96    |        | Select APORT3XCH0  |
|     | APORT3YCH1  | 97    |        | Select APORT3YCH1  |
| ... |             | ...   |        | .....  |
|     | APORT3YCH31 | 127   |        | Select APORT3YCH31   |
|     | APORT4YCH0  | 128   |        | Select APORT4YCH0  |
|     | APORT4XCH1  | 129   |        | Select APORT4XCH1  |
| ... |             | ...   |        | .....  |
|     | APORT4XCH31 | 159   |        | Select APORT4XCH31   |
|     | AVDD        | 224   |        | Select AVDD  |
|     | BUVDD       | 225   |        | Select BUVDD   |
|     | DVDD        | 226   |        | Select DVDD  |
|     | PAVDD       | 227   |        | Reserved for future use  |
|     | DECOUPLE    | 228   |        | Select DECOUPLE  |
|     | IOVDD       | 229   |        | Select IOVDD   |
|     | IOVDD1      | 230   |        | Select IOVDD1. Not Applicable if no IOVDD1 is available.                       |
|     | VSP         | 231   |        | Reserved for future expansion  |
|     | OPA2        | 242   |        | OPA2 output. Not Applicable if no OPA is available.                            |
|     | TEMP        | 243   |        | Temperature sensor   |
|     | DAC0OUT0    | 244   |        | DAC0 output 0. Not Applicable if no DAC is available.                          |
|     | R5VOUT      | 245   |        | 5V sub-system ADC mux output. Not Applicable if no 5V sub-system is available. |
|     | SP1         | 246   |        | Reserved for future expansion  |
|     | SP2         | 247   |        | Reserved for future expansion  |
|     | DAC0OUT1    | 248   |        | DAC0 output 1. Not Applicable if no DAC is available.                          |

| Bit | Name   | Reset     | Access | Description  |
|-----|--------|-----------|--------|--|
|     | SUBLSB | 249       |        | SUBLSB measurement enabled.  |
|     | OPA3   | 250       |        | OPA3 output. Not Applicable if no OPA is available.  |
|     | VSS    | 255       |        | VSS  |
| 7:5 | REF    | 0x0       | RW     | <b>Single Channel Reference Selection</b><br>Select reference to ADC single channel mode.      |
|     | Value  | Mode      |        | Description  |
|     | 0      | 1V25      |        | VFS = 1.25V with internal VBGR reference   |
|     | 1      | 2V5       |        | VFS = 2.5V with internal VBGR reference  |
|     | 2      | VDD       |        | VFS = AVDD with AVDD as reference source   |
|     | 3      | 5V        |        | VFS = 5V with internal VBGR reference  |
|     | 4      | EXTSINGLE |        | Single ended external reference  |
|     | 5      | 2XEXTDIFF |        | Differential external reference, 2x  |
|     | 6      | 2XVDD     |        | VFS = 2xAVDD with AVDD as the reference source   |
|     | 7      | CONF      |        | Use SINGLECTRLX to configure reference   |
| 4:3 | RES    | 0x0       | RW     | <b>Single Channel Resolution Select</b><br>Select single channel conversion resolution.        |
|     | Value  | Mode      |        | Description  |
|     | 0      | 12BIT     |        | 12-bit resolution.   |
|     | 1      | 8BIT      |        | 8-bit resolution.  |
|     | 2      | 6BIT      |        | 6-bit resolution.  |
|     | 3      | OVS       |        | Oversampling enabled. Oversampling rate is set in OVSRSSEL.                                    |
| 2   | ADJ    | 0         | RW     | <b>Single Channel Result Adjustment</b><br>Select single channel result adjustment.            |
|     | Value  | Mode      |        | Description  |
|     | 0      | RIGHT     |        | Results are right adjusted.  |
|     | 1      | LEFT      |        | Results are left adjusted.   |
| 1   | DIFF   | 0         | RW     | <b>Single Channel Differential Mode</b><br>Select single ended or differential input.          |
|     | Value  |           |        | Description  |
|     | 0      |           |        | Single ended input.  |
|     | 1      |           |        | Differential input.  |
| 0   | REP    | 0         | RW     | <b>Single Channel Repetitive Mode</b><br>Enable/disable repetitive single channel conversions. |
|     | Value  |           |        | Description  |

| Bit | Name | Reset | Access | Description  |
|-----|------|-------|--------|--|
| 0   |      |       |        | ADC will perform one conversion per trigger in single channel mode.                          |
| 1   |      |       |        | ADC will repeat conversions in single channel mode continuously until SINGLESTOP is written. |

### 27.5.5 ADCn\_SINGLECTRLX - Single Channel Control Register Continued

| Offset        | Bit Position |    |    |                  |                |    |    |    |    |        |    |    |         |    |          |     |    |        |    |    |         |     |   |   |   |   |            |         |     |   |   |   |  |  |
|---------------|--------------|----|----|------------------|----------------|----|----|----|----|--------|----|----|---------|----|----------|-----|----|--------|----|----|---------|-----|---|---|---|---|------------|---------|-----|---|---|---|--|--|
| 0x014         | 31           | 30 | 29 | 28               | 27             | 26 | 25 | 24 | 23 | 22     | 21 | 20 | 19      | 18 | 17       | 16  | 15 | 14     | 13 | 12 | 11      | 10  | 9 | 8 | 7 | 6 | 5          | 4       | 3   | 2 | 1 | 0 |  |  |
| <b>Reset</b>  | 0x0          |    |    | 0                | 0x00           |    |    |    |    | 0x0    |    |    | 0       |    | 0        | 0x0 |    | 0x0    |    |    | 0       | 0x0 |   |   |   |   |            | 0       | 0x0 |   |   |   |  |  |
| <b>Access</b> | RW           |    |    | RW               | RW             |    |    |    |    | RW     |    |    | RW      |    | RW       | RW  |    | RW     |    |    | RW      | RW  |   |   |   |   |            | RW      | RW  |   |   |   |  |  |
| <b>Name</b>   | REPDELAY     |    |    | CONVSTARTDELAYEN | CONVSTARTDELAY |    |    |    |    | PRSSEL |    |    | PRSMODE |    | FIFOFACT | DVL |    | VINATT |    |    | VREFATT |     |   |   |   |   | VREFATTFIX | VREFSEL |     |   |   |   |  |  |

| Bit   | Name              | Reset   | Access | Description  |
|-------|-------------------|---|--------|--|
| 31:29 | REPDELAY          | 0x0   | RW     | <b>REPDELAY Select for SINGLE REP Mode</b><br>Delay value between two repeated conversions.  |
|       | Value             | Mode  |        | Description  |
|       | 0                 | NODELAY   |        | No delay   |
|       | 1                 | 4CYCLES   |        | 4 conversion clock cycles  |
|       | 2                 | 8CYCLES   |        | 8 conversion clock cycles  |
|       | 3                 | 16CYCLES  |        | 16 conversion clock cycles   |
|       | 4                 | 32CYCLES  |        | 32 conversion clock cycles   |
|       | 5                 | 64CYCLES  |        | 64 conversion clock cycles   |
|       | 6                 | 128CYCLES   |        | 128 conversion clock cycles  |
|       | 7                 | 256CYCLES   |        | 256 conversion clock cycles  |
| 28    | <i>Reserved</i>   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 27    | CONVSTARTDELAY-EN | 0   | RW     | <b>Enable Delaying Next Conversion Start</b><br>Delay value for next conversion start event.   |
|       | Value             |   |        | Description  |
|       | 0                 |   |        | CONVSTARTDELAY is disabled.  |
|       | 1                 |   |        | CONVSTARTDELAY is enabled.   |
| 26:22 | CONVSTARTDELAY    | 0x00  | RW     | <b>Delay Value for Next Conversion Start If CONVSTARTDELAYEN is Set</b><br>Delay value for next conversion start event in 1us ticks (based on TIMEBASE). |
|       | Value             |   |        | Description  |
|       | DELAY             |   |        | Delay the next conversion start by (CONVSTARTDELAY+1) us   |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 21    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 20:17 | PRSEL           | 0x0   | RW     | <b>Single Channel PRS Trigger Select</b><br>Select PRS trigger for single channel.  |
|       | Value           | Mode  |        | Description   |
|       | 0               | PRSCH0  |        | PRS ch 0 triggers single channel  |
|       | 1               | PRSCH1  |        | PRS ch 1 triggers single channel  |
|       | 2               | PRSCH2  |        | PRS ch 2 triggers single channel  |
|       | 3               | PRSCH3  |        | PRS ch 3 triggers single channel  |
|       | 4               | PRSCH4  |        | PRS ch 4 triggers single channel  |
|       | 5               | PRSCH5  |        | PRS ch 5 triggers single channel  |
|       | 6               | PRSCH6  |        | PRS ch 6 triggers single channel  |
|       | 7               | PRSCH7  |        | PRS ch 7 triggers single channel  |
|       | 8               | PRSCH8  |        | PRS ch 8 triggers single channel  |
|       | 9               | PRSCH9  |        | PRS ch 9 triggers single channel  |
|       | 10              | PRSCH10   |        | PRS ch 10 triggers single channel   |
|       | 11              | PRSCH11   |        | PRS ch 11 triggers single channel   |
| 16    | PRSMODE         | 0   | RW     | <b>Single Channel PRS Trigger Mode</b><br>PRS trigger mode of single channel.   |
|       | Value           | Mode  |        | Description   |
|       | 0               | PULSED  |        | Single channel trigger is considered a regular asynchronous pulse that starts ADC warm-up, then acquisition/conversion sequence. The ADC_CLK controls the warmup-time.  |
|       | 1               | TIMED   |        | Single channel trigger should be a pulse long enough to provide the required warm-up time for the selected ADC warmup mode. The negative edge requests sample acquisition. DELAY can be used to delay the warm-up request if the pulse is too long. |
| 15    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 14    | FIFOFACT        | 0   | RW     | <b>Single Channel FIFO Overflow Action</b><br>Select how FIFO behaves when full   |
|       | Value           | Mode  |        | Description   |
|       | 0               | DISCARD   |        | FIFO stops accepting new data if full, triggers SINGLEOF IRQ.   |
|       | 1               | OVERWRITE   |        | FIFO overwrites old data when full, triggers SINGLEOF IRQ.  |
| 13:12 | DVL             | 0x0   | RW     | <b>Single Channel DV Level Select</b><br>Select single channel Data Valid level. SINGLE IRQ is set when (DVL+1) number of single channels have been converted and their results are available in the Single FIFO.                                   |

| Bit  | Name       | Reset      | Access | Description   |
|------|------------|------------|--------|---|
| 11:8 | VINATT     | 0x0        | RW     | <b>Code for VIN Attenuation Factor</b><br>Used to set the VIN attenuation factor.   |
| 7:4  | VREFATT    | 0x0        | RW     | <b>Code for VREF Attenuation Factor When VREFSEL is 1, 2 or 5</b><br>Used to set VREF attenuation factor.   |
| 3    | VREFATTFIX | 0          | RW     | <b>Enable Fixed Scaling on VREF</b><br>Enables fixed scaling on VREF  |
|      | Value      |            |        | Description   |
|      | 0          |            |        | VREFATT setting is used to scale VREF when VREFSEL is 1, 2 or 5.  |
|      | 1          |            |        | A fixed VREF attenuation is used to cover a large reference source range. When VREFATT = 0, the scaling factor is 1/4. For non-zero values of VREFATT, the scaling factor is 1/3. |
| 2:0  | VREFSEL    | 0x0        | RW     | <b>Single Channel Reference Selection</b><br>Select reference VREF to ADC single channel mode.  |
|      | Value      | Mode       |        | Description   |
|      | 0          | VBGR       |        | Internal 0.83V Bandgap reference  |
|      | 1          | VDDXWATT   |        | Scaled AVDD: $AVDD \cdot (\text{the VREF attenuation factor})$  |
|      | 2          | VREFPWATT  |        | Scaled singled ended external Vref: $ADCn\_EXTP \cdot (\text{the VREF attenuation factor})$   |
|      | 3          | VREFP      |        | Raw single ended external Vref: $ADCn\_EXTP$  |
|      | 4          | VENTROPY   |        | Special mode used to generate ENTROPY.  |
|      | 5          | VREFPNWATT |        | Scaled differential external Vref from : $(ADCn\_EXTP - ADCn\_EXTN) \cdot (\text{the VREF attenuation factor})$   |
|      | 6          | VREFPN     |        | Raw differential external Vref from : $(ADCn\_EXTP - ADCn\_EXTN)$   |
|      | 7          | VBGRLOW    |        | Internal Bandgap reference at low setting 0.78V   |

### 27.5.6 ADCn\_SCANCTRL - Scan Control Register

| Offset        | Bit Position |    |       |    |    |     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |     |   |     |   |     |      |     |
|---------------|--------------|----|-------|----|----|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|-----|---|-----|---|-----|------|-----|
| 0x018         | 31           | 30 | 29    | 28 | 27 | 26  | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6   | 5 | 4   | 3 | 2   | 1    | 0   |
| <b>Reset</b>  | 0            |    | 0     |    |    | 0x0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   | 0x0 |   | 0x0 |   | 0   | 0    | 0   |
| <b>Access</b> | RW           |    | RW    |    |    | RW  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   | RW  |   | RW  |   | RW  | RW   | RW  |
| <b>Name</b>   | CMPEN        |    | PRSEN |    |    | AT  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   | REF |   | RES |   | ADJ | DIFF | REP |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 31    | CMPEN           | 0   | RW     | <b>Compare Logic Enable for Scan</b><br>Enable/disable Compare Logic                     |
|       | Value           |   |        | Description  |
|       | 0               |   |        | Disable Compare Logic.   |
|       | 1               |   |        | Enable Compare Logic.  |
| 30    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 29    | PRSEN           | 0   | RW     | <b>Scan Sequence PRS Trigger Enable</b><br>Enabled/disable PRS trigger of scan sequence. |
|       | Value           |   |        | Description  |
|       | 0               |   |        | Scan sequence is not triggered by PRS input  |
|       | 1               |   |        | Scan sequence is triggered by PRS input selected by PRSSEL                               |
| 28    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 27:24 | AT              | 0x0   | RW     | <b>Scan Acquisition Time</b><br>Select the acquisition time for scan.                    |
|       | Value           | Mode  |        | Description  |
|       | 0               | 1CYCLE  |        | 1 conversion clock cycle acquisition time for scan                                       |
|       | 1               | 2CYCLES   |        | 2 conversion clock cycles acquisition time for scan                                      |
|       | 2               | 3CYCLES   |        | 3 conversion clock cycles acquisition time for scan                                      |
|       | 3               | 4CYCLES   |        | 4 conversion clock cycles acquisition time for scan                                      |
|       | 4               | 8CYCLES   |        | 8 conversion clock cycles acquisition time for scan                                      |
|       | 5               | 16CYCLES  |        | 16 conversion clock cycles acquisition time for scan                                     |
|       | 6               | 32CYCLES  |        | 32 conversion clock cycles acquisition time for scan                                     |
|       | 7               | 64CYCLES  |        | 64 conversion clock cycles acquisition time for scan                                     |
|       | 8               | 128CYCLES   |        | 128 conversion clock cycles acquisition time for scan                                    |
|       | 9               | 256CYCLES   |        | 256 conversion clock cycles acquisition time for scan                                    |

| Bit  | Name     | Reset  | Access | Description   |
|------|----------|--|--------|---|
| 23:8 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 7:5  | REF      | 0x0  | RW     | <b>Scan Sequence Reference Selection</b><br>Select reference to ADC scan sequence.    |
|      | Value    | Mode   |        | Description   |
|      | 0        | 1V25   |        | VFS = 1.25V with internal VBGR reference  |
|      | 1        | 2V5  |        | VFS = 2.5V with internal VBGR reference   |
|      | 2        | VDD  |        | VFS = AVDD with AVDD as reference source  |
|      | 3        | 5V   |        | VFS = 5V with internal VBGR reference   |
|      | 4        | EXTSINGLE  |        | Single ended external reference   |
|      | 5        | 2XEXTDIFF  |        | Differential external reference, 2x   |
|      | 6        | 2XVDD  |        | VFS=2xAVDD with AVDD as the reference source  |
|      | 7        | CONF   |        | Use SCANCTRLX to configure reference  |
| 4:3  | RES      | 0x0  | RW     | <b>Scan Sequence Resolution Select</b><br>Select scan sequence conversion resolution. |
|      | Value    | Mode   |        | Description   |
|      | 0        | 12BIT  |        | 12-bit resolution   |
|      | 1        | 8BIT   |        | 8-bit resolution  |
|      | 2        | 6BIT   |        | 6-bit resolution  |
|      | 3        | OVS  |        | Oversampling enabled. Oversampling rate is set in OVSRSSEL                            |
| 2    | ADJ      | 0  | RW     | <b>Scan Sequence Result Adjustment</b><br>Select scan sequence result adjustment.     |
|      | Value    | Mode   |        | Description   |
|      | 0        | RIGHT  |        | Results are right adjusted  |
|      | 1        | LEFT   |        | Results are left adjusted   |
| 1    | DIFF     | 0  | RW     | <b>Scan Sequence Differential Mode</b><br>Select single ended or differential input.  |
|      | Value    |  |        | Description   |
|      | 0        |  |        | Single ended input  |
|      | 1        |  |        | Differential input  |
| 0    | REP      | 0  | RW     | <b>Scan Sequence Repetitive Mode</b><br>Enable/disable repetitive scan sequence.      |
|      | Value    |  |        | Description   |
|      | 0        |  |        | Scan conversion mode is deactivated after one sequence.                               |

---

| Bit | Name | Reset | Access | Description  |
|-----|------|-------|--------|--|
|     | 1    |       |        | Scan conversion mode repeats continuously until SCANSTOP is written. |

---

### 27.5.7 ADCn\_SCANCTRLX - Scan Control Register Continued

| Offset        | Bit Position |    |    |                  |                |    |    |    |    |       |    |    |    |         |    |          |     |    |        |    |    |    |         |     |   |            |         |   |   |   |   |   |  |  |  |  |
|---------------|--------------|----|----|------------------|----------------|----|----|----|----|-------|----|----|----|---------|----|----------|-----|----|--------|----|----|----|---------|-----|---|------------|---------|---|---|---|---|---|--|--|--|--|
| 0x01C         | 31           | 30 | 29 | 28               | 27             | 26 | 25 | 24 | 23 | 22    | 21 | 20 | 19 | 18      | 17 | 16       | 15  | 14 | 13     | 12 | 11 | 10 | 9       | 8   | 7 | 6          | 5       | 4 | 3 | 2 | 1 | 0 |  |  |  |  |
| <b>Reset</b>  | 0x0          |    |    | 0                | 0x00           |    |    |    |    | 0x0   |    |    |    | 0       |    | 0        | 0x0 |    | 0x0    |    |    |    | 0       | 0x0 |   |            |         |   |   |   |   |   |  |  |  |  |
| <b>Access</b> | RW           |    |    | RW               | RW             |    |    |    |    | RW    |    |    |    | RW      |    | RW       | RW  |    | RW     |    |    |    | RW      | RW  |   |            |         |   |   |   |   |   |  |  |  |  |
| <b>Name</b>   | REPDELAY     |    |    | CONVSTARTDELAYEN | CONVSTARTDELAY |    |    |    |    | PRSEL |    |    |    | PRSMODE |    | FIFOFACT | DVL |    | VINATT |    |    |    | VREFATT |     |   | VREFATTFIX | VREFSEL |   |   |   |   |   |  |  |  |  |

| Bit   | Name              | Reset   | Access | Description   |
|-------|-------------------|---|--------|---|
| 31:29 | REPDELAY          | 0x0   | RW     | <b>REPDELAY Select for SCAN REP Mode</b><br>Delay value between two repeated conversions.   |
|       | Value             | Mode  |        | Description   |
|       | 0                 | NODELAY   |        | No delay  |
|       | 1                 | 4CYCLES   |        | 4 conversion clock cycles   |
|       | 2                 | 8CYCLES   |        | 8 conversion clock cycles   |
|       | 3                 | 16CYCLES  |        | 16 conversion clock cycles  |
|       | 4                 | 32CYCLES  |        | 32 conversion clock cycles  |
|       | 5                 | 64CYCLES  |        | 64 conversion clock cycles  |
|       | 6                 | 128CYCLES   |        | 128 conversion clock cycles   |
|       | 7                 | 256CYCLES   |        | 256 conversion clock cycles   |
| 28    | <i>Reserved</i>   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 27    | CONVSTARTDELAY-EN | 0   | RW     | <b>Enable Delaying Next Conversion Start</b><br>Delay value for next conversion start event.  |
|       | Value             |   |        | Description   |
|       | 0                 |   |        | CONVSTARTDELAY is disabled  |
|       | 1                 |   |        | CONVSTARTDELAY is enabled.  |
| 26:22 | CONVSTARTDELAY    | 0x00  | RW     | <b>Delay Next Conversion Start If CONVSTARTDELAYEN is Set</b><br>Delay value for next conversion start event in 1us ticks (based on TIMEBASE) |
|       | Value             |   |        | Description   |
|       | DELAY             |   |        | Delay the next conversion start by (DELAY+1) us   |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 21    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 20:17 | PRSEL           | 0x0   | RW     | <b>Scan Sequence PRS Trigger Select</b><br>Select PRS trigger for scan sequence.  |
|       | Value           | Mode  |        | Description   |
|       | 0               | PRSCH0  |        | PRS ch 0 triggers scan sequence   |
|       | 1               | PRSCH1  |        | PRS ch 1 triggers scan sequence   |
|       | 2               | PRSCH2  |        | PRS ch 2 triggers scan sequence   |
|       | 3               | PRSCH3  |        | PRS ch 3 triggers scan sequence   |
|       | 4               | PRSCH4  |        | PRS ch 4 triggers scan sequence   |
|       | 5               | PRSCH5  |        | PRS ch 5 triggers scan sequence   |
|       | 6               | PRSCH6  |        | PRS ch 6 triggers scan sequence   |
|       | 7               | PRSCH7  |        | PRS ch 7 triggers scan sequence   |
|       | 8               | PRSCH8  |        | PRS ch 8 triggers scan sequence   |
|       | 9               | PRSCH9  |        | PRS ch 9 triggers scan sequence   |
|       | 10              | PRSCH10   |        | PRS ch 10 triggers scan sequence  |
|       | 11              | PRSCH11   |        | PRS ch 11 triggers scan sequence  |
| 16    | PRSMODE         | 0   | RW     | <b>Scan PRS Trigger Mode</b><br>PRS trigger mode of scan.   |
|       | Value           | Mode  |        | Description   |
|       | 0               | PULSED  |        | Scan trigger is considered a regular async pulse that starts ADC warm-up, then acquisition/conversion sequence. The ADC_CLK controls the warmup-time.   |
|       | 1               | TIMED   |        | Scan trigger should be a pulse long enough to provide the required warm-up time for the selected ADC warmup mode. The negative edge requests sample acquisition. DELAY can be used to delay the warm-up request if the pulse is too long. |
| 15    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 14    | FIFOFACT        | 0   | RW     | <b>Scan FIFO Overflow Action</b><br>Select how FIFO behaves when full   |
|       | Value           | Mode  |        | Description   |
|       | 0               | DISCARD   |        | FIFO stops accepting new data if full, triggers SCANOF IRQ.   |
|       | 1               | OVERWRITE   |        | FIFO overwrites old data when full, triggers SCANOF IRQ.  |
| 13:12 | DVL             | 0x0   | RW     | <b>Scan DV Level Select</b><br>Select Scan Data Valid level. SCAN IRQ is set when (DVL+1) number of scan channels have been converted and their results are available in the SCAN FIFO.   |

| Bit  | Name       | Reset      | Access | Description   |
|------|------------|------------|--------|---|
| 11:8 | VINATT     | 0x0        | RW     | <b>Code for VIN Attenuation Factor</b><br>Used to set the VIN attenuation factor.   |
| 7:4  | VREFATT    | 0x0        | RW     | <b>Code for VREF Attenuation Factor When VREFSEL is 1, 2 or 5</b><br>Used to set VREF attenuation factor.   |
| 3    | VREFATTFIX | 0          | RW     | <b>Enable Fixed Scaling on VREF</b><br>Enables fixed scaling on VREF  |
|      | Value      |            |        | Description   |
|      | 0          |            |        | VREFATT setting is used to scale VREF when VREFSEL is 1, 2 or 5.  |
|      | 1          |            |        | A fixed VREF attenuation is used to cover a large reference source range. When VREFATT = 0, the scaling factor is 1/4. For non-zero values of VREFATT, the scaling factor is 1/3. |
| 2:0  | VREFSEL    | 0x0        | RW     | <b>Scan Channel Reference Selection</b><br>Select reference VREF to ADC scan channel mode.  |
|      | Value      | Mode       |        | Description   |
|      | 0          | VBGR       |        | Internal 0.83V Bandgap reference  |
|      | 1          | VDDXWATT   |        | Scaled AVDD: $AVDD \times (\text{the VREF attenuation factor})$   |
|      | 2          | VREFPWATT  |        | Scaled singled ended external Vref: $ADCn\_EXTP \times (\text{the VREF attenuation factor})$  |
|      | 3          | VREFP      |        | Raw single ended external Vref: $ADCn\_EXTP$  |
|      | 5          | VREFPNWATT |        | Scaled differential external Vref from : $(ADCn\_EXTP - ADCn\_EXTN) \times (\text{the VREF attenuation factor})$  |
|      | 6          | VREFPN     |        | Raw differential external Vref from : $(ADCn\_EXTP - ADCn\_EXTN)$   |
|      | 7          | VBGRLOW    |        | Internal Bandgap reference at low setting 0.78V   |

### 27.5.8 ADCn\_SCANMASK - Scan Sequence Input Mask Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |             |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------------|
| 0x020         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0           |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0x00000000  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | RW          |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | SCANINPUTEN |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
|-----|------|-------|--------|-------------|

31:0 SCANINPUTEN 0x00000000 RW **Scan Sequence Input Mask**

Set one or more bits in this mask to select which inputs are included in scan sequence in either single ended or differential mode. This works with SCANINPUTSEL register. The SCANINPUTSEL chooses 32 possible channels for single-ended or 32 pairs of possible channels for differential scanning from BUSES. These chosen channels are referred as ADCn\_INPUTx in the description. Four even inputs from first group of 8 ADCn\_INPUTx and four odd inputs from second group of 8 ADCn\_INPUTx have programmable NEGSEL, defined in SCANNEGSEL register. If the SCANMASK is set to 0 and scan conversion is triggered, ADC will do a conversion with garbage results since no inputs were enabled for conversion.

| Mode                    | Value                               | Description  |
|-------------------------|-------------------------------------|--|
| DIFF = 0                |                                     |  |
| INPUT0                  | xxxxxxxxxxxxxxxxxxxx<br>xxxxxxxx1   | ADCn_INPUT0 included in mask   |
| INPUT1                  | xxxxxxxxxxxxxxxxxxxx<br>xxxxxxxx1x  | ADCn_INPUT1 included in mask   |
| INPUT2                  | xxxxxxxxxxxxxxxxxxxx<br>xxxxxxxx1xx | ADCn_INPUT2 included in mask   |
| INPUT3                  | xxxxxxxxxxxxxxxxxxxx<br>xxxxxx1xxx  | ADCn_INPUT3 included in mask   |
| INPUT4                  | xxxxxxxxxxxxxxxxxxxx<br>xxxxx1xxxx  | ADCn_INPUT4 included in mask   |
| INPUT5                  | xxxxxxxxxxxxxxxxxxxx<br>xxxxx1xxxx  | ADCn_INPUT5 included in mask   |
| INPUT6                  | xxxxxxxxxxxxxxxxxxxx<br>xxx1xxxxx   | ADCn_INPUT6 included in mask   |
| INPUT7                  | xxxxxxxxxxxxxxxxxxxx<br>xx1xxxxxx   | ADCn_INPUT7 included in mask   |
| ...                     | .....                               | .....  |
| INPUT31                 | 1xxxxxxxxxxxxxxxxx<br>xxxxxxxx      | ADCn_INPUT31 included in mask  |
| DIFF = 1                |                                     |  |
| INPUT0INPUT0NEG-<br>SEL | xxxxxxxxxxxxxxxxxxxx<br>xxxxxxxx1   | (Positive input: ADCn_INPUT0 Negative input: chosen by IN-<br>PUT0NEGSEL) included in mask |

| Bit   | Name                 | Reset                                   | Access | Description   |
|-------|----------------------|---|--------|---|
|       | INPUT1INPUT2         | xxxxxxxxxxxxxxxxxxxxx<br>xxxxxxxx1x     |        | (Positive input: ADCn_INPUT1 Negative input: ADCn_INPUT2) included in mask              |
|       | INPUT2INPUT2NEGSEL   | xxxxxxxxxxxxxxxxxxxxx<br>xxxxxxxx1xx    |        | (Positive input: ADCn_INPUT2 Negative input: chosen by INPUT2NEGSEL) included in mask   |
|       | INPUT3INPUT4         | xxxxxxxxxxxxxxxxxxxxx<br>xxxxxx1xxx     |        | (Positive input: ADCn_INPUT3 Negative input: ADCn_INPUT4) included in mask              |
|       | INPUT4INPUT4NEGSEL   | xxxxxxxxxxxxxxxxxxxxx<br>xxxxx1xxxx     |        | (Positive input: ADCn_INPUT4 Negative input: chosen by INPUT4NEGSEL) included in mask   |
|       | INPUT5INPUT6         | xxxxxxxxxxxxxxxxxxxxx<br>xxxxx1xxxx     |        | (Positive input: ADCn_INPUT5 Negative input: ADCn_INPUT6) included in mask              |
|       | INPUT6INPUT6NEGSEL   | xxxxxxxxxxxxxxxxxxxxx<br>xxx1xxxxxx     |        | (Positive input: ADCn_INPUT6 Negative input: chosen by INPUT6NEGSEL) included in mask   |
|       | INPUT7INPUT0         | xxxxxxxxxxxxxxxxxxxxx<br>xxx1xxxxxx     |        | (Positive input: ADCn_INPUT7 Negative input: ADCn_INPUT8) included in mask              |
|       | INPUT8INPUT9         | xxxxxxxxxxxxxxxxxxxxx<br>xx1xxxxxxx     |        | (Positive input: ADCn_INPUT8 Negative input: ADCn_INPUT9) included in mask              |
|       | INPUT9INPUT9NEGSEL   | xxxxxxxxxxxxxxxxxxxxx<br>x1xxxxxxx      |        | (Positive input: ADCn_INPUT9 Negative input: chosen by INPUT9NEGSEL) included in mask   |
|       | INPUT10INPUT11       | xxxxxxxxxxxxxxxxxxxxx<br>1xxxxxxxx      |        | (Positive input: ADCn_INPUT10 Negative input: ADCn_INPUT11) included in mask            |
|       | INPUT11INPUT11NEGSEL | xxxxxxxxxxxxxxxxxxxxx1<br>xxxxxxxx      |        | (Positive input: ADCn_INPUT11 Negative input: chosen by INPUT11NEGSEL) included in mask |
|       | INPUT12INPUT13       | xxxxxxxxxxxxxxxxxxxxx1x<br>xxxxxxxx     |        | (Positive input: ADCn_INPUT12 Negative input: ADCn_INPUT13) included in mask            |
|       | INPUT13INPUT13NEGSEL | xxxxxxxxxxxxxxxxxxxxx1xx<br>xxxxxxxx    |        | (Positive input: ADCn_INPUT13 Negative input: chosen by INPUT13NEGSEL) included in mask |
|       | INPUT14INPUT15       | xxxxxxxxxxxxxxxxxxxxx1xxx<br>xxxxxxxx   |        | (Positive input: ADCn_INPUT14 Negative input: ADCn_INPUT15) included in mask            |
|       | INPUT15INPUT15NEGSEL | xxxxxxxxxxxxxxxxxxxxx1xxxx<br>xxxxxxxx  |        | (Positive input: ADCn_INPUT15 Negative input: chosen by INPUT15NEGSEL) included in mask |
|       | INPUT16INPUT17       | xxxxxxxxxxxxxxxxxxxxx1xxxxx<br>xxxxxxxx |        | (Positive input: ADCn_INPUT16 Negative input: ADCn_INPUT17) included in mask            |
| ..... | .....                | .....                                   |        | .....   |
|       | INPUT28INPUT29       | xxx1xxxxxxxxxxxxxxxx<br>xxxxxxxx        |        | (Positive input: ADCn_INPUT28 Negative input: ADCn_INPUT29) included in mask            |
|       | INPUT29INPUT30       | xx1xxxxxxxxxxxxxxxx<br>xxxxxxxx         |        | (Positive input: ADCn_INPUT29 Negative input: ADCn_INPUT30) included in mask            |
|       | INPUT30INPUT31       | x1xxxxxxxxxxxxxxxx<br>xxxxxxxx          |        | (Positive input: ADCn_INPUT30 Negative input: ADCn_INPUT31) included in mask            |
|       | INPUT31INPUT24       | 1xxxxxxxxxxxxxxxx<br>xxxxxxxx           |        | (Positive input: ADCn_INPUT31 Negative input: ADCn_INPUT24) included in mask            |

### 27.5.9 ADCn\_SCANINPUTSEL - Input Selection Register for Scan Mode

| Offset        | Bit Position   |    |    |    |    |    |    |                |    |    |    |    |    |    |               |    |    |    |    |    |    |              |   |   |   |   |   |   |   |   |   |   |
|---------------|----------------|----|----|----|----|----|----|----------------|----|----|----|----|----|----|---------------|----|----|----|----|----|----|--------------|---|---|---|---|---|---|---|---|---|---|
| 0x024         | 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24             | 23 | 22 | 21 | 20 | 19 | 18 | 17            | 16 | 15 | 14 | 13 | 12 | 11 | 10           | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0x00           |    |    |    |    |    |    | 0x00           |    |    |    |    |    |    | 0x00          |    |    |    |    |    |    | 0x00         |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> | RW             |    |    |    |    |    |    | RW             |    |    |    |    |    |    | RW            |    |    |    |    |    |    | RW           |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | INPUT24TO31SEL |    |    |    |    |    |    | INPUT16TO23SEL |    |    |    |    |    |    | INPUT8TO15SEL |    |    |    |    |    |    | INPUT0TO7SEL |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name            | Reset   | Access | Description |
|-------|-----------------|---|--------|-------------|
| 31:29 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |             |

|       |                |       |    |  |
|-------|----------------|-------|----|--|
| 28:24 | INPUT24TO31SEL | 0x00  | RW | <b>Inputs Chosen for ADCn_INPUT24-ADCn_INPUT31 as Referred in SCANMASK</b> |
|       | Mode           | Value |    | Description  |
|       | APORT0CH0TO7   | 0     |    | Select APORT0's CH0-CH7 as ADCn_INPUT24-ADCn_INPUT31                       |
|       | APORT0CH8TO15  | 1     |    | Select APORT0's CH8-CH15 as ADCn_INPUT24-ADCn_INPUT31                      |
|       | APORT1CH0TO7   | 4     |    | Select APORT1's CH0-CH7 as ADCn_INPUT24-ADCn_INPUT31                       |
|       | APORT1CH8TO15  | 5     |    | Select APORT1's CH8-CH15 as ADCn_INPUT24-ADCn_INPUT31                      |
|       | APORT1CH16TO23 | 6     |    | Select APORT1's CH16-CH23 as ADCn_INPUT24-ADCn_INPUT31                     |
|       | APORT1CH24TO31 | 7     |    | Select APORT1's CH24-CH31 as ADCn_INPUT24-ADCn_INPUT31                     |
|       | APORT2CH0TO7   | 8     |    | Select APORT2's CH0-CH7 as ADCn_INPUT24-ADCn_INPUT31                       |
|       | ...            | .     |    | .....  |
|       | APORT3CH0TO7   | 12    |    | Select APORT3's CH0-CH7 as ADCn_INPUT24-ADCn_INPUT31                       |
|       | ...            | .     |    | .....  |
|       | APORT4CH0TO7   | 16    |    | Select APORT4's CH0-CH7 as ADCn_INPUT24-ADCn_INPUT31                       |
|       | ...            | .     |    | .....  |

|       |                 |   |  |  |
|-------|-----------------|---|--|--|
| 23:21 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |  |
|-------|-----------------|---|--|--|

|       |                |       |    |  |
|-------|----------------|-------|----|--|
| 20:16 | INPUT16TO23SEL | 0x00  | RW | <b>Inputs Chosen for ADCn_INPUT16-ADCn_INPUT23 as Referred in SCANMASK</b> |
|       | Mode           | Value |    | Description  |
|       | APORT0CH0TO7   | 0     |    | Select APORT0's CH0-CH7 as ADCn_INPUT16-ADCn_INPUT23                       |
|       | APORT0CH8TO15  | 1     |    | Select APORT0's CH8-CH15 as ADCn_INPUT16-ADCn_INPUT23                      |
|       | APORT1CH0TO7   | 4     |    | Select APORT1's CH0-CH7 as ADCn_INPUT16-ADCn_INPUT23                       |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
|       | APORT1CH8TO15   | 5   |        | Select APORT1's CH8-CH15 as ADCn_INPUT16-ADCn_INPUT23                     |
|       | APORT1CH16TO23  | 6   |        | Select APORT1's CH16-CH23 as ADCn_INPUT16-ADCn_INPUT23                    |
|       | APORT1CH24TO31  | 7   |        | Select APORT1's CH24-CH31 as ADCn_INPUT16-ADCn_INPUT23                    |
|       | APORT2CH0TO7    | 8   |        | Select APORT2's CH0-CH7 as ADCn_INPUT16-ADCn_INPUT23                      |
|       | ...             | .   |        | .....   |
|       | APORT3CH0TO7    | 12  |        | Select APORT3's CH0-CH7 as ADCn_INPUT16-ADCn_INPUT23                      |
|       | ...             | .   |        | .....   |
|       | APORT4CH0TO7    | 16  |        | Select APORT4's CH0-CH7 as ADCn_INPUT16-ADCn_INPUT23                      |
|       | ...             | .   |        | .....   |
| 15:13 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 12:8  | INPUT8TO15SEL   | 0x00  | RW     | <b>Inputs Chosen for ADCn_INPUT8-ADCn_INPUT15 as Referred in SCANMASK</b> |
|       | Mode            | Value   |        | Description   |
|       | APORT0CH0TO7    | 0   |        | Select APORT0's CH0-CH7 as ADCn_INPUT8-ADCn_INPUT15                       |
|       | APORT0CH8TO15   | 1   |        | Select APORT0's CH8-CH15 as ADCn_INPUT8-ADCn_INPUT15                      |
|       | APORT1CH0TO7    | 4   |        | Select APORT1's CH0-CH7 as ADCn_INPUT8-ADCn_INPUT15                       |
|       | APORT1CH8TO15   | 5   |        | Select APORT1's CH8-CH15 as ADCn_INPUT8-ADCn_INPUT15                      |
|       | APORT1CH16TO23  | 6   |        | Select APORT1's CH16-CH23 as ADCn_INPUT8-ADCn_INPUT15                     |
|       | APORT1CH24TO31  | 7   |        | Select APORT1's CH24-CH31 as ADCn_INPUT8-ADCn_INPUT15                     |
|       | APORT2CH0TO7    | 8   |        | Select APORT2's CH0-CH7 as ADCn_INPUT8-ADCn_INPUT15                       |
|       | ...             | .   |        | .....   |
|       | APORT3CH0TO7    | 12  |        | Select APORT3's CH0-CH7 as ADCn_INPUT8-ADCn_INPUT15                       |
|       | ...             | .   |        | .....   |
|       | APORT4CH0TO7    | 16  |        | Select APORT4's CH0-CH7 as ADCn_INPUT8-ADCn_INPUT15                       |
|       | ...             | .   |        | .....   |
| 7:5   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 4:0   | INPUT0TO7SEL    | 0x00  | RW     | <b>Inputs Chosen for ADCn_INPUT7-ADCn_INPUT0 as Referred in SCANMASK</b>  |
|       | Mode            | Value   |        | Description   |
|       | APORT0CH0TO7    | 0   |        | Select APORT0's CH0-CH7 as ADCn_INPUT0-ADCn_INPUT7                        |
|       | APORT0CH8TO15   | 1   |        | Select APORT0's CH8-CH15 as ADCn_INPUT0-ADCn_INPUT7                       |
|       | APORT1CH0TO7    | 4   |        | Select APORT1's CH0-CH7 as ADCn_INPUT0-ADCn_INPUT7                        |
|       | APORT1CH8TO15   | 5   |        | Select APORT1's CH8-CH15 as ADCn_INPUT0-ADCn_INPUT7                       |
|       | APORT1CH16TO23  | 6   |        | Select APORT1's CH16-CH23 as ADCn_INPUT0-ADCn_INPUT7                      |

| Bit | Name           | Reset | Access | Description  |
|-----|----------------|-------|--------|--|
|     | APORT1CH24TO31 | 7     |        | Select APORT1's CH24-CH31 as ADCn_INPUT0-ADCn_INPUT7 |
|     | APORT2CH0TO7   | 8     |        | Select APORT2's CH0-CH7 as ADCn_INPUT0-ADCn_INPUT7   |
|     | ...            | .     |        | .....  |
|     | APORT3CH0TO7   | 12    |        | Select APORT3's CH0-CH7 as ADCn_INPUT0-ADCn_INPUT7   |
|     | ...            | .     |        | .....  |
|     | APORT4CH0TO7   | 16    |        | Select APORT4's CH0-CH7 as ADCn_INPUT0-ADCn_INPUT7   |
|     | ...            | .     |        | .....  |

### 27.5.10 ADCn\_SCANNEGSEL - Negative Input Select Register for Scan

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |               |               |              |              |              |              |              |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|---------------|---------------|--------------|--------------|--------------|--------------|--------------|---|---|---|---|---|---|---|---|
| 0x028  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15            | 14            | 13            | 12           | 11           | 10           | 9            | 8            | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0           | 0x3           | 0x2           | 0x1          | 0x3          | 0x2          | 0x1          | 0x0          |   |   |   |   |   |   |   |   |
| Access |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW            | RW            | RW            | RW           | RW           | RW           | RW           | RW           |   |   |   |   |   |   |   |   |
| Name   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | INPUT15NEGSEL | INPUT13NEGSEL | INPUT11NEGSEL | INPUT9NEGSEL | INPUT6NEGSEL | INPUT4NEGSEL | INPUT2NEGSEL | INPUT0NEGSEL |   |   |   |   |   |   |   |   |

| Bit   | Name          | Reset  | Access | Description  |       |      |             |   |        |   |   |         |  |   |         |  |   |         |  |
|-------|---------------|--|--------|--|-------|------|-------------|---|--------|---|---|---------|--|---|---------|--|---|---------|--|
| 31:16 | Reserved      | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |       |      |             |   |        |   |   |         |  |   |         |  |   |         |  |
| 15:14 | INPUT15NEGSEL | 0x0  | RW     | <p><b>Negative Input Select Register for ADCn_INPUT15 in Differential Scan Mode</b></p> <p>Selects negative channel</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>INPUT8</td> <td>Selects ADCn_INPUT8 as negative channel input</td> </tr> <tr> <td>1</td> <td>INPUT10</td> <td>Selects ADCn_INPUT10 as negative channel input</td> </tr> <tr> <td>2</td> <td>INPUT12</td> <td>Selects ADCn_INPUT12 as negative channel input</td> </tr> <tr> <td>3</td> <td>INPUT14</td> <td>Selects ADCn_INPUT14 as negative channel input</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | INPUT8 | Selects ADCn_INPUT8 as negative channel input | 1 | INPUT10 | Selects ADCn_INPUT10 as negative channel input | 2 | INPUT12 | Selects ADCn_INPUT12 as negative channel input | 3 | INPUT14 | Selects ADCn_INPUT14 as negative channel input |
| Value | Mode          | Description  |        |  |       |      |             |   |        |   |   |         |  |   |         |  |   |         |  |
| 0     | INPUT8        | Selects ADCn_INPUT8 as negative channel input  |        |  |       |      |             |   |        |   |   |         |  |   |         |  |   |         |  |
| 1     | INPUT10       | Selects ADCn_INPUT10 as negative channel input   |        |  |       |      |             |   |        |   |   |         |  |   |         |  |   |         |  |
| 2     | INPUT12       | Selects ADCn_INPUT12 as negative channel input   |        |  |       |      |             |   |        |   |   |         |  |   |         |  |   |         |  |
| 3     | INPUT14       | Selects ADCn_INPUT14 as negative channel input   |        |  |       |      |             |   |        |   |   |         |  |   |         |  |   |         |  |
| 13:12 | INPUT13NEGSEL | 0x3  | RW     | <p><b>Negative Input Select Register for ADCn_INPUT13 in Differential Scan Mode</b></p> <p>Selects negative channel</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>INPUT8</td> <td>Selects ADCn_INPUT8 as negative channel input</td> </tr> <tr> <td>1</td> <td>INPUT10</td> <td>Selects ADCn_INPUT10 as negative channel input</td> </tr> <tr> <td>2</td> <td>INPUT12</td> <td>Selects ADCn_INPUT12 as negative channel input</td> </tr> <tr> <td>3</td> <td>INPUT14</td> <td>Selects ADCn_INPUT14 as negative channel input</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | INPUT8 | Selects ADCn_INPUT8 as negative channel input | 1 | INPUT10 | Selects ADCn_INPUT10 as negative channel input | 2 | INPUT12 | Selects ADCn_INPUT12 as negative channel input | 3 | INPUT14 | Selects ADCn_INPUT14 as negative channel input |
| Value | Mode          | Description  |        |  |       |      |             |   |        |   |   |         |  |   |         |  |   |         |  |
| 0     | INPUT8        | Selects ADCn_INPUT8 as negative channel input  |        |  |       |      |             |   |        |   |   |         |  |   |         |  |   |         |  |
| 1     | INPUT10       | Selects ADCn_INPUT10 as negative channel input   |        |  |       |      |             |   |        |   |   |         |  |   |         |  |   |         |  |
| 2     | INPUT12       | Selects ADCn_INPUT12 as negative channel input   |        |  |       |      |             |   |        |   |   |         |  |   |         |  |   |         |  |
| 3     | INPUT14       | Selects ADCn_INPUT14 as negative channel input   |        |  |       |      |             |   |        |   |   |         |  |   |         |  |   |         |  |
| 11:10 | INPUT11NEGSEL | 0x2  | RW     | <p><b>Negative Input Select Register for ADCn_INPUT11 in Differential Scan Mode</b></p> <p>Selects negative channel</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>INPUT8</td> <td>Selects ADCn_INPUT8 as negative channel input</td> </tr> <tr> <td>1</td> <td>INPUT10</td> <td>Selects ADCn_INPUT10 as negative channel input</td> </tr> <tr> <td>2</td> <td>INPUT12</td> <td>Selects ADCn_INPUT12 as negative channel input</td> </tr> <tr> <td>3</td> <td>INPUT14</td> <td>Selects ADCn_INPUT14 as negative channel input</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | INPUT8 | Selects ADCn_INPUT8 as negative channel input | 1 | INPUT10 | Selects ADCn_INPUT10 as negative channel input | 2 | INPUT12 | Selects ADCn_INPUT12 as negative channel input | 3 | INPUT14 | Selects ADCn_INPUT14 as negative channel input |
| Value | Mode          | Description  |        |  |       |      |             |   |        |   |   |         |  |   |         |  |   |         |  |
| 0     | INPUT8        | Selects ADCn_INPUT8 as negative channel input  |        |  |       |      |             |   |        |   |   |         |  |   |         |  |   |         |  |
| 1     | INPUT10       | Selects ADCn_INPUT10 as negative channel input   |        |  |       |      |             |   |        |   |   |         |  |   |         |  |   |         |  |
| 2     | INPUT12       | Selects ADCn_INPUT12 as negative channel input   |        |  |       |      |             |   |        |   |   |         |  |   |         |  |   |         |  |
| 3     | INPUT14       | Selects ADCn_INPUT14 as negative channel input   |        |  |       |      |             |   |        |   |   |         |  |   |         |  |   |         |  |

| Bit | Name         | Reset   | Access | Description   |
|-----|--------------|---------|--------|---|
| 9:8 | INPUT9NEGSEL | 0x1     | RW     | <b>Negative Input Select Register for ADCn_INPUT9 in Differential Scan Mode</b><br><br>Selects negative channel |
|     | Value        | Mode    |        | Description   |
|     | 0            | INPUT8  |        | Selects ADCn_INPUT8 as negative channel input   |
|     | 1            | INPUT10 |        | Selects ADCn_INPUT10 as negative channel input  |
|     | 2            | INPUT12 |        | Selects ADCn_INPUT12 as negative channel input  |
|     | 3            | INPUT14 |        | Selects ADCn_INPUT14 as negative channel input  |
| 7:6 | INPUT6NEGSEL | 0x3     | RW     | <b>Negative Input Select Register for ADCn_INPUT1 in Differential Scan Mode</b><br><br>Selects negative channel |
|     | Value        | Mode    |        | Description   |
|     | 0            | INPUT1  |        | Selects ADCn_INPUT1 as negative channel input   |
|     | 1            | INPUT3  |        | Selects ADCn_INPUT3 as negative channel input   |
|     | 2            | INPUT5  |        | Selects ADCn_INPUT5 as negative channel input   |
|     | 3            | INPUT7  |        | Selects ADCn_INPUT7 as negative channel input   |
| 5:4 | INPUT4NEGSEL | 0x2     | RW     | <b>Negative Input Select Register for ADCn_INPUT4 in Differential Scan Mode</b><br><br>Selects negative channel |
|     | Value        | Mode    |        | Description   |
|     | 0            | INPUT1  |        | Selects ADCn_INPUT1 as negative channel input   |
|     | 1            | INPUT3  |        | Selects ADCn_INPUT3 as negative channel input   |
|     | 2            | INPUT5  |        | Selects ADCn_INPUT5 as negative channel input   |
|     | 3            | INPUT7  |        | Selects ADCn_INPUT7 as negative channel input   |
| 3:2 | INPUT2NEGSEL | 0x1     | RW     | <b>Negative Input Select Register for ADCn_INPUT2 in Differential Scan Mode</b><br><br>Selects negative channel |
|     | Value        | Mode    |        | Description   |
|     | 0            | INPUT1  |        | Selects ADCn_INPUT1 as negative channel input   |
|     | 1            | INPUT3  |        | Selects ADCn_INPUT3 as negative channel input   |
|     | 2            | INPUT5  |        | Selects ADCn_INPUT5 as negative channel input   |
|     | 3            | INPUT7  |        | Selects ADCn_INPUT7 as negative channel input   |
| 1:0 | INPUT0NEGSEL | 0x0     | RW     | <b>Negative Input Select Register for ADCn_INPUT0 in Differential Scan Mode</b><br><br>Selects negative channel |
|     | Value        | Mode    |        | Description   |

| Bit | Name | Reset  | Access | Description                                   |
|-----|------|--------|--------|---|
| 0   |      | INPUT1 |        | Selects ADCn_INPUT1 as negative channel input |
| 1   |      | INPUT3 |        | Selects ADCn_INPUT3 as negative channel input |
| 2   |      | INPUT5 |        | Selects ADCn_INPUT5 as negative channel input |
| 3   |      | INPUT7 |        | Selects ADCn_INPUT7 as negative channel input |

### 27.5.11 ADCn\_CMPTHR - Compare Threshold Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x02C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0x0000       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | ADGT         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | ADLT   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name | Reset  | Access | Description   |
|-------|------|--------|--------|---|
| 31:16 | ADGT | 0x0000 | RW     | <b>Greater Than Compare Threshold</b><br>Compare threshold value for greater-than comparison. Must match the conversion data representation chosen. |
| 15:0  | ADLT | 0x0000 | RW     | <b>Less Than Compare Threshold</b><br>Compare threshold value for less-than comparison. Must match the conversion data representation chosen.       |

## 27.5.12 ADCn\_BIASPROG - Bias Programming Register for Various Analog Blocks Used in ADC Operation

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |           |    |    |    |    |    |   |           |   |   |   |   |   |   |             |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------|----|----|----|----|----|---|-----------|---|---|---|---|---|---|-------------|---|
| 0x030  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8         | 7 | 6 | 5 | 4 | 3 | 2 | 1           | 0 |
| Reset  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0         |    |    |    |    |    |   | 0         |   |   |   |   |   |   | 0x0         |   |
| Access |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW        |    |    |    |    |    |   | RW        |   |   |   |   |   |   | RW          |   |
| Name   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | GPBIASACC |    |    |    |    |    |   | VFAULTCLR |   |   |   |   |   |   | ADCBIASPROG |   |

| Bit   | Name        | Reset   | Access | Description  |       |      |             |   |         |   |   |        |  |   |        |                     |    |        |                     |    |         |                      |    |         |                      |
|-------|-------------|---|--------|--|-------|------|-------------|---|---------|---|---|--------|--|---|--------|---------------------|----|--------|---------------------|----|---------|----------------------|----|---------|----------------------|
| 31:17 | Reserved    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |         |   |   |        |  |   |        |                     |    |        |                     |    |         |                      |    |         |                      |
| 16    | GPBIASACC   | 0   | RW     | <b>Accuracy Setting for the System Bias During ADC Operation</b><br>Select bias accuracy mode for ADC operation. For devices with multiple ADCs, the bias will use the high accuracy setting unless all ADC instances configure GPBIASACC to LOWACC.<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>HIGHACC</td> <td>High accuracy setting. Use when configured for an internal VBGR reference source.</td> </tr> <tr> <td>1</td> <td>LOWACC</td> <td>Low accuracy setting. Can be used for all references other than VBGR to conserve energy.</td> </tr> </tbody> </table>                                       | Value | Mode | Description | 0 | HIGHACC | High accuracy setting. Use when configured for an internal VBGR reference source. | 1 | LOWACC | Low accuracy setting. Can be used for all references other than VBGR to conserve energy. |   |        |                     |    |        |                     |    |         |                      |    |         |                      |
| Value | Mode        | Description   |        |  |       |      |             |   |         |   |   |        |  |   |        |                     |    |        |                     |    |         |                      |    |         |                      |
| 0     | HIGHACC     | High accuracy setting. Use when configured for an internal VBGR reference source.   |        |  |       |      |             |   |         |   |   |        |  |   |        |                     |    |        |                     |    |         |                      |    |         |                      |
| 1     | LOWACC      | Low accuracy setting. Can be used for all references other than VBGR to conserve energy.  |        |  |       |      |             |   |         |   |   |        |  |   |        |                     |    |        |                     |    |         |                      |    |         |                      |
| 15:13 | Reserved    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |         |   |   |        |  |   |        |                     |    |        |                     |    |         |                      |    |         |                      |
| 12    | VFAULTCLR   | 0   | RW     | <b>Clear VREFOF Flag</b><br>Use this bit to request clearing of the VREFOF flag. If VREFOF irq is enabled and is triggered, the user must set this bit in the ISR to clear VREFOF. The user needs to reset this bit to enable VREFOF to trigger further IRQs upon VREF overflow conditions.  |       |      |             |   |         |   |   |        |  |   |        |                     |    |        |                     |    |         |                      |    |         |                      |
| 11:4  | Reserved    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |         |   |   |        |  |   |        |                     |    |        |                     |    |         |                      |    |         |                      |
| 3:0   | ADCBIASPROG | 0x0   | RW     | <b>Bias Programming Value of Analog ADC Block</b><br>These bits are used to adjust the bias current in ADC analog block.<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>NORMAL</td> <td>Normal power (use for 1Msps operation)</td> </tr> <tr> <td>4</td> <td>SCALE2</td> <td>Scaling bias to 1/2</td> </tr> <tr> <td>8</td> <td>SCALE4</td> <td>Scaling bias to 1/4</td> </tr> <tr> <td>12</td> <td>SCALE8</td> <td>Scaling bias to 1/8</td> </tr> <tr> <td>14</td> <td>SCALE16</td> <td>Scaling bias to 1/16</td> </tr> <tr> <td>15</td> <td>SCALE32</td> <td>Scaling bias to 1/32</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | NORMAL  | Normal power (use for 1Msps operation)  | 4 | SCALE2 | Scaling bias to 1/2  | 8 | SCALE4 | Scaling bias to 1/4 | 12 | SCALE8 | Scaling bias to 1/8 | 14 | SCALE16 | Scaling bias to 1/16 | 15 | SCALE32 | Scaling bias to 1/32 |
| Value | Mode        | Description   |        |  |       |      |             |   |         |   |   |        |  |   |        |                     |    |        |                     |    |         |                      |    |         |                      |
| 0     | NORMAL      | Normal power (use for 1Msps operation)  |        |  |       |      |             |   |         |   |   |        |  |   |        |                     |    |        |                     |    |         |                      |    |         |                      |
| 4     | SCALE2      | Scaling bias to 1/2   |        |  |       |      |             |   |         |   |   |        |  |   |        |                     |    |        |                     |    |         |                      |    |         |                      |
| 8     | SCALE4      | Scaling bias to 1/4   |        |  |       |      |             |   |         |   |   |        |  |   |        |                     |    |        |                     |    |         |                      |    |         |                      |
| 12    | SCALE8      | Scaling bias to 1/8   |        |  |       |      |             |   |         |   |   |        |  |   |        |                     |    |        |                     |    |         |                      |    |         |                      |
| 14    | SCALE16     | Scaling bias to 1/16  |        |  |       |      |             |   |         |   |   |        |  |   |        |                     |    |        |                     |    |         |                      |    |         |                      |
| 15    | SCALE32     | Scaling bias to 1/32  |        |  |       |      |             |   |         |   |   |        |  |   |        |                     |    |        |                     |    |         |                      |    |         |                      |

## 27.5.13 ADCn\_CAL - Calibration Register

| Offset | Bit Position |          |    |    |    |               |    |    |    |            |    |    |    |               |            |    |    |    |                 |    |    |    |              |   |   |   |   |   |   |   |   |   |
|--------|--------------|----------|----|----|----|---------------|----|----|----|------------|----|----|----|---------------|------------|----|----|----|-----------------|----|----|----|--------------|---|---|---|---|---|---|---|---|---|
| 0x034  | 31           | 30       | 29 | 28 | 27 | 26            | 25 | 24 | 23 | 22         | 21 | 20 | 19 | 18            | 17         | 16 | 15 | 14 | 13              | 12 | 11 | 10 | 9            | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset  | 0            | 0x40     |    |    |    | 0x7           |    |    |    | 0x8        |    |    |    | 0             | 0x40       |    |    |    | 0x7             |    |    |    | 0x8          |   |   |   |   |   |   |   |   |   |
| Access | RW           | RW       |    |    |    | RW            |    |    |    | RW         |    |    |    | RW            | RW         |    |    |    | RW              |    |    |    | RW           |   |   |   |   |   |   |   |   |   |
| Name   | CALEN        | SCANGAIN |    |    |    | SCANOFFSETINV |    |    |    | SCANOFFSET |    |    |    | OFFSETINVMODE | SINGLEGAIN |    |    |    | SINGLEOFFSETINV |    |    |    | SINGLEOFFSET |   |   |   |   |   |   |   |   |   |

| Bit   | Name            | Reset | Access | Description  |
|-------|-----------------|-------|--------|--|
| 31    | CALEN           | 0     | RW     | <b>Calibration Mode is Enabled</b><br><br>When enabled, the adc performs conversion and sends raw data to the ADC fifos. This can also be used to debug the adc data conversion  |
| 30:24 | SCANGAIN        | 0x40  | RW     | <b>Scan Mode Gain Calibration Value</b><br><br>This register contains the gain calibration value used with scan conversions. This field is set to the production gain calibration value for the 1V25 internal reference during reset, hence the reset value might differ from device to device. The field is unsigned. Higher values lead to higher ADC results.   |
| 23:20 | SCANOFFSETINV   | 0x7   | RW     | <b>Scan Mode Offset Calibration Value for Negative Single-ended Mode</b><br><br>This register contains the offset calibration value used with scan conversions for negative single-ended mode. This field is set to the production offset calibration value for the 1V25 internal reference during reset, hence the reset value might differ from device to device. The field is encoded as a signed 2's complement number. Higher values lead to lower ADC results.                                 |
| 19:16 | SCANOFFSET      | 0x8   | RW     | <b>Scan Mode Offset Calibration Value for Differential or Positive Single-ended Mode</b><br><br>This register contains the offset calibration value used with scan conversions for differential or positive single-ended mode. This field is set to the production offset calibration value for the 1V25 internal reference during reset, hence the reset value might differ from device to device. The field is encoded as a signed 2's complement number. Higher values lead to lower ADC results. |
| 15    | OFFSETINVMODE   | 0     | RW     | <b>Negative Single-ended Offset Calibration is Enabled</b><br><br>When enabled, along with CALEN bit, the ADC performs negative singled ended conversion. When not enabled, if CALEN is set, DIFF bit of SINGLECTRL register decides whether to do positive single-ended or differential conversion.   |
| 14:8  | SINGLEGAIN      | 0x40  | RW     | <b>Single Mode Gain Calibration Value</b><br><br>This register contains the gain calibration value used with single conversions. This field is set to the production gain calibration value for the 1V25 internal reference during reset, hence the reset value might differ from device to device. The field is unsigned. Higher values lead to higher ADC results.   |
| 7:4   | SINGLEOFFSETINV | 0x7   | RW     | <b>Single Mode Offset Calibration Value for Negative Single-ended Mode</b><br><br>This register contains the offset calibration value used with single conversions for negative single-ended mode. This field is set to the production offset calibration value for the 1V25 internal reference during reset, hence the reset value might differ from device to device. The field is encoded as a signed 2's complement number. Higher values lead to lower ADC results.                             |

| Bit | Name         | Reset | Access | Description  |
|-----|--------------|-------|--------|--|
| 3:0 | SINGLEOFFSET | 0x8   | RW     | <b>Single Mode Offset Calibration Value for Differential or Positive Single-ended Mode</b> |

This register contains the offset calibration value used with single conversions for differential or positive single-ended mode. This field is set to the production offset calibration value for the 1V25 internal reference during reset, hence the reset value might differ from device to device. The field is encoded as a signed 2's complement number. Higher values lead to lower ADC results.



| Bit | Name            | Reset   | Access | Description  |
|-----|-----------------|---|--------|--|
| 9   | SCANOF          | 0   | R      | <b>Scan FIFO Overflow Interrupt Flag</b><br>Indicates scan result FIFO overflow when this bit is set. An overflow occurs if there is not room in the FIFO to store a new result.     |
| 8   | SINGLEOF        | 0   | R      | <b>Single FIFO Overflow Interrupt Flag</b><br>Indicates single result FIFO overflow when this bit is set. An overflow occurs if there is not room in the FIFO to store a new result. |
| 7:2 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 1   | SCAN            | 0   | R      | <b>Scan Conversion Complete Interrupt Flag</b><br>Indicates (DVL+1) number of scan channel results are available in the Scan FIFO.   |
| 0   | SINGLE          | 0   | R      | <b>Single Conversion Complete Interrupt Flag</b><br>Indicates (DVL+1) number of single channel results are available in the Single FIFO.   |

## 27.5.15 ADCn\_IFS - Interrupt Flag Set Register

| Offset        | Bit Position |    |         |             |          |             |         |        |    |    |    |    |    |    |         |           |    |    |    |    |    |    |        |          |        |          |   |   |   |   |   |   |  |
|---------------|--------------|----|---------|-------------|----------|-------------|---------|--------|----|----|----|----|----|----|---------|-----------|----|----|----|----|----|----|--------|----------|--------|----------|---|---|---|---|---|---|--|
| 0x03C         | 31           | 30 | 29      | 28          | 27       | 26          | 25      | 24     | 23 | 22 | 21 | 20 | 19 | 18 | 17      | 16        | 15 | 14 | 13 | 12 | 11 | 10 | 9      | 8        | 7      | 6        | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    | 0       | 0           | 0        | 0           | 0       | 0      |    |    |    |    |    |    | 0       | 0         |    |    |    |    |    |    |        |          |        |          |   |   |   |   |   |   |  |
| <b>Access</b> |              |    | W1      | W1          | W1       | W1          | W1      | W1     |    |    |    |    |    |    | W1      | W1        |    |    |    |    |    |    | W1     | W1       | W1     | W1       |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    | EM23ERR | PRSTIMEDERR | SCANPEND | SCANEXTPEND | PROGERR | VREFOV |    |    |    |    |    |    | SCANCMP | SINGLECMP |    |    |    |    |    |    | SCANUF | SINGLEUF | SCANOF | SINGLEOF |   |   |   |   |   |   |  |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 31:30 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 29    | EM23ERR         | 0   | W1     | <b>Set EM23ERR Interrupt Flag</b><br>Write 1 to set the EM23ERR interrupt flag         |
| 28    | PRSTIMEDERR     | 0   | W1     | <b>Set PRSTIMEDERR Interrupt Flag</b><br>Write 1 to set the PRSTIMEDERR interrupt flag |
| 27    | SCANPEND        | 0   | W1     | <b>Set SCANPEND Interrupt Flag</b><br>Write 1 to set the SCANPEND interrupt flag       |
| 26    | SCANEXTPEND     | 0   | W1     | <b>Set SCANEXTPEND Interrupt Flag</b><br>Write 1 to set the SCANEXTPEND interrupt flag |
| 25    | PROGERR         | 0   | W1     | <b>Set PROGERR Interrupt Flag</b><br>Write 1 to set the PROGERR interrupt flag         |
| 24    | VREFOV          | 0   | W1     | <b>Set VREFOV Interrupt Flag</b><br>Write 1 to set the VREFOV interrupt flag           |
| 23:18 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 17    | SCANCMP         | 0   | W1     | <b>Set SCANCMP Interrupt Flag</b><br>Write 1 to set the SCANCMP interrupt flag         |
| 16    | SINGLECMP       | 0   | W1     | <b>Set SINGLECMP Interrupt Flag</b><br>Write 1 to set the SINGLECMP interrupt flag     |
| 15:12 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 11    | SCANUF          | 0   | W1     | <b>Set SCANUF Interrupt Flag</b><br>Write 1 to set the SCANUF interrupt flag           |
| 10    | SINGLEUF        | 0   | W1     | <b>Set SINGLEUF Interrupt Flag</b><br>Write 1 to set the SINGLEUF interrupt flag       |
| 9     | SCANOF          | 0   | W1     | <b>Set SCANOF Interrupt Flag</b><br>Write 1 to set the SCANOF interrupt flag           |

| Bit | Name            | Reset   | Access | Description  |
|-----|-----------------|---|--------|--|
| 8   | SINGLEOF        | 0   | W1     | <b>Set SINGLEOF Interrupt Flag</b><br>Write 1 to set the SINGLEOF interrupt flag |
| 7:0 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |

## 27.5.16 ADCn\_IFC - Interrupt Flag Clear Register

| Offset        | Bit Position |    |         |             |          |             |         |        |    |    |    |    |    |    |         |           |    |    |    |    |    |    |        |          |        |          |   |   |   |   |   |   |  |
|---------------|--------------|----|---------|-------------|----------|-------------|---------|--------|----|----|----|----|----|----|---------|-----------|----|----|----|----|----|----|--------|----------|--------|----------|---|---|---|---|---|---|--|
| 0x040         | 31           | 30 | 29      | 28          | 27       | 26          | 25      | 24     | 23 | 22 | 21 | 20 | 19 | 18 | 17      | 16        | 15 | 14 | 13 | 12 | 11 | 10 | 9      | 8        | 7      | 6        | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    | 0       | 0           | 0        | 0           | 0       | 0      |    |    |    |    |    |    | 0       | 0         |    |    |    |    |    |    |        |          |        |          |   |   |   |   |   |   |  |
| <b>Access</b> |              |    | (R)W1   | (R)W1       | (R)W1    | (R)W1       | (R)W1   | (R)W1  |    |    |    |    |    |    | (R)W1   | (R)W1     |    |    |    |    |    |    | (R)W1  | (R)W1    | (R)W1  | (R)W1    |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    | EM23ERR | PRSTIMEDERR | SCANPEND | SCANEXTPEND | PROGERR | VREFOV |    |    |    |    |    |    | SCANCMP | SINGLECMP |    |    |    |    |    |    | SCANUF | SINGLEUF | SCANOF | SINGLEOF |   |   |   |   |   |   |  |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:30 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 29    | EM23ERR         | 0   | (R)W1  | <b>Clear EM23ERR Interrupt Flag</b><br>Write 1 to clear the EM23ERR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).         |
| 28    | PRSTIMEDERR     | 0   | (R)W1  | <b>Clear PRSTIMEDERR Interrupt Flag</b><br>Write 1 to clear the PRSTIMEDERR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 27    | SCANPEND        | 0   | (R)W1  | <b>Clear SCANPEND Interrupt Flag</b><br>Write 1 to clear the SCANPEND interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).       |
| 26    | SCANEXTPEND     | 0   | (R)W1  | <b>Clear SCANEXTPEND Interrupt Flag</b><br>Write 1 to clear the SCANEXTPEND interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 25    | PROGERR         | 0   | (R)W1  | <b>Clear PROGERR Interrupt Flag</b><br>Write 1 to clear the PROGERR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).         |
| 24    | VREFOV          | 0   | (R)W1  | <b>Clear VREFOV Interrupt Flag</b><br>Write 1 to clear the VREFOV interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).           |
| 23:18 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 17    | SCANCMP         | 0   | (R)W1  | <b>Clear SCANCMP Interrupt Flag</b><br>Write 1 to clear the SCANCMP interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).         |
| 16    | SINGLECMP       | 0   | (R)W1  | <b>Clear SINGLECMP Interrupt Flag</b><br>Write 1 to clear the SINGLECMP interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 15:12 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |

| Bit | Name            | Reset   | Access | Description   |
|-----|-----------------|---|--------|---|
| 11  | SCANUF          | 0   | (R)W1  | <b>Clear SCANUF Interrupt Flag</b><br><br>Write 1 to clear the SCANUF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 10  | SINGLEUF        | 0   | (R)W1  | <b>Clear SINGLEUF Interrupt Flag</b><br><br>Write 1 to clear the SINGLEUF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 9   | SCANOF          | 0   | (R)W1  | <b>Clear SCANOF Interrupt Flag</b><br><br>Write 1 to clear the SCANOF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |
| 8   | SINGLEOF        | 0   | (R)W1  | <b>Clear SINGLEOF Interrupt Flag</b><br><br>Write 1 to clear the SINGLEOF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 7:0 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |

## 27.5.17 ADCn\_IEN - Interrupt Enable Register

| Offset        | Bit Position |    |         |             |          |             |         |        |    |    |    |    |    |    |         |           |    |    |    |    |    |        |          |        |          |   |   |   |   |   |      |        |   |
|---------------|--------------|----|---------|-------------|----------|-------------|---------|--------|----|----|----|----|----|----|---------|-----------|----|----|----|----|----|--------|----------|--------|----------|---|---|---|---|---|------|--------|---|
| 0x044         | 31           | 30 | 29      | 28          | 27       | 26          | 25      | 24     | 23 | 22 | 21 | 20 | 19 | 18 | 17      | 16        | 15 | 14 | 13 | 12 | 11 | 10     | 9        | 8      | 7        | 6 | 5 | 4 | 3 | 2 | 1    | 0      |   |
| <b>Reset</b>  |              |    | 0       | 0           | 0        | 0           | 0       | 0      |    |    |    |    |    |    | 0       | 0         |    |    |    |    |    |        |          |        |          |   |   |   |   |   |      | 0      | 0 |
| <b>Access</b> |              |    | RW      | RW          | RW       | RW          | RW      | RW     |    |    |    |    |    |    | RW      | RW        |    |    |    |    |    | RW     | RW       | RW     | RW       |   |   |   |   |   | RW   | RW     |   |
| <b>Name</b>   |              |    | EM23ERR | PRSTIMEDERR | SCANPEND | SCANEXTPEND | PROGERR | VREFOV |    |    |    |    |    |    | SCANCMP | SINGLECMP |    |    |    |    |    | SCANUF | SINGLEUF | SCANOF | SINGLEOF |   |   |   |   |   | SCAN | SINGLE |   |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:30 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 29    | EM23ERR         | 0   | RW     | <b>EM23ERR Interrupt Enable</b><br>Enable/disable the EM23ERR interrupt         |
| 28    | PRSTIMEDERR     | 0   | RW     | <b>PRSTIMEDERR Interrupt Enable</b><br>Enable/disable the PRSTIMEDERR interrupt |
| 27    | SCANPEND        | 0   | RW     | <b>SCANPEND Interrupt Enable</b><br>Enable/disable the SCANPEND interrupt       |
| 26    | SCANEXTPEND     | 0   | RW     | <b>SCANEXTPEND Interrupt Enable</b><br>Enable/disable the SCANEXTPEND interrupt |
| 25    | PROGERR         | 0   | RW     | <b>PROGERR Interrupt Enable</b><br>Enable/disable the PROGERR interrupt         |
| 24    | VREFOV          | 0   | RW     | <b>VREFOV Interrupt Enable</b><br>Enable/disable the VREFOV interrupt           |
| 23:18 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 17    | SCANCMP         | 0   | RW     | <b>SCANCMP Interrupt Enable</b><br>Enable/disable the SCANCMP interrupt         |
| 16    | SINGLECMP       | 0   | RW     | <b>SINGLECMP Interrupt Enable</b><br>Enable/disable the SINGLECMP interrupt     |
| 15:12 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 11    | SCANUF          | 0   | RW     | <b>SCANUF Interrupt Enable</b><br>Enable/disable the SCANUF interrupt           |
| 10    | SINGLEUF        | 0   | RW     | <b>SINGLEUF Interrupt Enable</b><br>Enable/disable the SINGLEUF interrupt       |
| 9     | SCANOF          | 0   | RW     | <b>SCANOF Interrupt Enable</b><br>Enable/disable the SCANOF interrupt           |

| Bit | Name            | Reset   | Access | Description   |
|-----|-----------------|---|--------|---|
| 8   | SINGLEOF        | 0   | RW     | <b>SINGLEOF Interrupt Enable</b><br>Enable/disable the SINGLEOF interrupt |
| 7:2 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 1   | SCAN            | 0   | RW     | <b>SCAN Interrupt Enable</b><br>Enable/disable the SCAN interrupt         |
| 0   | SINGLE          | 0   | RW     | <b>SINGLE Interrupt Enable</b><br>Enable/disable the SINGLE interrupt     |

### 27.5.18 ADCn\_SINGLEDATA - Single Conversion Result Data (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x048         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DATA       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit  | Name | Reset      | Access | Description   |
|------|------|------------|--------|---|
| 31:0 | DATA | 0x00000000 | R      | <b>Single Conversion Result Data</b><br>This register holds the results from the last single channel mode conversion. Reading this field pops one entry from the SINGLE FIFO. |

### 27.5.19 ADCn\_SCANDATA - Scan Conversion Result Data (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x04C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DATA       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit  | Name | Reset      | Access | Description  |
|------|------|------------|--------|--|
| 31:0 | DATA | 0x00000000 | R      | <b>Scan Conversion Result Data</b><br>The register holds the results from the last scan mode conversion. Reading this field pops one entry from the SCAN FIFO. |

## 27.5.20 ADCn\_SINGLEDATAP - Single Conversion Result Data Peek Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x050         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DATAP      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name  | Reset      | Access | Description                               |
|---|-------|------------|--------|---|
| 31:0  | DATAP | 0x00000000 | R      | <b>Single Conversion Result Data Peek</b> |
| The register holds the results from the last single channel mode conversion. Reading this field will not pop an entry from the SINGLE FIFO. |       |            |        |   |

## 27.5.21 ADCn\_SCANDATAP - Scan Sequence Result Data Peek Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x054         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DATAP      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name  | Reset      | Access | Description                             |
|---|-------|------------|--------|---|
| 31:0  | DATAP | 0x00000000 | R      | <b>Scan Conversion Result Data Peek</b> |
| The register holds the results from the last scan mode conversion. Reading this field will not pop an entry from the SCAN FIFO. |       |            |        |   |

### 27.5.22 ADCn\_SCANDATAx - Scan Sequence Result Data + Data Source Register (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |             |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x068         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20          | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    | 0x00        |    |    |    |    | 0x0000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    | R           |    |    |    |    | R      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    | SCANINPUTID |    |    |    |    | DATA   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name        | Reset   | Access | Description   |
|-------|-------------|---|--------|---|
| 31:21 | Reserved    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 20:16 | SCANINPUTID | 0x00  | R      | <b>Scan Conversion Input ID</b><br>Indicates from which input the results in SCANDATA originated. Reading this field pops one entry from the SCAN FIFO. |
| 15:0  | DATA        | 0x0000  | R      | <b>Scan Conversion Result Data</b><br>Holds the results from the last scan conversion. Reading this field pops one entry from the SCAN FIFO.            |

### 27.5.23 ADCn\_SCANDATAxP - Scan Sequence Result Data + Data Source Peek Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |                 |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|-----------------|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x06C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20              | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    | 0x00            |    |    |    |    | 0x0000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    | R               |    |    |    |    | R      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    | SCANINPUTIDPEEK |    |    |    |    | DATAP  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:21 | Reserved        | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 20:16 | SCANINPUTIDPEEK | 0x00  | R      | <b>Scan Conversion Data Source Peek</b><br>Indicates from which input channel the results in SCANDATA originated. Reading this field does not pop any entry from the SCAN FIFO. |
| 15:0  | DATAP           | 0x0000  | R      | <b>Scan Conversion Result Data Peek</b><br>The register holds the results from the last scan conversion. Reading this field does not pop any entry from the SCAN FIFO.          |

## 27.5.24 ADCn\_APORTEQ - APORT Request Status Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |            |            |            |            |            |            |            |            |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x07C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9          | 8          | 7          | 6          | 5          | 4          | 3          | 2          | 1          | 0          |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R          | R          | R          | R          | R          | R          | R          | R          | R          | R          | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | APORT4YREQ | APORT4XREQ | APORT3YREQ | APORT3XREQ | APORT2YREQ | APORT2XREQ | APORT1YREQ | APORT1XREQ | APORT0YREQ | APORT0XREQ |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name       | Reset   | Access | Description  |
|-------|------------|---|--------|--|
| 31:10 | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 9     | APORT4YREQ | 0   | R      | <b>1 If the Bus Connected to APORT4Y is Requested</b><br>Reports if the bus connected to APORT4Y is being requested from the APORT |
| 8     | APORT4XREQ | 0   | R      | <b>1 If the Bus Connected to APORT4X is Requested</b><br>Reports if the bus connected to APORT4X is being requested from the APORT |
| 7     | APORT3YREQ | 0   | R      | <b>1 If the Bus Connected to APORT3Y is Requested</b><br>Reports if the bus connected to APORT3Y is being requested from the APORT |
| 6     | APORT3XREQ | 0   | R      | <b>1 If the Bus Connected to APORT3X is Requested</b><br>Reports if the bus connected to APORT3X is being requested from the APORT |
| 5     | APORT2YREQ | 0   | R      | <b>1 If the Bus Connected to APORT2Y is Requested</b><br>Reports if the bus connected to APORT2Y is being requested from the APORT |
| 4     | APORT2XREQ | 0   | R      | <b>1 If the Bus Connected to APORT2X is Requested</b><br>Reports if the bus connected to APORT2X is being requested from the APORT |
| 3     | APORT1YREQ | 0   | R      | <b>1 If the Bus Connected to APORT1Y is Requested</b><br>Reports if the bus connected to APORT1Y is being requested from the APORT |
| 2     | APORT1XREQ | 0   | R      | <b>1 If the Bus Connected to APORT1X is Requested</b><br>Reports if the bus connected to APORT1X is being requested from the APORT |
| 1     | APORT0YREQ | 0   | R      | <b>1 If the Bus Connected to APORT0Y is Requested</b><br>Reports if the bus connected to APORT0Y is being requested from the APORT |
| 0     | APORT0XREQ | 0   | R      | <b>1 If the Bus Connected to APORT0X is Requested</b><br>Reports if the bus connected to APORT0X is being requested from the APORT |

## 27.5.25 ADCn\_APORTCONFLICT - APORT Conflict Status Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                 |                 |                 |                 |                 |                 |                 |                 |                 |                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x080         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9               | 8               | 7               | 6               | 5               | 4               | 3               | 2               | 1               | 0               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R               | R               | R               | R               | R               | R               | R               | R               | R               | R               | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | APORT4YCONFLICT | APORT4XCONFLICT | APORT3YCONFLICT | APORT3XCONFLICT | APORT2YCONFLICT | APORT2XCONFLICT | APORT1YCONFLICT | APORT1XCONFLICT | APORT0YCONFLICT | APORT0XCONFLICT |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name            | Reset  | Access | Description  |
|-------|-----------------|--|--------|--|
| 31:10 | Reserved        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 9     | APORT4YCONFLICT | 0  | R      | <p><b>1 If the Bus Connected to APORT4Y is in Conflict With Another Peripheral</b></p> <p>Reports if the bus connected to APORT4Y is is also being requested by another peripheral</p> |
| 8     | APORT4XCONFLICT | 0  | R      | <p><b>1 If the Bus Connected to APORT4X is in Conflict With Another Peripheral</b></p> <p>Reports if the bus connected to APORT4X is is also being requested by another peripheral</p> |
| 7     | APORT3YCONFLICT | 0  | R      | <p><b>1 If the Bus Connected to APORT3Y is in Conflict With Another Peripheral</b></p> <p>Reports if the bus connected to APORT3Y is is also being requested by another peripheral</p> |
| 6     | APORT3XCONFLICT | 0  | R      | <p><b>1 If the Bus Connected to APORT3X is in Conflict With Another Peripheral</b></p> <p>Reports if the bus connected to APORT3X is is also being requested by another peripheral</p> |
| 5     | APORT2YCONFLICT | 0  | R      | <p><b>1 If the Bus Connected to APORT2Y is in Conflict With Another Peripheral</b></p> <p>Reports if the bus connected to APORT2Y is is also being requested by another peripheral</p> |
| 4     | APORT2XCONFLICT | 0  | R      | <p><b>1 If the Bus Connected to APORT2X is in Conflict With Another Peripheral</b></p> <p>Reports if the bus connected to APORT2X is is also being requested by another peripheral</p> |
| 3     | APORT1YCONFLICT | 0  | R      | <p><b>1 If the Bus Connected to APORT1Y is in Conflict With Another Peripheral</b></p> <p>Reports if the bus connected to APORT1Y is is also being requested by another peripheral</p> |
| 2     | APORT1XCONFLICT | 0  | R      | <p><b>1 If the Bus Connected to APORT1X is in Conflict With Another Peripheral</b></p> <p>Reports if the bus connected to APORT1X is is also being requested by another peripheral</p> |
| 1     | APORT0YCONFLICT | 0  | R      | <p><b>1 If the Bus Connected to APORT0Y is in Conflict With Another Peripheral</b></p> <p>Reports if the bus connected to APORT0Y is is also being requested by another peripheral</p> |

| Bit | Name            | Reset | Access | Description  |
|-----|-----------------|-------|--------|--|
| 0   | APORT0XCONFLICT | 0     | R      | <b>1 If the Bus Connected to APORT0X is in Conflict With Another Peripheral</b><br><br>Reports if the bus connected to APORT0X is also being requested by another peripheral |

### 27.5.26 ADCn\_SINGLEFIFOCOUNT - Single FIFO Count Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x084         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | SINGLEDc     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 31:3 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 2:0  | SINGLEDc        | 0x0   | R      | <b>Single Data Count</b><br><br>Number of unread data available in Single FIFO. |

### 27.5.27 ADCn\_SCANFIFOCOUNT - Scan FIFO Count Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x088         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | SCANDC       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 31:3 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 2:0  | SCANDC          | 0x0   | R      | <b>Scan Data Count</b><br><br>Number of unread data available in Scan FIFO. |

27.5.28 ADCn\_SINGLEFIFOCLEAR - Single FIFO Clear Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |                 |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-----------------|
| 0x08C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0               |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0               |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | W1              |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | SINGLEFIFOCLEAR |

| Bit  | Name            | Reset  | Access | Description   |
|------|-----------------|--|--------|---|
| 31:1 | Reserved        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 0    | SINGLEFIFOCLEAR | 0  | W1     | <b>Clear Single FIFO Content</b><br>Write a 1 to clear Single FIFO content. |

27.5.29 ADCn\_SCANFIFOCLEAR - Scan FIFO Clear Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |               |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---------------|
| 0x090         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0             |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0             |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | W1            |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | SCANFIFOCLEAR |

| Bit  | Name          | Reset  | Access | Description   |
|------|---------------|--|--------|---|
| 31:1 | Reserved      | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 0    | SCANFIFOCLEAR | 0  | W1     | <b>Clear Scan FIFO Content</b><br>Write a 1 to clear Scan FIFO content. |

### 27.5.30 ADCn\_APORMASTERDIS - APORT Bus Master Disable Register

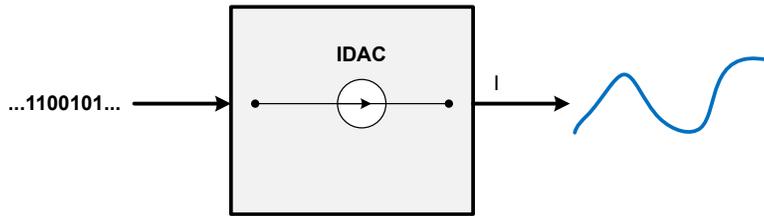
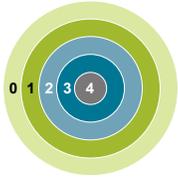
| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                  |                  |                  |                  |                  |                  |                  |                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0x094         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9                | 8                | 7                | 6                | 5                | 4                | 3                | 2                | 1  | 0  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0                | 0                | 0                | 0                | 0                | 0                | 0                | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW               | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | APORT4YMASTERDIS | APORT4XMASTERDIS | APORT3YMASTERDIS | APORT3XMASTERDIS | APORT2YMASTERDIS | APORT2XMASTERDIS | APORT1YMASTERDIS | APORT1XMASTERDIS |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

| Bit   | Name                     | Reset   | Access | Description   |       |             |   |                         |   |                          |
|-------|--------------------------|---|--------|---|-------|-------------|---|-------------------------|---|--------------------------|
| 31:10 | Reserved                 | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |             |   |                         |   |                          |
| 9     | APORT4YMASTERDIS         | 0   | RW     | <b>APORT4Y Master Disable</b><br><br>Determines if the ADC will request this APORT bus (if selected by POSSEL or NEGSEL or SCANINPUTSEL). When 1, ADC only passively monitors the APORT bus and the selection of the channel for the selected bus is ignored. The channel selection is done by the device that masters the APORT bus. This bit allows multiple APORT connected devices to monitor the same APORT bus simultaneously.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>APORT mastering enabled</td> </tr> <tr> <td>1</td> <td>APORT mastering disabled</td> </tr> </tbody> </table> | Value | Description | 0 | APORT mastering enabled | 1 | APORT mastering disabled |
| Value | Description              |   |        |   |       |             |   |                         |   |                          |
| 0     | APORT mastering enabled  |   |        |   |       |             |   |                         |   |                          |
| 1     | APORT mastering disabled |   |        |   |       |             |   |                         |   |                          |
| 8     | APORT4XMASTERDIS         | 0   | RW     | <b>APORT4X Master Disable</b><br><br>Determines if the ADC will request this APORT bus (if selected by POSSEL or NEGSEL or SCANINPUTSEL). When 1, ADC only passively monitors the APORT bus and the selection of the channel for the selected bus is ignored. The channel selection is done by the device that masters the APORT bus. This bit allows multiple APORT connected devices to monitor the same APORT bus simultaneously.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>APORT mastering enabled</td> </tr> <tr> <td>1</td> <td>APORT mastering disabled</td> </tr> </tbody> </table> | Value | Description | 0 | APORT mastering enabled | 1 | APORT mastering disabled |
| Value | Description              |   |        |   |       |             |   |                         |   |                          |
| 0     | APORT mastering enabled  |   |        |   |       |             |   |                         |   |                          |
| 1     | APORT mastering disabled |   |        |   |       |             |   |                         |   |                          |
| 7     | APORT3YMASTERDIS         | 0   | RW     | <b>APORT3Y Master Disable</b><br><br>Determines if the ADC will request this APORT bus (if selected by POSSEL or NEGSEL or SCANINPUTSEL). When 1, ADC only passively monitors the APORT bus and the selection of the channel for the selected bus is ignored. The channel selection is done by the device that masters the APORT bus. This bit allows multiple APORT connected devices to monitor the same APORT bus simultaneously.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>APORT mastering enabled</td> </tr> <tr> <td>1</td> <td>APORT mastering disabled</td> </tr> </tbody> </table> | Value | Description | 0 | APORT mastering enabled | 1 | APORT mastering disabled |
| Value | Description              |   |        |   |       |             |   |                         |   |                          |
| 0     | APORT mastering enabled  |   |        |   |       |             |   |                         |   |                          |
| 1     | APORT mastering disabled |   |        |   |       |             |   |                         |   |                          |

| Bit   | Name              | Reset                    | Access | Description  |
|-------|-------------------|--------------------------|--------|--|
| 6     | APORT3XMASTER-DIS | 0                        | RW     | <b>APORT3X Master Disable</b><br><br>Determines if the ADC will request this APORT bus (if selected by POSSEL or NEGSEL or SCANINPUTSEL). When 1, ADC only passively monitors the APORT bus and the selection of the channel for the selected bus is ignored. The channel selection is done by the device that masters the APORT bus. This bit allows multiple APORT connected devices to monitor the same APORT bus simultaneously. |
| Value |                   | Description              |        |  |
| 0     |                   | APORT mastering enabled  |        |  |
| 1     |                   | APORT mastering disabled |        |  |
| 5     | APORT2YMASTER-DIS | 0                        | RW     | <b>APORT2Y Master Disable</b><br><br>Determines if the ADC will request this APORT bus (if selected by POSSEL or NEGSEL or SCANINPUTSEL). When 1, ADC only passively monitors the APORT bus and the selection of the channel for the selected bus is ignored. The channel selection is done by the device that masters the APORT bus. This bit allows multiple APORT connected devices to monitor the same APORT bus simultaneously. |
| Value |                   | Description              |        |  |
| 0     |                   | APORT mastering enabled  |        |  |
| 1     |                   | APORT mastering disabled |        |  |
| 4     | APORT2XMASTER-DIS | 0                        | RW     | <b>APORT2X Master Disable</b><br><br>Determines if the ADC will request this APORT bus (if selected by POSSEL or NEGSEL or SCANINPUTSEL). When 1, ADC only passively monitors the APORT bus and the selection of the channel for the selected bus is ignored. The channel selection is done by the device that masters the APORT bus. This bit allows multiple APORT connected devices to monitor the same APORT bus simultaneously. |
| Value |                   | Description              |        |  |
| 0     |                   | APORT mastering enabled  |        |  |
| 1     |                   | APORT mastering disabled |        |  |
| 3     | APORT1YMASTER-DIS | 0                        | RW     | <b>APORT1Y Master Disable</b><br><br>Determines if the ADC will request this APORT bus (if selected by POSSEL or NEGSEL or SCANINPUTSEL). When 1, ADC only passively monitors the APORT bus and the selection of the channel for the selected bus is ignored. The channel selection is done by the device that masters the APORT bus. This bit allows multiple APORT connected devices to monitor the same APORT bus simultaneously. |
| Value |                   | Description              |        |  |
| 0     |                   | APORT mastering enabled  |        |  |
| 1     |                   | APORT mastering disabled |        |  |
| 2     | APORT1XMASTER-DIS | 0                        | RW     | <b>APORT1X Master Disable</b><br><br>Determines if the ADC will request this APORT bus (if selected by POSSEL or NEGSEL or SCANINPUTSEL). When 1, ADC only passively monitors the APORT bus and the selection of the channel for the selected bus is ignored. The channel selection is done by the device that masters the APORT bus. This bit allows multiple APORT connected devices to monitor the same APORT bus simultaneously. |
| Value |                   | Description              |        |  |

| Bit | Name            | Reset   | Access | Description              |
|-----|-----------------|---|--------|--------------------------|
|     | 0               |   |        | APORT mastering enabled  |
|     | 1               |   |        | APORT mastering disabled |
| 1:0 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |                          |

## 28. IDAC - Current Digital to Analog Converter



### Quick Facts

#### What?

The IDAC can sink or source a configurable constant current.

#### Why?

The IDAC can be used to bias external circuits or (in conjunction with the ADC) measure capacitance by injecting a controlled current into a component.

#### How?

In addition to providing a constant current, the IDAC can be switched on and off with a PRS signal all the way down to EM3.

### 28.1 Introduction

The current digital to analog converter (IDAC) can source or sink a configurable constant current from APORT and/or main pad (OUT-PAD). The current is configurable with several ranges of various step sizes.

### 28.2 Features

- Can source and sink current
- Programmable constant output current
  - Selectable current range between 0.05  $\mu\text{A}$  and 64  $\mu\text{A}$
  - Each range is linearly programmable in 32 steps
  - Support for current calibration
- Support for manual and PRS triggered output enable
- Available in EM0-EM3

### 28.3 Functional Description

An overview of the IDAC module is shown in [Figure 28.1 IDAC Overview on page 959](#). The IDAC is designed to source or sink a programmable current which can be controlled by setting the range and the step in the RANGESEL and STEPSEL bitfields in IDAC\_CURRPROG register. The IDAC output enable can be controlled by software or PRS. The IDAC is enabled by setting EN in IDAC\_CTRL.

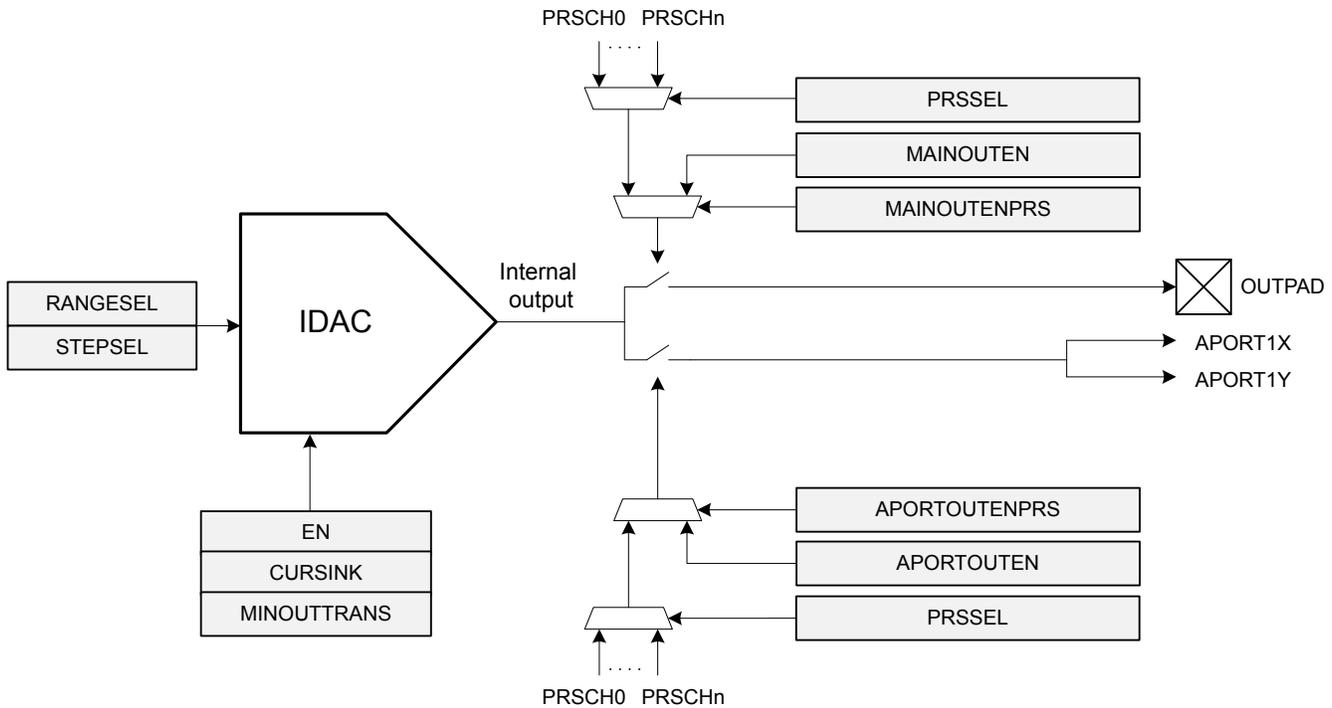


Figure 28.1. IDAC Overview

#### 28.3.1 Current Programming

The four different current ranges can be selected by configuring the RANGESEL bitfield in IDAC\_CURRPROG. The current output in each range is linearly programmable in 32 steps, and is controlled by the STEPSEL bitfield in IDAC\_CURRPROG. These current ranges and their step sizes are shown in [Table 28.1 Range Selection on page 959](#).

Table 28.1. Range Selection

| Range Select | Range Value [ $\mu$ A] | Step Size [nA] | Step Counts |
|--------------|------------------------|----------------|-------------|
| 0            | 0.05 - 1.6             | 50             | 32          |
| 1            | 1.6 - 4.7              | 100            | 32          |
| 2            | 0.5 - 16               | 500            | 32          |
| 3            | 2 - 64                 | 2000           | 32          |

#### 28.3.2 IDAC Enable and Warm-up

The IDAC is enabled by setting the EN bit in IDAC\_CTRL. When this bit is set, the IDAC must stabilize before its output current is stable.

It is important to wait until the IDAC is warmed up, or until any current programming is complete and the output current is stabilized, before entering EM1, EM2, or EM3.

### 28.3.3 Output Control

The IDAC output enable is controlled separately for APORT and main pad. If APORTOUTENPRS/MAINOUTENPRS is set, output enable is controlled by PRS, else it is controlled by software via APORTOUTEN/MAINOUTEN.

### 28.3.4 APORT Configuration

The IDAC APORT outputs can be routed to pins through the APORT system. Note that the IDAC has only two local APORT interfaces APORT1X and APORT1Y, which are connected to the APORT BUSCX and BUSCY, respectively. The pins are selected by requesting an APORT channel in APORTOUTSEL in IDAC\_CTRL. For mapping between APORT channel and physical pin, please refer to data sheet. The IDAC can be in either master or slave mode when connecting to the APORT. By default the IDAC is in master mode. To enable slave mode, set APORTMASTERDIS in IDAC\_CTRL. As IDAC is only capable of driving an APORT channel, only master mode is meaningful for IDAC. If the IDAC is in master mode, and another module is currently driving the requested channel, the APORTCONFLICT bitfield in IDAC\_STATUS will be set together with APORT1XCONFLICT or APORT1YCONFLICT in IDAC\_APORTCONFLICT. The APORTCONFLICT can also be configured to trigger an interrupt, see [28.3.5 Interrupts](#) for details.

### 28.3.5 Interrupts

The APORTCONFLICT interrupt flag in the IDAC\_IF register indicates that a conflict has occurred when requesting a channel from the APORT. The APORTCONFLICT interrupt can be enabled by setting the APORTCONFLICT bit in IDAC\_IEN, or cleared by setting the APORTCONFLICT bit in IDAC\_IFC.

### 28.3.6 Minimizing Output Transition

If the internal output of the IDAC differs from the voltage at the output pin, enabling the output can cause an unwanted transition. To minimize this transition, it is possible to charge or discharge the internal output node before enabling the output to the pin. Setting MINOUTTRANS in IDAC\_CTRL when the IDAC is sourcing current connects the internal node to GND. Alternatively, setting MINOUTTRANS when the IDAC is sinking current connects the internal output node to VDD. Setting APORTOUTEN/MAINOUTEN when MINOUTTRANS is set will halt the charge/discharge until either APORTOUTEN/MAINOUTEN is cleared or MINOUTTRANS is cleared.

### 28.3.7 Duty Cycle Configuration

The references for the IDAC can be duty-cycled, meaning that it can source current at very low overhead current consumption at the cost of response time and accuracy. By default duty-cycling is enabled in EM2 and EM3 and disabled in EM0 and EM1. Setting EM2DUTYCYCLEDIS in IDAC\_DUTYCONFIG will disable duty cycling in EM2 and EM3. Note that sinking current can not be done with duty-cycled references so measures needs to be taken to always disable duty-cycling while sinking current.

### 28.3.8 Calibration

The IDAC can be calibrated to accurately compensate for process, supply voltage and temperature variations. During the production test, the middle step of each range is calibrated at room temperature. The TUNING bitfield in the IDAC\_CAL register can be used to do further calibration of each step with an external resistor connected to IDAC\_OUT. The calibrated tuning value for each band can be read from the Device Information (DI) page.

### 28.3.9 PRS Triggered Charge Injection

The amount of charge sourced or sunk by the IDAC can be controlled by the PRS (e.g., using a timer as producer) via the output switch. [Figure 28.2 IDAC Charge Injection Example on page 961](#) shows a case where the IDAC is configured to periodically supply charge using the PRS. The amount of charge injected is proportional to the the period the IDAC is on. The total charge injected is the current multiplied by the time the output switch is enabled.

The PRS system is enabled by setting APORTOUTENPRS/MAINOUTENPRS in IDAC\_CTRL, and the PRS channel is selected by PRSSEL in IDAC\_CTRL. To generate the periodic control signal, the TIMER module can be used, by configuring for example a CC channel to compare match with a configurable level.

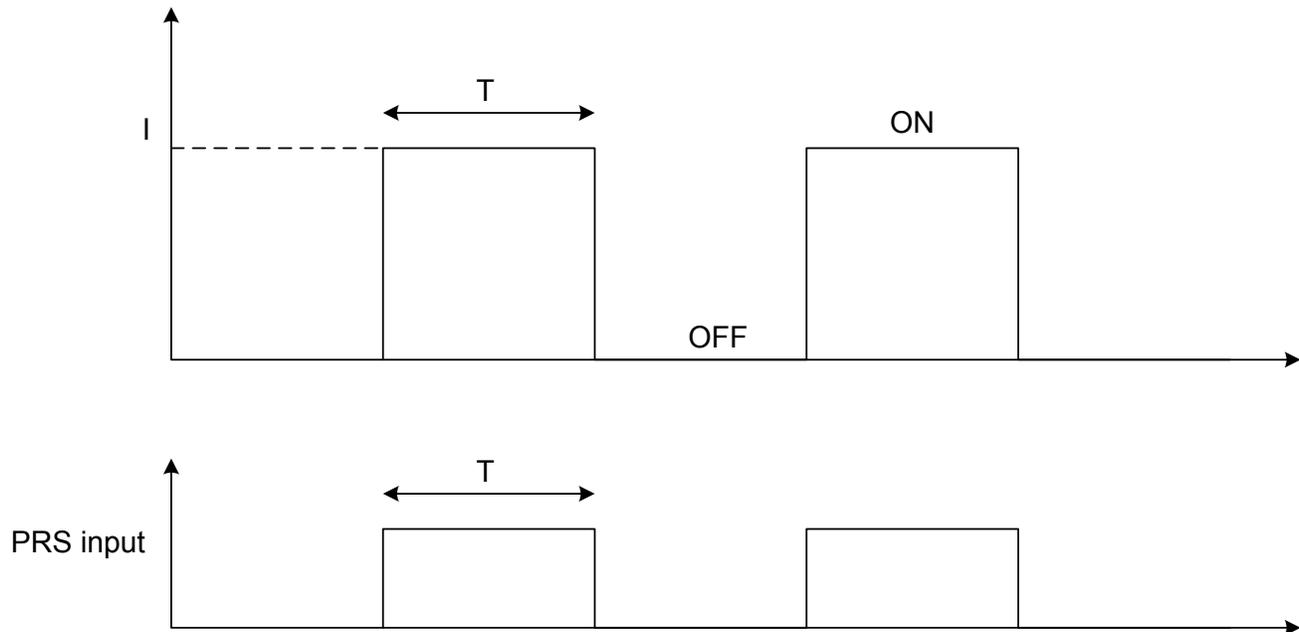


Figure 28.2. IDAC Charge Injection Example

### 28.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name               | Type  | Description                       |
|--------|--------------------|-------|-----------------------------------|
| 0x000  | IDAC_CTRL          | RW    | Control Register                  |
| 0x004  | IDAC_CURPROG       | RW    | Current Programming Register      |
| 0x00C  | IDAC_DUTYCONFIG    | RW    | Duty Cycle Configuration Register |
| 0x018  | IDAC_STATUS        | R     | Status Register                   |
| 0x020  | IDAC_IF            | R     | Interrupt Flag Register           |
| 0x024  | IDAC_IFS           | W1    | Interrupt Flag Set Register       |
| 0x028  | IDAC_IFC           | (R)W1 | Interrupt Flag Clear Register     |
| 0x02C  | IDAC_IEN           | RW    | Interrupt Enable Register         |
| 0x034  | IDAC_APORTREQ      | R     | APORT Request Status Register     |
| 0x038  | IDAC_APORTCONFLICT | R     | APORT Request Status Register     |

## 28.5 Register Description

### 28.5.1 IDAC\_CTRL - Control Register

| Offset        | Bit Position |    |    |    |    |    |    |    |       |    |    |    |              |    |           |    |               |    |                |    |          |    |        |   |             |   |            |   |             |   |         |   |    |  |
|---------------|--------------|----|----|----|----|----|----|----|-------|----|----|----|--------------|----|-----------|----|---------------|----|----------------|----|----------|----|--------|---|-------------|---|------------|---|-------------|---|---------|---|----|--|
| 0x000         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23    | 22 | 21 | 20 | 19           | 18 | 17        | 16 | 15            | 14 | 13             | 12 | 11       | 10 | 9      | 8 | 7           | 6 | 5          | 4 | 3           | 2 | 1       | 0 |    |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    | 0x0   |    |    |    | 0            |    | 0         |    | 0             |    | 0              |    | 0        |    | 0x00   |   | 0           |   | 0          |   | 0           |   | 0       |   |    |  |
| <b>Access</b> |              |    |    |    |    |    |    |    | RW    |    |    |    | RW           |    | RW        |    | RW            |    | RW             |    | RW       |    | RW     |   | RW          |   | RW         |   | RW          |   | RW      |   |    |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    | PRSEL |    |    |    | MAINOUTENPRS |    | MAINOUTEN |    | APORTOUTENPRS |    | APORTMASTERDIS |    | EM2DELAY |    | PWRSEL |   | APORTOUTSEL |   | APORTOUTEN |   | MINOUTTRANS |   | CURSINK |   | EN |  |

| Bit   | Name         | Reset  | Access | Description  |
|-------|--------------|--|--------|--|
| 31:24 | Reserved     | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 23:20 | PRSEL        | 0x0  | RW     | <b>IDAC Output Enable PRS Channel Select</b><br>Selects which PRS channel to use to enable output. |
|       | Value        | Mode   |        | Description  |
|       | 0            | PRSCH0   |        | PRS Channel 0 selected.  |
|       | 1            | PRSCH1   |        | PRS Channel 1 selected.  |
|       | 2            | PRSCH2   |        | PRS Channel 2 selected.  |
|       | 3            | PRSCH3   |        | PRS Channel 3 selected.  |
|       | 4            | PRSCH4   |        | PRS Channel 4 selected.  |
|       | 5            | PRSCH5   |        | PRS Channel 5 selected.  |
|       | 6            | PRSCH6   |        | PRS Channel 6 selected.  |
|       | 7            | PRSCH7   |        | PRS Channel 7 selected.  |
|       | 8            | PRSCH8   |        | PRS Channel 8 selected.  |
|       | 9            | PRSCH9   |        | PRS Channel 9 selected.  |
|       | 10           | PRSCH10  |        | PRS Channel 10 selected.   |
|       | 11           | PRSCH11  |        | PRS Channel 11 selected.   |
| 19    | MAINOUTENPRS | 0  | RW     | <b>PRS Controlled Main Pad Output Enable</b><br>Enable PRS Control of IDAC Main Pad output enable. |
|       | Value        |  |        | Description  |
|       | 0            |  |        | Main pad output enable controlled by IDAC_MAINOUTEN.   |
|       | 1            |  |        | Main pad output enable controlled by PRS input selected by PRSEL.                                  |
| 18    | MAINOUTEN    | 0  | RW     | <b>Output Enable</b><br>Set to enable IDAC main output to pad if MAINOUTENPRS is not set.          |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 17   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 16   | APORTOUTENPRS   | 0   | RW     | <b>PRS Controlled APORT Output Enable</b><br>Enable PRS Control of the IDAC APORT output enable.  |
|      | Value           |   |        | Description   |
|      | 0               |   |        | APORT output enable controlled by IDAC_APORTOUTEN.  |
|      | 1               |   |        | APORT output enable controlled by PRS channel selected by PRSSEL.   |
| 15   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 14   | APORTMASTERDIS  | 0   | RW     | <b>APORT Bus Master Disable</b><br>Determines if the IDAC will request the APORT bus selected by APORTOUTSEL. This bit allows multiple APORT connected devices to monitor the same APORT bus simultaneously by allowing the IDAC to not master the selected bus. When 1, the determination is expected to be from another peripheral, and the IDAC only passively looks at the bus. When 0, the selection of channel for a selected bus is ignored (the bus is not), and will be whatever selection the external device mastering the bus has configured for the APORT bus. |
|      | Value           |   |        | Description   |
|      | 0               |   |        | Bus mastering enabled   |
|      | 1               |   |        | Bus mastering disabled  |
| 13   | EM2DELAY        | 0   | RW     | <b>EM2 Delay</b><br>Delays EM2 entry until the IDAC output is stable  |
| 12   | PWRSEL          | 0   | RW     | <b>Power Select</b><br>Selects the power source for the IDAC  |
|      | Mode            | Value   |        | Description   |
|      | ANA             | 0   |        | VDDX_ANA  |
|      | IO              | 1   |        | IOVDD   |
| 11:4 | APORTOUTSEL     | 0x00  | RW     | <b>APORT Output Select</b><br>Select output mode.   |
|      | APORT1XCH0      | 0x20  |        | APORT1X Channel 0   |
|      | APORT1YCH1      | 0x21  |        | APORT1Y Channel 1   |
|      | APORT1XCH2      | 0x22  |        | APORT1X Channel 2   |
|      | APORT1YCH3      | 0x23  |        | APORT1Y Channel 3   |
|      | APORT1XCH4      | 0x24  |        | APORT1X Channel 4   |
|      | APORT1YCH5      | 0x25  |        | APORT1Y Channel 5   |
|      | ...             | ...   |        | ...   |
|      | APORT1XCH30     | 0x3e  |        | APORT1X Channel 30  |
|      | APORT1YCH31     | 0x3f  |        | APORT1Y Channel 31  |

| Bit | Name        | Reset | Access | Description   |
|-----|-------------|-------|--------|---|
| 3   | APORTOUTEN  | 0     | RW     | <b>APORT Output Enable</b><br>Set to enable the IDAC output to APORT if APORTOUTENPRS is not set.             |
| 2   | MINOUTTRANS | 0     | RW     | <b>Minimum Output Transition Enable</b><br>Set to enable minimum output transition mode for the IDAC.         |
| 1   | CURSINK     | 0     | RW     | <b>Current Sink Enable</b><br>Set to enable the IDAC as a current sink. By default, the IDAC sources current. |
| 0   | EN          | 0     | RW     | <b>Current DAC Enable</b><br>Set to enable the IDAC.  |

### 28.5.2 IDAC\_CURPROG - Current Programming Register

| Offset        | Bit Position |    |    |    |    |    |    |    |        |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |         |   |   |   |   |   |   |   |          |
|---------------|--------------|----|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---------|---|---|---|---|---|---|---|----------|
| 0x004         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |          |
| <b>Reset</b>  |              |    |    |    |    |    |    |    | 0x9B   |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x00    |   |   |   |   |   |   |   | 0x0      |
| <b>Access</b> |              |    |    |    |    |    |    |    | RW     |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RW      |   |   |   |   |   |   |   | RW       |
| <b>Name</b>   |              |    |    |    |    |    |    |    | TUNING |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | STEPSEL |   |   |   |   |   |   |   | RANGESEL |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 31:24 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 23:16 | TUNING          | 0x9B  | RW     | <b>Tune the Current to Given Accuracy</b><br>In production test. the middle step (16) of each range is calibrated and can be read from the Device Information (DI) page.   |
| 15:13 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 12:8  | STEPSEL         | 0x00  | RW     | <b>Current Step Size Select</b><br>Select the step within each range. The size of each step depends on the RANGESEL setting. RANGESEL settings of 0, 1, 2, and 3 correspond to step sizes of 50 nA, 100 nA, 500 nA, and 2000 nA, respectively. See step details. |
| 7:2   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 1:0   | RANGESEL        | 0x0   | RW     | <b>Current Range Select</b><br>Selects current range of the output.  |

| Value | Mode   | Description                        |
|-------|--------|------------------------------------|
| 0     | RANGE0 | Current range set to 0 - 1.6 uA.   |
| 1     | RANGE1 | Current range set to 1.6 - 4.7 uA. |
| 2     | RANGE2 | Current range set to 0.5 - 16 uA.  |
| 3     | RANGE3 | Current range set to 2 - 64 uA.    |

## 28.5.3 IDAC\_DUTYCONFIG - Duty Cycle Configuration Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |                 |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-----------------|--|
| 0x00C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0               |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0               |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | RW              |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | EM2DUTYCYCLEDIS |  |

| Bit  | Name             | Reset  | Access | Description   |
|------|------------------|--|--------|---|
| 31:2 | Reserved         | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 1    | EM2DUTYCYCLE-DIS | 0  | RW     | <b>Duty Cycle Enable</b><br><br>Set to disable duty cycling in EM2. |
| 0    | Reserved         | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |

## 28.5.4 IDAC\_STATUS - Status Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |               |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---------------|--|
| 0x018         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0             |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0             |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | R             |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | APORTCONFLICT |  |

| Bit  | Name          | Reset  | Access | Description  |
|------|---------------|--|--------|--|
| 31:2 | Reserved      | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 1    | APORTCONFLICT | 0  | R      | <b>APORT Conflict Output</b><br><br>1 if any of the APORT BUSes being requested by the IDAC are also being requested by another peripheral |
| 0    | Reserved      | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |

### 28.5.5 IDAC\_IF - Interrupt Flag Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x020         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | APORTCONFLICT |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name          | Reset   | Access | Description  |
|------|---------------|---|--------|--|
| 31:2 | Reserved      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 1    | APORTCONFLICT | 0   | R      | <b>APORT Conflict Interrupt Flag</b><br>1 if any of the APORT BUSes being requested by the IDAC are also being requested by another peripheral |
| 0    | Reserved      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |

### 28.5.6 IDAC\_IFS - Interrupt Flag Set Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x024         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | APORTCONFLICT |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name          | Reset   | Access | Description  |
|------|---------------|---|--------|--|
| 31:2 | Reserved      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 1    | APORTCONFLICT | 0   | W1     | <b>Set APORTCONFLICT Interrupt Flag</b><br>Write 1 to set the APORTCONFLICT interrupt flag |
| 0    | Reserved      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |

## 28.5.7 IDAC\_IFC - Interrupt Flag Clear Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |               |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---------------|---|
| 0x028         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1             | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | 0             |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | (R)W1         |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | APORTCONFLICT |   |

| Bit  | Name          | Reset   | Access | Description   |
|------|---------------|---|--------|---|
| 31:2 | Reserved      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 1    | APORTCONFLICT | 0   | (R)W1  | <b>Clear APORTCONFLICT Interrupt Flag</b><br><br>Write 1 to clear the APORTCONFLICT interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 0    | Reserved      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |

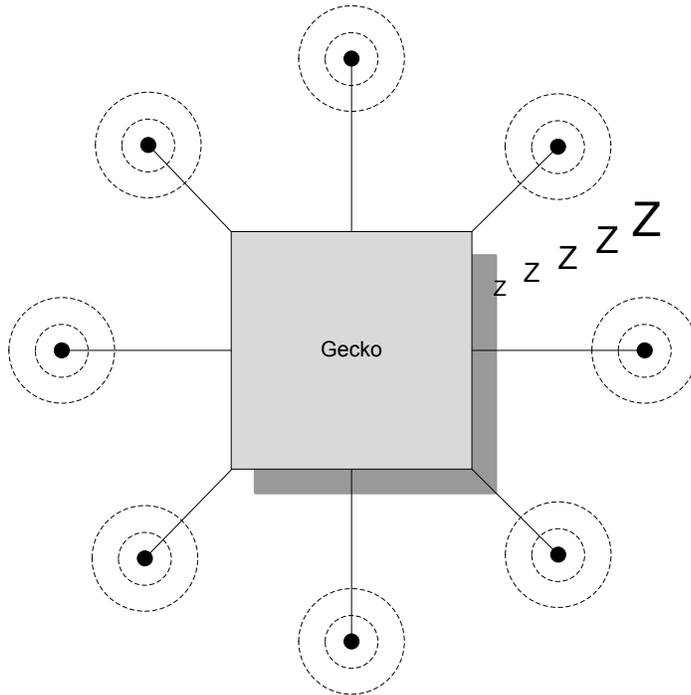
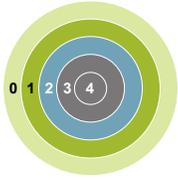
## 28.5.8 IDAC\_IEN - Interrupt Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |               |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---------------|---|
| 0x02C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1             | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | 0             |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | RW            |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | APORTCONFLICT |   |

| Bit  | Name          | Reset   | Access | Description   |
|------|---------------|---|--------|---|
| 31:2 | Reserved      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 1    | APORTCONFLICT | 0   | RW     | <b>APORTCONFLICT Interrupt Enable</b><br><br>Enable/disable the APORTCONFLICT interrupt |
| 0    | Reserved      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |



## 29. LESENSE - Low Energy Sensor Interface



### Quick Facts

#### What?

LESENSE is a low energy sensor interface capable of autonomously collecting and processing data from multiple sensors even when in EM2. Flexible configuration makes LESENSE a versatile sensor interface compatible with a wide range of sensors and measurement schemes.

#### Why?

Capability to autonomously monitor sensors allows the EFR32xG13 Wireless Gecko to reside in a low energy mode for long periods of time while keeping track of sensor status and sensor events.

#### How?

LESENSE is highly configurable and is capable of collecting data from a wide range of sensor types. Once the data is collected, the programmable state machine, LESENSE decoder, is capable of processing sensor data without CPU intervention. A large result buffer allows the chip to remain in EM2 for long periods of time while autonomously collecting data.

### 29.1 Introduction

LESENSE is a low energy sensor interface utilizing on-chip peripherals to perform measurement of a configurable set of sensors. The sensor measurements results can be processed by the LESENSE decoder, a configurable state machine with up to 32 states. The results can also be stored in a result buffer to be collected by the CPU or DMA for further processing.

LESENSE operates from EM0 down to EM2, and can wake up the CPU on configurable events.

## 29.2 Features

- Up to 16 sensors
- Autonomous sensor monitoring in EM0, EM1, and EM2
- Highly configurable decoding of sensor results
- Interrupt on sensor events
- Configurable enable signals to external sensors
- Circular buffer for storage of up to 16 sensor results
- Multiple evaluation modes minimize the need for software interaction
- Supports ADC0 sampling and evaluation
- Support for multiple sensor types
  - LC sensors
  - Capacitive sensing
  - General analog sensors

## 29.3 Functional Description

The LESENSE module is capable of controlling on-chip peripherals in order to perform monitoring of different sensors with little or no CPU intervention. LESENSE uses the analog comparators (ACMP) or ADC0 for measurement of sensor signals. LESENSE can also control the VDAC to generate accurate reference voltages. [Figure 29.1 LESENSE Block Diagram on page 970](#) shows an overview of the LESENSE module.

The LESENSE module consists of a sequencer, an evaluation block, a decoder, and a RAM block:

- The sequencer handles interaction with other peripherals and controls timing of sensor measurements. It also includes a counter that can be used to count pulses on the ACMP output.
- The evaluation block is used to process the data collected by the sequencer.
- To autonomously analyze sensor results, the LESENSE decoder provides the ability to define a finite state machine with up to 32 states, as well as define programmable actions upon state transitions. This allows the decoder to implement a wide range of decoding schemes, such as quadrature decoding.
- A RAM block is used for storage of configuration and measurement results. This allows LESENSE to have a relatively large result buffer enabling the chip to remain in a low energy mode for long periods of time while collecting sensor data.

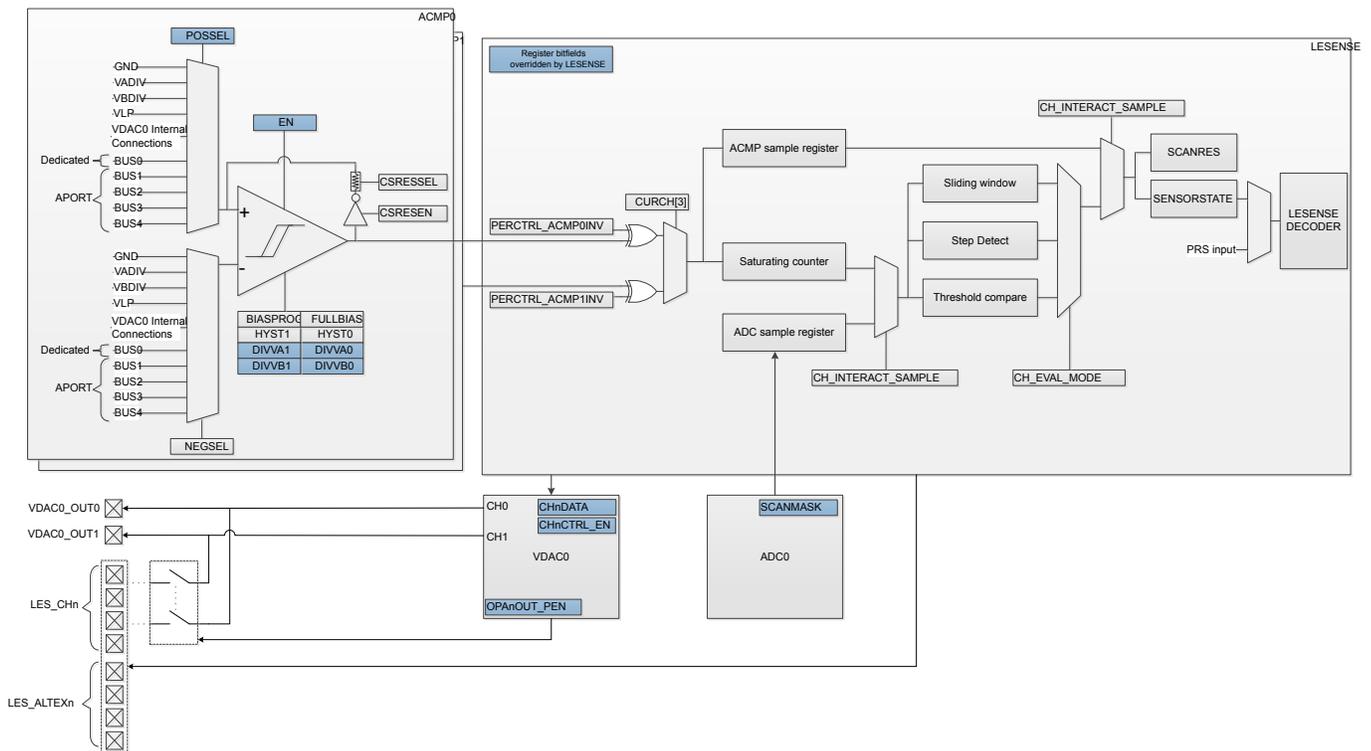


Figure 29.1. LESENSE Block Diagram

### 29.3.1 Channel Configuration

LESENSE has 16 individually configurable channels, each with its own set of configuration registers. Channel configuration is split into three registers; CH<sub>x</sub>\_TIMING, CH<sub>x</sub>\_INTERACT, and CH<sub>x</sub>\_EVAL. Individual timing for each sensor is configured in CH<sub>x</sub>\_TIMING, sensor interaction is configured in CH<sub>x</sub>\_INTERACT, and configurations regarding evaluation of the measurements are done in CH<sub>x</sub>\_EVAL. For improved readability, CH<sub>x</sub>\_CONF will be used to refer to the channel configuration registers (CH<sub>x</sub>\_TIMING, CH<sub>x</sub>\_INTERACT, and CH<sub>x</sub>\_EVAL) throughout this chapter.

By default, the channel configuration registers are directly mapped to the channel number. Configuring SCANCONF in CTRL makes it possible to alter this mapping.

Configuring SCANCONF to INVMAP will make channels 0-7 use the channel configuration registers for channels 8-15, and vice versa. This feature allows an application to quickly and easily switch the configuration set for the channels.

Setting SCANCONF to TOGGLE will make channel *x* alternate between using CH<sub>*x*</sub>\_CONF and CH<sub>*x*+8</sub>\_CONF. The configuration used is decided by the state of the corresponding bit in SCANRES. For instance, if channel 3 is performing a scan and bit 3 in SCANRES is set, CH<sub>11</sub>\_CONF will be used. Channels 8 through 15 will toggle between CH<sub>*x*</sub>\_CONF and CH<sub>*x*-8</sub>\_CONF. This mode provides an easy way to implement hysteresis on channel events, as threshold values can be changed depending on the sensor status.

Setting SCANCONF to DECDEF will make the state of the decoder define which scan configuration to be used. If the decoder state is at index 16 or higher, channel *x* will use CH<sub>*x*+8</sub>\_CONF, otherwise it will use CH<sub>*x*</sub>\_CONF. Similarly, channels 8 through 15 will use CH<sub>*x*</sub>\_CONF when the decoder state index is less than 8 and CH<sub>*x*-8</sub>\_CONF when the decoder state index is higher than 7. Allowing the decoder state to define which configuration to use enables easy implementation of hysteresis, for example, as different threshold values can be used for the same channel depending on the state of the application. [Table 29.1 LESENSE Scan Configuration Selection on page 971](#) summarizes how channel configuration is selected for different settings of SCANCONF.

**Table 29.1. LESENSE Scan Configuration Selection**

| LESENSE<br>channel <i>x</i> | SCANCONF                     |                                |                              |                                |                              |                                |
|-----------------------------|------------------------------|--------------------------------|------------------------------|--------------------------------|------------------------------|--------------------------------|
|                             | DIRMAP                       | INVMAP                         | TOGGLE                       |                                | DECDEF                       |                                |
|                             |                              |                                | SCANRES[ <i>n</i> ] = 0      | SCANRES[ <i>n</i> ] = 1        | DECSTATE < 16                | DECSTATE ≥ 16                  |
| 0 ≤ <i>x</i> < 8            | CH <sub><i>x</i></sub> _CONF | CH <sub><i>x</i>+8</sub> _CONF | CH <sub><i>x</i></sub> _CONF | CH <sub><i>x</i>+8</sub> _CONF | CH <sub><i>x</i></sub> _CONF | CH <sub><i>x</i>+8</sub> _CONF |
| 8 ≤ <i>x</i> < 16           | CH <sub><i>x</i></sub> _CONF | CH <sub><i>x</i>-8</sub> _CONF | CH <sub><i>x</i></sub> _CONF | CH <sub><i>x</i>-8</sub> _CONF | CH <sub><i>x</i></sub> _CONF | CH <sub><i>x</i>-8</sub> _CONF |

Channels are enabled in the CHEN register, where bit *x* enables channel *x*. During a scan, all enabled channels are measured, starting with the lowest indexed channel. [Figure 29.3 Scan Sequence on page 972](#) illustrates a scan sequence with channels 3, 5, and 9 enabled.

### 29.3.2 Scan Sequence

LESENSE runs on  $LFACLK_{LESENSE}$ , which is a prescaled version of  $LFACLK$ . The prescaling factor for  $LFACLK_{LESENSE}$  is selected in the CMU, available prescaling factors are:

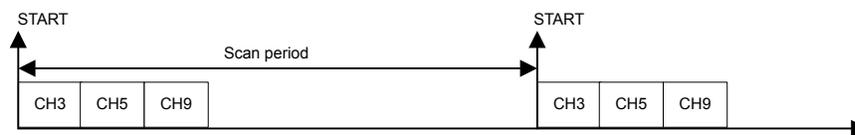
- DIV1:  $LFACLK_{LESENSE} = LFACLK/1$
- DIV2:  $LFACLK_{LESENSE} = LFACLK/2$
- DIV4:  $LFACLK_{LESENSE} = LFACLK/4$
- DIV8:  $LFACLK_{LESENSE} = LFACLK/8$

All enabled channels are scanned each scan period. How a new scan is started is configured in the `SCANMODE` bit field in `CTRL`. If set to `PERIODIC`, the scan frequency is generated using a counter which is clocked by  $LFACLK_{LESENSE}$ . This counter has its own prescaler. This prescaling factor is configured in `PCPRESC` in `TIMCTRL`. A new scan sequence is started each time the counter reaches the top value, `PCTOP`. The scan frequency is calculated using [Figure 29.2 Scan Frequency on page 972](#). If `SCANMODE` is set to `ONE-SHOT`, a single scan will be made when `START` in `CMD` is set. To start a new scan on a PRS event, set `SCANMODE` to `PRS` and configure PRS channel in `PRSEL`. The PRS start signal needs to be active for at least one  $LFACLK_{LESENSE}$  cycle to make sure LESENSE is able to register it.

$$F_{scan} = LFACLK_{LESENSE} / ((1 + PCTOP) * 2^{PCPRESC})$$

**Figure 29.2. Scan Frequency**

It is possible to interleave additional sensor measurements in between the periodic scans. Issuing a start command when LESENSE is idle will immediately start a new scan, without disrupting the frequency of the periodic scans. If the period counter overflows during the interleaved scan, the periodically scheduled scan will start immediately after the interleaved scan completes.



**Figure 29.3. Scan Sequence**

### 29.3.3 Sensor Timing

For each channel in the scan sequence, the LESENSE interface goes through three phases: idle, excite, and measure. The durations of the excite and measure phases are configured in the CHx\_TIMING registers. The excite phase duration can be configured to be either a number of AUXHFRCO cycles or a number of LFACTLK<sub>LESENSE</sub> cycles, depending on which one is selected by the EXCLK bit in the CHx\_INTERACT register. LESENSE includes two timers: A low frequency timer, running on LFACTLK<sub>LESENSE</sub>, and a high frequency timer, running on AUXHFRCO. The low frequency or high frequency timers can be prescaled by configuring LFPRESC or AUXPRESC, respectively, in the TIMCTRL register. The duration of the measure phase is programmed via MEASUREDLY and SAMPLEDLY in the CHx\_TIMING registers. The output of the ACMP will be ignored for MEASUREDLY EXCLK cycles after start of the sensor measurement. Sampling of the sensor will happen after SAMPLEDLY LFACTLK<sub>LESENSE</sub>, or AUXHFRCO cycles, depending on the configuration of the SAMPLECLK in the CHx\_INTERACT register. The configurable measure- and sample delays enables LESENSE to easily define exact time windows for sensor measurements. A start delay can be inserted before sensor measurement begin by configuring STARTDLY in TIMCTRL. This delay can be used to ensure that the VDAC conversion is done and voltages have stabilized before the sensor measurement begins. The AUXHFRCO startup can be delayed until the system enters the excite phase, by configuring AUX-STARTUP in TIMCTRL to ONDEMAND. This will reduce the time the AUXHFRCO is enabled and reduce power consumption, with the tradeoff that the starting point for high frequency timing will also be delayed the same amount as the AUXHFRCO startup time.

Figure 29.4 Timing Diagram, AUXHFRCO Based Timing on page 973 depicts a sensor sequence with AUXHFRCO based timing (EXTIME=5, MEASUREDLY=7, SAMPLEDLY=13), while Figure 29.5 Timing Diagram, LFACTLK Based Timing on page 974 depicts a sequence with LFACTLK<sub>LESENSE</sub> based timing (EXTIME=1, MEASUREDLY=1, SAMPLEDLY=2).

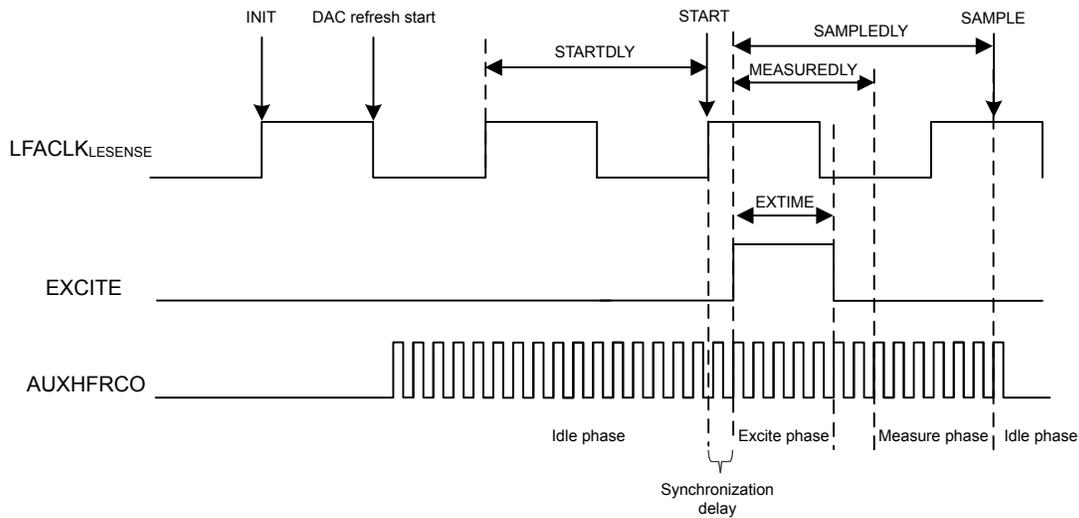
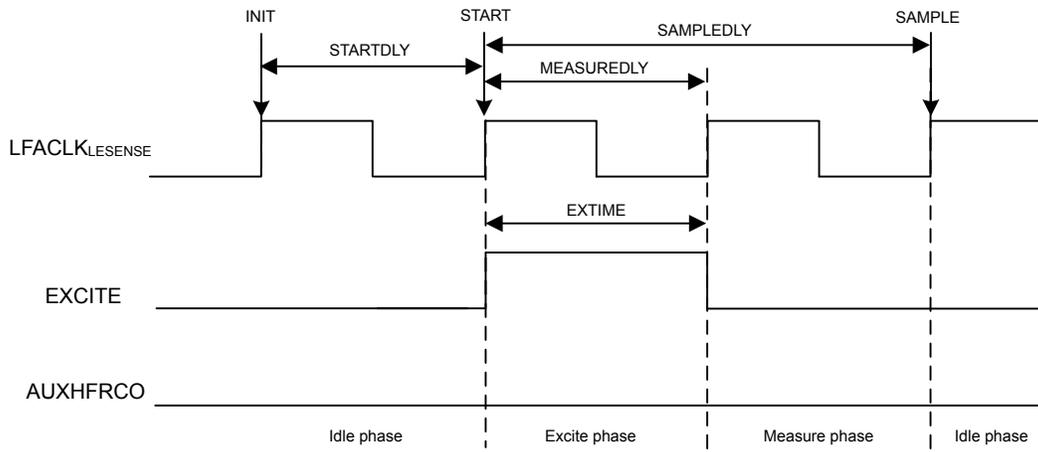


Figure 29.4. Timing Diagram, AUXHFRCO Based Timing



**Figure 29.5. Timing Diagram, LFACTK Based Timing**

### 29.3.4 Sensor Interaction

Many sensor types require some type of excitation in order to work. The LESENSE module can generate a variety of sensor stimuli, both on the same pin as the measurement is to be made on, as well as alternative pins.

By default, excitation is performed on the pin associated with the channel (i.e., excitation and sensor measurement is performed on the same pin). The mode of the pin during the excitation phase is configured by the EXMODE bitfield in CHx\_INTERACT. The available modes during the excite phase are:

- DISABLED: The pin is disabled.
- HIGH: The pin is driven high.
- LOW: The pin is driven low.
- DACOUT: The pin is connected to the output of a VDAC channel.

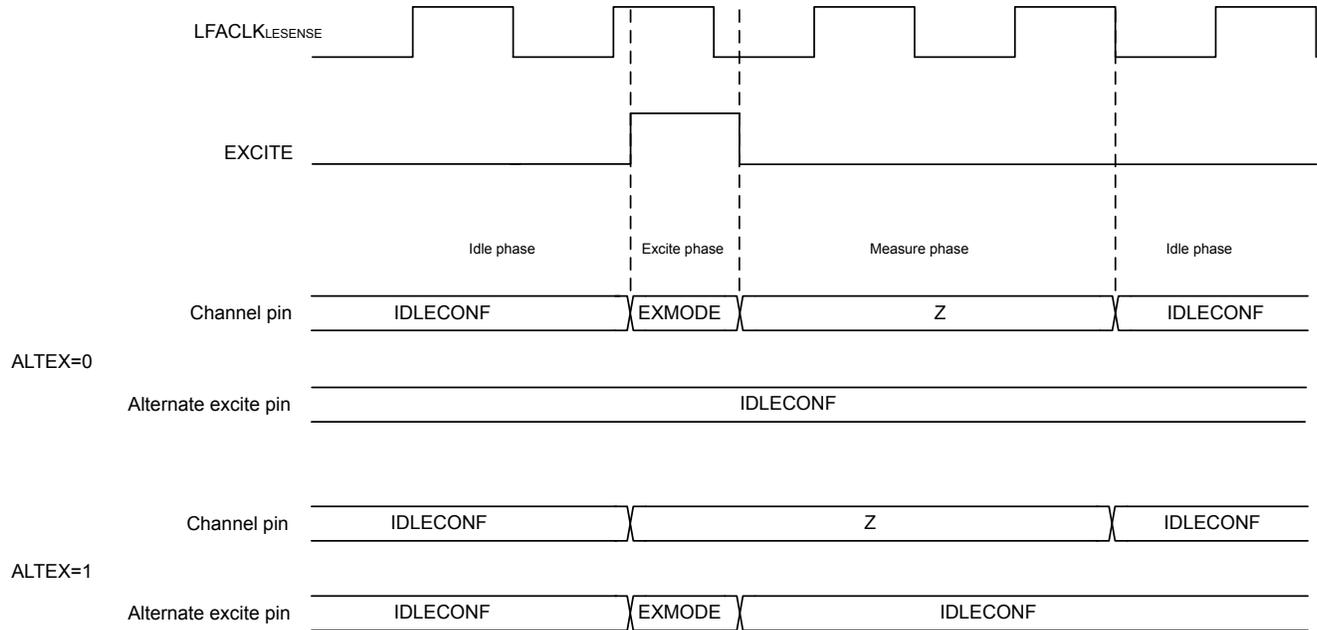
**Note:** Excitation with VDAC output is only available on some channels. Refer to [29.3.9 VDAC Interface](#) for details. If the VDAC is in opamp-mode, setting EXMODE to DACOUT will result in excitation with output from the opamp.

LESENSE is able to perform sensor excitation on a pin other than the one being measured. When ALTEX in CHx\_INTERACT is set, the excitation will occur on the alternative excite pin associated with the given channel. By default, the alternative excite pins are mapped to the LES\_ALTEX pins, but they can also be mapped to LESENSE CH<sub>X+8 mod 16</sub>. Mapping of the alternative excite pins is configured in ALTEXMAP in the CTRL register. [Table 29.2 LESENSE Excitation Pin Mapping on page 975](#) summarizes the mapping of excitation pins for different configurations.

**Table 29.2. LESENSE Excitation Pin Mapping**

| LESENSE channel | ALTEX = 0 | ALTEX = 1     |                  |
|-----------------|-----------|---------------|------------------|
|                 |           | ALTEXMAP = CH | ALTEXMAP = ALTEX |
| 0               | LES_CH0   | LES_CH8       | LES_ALTEX0       |
| 1               | LES_CH1   | LES_CH9       | LES_ALTEX1       |
| 2               | LES_CH2   | LES_CH10      | LES_ALTEX2       |
| 3               | LES_CH3   | LES_CH11      | LES_ALTEX3       |
| 4               | LES_CH4   | LES_CH12      | LES_ALTEX4       |
| 5               | LES_CH5   | LES_CH13      | LES_ALTEX5       |
| 6               | LES_CH6   | LES_CH14      | LES_ALTEX6       |
| 7               | LES_CH7   | LES_CH15      | LES_ALTEX7       |
| 8               | LES_CH8   | LES_CH0       | LES_ALTEX0       |
| 9               | LES_CH9   | LES_CH1       | LES_ALTEX1       |
| 10              | LES_CH10  | LES_CH2       | LES_ALTEX2       |
| 11              | LES_CH11  | LES_CH3       | LES_ALTEX3       |
| 12              | LES_CH12  | LES_CH4       | LES_ALTEX4       |
| 13              | LES_CH13  | LES_CH5       | LES_ALTEX5       |
| 14              | LES_CH14  | LES_CH6       | LES_ALTEX6       |
| 15              | LES_CH15  | LES_CH7       | LES_ALTEX7       |

[Figure 29.6 Pin Sequencing on page 976](#) illustrates the sequencing of the pin associated with the active channel and its alternative excite pin.



**Figure 29.6. Pin Sequencing**

The LES\_ALTEX<sub>n</sub> pins have the ability to excite regardless of what channel is active. Setting AEX<sub>n</sub> in ALTEXCONF will make LES\_ALTEX<sub>n</sub> excite for all channels using alternative excitation (i.e., ALTEX in CH<sub>x</sub>\_INTERACT is set).

**Note:** When exciting on the pin associated with the active channel, the pin will go through a tri-stated phase before returning to the idle configuration. This will not happen on pins used as alternative excitation pins.

The pin configuration for the idle phase can be configured individually for each LESENSE channel and alternative excite pin in the IDLECONF and ALTEXCONF registers. The modes available are the same as the modes available in the excitation phase. In the measure phase, the pin mode on the active channel is always disabled (analog input).

To allow the LESENSE mode to control a GPIO pin, the pin must be enabled in the ROUTEPEN register and configured as push-pull. The IDLECONF configuration should not be altered while the pin enable for a given pin is set in ROUTEPEN.

### 29.3.5 Sensor Sampling

During the measurement phase, LESENSE can sample data from sensors using either ADC0 or an ACMP. This is configured in CH<sub>x</sub>\_INTERACT\_SAMPLE. If the ACMP is used, LESENSE can evaluate the ACMP output at a single point in time (CH<sub>x</sub>\_INTERACT\_SAMPLE = ACMP), or count pulses on the ACMP output (CH<sub>x</sub>\_INTERACT\_SAMPLE = ACMPCOUNT) for a programmable period of time.

LESENSE includes the ability to sample both analog comparators simultaneously, effectively cutting the time spent on sensor interaction in some applications in half. Setting DUALSAMPLE in CTRL enables this mode. In dual sample mode, channels X and X+8 are paired, meaning they will be sampled at the same time. DUALSAMPLE mode only works when CH<sub>x</sub>\_INTERACT\_SAMPLE is set to ACMP.

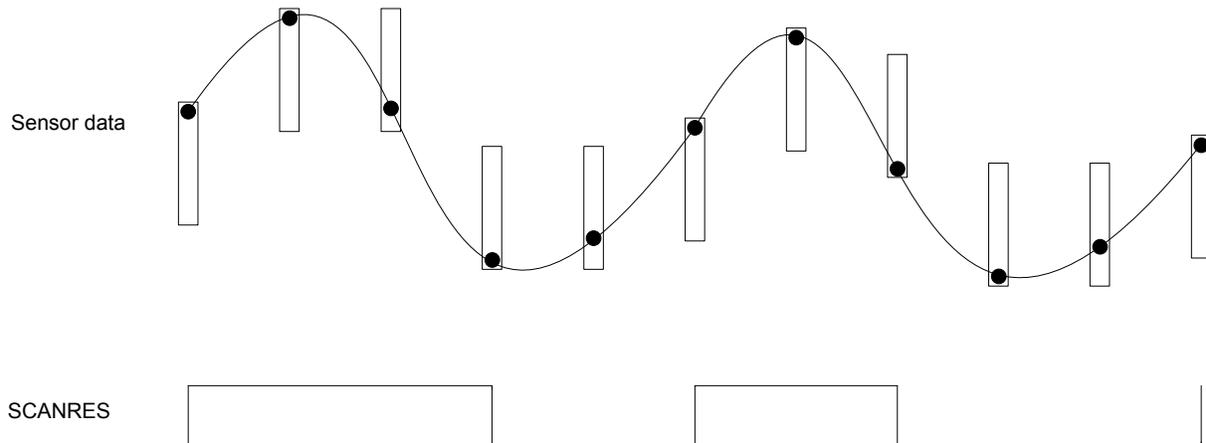
If ADC0 is used, LESENSE will initiate ADC conversions and fetch the ADC data for further evaluation. If the ADC is configured in differential mode, CH<sub>x</sub>\_INTERACT\_SAMPLE must be set to ADCDIFF. In this mode, the output from the ADC and the threshold used for comparison are given in two's complement notation.

See sections [29.3.12 ADC Interface](#) and [29.3.10 ACMP Interface](#) for more details on the LESENSE interface to the ADC and ACMPs. The sampled data from ADC or ACMP will be referred to as sensor data in the remainder of this manual.



### 29.3.6.2 Sliding Window

In sliding window mode, the sensor data is compared against the upper and lower limits of a window range. The window is defined by a base, given by `CHx_EVAL_COMPTHRES`, and a size configured in `EVALCTRL_WINSIZE`. The window size is constant and the same for all LESENSE channels, while the base is specific to each channel and will be updated by LESENSE when the sensor data is outside the current window range. If the sensor data is within the window range, the sensor evaluation will remain the same as it was for the previous measurement. If the sensor data is below the window range, the measurement will be evaluated to false. If the sensor data is above the window range, the measurement will be evaluated to true. In both cases, the window base in `CHx_EVAL_COMPTHRES` will be updated to reflect the new window range. [Figure 29.8 Sliding Window on page 978](#) shows how the sliding window evaluation mode can be used to implement a system with two self-calibrating thresholds.



**Figure 29.8. Sliding Window**

### 29.3.6.3 Step Detection

Step detection is used to detect steps in the sensor data compared to sensor data from the previous measurement. The size of the step is configured in `EVALCTRL_WINSIZE`. In this mode, step up and step down are evaluated as described in [Figure 29.9 Step Detection on page 978](#):

$$\text{STEP\_UP} = \text{SENSORDATA}_i \geq \text{SENSORDATA}_{i-1} + \text{EVALCTRL\_WINSIZE}$$

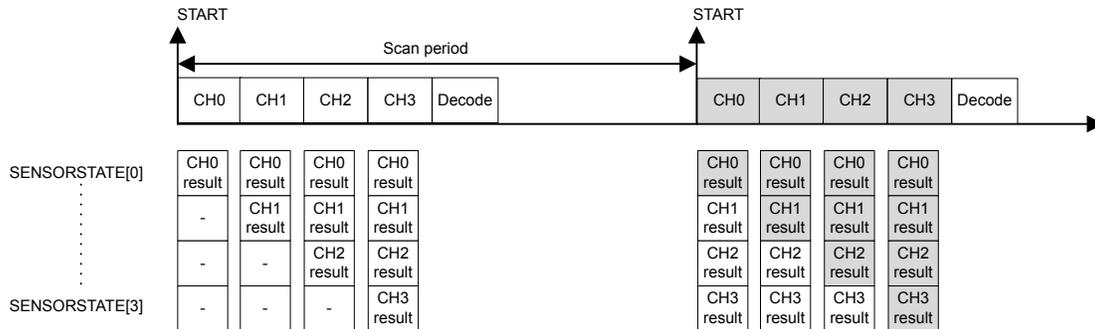
$$\text{STEP\_DOWN} = \text{SENSORDATA}_i < \text{SENSORDATA}_{i-1} - \text{EVALCTRL\_WINSIZE}$$

**Figure 29.9. Step Detection**

If either a step up or a step down is detected, the `SCANRES` bit for the active channel will be set. In addition, the `STEPPDIR` bit for the channel will be updated to indicate if a step up or a step down was detected. `STEPPDIR = 1` indicates a step up. In this mode, previous sensor data is stored in `CHx_EVAL_COMPTHRES`.

### 29.3.7 Decoder

Many applications, such as quadrature decoding, require some sort of processing of the sensor readings. In quadrature decoding, the sensors repeatedly pass through a set of states which correspond to the position of the sensors. This sequence, and many other decoding schemes, can be described as a finite state machine. To support this type of decoding without CPU intervention, the LESENSE module includes a highly configurable decoder capable of decoding input from up to four sensors. The decoder is implemented as a programmable state machine with up to 32 states. When doing a sensor scan, the results from the sensors are placed in the decoder input register, SENSORSTATE, if DECODE in CHx\_INTERACT is set. The resulting position after a scan is illustrated in [Figure 29.10 Sensor Scan and Decode Sequence on page 979](#), where the bottom blocks show how the SENSORSTATE register is filled. If step detection is enabled, the step direction is placed in SENSORSTATE in the position after the sensor result. When the scan sequence is complete, the decoder evaluates the state of the sensors chosen for decoding, as depicted in [Figure 29.10 Sensor Scan and Decode Sequence on page 979](#).



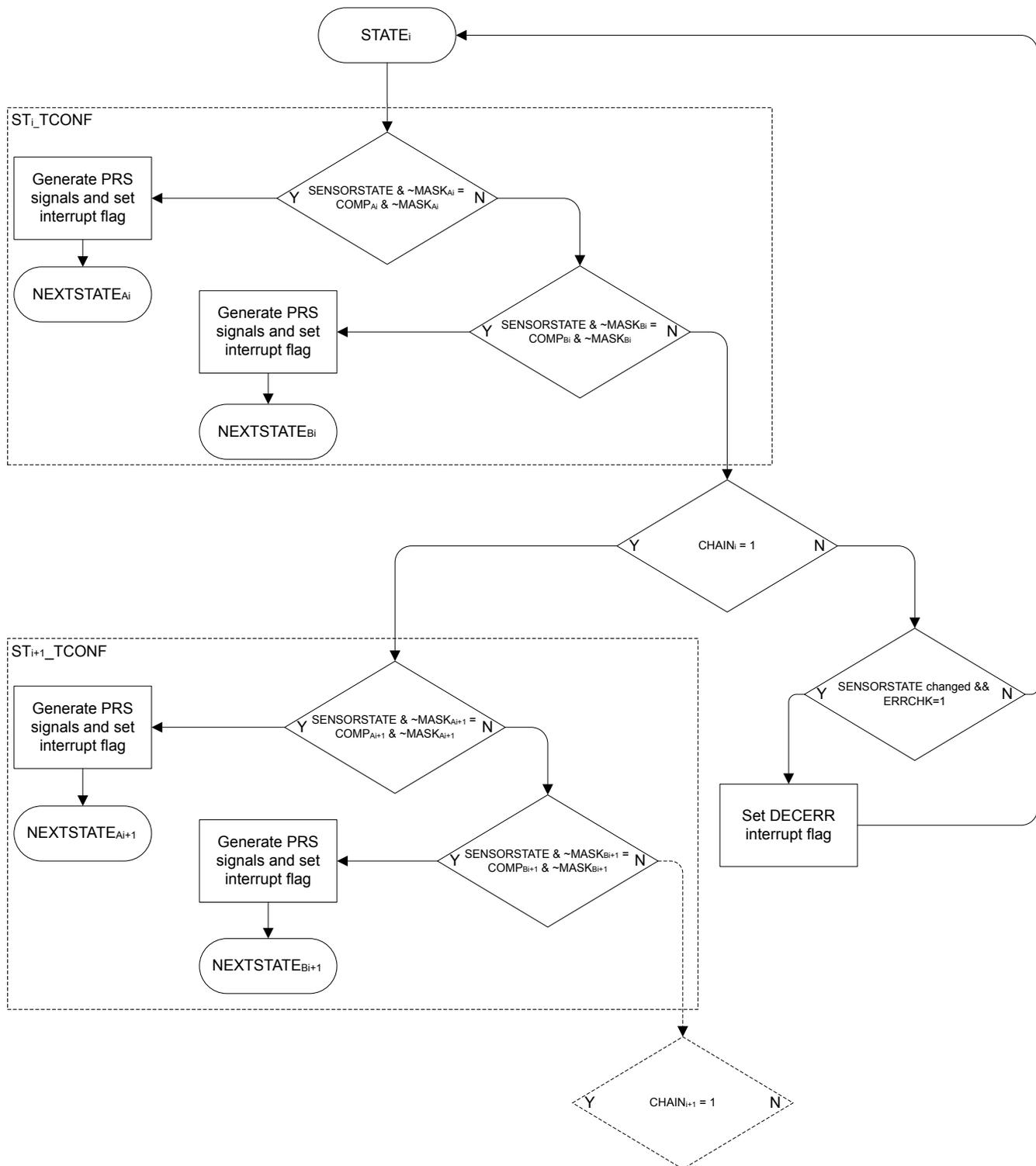
**Figure 29.10. Sensor Scan and Decode Sequence**

Upon a state transition, LESENSE can generate a pulse on one or more of the decoder PRS channels. Which PRS channel to generate a pulse on is configured in the PRSACT bit field. If PRSCNT in DECCTRL is set, count signals will be generated on decoder PRS channels 0 and 1 according to the PRSACT configuration. In this mode, channel 0 will pulse each time a count event occurs, while channel 1 indicates the count direction (1 being up and 0 being down). The count direction will be kept at its previous state in between count events. The EFR32xG13 Wireless Gecko pulse counter may be used to keep track of events based on these PRS outputs.

If SETIF is set, the DECODER interrupt flag will be set when the transition occurs. If INTMAP in DECCTRL and SETIF is set, a transition from state x or x+16 will set the CHx interrupt flag in addition to the DECODER flag.

Setting CHAIN in STx\_TCONFA enables the decoder to evaluate more than two possible transitions for each state. If none of the transitions defined in STx\_TCONFA or STx\_TCONFB match, the decoder will jump to the next descriptor pair and evaluate the transitions defined there. The decoder uses two LFACTK<sub>LESENSE</sub> cycles for each descriptor pair to be evaluated. If ERRCHK in CTRL is set, the decoder will check that the sensor state has not changed if none of the defined transitions match. The DECERR interrupt flag will be set if none of the transitions match and the sensor state has changed. [Figure 29.11 Decoder State Transition Evaluation on page 980](#) illustrates state transitions. The "Generate PRS signals and set interrupt flag" blocks will perform actions according to the configuration in STx\_TCONFA and STx\_TCONFB.

**Note:** If only one transition from a state is used, STx\_TCONFA and STx\_TCONFB should be configured equally.



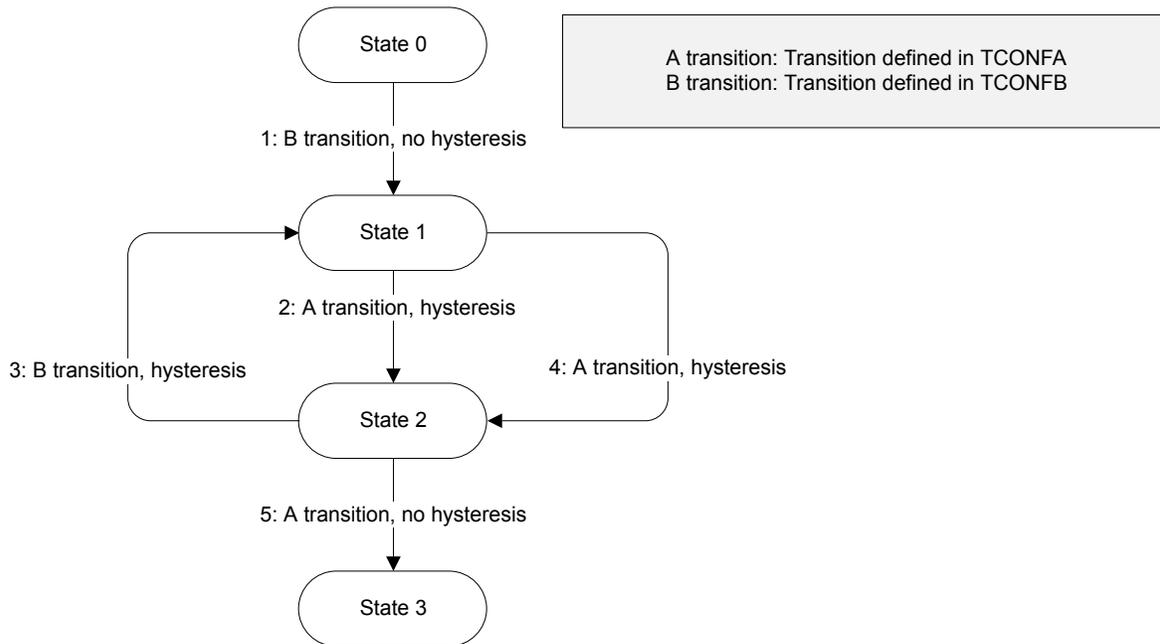
**Figure 29.11. Decoder State Transition Evaluation**

The DECODER has a PRS output named DECCMP. This output can be used to indicate which state, or subset of states, the decoder is currently in. This PRS output is enabled by setting DECCMPEN in PRSCTRL, and configured through DECCMPMASK and DECCMPVAL in PRSCTRL. The value of this PRS output is given by [Figure 29.12 DECCMP PRS Output on page 981](#),

$$\text{PRS\_DECCMP} = (\text{DECSTATE} \& \sim\text{DECCMPMASK}) == (\text{DECCMPVAL} \& \sim\text{DECCMPMASK})$$

**Figure 29.12. DECCMP PRS Output**

To prevent unnecessary interrupt requests or PRS outputs when the decoder toggles back and forth between two states, a hysteresis option is available. The hysteresis function is triggered if a type A transition is preceded by a type B transition, and vice versa. A type A transition is defined in STx\_TCONFA, and a type B transition is defined in STx\_TCONFB. When descriptor chaining is used, a jump to another descriptor will cancel out the hysteresis effect. [Figure 29.13 Decoder Hysteresis on page 981](#) illustrates how the hysteresis triggers upon state transitions.



**Figure 29.13. Decoder Hysteresis**

- When HYSTPRSx is set, PRS signal x is suppressed when the hysteresis triggers.
- When HYSTIRQ is set, interrupt requests are suppressed when the hysteresis triggers.

**Note:** The decoder error interrupt flag, DECERR, is not affected by the hysteresis.

### 29.3.8 Measurement Results

Part of the LESENSE RAM is treated as a circular buffer for storage of up to 16 sensor measurements results. Each time LESENSE writes data to the result buffer, the result write pointer (PTR\_WR) is incremented. Each time a new result is read through the BUFDATA register, the result read pointer (PTR\_RD) is incremented. The read pointer will not be incremented if there is no valid, unread data in the result buffer. By default LESENSE will not write additional data to a full result buffer until the data is read by software or DMA. Setting BUFOW in CTRL enables LESENSE to write to the result buffer even if it is full. In this mode, the result read pointer will follow the write pointer if the buffer is full. The result of this is that data read from the result read register (BUFDATA) will be the oldest unread result. The location pointers are available in PTR.

The result buffer has three flags in the STATUS register: BUFDATAV, BUFHALFFULL, and BUFFULL. The flags indicate when new data is available, when the buffer is half full, and when it is full, respectively.

The result buffer also has three interrupt flags in the IR register: BUFDATAV, BUFLEVEL, and BUFOF. BUFDATAV is set when data is available in the buffer. BUFLEVEL is set when the buffer is either full or half-full, depending on the configuration of BUFIDL in CTRL. BUFOF is set if the result buffer overflows.

During a scan, the state of each sensor is stored in SCANRES. If a sensor triggers, a 1 is stored in SCANRES, else a 0 is stored in SCANRES. Whether or not a sensor is said to be triggered depends of the configuration for the given channel. See 29.3.6 Sensor Evaluation for details. If STRSAMPLE in CHx\_EVAL is set, the sensor data for each channel will be stored in the LESENSE result buffer. If STRSCANRES in CTRL is set, the result vector, SCANRES, will also be stored in the result buffer. This will be stored after each scan and will be interleaved with the counter values. The contents of the result buffer can be read from BUFDATA or from BUF[x]\_DATA. When reading from BUF[x]\_DATA, neither the result read pointer or the status flags BUFDATAV, BUFHALFFULL, or BUFFULL will be updated. When reading through the BUFDATA register, the oldest unread result will be read.

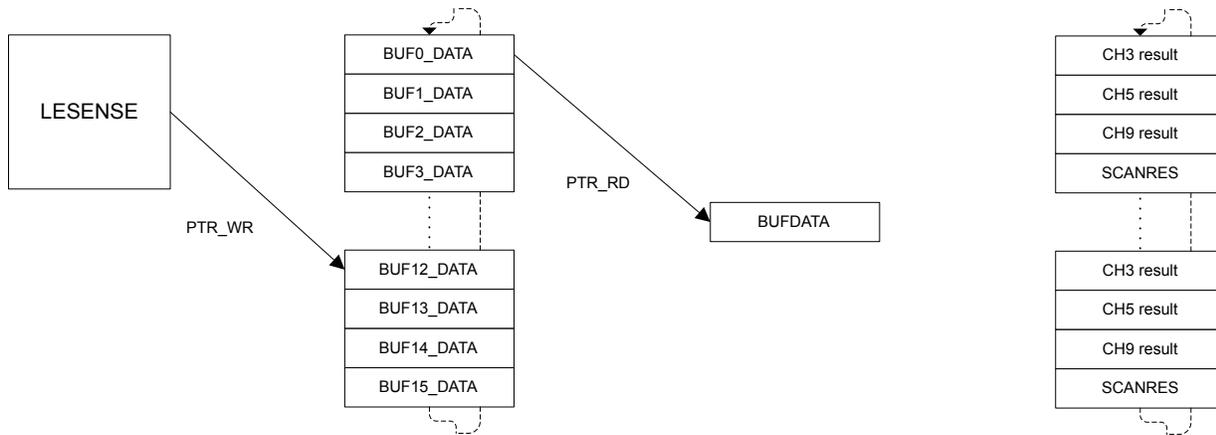


Figure 29.14. Circular Result Buffer

Figure 29.14 Circular Result Buffer on page 982 illustrates how the result buffer would be filled when channels 3,5, and 9 are enabled and have STRSAMPLE in CHx\_EVAL set, in addition to STRSCANRES in CTRL. The measurement result from the three channels will be sequentially written during the scan, while SCANRES is written to the result buffer upon scan completion.

### 29.3.9 VDAC Interface

LESENSE is able to drive the VDAC for generation of accurate reference voltages. This is enabled by setting DACCHxEN in PERCTRL. The refresh rate of the VDAC channels can be configured in DACCONVTRIG in PERCTRL. If DACCONVTRIG is set to CHANNELSTART, the VDAC channels are refreshed prior to each sensor measurement, as depicted in [Figure 29.4 Timing Diagram, AUXHFRCO Based Timing on page 973](#). If DACCONVTRIG is set to SCANSTART, the VDAC channels are refreshed prior to each scan. The conversion data is either taken from the data registers in the EFR32xG13 Wireless Gecko VDAC interface (VDAC0\_CH0DATA and VDAC0\_CH1DATA) or from the THRES bitfield in the CHx\_INTERACT register for the active LESENSE channel. VDAC data used is configured in DACCHxDATA in PERCTRL.

Bias configuration, calibration and reference selection is done in the EFR32xG13 Wireless Gecko VDAC module and LESENSE will not override these configurations.

LESENSE has the possibility to control switches that connect the VDAC alternate outputs. This allows LESENSE to excite sensors with output from the VDAC channels, this is done by setting CHx\_INTERACT\_EXMODE to DACOUT. The LESENSE channels can also be connected to the VDAC output when the given channel is idle, this is done by setting IDLECONF\_CHx to DAC.

**Note:** Only LESENSE channels 4, 5, 7, 10, 12, 13 have the possibility to excite using the VDAC alternate outputs, or connect to the VDAC alternate outputs during the idle phase.

The VDAC may be chosen as reference to the analog comparators for accurate reference generation. If the VDAC is configured in continuous mode this does not require any external components. If sample/off mode is used, an external capacitor is needed to maintain the voltage between samples. To configure the VDAC to use this external capacitor, connect the capacitor to the VDAC pin for the given channel and set SHORT in VDAC\_OPAX\_OUT.

**Note:** The VDAC mode should not be altered while DACACTIVE in STATUS is set

### 29.3.10 ACMP Interface

The analog comparators (ACMPs) are used to measure the sensors, and have to be configured according to the application in order for LESENSE to work properly. Depending on the configuration in the ACMP0MODE and ACMP1MODE bit-fields in PERCTRL, LESENSE will take control of the positive input mux and the voltage dividers (DIVVA, DIVVB) for ACMP0 and ACMP1. The remaining configuration of the analog comparators is done in the ACMP register interface.

If ACMPxMODE in PERCTRL is set to MUX, LESENSE will take control of the positive input mux of the ACMP, through the external override interface, described in the ACMP chapter (see [26.3.12 External Override Interface](#)). The offset given by LESENSE, EXT\_OFFSET, depends on whether one or two ACMPs are controlled by LESENSE. If only one ACMP is used, EXT\_OFFSET will have the same value as the active channel. If both ACMP0 and ACMP1 are used, LESENSE channel 0-7 will use ACMP0 with EXT\_OFFSET 0-7, and LESENSE channel 8-15 will use ACMP1 with EXT\_OFFSET 0-7.

If ACMPxMODE in PERCTRL is set to MUXTHRES, LESENSE will also take control of the voltage dividers in the ACMP, DIVVA and DIVVB. The thresholds used are individual to each channel and is configured using the 6 LSBs of CHx\_INTERACT\_THRES. By default, ACMP\_HYSTERESIS0\_DIVVX and ACMP\_HYSTERESIS1\_DIVVX will be given the same value, the 6 LSBs of CHx\_INTERACT\_THRES. To allow different values for ACMP\_HYSTERESIS0\_DIVVX and ACMP\_HYSTERESIS1\_DIVVX, ACMPxHYSTEN in PERCTRL needs to be set. This allows the hysteresis feature in the ACMP to be utilized. ACMP\_HYSTERESIS0\_DIVVX will get the value programmed in CHx\_INTERACT\_THRES[5:0], while ACMP\_HYSTERESIS1\_DIVVX will get the value programmed in CHx\_INTERACT\_THRES[11:6].

### 29.3.11 ACMP and VDAC Duty Cycling

By default, the analog comparators and the VDAC are shut down between LESENSE scans to save energy. If this is not desired, WARMUPMODE in PERCTRL can be configured to prevent them from being shut down.

Both the VDAC and analog comparators rely on a bias module for correct operation. This bias module has a low power mode which consumes less energy at the cost of reduced accuracy. BIASMODE in BIASCTRL configures how the bias module is controlled by LESENSE. When set to DUTYCYCLE, LESENSE will set the bias module in high accuracy mode whenever LESENSE is active, and keep it in the low power mode otherwise. When BIASMODE is set to HIGHACC, the high accuracy mode is always selected. When set to DONTTOUCH, LESENSE will not control the bias module.

### 29.3.12 ADC Interface

The LESENSE module can be configured to trigger conversions on ADC0 and use data from ADC0 to evaluate sensor status. In order to do this, the scan mode of the ADC has to be configured. When the sample delay configured in CHx\_TIMING\_SAMPLEDLY has expired, LESENSE will initiate an ADC sample. The active LESENSE channel determines which ADC0 channel to be sampled, where LESENSE channel X corresponds to ADC0 scan channel X.

### 29.3.13 DMA Requests

LESENSE issues a DMA request when the result buffer is either full or half full, depending on the configuration of BUFIDL in CTRL. The request is cleared when the buffer level drops below the threshold defined in BUFIDL. A single DMA request is also set whenever there is unread data in the buffer. DMAWU in CTRL configures at which buffer level LESENSE should wake-up the DMA when in EM2.

**Note:** The DMA controller should always fetch data from the BUFDATA register.

### 29.3.14 PRS Output

LESENSE is an asynchronous PRS producer and has twenty PRS outputs. The decoder has four outputs and in addition, all bits in the SCANRES register are available as PRS outputs. For further information on the decoder PRS output, refer to [29.3.7 Decoder](#).

### 29.3.15 RAM

LESENSE includes a RAM block used for storage of configuration and results. Registers mapped to the RAM include: STx\_TCONFA, STx\_TCONFB, BUFx\_DATA, BUFDATA, CHx\_TIMING, CHx\_INTERACT, and CHx\_EVAL. These registers have unknown value out of reset and have to be initialized before use.

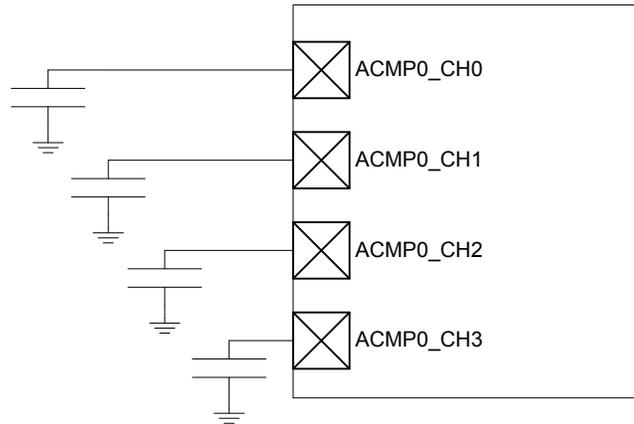
**Note:** Read-modify-write operations on uninitialized RAM register produces undefined values.

### 29.3.16 Application Examples

The following sections detail several example applications for the LESENSE block.

### 29.3.16.1 Capacitive Sense

Figure 29.15 Capacitive Sense Setup on page 985 illustrates how the EFR32xG13 Wireless Gecko can be configured to monitor four capacitive buttons.



**Figure 29.15. Capacitive Sense Setup**

The following steps show how to configure LESENSE to scan through the four buttons 100 times per second, issuing an interrupt if one of them is pressed.

1. Assuming  $LF_{ACLK_{LESENSE}}$  is 32 kHz, set PCPRESC to 3 and PCTOP to 39 in CTRL. This will set the LESENSE scan frequency to 100 Hz.
2. Enable channels 0 through 3 in CHEN and set IDLECONF for these channels to DISABLED. In capacitive sense mode, the GPIO should always be disabled (i.e., analog input).
3. Configure the ACMP to operate in CAPSENSE mode (refer to the ACMP chapter for more details).
4. Configure the following bit fields in CHx\_CONF, for channels 0 through 3:
  - a. Set EXTIME to 0. No excitation is needed in this mode.
  - b. Set SAMPLE to ACMPCOUNT and COMP to LESS. This makes LESENSE interpret a sensor as active if the frequency on a channel drops below the threshold (i.e., the button is pressed).
  - c. Set SAMPLEDLY to an appropriate value - each sensor will be measured for  $SAMPLEDLY/F_{LF_{ACLK_{LESENSE}}}$  seconds. MEASUREDLY should be set to 0
5. Set CTRTHRESHOLD to an appropriate value. An interrupt will be issued if the counter value for a sensor is below this threshold after the measurement phase.
6. Enable interrupts on channels 0 through 3.
7. Start scan sequence by writing a 1 to START in CMD.

In a capacitive sense application, it might be required to calibrate the threshold values on a periodic basis, for example to compensate for humidity and other physical variations. LESENSE is able to store up to 16 counter values from a configurable number of channels, making it possible to collect sample data while in EM2. When calibration is to be performed, the CPU only has to be woken up for a short period of time as the data to be processed already lies in the result registers. To enable storing of the count value for a channel, set STRSAMPLE in the CHx\_INTERACT register.

### 29.3.16.2 LC Sensor

Figure 29.16 LC Sensor Setup on page 986 below illustrates how the EFR32xG13 Wireless Gecko can be set up to monitor four LC sensors.

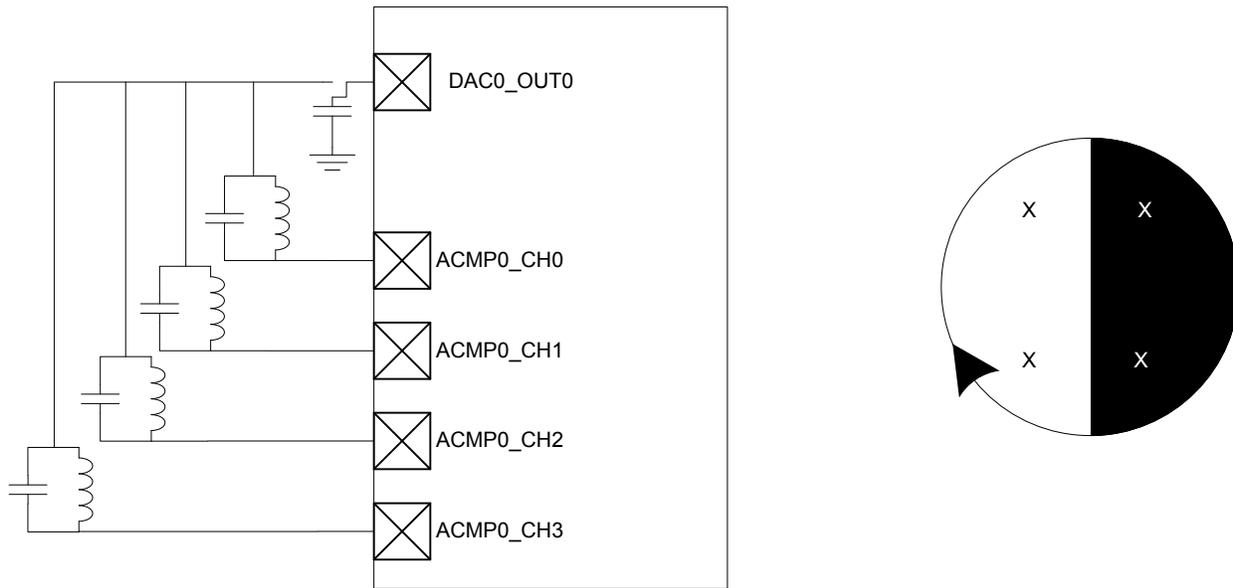


Figure 29.16. LC Sensor Setup

LESENSE can be used to excite and measure the damping factor in LC sensor oscillations. To measure the damping factor, the ACMP can be used to generate a high output each time the sensor voltage exceeds a certain level. These pulses are counted using an asynchronous counter and compared with the threshold in COMPTHRES in the CHx\_EVAL register. If the number of pulses exceeds the threshold level, the sensor is said to be active, otherwise it is inactive. Figure 29.17 LC Sensor Oscillations on page 986 illustrates how the output pulses from the ACMP correspond to damping of the oscillations. The results from sensor evaluation can automatically be fed into the decoder in order to keep track of rotations.

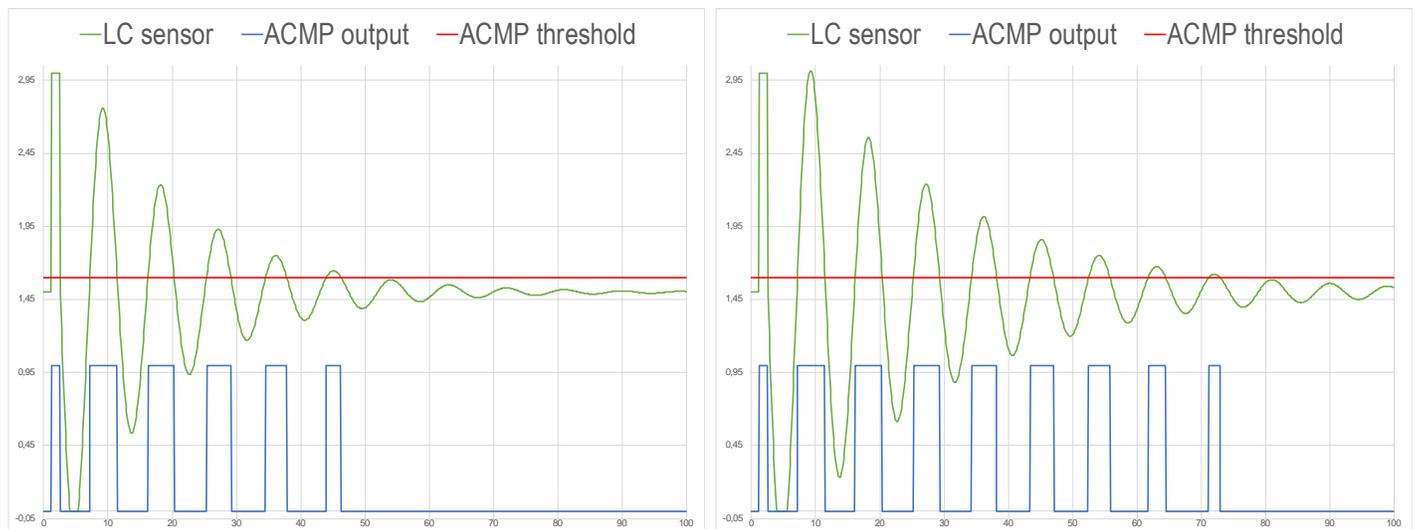


Figure 29.17. LC Sensor Oscillations

The following steps show how to configure LESENSE to scan through the four LC sensors 100 times per second.

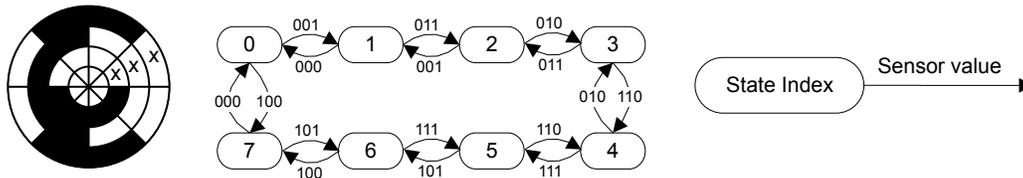
1. Assuming  $LFACLK_{LESENSE}$  is 32kHz, set PCPRESC to 3 and PCTOP to 39 in CTRL. This will set the LESENSE scan frequency to 100Hz.
2. Enable the VDAC and configure it to produce a voltage of  $V_{dd}/2$ .

3. Enable channels 0 through 3 in CHEN. Set IDLECONF for the active channels to DACOUT. The channel pins should be connected to the VDAC output (effectively shorting the LC sensor) in the idle phase to damp the oscillations.
4. Configure the ACMP to use scaled V<sub>dd</sub> as negative input, refer to ACMP chapter for details.
5. Enable and configure PCNT and asynchronous PRS.
6. Configure the GPIOs used as PUSH/PULL.
7. Configure the following bit fields in CH<sub>x</sub>\_CONF, for channels 0 through 3:
  - a. Set EXCLK to AUXHFRCO. AUXHFRCO is needed to achieve short excitation time.
  - b. Set EXTIME to an appropriate value. Excitation will last for EXTIME/F<sub>AUXHFRCO</sub> seconds.
  - c. Set EXMODE to HIGH. The LC sensors are excited by pulling the excitation pin high.
  - d. Set SAMPLE to ACMPCOUNT and COMP to LESS. Status of each sensor is evaluated based on the number of pulses generated by the ACMP. If they are less than the threshold value, the sensor is said to be active.
  - e. Set SAMPLEDLY to an appropriate value, each sensor will be measured for SAMPLEDLY/F<sub>LFACLK\_LESENSE</sub> seconds.
8. Set CTRTHRESHOLD to an appropriate value. If the sensor is active, the counter value after the measurement phase should be less than the threshold. If it is inactive, the counter value should be greater than the threshold.
9. Start scan sequence by writing a 1 to START in CMD.

**Note:** Exciting the LC sensor by pulling the excitation pin high allows the ESD protection in the pads to clamp any voltage swings below the ground voltage, giving a consistent starting point for the oscillations.

### 29.3.16.3 LESENSE Decoder 1

The example below illustrates how the LESENSE module can be used for decoding using three sensors.



**Figure 29.18. FSM Example 1**

Figure 29.18 FSM Example 1 on page 988, configure the following LESENSE registers:

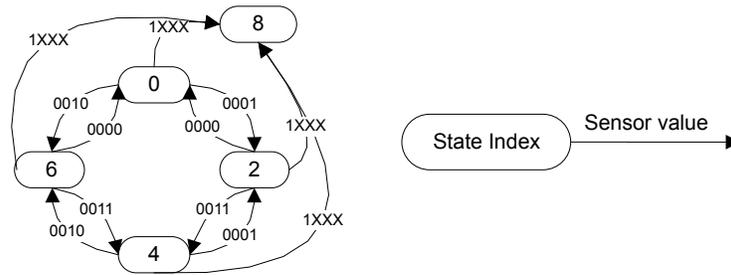
1. Configure the channels to be used, be sure to set DECODE in CHx\_EVAL.
2. Set PRSCNT to enable generation of count waveforms on PRS. Also configure a PCNT to listen to the PRS channels and count accordingly.
3. Configure the following in STx\_TCONFA and STx\_TCONFB:
  - a. Set MASK = 0b1000 in STx\_TCONFA and STx\_TCONFB for all used states. This enables three sensors to be evaluated by the decoder.
  - b. Configure the remaining bit fields in STx\_TCONFA and STx\_TCONFB as described in [Table 29.3 LESENSE Decoder Configuration for FSM Example 1 on page 988](#).
4. To initialize the decoder, run one scan, and read the present sensor status from SENSORSTATE. Then write the index of this state to DECSTATE.
5. Write to START in CMD to start scanning of sensors and decoding.

**Table 29.3. LESENSE Decoder Configuration for FSM Example 1**

| Register | TCONFA_NEXTSTATE | TCONFA_COMP | TCONFA_PRSACT | TCONFB_NEXTSTATE | TCONFB_COMP | TCONFB_PRSACT |
|----------|------------------|-------------|---------------|------------------|-------------|---------------|
| ST0      | 1                | 0b001       | UP            | 7                | 0b100       | DOWN          |
| ST1      | 2                | 0b011       | UP            | 0                | 0b000       | DOWN          |
| ST2      | 3                | 0b010       | UP            | 1                | 0b001       | DOWN          |
| ST3      | 4                | 0b110       | UP            | 2                | 0b011       | DOWN          |
| ST4      | 5                | 0b111       | UP            | 3                | 0b010       | DOWN          |
| ST5      | 6                | 0b101       | UP            | 4                | 0b110       | DOWN          |
| ST6      | 7                | 0b100       | UP            | 5                | 0b111       | DOWN          |
| ST7      | 0                | 0b000       | UP            | 6                | 0b101       | DOWN          |

### 29.3.16.4 LESENSE Decoder 2

The example below illustrates how the LESENSE decoder can be used to implement the state machine seen in [Figure 29.19 FSM Example 2](#) on page 989.



**Figure 29.19. FSM Example 2**

1. Configure STx\_TCONFA and STx\_TCONFB as described in [Table 29.4 LESENSE Decoder Configuration for FSM Example 2](#) on page 989.
2. To initialize the decoder, run one scan, and read the present sensor status from SENSORSTATE. Then write the index of this state to DECSTATE.
3. Write to START in CMD to start scanning of sensors and decoding.

**Table 29.4. LESENSE Decoder Configuration for FSM Example 2**

| Register   | NEXTSTATE | COMP   | MASK   | CHAIN |
|------------|-----------|--------|--------|-------|
| ST0_TCONFA | 8         | 0b1000 | 0b0111 | 1     |
| ST0_TCONFB | 2         | 0b0001 | 0b1000 | -     |
| ST1_TCONFA | 6         | 0b0010 | 0b1000 | 0     |
| ST1_TCONFB | 6         | 0b0010 | 0b1000 | -     |
| ST2_TCONFA | 8         | 0b1000 | 0b0111 | 1     |
| ST2_TCONFB | 4         | 0b0011 | 0b1000 | -     |
| ST3_TCONFA | 0         | 0b0000 | 0b1000 | 0     |
| ST3_TCONFB | 0         | 0b0000 | 0b1000 | -     |
| ST4_TCONFA | 8         | 0b1000 | 0b0111 | 1     |
| ST4_TCONFB | 6         | 0b0010 | 0b1000 | -     |
| ST5_TCONFA | 2         | 0b0001 | 0b1000 | 0     |
| ST5_TCONFB | 2         | 0b0001 | 0b1000 | -     |
| ST6_TCONFA | 8         | 0b1000 | 0b0111 | 1     |
| ST6_TCONFB | 0         | 0b0000 | 0b1000 | -     |
| ST7_TCONFA | 4         | 0b0011 | 0b1000 | 0     |
| ST7_TCONFB | 4         | 0b0011 | 0b1000 | -     |

## 29.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name                 | Type  | Description                          |
|--------|----------------------|-------|--------------------------------------|
| 0x000  | LESENSE_CTRL         | RW    | Control Register                     |
| 0x004  | LESENSE_TIMCTRL      | RW    | Timing Control Register              |
| 0x008  | LESENSE_PERCTRL      | RW    | Peripheral Control Register          |
| 0x00C  | LESENSE_DECCTRL      | RW    | Decoder Control Register             |
| 0x010  | LESENSE_BIASCTRL     | RW    | Bias Control Register                |
| 0x014  | LESENSE_EVALCTRL     | RW    | LESENSE Evaluation Control           |
| 0x018  | LESENSE_PRSCTRL      | RW    | PRS Control Register                 |
| 0x01C  | LESENSE_CMD          | W1    | Command Register                     |
| 0x020  | LESENSE_CHEN         | RW    | Channel Enable Register              |
| 0x024  | LESENSE_SCANRES      | RWH   | Scan Result Register                 |
| 0x028  | LESENSE_STATUS       | R     | Status Register                      |
| 0x02C  | LESENSE_PTR          | R     | Result Buffer Pointers               |
| 0x030  | LESENSE_BUFDATA      | R(a)  | Result Buffer Data Register          |
| 0x034  | LESENSE_CURCH        | R     | Current Channel Index                |
| 0x038  | LESENSE_DECSTATE     | RWH   | Current Decoder State                |
| 0x03C  | LESENSE_SENSORSTATE  | RWH   | Decoder Input Register               |
| 0x040  | LESENSE_IDLECONF     | RW    | GPIO Idle Phase Configuration        |
| 0x044  | LESENSE_ALTEXCONF    | RW    | Alternative Excite Pin Configuration |
| 0x050  | LESENSE_IF           | R     | Interrupt Flag Register              |
| 0x054  | LESENSE_IFS          | W1    | Interrupt Flag Set Register          |
| 0x058  | LESENSE_IFC          | (R)W1 | Interrupt Flag Clear Register        |
| 0x05C  | LESENSE_IEN          | RW    | Interrupt Enable Register            |
| 0x060  | LESENSE_SYNCBUSY     | R     | Synchronization Busy Register        |
| 0x064  | LESENSE_ROUTEPEN     | RW    | I/O Routing Register                 |
| 0x100  | LESENSE_ST0_TCONFA   | RW    | State Transition Configuration a     |
| 0x104  | LESENSE_ST0_TCONFB   | RW    | State Transition Configuration B     |
| ...    | LESENSE_STx_TCONFA   | RW    | State Transition Configuration a     |
| ...    | LESENSE_STx_TCONFB   | RW    | State Transition Configuration B     |
| 0x1F8  | LESENSE_ST31_TCONFA  | RW    | State Transition Configuration a     |
| 0x1FC  | LESENSE_ST31_TCONFB  | RW    | State Transition Configuration B     |
| 0x200  | LESENSE_BUF0_DATA    | RWH   | Scan Results                         |
| ...    | LESENSE_BUFx_DATA    | RWH   | Scan Results                         |
| 0x23C  | LESENSE_BUF15_DATA   | RWH   | Scan Results                         |
| 0x240  | LESENSE_CH0_TIMING   | RW    | Scan Configuration                   |
| 0x244  | LESENSE_CH0_INTERACT | RW    | Scan Configuration                   |

| Offset | Name                  | Type | Description        |
|--------|-----------------------|------|--------------------|
| 0x248  | LESENSE_CH0_EVAL      | RWH  | Scan Configuration |
| ...    | LESENSE_CHx_TIMING    | RW   | Scan Configuration |
| ...    | LESENSE_CHx_INTERACT  | RW   | Scan Configuration |
| ...    | LESENSE_CHx_EVAL      | RWH  | Scan Configuration |
| 0x330  | LESENSE_CH15_TIMING   | RW   | Scan Configuration |
| 0x334  | LESENSE_CH15_INTERACT | RW   | Scan Configuration |
| 0x338  | LESENSE_CH15_EVAL     | RWH  | Scan Configuration |

## 29.5 Register Description

### 29.5.1 LESENSE\_CTRL - Control Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |          |     |       |    |        |    |    |    |            |    |       |    |     |   |            |    |          |   |   |   |   |   |        |  |          |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----------|-----|-------|----|--------|----|----|----|------------|----|-------|----|-----|---|------------|----|----------|---|---|---|---|---|--------|--|----------|
| 0x000         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21       | 20  | 19    | 18 | 17     | 16 | 15 | 14 | 13         | 12 | 11    | 10 | 9   | 8 | 7          | 6  | 5        | 4 | 3 | 2 | 1 | 0 |        |  |          |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    | 0        | 0x0 |       | 0  |        | 0  | 0  |    | 0          |    | 0     |    | 0x0 |   |            |    | 0x0      |   |   |   |   |   | 0x0    |  |          |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    | RW       |     | RW    |    | RW     |    |    |    | RW         |    |       | RW |     |   |            | RW |          |   |   |   |   |   | RW     |  |          |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    | DEBUGRUN |     | DMAWU |    | BUFIDL |    |    |    | STRSCANRES |    | BUFOW |    |     |   | DUALSAMPLE |    | ALTEXMAP |   |   |   |   |   | PRSSEL |  | SCANMODE |

| Bit   | Name  | Reset   | Access | Description   |       |             |             |   |          |   |   |          |  |   |          |   |
|-------|---|---|--------|---|-------|-------------|-------------|---|----------|---|---|----------|--|---|----------|---|
| 31:23 | <i>Reserved</i>                               | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |             |             |   |          |   |   |          |  |   |          |   |
| 22    | DEBUGRUN                                      | 0   | RW     | <b>Debug Mode Run Enable</b><br>Set to keep LESENSE running in debug mode.<br><table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>LESENSE can not start new scans in debug mode</td> </tr> <tr> <td>1</td> <td>LESENSE can start new scans in debug mode</td> </tr> </tbody> </table>  | Value | Description | 0           | LESENSE can not start new scans in debug mode | 1        | LESENSE can start new scans in debug mode                   |   |          |  |   |          |   |
| Value | Description                                   |   |        |   |       |             |             |   |          |   |   |          |  |   |          |   |
| 0     | LESENSE can not start new scans in debug mode |   |        |   |       |             |             |   |          |   |   |          |  |   |          |   |
| 1     | LESENSE can start new scans in debug mode     |   |        |   |       |             |             |   |          |   |   |          |  |   |          |   |
| 21:20 | DMAWU   | 0x0   | RW     | <b>DMA Wake-up From EM2</b><br>Set buffer threshold for waking up the DMA controller when the system is in EM2<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>DISABLE</td> <td>No DMA wake-up from EM2</td> </tr> <tr> <td>1</td> <td>BUFDATAV</td> <td>DMA wake-up from EM2 when data is valid in the result buffer</td> </tr> <tr> <td>2</td> <td>BUFLEVEL</td> <td>DMA wake-up from EM2 when the result buffer is full/half-full depending on BUFIDL configuration</td> </tr> </tbody> </table> | Value | Mode        | Description | 0   | DISABLE  | No DMA wake-up from EM2                                     | 1 | BUFDATAV | DMA wake-up from EM2 when data is valid in the result buffer | 2 | BUFLEVEL | DMA wake-up from EM2 when the result buffer is full/half-full depending on BUFIDL configuration |
| Value | Mode  | Description   |        |   |       |             |             |   |          |   |   |          |  |   |          |   |
| 0     | DISABLE                                       | No DMA wake-up from EM2   |        |   |       |             |             |   |          |   |   |          |  |   |          |   |
| 1     | BUFDATAV                                      | DMA wake-up from EM2 when data is valid in the result buffer  |        |   |       |             |             |   |          |   |   |          |  |   |          |   |
| 2     | BUFLEVEL                                      | DMA wake-up from EM2 when the result buffer is full/half-full depending on BUFIDL configuration                                 |        |   |       |             |             |   |          |   |   |          |  |   |          |   |
| 19    | BUFIDL  | 0   | RW     | <b>Result Buffer Interrupt and DMA Trigger Level</b><br>Set buffer threshold for DMA requests and interrupt generation<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>HALFFULL</td> <td>DMA and interrupt flags set when result buffer is half-full</td> </tr> <tr> <td>1</td> <td>FULL</td> <td>DMA and interrupt flags set when result buffer is full</td> </tr> </tbody> </table>   | Value | Mode        | Description | 0   | HALFFULL | DMA and interrupt flags set when result buffer is half-full | 1 | FULL     | DMA and interrupt flags set when result buffer is full       |   |          |   |
| Value | Mode  | Description   |        |   |       |             |             |   |          |   |   |          |  |   |          |   |
| 0     | HALFFULL                                      | DMA and interrupt flags set when result buffer is half-full   |        |   |       |             |             |   |          |   |   |          |  |   |          |   |
| 1     | FULL  | DMA and interrupt flags set when result buffer is full  |        |   |       |             |             |   |          |   |   |          |  |   |          |   |
| 18    | <i>Reserved</i>                               | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |             |             |   |          |   |   |          |  |   |          |   |
| 17    | STRSCANRES                                    | 0   | RW     | <b>Enable Storing of SCANRES</b><br>When set, SCANRES will be stored in the result buffer after each scan   |       |             |             |   |          |   |   |          |  |   |          |   |

| Bit   | Name            | Reset   | Access  | Description  |
|-------|-----------------|---|---|--|
| 16    | BUFOW           | 0   | RW  | <b>Result Buffer Overwrite</b><br>If set, LESENSE will always write to the result buffer, even if it is full     |
| 15:14 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 13    | DUALSAMPLE      | 0   | RW  | <b>Enable Dual Sample Mode</b><br>When set, both ACMPs will be sampled simultaneously.                           |
| 12    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 11    | ALTEXMAP        | 0   | RW  | <b>Alternative Excitation Map</b><br>This bit is used to configure which pins alternate excitation is mapped to. |
|       | Value           | Mode  | Description   |  |
|       | 0               | ALTEX   | Alternative excitation is mapped to the LES_ALTEX pins.   |  |
|       | 1               | CH  | Alternative excitation is mapped to the pin of LESENSE channel (X+8 mod 16), X being the active channel.                                      |  |
| 10:9  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 8:7   | SCANCONF        | 0x0   | RW  | <b>Select Scan Configuration</b><br>These bits control which CHx_CONF registers to be used.                      |
|       | Value           | Mode  | Description   |  |
|       | 0               | DIRMAP  | The channel configuration register registers used are directly mapped to the channel number.  |  |
|       | 1               | INVMAP  | The channel configuration register registers used are CH <sub>X+8</sub> _CONF for channels 0-7 and CH <sub>X-8</sub> _CONF for channels 8-15. |  |
|       | 2               | TOGGLE  | The channel configuration register registers used toggles between CH <sub>X</sub> _CONF and CH <sub>X+8</sub> _CONF when channel x triggers   |  |
|       | 3               | DECDEF  | The decoder state defines the CONF registers to be used.  |  |
| 6     | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 5:2   | PRSEL           | 0x0   | RW  | <b>Scan Start PRS Select</b><br>Select PRS source for scan start if SCANMODE is set to PRS.                      |
|       | Value           | Mode  | Description   |  |
|       | 0               | PRSCH0  | PRS Channel 0 selected as input   |  |
|       | 1               | PRSCH1  | PRS Channel 1 selected as input   |  |
|       | 2               | PRSCH2  | PRS Channel 2 selected as input   |  |
|       | 3               | PRSCH3  | PRS Channel 3 selected as input   |  |
|       | 4               | PRSCH4  | PRS Channel 4 selected as input   |  |
|       | 5               | PRSCH5  | PRS Channel 5 selected as input   |  |
|       | 6               | PRSCH6  | PRS Channel 6 selected as input   |  |
|       | 7               | PRSCH7  | PRS Channel 7 selected as input   |  |

| Bit | Name     | Reset    | Access | Description  |
|-----|----------|----------|--------|--|
|     | 8        | PRSCH8   |        | PRS Channel 8 selected as input  |
|     | 9        | PRSCH9   |        | PRS Channel 9 selected as input  |
|     | 10       | PRSCH10  |        | PRS Channel 10 selected as input   |
|     | 11       | PRSCH11  |        | PRS Channel 11 selected as input   |
| 1:0 | SCANMODE | 0x0      | RW     | <b>Configure Scan Mode</b><br>These bits control how the scan frequency is decided |
|     | Value    | Mode     |        | Description  |
|     | 0        | PERIODIC |        | A new scan is started each time the period counter overflows                       |
|     | 1        | ONESHOT  |        | A single scan is performed when START in CMD is set                                |
|     | 2        | PRS      |        | Pulse on PRS channel   |

### 29.5.2 LESENSE\_TIMCTRL - Timing Control Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset | Bit Position |    |    |            |    |    |    |    |          |    |    |    |    |    |    |       |    |    |    |    |    |    |     |         |   |   |     |         |   |   |   |   |          |
|--------|--------------|----|----|------------|----|----|----|----|----------|----|----|----|----|----|----|-------|----|----|----|----|----|----|-----|---------|---|---|-----|---------|---|---|---|---|----------|
|        | 31           | 30 | 29 | 28         | 27 | 26 | 25 | 24 | 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16    | 15 | 14 | 13 | 12 | 11 | 10 | 9   | 8       | 7 | 6 | 5   | 4       | 3 | 2 | 1 | 0 |          |
| 0x004  |              |    |    | 0          |    |    |    |    | 0x0      |    |    |    |    |    |    | 0x00  |    |    |    |    |    |    | 0x0 |         |   |   | 0x0 |         |   |   |   |   | 0x0      |
| Reset  |              |    |    | 0          |    |    |    |    | 0x0      |    |    |    |    |    |    | 0x00  |    |    |    |    |    |    | 0x0 |         |   |   | 0x0 |         |   |   |   |   | 0x0      |
| Access |              |    |    | RW         |    |    |    |    | RW       |    |    |    |    |    |    | RW    |    |    |    |    |    |    | RW  |         |   |   | RW  |         |   |   |   |   | RW       |
| Name   |              |    |    | AUXSTARTUP |    |    |    |    | STARTDLY |    |    |    |    |    |    | PCTOP |    |    |    |    |    |    |     | PCPRESC |   |   |     | LFPRESC |   |   |   |   | AUXPRESC |

| Bit   | Name       | Reset   | Access | Description   |       |      |             |   |           |  |   |          |  |   |      |  |   |      |  |   |       |   |   |       |   |
|-------|------------|---|--------|---|-------|------|-------------|---|-----------|--|---|----------|--|---|------|--|---|------|--|---|-------|---|---|-------|---|
| 31:29 | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |      |             |   |           |  |   |          |  |   |      |  |   |      |  |   |       |   |   |       |   |
| 28    | AUXSTARTUP | 0   | RW     | <b>AUXHFRCO Startup Configuration</b><br>This bit can be set to ONDEMAND to delay startup of the AUXHFRCO when high frequency timer is used<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>PREDEMAND</td> <td>AUXHFRCO is started half a clock cycle before it's needed</td> </tr> <tr> <td>1</td> <td>ONDEMAND</td> <td>AUXHFRCO is started at the time it is needed</td> </tr> </tbody> </table>   | Value | Mode | Description | 0 | PREDEMAND | AUXHFRCO is started half a clock cycle before it's needed          | 1 | ONDEMAND | AUXHFRCO is started at the time it is needed                       |   |      |  |   |      |  |   |       |   |   |       |   |
| Value | Mode       | Description   |        |   |       |      |             |   |           |  |   |          |  |   |      |  |   |      |  |   |       |   |   |       |   |
| 0     | PREDEMAND  | AUXHFRCO is started half a clock cycle before it's needed   |        |   |       |      |             |   |           |  |   |          |  |   |      |  |   |      |  |   |       |   |   |       |   |
| 1     | ONDEMAND   | AUXHFRCO is started at the time it is needed  |        |   |       |      |             |   |           |  |   |          |  |   |      |  |   |      |  |   |       |   |   |       |   |
| 27:24 | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |      |             |   |           |  |   |          |  |   |      |  |   |      |  |   |       |   |   |       |   |
| 23:22 | STARTDLY   | 0x0   | RW     | <b>Start Delay Configuration</b><br>Delay sensor interaction STARTDELAY LFACLK <sub>LESENSE</sub> cycles for each channel   |       |      |             |   |           |  |   |          |  |   |      |  |   |      |  |   |       |   |   |       |   |
| 21:20 | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |      |             |   |           |  |   |          |  |   |      |  |   |      |  |   |       |   |   |       |   |
| 19:12 | PCTOP      | 0x00  | RW     | <b>Period Counter Top Value</b><br>These bits contain the top value for the period counter.   |       |      |             |   |           |  |   |          |  |   |      |  |   |      |  |   |       |   |   |       |   |
| 11    | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |      |             |   |           |  |   |          |  |   |      |  |   |      |  |   |       |   |   |       |   |
| 10:8  | PCPRESC    | 0x0   | RW     | <b>Period Counter Prescaling</b><br>This bitfield is used to divide the clock to the period counter<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>DIV1</td> <td>The period counter clock frequency is LFACLK<sub>LESENSE</sub>/1</td> </tr> <tr> <td>1</td> <td>DIV2</td> <td>The period counter clock frequency is LFACLK<sub>LESENSE</sub>/2</td> </tr> <tr> <td>2</td> <td>DIV4</td> <td>The period counter clock frequency is LFACLK<sub>LESENSE</sub>/4</td> </tr> <tr> <td>3</td> <td>DIV8</td> <td>The period counter clock frequency is LFACLK<sub>LESENSE</sub>/8</td> </tr> <tr> <td>4</td> <td>DIV16</td> <td>The period counter clock frequency is LFACLK<sub>LESENSE</sub>/16</td> </tr> <tr> <td>5</td> <td>DIV32</td> <td>The period counter clock frequency is LFACLK<sub>LESENSE</sub>/32</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | DIV1      | The period counter clock frequency is LFACLK <sub>LESENSE</sub> /1 | 1 | DIV2     | The period counter clock frequency is LFACLK <sub>LESENSE</sub> /2 | 2 | DIV4 | The period counter clock frequency is LFACLK <sub>LESENSE</sub> /4 | 3 | DIV8 | The period counter clock frequency is LFACLK <sub>LESENSE</sub> /8 | 4 | DIV16 | The period counter clock frequency is LFACLK <sub>LESENSE</sub> /16 | 5 | DIV32 | The period counter clock frequency is LFACLK <sub>LESENSE</sub> /32 |
| Value | Mode       | Description   |        |   |       |      |             |   |           |  |   |          |  |   |      |  |   |      |  |   |       |   |   |       |   |
| 0     | DIV1       | The period counter clock frequency is LFACLK <sub>LESENSE</sub> /1  |        |   |       |      |             |   |           |  |   |          |  |   |      |  |   |      |  |   |       |   |   |       |   |
| 1     | DIV2       | The period counter clock frequency is LFACLK <sub>LESENSE</sub> /2  |        |   |       |      |             |   |           |  |   |          |  |   |      |  |   |      |  |   |       |   |   |       |   |
| 2     | DIV4       | The period counter clock frequency is LFACLK <sub>LESENSE</sub> /4  |        |   |       |      |             |   |           |  |   |          |  |   |      |  |   |      |  |   |       |   |   |       |   |
| 3     | DIV8       | The period counter clock frequency is LFACLK <sub>LESENSE</sub> /8  |        |   |       |      |             |   |           |  |   |          |  |   |      |  |   |      |  |   |       |   |   |       |   |
| 4     | DIV16      | The period counter clock frequency is LFACLK <sub>LESENSE</sub> /16   |        |   |       |      |             |   |           |  |   |          |  |   |      |  |   |      |  |   |       |   |   |       |   |
| 5     | DIV32      | The period counter clock frequency is LFACLK <sub>LESENSE</sub> /32   |        |   |       |      |             |   |           |  |   |          |  |   |      |  |   |      |  |   |       |   |   |       |   |

| Bit | Name            | Reset   | Access   | Description  |
|-----|-----------------|---|--|--|
|     | 6               | DIV64   |  | The period counter clock frequency is $LFACTK_{LESENSE}/64$  |
|     | 7               | DIV128  |  | The period counter clock frequency is $LFACTK_{LESENSE}/128$   |
| 7   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |  |
| 6:4 | LFPRESC         | 0x0   | RW   | <b>Prescaling Factor for Low Frequency Timer</b><br>This bitfield is used to divide the clock to the low frequency timer   |
|     | Value           | Mode  | Description  |  |
|     | 0               | DIV1  | Low frequency timer is clocked with $LFACTK_{LESENSE}/1$   |  |
|     | 1               | DIV2  | Low frequency timer is clocked with $LFACTK_{LESENSE}/2$   |  |
|     | 2               | DIV4  | Low frequency timer is clocked with $LFACTK_{LESENSE}/4$   |  |
|     | 3               | DIV8  | Low frequency timer is clocked with $LFACTK_{LESENSE}/8$   |  |
|     | 4               | DIV16   | Low frequency timer is clocked with $LFACTK_{LESENSE}/16$  |  |
|     | 5               | DIV32   | Low frequency timer is clocked with $LFACTK_{LESENSE}/32$  |  |
|     | 6               | DIV64   | Low frequency timer is clocked with $LFACTK_{LESENSE}/64$  |  |
|     | 7               | DIV128  | Low frequency timer is clocked with $LFACTK_{LESENSE}/128$ |  |
| 3:2 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |  |
| 1:0 | AUXPRESC        | 0x0   | RW   | <b>Prescaling Factor for High Frequency Timer</b><br>This bitfield is used to divide the clock to the high frequency timer |
|     | Value           | Mode  | Description  |  |
|     | 0               | DIV1  | High frequency timer is clocked with $AUXHFRCO/1$          |  |
|     | 1               | DIV2  | High frequency timer is clocked with $AUXHFRCO/2$          |  |
|     | 2               | DIV4  | High frequency timer is clocked with $AUXHFRCO/4$          |  |
|     | 3               | DIV8  | High frequency timer is clocked with $AUXHFRCO/8$          |  |

### 29.5.3 LESENSE\_PERCTRL - Peripheral Control Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |            |    |             |             |          |          |           |    |           |    |    |    |    |    |    |    |    |    |    |    |   |             |   |            |   |   |            |            |          |          |
|---------------|--------------|----|------------|----|-------------|-------------|----------|----------|-----------|----|-----------|----|----|----|----|----|----|----|----|----|----|----|---|-------------|---|------------|---|---|------------|------------|----------|----------|
|               | 31           | 30 | 29         | 28 | 27          | 26          | 25       | 24       | 23        | 22 | 21        | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8           | 7 | 6          | 5 | 4 | 3          | 2          | 1        | 0        |
| 0x008         |              |    | 0x0        |    | 0           | 0           | 0        | 0        | 0x0       |    | 0x0       |    |    |    |    |    |    |    |    |    |    |    |   | 0           |   | 0          |   |   | 0          | 0          | 0        | 0        |
| <b>Reset</b>  |              |    | 0x0        |    | 0           | 0           | 0        | 0        | 0x0       |    | 0x0       |    |    |    |    |    |    |    |    |    |    |    |   | 0           |   | 0          |   |   | 0          | 0          | 0        | 0        |
| <b>Access</b> |              |    | RW         |    | RW          | RW          | RW       | RW       | RW        |    | RW        |    |    |    |    |    |    |    |    |    |    |    |   | RW          |   | RW         |   |   | RW         | RW         | RW       | RW       |
| <b>Name</b>   |              |    | WARMUPMODE |    | ACMP1HYSTEN | ACMP0HYSTEN | ACMP1INV | ACMP0INV | ACMP1MODE |    | ACMP0MODE |    |    |    |    |    |    |    |    |    |    |    |   | DACCONVTRIG |   | DACSTARTUP |   |   | DACCH1DATA | DACCH0DATA | DACCH1EN | DACCH0EN |

| Bit   | Name            | Reset  | Access | Description  |       |      |             |   |         |  |   |              |   |   |             |  |   |                 |  |
|-------|-----------------|--|--------|--|-------|------|-------------|---|---------|--|---|--------------|---|---|-------------|--|---|-----------------|--|
| 31:30 | Reserved        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |       |      |             |   |         |  |   |              |   |   |             |  |   |                 |  |
| 29:28 | WARMUPMODE      | 0x0  | RW     | <b>ACMP and VDAC Duty Cycle Mode</b><br>This bitfield is used to configure how the VDAC and ACMP are duty cycled when LESENSE is controlling them<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>NORMAL</td> <td>The analog comparators and VDAC are shut down when LESENSE is idle</td> </tr> <tr> <td>1</td> <td>KEEPACMPWARM</td> <td>The analog comparators are kept powered up when LESENSE is idle</td> </tr> <tr> <td>2</td> <td>KEEPDACWARM</td> <td>The VDAC is kept powered up when LESENSE is idle</td> </tr> <tr> <td>3</td> <td>KEEPACMPDACWARM</td> <td>The analog comparators and VDAC are kept powered up when LESENSE is idle</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | NORMAL  | The analog comparators and VDAC are shut down when LESENSE is idle | 1 | KEEPACMPWARM | The analog comparators are kept powered up when LESENSE is idle | 2 | KEEPDACWARM | The VDAC is kept powered up when LESENSE is idle                           | 3 | KEEPACMPDACWARM | The analog comparators and VDAC are kept powered up when LESENSE is idle |
| Value | Mode            | Description  |        |  |       |      |             |   |         |  |   |              |   |   |             |  |   |                 |  |
| 0     | NORMAL          | The analog comparators and VDAC are shut down when LESENSE is idle   |        |  |       |      |             |   |         |  |   |              |   |   |             |  |   |                 |  |
| 1     | KEEPACMPWARM    | The analog comparators are kept powered up when LESENSE is idle  |        |  |       |      |             |   |         |  |   |              |   |   |             |  |   |                 |  |
| 2     | KEEPDACWARM     | The VDAC is kept powered up when LESENSE is idle   |        |  |       |      |             |   |         |  |   |              |   |   |             |  |   |                 |  |
| 3     | KEEPACMPDACWARM | The analog comparators and VDAC are kept powered up when LESENSE is idle   |        |  |       |      |             |   |         |  |   |              |   |   |             |  |   |                 |  |
| 27    | ACMP1HYSTEN     | 0  | RW     | <b>ACMP1 Hysteresis Enable</b><br>Set to control ACMP1_HYSTERESIS0_DIVVX and ACMP1_HYSTERESIS1_DIVVX separately.   |       |      |             |   |         |  |   |              |   |   |             |  |   |                 |  |
| 26    | ACMP0HYSTEN     | 0  | RW     | <b>ACMP0 Hysteresis Enable</b><br>Set to control ACMP0_HYSTERESIS0_DIVVX and ACMP0_HYSTERESIS1_DIVVX separately.   |       |      |             |   |         |  |   |              |   |   |             |  |   |                 |  |
| 25    | ACMP1INV        | 0  | RW     | <b>Invert Analog Comparator 1 Output</b><br>This bit can be set to invert the output coming from ACMP1   |       |      |             |   |         |  |   |              |   |   |             |  |   |                 |  |
| 24    | ACMP0INV        | 0  | RW     | <b>Invert Analog Comparator 0 Output</b><br>This bit can be set to invert the output coming from ACMP0   |       |      |             |   |         |  |   |              |   |   |             |  |   |                 |  |
| 23:22 | ACMP1MODE       | 0x0  | RW     | <b>ACMP1 Mode</b><br>Configure how LESENSE controls ACMP1<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>DISABLE</td> <td>LESENSE does not control ACMP1</td> </tr> <tr> <td>1</td> <td>MUX</td> <td>LESENSE controls the input mux (POSSEL) of ACMP1</td> </tr> <tr> <td>2</td> <td>MUXTHRES</td> <td>LESENSE controls the input mux and the threshold value (VDDLEVEL) of ACMP1</td> </tr> </tbody> </table>  | Value | Mode | Description | 0 | DISABLE | LESENSE does not control ACMP1                                     | 1 | MUX          | LESENSE controls the input mux (POSSEL) of ACMP1                | 2 | MUXTHRES    | LESENSE controls the input mux and the threshold value (VDDLEVEL) of ACMP1 |   |                 |  |
| Value | Mode            | Description  |        |  |       |      |             |   |         |  |   |              |   |   |             |  |   |                 |  |
| 0     | DISABLE         | LESENSE does not control ACMP1   |        |  |       |      |             |   |         |  |   |              |   |   |             |  |   |                 |  |
| 1     | MUX             | LESENSE controls the input mux (POSSEL) of ACMP1   |        |  |       |      |             |   |         |  |   |              |   |   |             |  |   |                 |  |
| 2     | MUXTHRES        | LESENSE controls the input mux and the threshold value (VDDLEVEL) of ACMP1   |        |  |       |      |             |   |         |  |   |              |   |   |             |  |   |                 |  |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 21:20 | ACMP0MODE       | 0x0   | RW     | <b>ACMP0 Mode</b><br>Configure how LESENSE controls ACMP0  |
|       | Value           | Mode  |        | Description  |
|       | 0               | DISABLE   |        | LESENSE does not control ACMP0   |
|       | 1               | MUX   |        | LESENSE controls the input mux (POSSEL) of ACMP0   |
|       | 2               | MUXTHRES  |        | LESENSE controls the input mux (POSSEL) and the threshold value (VDDLEVEL) of ACMP0  |
| 19:9  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 8     | DACCONVTRIG     | 0   | RW     | <b>VDAC Conversion Trigger Configuration</b><br>This bit is used to configure how frequently a VDAC conversion is triggered                    |
|       | Value           | Mode  |        | Description  |
|       | 0               | CHANNELSTART  |        | VDAC is enabled before every LESENSE channel measurement.  |
|       | 1               | SCANSTART   |        | VDAC is only enabled once per scan.  |
| 7     | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 6     | DACSTARTUP      | 0   | RW     | <b>VDAC Startup Configuration</b><br>This bit is used to configure the duration between the VDAC conversion trigger and the sensor interaction |
|       | Value           | Mode  |        | Description  |
|       | 0               | FULLCYCLE   |        | VDAC is started a full LFACTK <sub>LESENSE</sub> cycle before sensor interaction starts.   |
|       | 1               | HALFCYCLE   |        | VDAC is started half a LFACTK <sub>LESENSE</sub> cycle before sensor interaction starts.   |
| 5:4   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 3     | DACCH1DATA      | 0   | RW     | <b>VDAC CH1 Data Selection</b><br>This bit decides if the data used for VDAC conversion is taken from the VDAC interface or from LESENSE       |
|       | Value           | Mode  |        | Description  |
|       | 0               | DACDATA   |        | VDAC data is defined by CH1DATA in the VDAC interface.   |
|       | 1               | THRES   |        | VDAC data is defined by THRES in CH <sub>x</sub> _INTERACT.  |
| 2     | DACCH0DATA      | 0   | RW     | <b>VDAC CH0 Data Selection</b><br>This bit decides if the data used for VDAC conversion is taken from the VDAC interface or from LESENSE       |
|       | Value           | Mode  |        | Description  |
|       | 0               | DACDATA   |        | VDAC data is defined by CH0DATA in the VDAC interface.   |
|       | 1               | THRES   |        | VDAC data is defined by THRES in CH <sub>x</sub> _INTERACT.  |

| Bit | Name     | Reset | Access | Description  |
|-----|----------|-------|--------|--|
| 1   | DACCH1EN | 0     | RW     | <b>VDAC CH1 Enable</b><br>Enable LESENSE control of VDACC0 CH1 |
| 0   | DACCH0EN | 0     | RW     | <b>VDAC CH0 Enable</b><br>Enable LESENSE control of VDACC0 CH0 |

### 29.5.4 LESENSE\_DECCTRL - Decoder Control Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |        |    |    |    |    |        |    |    |    |    |        |    |    |    |    |    |        |    |   |       |        |         |          |          |          |        |        |         |    |   |
|---------------|--------------|----|----|----|--------|----|----|----|----|--------|----|----|----|----|--------|----|----|----|----|----|--------|----|---|-------|--------|---------|----------|----------|----------|--------|--------|---------|----|---|
|               | 31           | 30 | 29 | 28 | 27     | 26 | 25 | 24 | 23 | 22     | 21 | 20 | 19 | 18 | 17     | 16 | 15 | 14 | 13 | 12 | 11     | 10 | 9 | 8     | 7      | 6       | 5        | 4        | 3        | 2      | 1      | 0       |    |   |
| 0x00C         |              |    |    |    |        |    |    |    |    |        |    |    |    |    |        |    |    |    |    |    |        |    |   |       |        |         |          |          |          |        |        |         |    |   |
| <b>Reset</b>  |              |    |    |    | 0x0    |    |    |    |    | 0x0    |    |    |    |    | 0x0    |    |    |    |    |    | 0x0    |    |   |       | 0      | 0       | 0        | 0        | 0        | 0      | 0      | 0       | 0  | 0 |
| <b>Access</b> |              |    |    |    | RW     |    |    |    |    | RW     |    |    |    |    | RW     |    |    |    |    |    | RW     |    |   | RW    | RW     | RW      | RW       | RW       | RW       | RW     | RW     | RW      | RW |   |
| <b>Name</b>   |              |    |    |    | PRSEL3 |    |    |    |    | PRSEL2 |    |    |    |    | PRSEL1 |    |    |    |    |    | PRSEL0 |    |   | INPUT | PRSCNT | HYSTIRQ | HYSTPRS2 | HYSTPRS1 | HYSTPRS0 | INTMAP | ERRCHK | DISABLE |    |   |

| Bit   | Name            | Reset   | Access                           | Description   |
|-------|-----------------|---|----------------------------------|---|
| 31:29 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                  |   |
| 28:25 | PRSEL3          | 0x0   | RW                               | <b>LESENSE Decoder PRS Input 3 Configuration</b><br>Select PRS input for bit 3 of the LESENSE decoder |
|       | Value           | Mode  | Description                      |   |
|       | 0               | PRSCH0  | PRS Channel 0 selected as input  |   |
|       | 1               | PRSCH1  | PRS Channel 1 selected as input  |   |
|       | 2               | PRSCH2  | PRS Channel 2 selected as input  |   |
|       | 3               | PRSCH3  | PRS Channel 3 selected as input  |   |
|       | 4               | PRSCH4  | PRS Channel 4 selected as input  |   |
|       | 5               | PRSCH5  | PRS Channel 5 selected as input  |   |
|       | 6               | PRSCH6  | PRS Channel 6 selected as input  |   |
|       | 7               | PRSCH7  | PRS Channel 7 selected as input  |   |
|       | 8               | PRSCH8  | PRS Channel 8 selected as input  |   |
|       | 9               | PRSCH9  | PRS Channel 9 selected as input  |   |
|       | 10              | PRSCH10   | PRS Channel 10 selected as input |   |
|       | 11              | PRSCH11   | PRS Channel 11 selected as input |   |
| 24    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                  |   |
| 23:20 | PRSEL2          | 0x0   | RW                               | <b>LESENSE Decoder PRS Input 2 Configuration</b><br>Select PRS input for bit 2 of the LESENSE decoder |
|       | Value           | Mode  | Description                      |   |
|       | 0               | PRSCH0  | PRS Channel 0 selected as input  |   |
|       | 1               | PRSCH1  | PRS Channel 1 selected as input  |   |
|       | 2               | PRSCH2  | PRS Channel 2 selected as input  |   |
|       | 3               | PRSCH3  | PRS Channel 3 selected as input  |   |
|       | 4               | PRSCH4  | PRS Channel 4 selected as input  |   |

| Bit | Name | Reset   | Access | Description                      |
|-----|------|---------|--------|----------------------------------|
|     | 5    | PRSCH5  |        | PRS Channel 5 selected as input  |
|     | 6    | PRSCH6  |        | PRS Channel 6 selected as input  |
|     | 7    | PRSCH7  |        | PRS Channel 7 selected as input  |
|     | 8    | PRSCH8  |        | PRS Channel 8 selected as input  |
|     | 9    | PRSCH9  |        | PRS Channel 9 selected as input  |
|     | 10   | PRSCH10 |        | PRS Channel 10 selected as input |
|     | 11   | PRSCH11 |        | PRS Channel 11 selected as input |

19 *Reserved* *To ensure compatibility with future devices, always write bits to 0. More information in [1.2 Conventions](#)*

18:15 PRSSEL1 0x0 RW **LESENSE Decoder PRS Input 1 Configuration**

Select PRS input for the bit 1 of the LESENSE decoder

| Value | Mode    | Description                      |
|-------|---------|----------------------------------|
| 0     | PRSCH0  | PRS Channel 0 selected as input  |
| 1     | PRSCH1  | PRS Channel 1 selected as input  |
| 2     | PRSCH2  | PRS Channel 2 selected as input  |
| 3     | PRSCH3  | PRS Channel 3 selected as input  |
| 4     | PRSCH4  | PRS Channel 4 selected as input  |
| 5     | PRSCH5  | PRS Channel 5 selected as input  |
| 6     | PRSCH6  | PRS Channel 6 selected as input  |
| 7     | PRSCH7  | PRS Channel 7 selected as input  |
| 8     | PRSCH8  | PRS Channel 8 selected as input  |
| 9     | PRSCH9  | PRS Channel 9 selected as input  |
| 10    | PRSCH10 | PRS Channel 10 selected as input |
| 11    | PRSCH11 | PRS Channel 11 selected as input |

14 *Reserved* *To ensure compatibility with future devices, always write bits to 0. More information in [1.2 Conventions](#)*

13:10 PRSSEL0 0x0 RW **LESENSE Decoder PRS Input 0 Configuration**

Select PRS input for the bit 0 of the LESENSE decoder

| Value | Mode   | Description                     |
|-------|--------|---------------------------------|
| 0     | PRSCH0 | PRS Channel 0 selected as input |
| 1     | PRSCH1 | PRS Channel 1 selected as input |
| 2     | PRSCH2 | PRS Channel 2 selected as input |
| 3     | PRSCH3 | PRS Channel 3 selected as input |
| 4     | PRSCH4 | PRS Channel 4 selected as input |
| 5     | PRSCH5 | PRS Channel 5 selected as input |
| 6     | PRSCH6 | PRS Channel 6 selected as input |
| 7     | PRSCH7 | PRS Channel 7 selected as input |

| Bit | Name            | Reset   | Access | Description   |
|-----|-----------------|---|--------|---|
|     | 8               | PRSCH8  |        | PRS Channel 8 selected as input   |
|     | 9               | PRSCH9  |        | PRS Channel 9 selected as input   |
|     | 10              | PRSCH10   |        | PRS Channel 10 selected as input  |
|     | 11              | PRSCH11   |        | PRS Channel 11 selected as input  |
| 9   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 8   | INPUT           | 0   | RW     | <b>LESENSE Decoder Input Configuration</b><br>Select input to the LESENSE decoder   |
|     | Value           | Mode  |        | Description   |
|     | 0               | SENSORSTATE   |        | The SENSORSTATE register is used as input to the decoder.   |
|     | 1               | PRS   |        | PRS channels are used as input to the decoder.  |
| 7   | PRSCNT          | 0   | RW     | <b>Enable Count Mode on Decoder PRS Channels 0 and 1</b><br>When set, decoder PRS0 and PRS1 will be used to produce output which can be used by a PCNT to count up or down. |
| 6   | HYSTIRQ         | 0   | RW     | <b>Enable Decoder Hysteresis on Interrupt Requests</b><br>When set, hysteresis is enabled in the decoder, suppressing interrupt requests.                                   |
| 5   | HYSTPRS2        | 0   | RW     | <b>Enable Decoder Hysteresis on PRS2 Output</b><br>When set, hysteresis is enabled in the decoder, suppressing changes on PRS channel 2                                     |
| 4   | HYSTPRS1        | 0   | RW     | <b>Enable Decoder Hysteresis on PRS1 Output</b><br>When set, hysteresis is enabled in the decoder, suppressing changes on PRS channel 1                                     |
| 3   | HYSTPRS0        | 0   | RW     | <b>Enable Decoder Hysteresis on PRS0 Output</b><br>When set, hysteresis is enabled in the decoder, suppressing changes on PRS channel 0                                     |
| 2   | INTMAP          | 0   | RW     | <b>Enable Decoder to Channel Interrupt Mapping</b><br>When set, a transition from state x in the decoder will set interrupt flag CH[x mod 16]                               |
| 1   | ERRCHK          | 0   | RW     | <b>Enable Check of Current State</b><br>When set, the decoder checks the current state in addition to the states defined in TCONF   |
| 0   | DISABLE         | 0   | RW     | <b>Disable the Decoder</b><br>When set, the decoder is disabled. When disabled the decoder will keep its current state  |

### 29.5.5 LESENSE\_BIASCTRL - Bias Control Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |          |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|----------|
| 0x010         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0        |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0x0      |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | RW       |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | BIASMODE |

| Bit  | Name     | Reset  | Access | Description  |
|------|----------|--|--------|--|
| 31:2 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 1:0  | BIASMODE | 0x0  | RW     | <b>Select Bias Mode</b><br>This bitfield is used to configure how LESENSE interacts with the bias module |
|      | Value    | Mode   |        | Description  |
|      | 0        | DONTTOUCH  |        | Bias module is controlled by the EMU and is not affected by LESENSE                                      |
|      | 1        | DUTYCYCLE  |        | Bias module duty cycled between low power and high accuracy mode   |
|      | 2        | HIGHACC  |        | Bias module always in high accuracy mode   |

### 29.5.6 LESENSE\_EVALCTRL - LESENSE Evaluation Control (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x014         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | WINSIZE |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description  |
|-------|----------|--|--------|--|
| 31:16 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 15:0  | WINSIZE  | 0x0000   | RW     | <b>Sliding Window and Step Detection Size</b><br>In sliding window mode, this bitfield configures the window size. In step detection mode, this bitfield is used to configure the threshold for step detection |

### 29.5.7 LESENSE\_PRCTRL - PRS Control Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |    |    |    |    |    |   |            |   |   |   |   |   |   |   |   |  |           |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|----|----|---|------------|---|---|---|---|---|---|---|---|--|-----------|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8          | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |           |  |
| 0x018         |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |    |    |    |    |    |   |            |   |   |   |   |   |   |   |   |  |           |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0        |    |    |    |    |    |   | 0x00       |   |   |   |   |   |   |   |   |  | 0x00      |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW       |    |    |    |    |    |   | RW         |   |   |   |   |   |   |   |   |  | RW        |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DECCMPEN |    |    |    |    |    |   | DECCMPMASK |   |   |   |   |   |   |   |   |  | DECCMPVAL |  |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 31:17 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 16    | DECCMPEN        | 0   | RW     | <b>Enable PRS Output DECCMP</b><br>Enables decoder state compare match PRS output      |
| 15:13 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 12:8  | DECCMPMASK      | 0x00  | RW     | <b>Decoder State Compare Value Mask</b><br>Masks DECCMPVAL and DECSTATE for comparison |
| 7:5   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 4:0   | DECCMPVAL       | 0x00  | RW     | <b>Decoder State Compare Value</b><br>Triggers PRS output when equal to DECSTATE       |



### 29.5.10 LESENSE\_SCANRES - Scan Result Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| 0x024         |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| <b>Reset</b>  | 0x0000       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| <b>Access</b> | RWH          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| <b>Name</b>   | STEPDIR      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | SCANRES |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |

| Bit   | Name    | Reset  | Access | Description   |
|-------|---------|--------|--------|---|
| 31:16 | STEPDIR | 0x0000 | RWH    | <b>Direction of Previous Step Detection</b><br>In step detection mode, bit X will be set if a step up was detected on channel X |
| 15:0  | SCANRES | 0x0000 | RWH    | <b>Scan Results</b><br>Bit X will be set depending on channel X evaluation  |

### 29.5.11 LESENSE\_STATUS - Status Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |           |            |         |         |             |          |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|-----------|------------|---------|---------|-------------|----------|---|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4         | 3          | 2       | 1       | 0           |          |   |
| 0x028         |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |           |            |         |         |             |          |   |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | 0         | 0          | 0       | 0       | 0           | 0        | 0 |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | R         | R          | R       | R       | R           | R        | R |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | DACACTIVE | SCANACTIVE | RUNNING | BUFFULL | BUFHALFFULL | BUFDATAV |   |

| Bit  | Name            | Reset   | Access | Description  |
|------|-----------------|---|--------|--|
| 31:6 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 5    | DACACTIVE       | 0   | R      | <b>LESENSE VDAC Interface is Active</b><br>LESENSE is currently using the VDAC.                                |
| 4    | SCANACTIVE      | 0   | R      | <b>LESENSE Scan Active</b><br>LESENSE is currently interfacing to sensors.                                     |
| 3    | RUNNING         | 0   | R      | <b>LESENSE Periodic Counter Running</b><br>LESENSE is running in periodic mode.                                |
| 2    | BUFFULL         | 0   | R      | <b>Result Buffer Full</b><br>Set when the result buffer is full  |
| 1    | BUFHALFFULL     | 0   | R      | <b>Result Buffer Half Full</b><br>Set when the result buffer is half full                                      |
| 0    | BUFDATAV        | 0   | R      | <b>Result Data Valid</b><br>Set when data is available in the result buffer. Cleared when the buffer is empty. |

**29.5.12 LESENSE\_PTR - Result Buffer Pointers (Async Reg)**

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |     |   |   |   |     |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|-----|---|---|---|-----|---|---|---|
| 0x02C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7   | 6 | 5 | 4 | 3   | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x0 |   |   |   | 0x0 |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | R   |   |   |   | R   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | WR  |   |   |   | RD  |   |   |   |

| Bit  | Name     | Reset   | Access | Description  |
|------|----------|---|--------|--|
| 31:8 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 7:4  | WR       | 0x0   | R      | <b>Result Buffer Write Pointer</b><br>These bits show the next index in the result buffer to be written to. Incremented when LESENSE writes to result buffer |
| 3:0  | RD       | 0x0   | R      | <b>Result Buffer Read Pointer</b><br>These bits show the index of the oldest unread data in the result buffer. Incremented on read from BUFDATA.             |

**29.5.13 LESENSE\_BUFDATA - Result Buffer Data Register (Async Reg) (Actionable Reads)**

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |         |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|---------|----|---|---|---|---|---|---|---|---|---|---|
| 0x030         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11      | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0xX        |    |    |    | 0XXXXX  |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R          |    |    |    | R       |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | BUFDATASRC |    |    |    | BUFDATA |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name       | Reset   | Access | Description   |
|-------|------------|---|--------|---|
| 31:20 | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 19:16 | BUFDATASRC | 0xX   | R      | <b>Result Data Source</b><br>This bitfield contains the channel index for the sensor result in BUFDATA. |
| 15:0  | BUFDATA    | 0XXXXX  | R      | <b>Result Data</b><br>This register can be used to read the oldest unread data from the result buffer.  |

**29.5.14 LESENSE\_CURCH - Current Channel Index (Async Reg)**

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0x034         |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

| Bit  | Name     | Reset   | Access | Description  |
|------|----------|---|--------|--|
| 31:4 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 3:0  | CURCH    | 0x0   | R      | <b>Current Channel Index</b><br>Shows the index of the current channel |

**29.5.15 LESENSE\_DECSTATE - Current Decoder State (Async Reg)**

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0x038         |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

| Bit  | Name     | Reset   | Access | Description   |
|------|----------|---|--------|---|
| 31:5 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 4:0  | DECSTATE | 0x00  | RWH    | <b>Current Decoder State</b><br>Shows the current decoder state |

### 29.5.16 LESENSE\_SENSORSTATE - Decoder Input Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |             |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|-------------|---|---|---|
| 0x03C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3           | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0x0         | 0 |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | RWH         | 0 |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | SENSORSTATE | 0 |   |   |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 31:4 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 3:0  | SENSORSTATE     | 0x0   | RWH    | <b>Decoder Input Register</b><br>Shows the status of sensors chosen as input to the decoder |

**29.5.17 LESENSE\_IDLECONF - GPIO Idle Phase Configuration (Async Reg)**For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |      |      |      |      |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|---------------|--------------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0x040         | 31           | 30   | 29   | 28   | 27   | 26   | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| <b>Reset</b>  | 0x0          | 0x0  | 0x0  | 0x0  | 0x0  | 0x0  | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 |
| <b>Access</b> | RW           | RW   | RW   | RW   | RW   | RW   | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  |
| <b>Name</b>   | CH15         | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

| Bit   | Name  | Reset   | Access | Description  |
|-------|-------|---------|--------|--|
| 31:30 | CH15  | 0x0     | RW     | <b>Channel 15 Idle Phase Configuration</b><br>This bitfield determines how the channel is configured during the idle phase   |
|       | Value | Mode    |        | Description  |
|       | 0     | DISABLE |        | CH15 output is disabled in idle phase  |
|       | 1     | HIGH    |        | CH15 output is high in idle phase  |
|       | 2     | LOW     |        | CH15 output is low in idle phase   |
|       | 3     | DAC     |        | CH15 output is connected to VDAC output in idle phase. Note that this mode is only available on channels 4, 5, 7, 10, 12, 13 |
| 29:28 | CH14  | 0x0     | RW     | <b>Channel 14 Idle Phase Configuration</b><br>This bitfield determines how the channel is configured during the idle phase   |
|       | Value | Mode    |        | Description  |
|       | 0     | DISABLE |        | CH14 output is disabled in idle phase  |
|       | 1     | HIGH    |        | CH14 output is high in idle phase  |
|       | 2     | LOW     |        | CH14 output is low in idle phase   |
|       | 3     | DAC     |        | CH14 output is connected to VDAC output in idle phase. Note that this mode is only available on channels 4, 5, 7, 10, 12, 13 |
| 27:26 | CH13  | 0x0     | RW     | <b>Channel 13 Idle Phase Configuration</b><br>This bitfield determines how the channel is configured during the idle phase   |
|       | Value | Mode    |        | Description  |
|       | 0     | DISABLE |        | CH13 output is disabled in idle phase  |
|       | 1     | HIGH    |        | CH13 output is high in idle phase  |
|       | 2     | LOW     |        | CH13 output is low in idle phase   |
|       | 3     | DAC     |        | CH13 output is connected to VDAC output in idle phase. Note that this mode is only available on channels 4, 5, 7, 10, 12, 13 |
| 25:24 | CH12  | 0x0     | RW     | <b>Channel 12 Idle Phase Configuration</b><br>This bitfield determines how the channel is configured during the idle phase   |
|       | Value | Mode    |        | Description  |

| Bit   | Name  | Reset   | Access | Description  |
|-------|-------|---------|--------|--|
|       | 0     | DISABLE |        | CH12 output is disabled in idle phase  |
|       | 1     | HIGH    |        | CH12 output is high in idle phase  |
|       | 2     | LOW     |        | CH12 output is low in idle phase   |
|       | 3     | DAC     |        | CH12 output is connected to VDAC output in idle phase. Note that this mode is only available on channels 4, 5, 7, 10, 12, 13 |
| 23:22 | CH11  | 0x0     | RW     | <b>Channel 11 Idle Phase Configuration</b><br>This bitfield determines how the channel is configured during the idle phase   |
|       | Value | Mode    |        | Description  |
|       | 0     | DISABLE |        | CH11 output is disabled in idle phase  |
|       | 1     | HIGH    |        | CH11 output is high in idle phase  |
|       | 2     | LOW     |        | CH11 output is low in idle phase   |
|       | 3     | DAC     |        | CH11 output is connected to VDAC output in idle phase. Note that this mode is only available on channels 4, 5, 7, 10, 12, 13 |
| 21:20 | CH10  | 0x0     | RW     | <b>Channel 10 Idle Phase Configuration</b><br>This bitfield determines how the channel is configured during the idle phase   |
|       | Value | Mode    |        | Description  |
|       | 0     | DISABLE |        | CH10 output is disabled in idle phase  |
|       | 1     | HIGH    |        | CH10 output is high in idle phase  |
|       | 2     | LOW     |        | CH10 output is low in idle phase   |
|       | 3     | DAC     |        | CH10 output is connected to VDAC output in idle phase. Note that this mode is only available on channels 4, 5, 7, 10, 12, 13 |
| 19:18 | CH9   | 0x0     | RW     | <b>Channel 9 Idle Phase Configuration</b><br>This bitfield determines how the channel is configured during the idle phase    |
|       | Value | Mode    |        | Description  |
|       | 0     | DISABLE |        | CH9 output is disabled in idle phase   |
|       | 1     | HIGH    |        | CH9 output is high in idle phase   |
|       | 2     | LOW     |        | CH9 output is low in idle phase  |
|       | 3     | DAC     |        | CH9 output is connected to VDAC output in idle phase. Note that this mode is only available on channels 4, 5, 7, 10, 12, 13  |
| 17:16 | CH8   | 0x0     | RW     | <b>Channel 8 Idle Phase Configuration</b><br>This bitfield determines how the channel is configured during the idle phase    |
|       | Value | Mode    |        | Description  |
|       | 0     | DISABLE |        | CH8 output is disabled in idle phase   |
|       | 1     | HIGH    |        | CH8 output is high in idle phase   |
|       | 2     | LOW     |        | CH8 output is low in idle phase  |
|       | 3     | DAC     |        | CH8 output is connected to VDAC output in idle phase. Note that this mode is only available on channels 4, 5, 7, 10, 12, 13  |

| Bit   | Name  | Reset   | Access | Description   |
|-------|-------|---------|--------|---|
| 15:14 | CH7   | 0x0     | RW     | <b>Channel 7 Idle Phase Configuration</b><br>This bitfield determines how the channel is configured during the idle phase   |
|       | Value | Mode    |        | Description   |
|       | 0     | DISABLE |        | CH7 output is disabled in idle phase  |
|       | 1     | HIGH    |        | CH7 output is high in idle phase  |
|       | 2     | LOW     |        | CH7 output is low in idle phase   |
|       | 3     | DAC     |        | CH7 output is connected to VDAC output in idle phase. Note that this mode is only available on channels 4, 5, 7, 10, 12, 13 |
| 13:12 | CH6   | 0x0     | RW     | <b>Channel 6 Idle Phase Configuration</b><br>This bitfield determines how the channel is configured during the idle phase   |
|       | Value | Mode    |        | Description   |
|       | 0     | DISABLE |        | CH6 output is disabled in idle phase  |
|       | 1     | HIGH    |        | CH6 output is high in idle phase  |
|       | 2     | LOW     |        | CH6 output is low in idle phase   |
|       | 3     | DAC     |        | CH6 output is connected to VDAC output in idle phase. Note that this mode is only available on channels 4, 5, 7, 10, 12, 13 |
| 11:10 | CH5   | 0x0     | RW     | <b>Channel 5 Idle Phase Configuration</b><br>This bitfield determines how the channel is configured during the idle phase   |
|       | Value | Mode    |        | Description   |
|       | 0     | DISABLE |        | CH5 output is disabled in idle phase  |
|       | 1     | HIGH    |        | CH5 output is high in idle phase  |
|       | 2     | LOW     |        | CH5 output is low in idle phase   |
|       | 3     | DAC     |        | CH5 output is connected to VDAC output in idle phase. Note that this mode is only available on channels 4, 5, 7, 10, 12, 13 |
| 9:8   | CH4   | 0x0     | RW     | <b>Channel 4 Idle Phase Configuration</b><br>This bitfield determines how the channel is configured during the idle phase   |
|       | Value | Mode    |        | Description   |
|       | 0     | DISABLE |        | CH4 output is disabled in idle phase  |
|       | 1     | HIGH    |        | CH4 output is high in idle phase  |
|       | 2     | LOW     |        | CH4 output is low in idle phase   |
|       | 3     | DAC     |        | CH4 output is connected to VDAC output in idle phase. Note that this mode is only available on channels 4, 5, 7, 10, 12, 13 |
| 7:6   | CH3   | 0x0     | RW     | <b>Channel 3 Idle Phase Configuration</b><br>This bitfield determines how the channel is configured during the idle phase   |
|       | Value | Mode    |        | Description   |
|       | 0     | DISABLE |        | CH3 output is disabled in idle phase  |

| Bit | Name  | Reset   | Access | Description   |
|-----|-------|---------|--------|---|
|     | 1     | HIGH    |        | CH3 output is high in idle phase  |
|     | 2     | LOW     |        | CH3 output is low in idle phase   |
|     | 3     | DAC     |        | CH3 output is connected to VDAC output in idle phase. Note that this mode is only available on channels 4, 5, 7, 10, 12, 13 |
| 5:4 | CH2   | 0x0     | RW     | <b>Channel 2 Idle Phase Configuration</b><br>This bitfield determines how the channel is configured during the idle phase   |
|     | Value | Mode    |        | Description   |
|     | 0     | DISABLE |        | CH2 output is disabled in idle phase  |
|     | 1     | HIGH    |        | CH2 output is high in idle phase  |
|     | 2     | LOW     |        | CH2 output is low in idle phase   |
|     | 3     | DAC     |        | CH2 output is connected to VDAC output in idle phase. Note that this mode is only available on channels 4, 5, 7, 10, 12, 13 |
| 3:2 | CH1   | 0x0     | RW     | <b>Channel 1 Idle Phase Configuration</b><br>This bitfield determines how the channel is configured during the idle phase   |
|     | Value | Mode    |        | Description   |
|     | 0     | DISABLE |        | CH1 output is disabled in idle phase  |
|     | 1     | HIGH    |        | CH1 output is high in idle phase  |
|     | 2     | LOW     |        | CH1 output is low in idle phase   |
|     | 3     | DAC     |        | CH1 output is connected to VDAC output in idle phase. Note that this mode is only available on channels 4, 5, 7, 10, 12, 13 |
| 1:0 | CH0   | 0x0     | RW     | <b>Channel 0 Idle Phase Configuration</b><br>This bitfield determines how the channel is configured during the idle phase   |
|     | Value | Mode    |        | Description   |
|     | 0     | DISABLE |        | CH0 output is disabled in idle phase  |
|     | 1     | HIGH    |        | CH0 output is high in idle phase  |
|     | 2     | LOW     |        | CH0 output is low in idle phase   |
|     | 3     | DAC     |        | CH0 output is connected to VDAC output in idle phase. Note that this mode is only available on channels 4, 5, 7, 10, 12, 13 |

**29.5.18 LESENSE\_ALTEXCONF - Alternative Excite Pin Configuration (Async Reg)**For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |      |      |      |      |      |      |      |      |           |           |           |           |           |           |           |           |     |     |     |     |     |     |     |     |
|---------------|--------------|----|----|----|----|----|----|----|------|------|------|------|------|------|------|------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----|-----|-----|-----|-----|-----|-----|-----|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23   | 22   | 21   | 20   | 19   | 18   | 17   | 16   | 15        | 14        | 13        | 12        | 11        | 10        | 9         | 8         | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| 0x044         |              |    |    |    |    |    |    |    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0x0       | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0x0       | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 |
| <b>Access</b> |              |    |    |    |    |    |    |    | RW        | RW        | RW        | RW        | RW        | RW        | RW        | RW        | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  |
| <b>Name</b>   |              |    |    |    |    |    |    |    | AEX7 | AEX6 | AEX5 | AEX4 | AEX3 | AEX2 | AEX1 | AEX0 | IDLECONF7 | IDLECONF6 | IDLECONF5 | IDLECONF4 | IDLECONF3 | IDLECONF2 | IDLECONF1 | IDLECONF0 |     |     |     |     |     |     |     |     |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:24 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 23    | AEX7            | 0   | RW     | <b>ALTEX7 Always Excite Enable</b><br>Set this bit to excite ALTEX7 regardless of what channel is active                            |
| 22    | AEX6            | 0   | RW     | <b>ALTEX6 Always Excite Enable</b><br>Set this bit to excite ALTEX6 regardless of what channel is active                            |
| 21    | AEX5            | 0   | RW     | <b>ALTEX5 Always Excite Enable</b><br>Set this bit to excite ALTEX5 regardless of what channel is active                            |
| 20    | AEX4            | 0   | RW     | <b>ALTEX4 Always Excite Enable</b><br>Set this bit to excite ALTEX4 regardless of what channel is active                            |
| 19    | AEX3            | 0   | RW     | <b>ALTEX3 Always Excite Enable</b><br>Set this bit to excite ALTEX3 regardless of what channel is active                            |
| 18    | AEX2            | 0   | RW     | <b>ALTEX2 Always Excite Enable</b><br>Set this bit to excite ALTEX2 regardless of what channel is active                            |
| 17    | AEX1            | 0   | RW     | <b>ALTEX1 Always Excite Enable</b><br>Set this bit to excite ALTEX1 regardless of what channel is active                            |
| 16    | AEX0            | 0   | RW     | <b>ALTEX0 Always Excite Enable</b><br>Set this bit to excite ALTEX0 regardless of what channel is active                            |
| 15:14 | IDLECONF7       | 0x0   | RW     | <b>ALTEX7 Idle Phase Configuration</b><br>This bitfield determines how the alternate excite pin is configured during the idle phase |
|       | Value           | Mode  |        | Description   |
|       | 0               | DISABLE   |        | ALTEX7 output is disabled in idle phase   |
|       | 1               | HIGH  |        | ALTEX7 output is high in idle phase   |
|       | 2               | LOW   |        | ALTEX7 output is low in idle phase  |
| 13:12 | IDLECONF6       | 0x0   | RW     | <b>ALTEX6 Idle Phase Configuration</b><br>This bitfield determines how the alternate excite pin is configured during the idle phase |

| Bit   | Name      | Reset   | Access | Description   |
|-------|-----------|---------|--------|---|
|       | Value     | Mode    |        | Description   |
|       | 0         | DISABLE |        | ALTEX6 output is disabled in idle phase   |
|       | 1         | HIGH    |        | ALTEX6 output is high in idle phase   |
|       | 2         | LOW     |        | ALTEX6 output is low in idle phase  |
| 11:10 | IDLECONF5 | 0x0     | RW     | <b>ALTEX5 Idle Phase Configuration</b><br>This bitfield determines how the alternate excite pin is configured during the idle phase |
|       | Value     | Mode    |        | Description   |
|       | 0         | DISABLE |        | ALTEX5 output is disabled in idle phase   |
|       | 1         | HIGH    |        | ALTEX5 output is high in idle phase   |
|       | 2         | LOW     |        | ALTEX5 output is low in idle phase  |
| 9:8   | IDLECONF4 | 0x0     | RW     | <b>ALTEX4 Idle Phase Configuration</b><br>This bitfield determines how the alternate excite pin is configured during the idle phase |
|       | Value     | Mode    |        | Description   |
|       | 0         | DISABLE |        | ALTEX4 output is disabled in idle phase   |
|       | 1         | HIGH    |        | ALTEX4 output is high in idle phase   |
|       | 2         | LOW     |        | ALTEX4 output is low in idle phase  |
| 7:6   | IDLECONF3 | 0x0     | RW     | <b>ALTEX3 Idle Phase Configuration</b><br>This bitfield determines how the alternate excite pin is configured during the idle phase |
|       | Value     | Mode    |        | Description   |
|       | 0         | DISABLE |        | ALTEX3 output is disabled in idle phase   |
|       | 1         | HIGH    |        | ALTEX3 output is high in idle phase   |
|       | 2         | LOW     |        | ALTEX3 output is low in idle phase  |
| 5:4   | IDLECONF2 | 0x0     | RW     | <b>ALTEX2 Idle Phase Configuration</b><br>This bitfield determines how the alternate excite pin is configured during the idle phase |
|       | Value     | Mode    |        | Description   |
|       | 0         | DISABLE |        | ALTEX2 output is disabled in idle phase   |
|       | 1         | HIGH    |        | ALTEX2 output is high in idle phase   |
|       | 2         | LOW     |        | ALTEX2 output is low in idle phase  |
| 3:2   | IDLECONF1 | 0x0     | RW     | <b>ALTEX1 Idle Phase Configuration</b><br>This bitfield determines how the alternate excite pin is configured during the idle phase |
|       | Value     | Mode    |        | Description   |
|       | 0         | DISABLE |        | ALTEX1 output is disabled in idle phase   |
|       | 1         | HIGH    |        | ALTEX1 output is high in idle phase   |
|       | 2         | LOW     |        | ALTEX1 output is low in idle phase  |

| Bit | Name      | Reset   | Access | Description   |
|-----|-----------|---------|--------|---|
| 1:0 | IDLECONF0 | 0x0     | RW     | <b>ALTEX0 Idle Phase Configuration</b><br>This bitfield determines how the alternate excite pin is configured during the idle phase |
|     | Value     | Mode    |        | Description   |
|     | 0         | DISABLE |        | ALTEX0 output is disabled in idle phase   |
|     | 1         | HIGH    |        | ALTEX0 output is high in idle phase   |
|     | 2         | LOW     |        | ALTEX0 output is low in idle phase  |

## 29.5.19 LESENSE\_IF - Interrupt Flag Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |       |    |       |    |          |    |          |    |        |    |     |    |              |   |      |   |      |   |      |   |      |   |      |   |      |  |     |  |     |  |     |  |     |  |     |  |     |  |     |  |     |  |     |  |     |
|---------------|--------------|----|----|----|----|----|----|----|----|-------|----|-------|----|----------|----|----------|----|--------|----|-----|----|--------------|---|------|---|------|---|------|---|------|---|------|---|------|--|-----|--|-----|--|-----|--|-----|--|-----|--|-----|--|-----|--|-----|--|-----|--|-----|
| 0x050         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22    | 21 | 20    | 19 | 18       | 17 | 16       | 15 | 14     | 13 | 12  | 11 | 10           | 9 | 8    | 7 | 6    | 5 | 4    | 3 | 2    | 1 | 0    |   |      |  |     |  |     |  |     |  |     |  |     |  |     |  |     |  |     |  |     |  |     |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    | R     | 0  | R     | 0  | R        | 0  | R        | 0  | R      | 0  | R   | 0  | R            | 0 | R    | 0 | R    | 0 | R    | 0 | R    | 0 | R    | 0 |      |  |     |  |     |  |     |  |     |  |     |  |     |  |     |  |     |  |     |  |     |
| <b>Access</b> |              |    |    |    |    |    |    |    |    | R     |    | R     |    | R        |    | R        |    | R      |    | R   |    | R            |   | R    |   | R    |   | R    |   | R    |   | R    |   |      |  |     |  |     |  |     |  |     |  |     |  |     |  |     |  |     |  |     |  |     |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    | CNTOF |    | BUFOF |    | BUFLEVEL |    | BUFDATAV |    | DECERR |    | DEC |    | SCANCOMPLETE |   | CH15 |   | CH14 |   | CH13 |   | CH12 |   | CH11 |   | CH10 |  | CH9 |  | CH8 |  | CH7 |  | CH6 |  | CH5 |  | CH4 |  | CH3 |  | CH2 |  | CH1 |  | CH0 |

| Bit   | Name         | Reset  | Access | Description  |
|-------|--------------|--|--------|--|
| 31:23 | Reserved     | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 22    | CNTOF        | 0  | R      | <b>CNTOF Interrupt Flag</b><br>Set when the LESENSE counter overflows.             |
| 21    | BUFOF        | 0  | R      | <b>BUFOF Interrupt Flag</b><br>Set when the result buffer overflows                |
| 20    | BUFLEVEL     | 0  | R      | <b>BUFLEVEL Interrupt Flag</b><br>Set when the data buffer is full.                |
| 19    | BUFDATAV     | 0  | R      | <b>BUFDATAV Interrupt Flag</b><br>Set when data is available in the result buffer. |
| 18    | DECERR       | 0  | R      | <b>DECERR Interrupt Flag</b><br>Set when the decoder detects an error              |
| 17    | DEC          | 0  | R      | <b>DEC Interrupt Flag</b><br>Set when the decoder has issued an interrupt request  |
| 16    | SCANCOMPLETE | 0  | R      | <b>SCANCOMPLETE Interrupt Flag</b><br>Set when a scan sequence is completed        |
| 15    | CH15         | 0  | R      | <b>CH15 Interrupt Flag</b><br>Set when channel 15 triggers                         |
| 14    | CH14         | 0  | R      | <b>CH14 Interrupt Flag</b><br>Set when channel 14 triggers                         |
| 13    | CH13         | 0  | R      | <b>CH13 Interrupt Flag</b><br>Set when channel 13 triggers                         |
| 12    | CH12         | 0  | R      | <b>CH12 Interrupt Flag</b><br>Set when channel 12 triggers                         |
| 11    | CH11         | 0  | R      | <b>CH11 Interrupt Flag</b><br>Set when channel 11 triggers                         |
| 10    | CH10         | 0  | R      | <b>CH10 Interrupt Flag</b><br>Set when channel 10 triggers                         |

| Bit | Name | Reset | Access | Description  |
|-----|------|-------|--------|--|
| 9   | CH9  | 0     | R      | <b>CH9 Interrupt Flag</b><br>Set when channel 9 triggers |
| 8   | CH8  | 0     | R      | <b>CH8 Interrupt Flag</b><br>Set when channel 8 triggers |
| 7   | CH7  | 0     | R      | <b>CH7 Interrupt Flag</b><br>Set when channel 7 triggers |
| 6   | CH6  | 0     | R      | <b>CH6 Interrupt Flag</b><br>Set when channel 6 triggers |
| 5   | CH5  | 0     | R      | <b>CH5 Interrupt Flag</b><br>Set when channel 5 triggers |
| 4   | CH4  | 0     | R      | <b>CH4 Interrupt Flag</b><br>Set when channel 4 triggers |
| 3   | CH3  | 0     | R      | <b>CH3 Interrupt Flag</b><br>Set when channel 3 triggers |
| 2   | CH2  | 0     | R      | <b>CH2 Interrupt Flag</b><br>Set when channel 2 triggers |
| 1   | CH1  | 0     | R      | <b>CH1 Interrupt Flag</b><br>Set when channel 1 triggers |
| 0   | CH0  | 0     | R      | <b>CH0 Interrupt Flag</b><br>Set when channel 0 triggers |

### 29.5.20 LESENSE\_IFS - Interrupt Flag Set Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |       |       |          |          |        |     |              |      |      |      |      |      |      |     |     |     |     |     |     |     |     |     |     |     |    |    |    |    |
|---------------|--------------|----|----|----|----|----|----|----|----|-------|-------|----------|----------|--------|-----|--------------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|
| 0x054         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22    | 21    | 20       | 19       | 18     | 17  | 16           | 15   | 14   | 13   | 12   | 11   | 10   | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |     |    |    |    |    |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    | 0     | 0     | 0        | 0        | 0      | 0   | 0            | 0    | 0    | 0    | 0    | 0    | 0    | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 0  |    |
| <b>Access</b> |              |    |    |    |    |    |    |    |    | W1    | W1    | W1       | W1       | W1     | W1  | W1           | W1   | W1   | W1   | W1   | W1   | W1   | W1  | W1  | W1  | W1  | W1  | W1  | W1  | W1  | W1  | W1  | W1  | W1 | W1 | W1 | W1 |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    | CNTOF | BUFOF | BUFLEVEL | BUFDATAV | DECERR | DEC | SCANCOMPLETE | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH1 | CH0 |    |    |    |    |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 31:23 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 22    | CNTOF           | 0   | W1     | <b>Set CNTOF Interrupt Flag</b><br>Write 1 to set the CNTOF interrupt flag               |
| 21    | BUFOF           | 0   | W1     | <b>Set BUFOF Interrupt Flag</b><br>Write 1 to set the BUFOF interrupt flag               |
| 20    | BUFLEVEL        | 0   | W1     | <b>Set BUFLEVEL Interrupt Flag</b><br>Write 1 to set the BUFLEVEL interrupt flag         |
| 19    | BUFDATAV        | 0   | W1     | <b>Set BUFDATAV Interrupt Flag</b><br>Write 1 to set the BUFDATAV interrupt flag         |
| 18    | DECERR          | 0   | W1     | <b>Set DECERR Interrupt Flag</b><br>Write 1 to set the DECERR interrupt flag             |
| 17    | DEC             | 0   | W1     | <b>Set DEC Interrupt Flag</b><br>Write 1 to set the DEC interrupt flag                   |
| 16    | SCANCOMPLETE    | 0   | W1     | <b>Set SCANCOMPLETE Interrupt Flag</b><br>Write 1 to set the SCANCOMPLETE interrupt flag |
| 15    | CH15            | 0   | W1     | <b>Set CH15 Interrupt Flag</b><br>Write 1 to set the CH15 interrupt flag                 |
| 14    | CH14            | 0   | W1     | <b>Set CH14 Interrupt Flag</b><br>Write 1 to set the CH14 interrupt flag                 |
| 13    | CH13            | 0   | W1     | <b>Set CH13 Interrupt Flag</b><br>Write 1 to set the CH13 interrupt flag                 |
| 12    | CH12            | 0   | W1     | <b>Set CH12 Interrupt Flag</b><br>Write 1 to set the CH12 interrupt flag                 |
| 11    | CH11            | 0   | W1     | <b>Set CH11 Interrupt Flag</b><br>Write 1 to set the CH11 interrupt flag                 |

| Bit | Name | Reset | Access | Description  |
|-----|------|-------|--------|--|
| 10  | CH10 | 0     | W1     | <b>Set CH10 Interrupt Flag</b><br>Write 1 to set the CH10 interrupt flag |
| 9   | CH9  | 0     | W1     | <b>Set CH9 Interrupt Flag</b><br>Write 1 to set the CH9 interrupt flag   |
| 8   | CH8  | 0     | W1     | <b>Set CH8 Interrupt Flag</b><br>Write 1 to set the CH8 interrupt flag   |
| 7   | CH7  | 0     | W1     | <b>Set CH7 Interrupt Flag</b><br>Write 1 to set the CH7 interrupt flag   |
| 6   | CH6  | 0     | W1     | <b>Set CH6 Interrupt Flag</b><br>Write 1 to set the CH6 interrupt flag   |
| 5   | CH5  | 0     | W1     | <b>Set CH5 Interrupt Flag</b><br>Write 1 to set the CH5 interrupt flag   |
| 4   | CH4  | 0     | W1     | <b>Set CH4 Interrupt Flag</b><br>Write 1 to set the CH4 interrupt flag   |
| 3   | CH3  | 0     | W1     | <b>Set CH3 Interrupt Flag</b><br>Write 1 to set the CH3 interrupt flag   |
| 2   | CH2  | 0     | W1     | <b>Set CH2 Interrupt Flag</b><br>Write 1 to set the CH2 interrupt flag   |
| 1   | CH1  | 0     | W1     | <b>Set CH1 Interrupt Flag</b><br>Write 1 to set the CH1 interrupt flag   |
| 0   | CH0  | 0     | W1     | <b>Set CH0 Interrupt Flag</b><br>Write 1 to set the CH0 interrupt flag   |

## 29.5.21 LESENSE\_IFC - Interrupt Flag Clear Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |       |       |          |          |        |       |              |       |       |       |       |       |       |       |       |       |       |       |       |       |       |     |     |
|---------------|--------------|----|----|----|----|----|----|----|----|----|-------|-------|----------|----------|--------|-------|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-----|-----|
| 0x058         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21    | 20    | 19       | 18       | 17     | 16    | 15           | 14    | 13    | 12    | 11    | 10    | 9     | 8     | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0   |     |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    | 0     | 0     | 0        | 0        | 0      | 0     | 0            | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0   |     |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    | (R)W1 | (R)W1 | (R)W1    | (R)W1    | (R)W1  | (R)W1 | (R)W1        | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 | (R)W1 |     |     |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    | CNTOF | BUFOF | BUFLEVEL | BUFDATAV | DECERR | DEC   | SCANCOMPLETE | CH15  | CH14  | CH13  | CH12  | CH11  | CH10  | CH9   | CH8   | CH7   | CH6   | CH5   | CH4   | CH3   | CH2   | CH1 | CH0 |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:23 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 22    | CNTOF           | 0   | (R)W1  | <b>Clear CNTOF Interrupt Flag</b><br><br>Write 1 to clear the CNTOF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).               |
| 21    | BUFOF           | 0   | (R)W1  | <b>Clear BUFOF Interrupt Flag</b><br><br>Write 1 to clear the BUFOF interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).               |
| 20    | BUFLEVEL        | 0   | (R)W1  | <b>Clear BUFLEVEL Interrupt Flag</b><br><br>Write 1 to clear the BUFLEVEL interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).         |
| 19    | BUFDATAV        | 0   | (R)W1  | <b>Clear BUFDATAV Interrupt Flag</b><br><br>Write 1 to clear the BUFDATAV interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).         |
| 18    | DECERR          | 0   | (R)W1  | <b>Clear DECERR Interrupt Flag</b><br><br>Write 1 to clear the DECERR interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).             |
| 17    | DEC             | 0   | (R)W1  | <b>Clear DEC Interrupt Flag</b><br><br>Write 1 to clear the DEC interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                   |
| 16    | SCANCOMPLETE    | 0   | (R)W1  | <b>Clear SCANCOMPLETE Interrupt Flag</b><br><br>Write 1 to clear the SCANCOMPLETE interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 15    | CH15            | 0   | (R)W1  | <b>Clear CH15 Interrupt Flag</b><br><br>Write 1 to clear the CH15 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                 |
| 14    | CH14            | 0   | (R)W1  | <b>Clear CH14 Interrupt Flag</b><br><br>Write 1 to clear the CH14 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).                 |

| Bit | Name | Reset | Access | Description   |
|-----|------|-------|--------|---|
| 13  | CH13 | 0     | (R)W1  | <b>Clear CH13 Interrupt Flag</b><br>Write 1 to clear the CH13 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 12  | CH12 | 0     | (R)W1  | <b>Clear CH12 Interrupt Flag</b><br>Write 1 to clear the CH12 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 11  | CH11 | 0     | (R)W1  | <b>Clear CH11 Interrupt Flag</b><br>Write 1 to clear the CH11 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 10  | CH10 | 0     | (R)W1  | <b>Clear CH10 Interrupt Flag</b><br>Write 1 to clear the CH10 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 9   | CH9  | 0     | (R)W1  | <b>Clear CH9 Interrupt Flag</b><br>Write 1 to clear the CH9 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |
| 8   | CH8  | 0     | (R)W1  | <b>Clear CH8 Interrupt Flag</b><br>Write 1 to clear the CH8 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |
| 7   | CH7  | 0     | (R)W1  | <b>Clear CH7 Interrupt Flag</b><br>Write 1 to clear the CH7 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |
| 6   | CH6  | 0     | (R)W1  | <b>Clear CH6 Interrupt Flag</b><br>Write 1 to clear the CH6 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |
| 5   | CH5  | 0     | (R)W1  | <b>Clear CH5 Interrupt Flag</b><br>Write 1 to clear the CH5 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |
| 4   | CH4  | 0     | (R)W1  | <b>Clear CH4 Interrupt Flag</b><br>Write 1 to clear the CH4 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |
| 3   | CH3  | 0     | (R)W1  | <b>Clear CH3 Interrupt Flag</b><br>Write 1 to clear the CH3 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |
| 2   | CH2  | 0     | (R)W1  | <b>Clear CH2 Interrupt Flag</b><br>Write 1 to clear the CH2 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |
| 1   | CH1  | 0     | (R)W1  | <b>Clear CH1 Interrupt Flag</b><br>Write 1 to clear the CH1 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |
| 0   | CH0  | 0     | (R)W1  | <b>Clear CH0 Interrupt Flag</b><br>Write 1 to clear the CH0 interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).   |

## 29.5.22 LESENSE\_IEN - Interrupt Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |       |       |          |          |        |     |              |      |      |      |      |      |      |     |     |     |     |     |     |     |     |     |     |
|---------------|--------------|----|----|----|----|----|----|----|----|-------|-------|----------|----------|--------|-----|--------------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0x05C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22    | 21    | 20       | 19       | 18     | 17  | 16           | 15   | 14   | 13   | 12   | 11   | 10   | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    | 0     | 0     | 0        | 0        | 0      | 0   | 0            | 0    | 0    | 0    | 0    | 0    | 0    | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |     |
| <b>Access</b> |              |    |    |    |    |    |    |    |    | RW    | RW    | RW       | RW       | RW     | RW  | RW           | RW   | RW   | RW   | RW   | RW   | RW   | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  | RW  |     |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    | CNTOF | BUFOF | BUFLEVEL | BUFDATAV | DECERR | DEC | SCANCOMPLETE | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:23 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 22    | CNTOF           | 0   | RW     | <b>CNTOF Interrupt Enable</b><br>Enable/disable the CNTOF interrupt               |
| 21    | BUFOF           | 0   | RW     | <b>BUFOF Interrupt Enable</b><br>Enable/disable the BUFOF interrupt               |
| 20    | BUFLEVEL        | 0   | RW     | <b>BUFLEVEL Interrupt Enable</b><br>Enable/disable the BUFLEVEL interrupt         |
| 19    | BUFDATAV        | 0   | RW     | <b>BUFDATAV Interrupt Enable</b><br>Enable/disable the BUFDATAV interrupt         |
| 18    | DECERR          | 0   | RW     | <b>DECERR Interrupt Enable</b><br>Enable/disable the DECERR interrupt             |
| 17    | DEC             | 0   | RW     | <b>DEC Interrupt Enable</b><br>Enable/disable the DEC interrupt                   |
| 16    | SCANCOMPLETE    | 0   | RW     | <b>SCANCOMPLETE Interrupt Enable</b><br>Enable/disable the SCANCOMPLETE interrupt |
| 15    | CH15            | 0   | RW     | <b>CH15 Interrupt Enable</b><br>Enable/disable the CH15 interrupt                 |
| 14    | CH14            | 0   | RW     | <b>CH14 Interrupt Enable</b><br>Enable/disable the CH14 interrupt                 |
| 13    | CH13            | 0   | RW     | <b>CH13 Interrupt Enable</b><br>Enable/disable the CH13 interrupt                 |
| 12    | CH12            | 0   | RW     | <b>CH12 Interrupt Enable</b><br>Enable/disable the CH12 interrupt                 |
| 11    | CH11            | 0   | RW     | <b>CH11 Interrupt Enable</b><br>Enable/disable the CH11 interrupt                 |

| Bit | Name | Reset | Access | Description   |
|-----|------|-------|--------|---|
| 10  | CH10 | 0     | RW     | <b>CH10 Interrupt Enable</b><br>Enable/disable the CH10 interrupt |
| 9   | CH9  | 0     | RW     | <b>CH9 Interrupt Enable</b><br>Enable/disable the CH9 interrupt   |
| 8   | CH8  | 0     | RW     | <b>CH8 Interrupt Enable</b><br>Enable/disable the CH8 interrupt   |
| 7   | CH7  | 0     | RW     | <b>CH7 Interrupt Enable</b><br>Enable/disable the CH7 interrupt   |
| 6   | CH6  | 0     | RW     | <b>CH6 Interrupt Enable</b><br>Enable/disable the CH6 interrupt   |
| 5   | CH5  | 0     | RW     | <b>CH5 Interrupt Enable</b><br>Enable/disable the CH5 interrupt   |
| 4   | CH4  | 0     | RW     | <b>CH4 Interrupt Enable</b><br>Enable/disable the CH4 interrupt   |
| 3   | CH3  | 0     | RW     | <b>CH3 Interrupt Enable</b><br>Enable/disable the CH3 interrupt   |
| 2   | CH2  | 0     | RW     | <b>CH2 Interrupt Enable</b><br>Enable/disable the CH2 interrupt   |
| 1   | CH1  | 0     | RW     | <b>CH1 Interrupt Enable</b><br>Enable/disable the CH1 interrupt   |
| 0   | CH0  | 0     | RW     | <b>CH0 Interrupt Enable</b><br>Enable/disable the CH0 interrupt   |

### 29.5.23 LESENSE\_SYNCBUSY - Synchronization Busy Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |     |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|-----|---|---|---|---|---|---|---|
| 0x060         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | R   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | CMD |   |   |   |   |   |   |   |

| Bit  | Name            | Reset   | Access | Description  |
|------|-----------------|---|--------|--|
| 31:8 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 7    | CMD             | 0   | R      | <b>CMD Register Busy</b><br>Set when the value written to CMD is being synchronized. |
| 6:0  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |

### 29.5.24 LESENSE\_ROUTEPEN - I/O Routing Register (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |           |           |           |           |           |           |           |           |         |         |         |         |         |         |        |        |        |        |        |        |        |        |        |        |    |    |
|---------------|--------------|----|----|----|----|----|----|----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|---------|---------|---------|---------|---------|---------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|----|----|
| 0x064         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23        | 22        | 21        | 20        | 19        | 18        | 17        | 16        | 15      | 14      | 13      | 12      | 11      | 10      | 9      | 8      | 7      | 6      | 5      | 4      | 3      | 2      | 1      | 0      |    |    |
| <b>Reset</b>  |              |    |    |    |    |    |    |    | 0         | 0         | 0         | 0         | 0         | 0         | 0         | 0         | 0       | 0       | 0       | 0       | 0       | 0       | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0  | 0  |
| <b>Access</b> |              |    |    |    |    |    |    |    | RW        | RW      | RW      | RW      | RW      | RW      | RW      | RW     | RW     | RW     | RW     | RW     | RW     | RW     | RW     | RW     | RW     | RW | RW |
| <b>Name</b>   |              |    |    |    |    |    |    |    | ALTEX7PEN | ALTEX6PEN | ALTEX5PEN | ALTEX4PEN | ALTEX3PEN | ALTEX2PEN | ALTEX1PEN | ALTEX0PEN | CH15PEN | CH14PEN | CH13PEN | CH12PEN | CH11PEN | CH10PEN | CH9PEN | CH8PEN | CH7PEN | CH6PEN | CH5PEN | CH4PEN | CH3PEN | CH2PEN | CH1PEN | CH0PEN |    |    |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:24 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 23    | ALTEX7PEN       | 0   | RW     | <b>ALTEX7 Pin Enable</b><br>Set this bit to enable LESENSE ALTEX7 pin |
| 22    | ALTEX6PEN       | 0   | RW     | <b>ALTEX6 Pin Enable</b><br>Set this bit to enable LESENSE ALTEX6 pin |
| 21    | ALTEX5PEN       | 0   | RW     | <b>ALTEX5 Pin Enable</b><br>Set this bit to enable LESENSE ALTEX5 pin |
| 20    | ALTEX4PEN       | 0   | RW     | <b>ALTEX4 Pin Enable</b><br>Set this bit to enable LESENSE ALTEX4 pin |
| 19    | ALTEX3PEN       | 0   | RW     | <b>ALTEX3 Pin Enable</b><br>Set this bit to enable LESENSE ALTEX3 pin |
| 18    | ALTEX2PEN       | 0   | RW     | <b>ALTEX2 Pin Enable</b><br>Set this bit to enable LESENSE ALTEX2 pin |
| 17    | ALTEX1PEN       | 0   | RW     | <b>ALTEX1 Pin Enable</b><br>Set this bit to enable LESENSE ALTEX1 pin |
| 16    | ALTEX0PEN       | 0   | RW     | <b>ALTEX0 Pin Enable</b><br>Set this bit to enable LESENSE ALTEX0 pin |
| 15    | CH15PEN         | 0   | RW     | <b>CH15 Pin Enable</b><br>Set this bit to enable LESENSE CH15 pin     |
| 14    | CH14PEN         | 0   | RW     | <b>CH14 Pin Enable</b><br>Set this bit to enable LESENSE CH14 pin     |
| 13    | CH13PEN         | 0   | RW     | <b>CH13 Pin Enable</b><br>Set this bit to enable LESENSE CH13 pin     |
| 12    | CH12PEN         | 0   | RW     | <b>CH12 Pin Enable</b><br>Set this bit to enable LESENSE CH12 pin     |
| 11    | CH11PEN         | 0   | RW     | <b>CH11 Pin Enable</b><br>Set this bit to enable LESENSE CH11 pin     |

| Bit | Name    | Reset | Access | Description   |
|-----|---------|-------|--------|---|
| 10  | CH10PEN | 0     | RW     | <b>CH10 Pin Enable</b><br>Set this bit to enable LESENSE CH10 pin |
| 9   | CH9PEN  | 0     | RW     | <b>CH9 Pin Enable</b><br>Set this bit to enable LESENSE CH9 pin   |
| 8   | CH8PEN  | 0     | RW     | <b>CH8 Pin Enable</b><br>Set this bit to enable LESENSE CH8 pin   |
| 7   | CH7PEN  | 0     | RW     | <b>CH7 Pin Enable</b><br>Set this bit to enable LESENSE CH7 pin   |
| 6   | CH6PEN  | 0     | RW     | <b>CH6 Pin Enable</b><br>Set this bit to enable LESENSE CH6 pin   |
| 5   | CH5PEN  | 0     | RW     | <b>CH5 Pin Enable</b><br>Set this bit to enable LESENSE CH5 pin   |
| 4   | CH4PEN  | 0     | RW     | <b>CH4 Pin Enable</b><br>Set this bit to enable LESENSE CH4 pin   |
| 3   | CH3PEN  | 0     | RW     | <b>CH3 Pin Enable</b><br>Set this bit to enable LESENSE CH3 pin   |
| 2   | CH2PEN  | 0     | RW     | <b>CH2 Pin Enable</b><br>Set this bit to enable LESENSE CH2 pin   |
| 1   | CH1PEN  | 0     | RW     | <b>CH1 Pin Enable</b><br>Set this bit to enable LESENSE CH1 pin   |
| 0   | CH0PEN  | 0     | RW     | <b>CH0 Pin Enable</b><br>Set this bit to enable LESENSE CH0 pin   |



| Bit  | Name            | Reset   | Access | Description  |
|------|-----------------|---|--------|--|
| 13   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 12:8 | NEXTSTATE       | 0xXX  | RW     | <b>Next State Index</b><br>Index of next state to be entered if the sensor state equals COMP |
| 7:4  | MASK            | 0xX   | RW     | <b>Sensor Mask</b><br>Set bit X to exclude sensor X from evaluation.                         |
| 3:0  | COMP            | 0xX   | RW     | <b>Sensor Compare Value</b><br>State transition is triggered when sensor state equals COMP   |

### 29.5.26 LESENSE\_STx\_TCONFB - State Transition Configuration B (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |        |       |    |    |           |    |    |      |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|--------|-------|----|----|-----------|----|----|------|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|--|--|--|--|--|--|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18     | 17    | 16 | 15 | 14        | 13 | 12 | 11   | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |
| 0x104         |              |    |    |    |    |    |    |    |    |    |    |    |    |        |       |    |    |           |    |    |      |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    | 0xX    | X     |    |    | 0xXX      |    |    | 0xX  |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    | RW     | RW    |    |    | RW        |    |    | RW   |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    | PRSACT | SETIF |    |    | NEXTSTATE |    |    | MASK |    |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |

| Bit   | Name               | Reset   | Access | Description   |
|-------|--------------------|---|--------|---|
| 31:19 | <i>Reserved</i>    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 18:16 | PRSACT             | 0xX   | RW     | <b>Configure Transition Action</b><br>Configure which action to perform when sensor state equals COMP |
|       | DECCTRL_PRSCNT = 0 |   |        |   |
|       | Mode               | Value   |        | Description   |
|       | NONE               | 0   |        | No PRS pulses generated   |
|       | PRS0               | 1   |        | Generate pulse on PRS0  |
|       | PRS1               | 2   |        | Generate pulse on PRS1  |
|       | PRS01              | 3   |        | Generate pulse on PRS0 and PRS1   |
|       | PRS2               | 4   |        | Generate pulse on PRS2  |
|       | PRS02              | 5   |        | Generate pulse on PRS0 and PRS2   |
|       | PRS12              | 6   |        | Generate pulse on PRS1 and PRS2   |
|       | PRS012             | 7   |        | Generate pulse on PRS0, PRS1 and PRS2   |
|       | DECCTRL_PRSCNT = 1 |   |        |   |
|       | NONE               | 0   |        | Do not count  |
|       | UP                 | 1   |        | Count up  |
|       | DOWN               | 2   |        | Count down  |
|       | PRS2               | 4   |        | Generate pulse on PRS2  |
|       | UPANDPRS2          | 5   |        | Count up and generate pulse on PRS2.  |
|       | DOWNANDPRS2        | 6   |        | Count down and generate pulse on PRS2.  |
| 15    | SETIF              | X   | RW     | <b>Set Interrupt Flag</b><br>Set interrupt flag when sensor state equals COMP                         |
| 14:13 | <i>Reserved</i>    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |

| Bit  | Name      | Reset | Access | Description  |
|------|-----------|-------|--------|--|
| 12:8 | NEXTSTATE | 0xXX  | RW     | <b>Next State Index</b><br>Index of next state to be entered if the sensor state equals COMP |
| 7:4  | MASK      | 0xX   | RW     | <b>Sensor Mask</b><br>Set bit X to exclude sensor X from evaluation.                         |
| 3:0  | COMP      | 0xX   | RW     | <b>Sensor Compare Value</b><br>State transition is triggered when sensor state equals COMP   |

### 29.5.27 LESENSE\_BUFx\_DATA - Scan Results (Async Reg)

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |    |    |    |    |   |   |   |        |   |   |   |   |   |   |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|----|----|----|----|---|---|---|--------|---|---|---|---|---|---|--|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19      | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6      | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| 0x200         |              |    |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |    |    |    |    |   |   |   |        |   |   |   |   |   |   |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    | 0xX     |    |    |    |    |    |    |    |    |    |   |   |   | 0XXXXX |   |   |   |   |   |   |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    | R       |    |    |    |    |    |    |    |    |    |   |   |   | RWH    |   |   |   |   |   |   |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    | DATASRC |    |    |    |    |    |    |    |    |    |   |   |   | DATA   |   |   |   |   |   |   |  |  |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 31:20 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 19:16 | DATASRC         | 0xX   | R      | <b>Result Data Source</b><br>This bitfield contains the channel index for the sensor result in DATA. |
| 15:0  | DATA            | 0XXXXX  | RWH    | <b>Scan Result Buffer</b><br>This bitfield contains the sensor result.                               |

**29.5.28 LESENSE\_CHx\_TIMING - Scan Configuration (Async Reg)**

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |            |    |    |    |    |    |    |    |           |    |    |    |    |    |   |   |        |   |   |   |   |   |   |   |  |  |
|---------------|--------------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|-----------|----|----|----|----|----|---|---|--------|---|---|---|---|---|---|---|--|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| 0x240         |              |    |    |    |    |    |    |    |            |    |    |    |    |    |    |    |           |    |    |    |    |    |   |   |        |   |   |   |   |   |   |   |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    | 0xFFFF     |    |    |    |    |    |    |    | 0XXX      |    |    |    |    |    |   |   | 0XXX   |   |   |   |   |   |   |   |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    | RW         |    |    |    |    |    |    |    | RW        |    |    |    |    |    |   |   | RW     |   |   |   |   |   |   |   |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    | MEASUREDLY |    |    |    |    |    |    |    | SAMPLEDLY |    |    |    |    |    |   |   | EXTIME |   |   |   |   |   |   |   |  |  |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:24 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 23:14 | MEASUREDLY      | 0xFFFF  | RW     | <b>Set Measure Delay</b><br>Configure measure delay. Sensor measuring is delayed for MEASUREDLY EXCLK cycles. |
| 13:6  | SAMPLEDLY       | 0xFF  | RW     | <b>Set Sample Delay</b><br>Configure sample delay. Sampling will occur after SAMPLEDLY SAMPLECLK cycles.      |
| 5:0   | EXTIME          | 0xFF  | RW     | <b>Set Excitation Time</b><br>Configure excitation time. Excitation will last EXTIME EXCLK cycles.            |

**29.5.29 LESENSE\_CHx\_INTERACT - Scan Configuration (Async Reg)**

For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |       |           |       |        |    |    |       |    |    |        |    |    |   |   |   |   |   |       |   |   |   |   |  |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|-------|-----------|-------|--------|----|----|-------|----|----|--------|----|----|---|---|---|---|---|-------|---|---|---|---|--|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21    | 20        | 19    | 18     | 17 | 16 | 15    | 14 | 13 | 12     | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4     | 3 | 2 | 1 | 0 |  |  |
| 0x244         |              |    |    |    |    |    |    |    |    |    |       |           |       |        |    |    |       |    |    |        |    |    |   |   |   |   |   |       |   |   |   |   |  |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    | X     | X         | X     | 0xX    |    |    | 0xX   |    |    | 0xX    |    |    |   |   |   |   |   | 0xxxx |   |   |   |   |  |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    | RW    | RW        | RW    | RW     |    |    | RW    |    |    | RW     |    |    |   |   |   |   |   | RW    |   |   |   |   |  |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    | ALTEX | SAMPLECLK | EXCLK | EXMODE |    |    | SETIF |    |    | SAMPLE |    |    |   |   |   |   |   | THRES |   |   |   |   |  |  |

| Bit   | Name            | Reset   | Access | Description   |       |      |             |   |         |                                |   |          |                                  |   |     |                               |   |        |             |
|-------|-----------------|---|--------|---|-------|------|-------------|---|---------|--------------------------------|---|----------|----------------------------------|---|-----|-------------------------------|---|--------|-------------|
| 31:22 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |       |      |             |   |         |                                |   |          |                                  |   |     |                               |   |        |             |
| 21    | ALTEX           | X   | RW     | <b>Use Alternative Excite Pin</b><br>If set, alternative excite pin will be used for excitation   |       |      |             |   |         |                                |   |          |                                  |   |     |                               |   |        |             |
| 20    | SAMPLECLK       | X   | RW     | <b>Select Clock Used for Timing of Sample Delay</b><br>This bit is used to configure which clock is used for timing of SAMPLEDLY<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>LFACLK</td> <td>LFACLK will be used for timing</td> </tr> <tr> <td>1</td> <td>AUXHFRCO</td> <td>AUXHFRCO will be used for timing</td> </tr> </tbody> </table>  | Value | Mode | Description | 0 | LFACLK  | LFACLK will be used for timing | 1 | AUXHFRCO | AUXHFRCO will be used for timing |   |     |                               |   |        |             |
| Value | Mode            | Description   |        |   |       |      |             |   |         |                                |   |          |                                  |   |     |                               |   |        |             |
| 0     | LFACLK          | LFACLK will be used for timing  |        |   |       |      |             |   |         |                                |   |          |                                  |   |     |                               |   |        |             |
| 1     | AUXHFRCO        | AUXHFRCO will be used for timing  |        |   |       |      |             |   |         |                                |   |          |                                  |   |     |                               |   |        |             |
| 19    | EXCLK           | X   | RW     | <b>Select Clock Used for Excitation Timing</b><br>This bit is used to configure which clock is used for timing of EXTIME and MEASUREDLY<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>LFACLK</td> <td>LFACLK will be used for timing</td> </tr> <tr> <td>1</td> <td>AUXHFRCO</td> <td>AUXHFRCO will be used for timing</td> </tr> </tbody> </table>   | Value | Mode | Description | 0 | LFACLK  | LFACLK will be used for timing | 1 | AUXHFRCO | AUXHFRCO will be used for timing |   |     |                               |   |        |             |
| Value | Mode            | Description   |        |   |       |      |             |   |         |                                |   |          |                                  |   |     |                               |   |        |             |
| 0     | LFACLK          | LFACLK will be used for timing  |        |   |       |      |             |   |         |                                |   |          |                                  |   |     |                               |   |        |             |
| 1     | AUXHFRCO        | AUXHFRCO will be used for timing  |        |   |       |      |             |   |         |                                |   |          |                                  |   |     |                               |   |        |             |
| 18:17 | EXMODE          | 0xX   | RW     | <b>Set GPIO Mode</b><br>GPIO mode for the excitation phase of the scan sequence. Note that DACOUT is only available on channels 4, 5, 7, 10, 12, 13<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>DISABLE</td> <td>Disabled</td> </tr> <tr> <td>1</td> <td>HIGH</td> <td>Push Pull, GPIO is driven high</td> </tr> <tr> <td>2</td> <td>LOW</td> <td>Push Pull, GPIO is driven low</td> </tr> <tr> <td>3</td> <td>DACOUT</td> <td>VDAC output</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | DISABLE | Disabled                       | 1 | HIGH     | Push Pull, GPIO is driven high   | 2 | LOW | Push Pull, GPIO is driven low | 3 | DACOUT | VDAC output |
| Value | Mode            | Description   |        |   |       |      |             |   |         |                                |   |          |                                  |   |     |                               |   |        |             |
| 0     | DISABLE         | Disabled  |        |   |       |      |             |   |         |                                |   |          |                                  |   |     |                               |   |        |             |
| 1     | HIGH            | Push Pull, GPIO is driven high  |        |   |       |      |             |   |         |                                |   |          |                                  |   |     |                               |   |        |             |
| 2     | LOW             | Push Pull, GPIO is driven low   |        |   |       |      |             |   |         |                                |   |          |                                  |   |     |                               |   |        |             |
| 3     | DACOUT          | VDAC output   |        |   |       |      |             |   |         |                                |   |          |                                  |   |     |                               |   |        |             |
| 16:14 | SETIF           | 0xX   | RW     | <b>Enable Interrupt Generation</b><br>Select interrupt generation mode for CHx interrupt flag.<br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> </tbody> </table>  | Value | Mode | Description |   |         |                                |   |          |                                  |   |     |                               |   |        |             |
| Value | Mode            | Description   |        |   |       |      |             |   |         |                                |   |          |                                  |   |     |                               |   |        |             |

| Bit   | Name   | Reset     | Access | Description   |
|-------|--------|-----------|--------|---|
|       | 0      | NONE      |        | No interrupt is generated   |
|       | 1      | LEVEL     |        | Set interrupt flag if the sensor triggers.  |
|       | 2      | POSEDGE   |        | Set interrupt flag on positive edge of the sensor state   |
|       | 3      | NEGEDGE   |        | Set interrupt flag on negative edge of the sensor state   |
|       | 4      | BOTHEDGES |        | Set interrupt flag on both edges of the sensor state  |
| 13:12 | SAMPLE | 0xX       | RW     | <b>Select Sample Mode</b><br>Select measurement to be used for evaluation                           |
|       | Value  | Mode      |        | Description   |
|       | 0      | ACMPCOUNT |        | Counter output will be used in evaluation   |
|       | 1      | ACMP      |        | ACMP output will be used in evaluation  |
|       | 2      | ADC       |        | ADC output will be used in evaluation   |
|       | 3      | ADCDIFF   |        | Differential ADC output will be used in evaluation  |
| 11:0  | THRES  | 0xXXX     | RW     | <b>ACMP Threshold or VDAC Data</b><br>Set threshold used for ACMP, or data used in VDAC conversion. |

### 29.5.30 LESENSE\_CHx\_EVAL - Scan Configuration (Async Reg)

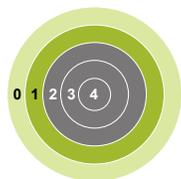
For more information about asynchronous registers see [4.3 Access to Low Energy Peripherals \(Asynchronous Registers\)](#).

| Offset        | Bit Position |    |    |    |    |    |    |    |    |      |            |    |           |        |      |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|------|------------|----|-----------|--------|------|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
|               | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22   | 21         | 20 | 19        | 18     | 17   | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| 0x248         |              |    |    |    |    |    |    |    |    |      |            |    |           |        |      |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    | 0xX  | X          |    | 0xX       | X      | X    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    | RW   | RW         |    | RW        | RW     | RW   |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    | MODE | SCANRESINV |    | STRSAMPLE | DECODE | COMP |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|               |              |    |    |    |    |    |    |    |    |      |            |    |           |        |      |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit   | Name       | Reset   | Access | Description   |
|-------|------------|---|--------|---|
| 31:23 | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 22:21 | MODE       | 0xX   | RW     | <b>Configure Evaluation Mode</b><br>Select which evaluation mode to be used on the measurement result   |
|       | Value      | Mode  |        | Description   |
|       | 0          | THRES   |        | Threshold comparison is used to evaluate sensor result  |
|       | 1          | SLIDINGWIN  |        | Sliding window is used to evaluate sensor result  |
|       | 2          | STEPDET   |        | Step detection is used to evaluate sensor result  |
| 20    | SCANRESINV | X   | RW     | <b>Enable Inversion of Result</b><br>If set, the bit stored in SCANRES will be inverted.  |
| 19:18 | STRSAMPLE  | 0xX   | RW     | <b>Enable Storing of Sensor Sample in Result Buffer</b><br>If set, the sensor sample value will be stored and available in the result buffer        |
|       | Value      | Mode  |        | Description   |
|       | 0          | DISABLE   |        | Nothing will be stored in the result buffer.  |
|       | 1          | DATA  |        | The sensor sample data will be stored in the result buffer.   |
|       | 2          | DATASRC   |        | The data source (i.e., the channel) will be stored alongside the sensor sample data.  |
| 17    | DECODE     | X   | RW     | <b>Send Result to Decoder</b><br>If set, the result from this channel will be shifted into the decoder register.                                    |
| 16    | COMP       | X   | RW     | <b>Select Mode for Threshold Comparison</b><br>Set compare mode for threshold comparisons (CHx_INTERACT_SAMPLE != ACMP and CHx_EVAL_MODE == THRES). |
|       | Value      | Mode  |        | Description   |
|       | 0          | LESS  |        | Comparison evaluates to 1 if sensor data is less than COMPTHRES.  |
|       | 1          | GE  |        | Comparison evaluates to 1 if sensor data is greater than or equal to COMPTHRES.   |

| Bit  | Name      | Reset | Access | Description   |
|------|-----------|-------|--------|---|
| 15:0 | COMPTHRES | 0XXXX | RWH    | <b>Decision Threshold for Sensor Data</b><br><br>In threshold comparison mode, this bitfield is used to configure threshold used for comparison. In step detection mode, this bitfield is written by LESENSE, and contains the value from previous sensor measurement. In sliding window mode, this bitfield is written by LESENSE, and contains the window base for the given channel. |

## 30. GPCRC - General Purpose Cyclic Redundancy Check



### Quick Facts

#### What?

The GPCRC is an error-detecting module commonly used in digital networks and storage systems to detect accidental changes to data.

#### Why?

The GPCRC module can detect errors in data, giving a higher system reliability and robustness.

#### How?

Blocks of data entering GPCRC module can have a short checksum, based on the remainder of a polynomial division of their contents; on retrieval the calculation is repeated, and corrective action can be taken against presumed data corruption if the check values do not match.

### 30.1 Introduction

The GPCRC module is a slave peripheral that implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7(IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application. Common 16-bit polynomials are 0x1021 (CCITT-16), 0x3D65 (IEC16-MBus), and 0x8005 (zigbee, 802.15.4, and USB).

### 30.2 Features

- Programmable 16-bit polynomial, fixed 32-bit polynomial
- Byte-level bit reversal for the CRC input
- Byte-order reorientation for the CRC input
- Word or half-word bit reversal of the CRC result
- Ability to configure and seed an operation in a single register write
- Single-cycle CRC computation for 32-, 16-, or 8-bit blocks
- DMA operation

### 30.3 Functional Description

An overview of the GPCRC module is shown in [Figure 30.1 GPCRC Overview on page 1038](#).

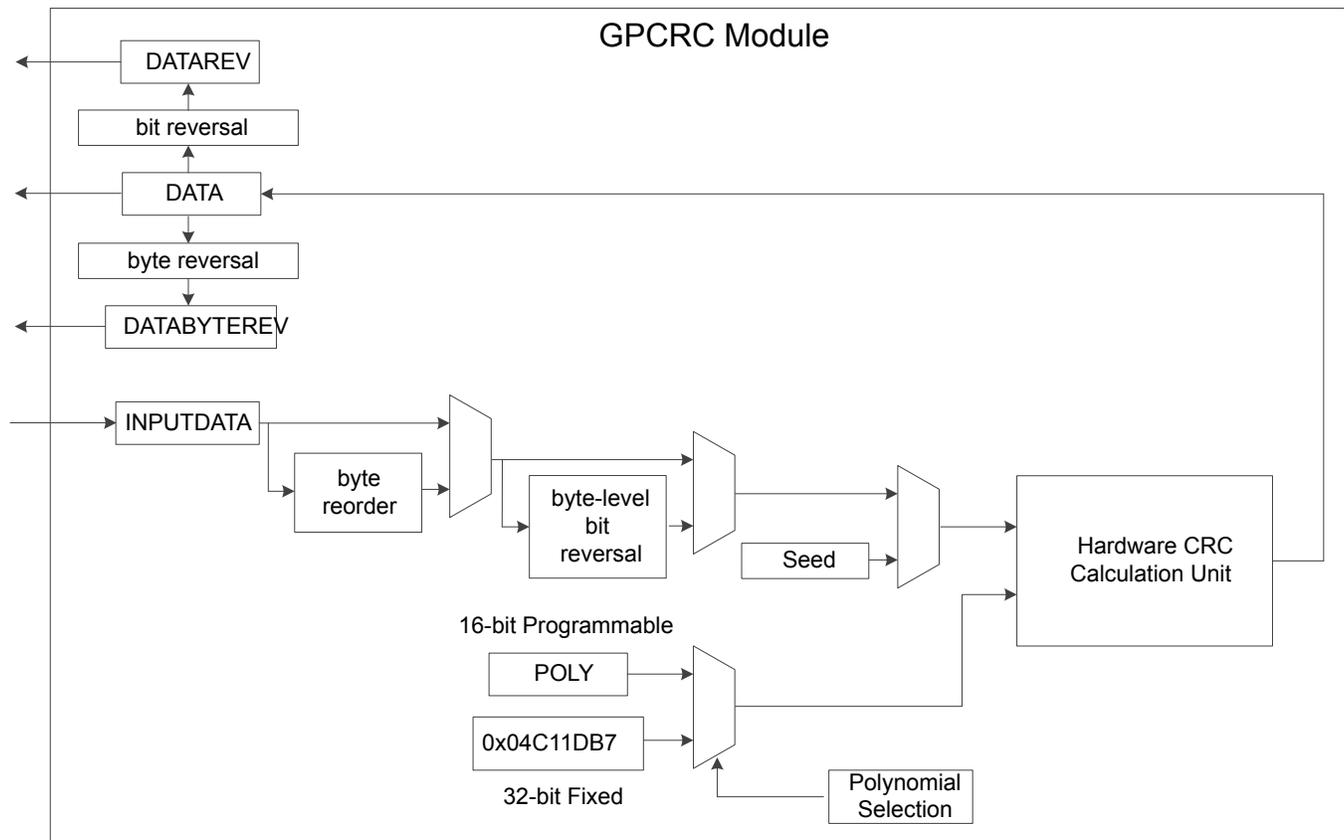


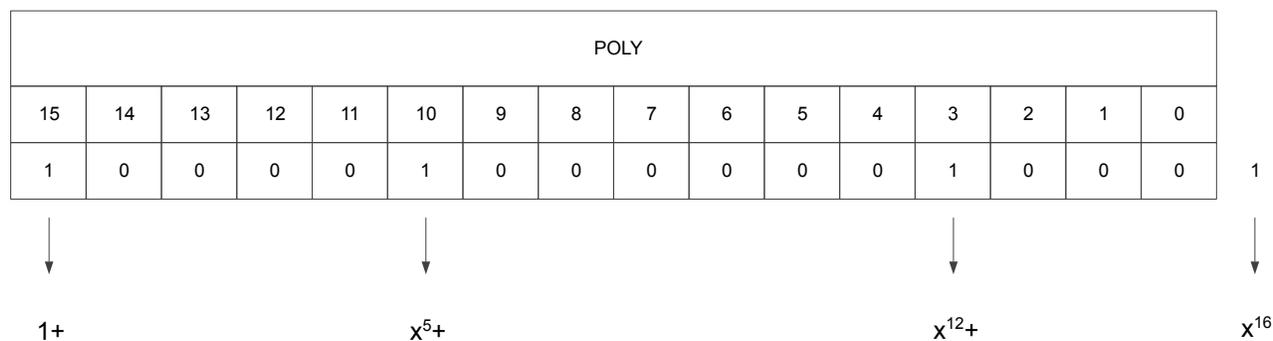
Figure 30.1. GPCRC Overview

### 30.3.1 Polynomial Specification

POLYSEL in GPCRC\_CTRL selects between 32-bit and 16-bit polynomial functions. When a 32-bit polynomial is selected, the fixed IEEE 802.3 polynomial(0x04C11DB7) is used. When a 16-bit polynomial is selected, any valid polynomial can be defined by the user in GPCRC\_POLY.

A valid 16-bit CRC polynomial must have an  $x^{16}$  term and an  $x^0$  term. Theoretically, a 16-bit polynomial has 17 terms total. The convention used is to omit the  $x^{16}$  term. The polynomial should be written in **reversed** (little endian) bit order. The most significant bit corresponds to the lowest order term. Thus, the most significant bit in CRC\_POLY represents the  $x^0$  term, and the least significant bit in CRC\_POLY represents the  $x^{15}$  term. The highest significant bit of CRC\_POLY should always set to 1. The polynomial representation for the CRC-16-CCIT polynomial  $x^{16} + x^{12} + x^5 + 1$ , or 0x8408 in reversed order, is shown in [Figure 30.2 Polynomial Representation on page 1039](#).

CRC-16-CCITT Normal: 0x1021 Reversed: 0x8408



**Figure 30.2. Polynomial Representation**

### 30.3.2 Input and Output Specification

The CRC input data can be written to the GPCRC\_INPUTDATA, GPCRC\_INPUTDATAWORD or GPCRC\_INPUTDATABYTE register via the APB bus based on different data size. If BYTEMODE in GPCRC\_CTRL is set, only the least significant byte of the data word will be used for the CRC calculation no matter which input register is written. There are also three output registers for different ordering. Reading from GPCRC\_DATA will get the result based on the polynomial in reversed order, while reading from GPCRC\_DATAREV will get the result based on the polynomial in normal order. The CRC calculation needs one clock cycle, reading from GPCRC\_DATA, GPCRC\_DATAREV or GPCRC\_DATABYTEREV register or writing to GPCRC\_CMD register is halted while the calculation is in progress.

### 30.3.3 Initialization

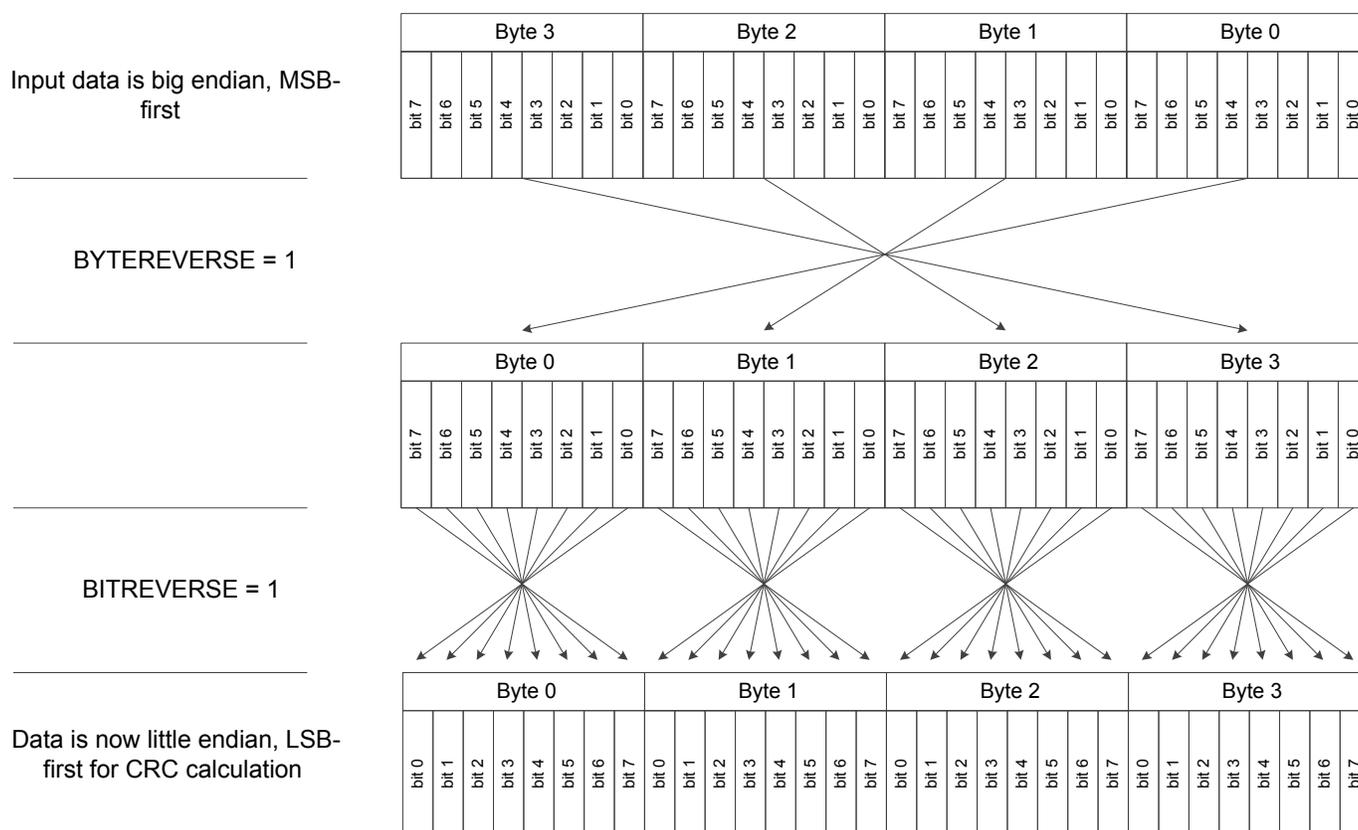
The CRC can be pre-loaded or re-initialized by first writing a 32-bit programmable init value to INIT in GPCRC\_INIT and then setting INIT in GPCRC\_CMD. It can also be re-initialized automatically when read from DATA, DATAREV or DATABYTEREV provided that AUTOINIT in GPCRC\_CTRL is set, the CRC would be re-initialized with the stored init value.

### 30.3.4 DMA Usage

A DMA channel may be used to transfer data into the CRC engine. All bytes and half-word writes must be word-aligned. The recommended DMA usage model is to use the DMA to transfer all available words of data and use software writes to capture any remaining bytes.

### 30.3.5 Byte-Level Bit Reversal and Byte Reordering

The byte-level bit reversal and byte reordering operations occur before the data is used in the CRC calculation. Byte reordering can occur on words or half words. The hardware ignores the BYTEREVERSE field with any byte writes or operations with byte mode enabled (BYTEMODE = 1), but the bit reversal settings (BITREVERSE) are still applied to the byte. 32-bit little endian MSB-first data can be treated like 32-bit little endian LSB-first data, as shown in [Figure 30.3 Data Ordering Example - 32-bit MSB -first to LSB-first on page 1040](#). In this example, 32-bit data is written to GPCRC\_INPUTDATA, BYTEREVERSE is set for byte ordering, and BITREVERSE is set for byte-level bit reversal.



**Figure 30.3. Data Ordering Example - 32-bit MSB -first to LSB-first**

When handling 16-bit data, the byte reordering function only swap the two lowest bytes and clear the two highest bytes, as shown in [Figure 30.4 Data Ordering Example - 16-bit MSB -first to LSB-first on page 1041](#). In this example, 16-bit data is written to GPCRC\_INPUTDATAWORD, BYTEREVERSE is set for byte ordering, and BITREVERSE is set for byte-level bit reversal.

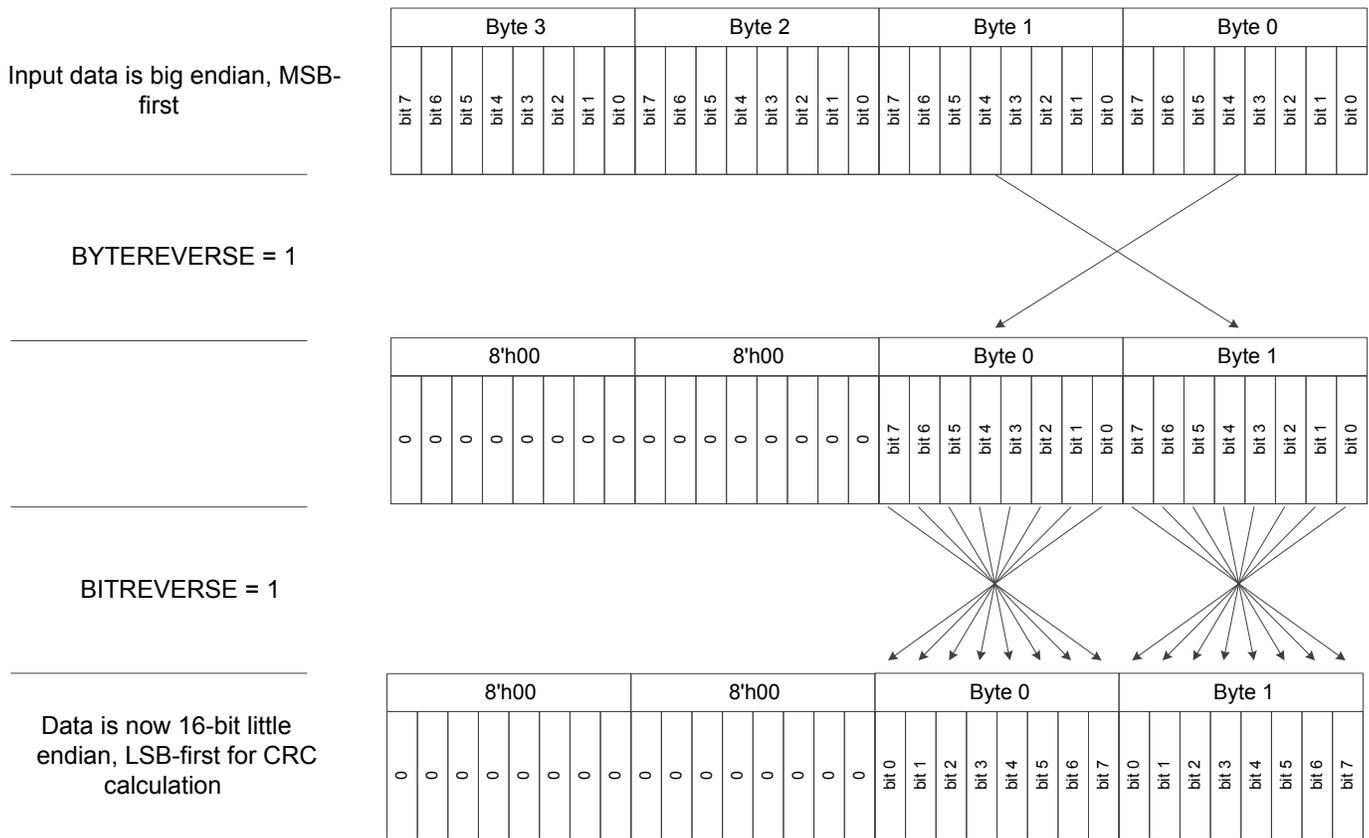


Figure 30.4. Data Ordering Example - 16-bit MSB -first to LSB-first

Assuming a word input byte order of B3 B2 B1 B0, the values used in the CRC calculation for the various settings of the byte-level bit reversal and byte reordering are shown in Table 30.1 Byte-Level Bit Reversal and Byte Reordering Results (B3 B2 B1 B0 Input Order) on page 1041.

Table 30.1. Byte-Level Bit Reversal and Byte Reordering Results (B3 B2 B1 B0 Input Order)

| Input Width(bits) | BYTEREVERSE Setting | BITREVERSE Setting | Input to CRC Calculation |
|-------------------|---------------------|--------------------|--------------------------|
| 32                | 0                   | 0                  | B3 B2 B1 B0              |
| 32                | 1                   | 1                  | 'B0 'B1 'B2 'B3          |
| 32                | 1                   | 0                  | B0 B1 B2 B3              |
| 32                | 0                   | 1                  | 'B3 'B2 'B1 'B0          |
| 16                | 0                   | 0                  | XX XX B1 B0              |
| 16                | 1                   | 1                  | XX XX 'B0 'B1            |
| 16                | 1                   | 0                  | XX XX B0 B1              |
| 16                | 0                   | 1                  | XX XX 'B1 'B0            |
| 8                 | -                   | 0                  | XX XX XX XX B0           |
| 8                 | -                   | 1                  | XX XX XX XX 'B0          |

| Input Width(bits)   | BYTEREVERSE Setting | BITREVERSE Setting | Input to CRC Calculation |
|---|---------------------|--------------------|--------------------------|
| <b>Note:</b> <ol style="list-style-type: none"> <li>1. X indicates a "don't care".</li> <li>2. Bn is the byte field within the word.</li> <li>3. 'Bn is the bit-reversed byte field within the word.</li> </ol> |                     |                    |                          |

### 30.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name                 | Type | Description                    |
|--------|----------------------|------|--------------------------------|
| 0x000  | GPCRC_CTRL           | RW   | Control Register               |
| 0x004  | GPCRC_CMD            | W1   | Command Register               |
| 0x008  | GPCRC_INIT           | RWH  | CRC Init Value                 |
| 0x00C  | GPCRC_POLY           | RW   | CRC Polynomial Value           |
| 0x010  | GPCRC_INPUTDATA      | W    | Input 32-bit Data Register     |
| 0x014  | GPCRC_INPUTDATAHWORD | W    | Input 16-bit Data Register     |
| 0x018  | GPCRC_INPUTDATABYTE  | W    | Input 8-bit Data Register      |
| 0x01C  | GPCRC_DATA           | R    | CRC Data Register              |
| 0x020  | GPCRC_DATAREV        | R    | CRC Data Reverse Register      |
| 0x024  | GPCRC_DATABYTEREV    | R    | CRC Data Byte Reverse Register |



| Bit | Name            | Reset   | Access   | Description   |
|-----|-----------------|---|--|---|
| 3:1 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |   |
| 0   | EN              | 0   | RW   | <b>CRC Functionality Enable</b><br>Enables CRC functionality. |
|     | Value           | Mode  | Description  |   |
|     | 0               | DISABLE   | Disable CRC function. Reordering function is available, only BITREVERSE and BYTEREVERSE bits are configurable in this mode |   |
|     | 1               | ENABLE  | Writes to inputdata registers result in CRC operations   |   |

### 30.5.2 GPCRC\_CMD - Command Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |      |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|------|
| 0x004         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0    |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0    |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | W1   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | INIT |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 31:1 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 0    | INIT            | 0   | W1     | <b>Initialization Enable</b><br>Writing 1 to this bit initialize the CRC by writing the INIT value in CRC_INIT to CRC_DATA. |

### 30.5.3 GPCRC\_INIT - CRC Init Value

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |            |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|------------|
| 0x008         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0          |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0x00000000 |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | RWH        |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | INIT       |

| Bit  | Name | Reset      | Access | Description  |
|------|------|------------|--------|--|
| 31:0 | INIT | 0x00000000 | RWH    | <b>CRC Initialization Value</b><br>This value is loaded into CRC_DATA upon issuing the INIT command in CRC_CMD |

### 30.5.4 GPCRC\_POLY - CRC Polynomial Value

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x00C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | POLY   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description   |
|-------|----------|--|--------|---|
| 31:16 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 15:0  | POLY     | 0x0000   | RW     | <b>CRC Polynomial Value</b><br><br>This value defines 16-bit POLY, which is used as the polynomial during the 16-bit CRC calculation. The polynomial is defined in reversed representation, meaning that the lowest degree term is in the highest bit position of POLY. Additionally, the highest degree term in the polynomial is implicit. Further examples of the CRC configuration can be found in the documentation. |

### 30.5.5 GPCRC\_INPUTDATA - Input 32-bit Data Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x010         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | INPUTDATA  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name      | Reset      | Access | Description  |
|------|-----------|------------|--------|--|
| 31:0 | INPUTDATA | 0x00000000 | W      | <b>Input Data for 32-bit</b><br><br>CRC Input 32-bit Data can be written to this register. Each time this register is written, the CRC value is updated. |

## 30.5.6 GPCRC\_INPUTDATAWORD - Input 16-bit Data Register

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x014  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Access |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Name   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | INPUTDATAWORD |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name          | Reset   | Access | Description  |
|-------|---------------|---|--------|--|
| 31:16 | Reserved      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 15:0  | INPUTDATAWORD | 0x0000  | W      | <b>Input Data for 16-bit</b><br>CRC Input 16-bit Data can be written to this register. Each time this register is written, the CRC value is updated. |

## 30.5.7 GPCRC\_INPUTDATABYTE - Input 8-bit Data Register

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x018  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Access |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Name   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | INPUTDATABYTE |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name          | Reset   | Access | Description  |
|------|---------------|---|--------|--|
| 31:8 | Reserved      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 7:0  | INPUTDATABYTE | 0x00  | W      | <b>Input Data for 8-bit</b><br>CRC Input 8-bit Data can be written to this register. Each time this register is written, the CRC value is updated. |

**30.5.8 GPCRC\_DATA - CRC Data Register**

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x01C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DATA       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name | Reset      | Access | Description              |
|---|------|------------|--------|--------------------------|
| 31:0  | DATA | 0x00000000 | R      | <b>CRC Data Register</b> |
| CRC Data Register, read only. The CRC data register may still be indirectly written from software, by writing the INIT register and then issue an INITIALIZE command. |      |            |        |                          |

**30.5.9 GPCRC\_DATAREV - CRC Data Reverse Register**

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x020         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DATAREV    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

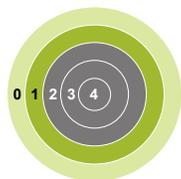
| Bit   | Name    | Reset      | Access | Description               |
|---|---------|------------|--------|---------------------------|
| 31:0  | DATAREV | 0x00000000 | R      | <b>Data Reverse Value</b> |
| Bit reversed version of CRC Data register. When a 32-bit CRC polynomial is selected, the reversal occurs on the entire 32-bit word. When a 16-bit CRC polynomial is selected, the bits [15:0] are reversed. |         |            |        |                           |

## 30.5.10 GPCRC\_DATABYTEREV - CRC Data Byte Reverse Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x024         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R           |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DATABYTEREV |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name        | Reset      | Access | Description   |
|------|-------------|------------|--------|---|
| 31:0 | DATABYTEREV | 0x00000000 | R      | <b>Data Byte Reverse Value</b><br>Byte reversed version of CRC Data register. When a 32-bit CRC polynomial is selected, the bytes are swizzled to {B0, B1, B2, B3}. When a 16-bit CRC polynomial is selected, the bytes are swizzled to {0, 0, B0, B1}. |

## 31. TRNG - True Random Number Generator



### Quick Facts

#### What?

The TRNG module is a non-deterministic random number generator based on a full hardware solution.

#### Why?

Secure cryptography commonly relies on randomly-generated numbers for key generation. Software solutions for random number generation do not usually produce results with enough entropy to satisfy existing standards. Dedicated hardware can provide suitable entropy in an energy-efficient, non-intrusive manner, while also relieving software burden.

#### How?

Ring oscillators and sampling logic combine to produce non-deterministic random numbers.

### 31.1 Introduction

The TRNG module is a non-deterministic random number generator based on a full hardware solution. The TRNG output passes the NIST 800-22 and AIS31 test suites.

### 31.2 Features

- Simple bus interface to access random numbers, control, and status registers
- 64 x 32-bit FIFO for random number access
- Interrupt sources from different FIFO, error, and noise alarm events
- Passes NIST 800-22 and AIS31
- Ready for NIST 800-90B
- Health tests compliant to NIST 800-90B and AIS31

### 31.3 Functional Description

Software drivers provided by Silicon Labs offer a simple API interface to the TRNG module. It is highly recommended to use the provided software libraries to access the TRNG module. An overview of the TRNG module is shown in [Figure 31.1 TRNG Overview on page 1050](#).

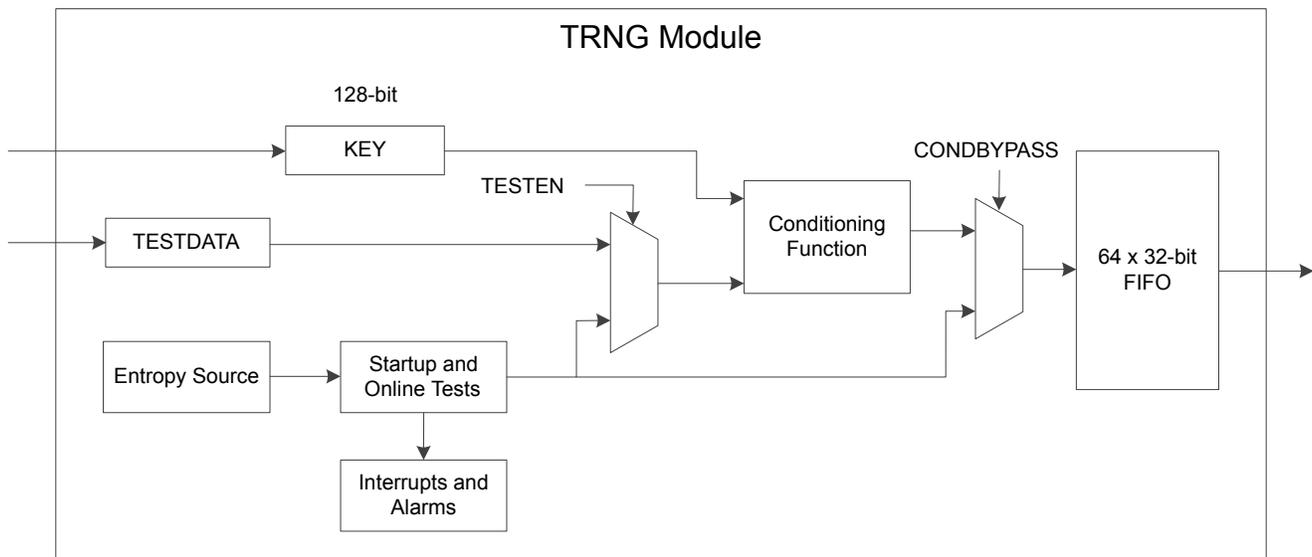


Figure 31.1. TRNG Overview

#### 31.3.1 Built-In Tests

The TRNG module includes several built-in tests to detect issues with the noise source, ensure entropy, and meet cryptography standards. The Repetition Count Test and Adaptive Proportion Test with window sizes of 64 and 4096 bits described in section 6.5.1.2 of NIST-800-90B (<http://csrc.nist.gov/publications/drafts/800-90/draft-sp800-90b.pdf>) are implemented in hardware and run continuously on the data. All three tests have corresponding interrupt flags that can optionally be used to generate a system interrupt.

The AIS31 Online Test described in section 5.5.3 of [https://www.bsi.bund.de/SharedDocs/Downloads/DE/BSI/Zertifizierung/Interpretationen/AIS\\_31\\_Functionality\\_classes\\_for\\_random\\_number\\_generators\\_e.pdf](https://www.bsi.bund.de/SharedDocs/Downloads/DE/BSI/Zertifizierung/Interpretationen/AIS_31_Functionality_classes_for_random_number_generators_e.pdf) is also implemented in hardware, and runs continuously on the data. Both the preliminary noise alarm and the noise alarm are optionally available as interrupt sources from the TRNG module. If a noise alarm occurs, the TRNG will be shut down, and must be reset with a software reset.

Additionally, the NIST-800-90B and AIS31 startup tests may be optionally enabled or disabled by software. The NIST-800-90B startup test is enabled if the CONTROL\_BYPNIST bit is cleared to 0. The AIS31 startup test is likewise enabled when CONTROL\_BYPAIS31 is cleared to 0. If either the NIST-800-90B or AIS31 startup tests are enabled, no data will be written to the output FIFO until the startup requirements for these tests pass.

#### 31.3.2 FIFO Interface

The TRNG module includes a 64-word output FIFO to hold the output data as it becomes available. The number of 32-bit words available in the FIFO may be checked at any time by reading the FIFOLEVEL register. When the FIFO is completely filled, the TRNG will be shut down, the STATUS\_FULLIF flag will be set, and no further data will be written to the FIFO until the FIFO has been flushed. Data may be read from the FIFO one word (32-bits) at a time via the FIFO register. The STATUS\_FULLIF flag is cleared upon reading the FIFOLEVEL register.

### 31.3.3 Data Format - Byte Ordering

All cryptographic data is handled following the big-endian format (AES standard). The first byte (lowest address) of the data is the Most Significant Byte (MSB). However, the bus interfaces on the core use little endian format for internal byte ordering within a 32-bit word. The Least Significant Byte (LSB) within a word is stored at the lowest address.

For example, a 128-bit block 0x00112233445566778899AABBCCDDEEFF is read from the FIFO in the following order:

Word 1 = 0x33221100

Word 2 = 0x77665544

Word 3 = 0xBBAA9988

Word 4 = 0xFFDDEECC

This is important to note when checking the conditioning function for validity. The KEY registers also follow this standard, with KEY0 holding the MSB of a 128-bit value and KEY3 holding the LSB.

### 31.3.4 TRNG Usage

It is highly recommended to use the software libraries provided by Silicon Labs to access the TRNG module. The information in the following sections are reference for users who choose to write their own low-level software drivers.

### 31.3.4.1 Checking the Conditioning Function

The conditioning function receives 512 bits from the entropy source and generates 128 bits of output. The conditioning function can be tested by writing a known key and known data into the block with test mode enabled, then validating against the expected output. The sequence of operations to test the conditioning function is as follows:

1. Apply a software reset by setting CONTROL\_SOFTRESET to 1, then clearing it to 0.
2. Configure the CONTROL register. Important configuration options include:
  - Enable test mode by setting CONTROL\_TESTEN to 1.
  - Ensure the conditioning function is used by clearing CONTROL\_CONDBYPASS to 0.
3. Write the key into registers KEY0, KEY1, KEY2, and KEY3.
4. Write the 512 bits of known data to TESTDATA 32 bits at a time, polling for STATUS\_TESTDATABUSY = 0 after each write.
5. Read the 128-bit result from the FIFO 32 bits at a time.

Table 31.1 Known-Answer Test for Conditioning Function on page 1052 shows an example with a given key, known data input, and expected output (taken from section F.2.1 in <http://csrc.nist.gov/publications/nistpubs/800-38a/sp800-38a.pdf>).

**Table 31.1. Known-Answer Test for Conditioning Function**

|                 | 128-bit Format   | 32-bit Bus Format  |
|-----------------|--|--|
| Key             | 0x2B7E151628AED2A6ABF7158809CF4F3C   | 0x16157E2B<br>0xA6D2AE28<br>0x8815F7AB<br>0x3C4FCF09   |
| Input           | 0x6BC0BCE12A459991E134741A7F9E1925<br><br>0xAE2D8A571E03AC9C9EB76FAC45AF8E51<br><br>0x30C81C46A35CE411E5FBC1191A0A52EF<br><br>0xF69F2445DF4F9B17AD2B417BE66C3710 | 0xE1BCC06B<br>0x9199452A<br>0x1A7434E1<br>0x25199E7F<br>0x578A2DAE<br>0x9CAC031E<br>0xAC6FB79E<br>0x518EAF45<br>0x461CC830<br>0x11E45CA3<br>0x19C1FBE5<br>0xEF520A1A<br>0x45249FF6<br>0x179B4FDF<br>0x7B412BAD<br>0x10376CE6 |
| Expected output | 0x3FF1CAA1681FAC09120ECA307586E1A7   | 0xA1CAF13F<br>0x09AC1F68<br>0x30CA0E12<br>0xA7E18675   |

### 31.3.4.2 Checking the Entropy Source

The entropy source may be checked using the three built in test sources: repetition count, 64-sample adaptive proportion, and 4096-sample adaptive proportion. The entropy source may be tested using the following sequence:

1. Apply a software reset by setting CONTROL\_SOFTRESET to 1, then clearing it to 0.
2. Configure the CONTROL register. Important configuration options include:
  - Disable test mode by clearing CONTROL\_TESTEN to 0.
  - Bypass the conditioning function by setting CONTROL\_CONDBYPASS to 1.
  - Enable the TRNG by setting CONTROL\_ENABLE to 1.
3. Check the FIFOLEVEL register to monitor the amount of generated random numbers or wait for the STATUS\_FULLIF flag to set, indicating the FIFO is full. Note that STATUS\_FULLIF may be configured to generate an interrupt if desired.
4. When FIFOLEVEL has reached the expected value or when STATUS\_FULLIF is set, read the random numbers using the FIFO register. Those values can be discarded.
5. Continue reading and discarding the random data until at least 4097 x 2 bits (257 x 32-bit words) have been read. This ensures that enough time has passed for the longest test to run.
6. Check the STATUS register for error flags.

### 31.3.4.3 Programming a Random Key

1. Check the FIFOLEVEL register to monitor the amount of generated random numbers or wait for the STATUS\_FULLIF flag to set, indicating the FIFO is full. Note that STATUS\_FULLIF may be configured to generate an interrupt if desired.
2. When FIFOLEVEL has reached the expected value or when STATUS\_FULLIF is set, read the random numbers using the FIFO register.
3. Use four 32-bit random values to program a random key to the KEY0, KEY1, KEY2, and KEY3 registers.
4. Apply a software reset by setting CONTROL\_SOFTRESET to 1, then clearing it to 0. This will flush the FIFO data.

### 31.3.4.4 Reading Samples

1. Check the FIFOLEVEL register to monitor the amount of generated random numbers or wait for the STATUS\_FULLIF flag to set, indicating the FIFO is full. Note that STATUS\_FULLIF may be configured to generate an interrupt if desired.
2. When FIFOLEVEL has reached the expected value or when STATUS\_FULLIF is set, read the random numbers using the FIFO register.

## 31.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name              | Type | Description           |
|--------|-------------------|------|-----------------------|
| 0x000  | TRNGn_CONTROL     | RW   | Main Control Register |
| 0x004  | TRNGn_FIFOLEVEL   | R(a) | FIFO Level Register   |
| 0x00C  | TRNGn_FIFODEPTH   | R    | FIFO Depth Register   |
| 0x010  | TRNGn_KEY0        | RW   | Key Register 0        |
| 0x014  | TRNGn_KEY1        | RW   | Key Register 1        |
| 0x018  | TRNGn_KEY2        | RW   | Key Register 2        |
| 0x01C  | TRNGn_KEY3        | RW   | Key Register 3        |
| 0x020  | TRNGn_TESTDATA    | RW   | Test Data Register    |
| 0x030  | TRNGn_STATUS      | RWH  | Status Register       |
| 0x034  | TRNGn_INITWAITVAL | RW   | Initial Wait Counter  |
| 0x100  | TRNGn_FIFO        | R(a) | FIFO Data             |

### 31.5 Register Description

#### 31.5.1 TRNGn\_CONTROL - Main Control Register

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |         |          |        |        |           |         |            |          |             |            |        |    |    |    |    |    |    |    |    |        |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|---------|----------|--------|--------|-----------|---------|------------|----------|-------------|------------|--------|----|----|----|----|----|----|----|----|--------|
| 0x000  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13       | 12      | 11       | 10     | 9      | 8         | 7       | 6          | 5        | 4           | 3          | 2      | 1  | 0  |    |    |    |    |    |    |        |
| Reset  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0        | 0       | 0        | 0      | 0      | 0         | 0       | 0          | 0        | 0           | 0          | 0      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |        |
| Access |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW       | RW      | RW       | RW     | RW     | RW        | RW      | RW         | RW       | RW          | RW         | RW     | RW | RW | RW | RW | RW | RW | RW | RW |        |
| Name   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | BYPAIS31 | BYPNIST | FORCERUN | ALMIEN | PREIEN | SOFTRESET | FULLIEN | APT4096IEN | APT64IEN | REPCOUNTIEN | CONDBYPASS | TESTEN |    |    |    |    |    |    |    |    | ENABLE |

| Bit   | Name      | Reset   | Access | Description  |       |      |             |   |        |  |   |        |  |
|-------|-----------|---|--------|--|-------|------|-------------|---|--------|--|---|--------|--|
| 31:14 | Reserved  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |        |  |   |        |  |
| 13    | BYPAIS31  | 0   | RW     | <b>AIS31 Start-up Test Bypass.</b><br>Bypass for AIS31 startup test.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>NORMAL</td> <td>AIS31 startup test is applied. No data will be written to the FIFO until the test passes.</td> </tr> <tr> <td>1</td> <td>BYPASS</td> <td>AIS31 startup test is bypassed.</td> </tr> </tbody> </table>                     | Value | Mode | Description | 0 | NORMAL | AIS31 startup test is applied. No data will be written to the FIFO until the test passes.        | 1 | BYPASS | AIS31 startup test is bypassed.                          |
| Value | Mode      | Description   |        |  |       |      |             |   |        |  |   |        |  |
| 0     | NORMAL    | AIS31 startup test is applied. No data will be written to the FIFO until the test passes.                                       |        |  |       |      |             |   |        |  |   |        |  |
| 1     | BYPASS    | AIS31 startup test is bypassed.   |        |  |       |      |             |   |        |  |   |        |  |
| 12    | BYPNIST   | 0   | RW     | <b>NIST Start-up Test Bypass.</b><br>Bypass for NIST-800-90B startup test.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>NORMAL</td> <td>NIST-800-90B startup test is applied. No data will be written to the FIFO until the test passes.</td> </tr> <tr> <td>1</td> <td>BYPASS</td> <td>NIST-800-90B startup test is bypassed.</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | NORMAL | NIST-800-90B startup test is applied. No data will be written to the FIFO until the test passes. | 1 | BYPASS | NIST-800-90B startup test is bypassed.                   |
| Value | Mode      | Description   |        |  |       |      |             |   |        |  |   |        |  |
| 0     | NORMAL    | NIST-800-90B startup test is applied. No data will be written to the FIFO until the test passes.                                |        |  |       |      |             |   |        |  |   |        |  |
| 1     | BYPASS    | NIST-800-90B startup test is bypassed.  |        |  |       |      |             |   |        |  |   |        |  |
| 11    | FORCERUN  | 0   | RW     | <b>Oscillator Force Run</b><br>Set this bit to force oscillators to run even when FIFO is full.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>NORMAL</td> <td>Oscillators will shut down when FIFO is full</td> </tr> <tr> <td>1</td> <td>RUN</td> <td>Oscillators will continue to run even after FIFO is full</td> </tr> </tbody> </table>                 | Value | Mode | Description | 0 | NORMAL | Oscillators will shut down when FIFO is full   | 1 | RUN    | Oscillators will continue to run even after FIFO is full |
| Value | Mode      | Description   |        |  |       |      |             |   |        |  |   |        |  |
| 0     | NORMAL    | Oscillators will shut down when FIFO is full  |        |  |       |      |             |   |        |  |   |        |  |
| 1     | RUN       | Oscillators will continue to run even after FIFO is full  |        |  |       |      |             |   |        |  |   |        |  |
| 10    | ALMIEN    | 0   | RW     | <b>Interrupt enable for AIS31 noise alarm</b><br>Enable/disable AIS31 noise alarm interrupt.   |       |      |             |   |        |  |   |        |  |
| 9     | PREIEN    | 0   | RW     | <b>Interrupt enable for AIS31 preliminary noise alarm</b><br>Enable/disable AIS31 preliminary noise alarm interrupt.   |       |      |             |   |        |  |   |        |  |
| 8     | SOFTRESET | 0   | RW     | <b>Software Reset</b><br>Set to reset the module. This bit is not cleared automatically.   |       |      |             |   |        |  |   |        |  |

| Bit | Name            | Reset   | Access | Description   |
|-----|-----------------|---|--------|---|
|     | Value           | Mode  |        | Description   |
|     | 0               | NORMAL  |        | Module not in reset   |
|     | 1               | RESET   |        | The continuous test, the conditioning function and the FIFO are reset   |
| 7   | FULLIEN         | 0   | RW     | <b>Interrupt Enable for FIFO Full</b><br>Enable/Disable FIFO full interrupt.  |
| 6   | APT4096IEN      | 0   | RW     | <b>Interrupt Enable for Adaptive Proportion Test Failure (4096-sample Window)</b><br>Enable/Disable 4096-sample Adaptive Proportion test failure interrupt. |
| 5   | APT64IEN        | 0   | RW     | <b>Interrupt Enable for Adaptive Proportion Test Failure (64-sample Window)</b><br>Enable/Disable 64-sample Adaptive Proportion test failure interrupt.     |
| 4   | REPCOUNTIEN     | 0   | RW     | <b>Interrupt Enable for Repetition Count Test Failure</b><br>Enable/Disable Repetition Count Test failure interrupt.  |
| 3   | CONDBYPASS      | 0   | RW     | <b>Conditioning Bypass</b><br>Enables bypassing of the conditioning function (to observe entropy source directly).  |
|     | Value           | Mode  |        | Description   |
|     | 0               | NORMAL  |        | The conditionig function is used  |
|     | 1               | BYPASS  |        | The conditioning function is bypassed   |
| 2   | TESTEN          | 0   | RW     | <b>Test Enable</b><br>Selects the input for the conditioning function and continuous tests.   |
|     | Value           | Mode  |        | Description   |
|     | 0               | NOISE   |        | Non-deterministic random number generation  |
|     | 1               | TESTDATA  |        | Pseudo-random number generation   |
| 1   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 0   | ENABLE          | 0   | RW     | <b>TRNG Module Enable</b><br>Enable the TRNG. The module will generate random numbers unless the FIFO is full.  |
|     | Value           | Mode  |        | Description   |
|     | 0               | DISABLED  |        | Module disabled   |
|     | 1               | ENABLED   |        | Module enabled  |

### 31.5.2 TRNGn\_FIFOLEVEL - FIFO Level Register (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x004         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | VALUE      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit  | Name  | Reset      | Access | Description   |
|------|-------|------------|--------|---|
| 31:0 | VALUE | 0x00000000 | R      | <b>FIFO Level</b><br><br>Number of 32-bit words of random data available in the FIFO. The STATUS_FULLIF flag is cleared when FIFOLEVEL is read. |

### 31.5.3 TRNGn\_FIFODEPTH - FIFO Depth Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x00C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000040 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | VALUE      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit  | Name  | Reset      | Access | Description  |
|------|-------|------------|--------|--|
| 31:0 | VALUE | 0x00000040 | R      | <b>FIFO Depth.</b><br><br>Maximum number of 32-bit words that can be stored in the FIFO. |

### 31.5.4 TRNGn\_KEY0 - Key Register 0

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x010         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | VALUE      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit  | Name  | Reset      | Access | Description                                      |
|------|-------|------------|--------|--|
| 31:0 | VALUE | 0x00000000 | RW     | <b>Key 0</b><br>AES Key 32-bit sub-word 0 (MSB). |

### 31.5.5 TRNGn\_KEY1 - Key Register 1

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x014         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | VALUE      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit  | Name  | Reset      | Access | Description                                |
|------|-------|------------|--------|--|
| 31:0 | VALUE | 0x00000000 | RW     | <b>Key 1</b><br>AES Key 32-bit sub-word 1. |

### 31.5.6 TRNGn\_KEY2 - Key Register 2

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x018         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | VALUE      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit  | Name  | Reset      | Access | Description                                |
|------|-------|------------|--------|--|
| 31:0 | VALUE | 0x00000000 | RW     | <b>Key 2</b><br>AES Key 32-bit sub-word 2. |

### 31.5.7 TRNGn\_KEY3 - Key Register 3

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x01C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | VALUE      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit  | Name  | Reset      | Access | Description                                      |
|------|-------|------------|--------|--|
| 31:0 | VALUE | 0x00000000 | RW     | <b>Key 3</b><br>AES Key 32-bit sub-word 3 (LSB). |

### 31.5.8 TRNGn\_TESTDATA - Test Data Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x020         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | VALUE      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit  | Name  | Reset      | Access | Description  |
|------|-------|------------|--------|--|
| 31:0 | VALUE | 0x00000000 | RW     | <b>Test data input to conditioning function or to the continuous tests</b><br><br>Each word written to this register represents 32 bits of input data for the selected test in test mode (CONTROL_TESTEN = 1). TESTDATABUSY in the STATUS register will be set to 1 each time data is written, and will clear to 0 when the next data word can be written. Writes to this register are ignored if the TESTEN bit in the CONTROL register is 0. |

### 31.5.9 TRNGn\_STATUS - Status Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |       |       |        |           |         |            |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |              |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------|-------|--------|-----------|---------|------------|---|---|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------|
| 0x030         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9     | 8     | 7      | 6         | 5       | 4          | 3 | 2 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |              |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0     | 0     | 0      | 0         | 0       |            |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0            |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R     | RWH   | R      | R         | R       |            |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | R            |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | ALMIF | PREIF | FULLIF | APT4096IF | APT64IF | REPCOUNTIF |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TESTDATABUSY |

| Bit   | Name            | Reset   | Access  | Description  |
|-------|-----------------|---|---|--|
| 31:10 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 9     | ALMIF           | 0   | R   | <b>AIS31 Noise Alarm interrupt status</b><br>Set when a noise alarm is detected in the AIS31 online test.  |
| 8     | PREIF           | 0   | RWH   | <b>AIS31 Preliminary Noise Alarm interrupt status</b><br>Set when a preliminary noise alarm is detected in the AIS31 online test.                          |
| 7     | FULLIF          | 0   | R   | <b>FIFO Full Interrupt Status</b><br>Set when the FIFO is full. The STATUS_FULLIF flag is cleared by reading FIFOLEVEL.                                    |
| 6     | APT4096IF       | 0   | R   | <b>Adaptive Proportion test failure (4096-sample window) interrupt status</b><br>Set when an Adaptive Proportion test (4096-sample window) failure occurs. |
| 5     | APT64IF         | 0   | R   | <b>Adaptive Proportion test failure (64-sample window) interrupt status</b><br>Set when an Adaptive Proportion test (64-sample window) failure occurs.     |
| 4     | REPCOUNTIF      | 0   | R   | <b>Repetition Count Test Interrupt Status</b><br>Set when a Repetition Count Test failure occurs.  |
| 3:1   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 0     | TESTDATABUSY    | 0   | R   | <b>Test Data Busy</b><br>Indicates that data written to TESTDATA is being processed.   |
|       | <b>Value</b>    | <b>Mode</b>   | <b>Description</b>  |  |
|       | 0               | IDLE  | TESTDATA write is finished processing or no test in progress. |  |
|       | 1               | BUSY  | TESTDATA write is still being processed.                      |  |

### 31.5.10 TRNGn\_INITWAITVAL - Initial Wait Counter

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |       |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|-------|---|---|---|---|---|---|---|
| 0x034         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7     | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0xFF  |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RW    |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | VALUE |   |   |   |   |   |   |   |

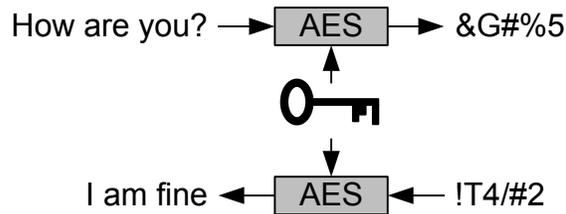
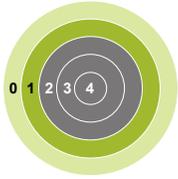
| Bit  | Name     | Reset  | Access | Description   |
|------|----------|--|--------|---|
| 31:8 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 7:0  | VALUE    | 0xFF   | RW     | <b>Wait counter value</b><br>Number of clock cycles to wait before sampling data from the noise source. |

### 31.5.11 TRNGn\_FIFO - FIFO Data (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x100         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | VALUE      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name  | Reset      | Access | Description  |
|------|-------|------------|--------|--|
| 31:0 | VALUE | 0x00000000 | R      | <b>FIFO Read Data</b><br>Data may be read from the FIFO 32 bits at a time using this register. |

## 32. CRYPTO - Crypto Accelerator



### Quick Facts

#### What?

A fast and energy efficient autonomous hardware accelerator for AES encryption and decryption with 128- or 256-bit keys, ECC over prime and binary Galois finite fields, SHA-1, SHA-224 and SHA-256.

#### Why?

Efficient cryptography with little or no CPU intervention helps to meet the speed and energy demands of the application. Hardware implementations are generally more secure against side-channel attacks than software implementations.

#### How?

Programmable sequences of instructions on big numbers allow fast processing with little CPU intervention. Furthermore, CRYPTO is linked to the Buffer Controller (BUFC), thus enabling fast and efficient autonomous cipher operations on data buffer content.

### 32.1 Introduction

The CRYPTO module allows efficient acceleration of common cryptographic operations and allows these to be used efficiently with a low CPU load. Operations performed by CRYPTO can be set up as a sequence of instructions on a set of 128-bit, 256-bit or 512-bit registers to implement or accelerate Elliptic Curve Cryptography (ECC), SHA-1, SHA-224, SHA-256, and various block cipher modes based on the Advanced Encryption Standard, also known as AES (FIPS-197).

CRYPTO is capable of autonomously fetching data, performing cipher operations and storing data across multiple blocks. When the source data is not a multiple of 16 bytes (128 bits), Zero-padding can be included in the last block. Block operations such as Counter Mode (CTR), Electronic Code Book (ECB), Cipher Block Chaining (CBC), Cipher Feedback (CFB) and Output Feedback (OFB) are easily implemented. Block Cipher modes of operation such as Electronic Code Book (ECB), Counter Mode (CTR), Cipher Block Chaining (CBC), CBC-MAC (CBC Message Authentication Code), CCM (Counter with CBC-MAC) and GCM (Galois Counter mode) are easily implemented.

CRYPTO is delivered with an extensive software library in Simplicity Studio that implements all major cryptographic algorithms, including but not limited to AES, SHA-1, SHA-2, ECC, and legacy algorithms DES, 3DES, MD4, MD5 and RC4. The implementation accelerates the algorithms using CRYPTO when possible.

## 32.2 Features

- Efficient AES core
  - Encryption/decryption using 128-bit key (54 clock cycles) or 256-bit key (75 clock cycles)
  - Key buffer
  - Supports autonomous cipher block modes (e.g. ECB, CTR, CBC, PCBC, CFB, CBC-MAC, GMAC, CCM, CCM\* and GCM) across multiple blocks
- Accelerated SHA-1, SHA-224 and SHA-256
- Accelerated Elliptic Curve Cryptography (ECC)
  - Binary and Prime fields
  - Supports NIST recommended curves: P-192, P-224, P-256, K-163, K-233, B-163, and B-233
- Galois/Counter Mode (GCM)
  - ALU operations on GCM  $GF(2^{128})$  field
- Flexible 256-bit ALU and sequencer
  - 5 general purpose 256-bit registers
  - Supports ADD, SUB, MUL, shift, XOR, etc.
  - Up to 20 instructions can be chained to implement various block cipher modes
- Efficient operation
  - Automatic data loading and storing from registers (through BUFC, the buffer controller)
  - DMA request signals for data read and write
  - Optional XOR Data write
  - Interrupt on finished operations
- Extensive software support
  - Extensive software library in Simplicity Studio
  - Implements all major cryptographic algorithms: AES, SHA-1, SHA-2, and ECC
  - Implements legacy algorithms: DES, 3DES, MD4, MD5, and RC4
  - Hardware accelerated when possible

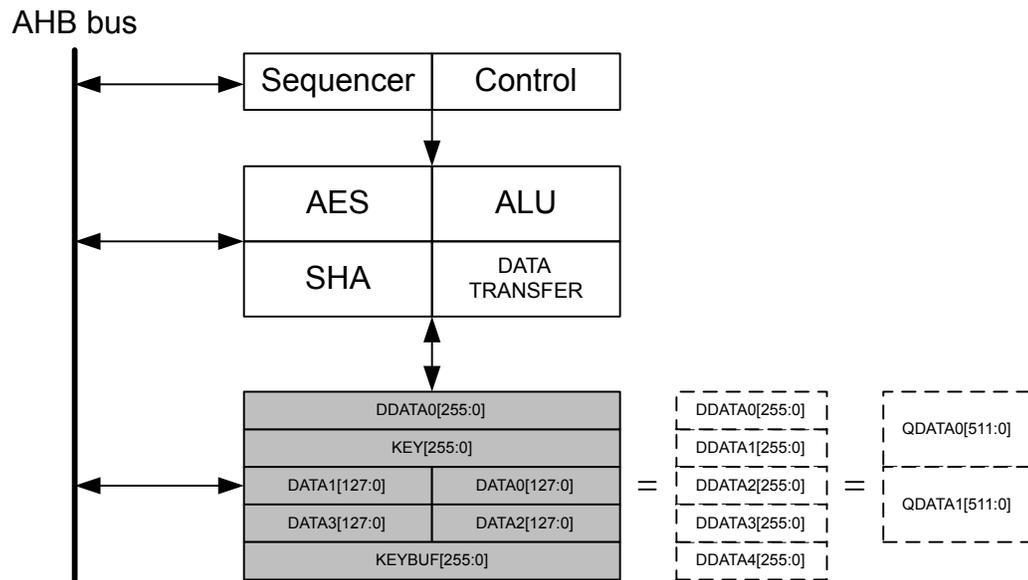
## 32.3 Usage and Programming Interface

Many security systems fail due to mistakes in the implementation. Therefore implementations should be left to experts in cryptographic algorithms.

To solve this, the module is supported by an hardened cryptography software library and API delivered through Silicon Labs' Simplicity Studio. The software API is a frontend for performing all supported cryptographic operations both for radio-protocols and applications, and must be used to receive prompt support.

### 32.4 Functional Description

A block diagram of the CRYPTO module is shown in [Figure 32.1 CRYPTO Overview on page 1064](#).



**Figure 32.1. CRYPTO Overview**

### 32.4.1 Data and Key Registers

The CRYPTO module contains five 256-bit registers. Accelerators are implemented through instructions operating on these registers, either by copying data between registers and external components like the BUFC or through DMA, or by executing instructions on the registers.

Depending on the instruction, the registers can be accessed as 128-bit, 256-bit or 512-bit registers. The registers can also be accessed through different interface registers to achieve different results.

When writing to and reading from the CRYPTO\_DATAx, CRYPTO\_KEY, CRYPTO\_KEYBUF, CRYPTO\_DDATAx and CRYPTO\_QDATAx registers, the least significant part is accessed first and the most significant part last, see [Figure 32.2 CRYPTO Data and Key Register Operation on page 1066](#). The same is the case for the XOR and byte-access registers for DATA0 and DATA1. It is important to note that some of the 256-bit registers are composed of the 128-bit registers, and both the 512-bit registers are composed of the 256-bit registers.

**Note:** From here on, the 128, 256 and 512-bit registers are named DATAx, DDATAx, QDATAx, etc. And the access-points to these registers are named CRYPTO\_DATAx, CRYPTO\_DDATAx, CRYPTO\_QDATAx, etc.

DATA0 can be accessed through CRYPTO\_DATA0 (32-bit), CRYPTO\_DATA0XOR (32-bit), CRYPTO\_DATA0BYTE (8-bit) and CRYPTO\_DATA0XORBYTE (8-bit). Direct access to bytes 12 - 15 is available through CRYPTO\_DATA0BYTE12-15 (8-bit). The DATA0XOR (in CRYPTO\_DATA0XOR) is used for XOR'ing a value with the current value in DATA0. This is used in a large variety of block cipher modes. All of these registers operate on DATA0.

DATA1 can be accessed through CRYPTO\_DATA1 (32-bit) and CRYPTO\_DATA1BYTE (8-bit).

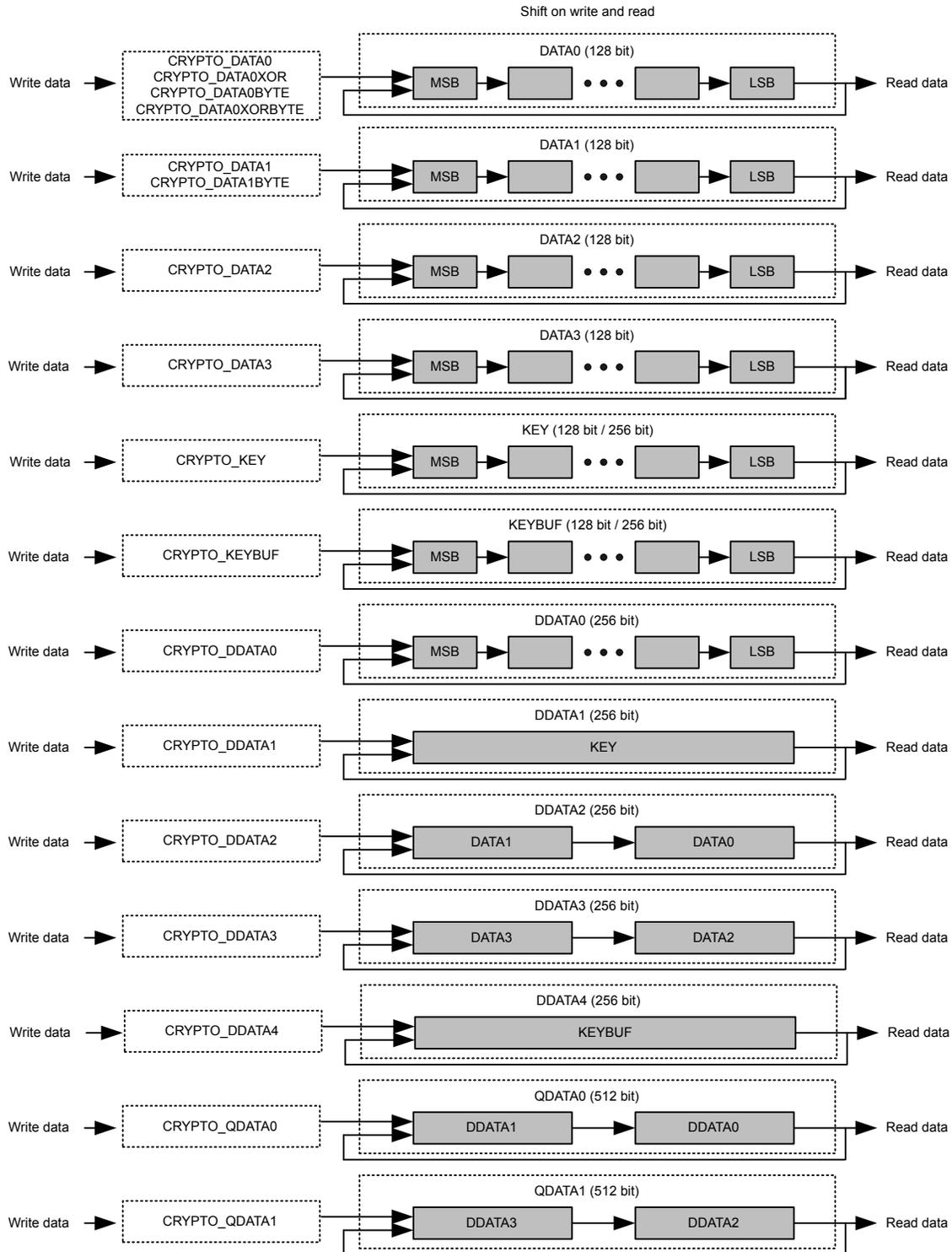
The remaining data registers have regular 32-bit access through their respective registers. Note that all data registers require a full read or write to be fully accessed. This means that the 128-bit registers need four 32-bit reads/writes, the 256-bit registers need 8 reads/writes and the 512-bit registers need 16 reads/writes. For a read, if all read accesses are not done, the register will end up as a shifted version of the original value.

**Note:** For byte-wise data accesses (DDATAxBYTE, DATAxBYTE, etc.), all reads and writes must be performed in groups of 4, due to internal buffering and shifting of 32 bits at a time. Accessing a number of bytes that is not a multiple of four can cause data incoherency in all of the data registers.

The KEY and KEYBUF registers are 256 bit wide when AES256 is set in CRYPTO\_CTRL. Else they are 128 bit wide. When used as a part of DDATAx and QDATAx, they are always 256 bit wide.

The registers DDATA0BIG and QDATA1BIG produce byte-swapped versions of DDATA0 and QDATA1 respectively. These may be used when a computation requires byte-swapping. An example of this is SHA computation, where data needs to be changed to big endian before CRYPTO can work with it. Little endian data is then loaded in through QDATA1BIG and the resulting little endian hash can be read out from DDATA0BIG, see [32.4.5 SHA](#).

Except for KEYBUF, the contents of all data registers are lost when going to EM2.



**Figure 32.2. CRYPTO Data and Key Register Operation**

### 32.4.1.1 DATA0 Zero

DATA0ZERO in CRYPTO\_DSTATUS contains status flags indicating if any 32-bit blocks within DATA0 is 0. For example, if DATA0[95:64] is equal to 0x00000000, ZERO64TO95 is set.

### 32.4.1.2 DDATA0 and DDATA1 Quick Observation

DDATA0LSBS in CRYPTO\_DSTATUS shows the 4 least significant bits in DDATA0. DDATA0MSBS in CRYPTO\_DSTATUS shows the 4 most significant bits of DDATA0, while DDATA1MSB in CRYPTO\_DSTATUS shows the msb of DDATA1. These observation bitfields are useful for determining the sign of the value in the data registers without having to read out the full register data register values

The 4 bits observed by DDATA0MSBS will change depending on RESULTWIDTH in CRYPTO\_WAC. When using 260-bit results, DDATA0MSBS shows bits 259-256, when using 256-bit results, it is bits 255-252, and for 128-bit results, bits 127-124 can be observed. When RESULTWIDTH is 260 bits, the 4 most significant bits, e.g. bits 259-256 are also available in CRYPTO\_DDATA0BYTE32, where they can also be written. Using this register is the only way of inputting the upper 4 bits of a 260-bit number to CRYPTO.

### 32.4.1.3 Result Width

RESULTWIDTH in CRYPTO\_WAC determines the width of the operation when performing arithmetic/shift instructions with CRYPTO. Using less wide results will reduce the current consumption of the CRYPTO module. The higher-order bits that are beyond the selected result width are ignored in the computation of arithmetic/shift operations, however, these higher-order bits will be undefined in the result of such instructions.

When RESULTWIDTH=260BIT, all DDATA registers effectively become 260 bits wide, so that the upper 4 bits are not lost when transferring data from DDATA0 to the other DDATA registers. Likewise, the arithmetic/shift instructions shall consider the full 260-bit values of DDATA0-DDATA4 when used as operation inputs. Note that DDATA0 is the only 260-bit register of which MSBs can be observed/written. The upper 4 bits are observed through DDATA0MSBS in CRYPTO\_DSTATUS or through CRYPTO\_DDATA0BYTE32. For all DDATAx registers, the extra MSBs are cleared when DDATAx is written. Furthermore, for a particular x, a write to DDATAx or any of its aliased registers will cause DDATAx MSBs to be cleared. Note, writing to KEY/KEYBUF will only clear MSBs of DDATA1/DDATA4 when AES256 mode is set. Likewise, writing to DATA0/DATA2 will not clear DDATA2/DDATA3 MSBs.

Since the DATA0-DATA3 registers are always 128-bit, all bit positions greater than 128 are interpreted as 0 when RESULTWIDTH is greater than 128 bits. However, the assignment instructions DATAxTODDATAy will not zero-out the upper 128 bits of the DDATAy target. Instead, those upper words become undefined after such operations.

## 32.4.2 Instructions and Execution

The CRYPTO module implements a set of instructions in order to load and manipulate data effectively. These instructions are grouped into four types:

- ALU instructions - arithmetic and logical bitwise operations
- Transfer instructions - moving data between registers and external peripherals like DMA and the BUFC
- Conditional instructions - conditionally execute instructions based on context
- Special instructions - various crypto and support instructions

A single instruction can be executed by writing INSTR in CRYPTO\_CMD. This will execute the instruction, and the interface of CRYPTO will be locked until the execution has completed. Multiple commands can safely be issued after each other by the CPU as long as NOBUSYSTALL in CRYPTO\_CTRL is not set. If CRYPTO gets a new command or a data access request while busy it will then stall the bus, and execute the new command as soon as it is done with the previous one. Note, there are some exceptions to this rule. For example, see [32.4.8 DMA](#).

Stalling of the bus can be disabled by setting NOBUSYSTALL in CRYPTO\_CTRL, however manipulating (reading or writing) registers while running an instruction will result in undefined behaviour. Additionally, if NOBUSYSTALL=0 and a new command or data access request is made while the CRYPTO is simultaneously performing a data transfer instruction, it is possible for system lockup due to bus stalling loops. The safest approach is to always check if an instruction is running by looking at INSTRRUNNING in CRYPTO\_STATUS.

Note that this automatic stalling feature does not apply to automated CRYPTO instruction sequences (described next), since there may be cycle delays between individual instructions for which bus accesses are not prevented. For sequences, always check the SEQRUNNING status bit or the SEQDONE interrupt flag to ensure the sequence is finished before attempting CRYPTO register accesses.

### 32.4.2.1 Sequences

For executing a set of instructions, it is more efficient to load them into the CRYPTO module and run them as a sequence. This is done by writing the instructions into CRYPTO\_SEQ0-CRYPTO\_SEQ4, and marking the end of the instruction sequence with either an END or an EXEC instruction. The END simply means end-of-instructions, while writing EXEC means end-of-instructions and execute immediately.

The five registers allow up to 20 instructions to be loaded. To start execution, either end the instructions with an EXEC instruction, or set SEQSTART in CRYPTO\_CMD. CRYPTO will then execute the instructions, starting in CRYPTO\_SEQ0, and ending at the first END instruction. SEQRUNNING in CRYPTO\_STATUS is set while the sequence is running, and the interrupt flag SEQDONE in CRYPTO\_IF will be set when the sequence has completed.

A sequence can be stopped by issuing the SEQSTOP command in the CRYPTO\_CMD register. This command also clears the state of ongoing CRYPTO instructions including DMA and BUFC access. Check SEQRUNNING in CRYPTO\_STATUS after issuing the SEQSTOP command flag to make sure any ongoing sequence/transfer has completed before accessing data registers again.

### 32.4.2.2 Available Instructions

The available ALU instructions are listed in [Table 32.1 ALU Instructions on page 1069](#), data transfer instructions are listed in [Table 32.2 Transfer Instructions on page 1070](#), conditional instructions are listed in [Table 32.3 Conditional Instructions on page 1071](#) and special instructions are listed in [Table 32.4 Special Instructions on page 1071](#). The tables explain the side-effects of the instructions and shows which registers are affected. For instructions involving BUFC, the BUFC Buffers are defined by READBUFSEL and WRITEBUFSEL in CRYPTO\_CTRL for BUFC reads and writes respectively. V0 and V1 in the instructions descriptions can be any of the DDATAx registers and a selection of the DATAx registers. They can be selected using the SELDDATAxDDATAy, SELDATAxDDATAy, SELDDATAxDATAy and SELDATAxDATAy instructions. The first register in the instruction will be selected for V0, and the second for V1. This configuration stays even when the sequence is complete, and can also be set up front. The currently selected V0 and V1 can be read V0 and V1 in CRYPTO\_CSTATUS.

**Table 32.1. ALU Instructions**

| Instruction | Description  | Constraints/Notes  |
|-------------|--|--|
| ADD         | $DDATA0 = V0 + V1$   | If V0 != DDATA0, then V1 != DDATA0   |
| ADDO        | $DDATA0 = V0 + V1$   | Carry is only set, not cleared.<br>If V0 != DDATA0, then V1 != DDATA0                  |
| ADDC        | $DDATA0 = V0 + V1 + \text{carry}$  | If V0 != DDATA0, then V1 != DDATA0   |
| ADDIC       | $DDATA0 = V0 + V1 + \text{carry} \ll 128$  | If V0 != DDATA0, then V1 != DDATA0.<br>If resultwidth is 128b, then carry is undefined |
| MADD        | $DDATA0 = (V0 + V1) \bmod P$   | If V0 != DDATA0, then V1 != DDATA0   |
| MADD32      | $DDATA0[i] = V0[i] + V1[i]$ .<br>Word-wise addition  | carry is not modified.<br>If V0 != DDATA0, then V1 != DDATA0                           |
| SUB         | $DDATA0 = V0 - V1$   | V1 != DDATA0.<br>If V1 is 128b and resultwidth > 128b,<br>then upper 128b are unknown  |
| SUBC        | $DDATA0 = V0 - V1 - \text{carry}$  | V1 != DDATA0.<br>If V1 is 128b and resultwidth > 128b,<br>then upper 128b are unknown  |
| MSUB        | $DDATA0 = (V0 - V1) \bmod P$   | V1 != DDATA0.<br>If V1 is 128b and resultwidth > 128b,<br>then upper 128b are unknown  |
| MUL         | $DDATA0 = DDATA1 * V1$ .<br>See <a href="#">32.4.2.3 MULx Details</a>                                | V1 != DDATA0, DDATA1   |
| MULC        | $DDATA0 = DDATA1 * V1 + (DDATA0 \ll \text{MULWIDTH})$ .<br>See <a href="#">32.4.2.3 MULx Details</a> | V1 != DDATA0, DDATA1   |
| MMUL        | $DDATA0 = (DDATA1 * V1) \bmod P$   | V1 != DDATA0, DDATA1   |
| MULO        | $DDATA0 = DDATA1 * V1$ .<br>See <a href="#">32.4.2.3 MULx Details</a>                                | V1 != DDATA0, DDATA1. Carry is only set, not cleared                                   |
| SHL         | $DDATA0 = V0 \ll 1$  | If V0 is 128b and resultwidth is 260b, then upper 4b are unknown                       |
| SHLC        | $DDATA0 = V0 \ll 1 \mid \text{carry}$  | If V0 is 128b and resultwidth is 260b, then upper 4b are unknown                       |
| SHLB        | $DDATA0 = V0 \ll 1 \mid V0[\text{resultwidth}-1]$  | If V0 is 128b and resultwidth is 260b, then upper 4b are unknown                       |
| SHL1        | $DDATA0 = V0 \ll 1 \mid 1$   | If V0 is 128b and resultwidth is 260b, then upper 4b are unknown                       |
| SHR         | $DDATA0 = V0 \gg 1$  |  |
| SHRC        | $DDATA0 = V0 \gg 1 \mid \text{carry} \ll \text{resultwidth}-1$                                       |  |

| Instruction | Description  | Constraints/Notes                                  |
|-------------|--|--|
| SHRB        | $DDATA0 = V0 \gg 1 \mid V0[0] \ll \text{resultwidth}-1$                    |  |
| SHR1        | $DDATA0 = V0 \gg 1 \mid 1 \ll \text{resultwidth}-1$                        |  |
| SHRA        | $DDATA0 = V0 \gg 1 \mid V0[\text{resultwidth}-1] \ll \text{resultwidth}-1$ |  |
| CLR         | $DDATA0 = 0$   |  |
| XOR         | $DDATA0 = V0 \wedge V1$  | If $V0 \neq DDATA0$ , then $V1 \neq DDATA0$        |
| INV         | $DDATA0 = \sim V0$   |  |
| CSET        | $CARRY = 1$  |  |
| CCLR        | $CARRY = 0$  |  |
| BBSWAP128   | $DDATA0[127:0] = \text{bbswap}(V0[127:0])$                                 | See <a href="#">32.4.2.5 BBSWAP128 Instruction</a> |
| INC         | $DDATA0 = DDATA0 + 1$  |  |
| DEC         | $DDATA0 = DDATA0 - 1$  |  |

Table 32.2. Transfer Instructions

| Instruction         | Operation   | Constraints/Notes  |
|---------------------|---|--|
| DATAxTOBUF          | $BUFC = DATAx$                                      | $x = 0,1$ . BUFC buffer defined by WRITEBUFSEL   |
| DATAxXORBUF         | $BUFC = BUFC \wedge DATAx$                          | $x = 0,1$ . BUFC buffer defined by WRITEBUFSEL   |
| BUFTODATAx          | $DATAx = BUFC$                                      | $x = 0,1$ . BUFC buffer defined by READBUFSEL  |
| BUFTODATA0XOR       | $DATA0 = DATA0 \wedge BUFC$                         | BUFC buffer defined by READBUFSEL  |
| DATATODMA0          | $DMA = DATAx$ , DMA request DMA0RD                  | $DATAx = DATA0, DDATA0, DDATA0BIG, QDATA0$ as defined by DMA0RSEL  |
| DMA0TODATA          | $DATAx = DMA$ , DMA request DATA0WR                 | $DATAx = DATA0, DDATA0, DDATA0BIG, QDATA0$   |
| DMA0TODATA0XOR      | $DATA0 = DATA0 \wedge DMA$ , DMA request DATA0XORWR |  |
| DATATODMA1          | $DMA = DATAx$ , DMA request DMA1RD                  | $DATAx = DATA1, DDATA1, QDATA1, QDATA1BIG$ as defined by DMA1RSEL  |
| DMA1TODATA          | $DATAx = DMA$ , DMA request DATA0WR                 | $DATAx = DATA1, DDATA1, QDATA1, QDATA1BIG$   |
| DATAxTODATAy        | $DATAY = DATAx$                                     |  |
| DATAxTODATA0XOR     | $DATA0 = DATA0 \wedge DATAx$                        | If resultwidth is 128b, then carry is undefined  |
| DATAxTODATA0XOR-LEN | $DATA0 = DATA0 \wedge (DATAx \& (2^{**}LENGTH-1))$  | LENGTH is LENGTHA or LENGTHB depending on active part of sequence. If resultwidth is 128b, then carry is undefined |
| DDATAxTODDATAy      | $DDATAy = DDATAx$                                   |  |
| DDATAxHTODATA1      | $DATA1 = DDATAx[255:128]$                           | Bits $DDATA2[259:256]$ become undefined  |
| DDATAxLTODATAy      | $DATAY = DDATAx[127:0]$                             |  |
| SELDDATAxDDATAy     | Use DDATAx as V0, DDATAy as V1                      | $x = 0,1,2,3,4; y = 0,1,2,3,4$   |
| SELDATAxDDATAy      | Use DATAx as V0, DDATAy as V1                       | $x = 0,1,2; y = 0,1,2,3,4$   |
| SELDDATAxDATAy      | Use DDATAx as V0, DATAy as V1                       | $x = 0,1,2,3,4; y = 0,1$   |
| SELDATAxDATAy       | Use DATAx as V0, DATAy as V1                        | $x = 0,1,2; y = 0,1$   |

**Table 32.3. Conditional Instructions**

| Instruction  | Operation   | Constraints |
|--------------|---|-------------|
| EXECIFA      | Execute following instructions if in part A of sequence             |             |
| EXECIFB      | Execute following instructions if in part B of sequence             |             |
| EXECIFNLAST  | Execute following instructions if not in last iteration of sequence |             |
| EXECIFLAST   | Execute following instructions if in last iteration of sequence     |             |
| EXECIFCARRY  | Execute following instructions if carry bit is set                  |             |
| EXECIFNCARRY | Execute following instructions if carry bit not is set              |             |
| EXECALWAYS   | Always execute following instructions                               |             |

**Table 32.4. Special Instructions**

| Instruction | Operation   |
|-------------|---|
| END         | Ends execution.   |
| EXEC        | When written to CRYPTO_SEQx register, automatically triggers execution of all instruction up to this point. |
| AESENC      | DATA0 = AESENC(DATA0)   |
| AESDEC      | DATA0 = AESDEC(DATA0)   |
| SHA         | DDATA0 = SHA(Q1)  |
| DATA1INC    | DATA1 = inc(DATA1).<br>See <a href="#">32.4.2.4 DATA1INC and DATA1INCCLR Instructions</a>                   |
| DATA1INCCLR | DATA1 = clearinc(DATA1).<br>See <a href="#">32.4.2.4 DATA1INC and DATA1INCCLR Instructions</a>              |

### 32.4.2.3 MULx Details

For the MULx instructions (not MMUL), MULWIDTH in CRYPTO\_WAC specifies the width of operands DDATA1 (and sometimes V1). This is useful in order to optimize performance because multiplications take the same number of cycles as the bits in the operands plus a couple of cycles for setup.

As with the other ALU instructions, RESULTWIDTH limits the width of the final result of the MULx and MMUL instructions.

### 32.4.2.4 DATA1INC and DATA1INCCLR Instructions

DATA1INC and DATA1INCCLR operate on the 1, 2, 3 or 4 most significant bytes in DATA1, depending on INCWIDTH in CRYPTO\_CTRL. DATA1INC increments these bytes in big endian, while DATA1INCCLR clears the bytes.

### 32.4.2.5 BBSWAP128 Instruction

The BBSWAP128 instruction copies the contents of the V0 operand to DDATA0 while swapping the bits of the lower 16 bytes. The operand is not changed. This operation is required for GCM. See [32.4.7 GCM and GMAC](#)

### 32.4.2.6 Carry

The carry output from most instructions can be observed through the CARRY bit in CRYPTO\_DSTATUS. Shift-instructions set CARRY to the value that is shifted out of the register, addition and multiplication set it on register overflow, and subtraction sets it on borrow, e.g. underflow.

In addition to generating carry information, some instructions also use the current value of CARRY. ADDC, SUBC, SHLC and SHRC all use carry to generate the result. For all of these instructions, carry allows a program to chain instructions together to operate on bigger numbers than allowed by CRYPTO. For example, by chaining first an ADD, and then an ADDC which uses the carry from the ADD operation, two 512-bit numbers can be added. By chaining more instructions, even larger numbers can be manipulated.

Other uses of CARRY include observation. To check if a register is 0, one can subtract 1 using the DEC instruction, and check if goes negative by checking the CARRY bit. CARRY can be set manually and in CRYPTO programs using the CSET and CCLR instructions, which set and clear the CARRY bit.

The MULC instruction does not use CARRY like the other carry instructions (i.e., instructions ending in 'C' such as 'ADDC'), but rather preserves the old contents of the multiplication register.

### 32.4.3 Repeated Sequence

To maximize efficiency, it is desirable to be able to run a set of instructions over multiple blocks of data autonomously. To repeat a sequence over a larger set of data, set LENGTHA in CRYPTO\_SEQCTRL to the number of bytes in the set, and BLOCKSIZE to the size of the blocks in the set. The sequence will then be repeated N times, where N is LENGTHA / BLOCKSIZE if LENGTHA is a multiple of BLOCKSIZE, or ceiling( LENGTHA / BLOCKSIZE ) if not. In the latter case, data written by DMA or received from BUFC will be zero-padded up to BLOCKSIZE if it is written to a register which has a size equal to BLOCKSIZE. One notable exception is when LENGTHA is 0. In this case the sequence will still execute once, but the block transfer instructions will not execute.

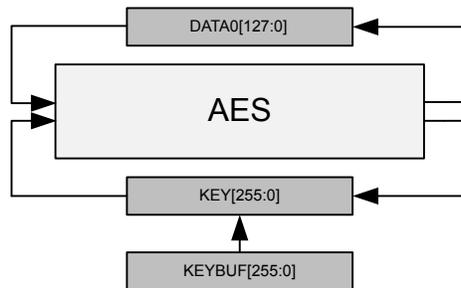
**Note:** If DMAxRSEL in CRYPTO\_CTRL selects a register that is smaller than the specified blocksize, DATATODMAx/DMAxTODATA instructions will not use the full blocksize, but will only transfer enough data to empty/fill the register once. For example, if BLOCKSIZE is set to 64B and DMA0RSEL=DDATA0, the instruction DATATODMA0 will only read 32B instead of 64B. The processing of LENGTHA/B will continue as if all 64B had been transferred.

A repeated sequence can also be made do slightly different operations on different parts of the data set. A sequence can be divided into two parts; part A, and part B. By configuring LENGTHA in CRYPTO\_SEQCTRL to the length of part A, and LENGTHB in CRYPTO\_SEQCTRLB to the length of part B, CRYPTO will first run iterations over part A, knowing it is A, and then part B, knowing it is part B. By using the conditional instructions listed in [Table 32.3 Conditional Instructions on page 1071](#), a program can execute different instructions depending on whether it is in part A or part B.

### 32.4.4 AES

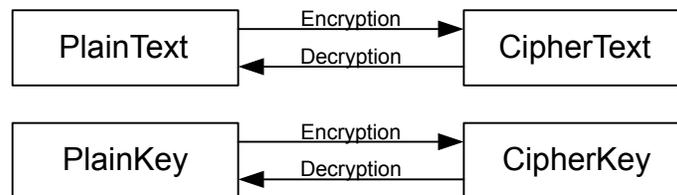
The AES core operates on data in the 128-bit register DATA0 using the either a 128-bit or 256-bit key from the KEY register. The key width is specified by AES256 in CRYPTO\_CTRL. AES operations are implemented as the AESENC and AESDEC instructions, for AES encryption and AES decryption respectively. An overview of the AES functionality is shown in [Figure 32.3 CRYPTO AES Overview on page 1073](#).

AES encryption and decryption enables various block cipher modes like ECB, CTR, CBC, PCBC, CFB, OFB, CBC-MAC, GMAC, CCM, CCM\*, and GCM.



**Figure 32.3. CRYPTO AES Overview**

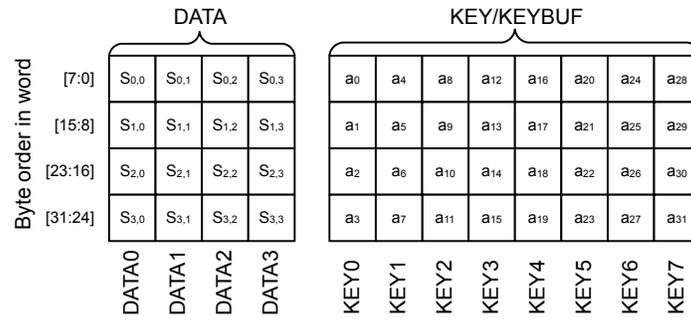
The input data before encryption is called the PlainText and output from the encryption is called CipherText. For encryption, the key is called PlainKey. After encryption, the resulting key in the KEY registers is the CipherKey. This key must be loaded into the KEY registers prior to the decryption. After one decryption, the resulting key will be the PlainKey. The resulting PlainKey/CipherKey is only dependent on the value in the KEY registers before encryption/decryption. The resulting keys and data are shown in [Figure 32.4 CRYPTO Key and Data Definitions on page 1073](#).



**Figure 32.4. CRYPTO Key and Data Definitions**

The KEY is by default loaded from KEYBUF prior to each AESENC or AESDEC instruction. If the KEY is not to be overwritten, key buffering should be disabled (KEYBUFDIS in CRYPTO\_CTRL). Disabling key buffering also allows the use of key loading through DMA.

The data and key orientation in the CRYPTO registers are shown in [Figure 32.5 CRYPTO Data and Key Orientation as Defined in the Advanced Encryption Standard on page 1074](#).



**Figure 32.5. CRYPTO Data and Key Orientation as Defined in the Advanced Encryption Standard**

### 32.4.5 SHA

The CRYPTO SHA instruction implements SHA-1 with a 160-bit digest or SHA-2 with a 224-bit digest (SHA-224) or 256-bit digest (SHA-256). Depending on SHAMODE in CRYPTO\_CTRL, SHA-1, SHA-224 or SHA-256 will be run on the data in QDATA1, and the result will be put on DDATA0. The contents in QDATA1 will be destroyed in the process.

To run SHA on a dataset, it must first be pre-processed by appending a bit '1' to the message, then padding the data with '0' bits until the message length in bits modulo 512 is 448. Then append the length of the message before pre-processing as a 64-bit big-endian integer. This pre-processing is known as MD-strengthening, and must be done by software before processing with the CRYPTO module.

The pre-processed data can now be run through the CRYPTO module. Begin by writing the values listed in [Table 32.5 SHA Init Values on page 1075](#) to CRYPTO\_DDATA1 from top to bottom, then execute the instructions listed in [Table 32.6 SHA Preparations on page 1075](#).

**Table 32.5. SHA Init Values**

| SHA-1      | SHA-224    | SHA-256    |
|------------|------------|------------|
| 0x67452301 | 0xC1059ED8 | 0x6A09E667 |
| 0xEFCDA89  | 0x367CD507 | 0xBB67AE85 |
| 0x98BADCFE | 0x3070DD17 | 0x3C6EF372 |
| 0x10325476 | 0xF70E5939 | 0xA54FF53A |
| 0xC3D2E1F0 | 0xFFC00B31 | 0x510E527F |
| 0x00000000 | 0x68581511 | 0x9B05688C |
| 0x00000000 | 0x64F98FA7 | 0x1F83D9AB |
| 0x00000000 | 0xBEFA4FA4 | 0x5BE0CD19 |

**Table 32.6. SHA Preparations**

| STEP  | ACTION          | Description  |
|-------|-----------------|--|
| STEP0 | DDATA1TODDATA0  | Copy init data to DDATA0                                 |
| STEP1 | SELDDATA0DDATA1 | Select DDATA0 and DDATA1 as operands for SHA instruction |

Then, for each 512-bit block, write the block to CRYPTO\_QDATA1BIG, execute the instructions listed in [Table 32.7 SHA for 512-bit Block on page 1075](#).

**Table 32.7. SHA for 512-bit Block**

| STEP  | ACTION         | Description                             |
|-------|----------------|---|
| STEP0 | SHA            | Perform SHA operation on data in QDATA1 |
| STEP1 | MADD32         | Accumulate with previous data in DDATA1 |
| STEP2 | DDATA0TODDATA1 | Copy hash to DDATA1                     |

After the last iteration, the resulting hash can be read out from CRYPTO\_DDATA0BIG.

### 32.4.6 ECC

The CRYPTO module implements support for Elliptic Curve Cryptography through the modular instructions MADD, MMUL and MSUB, which perform modular addition, multiplication and subtraction respectively. The instructions can operate on a set of both prime fields GF(p) and binary fields GF(2<sup>m</sup>).

The type of modular arithmetic used and the modulus for the modular operations are specified by MODOP and MODULUS in CRYPTO\_WAC respectively. Changing these in the middle of an operation leads to undefined behaviour.

### 32.4.7 GCM and GMAC

CRYPTO implements support for Galois/Counter Mode (GCM), and also Galois Message Authentication Code (GMAC), by providing AES instructions and allowing multiplication on the field  $GF(2^{128})$  defined by the polynomial  $x^{128} + x^7 + x^2 + x + 1$ .

**Note:** BBSWAP128 needs to be applied to both operands and the result of the MMUL instruction when using it for GCM and GMAC

Efficient sequencer programs can be set up to perform GCM authentication and encryption/decryption on data from either BUFC, DMA, or CPU. To achieve a single-pass solution, LENGTHA in CRYPTO\_SEQCTRL is set to the length of the authentication part, and LENGTHB is set to the length of the rest of the message. Conditional instructions can then be used to make sure the two parts of the message are processed correctly. A similar approach is used to implement CCM.

### 32.4.8 DMA

The CRYPTO module has 5 DMA request signals (see [Table 32.8 DMA Signals on page 1076](#)) split over 2 internal DMA channels: DMA0 and DMA1. These DMA channels are not associated with channel 0 and 1 of the system DMA, and any system DMA channel can serve any of the 5 DMA requests. See the DMA chapter for information on how to configure the system DMA.

The DMA signals are set through the use of DMA oriented instructions, and cleared by reading or writing the respective CRYPTO data registers.

**Table 32.8. DMA Signals**

| Name      | Set on  | Cleared on  |
|-----------|---|---|
| DMA0WR    | Instruction DMA0TODATA, and DMA0TODATA XOR if COMBDMA0WEREQ in CRYPTO_CTRL is set | Full CRYPTO_DATA0, CRYPTO_DDATA0, CRYPTO_DDATA0BIG or CRYPTO_QDATA0 write, or CRYPTO_DDATA0 XOR if COMBDMA0WEDMAREQ in CRYPTO_CTRL is set |
| DMA0XORWR | Instruction DMA0TODATA XOR  | Full CRYPTO_DATA0 XOR write   |
| DMA0RD    | Instructions DATATODMA0   | Full CRYPTO_DATA0, CRYPTO_DDATA0, CRYPTO_DDATA0BIG or CRYPTO_QDATA0 read, depending on DMA0MODE in CRYPTO_CTRL                            |
| DMA1WR    | Instructions DMA1TODATA   | Full CRYPTO_DATA1, CRYPTO_DDATA1, CRYPTO_QDATA1 or CRYPTO_QDATA1BIG write   |
| DMA1RD    | Instructions DATATODMA1   | Full CRYPTO_DATA1, CRYPTO_DDATA1, CRYPTO_QDATA1 or CRYPTO_QDATA1BIG read, depending on DMA1MODE in CRYPTO_CTRL                            |

**Note:** DMAxRSEL in CRYPTO\_CTRL has to be set to the data registers that are to be read using the respective DMA channels on a DATATODMAx instruction. As an important note, DMAxRSEL in CRYPTO\_CTRL selects what is read from **any** of the selectable read registers during an ongoing DATATODMAx transfer .

When a DMA oriented CRYPTO instruction is used (either through a STEP in a Sequence or through CRYPTO\_CMD), the corresponding DMA signal is set. The instruction is complete when the entire source/destination is read/written (e.g. if DMA0TODATA is used, the operation is complete when a total of 128 valid bits have been written through the CRYPTO\_DATA0 register). DMAACTIVE in CRYPTO\_STATUS is set while CRYPTO is working on a DMA-related instruction, e.g. waiting for the DMA to read or write data to CRYPTO (see [32.4.8.1 DMA Initial Bytes Skip](#)).

Normally, when a sequence or instruction is executed, access to most CRYPTO registers will stall the CPU or DMA that is trying to access CRYPTO until the operation is done, preventing accesses to CRYPTO that could potentially interfere with an operation. During DMA operations, all non-DMA registers are writeable and readable, but progress through the DMA operation will only be tracked with the registers targeted by the DMA operation (i.e., if the DMA operation is supposed to transfer 3 words to DATA0, the DMA can first choose to transfer data to e.g. DATA3, and then fulfill the transfer to DATA0).

Because the bus interface to CRYPTO is normally locked outside of DMA transfers, a wrongly set up DMA transfer (e.g., transferring one byte too many) may lock up the interface.. One way to assist in debugging such issues can be setting NOBUSYSTALL in CRYPTO\_CTRL. This will prevent any stall on CRYPTO register accesses during sequences and instructions. Use this option with care, as modifying a register that is being used by CRYPTO can lead to undefined behavior.

### 32.4.8.1 DMA Initial Bytes Skip

The DMA must be configured to use 32-bit transfer size. This normally would imply that the source data must be aligned to a 4 byte address boundary. However, it is possible to skip the initial bytes (1 to 3) when using DMA to write to DATA0 or DATA1 through a CRYPTO instruction operation. The number of bytes to skip are set in DMA0SKIP and DMA1SKIP in CRYPTO\_SEQCTRL. This implies that if DMA0SKIP is set to another value than 0, the initial DMA access will require 5 DMA transfers, even though only 4x32-bit is required.

**Note:** Any valid unused bytes from a previous DMA write will be used before new DMA data is requested. This data is invalidated by using STOP in CRYPTO\_CMD.

### 32.4.8.2 DMA Unaligned Read/Write

Except for DATA0 and DATA1, which can be loaded bitwise using the CRYPTO\_DATA0BYTE, CRYPTO\_DATA0XORBYTE and CRYPTO\_DATA1BYTE registers, the CRYPTO data registers are loaded 32-bits at a time. Special care must be taken when using the DMA and the data buffer is not aligned to a 32-bit address, because the DMA does not directly support 32-bit unaligned accesses.

As an example, let an in-memory 16-byte data buffer start at address  $4*N + M$  and end at the byte before  $4*N + 16 + M$ , where  $M$  is between 0 and 3 inclusive. With an  $M=0$ , we have fully aligned accesses, and everything is fine. For  $M>0$  however, the access is unaligned. If  $M=1$ , that means that the first 32-bit aligned word of the memory buffer contains 1 byte before the buffer, and 3 bytes of the buffer. Similarly, the last 32-bit aligned word of the memory buffer contains the last byte of the buffer, and three bytes after the buffer.

When doing an unaligned read, we want to only pass the 16 bytes of the buffer to the CRYPTO module. Not the  $N$  bytes before in the 32-bit aligned word, and not the  $4-N$  words at the end. To achieve this, set  $DxDMAREADMODE$  in CRYPTO\_CTRL to either UNALIGNEDFULL or UNALIGNEDLENLIMIT, and set  $DATAxDMASKIP$  in CRYPTO\_SEQCTRL equal to  $N$ . When reading in data using a DMA-oriented instruction to  $DATAx$ ,  $DDATAx$  or  $QDATAx$ , the read will now only contain the 16 bytes, and not the  $N$  bytes before or  $4-N$  words after. Note that in this case, the DMA has to be set up to transfer 5 32-bit words instead of the effective 4.

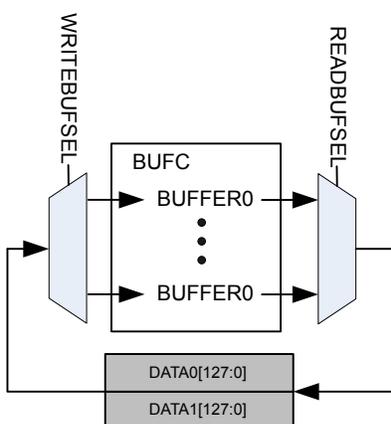
Being able to read unaligned data does not solve all cases however. If data is to be written back to the buffer after passing through CRYPTO, e.g. when doing an in-place encryption or decryption, it is very undesirable to actually modify the  $N$  bytes before and  $4-N$  bytes after the buffer. This is solved using the UAR-suffixed registers in CRYPTO when reading data out from the CRYPTO module, e.g. CRYPTO\_DATA0UAR, CRYPTO\_DATA1UAR, CRYPTO\_DDATA0UAR, CRYPTO\_DDATA1UAR, CRYPTO\_QDATA0UAR, etc. When an unaligned buffer is written to a CRYPTO buffer, CRYPTO stores the  $N$  first bytes and the  $4-N$  last bytes internally. When reading out from an UAR register, these bytes are placed back into the data if  $DATAxDMAPRES$  is set in CRYPTO\_SEQCTRL.

Note that the latter case only works if the first  $N$  and the last  $4-N$  bytes are not changed while CRYPTO works on the data. Internally CRYPTO has 2 buffers for the bytes before and after. The first one is connected to read/write of the DATA0, DDATA0 and QDATA0 registers, and the second is connected to the DATA1, DDATA1 and QDATA1 registers.

If  $DMAxRMODE$  in CRYPTO\_CTRL is set to FULL or UNALIGNEDFULL and the corresponding  $DMAxPRES$  in CRYPTO\_SEQCTRL is set, then a whole number of data buffers have to be written by the DMA. In all other cases, it is enough to write the number of 32-bit words to pass all LENGTH bits to the target CRYPTO buffer.

### 32.4.9 BUFC Data Transfer

To allow automatic encryption/decryption or other operations on radio data, CRYPTO has instructions for moving data from and to BUFC, the Buffer Controller. Both DATA0 and DATA1 can be loaded with data from the buffer selected by READBUFSEL (CRYPTO\_CTRL register) as shown in [Figure 32.6 CRYPTO BUFC Data Transfer on page 1078](#). Similarly, the content of DATA0 and DATA1 can be written to the buffer selected by WRITEBUFSEL (also in the CRYPTO\_CTRL register).



**Figure 32.6. CRYPTO BUFC Data Transfer**

When reading from CRYPTO to the BUFC, the number of bytes read are determined by the DMAxRMODE configuration in CRYPTO\_CTRL. If it is set to either LENLIMIT or LENLIMITBYTE, only the number of bytes given by LENGTH in CRYPTO\_SEQCTRL are transferred. Else the full width of the last buffer is also written, e.g. a full number of 16-byte buffers are written to the BUFC.

**Note:**

The buffer selected by READBUFSEL and WRITEBUFSEL in the CRYPTO\_CTRL registers must be appropriately configured in the BUFC module prior to using instructions involving BUFC.

All BUFC reads start at the current BUFC read pointer, and move the pointer according to the number of bytes read. BUFC writes normally also work in the same way, starting at the current BUFC write pointer, and moving it the right number of positions. For BUFC XOR writes, software has the option to change this by setting either of DATAxTOBUF XORROW in CRYPTO\_CTRL. With this bit set, the BUFC write pointer will be reset to the start of the previous write before writing to the BUFC. Using this feature, BUFC data can be written with using the DATAxTOBUFC instructions, and then XOR'ed with another set of data using the DATAxTOBUFC XOR instruction.

BUFACTIVE in CRYPTO\_STATUS is set while CRYPTO is reading or writing from/to the BUFC.

### 32.4.10 Debugging

There are multiple ways of debugging CRYPTO sequences. The most straight-forward way is to write individual instructions to INSTR in CRYPTO\_CMD. An instruction can be written, and data can be read out and examined before running another instruction.

Running individual instructions to debug a program falls short when working with repeated sequences. In these cases, a sequence is run multiple times over a set of data. This cannot be directly replicated with individual instructions

To debug a sequence, set HALT in CRYPTO\_SEQCTRL. When set, CRYPTO requires software or the debugger to step it through each instruction in the sequence. To step through the sequence, set SEQSTEP in CRYPTO\_CMD. This will execute the current instruction, and make CRYPTO ready to execute the next one.

When stepping through a sequence, the current instruction index can be read from SEQIP in CRYPTO\_CSTATUS. SEQSKIP, also in CRYPTO\_CSTATUS tells whether the next instruction will be executed or not, based on previous conditionals in the program. SEQPART in CRYPTO\_CSTATUS shows whether CRYPTO is currently in part A or B of a sequence. Even with NOBUSYSTALL in CRYPTO\_CTRL cleared, read and write accesses to CRYPTO will be allowed when CRYPTO is waiting to be stepped. This is to allow data registers to be inspected during debugging.

**Note:** The data registers in CRYPTO (those marked read-actionable) require shifting of data in order to return the result. For this reason, reading these registers will have no effect and will return unknown values during normal debugger read accesses (see [7.3.7 Debugger Reads of Actionable Registers](#)).

### 32.4.11 Example: Cipher Block Chaining (CBC)

In the following the setup and operation of CBC is explained and illustrated. The example can easily be adjusted to perform other cipher block modes.

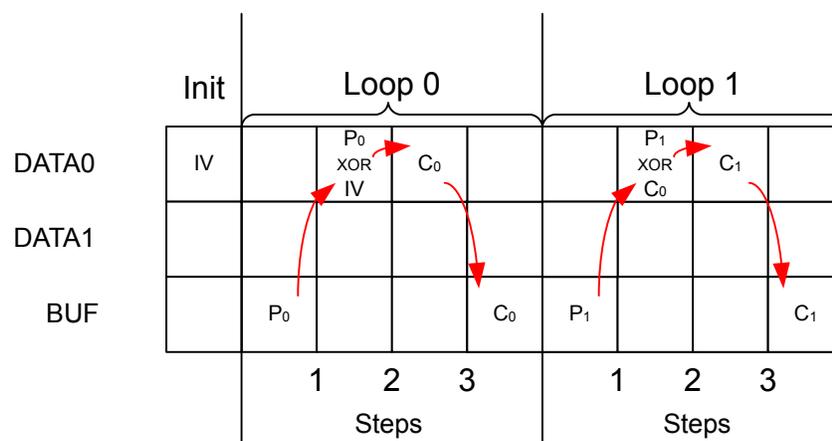
### 32.4.11.1 CBC Encryption

In CBC encryption, the cipher input is the PlainText XOR'ed with the previous cipher output (an initialization vector IV is used during the first block). This mode is easily implemented using the CRYPTO instruction sequence BUFTODATA0XOR, AESENC then DATA0TOBUF. The BUFTODATA0XOR reads data from the buffer set by READBUFSEL and XOR's it with the content in DATA0. Then the cipher operation is performed and subsequently the DATA0TOBUF writes the content of DATA0 to the buffer set by WRITEBUFSEL (normally the same as READBUFSEL).

Prior to the operation, the initialization vector IV and key must be loaded to DATA0 and KEYBUF, respectively. Additionally, the total number of bytes to be included in the repeated sequence must be set in LENGTHA in CRYPTO\_SEQCTRL. Finally, the buffers selected by READBUFSEL and WRITEBUFSEL must be configured correctly in the BUFC. The sequence is started by issuing the SEQ-START command in CRYPTO\_CMD.

In [Figure 32.7 CBC Encryption Operation on page 1080](#) the CBC encryption is illustrated and in [Table 32.9 CBC Encryption Steps on page 1080](#) each step in the loop is explained.

### CBC Encryption



**Figure 32.7. CBC Encryption Operation**

**Table 32.9. CBC Encryption Steps**

| STEP  | ACTION        | Description   |
|-------|---------------|---|
| STEP0 | BUFTODATA0XOR | Move data (PlainText, $P_i$ ) from buffer to DATA0 using XOR write. |
| STEP1 | CIPHER        | The AES Cipher Core operates on DATA0                               |
| STEP2 | DATA0TOBUF    | The cipher output $C_i$ is written to the buffer.                   |

### 32.4.11.2 CBC Decryption

In CBC decryption, CipherText ( $C_i$ ) is used as input to the Cipher Core. The output from the Cipher Core is XOR'ed with the CipherText from the previous block  $C_{i-1}$  to form the PlainText  $P_i$  (an initialization vector IV is used as  $C_{i-1}$  during the first block).

Because each block requires both  $C_{i-1}$  and  $C_i$ , decryption is somewhat more complex than encryption. Nevertheless, CBC decryption can be performed in as a repeated sequence by having  $C_{i-1}$  from the previous block stored in DATA1 and then writing it to buffer without updating the write pointer (using the DATA1TOBUF instruction). Then the cipher output is XOR'ed with  $C_{i-1}$  in the buffer by using the DATA0TOBUF XOR instruction.

In [Figure 32.8 CBC Decryption Operation on page 1081](#) the CBC decryption is illustrated and in [Table 32.10 CBC Decryption Steps on page 1081](#) each step in the loop is explained.

### CBC Decryption

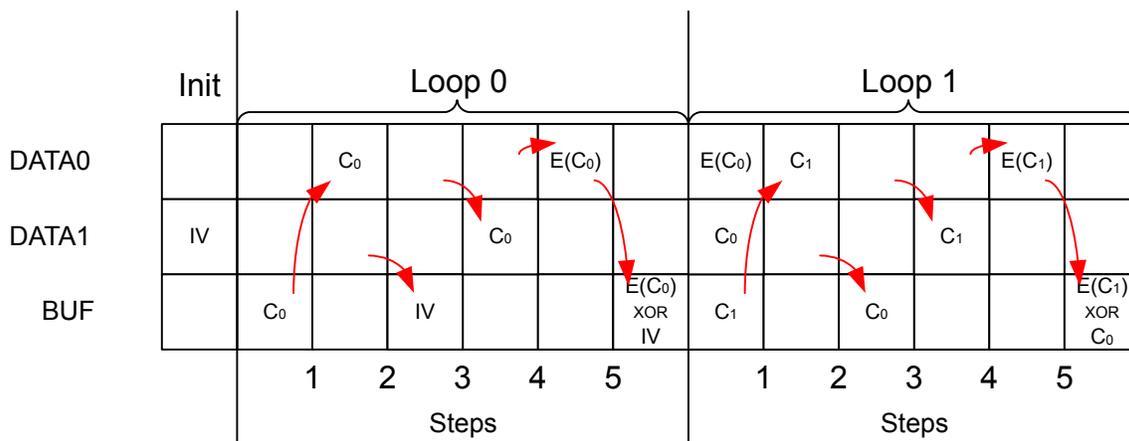


Figure 32.8. CBC Decryption Operation

Table 32.10. CBC Decryption Steps

| STEP  | ACTION           | Description  |
|-------|------------------|--|
| STEP0 | BUFTODATA0       | Moves data (CipherText, $C_i$ ) from buffer to DATA0   |
| STEP1 | DATA1TOBUF       | DATA1 (CipherText, $C_{i-1}$ ) is moved to buffer. BUFC Write pointer is not incremented!                  |
| STEP2 | DATA0TODATA1     | Value of DATA0 is copied to DATA1.   |
| STEP3 | CIPHER Operation | The AES Cipher Core operates on DATA0  |
| STEP4 | DATA0TOBUF XOR   | The cipher output is XOR'ed with $C_{i-1}$ (placed in the buffer at Step 2) to form the PlainText, $P_i$ . |

## 32.5 Register Map

The offset register address is relative to the registers base address.

| Offset | Name                | Type       | Description                    |
|--------|---------------------|------------|--------------------------------|
| 0x000  | CRYPTO_CTRL         | RW         | Control Register               |
| 0x004  | CRYPTO_WAC          | RW         | Wide Arithmetic Configuration  |
| 0x008  | CRYPTO_CMD          | W          | Command Register               |
| 0x010  | CRYPTO_STATUS       | R          | Status Register                |
| 0x014  | CRYPTO_DSTATUS      | R          | Data Status Register           |
| 0x018  | CRYPTO_CSTATUS      | R          | Control Status Register        |
| 0x020  | CRYPTO_KEY          | RWH(nB)(a) | KEY Register Access            |
| 0x024  | CRYPTO_KEYBUF       | RWH(nB)(a) | KEY Buffer Register Access     |
| 0x030  | CRYPTO_SEQCTRL      | RWH        | Sequence Control               |
| 0x034  | CRYPTO_SEQCTRLB     | RWH        | Sequence Control B             |
| 0x040  | CRYPTO_IF           | R          | AES Interrupt Flags            |
| 0x044  | CRYPTO_IFS          | W1         | Interrupt Flag Set Register    |
| 0x048  | CRYPTO_IFC          | (R)W1      | Interrupt Flag Clear Register  |
| 0x04C  | CRYPTO_IEN          | RW         | Interrupt Enable Register      |
| 0x050  | CRYPTO_SEQ0         | RW         | Sequence Register 0            |
| 0x054  | CRYPTO_SEQ1         | RW         | Sequence Register 1            |
| 0x058  | CRYPTO_SEQ2         | RW         | Sequence Register 2            |
| 0x05C  | CRYPTO_SEQ3         | RW         | Sequence Register 3            |
| 0x060  | CRYPTO_SEQ4         | RW         | Sequence Register 4            |
| 0x080  | CRYPTO_DATA0        | RWH(nB)(a) | DATA0 Register Access          |
| 0x084  | CRYPTO_DATA1        | RWH(nB)(a) | DATA1 Register Access          |
| 0x088  | CRYPTO_DATA2        | RWH(nB)(a) | DATA2 Register Access          |
| 0x08C  | CRYPTO_DATA3        | RWH(nB)(a) | DATA3 Register Access          |
| 0x0A0  | CRYPTO_DATA0XOR     | RWH(nB)(a) | DATA0XOR Register Access       |
| 0x0B0  | CRYPTO_DATA0BYTE    | RWH(nB)(a) | DATA0 Register Byte Access     |
| 0x0B4  | CRYPTO_DATA1BYTE    | RWH(nB)(a) | DATA1 Register Byte Access     |
| 0x0BC  | CRYPTO_DATA0XORBYTE | RWH(nB)(a) | DATA0 Register Byte XOR Access |
| 0x0C0  | CRYPTO_DATA0BYTE12  | RWH(nB)    | DATA0 Register Byte 12 Access  |
| 0x0C4  | CRYPTO_DATA0BYTE13  | RWH(nB)    | DATA0 Register Byte 13 Access  |
| 0x0C8  | CRYPTO_DATA0BYTE14  | RWH(nB)    | DATA0 Register Byte 14 Access  |
| 0x0CC  | CRYPTO_DATA0BYTE15  | RWH(nB)    | DATA0 Register Byte 15 Access  |
| 0x100  | CRYPTO_DDATA0       | RWH(nB)(a) | DDATA0 Register Access         |
| 0x104  | CRYPTO_DDATA1       | RWH(nB)(a) | DDATA1 Register Access         |
| 0x108  | CRYPTO_DDATA2       | RWH(nB)(a) | DDATA2 Register Access         |
| 0x10C  | CRYPTO_DDATA3       | RWH(nB)(a) | DDATA3 Register Access         |

| Offset | Name                | Type       | Description                       |
|--------|---------------------|------------|-----------------------------------|
| 0x110  | CRYPTO_DDATA4       | RWH(nB)(a) | DDATA4 Register Access            |
| 0x130  | CRYPTO_DDATA0BIG    | RWH(nB)(a) | DDATA0 Register Big Endian Access |
| 0x140  | CRYPTO_DDATA0BYTE   | RWH(nB)(a) | DDATA0 Register Byte Access       |
| 0x144  | CRYPTO_DDATA1BYTE   | RWH(nB)(a) | DDATA1 Register Byte Access       |
| 0x148  | CRYPTO_DDATA0BYTE32 | RWH(nB)    | DDATA0 Register Byte 32 Access    |
| 0x180  | CRYPTO_QDATA0       | RWH(nB)(a) | QDATA0 Register Access            |
| 0x184  | CRYPTO_QDATA1       | RWH(nB)(a) | QDATA1 Register Access            |
| 0x1A4  | CRYPTO_QDATA1BIG    | RWH(nB)(a) | QDATA1 Register Big Endian Access |
| 0x1C0  | CRYPTO_QDATA0BYTE   | RWH(nB)(a) | QDATA0 Register Byte Access       |
| 0x1C4  | CRYPTO_QDATA1BYTE   | RWH(nB)(a) | QDATA1 Register Byte Access       |

## 32.6 Register Description

### 32.6.1 CRYPTO\_CTRL - Control Register

| Offset        | Bit Position  |    |          |    |    |    |          |    |    |    |          |    |    |    |          |    |          |    |    |    |    |             |   |   |   |   |   |   |   |   |     |           |     |
|---------------|---------------|----|----------|----|----|----|----------|----|----|----|----------|----|----|----|----------|----|----------|----|----|----|----|-------------|---|---|---|---|---|---|---|---|-----|-----------|-----|
| 0x000         | 31            | 30 | 29       | 28 | 27 | 26 | 25       | 24 | 23 | 22 | 21       | 20 | 19 | 18 | 17       | 16 | 15       | 14 | 13 | 12 | 11 | 10          | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1   | 0         |     |
| <b>Reset</b>  | 0             |    | 0x0      |    |    |    | 0x0      |    |    |    | 0x0      |    |    |    | 0x0      |    | 0x0      |    |    |    |    | 0           |   |   |   |   |   |   |   |   | 0   | 0         | 0   |
| <b>Access</b> | RW            |    | RW       |    |    |    | RW       |    |    |    | RW       |    |    |    | RW       |    | RW       |    |    |    |    | RW          |   |   |   |   |   |   |   |   | RW  | RW        | RW  |
| <b>Name</b>   | COMBDMA0WEREQ |    | DMA1RSEL |    |    |    | DMA1MODE |    |    |    | DMA0RSEL |    |    |    | DMA0MODE |    | INCWIDTH |    |    |    |    | NOBUSYSTALL |   |   |   |   |   |   |   |   | SHA | KEYBUFDIS | AES |

| Bit   | Name            | Reset   | Access   | Description  |
|-------|-----------------|---|--|--|
| 31    | COMBDMA0WEREQ   | 0   | RW   | <b>Combined Data0 Write DMA Request</b><br><br>When cleared, the DATA0WR and DATA0XORWR operate independently. When set, DATA0XORWR requests are also given through DATA0WR  |
| 30    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |  |
| 29:28 | DMA1RSEL        | 0x0   | RW   | <b>DATA0 DMA Unaligned Read Register Select</b><br><br>Specifies which read register is used for DMA1RD DMA requests (see related notes in <a href="#">32.4.8 DMA</a> and <a href="#">32.4.3 Repeated Sequence</a> ) |
|       | Value           | Mode  | Description  |  |
|       | 0               | DATA1   |  |  |
|       | 1               | DDATA1  |  |  |
|       | 2               | QDATA1  |  |  |
|       | 3               | QDATA1BIG   |  |  |
| 27:26 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |  |
| 25:24 | DMA1MODE        | 0x0   | RW   | <b>DMA1 Read Mode</b><br><br>This field determines how data is read when using DMA   |
|       | Value           | Mode  | Description  |  |
|       | 0               | FULL  | Target register is fully read/written during every DMA transaction   |  |
|       | 1               | LENLIMIT  | Length Limited. When the current length, i.e. LENGTHA or LENGTHB indicates that there are less bytes available than the register size, only length + 1 bytes + necessary zero padding is read. Zero padding is automatically added when writing. |  |
|       | 2               | FULLBYTE  | Target register is fully read/written during every DMA transaction. Byte-wise DMA.   |  |

| Bit   | Name            | Reset   | Access  | Description   |
|-------|-----------------|---|---|---|
|       | 3               | LENLIMITBYTE  |   | Length Limited. When the current length, i.e. LENGTHA or LENGTHB indicates that there are less bytes available than the register size, only length + 1 bytes + necessary zero padding is read. Byte-wise DMA. Zero padding is automatically added when writing. |
| 23:22 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |
| 21:20 | DMA0RSEL        | 0x0   | RW  | <b>DMA0 Read Register Select</b><br>Specifies which read register is used for DMA0RD DMA requests (see related notes in <a href="#">32.4.8 DMA</a> and <a href="#">32.4.3 Repeated Sequence</a> )   |
|       | Value           | Mode  | Description   |   |
|       | 0               | DATA0   |   |   |
|       | 1               | DDATA0  |   |   |
|       | 2               | DDATA0BIG   |   |   |
|       | 3               | QDATA0  |   |   |
| 19:18 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |
| 17:16 | DMA0MODE        | 0x0   | RW  | <b>DMA0 Read Mode</b><br>This field determines how data is read when using DMA.   |
|       | Value           | Mode  | Description   |   |
|       | 0               | FULL  | Target register is fully read/written during every DMA transaction  |   |
|       | 1               | LENLIMIT  | Length Limited. When the current length, i.e. LENGTHA or LENGTHB indicates that there are less bytes available than the register size, only length + necessary zero padding is read. Zero padding is automatically added when writing.                |   |
|       | 2               | FULLBYTE  | Target register is fully read/written during every DMA transaction. Byte-wise DMA.  |   |
|       | 3               | LENLIMITBYTE  | Length Limited. When the current length, i.e. LENGTHA or LENGTHB indicates that there are less bytes available than the register size, only length + necessary zero padding is read. Byte-wise DMA. Zero padding is automatically added when writing. |   |
| 15:14 | INCWIDTH        | 0x0   | RW  | <b>Increment Width</b><br>This field determines the number of bytes used for the increment function in data1.   |
|       | Value           | Mode  | Description   |   |
|       | 0               | INCWIDTH1   | Byte 15 in DATA1 is used for the increment function.  |   |
|       | 1               | INCWIDTH2   | Bytes 14 and 15 in DATA1 are used for the increment function.   |   |
|       | 2               | INCWIDTH3   | Bytes 13 to 15 in DATA1 are used for the increment function.  |   |
|       | 3               | INCWIDTH4   | Bytes 12 to 15 in DATA1 are used for the increment function.  |   |
| 13:11 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |
| 10    | NOBUSYSTALL     | 0   | RW  | <b>No Stalling of Bus When Busy</b><br>When set, bus accesses will not be stalled on access during an operation   |

| Bit | Name      | Reset  | Access                          | Description  |
|-----|-----------|--|---------------------------------|--|
| 9:3 | Reserved  | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |                                 |  |
| 2   | SHA       | 0  | RW                              | <b>SHA Mode</b><br>Select SHA-1 or SHA-2 mode.             |
|     | Value     | Mode   | Description                     |  |
|     | 0         | SHA1   | SHA-1 mode                      |  |
|     | 1         | SHA2   | SHA-2 mode (SHA-224 or SHA-256) |  |
| 1   | KEYBUFDIS | 0  | RW                              | <b>Key Buffer Disable</b><br>Set to Disable key buffering. |
| 0   | AES       | 0  | RW                              | <b>AES Mode</b><br>Select AES mode                         |
|     | Value     | Mode   | Description                     |  |
|     | 0         | AES128   | AES-128 mode                    |  |
|     | 1         | AES256   | AES-256 mode                    |  |

## 32.6.2 CRYPTO\_WAC - Wide Arithmetic Configuration

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |             |    |          |    |    |    |       |    |         |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|-------------|----|----------|----|----|----|-------|----|---------|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x004         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21          | 20 | 19       | 18 | 17 | 16 | 15    | 14 | 13      | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    | 0x0         |    | 0x0      |    |    |    | 0     |    | 0x0     |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    | RW          |    | RW       |    |    |    | RW    |    | RW      |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    | RESULTWIDTH |    | MULWIDTH |    |    |    | MODOP |    | MODULUS |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name            | Reset   | Access   | Description   |
|-------|-----------------|---|--|---|
| 31:12 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |   |
| 11:10 | RESULTWIDTH     | 0x0   | RW   | <b>Result Width</b><br>Result-size for non-modulus instructions                         |
|       | Value           | Mode  | Description  |   |
|       | 0               | 256BIT  | Results have 256 bits  |   |
|       | 1               | 128BIT  | Results have 128 bits  |   |
|       | 2               | 260BIT  | Results have 260 bits. Upper bits of result can be read through DDA-TA0MSBS in CRYPTO_STATUS |   |
| 9:8   | MULWIDTH        | 0x0   | RW   | <b>Multiply Width</b><br>Number of bits to multiply on non-modulus multiply instruction |
|       | Value           | Mode  | Description  |   |
|       | 0               | MUL256  | Multiply 256 bits  |   |
|       | 1               | MUL128  | Multiply 128 bits  |   |
|       | 2               | MULMOD  | Same number of bits as specified by MODULUS  |   |
| 7:5   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |   |
| 4     | MODOP           | 0   | RW   | <b>Modular Operation Field Type</b><br>Field type used for modular operations           |
|       | Value           | Mode  | Description  |   |
|       | 0               | BINARY  | Modular operations use XOR as required by certain algorithms                                 |   |
|       | 1               | REGULAR   | Modular operations use normal modular arithmetic, not XOR                                    |   |
| 3:0   | MODULUS         | 0x0   | RW   | <b>Modular Operation Modulus</b><br>Modulus used for modular operations                 |
|       | Value           | Mode  | Description  |   |
|       | 0               | BIN256  | Generic modulus. $p = 2^{256}$   |   |

| Bit | Name | Reset        | Access | Description  |
|-----|------|--------------|--------|--|
| 1   |      | BIN128       |        | Generic modulus. $p = 2^{128}$   |
| 2   |      | ECCBIN233P   |        | Modulus for B-233 and K-233 ECC curves. $p(t) = t^{233} + t^{74} + 1$          |
| 3   |      | ECCBIN163P   |        | Modulus for B-163 and K-163 ECC curves. $p(t) = t^{163} + t^7 + t^6 + t^3 + 1$ |
| 4   |      | GCMBIN128    |        | Modulus for GCM. $P(t) = t^{128} + t^7 + t^2 + t + 1$                          |
| 5   |      | ECCPRIME256P |        | Modulus for P-256 ECC curve. $p = 2^{256} - 2^{224} + 2^{192} + 2^{96} - 1$    |
| 6   |      | ECCPRIME224P |        | Modulus for P-224 ECC curve. $p = 2^{224} - 2^{96} - 1$                        |
| 7   |      | ECCPRIME192P |        | Modulus for P-192 ECC curve. $p = 2^{192} - 2^{64} - 1$                        |
| 8   |      | ECCBIN233N   |        | P modulus for B-233 ECC curve  |
| 9   |      | ECCBIN233KN  |        | P modulus for K-233 ECC curve  |
| 10  |      | ECCBIN163N   |        | P modulus for B-163 ECC curve  |
| 11  |      | ECCBIN163KN  |        | P modulus for K-163 ECC curve  |
| 12  |      | ECCPRIME256N |        | P modulus for P-256 ECC curve  |
| 13  |      | ECCPRIME224N |        | P modulus for P-224 ECC curve  |
| 14  |      | ECCPRIME192N |        | P modulus for P-192 ECC curve  |

### 32.6.3 CRYPTO\_CMD - Command Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |         |         |          |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|---------|---------|----------|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x008         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19      | 18      | 17       | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    | 0       | 0       | 0        |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    | W1      | W1      | W1       |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    | SEQSTEP | SEQSTOP | SEQSTART |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name            | Reset   | Access   | Description  |
|-------|-----------------|---|--|--|
| 31:12 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |  |
| 11    | SEQSTEP         | 0   | W1   | <b>Sequence Step</b><br>When in a halted sequence, executes the current instruction and moves to the next  |
| 10    | SEQSTOP         | 0   | W1   | <b>Sequence Stop</b><br>Set to stop encryption/decryption regardless of it being a single or a SEQUENCE.   |
| 9     | SEQSTART        | 0   | W1   | <b>Encryption/Decryption SEQUENCE Start</b><br>Set to start encryption/decryption SEQUENCE.  |
| 8     | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |  |
| 7:0   | INSTR           | 0x00  | W  | <b>Execute Instruction</b><br>Write to this field to perform any of the instructions described below. Illegal values are ignored. See <a href="#">32.4.2.2 Available Instructions</a> for details and requirements of each instruction |
|       | Value           | Mode  | Description  |  |
|       | 0               | END   | End of program   |  |
|       | 1               | EXEC  | Start executing instructions up to this point, which also marks end of program |  |
|       | 3               | DATA1INC  | See detailed instruction listing   |  |
|       | 4               | DATA1INCCLR   | See detailed instruction listing   |  |
|       | 5               | AESENC  | AES Encryption   |  |
|       | 6               | AESDEC  | AES Decryption   |  |
|       | 7               | SHA   | SHA  |  |
|       | 8               | ADD   | Add  |  |
|       | 9               | ADDC  | Add with carry   |  |
|       | 12              | MADD  | Modular addition   |  |
|       | 13              | MADD32  | Word-wise addition   |  |
|       | 16              | SUB   | Subtract   |  |
|       | 17              | SUBC  | Subtract with carry  |  |
|       | 20              | MSUB  | Modular subtraction  |  |

| Bit | Name                | Reset | Access | Description   |
|-----|---------------------|-------|--------|---|
| 24  | MUL                 |       |        | Multiply  |
| 25  | MULC                |       |        | See detailed instruction listing  |
| 28  | MMUL                |       |        | Modular multiplication  |
| 29  | MULO                |       |        | See detailed instruction listing  |
| 32  | SHL                 |       |        | Shift left  |
| 33  | SHLC                |       |        | Shift left with carry (Rotate left)   |
| 34  | SHLB                |       |        | See detailed instruction listing  |
| 35  | SHL1                |       |        | See detailed instruction listing  |
| 36  | SHR                 |       |        | Shift right   |
| 37  | SHRC                |       |        | Shift right with carry (Rotate right)                                       |
| 38  | SHRB                |       |        | See detailed instruction listing  |
| 39  | SHR1                |       |        | See detailed instruction listing  |
| 40  | ADDO                |       |        | See detailed instruction listing  |
| 41  | ADDIC               |       |        | See detailed instruction listing  |
| 48  | CLR                 |       |        | Clear DDATA0  |
| 49  | XOR                 |       |        | XOR   |
| 50  | INV                 |       |        | Invert operand  |
| 52  | CSET                |       |        | Carry set   |
| 53  | CCLR                |       |        | Carry clear   |
| 54  | BBSWAP128           |       |        | See detailed instruction listing  |
| 56  | INC                 |       |        | Increment DDATA0  |
| 57  | DEC                 |       |        | Decrement DDATA0  |
| 62  | SHRA                |       |        | Arithmetic shift right  |
| 64  | DATA0TODATA0        |       |        | DATA0 = DATA0   |
| 65  | DATA0TODATA0XOR     |       |        | DATA0 = DATA0 ^ DATA0   |
| 66  | DATA0TODATA0XOR-LEN |       |        | DATA0[ <i>len-1:0</i> ] = DATA0[ <i>len-1:0</i> ] ^ DATA0[ <i>len-1:0</i> ] |
| 68  | DATA0TODATA1        |       |        | DATA1 = DATA0   |
| 69  | DATA0TODATA2        |       |        | DATA2 = DATA0   |
| 70  | DATA0TODATA3        |       |        | DATA3 = DATA0   |
| 72  | DATA1TODATA0        |       |        | DATA0 = DATA1   |
| 73  | DATA1TODATA0XOR     |       |        | DATA0 = DATA0 ^ DATA1   |
| 74  | DATA1TODATA0XOR-LEN |       |        | DATA0[ <i>len-1:0</i> ] = DATA0[ <i>len-1:0</i> ] ^ DATA1[ <i>len-1:0</i> ] |
| 77  | DATA1TODATA2        |       |        | DATA2 = DATA1   |
| 78  | DATA1TODATA3        |       |        | DATA3 = DATA1   |
| 80  | DATA2TODATA0        |       |        | DATA0 = DATA2   |
| 81  | DATA2TODATA0XOR     |       |        | DATA0 = DATA0 ^ DATA2   |

| Bit | Name | Reset               | Access | Description  |
|-----|------|---------------------|--------|--|
| 82  |      | DATA2TODATA0XOR-LEN |        | $DATA0[\text{len}-1:0] = DATA0[\text{len}-1:0] \wedge DATA2[\text{len}-1:0]$ |
| 84  |      | DATA2TODATA1        |        | $DATA1 = DATA2$  |
| 86  |      | DATA2TODATA3        |        | $DATA3 = DATA2$  |
| 88  |      | DATA3TODATA0        |        | $DATA0 = DATA3$  |
| 89  |      | DATA3TODATA0XOR     |        | $DATA0 = DATA0 \wedge DATA3$   |
| 90  |      | DATA3TODATA0XOR-LEN |        | $DATA0[\text{len}-1:0] = DATA0[\text{len}-1:0] \wedge DATA3[\text{len}-1:0]$ |
| 92  |      | DATA3TODATA1        |        | $DATA1 = DATA3$  |
| 93  |      | DATA3TODATA2        |        | $DATA2 = DATA3$  |
| 99  |      | DATATODMA0          |        | See detailed instruction listing   |
| 100 |      | DATA0TOBUF          |        | See detailed instruction listing   |
| 101 |      | DATA0TOBUF XOR      |        | See detailed instruction listing   |
| 107 |      | DATATODMA1          |        | See detailed instruction listing   |
| 108 |      | DATA1TOBUF          |        | See detailed instruction listing   |
| 109 |      | DATA1TOBUF XOR      |        | See detailed instruction listing   |
| 112 |      | DMA0TODATA          |        | See detailed instruction listing   |
| 113 |      | DMA0TODATA XOR      |        | See detailed instruction listing   |
| 114 |      | DMA1TODATA          |        | See detailed instruction listing   |
| 120 |      | BUFTODATA0          |        | See detailed instruction listing   |
| 121 |      | BUFTODATA0 XOR      |        | See detailed instruction listing   |
| 122 |      | BUFTODATA1          |        | See detailed instruction listing   |
| 129 |      | DDATA0TODDATA1      |        | $DDATA1 = DDATA0$  |
| 130 |      | DDATA0TODDATA2      |        | $DDATA2 = DDATA0$  |
| 131 |      | DDATA0TODDATA3      |        | $DDATA3 = DDATA0$  |
| 132 |      | DDATA0TODDATA4      |        | $DDATA4 = DDATA0$  |
| 133 |      | DDATA0LTODATA0      |        | $DATA0 = DDATA0[127:0]$  |
| 134 |      | DDATA0HTODATA1      |        | $DATA1 = DDATA0[255:128]$  |
| 135 |      | DDATA0LTODATA2      |        | $DATA2 = DDATA0[127:0]$  |
| 136 |      | DDATA1TODDATA0      |        | $DDATA0 = DDATA1$  |
| 138 |      | DDATA1TODDATA2      |        | $DDATA2 = DDATA1$  |
| 139 |      | DDATA1TODDATA3      |        | $DDATA3 = DDATA1$  |
| 140 |      | DDATA1TODDATA4      |        | $DDATA4 = DDATA1$  |
| 141 |      | DDATA1LTODATA0      |        | $DATA0 = DDATA1[127:0]$  |
| 142 |      | DDATA1HTODATA1      |        | $DATA1 = DDATA1[255:128]$  |
| 143 |      | DDATA1LTODATA2      |        | $DATA2 = DDATA1[127:0]$  |
| 144 |      | DDATA2TODDATA0      |        | $DDATA0 = DDATA2$  |
| 145 |      | DDATA2TODDATA1      |        | $DDATA1 = DDATA2$  |

| Bit | Name | Reset           | Access | Description                    |
|-----|------|-----------------|--------|--------------------------------|
| 147 |      | DDATA2TODDATA3  |        | DDATA3 = DDATA2                |
| 148 |      | DDATA2TODDATA4  |        | DDATA4 = DDATA2                |
| 151 |      | DDATA2LTODATA2  |        | DATA2 = DDATA2[127:0]          |
| 152 |      | DDATA3TODDATA0  |        | DDATA0 = DDATA3                |
| 153 |      | DDATA3TODDATA1  |        | DDATA1 = DDATA3                |
| 154 |      | DDATA3TODDATA2  |        | DDATA2 = DDATA3                |
| 156 |      | DDATA3TODDATA4  |        | DDATA4 = DDATA3                |
| 157 |      | DDATA3LTODATA0  |        | DATA0 = DDATA3[127:0]          |
| 158 |      | DDATA3HTODATA1  |        | DATA1 = DDATA3[255:128]        |
| 160 |      | DDATA4TODDATA0  |        | DDATA0 = DDATA4                |
| 161 |      | DDATA4TODDATA1  |        | DDATA1 = DDATA4                |
| 162 |      | DDATA4TODDATA2  |        | DDATA2 = DDATA4                |
| 163 |      | DDATA4TODDATA3  |        | DDATA3 = DDATA4                |
| 165 |      | DDATA4LTODATA0  |        | DATA0 = DDATA4[127:0]          |
| 166 |      | DDATA4HTODATA1  |        | DATA1 = DDATA4[255:128]        |
| 167 |      | DDATA4LTODATA2  |        | DATA2 = DDATA4[127:0]          |
| 168 |      | DATA0TODDATA0   |        | DDATA0 = DATA0                 |
| 169 |      | DATA0TODDATA1   |        | DDATA1 = DATA0                 |
| 176 |      | DATA1TODDATA0   |        | DDATA0 = DATA1                 |
| 177 |      | DATA1TODDATA1   |        | DDATA1 = DATA1                 |
| 184 |      | DATA2TODDATA0   |        | DDATA0 = DATA2                 |
| 185 |      | DATA2TODDATA1   |        | DDATA1 = DATA2                 |
| 186 |      | DATA2TODDATA2   |        | DDATA2 = DATA2                 |
| 192 |      | SELDDATA0DDATA0 |        | Use DDATA0 as V0, DDATA0 as V1 |
| 193 |      | SELDDATA1DDATA0 |        | Use DDATA1 as V0, DDATA0 as V1 |
| 194 |      | SELDDATA2DDATA0 |        | Use DDATA2 as V0, DDATA0 as V1 |
| 195 |      | SELDDATA3DDATA0 |        | Use DDATA3 as V0, DDATA0 as V1 |
| 196 |      | SELDDATA4DDATA0 |        | Use DDATA4 as V0, DDATA0 as V1 |
| 197 |      | SELDATA0DDATA0  |        | Use DATA0 as V0, DDATA0 as V1  |
| 198 |      | SELDATA1DDATA0  |        | Use DATA1 as V0, DDATA1 as V1  |
| 199 |      | SELDATA2DDATA0  |        | Use DATA2 as V0, DDATA2 as V1  |
| 200 |      | SELDDATA0DDATA1 |        | Use DDATA0 as V0, DDATA1 as V1 |
| 201 |      | SELDDATA1DDATA1 |        | Use DDATA1 as V0, DDATA1 as V1 |
| 202 |      | SELDDATA2DDATA1 |        | Use DDATA2 as V0, DDATA1 as V1 |
| 203 |      | SELDDATA3DDATA1 |        | Use DDATA3 as V0, DDATA1 as V1 |
| 204 |      | SELDDATA4DDATA1 |        | Use DDATA4 as V0, DDATA1 as V1 |
| 205 |      | SELDATA0DDATA1  |        | Use DATA0 as V0, DDATA0 as V1  |

| Bit | Name | Reset           | Access | Description                    |
|-----|------|-----------------|--------|--------------------------------|
| 206 |      | SELDATA1DDATA1  |        | Use DATA1 as V0, DDATA1 as V1  |
| 207 |      | SELDATA2DDATA1  |        | Use DATA2 as V0, DDATA2 as V1  |
| 208 |      | SELDDATA0DDATA2 |        | Use DDATA0 as V0, DDATA2 as V1 |
| 209 |      | SELDDATA1DDATA2 |        | Use DDATA1 as V0, DDATA2 as V1 |
| 210 |      | SELDDATA2DDATA2 |        | Use DDATA2 as V0, DDATA2 as V1 |
| 211 |      | SELDDATA3DDATA2 |        | Use DDATA3 as V0, DDATA2 as V1 |
| 212 |      | SELDDATA4DDATA2 |        | Use DDATA4 as V0, DDATA2 as V1 |
| 213 |      | SELDATA0DDATA2  |        | Use DATA0 as V0, DDATA0 as V1  |
| 214 |      | SELDATA1DDATA2  |        | Use DATA1 as V0, DDATA1 as V1  |
| 215 |      | SELDATA2DDATA2  |        | Use DATA2 as V0, DDATA2 as V1  |
| 216 |      | SELDDATA0DDATA3 |        | Use DDATA0 as V0, DDATA3 as V1 |
| 217 |      | SELDDATA1DDATA3 |        | Use DDATA1 as V0, DDATA3 as V1 |
| 218 |      | SELDDATA2DDATA3 |        | Use DDATA2 as V0, DDATA3 as V1 |
| 219 |      | SELDDATA3DDATA3 |        | Use DDATA3 as V0, DDATA3 as V1 |
| 220 |      | SELDDATA4DDATA3 |        | Use DDATA4 as V0, DDATA3 as V1 |
| 221 |      | SELDATA0DDATA3  |        | Use DATA0 as V0, DDATA0 as V1  |
| 222 |      | SELDATA1DDATA3  |        | Use DATA1 as V0, DDATA1 as V1  |
| 223 |      | SELDATA2DDATA3  |        | Use DATA2 as V0, DDATA2 as V1  |
| 224 |      | SELDDATA0DDATA4 |        | Use DDATA0 as V0, DDATA4 as V1 |
| 225 |      | SELDDATA1DDATA4 |        | Use DDATA1 as V0, DDATA4 as V1 |
| 226 |      | SELDDATA2DDATA4 |        | Use DDATA2 as V0, DDATA4 as V1 |
| 227 |      | SELDDATA3DDATA4 |        | Use DDATA3 as V0, DDATA4 as V1 |
| 228 |      | SELDDATA4DDATA4 |        | Use DDATA4 as V0, DDATA4 as V1 |
| 229 |      | SELDATA0DDATA4  |        | Use DATA0 as V0, DDATA4 as V1  |
| 230 |      | SELDATA1DDATA4  |        | Use DATA1 as V0, DDATA4 as V1  |
| 231 |      | SELDATA2DDATA4  |        | Use DATA2 as V0, DDATA4 as V1  |
| 232 |      | SELDDATA0DATA0  |        | Use DDATA0 as V0, DATA0 as V1  |
| 233 |      | SELDDATA1DATA0  |        | Use DDATA1 as V0, DATA0 as V1  |
| 234 |      | SELDDATA2DATA0  |        | Use DDATA2 as V0, DATA0 as V1  |
| 235 |      | SELDDATA3DATA0  |        | Use DDATA3 as V0, DATA0 as V1  |
| 236 |      | SELDDATA4DATA0  |        | Use DDATA4 as V0, DATA0 as V1  |
| 237 |      | SELDATA0DATA0   |        | Use DATA0 as V0, DATA0 as V1   |
| 238 |      | SELDATA1DATA0   |        | Use DATA1 as V0, DATA0 as V1   |
| 239 |      | SELDATA2DATA0   |        | Use DATA2 as V0, DATA0 as V1   |
| 240 |      | SELDDATA0DATA1  |        | Use DDATA0 as V0, DATA1 as V1  |
| 241 |      | SELDDATA1DATA1  |        | Use DDATA1 as V0, DATA1 as V1  |
| 242 |      | SELDDATA2DATA1  |        | Use DDATA2 as V0, DATA1 as V1  |

| Bit | Name | Reset          | Access | Description   |
|-----|------|----------------|--------|---|
| 243 |      | SELDDATA3DATA1 |        | Use DDATA3 as V0, DATA1 as V1                                   |
| 244 |      | SELDDATA4DATA1 |        | Use DDATA4 as V0, DATA1 as V1                                   |
| 245 |      | SELDATA0DATA1  |        | Use DATA0 as V0, DATA1 as V1                                    |
| 246 |      | SELDATA1DATA1  |        | Use DATA1 as V0, DATA1 as V1                                    |
| 247 |      | SELDATA2DATA1  |        | Use DATA2 as V0, DATA1 as V1                                    |
| 248 |      | EXECIFA        |        | Run following if in A sequence                                  |
| 249 |      | EXECIFB        |        | Run following if in B sequence                                  |
| 250 |      | EXECIFNLAST    |        | Run following if in last iteration of combined A and B sequence |
| 251 |      | EXECIFLAST     |        | Run following if in last iteration of combined A and B sequence |
| 252 |      | EXECIFCARRY    |        | Run following if CARRY bit is set                               |
| 253 |      | EXECIFNCARRY   |        | Run following if CARRY bit is not set                           |
| 254 |      | EXECALWAYS     |        | Resume execution  |

### 32.6.4 CRYPTO\_STATUS - Status Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |           |    |             |    |            |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------|----|-------------|----|------------|----|---|---|---|---|---|---|---|---|---|---|
| 0x010         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15        | 14 | 13          | 12 | 11         | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R         | 0  | R           | 0  | R          | 0  |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R         |    | R           |    | R          |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DMAACTIVE |    | INSTRUNNING |    | SEQRUNNING |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 31:3 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 2    | DMAACTIVE       | 0   | R      | <b>DMA Action is Active</b><br><br>This bit indicates that the AES module is waiting for a DMA transfer to complete.  |
| 1    | INSTRUNNING     | 0   | R      | <b>Action is Active</b><br><br>This bit indicates that the AES module busy executing an instruction. The origin of the instruction is either through CRYPTO_CMD or due to a running SEQUENCE. |
| 0    | SEQRUNNING      | 0   | R      | <b>AES SEQUENCE Running</b><br><br>This bit indicates that the AES module is running an encryption/decryption SEQUENCE.   |

### 32.6.5 CRYPTO\_DSTATUS - Data Status Register

| Offset        | Bit Position |    |    |    |    |    |    |       |    |    |    |    |    |           |            |    |    |    |    |    |    |    |            |   |   |   |           |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|-------|----|----|----|----|----|-----------|------------|----|----|----|----|----|----|----|------------|---|---|---|-----------|---|---|---|---|---|
| 0x014         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24    | 23 | 22 | 21 | 20 | 19 | 18        | 17         | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9          | 8 | 7 | 6 | 5         | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    | 0     |    |    |    |    |    | X         | 0xX        |    |    |    |    |    |    |    | 0xX        |   |   |   |           |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    | R     |    |    |    |    |    | R         | R          |    |    |    |    |    |    |    | R          |   |   |   |           |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    | CARRY |    |    |    |    |    | DDATA1MSB | DDATA0MSBS |    |    |    |    |    |    |    | DDATA0LSBS |   |   |   | DATA0ZERO |   |   |   |   |   |

| Bit   | Name       | Reset   | Access                                | Description   |
|-------|------------|---|---------------------------------------|---|
| 31:25 | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                       |   |
| 24    | CARRY      | 0   | R                                     | <b>Carry From Arithmetic Operation</b><br>Set on carry from arithmetic operations                     |
| 23:21 | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                       |   |
| 20    | DDATA1MSB  | X   | R                                     | <b>MSB in DDATA1</b><br>Allows read of 255 in DDATA1. Does not depend on RESULTWIDTH in CRYPTO_WAC    |
| 19:16 | DDATA0MSBS | 0xX   | R                                     | <b>MSB in DDATA0</b><br>Allows read of 4 MSBs in DDATA0. The bits depend on RESULTWIDTH in CRYPTO_WAC |
| 15:12 | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                       |   |
| 11:8  | DDATA0LSBS | 0xX   | R                                     | <b>LSBs in DDATA0</b><br>Allows read of 4 LSBs in DDATA0  |
| 7:4   | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                                       |   |
| 3:0   | DATA0ZERO  | 0xX   | R                                     | <b>Data 0 Zero</b><br>This field contains flags indicating if any 32 bit part of DATA0 is 0.          |
|       | Value      | Mode  | Description                           |   |
|       | 1          | ZERO0TO31   | In DATA0 bits 0 to 31 are all zero.   |   |
|       | 2          | ZERO32TO63  | In DATA0 bits 32 to 63 are all zero.  |   |
|       | 4          | ZERO64TO95  | In DATA0 bits 64 to 95 are all zero.  |   |
|       | 8          | ZERO96TO127   | In DATA0 bits 96 to 127 are all zero. |   |

### 32.6.6 CRYPTO\_CSTATUS - Control Status Register

| Offset        | Bit Position |    |    |    |    |    |    |    |       |    |    |    |         |    |         |    |    |    |    |    |    |    |   |   |     |   |    |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|-------|----|----|----|---------|----|---------|----|----|----|----|----|----|----|---|---|-----|---|----|---|---|---|---|---|
| 0x018         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23    | 22 | 21 | 20 | 19      | 18 | 17      | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7   | 6 | 5  | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    | 0x00  |    |    |    | 0       |    | 0       |    |    |    |    |    |    |    |   |   | 0x1 |   |    |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    | R     |    |    |    | R       |    | R       |    |    |    |    |    |    |    |   |   | R   |   |    |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    | SEQIP |    |    |    | SEQSKIP |    | SEQPART |    |    |    |    |    |    |    |   |   | V1  |   | V0 |   |   |   |   |   |

| Bit   | Name            | Reset   | Access      | Description  |
|-------|-----------------|---|-------------|--|
| 31:25 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 24:20 | SEQIP           | 0x00  | R           | <b>Sequence Next Instruction Pointer</b><br>Next sequence instruction when in halted sequence                    |
| 19:18 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 17    | SEQSKIP         | 0   | R           | <b>Sequence Skip Next Instruction</b><br>When in halted sequence, tells whether next instruction will be skipped |
| 16    | SEQPART         | 0   | R           | <b>Sequence Part</b><br>Shows whether currently in part A or B of a sequence                                     |
|       | Value           | Mode  | Description |  |
|       | 0               | SEQA  |             |  |
|       | 1               | SEQB  |             |  |
| 15:11 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 10:8  | V1              | 0x2   | R           | <b>Selected ALU Operand 1</b><br>Selectable operand for arithmetic operations                                    |
|       | Value           | Mode  | Description |  |
|       | 0               | DDATA0  |             |  |
|       | 1               | DDATA1  |             |  |
|       | 2               | DDATA2  |             |  |
|       | 3               | DDATA3  |             |  |
|       | 4               | DDATA4  |             |  |
|       | 5               | DATA0   |             |  |
|       | 6               | DATA1   |             |  |
|       | 7               | DATA2   |             |  |
| 7:3   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |

| Bit  | Name  | Reset  | Access      | Description                   |
|--|-------|--------|-------------|-------------------------------|
| 2:0  | V0    | 0x1    | R           | <b>Selected ALU Operand 0</b> |
| Selectable operand for arithmetic operations |       |        |             |                               |
|  | Value | Mode   | Description |                               |
|  | 0     | DDATA0 |             |                               |
|  | 1     | DDATA1 |             |                               |
|  | 2     | DDATA2 |             |                               |
|  | 3     | DDATA3 |             |                               |
|  | 4     | DDATA4 |             |                               |
|  | 5     | DATA0  |             |                               |
|  | 6     | DATA1  |             |                               |
|  | 7     | DATA2  |             |                               |

### 32.6.7 CRYPTO\_KEY - KEY Register Access (No Bit Access) (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |     |             |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----|-------------|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x020         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15  | 14          | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | KEY | 0XXXXXXXXXX |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | KEY | RWH         |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | KEY |             |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit   | Name | Reset           | Access | Description       |
|---|------|-----------------|--------|-------------------|
| 31:0  | KEY  | 0XXXXXXXXX<br>X | RWH    | <b>Key Access</b> |
| Access the KEY. 4x32bits (8x32bits if AES256 in CRYPTO_CTRL is set) read/write accesses are required to fully read/write KEY. |      |                 |        |                   |

**32.6.8 CRYPTO\_KEYBUF - KEY Buffer Register Access (No Bit Access) (Actionable Reads)**

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x024         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0XXXXXXXXXX |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | KEYBUF      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit   | Name   | Reset           | Access | Description              |
|---|--------|-----------------|--------|--------------------------|
| 31:0  | KEYBUF | 0XXXXXXXXX<br>X | RWH    | <b>Key Buffer Access</b> |
| Access to KEYBUF. 4x32bits (8x32bits if AES256 in CRYPTO_CTRL is set) read/write accesses are required to fully read/write KEYBUF |        |                 |        |                          |

### 32.6.9 CRYPTO\_SEQCTRL - Sequence Control

| Offset        | Bit Position |    |           |           |          |    |          |    |    |    |           |    |    |    |    |    |    |    |    |    |    |    |   |   |   |         |   |   |   |   |   |   |  |
|---------------|--------------|----|-----------|-----------|----------|----|----------|----|----|----|-----------|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---------|---|---|---|---|---|---|--|
| 0x030         | 31           | 30 | 29        | 28        | 27       | 26 | 25       | 24 | 23 | 22 | 21        | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6       | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  | 0            |    | 0         | 0         | 0x0      |    | 0x0      |    |    |    | 0x0       |    |    |    |    |    |    |    |    |    |    |    |   |   |   | 0x0000  |   |   |   |   |   |   |  |
| <b>Access</b> | RW           |    | RW        | RW        | RWH      |    | RWH      |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |    |   |   |   | RWH     |   |   |   |   |   |   |  |
| <b>Name</b>   | HALT         |    | DMA1PRESA | DMA0PRESA | DMA1SKIP |    | DMA0SKIP |    |    |    | BLOCKSIZE |    |    |    |    |    |    |    |    |    |    |    |   |   |   | LENGTHA |   |   |   |   |   |   |  |

| Bit   | Name            | Reset   | Access                   | Description   |
|-------|-----------------|---|--------------------------|---|
| 31    | HALT            | 0   | RW                       | <b>Halt Sequence</b><br>Allows stepping through CRYPTO instructions in the sequence for debugging.  |
| 30    | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                          |   |
| 29    | DMA1PRESA       | 0   | RW                       | <b>DMA1 Preserve a</b><br>Set to write skipped bytes back on next DMA1WR triggered write. Use this together with DMA1SKIP to enable in-place conversions with CRYPTO  |
| 28    | DMA0PRESA       | 0   | RW                       | <b>DMA0 Preserve a</b><br>Set to write skipped bytes back on next DMA0WR triggered write. Use this together with DMA0SKIP to enable in-place conversions with CRYPTO  |
| 27:26 | DMA1SKIP        | 0x0   | RWH                      | <b>DMA1 Skip</b><br>Set to number of bytes to exclude from data received by next DMA1RD instruction   |
| 25:24 | DMA0SKIP        | 0x0   | RWH                      | <b>DMA0 Skip</b><br>Set to number of bytes to exclude from data received by next DMA0RD instruction   |
| 23:22 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                          |   |
| 21:20 | BLOCKSIZE       | 0x0   | RW                       | <b>Size of Data Blocks</b><br>Defines the width of blocks processed in each iteration of a sequence running on a dataset (see related note in <a href="#">32.4.3 Repeated Sequence</a> )  |
|       | Value           | Mode  | Description              |   |
|       | 0               | 16BYTES   | A block is 16 bytes long |   |
|       | 1               | 32BYTES   | A block is 32 bytes long |   |
|       | 2               | 64BYTES   | A block is 64 bytes long |   |
| 19:14 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                          |   |
| 13:0  | LENGTHA         | 0x0000  | RWH                      | <b>Buffer Length a in Bytes</b><br>This field sets the number of bytes to be handled during the repeated sequence. Set it to the exact number of bytes. If the number is not a multiple of BLOCKSIZE, the last data block is zero-padded. Format is unsigned integer. |

### 32.6.10 CRYPTO\_SEQCTRLB - Sequence Control B

| Offset        | Bit Position |    |           |           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|-----------|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|---|---|---|---|---|---|---|---|---|---|
| 0x034         | 31           | 30 | 29        | 28        | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11      | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    | 0         | 0         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000  |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    | RW        | RW        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH     |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    | DMA1PRESB | DMA0PRESB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LENGTHB |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name      | Reset   | Access | Description  |
|-------|-----------|---|--------|--|
| 31:30 | Reserved  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 29    | DMA1PRESB | 0   | RW     | <b>DMA1 Preserve B</b><br><br>For unaligned sequences, set this bit along with DMA1PRESA for in-place conversions where all data is written out from CRYPTO again. If only the second part of a data-set is written, enable only this to preserve the data read in during part A |
| 28    | DMA0PRESB | 0   | RW     | <b>DMA0 Preserve B</b><br><br>For unaligned sequences, set this bit along with DMA0PRESA for in-place conversions where all data is written out from CRYPTO again. If only the second part of a data-set is written, enable only this to preserve the data read in during part A |
| 27:14 | Reserved  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 13:0  | LENGTHB   | 0x0000  | RWH    | <b>Buffer Length B in Bytes</b><br><br>Sets the number of bytes to be handled in a second iteration over a programmed sequence.  |









### 32.6.16 CRYPTO\_SEQ1 - Sequence Register 1

| Offset        | Bit Position |    |    |    |    |    |    |    |        |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |        |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|--------|---|---|---|---|---|---|---|
| 0x054         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0x00         |    |    |    |    |    |    |    | 0x00   |    |    |    |    |    |    |    | 0x00   |    |    |    |    |    |   |   | 0x00   |   |   |   |   |   |   |   |
| <b>Access</b> | RW           |    |    |    |    |    |    |    | RW     |    |    |    |    |    |    |    | RW     |    |    |    |    |    |   |   | RW     |   |   |   |   |   |   |   |
| <b>Name</b>   | INSTR7       |    |    |    |    |    |    |    | INSTR6 |    |    |    |    |    |    |    | INSTR5 |    |    |    |    |    |   |   | INSTR4 |   |   |   |   |   |   |   |

| Bit   | Name   | Reset | Access | Description   |
|-------|--------|-------|--------|---|
| 31:24 | INSTR7 | 0x00  | RW     | <b>Sequence Instruction 7</b><br>Sequence instruction. See INSTR in CRYPTO_CMD for a possible values. |
| 23:16 | INSTR6 | 0x00  | RW     | <b>Sequence Instruction 6</b><br>Sequence instruction. See INSTR in CRYPTO_CMD for a possible values. |
| 15:8  | INSTR5 | 0x00  | RW     | <b>Sequence Instruction 5</b><br>Sequence instruction. See INSTR in CRYPTO_CMD for a possible values. |
| 7:0   | INSTR4 | 0x00  | RW     | <b>Sequence Instruction 4</b><br>Sequence instruction. See INSTR in CRYPTO_CMD for a possible values. |

### 32.6.17 CRYPTO\_SEQ2 - Sequence Register 2

| Offset        | Bit Position |    |    |    |    |    |    |    |         |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |        |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|---------|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|--------|---|---|---|---|---|---|---|
| 0x058         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0x00         |    |    |    |    |    |    |    | 0x00    |    |    |    |    |    |    |    | 0x00   |    |    |    |    |    |   |   | 0x00   |   |   |   |   |   |   |   |
| <b>Access</b> | RW           |    |    |    |    |    |    |    | RW      |    |    |    |    |    |    |    | RW     |    |    |    |    |    |   |   | RW     |   |   |   |   |   |   |   |
| <b>Name</b>   | INSTR11      |    |    |    |    |    |    |    | INSTR10 |    |    |    |    |    |    |    | INSTR9 |    |    |    |    |    |   |   | INSTR8 |   |   |   |   |   |   |   |

| Bit   | Name    | Reset | Access | Description  |
|-------|---------|-------|--------|--|
| 31:24 | INSTR11 | 0x00  | RW     | <b>Sequence Instruction 11</b><br>Sequence instruction. See INSTR in CRYPTO_CMD for a possible values. |
| 23:16 | INSTR10 | 0x00  | RW     | <b>Sequence Instruction 10</b><br>Sequence instruction. See INSTR in CRYPTO_CMD for a possible values. |
| 15:8  | INSTR9  | 0x00  | RW     | <b>Sequence Instruction 9</b><br>Sequence instruction. See INSTR in CRYPTO_CMD for a possible values.  |
| 7:0   | INSTR8  | 0x00  | RW     | <b>Sequence Instruction 8</b><br>Sequence instruction. See INSTR in CRYPTO_CMD for a possible values.  |

### 32.6.18 CRYPTO\_SEQ3 - Sequence Register 3

| Offset        | Bit Position |    |    |    |    |    |    |    |         |    |    |    |    |    |    |    |         |    |    |    |    |    |   |   |         |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|---------|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---------|---|---|---|---|---|---|---|
| 0x05C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0x00         |    |    |    |    |    |    |    | 0x00    |    |    |    |    |    |    |    | 0x00    |    |    |    |    |    |   |   | 0x00    |   |   |   |   |   |   |   |
| <b>Access</b> | RW           |    |    |    |    |    |    |    | RW      |    |    |    |    |    |    |    | RW      |    |    |    |    |    |   |   | RW      |   |   |   |   |   |   |   |
| <b>Name</b>   | INSTR15      |    |    |    |    |    |    |    | INSTR14 |    |    |    |    |    |    |    | INSTR13 |    |    |    |    |    |   |   | INSTR12 |   |   |   |   |   |   |   |

| Bit   | Name    | Reset | Access | Description  |
|-------|---------|-------|--------|--|
| 31:24 | INSTR15 | 0x00  | RW     | <b>Sequence Instruction 15</b><br>Sequence instruction. See INSTR in CRYPTO_CMD for a possible values. |
| 23:16 | INSTR14 | 0x00  | RW     | <b>Sequence Instruction 14</b><br>Sequence instruction. See INSTR in CRYPTO_CMD for a possible values. |
| 15:8  | INSTR13 | 0x00  | RW     | <b>Sequence Instruction 13</b><br>Sequence instruction. See INSTR in CRYPTO_CMD for a possible values. |
| 7:0   | INSTR12 | 0x00  | RW     | <b>Sequence Instruction 12</b><br>Sequence instruction. See INSTR in CRYPTO_CMD for a possible values. |

### 32.6.19 CRYPTO\_SEQ4 - Sequence Register 4

| Offset        | Bit Position |    |    |    |    |    |    |    |         |    |    |    |    |    |    |    |         |    |    |    |    |    |   |   |         |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|---------|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---------|---|---|---|---|---|---|---|
| 0x060         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0x00         |    |    |    |    |    |    |    | 0x00    |    |    |    |    |    |    |    | 0x00    |    |    |    |    |    |   |   | 0x00    |   |   |   |   |   |   |   |
| <b>Access</b> | RW           |    |    |    |    |    |    |    | RW      |    |    |    |    |    |    |    | RW      |    |    |    |    |    |   |   | RW      |   |   |   |   |   |   |   |
| <b>Name</b>   | INSTR19      |    |    |    |    |    |    |    | INSTR18 |    |    |    |    |    |    |    | INSTR17 |    |    |    |    |    |   |   | INSTR16 |   |   |   |   |   |   |   |

| Bit   | Name    | Reset | Access | Description  |
|-------|---------|-------|--------|--|
| 31:24 | INSTR19 | 0x00  | RW     | <b>Sequence Instruction 19</b><br>Sequence instruction. See INSTR in CRYPTO_CMD for a possible values. |
| 23:16 | INSTR18 | 0x00  | RW     | <b>Sequence Instruction 18</b><br>Sequence instruction. See INSTR in CRYPTO_CMD for a possible values. |
| 15:8  | INSTR17 | 0x00  | RW     | <b>Sequence Instruction 17</b><br>Sequence instruction. See INSTR in CRYPTO_CMD for a possible values. |
| 7:0   | INSTR16 | 0x00  | RW     | <b>Sequence Instruction 16</b><br>Sequence instruction. See INSTR in CRYPTO_CMD for a possible values. |

### 32.6.20 CRYPTO\_DATA0 - DATA0 Register Access (No Bit Access) (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x080         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0XXXXXXXXX |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DATA0      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit  | Name  | Reset           | Access | Description          |
|--|-------|-----------------|--------|----------------------|
| 31:0   | DATA0 | 0XXXXXXXXX<br>X | RWH    | <b>Data 0 Access</b> |
| Access to DATA0. 4x32bits read/write accesses are required to fully read/write DATA0 |       |                 |        |                      |

### 32.6.21 CRYPTO\_DATA1 - DATA1 Register Access (No Bit Access) (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x084         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0XXXXXXXXX |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DATA1      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit  | Name  | Reset           | Access | Description          |
|--|-------|-----------------|--------|----------------------|
| 31:0   | DATA1 | 0XXXXXXXXX<br>X | RWH    | <b>Data 1 Access</b> |
| Access to DATA1. 4x32bits read/write accesses are required to fully read/write DATA1 |       |                 |        |                      |

### 32.6.22 CRYPTO\_DATA2 - DATA2 Register Access (No Bit Access) (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x088         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0XXXXXXXXX |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DATA2      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit   | Name  | Reset           | Access | Description          |
|---|-------|-----------------|--------|----------------------|
| 31:0  | DATA2 | 0XXXXXXXXX<br>X | RWH    | <b>Data 2 Access</b> |
| Access to DATA2. 4x32bits read/write accesses are required to fully read/write DATA2. |       |                 |        |                      |

### 32.6.23 CRYPTO\_DATA3 - DATA3 Register Access (No Bit Access) (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x08C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0XXXXXXXXX |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DATA3      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit   | Name  | Reset           | Access | Description          |
|---|-------|-----------------|--------|----------------------|
| 31:0  | DATA3 | 0XXXXXXXXX<br>X | RWH    | <b>Data 3 Access</b> |
| Access to DATA3. 4x32bits read/write accesses are required to fully read/write DATA3. |       |                 |        |                      |

### 32.6.24 CRYPTO\_DATA0XOR - DATA0XOR Register Access (No Bit Access) (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x0A0         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0XXXXXXXXXX |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DATA0XOR    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
|-----|------|-------|--------|-------------|

|      |          |                 |     |                          |
|------|----------|-----------------|-----|--------------------------|
| 31:0 | DATA0XOR | 0XXXXXXXXX<br>X | RWH | <b>XOR Data 0 Access</b> |
|------|----------|-----------------|-----|--------------------------|

Any value written to this register will be XOR'ed with the value of DATA0. The result is stored in DATA0. Reads return DATA0 directly. 4x32bits read/write accesses are required to perform a full XOR write to DATA0

### 32.6.25 CRYPTO\_DATA0BYTE - DATA0 Register Byte Access (No Bit Access) (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x0B0         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
|-----|------|-------|--------|-------------|

|      |                 |   |  |  |
|------|-----------------|---|--|--|
| 31:8 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |  |
|------|-----------------|---|--|--|

|     |           |      |     |                           |
|-----|-----------|------|-----|---------------------------|
| 7:0 | DATA0BYTE | 0xXX | RWH | <b>Data 0 Byte Access</b> |
|-----|-----------|------|-----|---------------------------|

Access to DATA0. 16x8bits read/write accesses are required to fully read/write DATA0. Accesses must be performed in multiples of 4, or data incoherency may occur

### 32.6.26 CRYPTO\_DATA1BYTE - DATA1 Register Byte Access (No Bit Access) (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |           |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|-----------|---|---|---|---|---|---|---|
| 0x0B4         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0xXX      |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RWH       |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | DATA1BYTE |   |   |   |   |   |   |   |

| Bit  | Name      | Reset  | Access | Description  |
|------|-----------|--|--------|--|
| 31:8 | Reserved  | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 7:0  | DATA1BYTE | 0xXX   | RWH    | <b>Data 1 Byte Access</b><br>Access to DATA1. 16x8bits read/write accesses are required to fully read/write DATA1. Accesses must be performed in multiples of 4, or data incoherency may occur |

### 32.6.27 CRYPTO\_DATA0XORBYTE - DATA0 Register Byte XOR Access (No Bit Access) (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |              |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|--------------|---|---|---|---|---|---|---|
| 0x0BC         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0xXX         |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RWH          |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | DATA0XORBYTE |   |   |   |   |   |   |   |

| Bit  | Name         | Reset  | Access | Description   |
|------|--------------|--|--------|---|
| 31:8 | Reserved     | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 7:0  | DATA0XORBYTE | 0xXX   | RWH    | <b>Data 0 XOR Byte Access</b><br>Access to DATA0. 16x8bits read/write accesses are required to fully read/write DATA0. Written data is XOR'ed with the already present data in DATA0. Accesses must be performed in multiples of 4, or data incoherency may occur |

### 32.6.28 CRYPTO\_DATA0BYTE12 - DATA0 Register Byte 12 Access (No Bit Access)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |             |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|-------------|---|---|---|
| 0x0C0         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3           | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0xXX        |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | RWH         |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | DATA0BYTE12 |   |   |   |

| Bit  | Name        | Reset  | Access | Description  |
|------|-------------|--|--------|--|
| 31:8 | Reserved    | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 7:0  | DATA0BYTE12 | 0xXX   | RWH    | <b>Data 0 Byte 12 Access</b><br>Access to DATA0 byte 12. |

### 32.6.29 CRYPTO\_DATA0BYTE13 - DATA0 Register Byte 13 Access (No Bit Access)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |             |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|-------------|---|---|---|
| 0x0C4         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3           | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0xXX        |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | RWH         |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | DATA0BYTE13 |   |   |   |

| Bit  | Name        | Reset  | Access | Description  |
|------|-------------|--|--------|--|
| 31:8 | Reserved    | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 7:0  | DATA0BYTE13 | 0xXX   | RWH    | <b>Data 0 Byte 13 Access</b><br>Access to DATA0 byte 13. |

## 32.6.30 CRYPTO\_DATA0BYTE14 - DATA0 Register Byte 14 Access (No Bit Access)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |             |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|-------------|---|---|---|
| 0x0C8         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3           | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0xXX        |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | RWH         |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | DATA0BYTE14 |   |   |   |

| Bit  | Name        | Reset  | Access | Description  |
|------|-------------|--|--------|--|
| 31:8 | Reserved    | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 7:0  | DATA0BYTE14 | 0xXX   | RWH    | <b>Data 0 Byte 14 Access</b><br>Access to DATA0 byte 14. |

## 32.6.31 CRYPTO\_DATA0BYTE15 - DATA0 Register Byte 15 Access (No Bit Access)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |             |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|-------------|---|---|---|
| 0x0CC         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3           | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0xXX        |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | RWH         |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | DATA0BYTE15 |   |   |   |

| Bit  | Name        | Reset  | Access | Description  |
|------|-------------|--|--------|--|
| 31:8 | Reserved    | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 7:0  | DATA0BYTE15 | 0xXX   | RWH    | <b>Data 0 Byte 15 Access</b><br>Access to DATA0 byte 15. |

### 32.6.32 CRYPTO\_DDATA0 - DDATA0 Register Access (No Bit Access) (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x100         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0XXXXXXXXX |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DDATA0     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
|-----|------|-------|--------|-------------|

|      |        |                 |     |                             |
|------|--------|-----------------|-----|-----------------------------|
| 31:0 | DDATA0 | 0XXXXXXXXX<br>X | RWH | <b>Double Data 0 Access</b> |
|------|--------|-----------------|-----|-----------------------------|

Access to DDATA0. 8x32bits read/write accesses are required to fully read/write DDATA0.

### 32.6.33 CRYPTO\_DDATA1 - DDATA1 Register Access (No Bit Access) (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x104         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0XXXXXXXXX |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DDATA1     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
|-----|------|-------|--------|-------------|

|      |        |                 |     |                             |
|------|--------|-----------------|-----|-----------------------------|
| 31:0 | DDATA1 | 0XXXXXXXXX<br>X | RWH | <b>Double Data 0 Access</b> |
|------|--------|-----------------|-----|-----------------------------|

Access to DDATA1, which is equal to the full width of KEY regardless of AES256 in CRYPTO\_CTRL. 8x32bits read/write accesses are required to fully read/write DDATA1.

### 32.6.34 CRYPTO\_DDATA2 - DDATA2 Register Access (No Bit Access) (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x108         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0XXXXXXXXX |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DDATA2     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit   | Name   | Reset           | Access | Description                 |
|---|--------|-----------------|--------|-----------------------------|
| 31:0  | DDATA2 | 0XXXXXXXXX<br>X | RWH    | <b>Double Data 0 Access</b> |
| Access to DDATA2, which consists of {DATA1, DATA0}. 8x32bits read/write accesses are required to fully read/write DDATA2. |        |                 |        |                             |

### 32.6.35 CRYPTO\_DDATA3 - DDATA3 Register Access (No Bit Access) (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x10C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0XXXXXXXXX |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DDATA3     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit   | Name   | Reset           | Access | Description                 |
|---|--------|-----------------|--------|-----------------------------|
| 31:0  | DDATA3 | 0XXXXXXXXX<br>X | RWH    | <b>Double Data 0 Access</b> |
| Access to DDATA3, which consists of {DATA3, DATA2}. 8x32bits read/write accesses are required to fully read/write DDATA3. |        |                 |        |                             |

**32.6.36 CRYPTO\_DDATA4 - DDATA4 Register Access (No Bit Access) (Actionable Reads)**

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x110         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0XXXXXXXXX |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DDATA4     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
|-----|------|-------|--------|-------------|

|      |        |                 |     |                             |
|------|--------|-----------------|-----|-----------------------------|
| 31:0 | DDATA4 | 0XXXXXXXXX<br>X | RWH | <b>Double Data 0 Access</b> |
|------|--------|-----------------|-----|-----------------------------|

Access to DDATA4, which is equal to the full width of KEYBUF regardless of AES256 in CRYPTO\_CTRL. 8x32bits read/write accesses are required to fully read/write DDATA4.

**32.6.37 CRYPTO\_DDATA0BIG - DDATA0 Register Big Endian Access (No Bit Access) (Actionable Reads)**

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x130         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0XXXXXXXXX |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DDATA0BIG  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
|-----|------|-------|--------|-------------|

|      |           |                 |     |  |
|------|-----------|-----------------|-----|--|
| 31:0 | DDATA0BIG | 0XXXXXXXXX<br>X | RWH | <b>Double Data 0 Big Endian Access</b> |
|------|-----------|-----------------|-----|--|

Big endian access to DDATA0. 8x32bits read/write accesses are required to fully read/write DDATA0.

### 32.6.38 CRYPTO\_DDATA0BYTE - DDATA0 Register Byte Access (No Bit Access) (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |            |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|------------|---|---|---|---|---|---|---|
| 0x140         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0xXX       |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RWH        |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | DDATA0BYTE |   |   |   |   |   |   |   |

| Bit  | Name       | Reset   | Access | Description   |
|------|------------|---|--------|---|
| 31:8 | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 7:0  | DDATA0BYTE | 0xXX  | RWH    | <b>Ddata 0 Byte Access</b><br>Access to DDATA0. 32x8bits read/write accesses are required to fully read/write DDATA0. Accesses must be performed in multiples of 4, or data incoherency may occur |

### 32.6.39 CRYPTO\_DDATA1BYTE - DDATA1 Register Byte Access (No Bit Access) (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |            |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|------------|---|---|---|---|---|---|---|
| 0x144         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0xXX       |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RWH        |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | DDATA1BYTE |   |   |   |   |   |   |   |

| Bit  | Name       | Reset   | Access | Description   |
|------|------------|---|--------|---|
| 31:8 | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 7:0  | DDATA1BYTE | 0xXX  | RWH    | <b>Ddata 1 Byte Access</b><br>Access to DDATA1. 32x8bits read/write accesses are required to fully read/write DDATA1. Accesses must be performed in multiples of 4, or data incoherency may occur |

### 32.6.40 CRYPTO\_DDATA0BYTE32 - DDATA0 Register Byte 32 Access (No Bit Access)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |              |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|--------------|---|---|---|
| 0x148         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3            | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | 0xX          | 0 |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | RWH          |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   | DDATA0BYTE32 |   |   |   |

| Bit  | Name         | Reset | Access | Description  |
|------|--------------|-------|--------|--|
| 31:4 | Reserved     |       |        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |
| 3:0  | DDATA0BYTE32 | 0xX   | RWH    | <b>Ddata 0 Byte 32 Access</b><br>Access to DDATA0 byte 32. This is used when RESULTWIDTH in CRYPTO_WAC is set to 260BIT. |

### 32.6.41 CRYPTO\_QDATA0 - QDATA0 Register Access (No Bit Access) (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x180         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0XXXXXXXXXX |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | QDATA0      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name   | Reset           | Access | Description   |
|------|--------|-----------------|--------|---|
| 31:0 | QDATA0 | 0XXXXXXXXX<br>X | RWH    | <b>Quad Data 0 Access</b><br>Access to QDATA0, which is equal to {DDATA1, DDATA0}. 16x32bits read/write accesses are required to fully read/write QDATA0. |

### 32.6.42 CRYPTO\_QDATA1 - QDATA1 Register Access (No Bit Access) (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x184         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0XXXXXXXXX |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | QDATA1     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
|-----|------|-------|--------|-------------|

|  |        |                 |     |                           |
|--|--------|-----------------|-----|---------------------------|
| 31:0   | QDATA1 | 0XXXXXXXXX<br>X | RWH | <b>Quad Data 1 Access</b> |
| <p>Access to QDATA1, which is equal to {DATA3, DATA2, DATA1, DATA0} and {DDATA3, DDATA2}. 16x32bits read/write accesses are required to fully read/write QDATA1.</p> |        |                 |     |                           |

### 32.6.43 CRYPTO\_QDATA1BIG - QDATA1 Register Big Endian Access (No Bit Access) (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|
| 0x1A4         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0XXXXXXXXX |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | QDATA1BIG  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
|-----|------|-------|--------|-------------|

|   |           |                 |     |                                      |
|---|-----------|-----------------|-----|--------------------------------------|
| 31:0  | QDATA1BIG | 0XXXXXXXXX<br>X | RWH | <b>Quad Data 1 Big Endian Access</b> |
| <p>Big endian access to QDATA1, which is equal to {DATA3, DATA2, DATA1, DATA0} and {DDATA3, DDATA2}. 16x32bits read/write accesses are required to fully read/write QDATA1.</p> |           |                 |     |                                      |

### 32.6.44 CRYPTO\_QDATA0BYTE - QDATA0 Register Byte Access (No Bit Access) (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |            |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|------------|---|---|---|---|---|---|---|
| 0x1C0         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0xXX       |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RWH        |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | QDATA0BYTE |   |   |   |   |   |   |   |

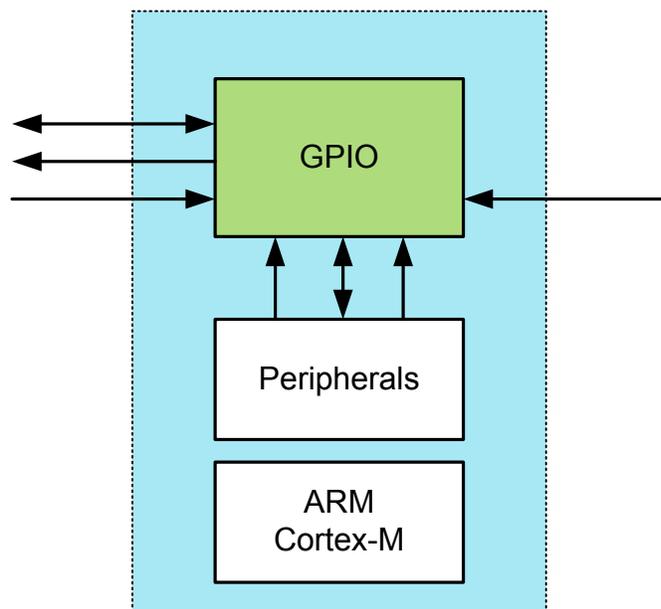
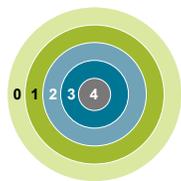
| Bit  | Name       | Reset  | Access | Description   |
|------|------------|--|--------|---|
| 31:8 | Reserved   | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 7:0  | QDATA0BYTE | 0xXX   | RWH    | <b>Qdata 0 Byte Access</b><br><br>Access to QDATA0. 64x8bits read/write accesses are required to fully read/write QDATA0. Accesses must be performed in multiples of 4, or data incoherency may occur |

### 32.6.45 CRYPTO\_QDATA1BYTE - QDATA1 Register Byte Access (No Bit Access) (Actionable Reads)

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |            |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|------------|---|---|---|---|---|---|---|
| 0x1C4         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0xXX       |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RWH        |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | QDATA1BYTE |   |   |   |   |   |   |   |

| Bit  | Name       | Reset  | Access | Description   |
|------|------------|--|--------|---|
| 31:8 | Reserved   | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 7:0  | QDATA1BYTE | 0xXX   | RWH    | <b>Qdata 1 Byte Access</b><br><br>Access to QDATA1. 64x8bits read/write accesses are required to fully read/write QDATA1. Accesses must be performed in multiples of 4, or data incoherency may occur |

## 33. GPIO - General Purpose Input/Output



### Quick Facts

#### What?

The General Purpose Input/Output (GPIO) is used for pin configuration, direct pin manipulation and sensing, as well as routing for peripheral pin connections.

#### Why?

Easy to use and highly configurable input/output pins are important to fit many communication protocols as well as minimizing software control overhead. Flexible routing of peripheral functions helps to ease PCB layout.

#### How?

Each pin on the device can be individually configured as either an input or an output with several different drive modes. Also, individual bit manipulation registers minimize control overhead. Peripheral connections to pins can be routed to several different locations, thus solving congestion issues that may arise with multiple functions on the same pin. Fully asynchronous interrupts can also be generated from any pin.

### 33.1 Introduction

In the EFR32xG13 Wireless Gecko devices the General Purpose Input/Output (GPIO) pins are organized into ports with up to 16 pins each. These GPIO pins can individually be configured as either an output or input. More advanced configurations like open-drain, open-source, and glitch filtering can be configured for each individual GPIO pin. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enable interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

**Note:** To use the GPIO, the GPIO clock must first be enabled in `CMU_HFBUSCLKEN0`. Setting this bit enables the HFBUSCLK for the GPIO.

## 33.2 Features

- Individual configuration for each pin
  - Tristate (reset state)
  - Push-pull
  - Open-drain
  - Pull-up resistor
  - Pull-down resistor
  - Drive strength
    - 1 mA
    - 10 mA
  - Slewrate
  - Over Voltage Tolerance
- EM4 IO pin retention
  - Output enable
  - Output value
  - Pull enable
  - Pull direction
  - Over Voltage Tolerance
- EM4 wake-up on selected GPIO pins
- Glitch suppression input filter
- Alternate functions (e.g. peripheral outputs and inputs)
  - Routed to several locations on the device
  - Pin connections can be enabled individually
  - Output data can be overridden by peripheral
  - Output enable can be overridden by peripheral
- Toggle register for output data
- Dedicated data input register (read-only)
- Interrupts
  - 2 Interrupt lines using either levels or edges
    - EM4 wake-up pins are selectable for level interrupts
    - All GPIO pins are selectable for edge interrupts
  - Separate enable, status, set and clear registers
  - Asynchronous sensing
  - Rising, falling or both edges
  - High or low level detection
  - Wake up from EM0 Active-EM3 Stop
- Peripheral Reflex System producer
  - All GPIO pins are selectable
- Configuration lock functionality to avoid accidental changes

### 33.3 Functional Description

An overview of the GPIO module is shown in [Figure 33.1 Pin Configuration on page 1122](#). The GPIO pins are grouped into 16-pin ports. Each individual GPIO pin is called P<sub>xn</sub> where x indicates the port (A, B, C ...) and n indicates the pin number (0,1,...,15). Fewer than 16 bits may be available on some ports, depending on the total number of I/O pins on the package. After a reset, both input and output are disabled for all pins on the device, except for the Serial Wire Debug pins.

To use a pin, the Mode Register (GPIO\_P<sub>x</sub>\_MODEL/GPIO\_P<sub>x</sub>\_MODEH) must be configured for the pin to make it an input or output. These registers can also do more advanced configuration, which is covered in [33.3.1 Pin Configuration](#). When the port is configured as an input or an output, the Data In Register (GPIO\_P<sub>x</sub>\_DIN) can be used to read the level of each pin in the port (bit n in the register is connected to pin n on the port). When configured as an output, the value of the Data Out Register (GPIO\_P<sub>x</sub>\_DOUT) will be driven to the pin.

The DOUT value can be changed in 4 different ways:

- Writing to the GPIO\_P<sub>x</sub>\_DOUT register
- Writing the BITSET address of the GPIO\_P<sub>x</sub>\_DOUT register sets the DOUT bits
- Writing the BITCLEAR address of the GPIO\_P<sub>x</sub>\_DOUT register clears the DOUT bits
- Writing the GPIO\_P<sub>x</sub>\_DOUTTGL register toggles the corresponding DOUT bits

Reading the GPIO\_P<sub>x</sub>\_DOUT register will return its contents. Reading the GPIO\_P<sub>x</sub>\_DOUTTGL register will return 0.

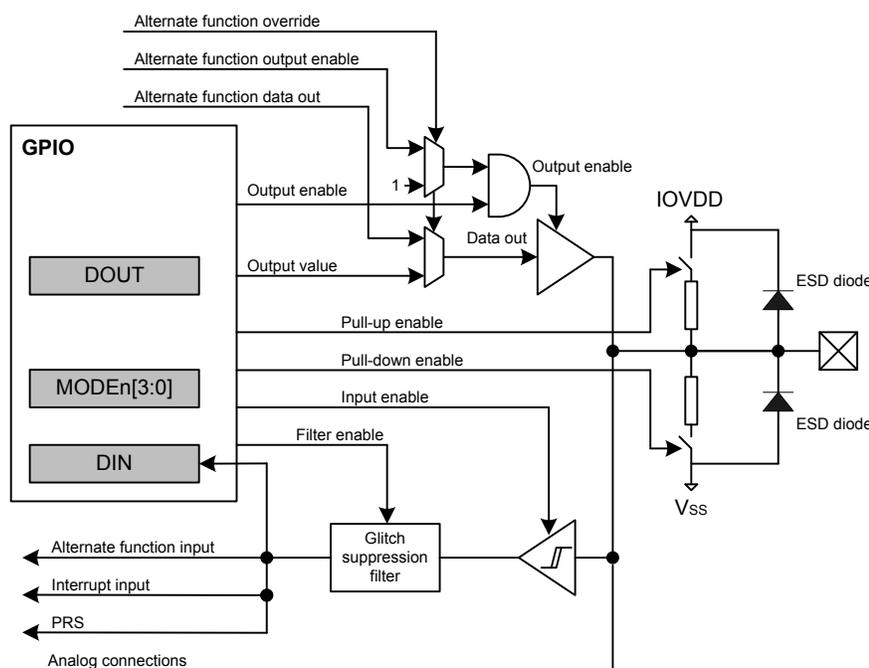


Figure 33.1. Pin Configuration

### 33.3.1 Pin Configuration

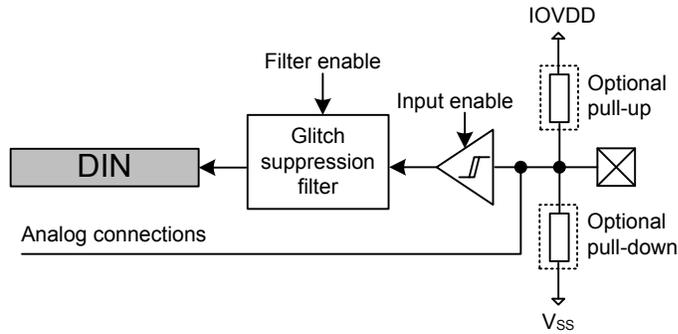
In addition to setting the pins as either outputs or inputs, the GPIO\_Px\_MODEL and GPIO\_Px\_MODEH registers can be used for more advanced configurations. GPIO\_Px\_MODEL contains 8 bit fields named MODEn (n=0,1,..7) which control pins 0-7, while GPIO\_Px\_MODEH contains 8 bit fields named MODEn (n=8,9,..15) which control pins 8-15. In some modes GPIO\_Px\_DOUT is also used for extra configurations like pull-up/down and glitch suppression filter enable. [Table 33.1 Pin Configuration on page 1123](#) shows the available configurations.

**Table 33.1. Pin Configuration**

| MODEn                   | Input                  | Output                 | DOUT | Pull-down | Pull-up | Alt Port Ctrl | Input Filter | Description   |
|-------------------------|------------------------|------------------------|------|-----------|---------|---------------|--------------|---|
| DISABLED                | Disabled               | Disabled               | 0    |           |         |               |              | Input disabled  |
|                         |                        |                        | 1    |           | On      |               |              | Input disabled with pull-up                                       |
| INPUT                   | Enabled if not DINDIS  |                        | 0    |           |         |               |              | Input enabled   |
|                         |                        |                        | 1    |           |         |               | On           | Input enabled with filter   |
| INPUTPULL               |                        | 0                      | On   |           |         |               |              | Input enabled with pull-down                                      |
|                         |                        | 1                      |      | On        |         |               |              | Input enabled with pull-up  |
| INPUTPULLFILTER         |                        | 0                      | On   |           |         |               | On           | Input enabled with pull-down and filter                           |
|                         |                        | 1                      |      | On        |         |               | On           | Input enabled with pull-up and filter                             |
| PUSHPULL                |                        | Push-pull              | x    |           |         |               |              | Push-pull   |
| PUSHPULLALT             |                        |                        | x    |           |         | On            |              | Push-pull with alternate port control values                      |
| WIREDOR                 |                        | Open Source (Wired-OR) | x    |           |         |               |              | Open-source   |
| WIREDORPULLDOWN         |                        |                        | x    | On        |         |               |              | Open-source with pull-down  |
| WIREDAND                | Open Drain (Wired-AND) | x                      |      |           |         |               |              | Open-drain  |
| WIREDANDFILTER          |                        | x                      |      |           |         |               | On           | Open-drain with filter  |
| WIREDANDPULLUP          |                        | x                      |      |           | On      |               |              | Open-drain with pull-up   |
| WIREDANDPULLUPFILTER    |                        | x                      |      |           | On      |               | On           | Open-drain with pull-up and filter                                |
| WIREDANDALT             |                        | x                      |      |           |         | On            |              | Open-drain with alternate port control values                     |
| WIREDANDALTFILTER       |                        | x                      |      |           |         | On            | On           | Open-drain with alternate port control values and filter          |
| WIREDANDALTPULLUP       |                        | x                      |      |           | On      | On            |              | Open-drain with alternate port control values and pull-up         |
| WIREDANDALTPULLUPFILTER |                        | x                      |      |           | On      | On            | On           | Open-drain with alternate port control values, pull-up and filter |

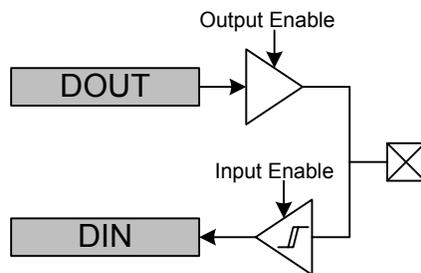
MODEn determines which mode the pin is in at a given time. Setting MODEn to DISABLED disables the pin, reducing power consumption to a minimum. When the output driver, input driver and Over Voltage Tolerance is disabled, the pin can be used as a connection for an analog module. An input is enabled by setting MODEn to any value other than DISABLED while DINDIS for the given port is cleared.

Set DINDIS to disable the input of a gpio port. The pull-up, pull-down and glitch filter function can optionally be applied to the input, see [Figure 33.2 Tristated Output With Optional Pull-up or Pull-down on page 1124](#).



**Figure 33.2. Tristated Output With Optional Pull-up or Pull-down**

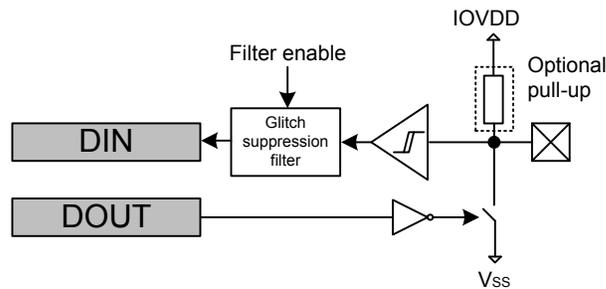
When MODEn is PUSH\_PULL or PUSH\_PULLALT, the pin operates in push-pull mode. In this mode, the pin can have alternate port control values and can be driven either high or low, dependent on the value of GPIO\_Px\_DOUT. The push-pull configuration is shown in [Figure 33.3 Push-Pull Configuration on page 1124](#).



**Figure 33.3. Push-Pull Configuration**

When MODEn is WIRE\_DOR or WIRE\_DOR\_PULLDOWN, the pin operates in open-source mode (with a pull-down resistor for WIRE\_DOR\_PULLDOWN). When driving a high value in open-source mode, the pull-down is disconnected to save power.

When the mode is prefixed with WIRE\_DAND, the pin operates in open-drain mode as shown in [Figure 33.4 Open-drain on page 1124](#). In open-drain mode, the pin can have an input filter, a pull-up, alternate port control values or any combination of these. When driving a low value in open-drain mode, the pull-up is disconnected to save power.



**Figure 33.4. Open-drain**

### 33.3.1.1 Over Voltage Tolerance

Over voltage capability is available for most pins. If available, it allows the pin to be used at the minimum of IOVDD + 2V and 5.5V (for 5V tolerant pads). The data sheet specifies which pins can be used as 5V tolerant pins. Default over voltage is enabled for each pin supporting that feature. Over voltage tolerance (OVT) can be disabled on a per pin basis. The over voltage tolerance feature applied to the selected pins is configured in the GPIO\_Px\_OVTDIS register. Disabling the over voltage tolerance for a pin will provide less distortion on that pin, which is useful when the pin is used as analog input.

**Note:** The VDAC (and OPAMPs) can drive outputs above IOVDD and therefore the involved pads typically require OVT to be enabled.

### 33.3.1.2 Alternate Port Control

The Alternate Port Control allows for additional flexibility of port level settings. A user may setup two different port configurations (normal and alternate modes) and select which is applied on a pin by pin bases. For example you may configure half of port A to use the low drive strength setting (normal mode) while the other half uses high drive strength (alternate mode).

Alternate port control is enabled when MODEN is set to any of the ALT enumerated modes (ie. PUSH/PULL/ALT). When MODEN is an alternate mode, the pin uses the alternate port control values specified in the DINDISALT, SLEWRATEALT, and DRIVESTRENGTHALT fields in GPIO\_Px\_CTRL. In all other modes, the port control values are used from the DINDIS, SLEWRATE, and DRIVESTRENGTH fields in GPIO\_Px\_CTRL.

### 33.3.1.3 Drive Strength

The drive strength can be applied to pins on a port-by-port basis. The drive strength applied to pins configured using normal MODEN settings can be controlled using the DRIVESTRENGTH field in GPIO\_Px\_CTRL. The drive strength applied to pins configured using alternate MODEN settings can be controlled using the DRIVESTRENGTHALT field.

### 33.3.1.4 Slewrate

The slewrate can be applied to pins on a port-by-port basis. The slewrate applied to pins configured using normal MODEN settings can be controlled using the SLEWRATE fields in GPIO\_Px\_CTRL. The slewrate applied to pins configured using the alternate MODEN settings can be controlled using the SLEWRATEALT field.

### 33.3.1.5 Input Disable

The pin inputs can be disabled on a port-by-port basis. The input of pins configured using the normal MODEN settings can be disabled by setting DINDIS in GPIO\_Px\_CTRL. The input of pins configured using the alternate MODEN settings can be disabled by setting DINDISALT.

### 33.3.1.6 Configuration Lock

GPIO\_Px\_MODEL, GPIO\_Px\_MODEH, GPIO\_Px\_CTRL, GPIO\_Px\_PINLOCKN, GPIO\_Px\_OVTDIS, GPIO\_EXTIPSELL, GPIO\_EXTIPSELH, GPIO\_EXTIPINSELL, GPIO\_EXTIPINSELH, GPIO\_INSENSE, GPIO\_ROUTEOPEN, and GPIO\_ROUTELOC0 can be locked by writing any value other than 0xA534 to GPIO\_LOCK. Writing the value 0xA534 to the GPIOx\_LOCK register unlocks the configuration registers.

In addition to configuration lock, GPIO\_Px\_MODEL, GPIO\_Px\_MODEH, GPIO\_Px\_DOUT, GPIO\_Px\_DOUTTGL, and GPIO\_Px\_OVTDIS can be locked individually for each pin by clearing the corresponding bit in GPIO\_Px\_PINLOCKN. When a bit in the GPIO\_Px\_PINLOCKN register is cleared, it will stay cleared until reset.

### 33.3.2 EM4 Wake-up

It is possible to trigger a wake-up from EM4 using any of the selectable EM4WU GPIO pins. The wake-up request can be triggered through the pins by enabling the corresponding bit in the GPIO\_EM4WUEN register. When EM4 wake-up is enabled for the pin, the input filter is enabled during EM4. This is done to avoid false wake-up caused by glitches. In addition, the polarity of the EM4 wake-up request can be selected using the GPIO\_EXTILEVEL register.

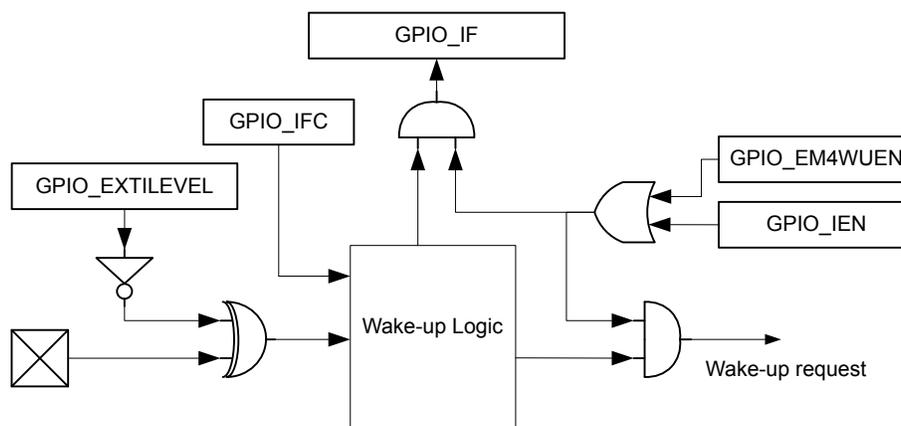


Figure 33.5. EM4 Wake-up Logic

The pins used for EM4 wake-up must be configured as inputs with glitch filters using the GPIO\_Px\_MODEL/GPIO\_Px\_MODEH register. If the input is disabled and the wakeup polarity is low, a false wakeup will occur when entering EM4. If the input is enabled, the glitch filtered is disabled, and the polarity is set low, a glitch will occur when going into EM4 that will cause an immediate wake-up. Before going down to EM4, it is important to clear the wake-up logic by setting the GPIO\_IFC bit, which clears the wake-up logic, including the GPIO\_IF register. It is possible to determine which pin caused the EM4WU by reading the GPIO\_IF register. The mapping between EM4WU pins and the bit indexes in the GPIO\_EM4WUEN, GPIO\_EXTILEVEL, GPIO\_IFC, GPIO\_IFS, GPIO\_IEN, and GPIO\_IF registers is as follows:

Table 33.2. EM4WU Register Bit Index to EM4WU Pin Mapping

| EM4WU Register Bit Indexes                                     | EM4WU Pin    |
|--|--------------|
| 16   | GPIO_EM4WU0  |
| 17   | GPIO_EM4WU1  |
| 18   | GPIO_EM4WU2  |
| 19   | GPIO_EM4WU3  |
| ...  | ...          |
| 31   | GPIO_EM4WU15 |
| <b>Note:</b> See the device data sheet for actual pin location |              |

### 33.3.3 EM4 Retention

By default, GPIO pins revert back to their reset state when EM4 is entered. The GPIO pins can be configured to retain the settings for output enable, output value, pull enable, pull direction and over voltage tolerance while in EM4.

EM4 GPIO retention is controlled with the EM4IORETMODE field in the EMU\_EM4CTRL register. Setting EM4IORETMODE to EM4EXIT will cause retention to persist while in EM4 and reset the GPIOs during wakeup. Setting EM4IORETMODE to SWUNLATCH will cause the retention to persist until the EM4UNLATCH bit is written by software. Note that when using SWUNLATCH, the GPIO register values are still reset on wakeup from EM4. In order to ensure that the GPIO state does not change, software must re-write the GPIO registers before setting EM4UNLATCH and ending EM4 GPIO retention. See the EMU chapter for additional documentation on its registers and the EM4UNLATCH bit.

### 33.3.4 Alternate Functions

Alternate functions are connections to pins from peripherals, i.e. Timers, USARTs, etc.. These peripherals contain route registers, where the pin connections are enabled. In addition, the route registers contain a location bit field that configures which pin an output of that peripheral will be connected to if enabled. After connecting a peripheral, the pin configuration stays as set in GPIO\_Px\_MODEL, GPIO\_Px\_MODEH and GPIO\_Px\_DOUT registers. For example, the pin configuration must be set to output enable in GPIO\_Px\_MODEL or GPIO\_Px\_MODEH for a peripheral to be able to use the pin as an output.

It is not recommended to select two or more peripherals as output on the same pin. The reader is referred to the pin map section of the device data sheet for more information on the possible locations of each alternate function.

#### 33.3.4.1 Analog Connections

When using the GPIO pin for analog functionality, it is recommended to disable the over voltage tolerance by setting the corresponding pin in the GPIO\_Px\_OVTDIS register and setting the MODEN in GPIO\_Px\_MODEL or GPIO\_Px\_MODEH equal to DISABLE to disable the input sense, output driver and pull resistors.

#### 33.3.4.2 Debug Connections

##### 33.3.4.2.1 Serial Wire Debug Connection

The SW Debug Port is routed as an alternate function and the SWDIO and SWCLK pin connections are enabled by default with internal pull up and pull down resistors, respectively. It is possible to disable these pin connections (and disable the pull resistors) by setting the SWDIOTMSPEN and SWCLKTCKPEN bits in GPIO\_ROUTEPEN to 0.

##### 33.3.4.2.2 JTAG Debug Connection

The JTAG Debug Port is routed as an alternate function and the TMS, TCK, TDO, and TDI pin connections are enabled by default with internal pull up, pull down, no pull, and pull up resistors, respectively. It is possible to disable these pin connections (and disable the pull resistors) by setting the SWDIOTMSPEN, SWCLKTCKPEN, TDOPEN, and TDIPEN bits in GPIO\_ROUTEPEN to 0.

##### 33.3.4.2.3 Disabling Debug Connections

When the debug pins are disabled, the device can no longer be accessed by a debugger. A reset will set the debug pins back to their enabled default state. The GPIO\_ROUTEPEN register can only be updated when the debugger is disconnected from the system. Any attempts to modify GPIO\_ROUTEPEN when the debugger is connected will not occur. If you do disable the debug pins, make sure you have at least a 3 second timeout at the start of your program code before you disable the debug pins. This way the debugger will have time to connect to the device after a reset and before the pins are disabled.

##### 33.3.4.2.4 ETM Trace Connections

There are five trace pins available on the device. One trace clock which can be enabled by setting the ETMTCLKPEN bitfield in GPIO\_ROUTEPEN. The four data pins can be enabled individually by setting ETMTD0PEN, ETMTD1PEN, ETMTD2PEN and ETMTD3PEN respectively in GPIO\_ROUTEPEN. It is possible to choose which pins the trace data will be exported to. The lowest trace bit will be routed to the first enabled trace pin. For example, if the ETM data port size is 2 bits and TD0 and TD3 are enabled, will make bit 0 be routed to TD0 while bit 1 will be routed to TD3.

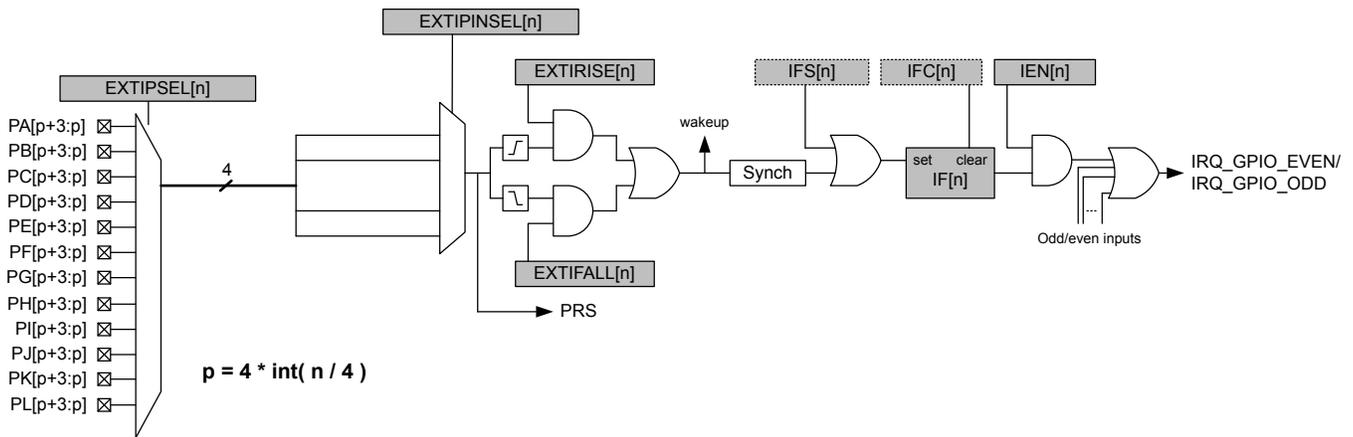
Both the TCLK and all the TD pins can also be routed to alternate locations by configuring the ETMLOC bitfield in GPIO\_ROUTELOC0.

### 33.3.5 Interrupt Generation

Interrupts may be triggered on edge events for any GPIO pin, or on pin input levels for GPIO capable of EM4 wake-up.

### 33.3.5.1 Edge Interrupt Generation

The GPIO can generate an interrupt from any edge of the input of any GPIO pin on the device. The edge interrupts have asynchronous sense capability, enabling wake-up from energy modes as low as EM3 Stop, see [Figure 33.6 Pin N Interrupt Generation on page 1128](#).



**Figure 33.6. Pin N Interrupt Generation**

External pin interrupts can be represented in the form of EXTI[index], where index is the external interrupt number. For example, the EXTI7 interrupt has an index of 7. All pins within a group of four (0-3,4-7,8-11,12-15) from all ports are grouped together to trigger one interrupt. The group of pins available to trigger an interrupt is determined by the interrupt index and calculated as  $\text{int}(\text{index}/4)$ . For example the first 4 interrupts (EXTI0 - EXTI3) are triggered by pins in the first group (Px[3:0]) and the second 4 interrupts (EXTI4-EXTI7) are triggered by pins in the second group (Px[7:4]).

The EXTIPSELn bits in GPIO\_EXTIPSELL or GPIO\_EXTIPSELH select which PORT in the group will trigger the interrupt. The EXTIPINSELn bits in GPIO\_EXTIPINSELL or GPIO\_EXTIPINSELH will determine which pin inside the selected group will trigger the interrupt.

For example if EXTIPSEL11 = PORTB and EXTPINSEL11 = 0 then PB8 will be used for EXTI11. EXTI11 uses the third group ( $11/4 = 2$ ) so the list of possible pins is Px[11:8]. The setting of EXTIPSEL11 further narrows the selection to PB[11:8]. Finally EXTPINSEL11 selects the first pin in that group which is PB8.

The GPIO\_EXTIRISE[n] and GPIO\_EXTIFALL[n] registers enable sensing of rising and falling edges. By setting the EXT[n] bit in GPIO\_IEN, a high interrupt flag n, will trigger one of two interrupt lines. The even interrupt line is triggered by any enabled even numbered interrupt flag index, while the odd interrupt line is triggered by odd flag indexes. The interrupt flags can be set and cleared by software when writing the GPIO\_IFS and GPIO\_IFC registers. Since the external interrupts are asynchronous, they are sensitive to noise. To increase noise tolerance, the MODEL and MODEH fields in the GPIO\_Px\_MODEL and GPIO\_Px\_MODEH registers, respectively, should be set to include glitch filtering for pins that have external interrupts enabled.

### 33.3.5.2 Level Interrupt Generation

GPIO can generate a level interrupt using the input of any GPIO EM4 wake-up pins on the device. The interrupts have asynchronous sense capability, enabling wake-up from energy modes as low as EM4.

In order to enable the level interrupt, set the EM4WU field in the GPIO\_IEN register and the EM4WUn field in the GPIO\_EXTILEVEL register. Upon a level interrupt occurring, the corresponding EM4WU index in the GPIO\_IF register will be set along with the odd or even interrupt line depending on the index inside of GPIO\_IF. For example, by setting the EM4WU8 in GPIO\_EXTILEVEL and EM4WU[8] in GPIO\_IEN, the interrupt flag EM4WU[8] in GPIO\_IF will be triggered by a high level on pin EM4WU8 and a interrupt request will be sent on IRQ\_GPIO\_EVEN.

The wake-up granularity of the level interrupts is based on the settings of the EM4WU field in the GPIO\_IEN register and the EM4WUEN field in the GPIO\_EM4WUEN register, see [Table 33.3 Level Interrupt Energy Mode Wakeup on page 1129](#)

**Table 33.3. Level Interrupt Energy Mode Wakeup**

| GPIO_IEN | GPIO_EM4WUEN | Energy Mode Wakeup    |
|----------|--------------|-----------------------|
| 0        | 0            | No Interrupt          |
| 0        | 1            | EM4H,EM4S             |
| 1        | 0            | EM1,EM2,EM3,EM4H,EM4S |
| 1        | 1            | EM1,EM2,EM3,EM4H,EM4S |

### 33.3.6 Output to PRS

All pins within a group of four(0-3,4-7,8-11,12-15) from all ports are grouped together to form one PRS producer which outputs to the PRS. The pin from which the output should be taken is selected in the same fashion as the edge interrupts.

PRS output is not affected by the interrupt edge detection logic or gated by the IEN bits. See [Figure 33.6 Pin N Interrupt Generation on page 1128](#) for an illustration of where the PRS output signal is generated.

### 33.3.7 Synchronization

To avoid metastability in synchronous logic connected to the pins, all inputs are synchronized with double flip-flops. The flip-flops for the input data run on the HFBUSCLK. Consequently, when a pin changes state, the change will have propagated to GPIO\_Px\_DIN after two 2 HFBUSCLK cycles. Synchronization (also running on the HFBUSCLK) is also added for interrupt input. To save power when the external interrupts or level interrupts are not used, the synchronization flip-flops for these can be turned off by clearing INT or EM4WU, respectively, in GPIO\_INSENSE register.

### 33.4 Register Map

The offset register address is relative to the registers base address.

| Offset | Name             | Type  | Description                                      |
|--------|------------------|-------|--|
| 0x000  | GPIO_PA_CTRL     | RW    | Port Control Register                            |
| 0x004  | GPIO_PA_MODEL    | RW    | Port Pin Mode Low Register                       |
| 0x008  | GPIO_PA_MODEH    | RW    | Port Pin Mode High Register                      |
| 0x00C  | GPIO_PA_DOUT     | RW    | Port Data Out Register                           |
| 0x018  | GPIO_PA_DOUTTGL  | W1    | Port Data Out Toggle Register                    |
| 0x01C  | GPIO_PA_DIN      | R     | Port Data in Register                            |
| 0x020  | GPIO_PA_PINLOCKN | RW    | Port Unlocked Pins Register                      |
| 0x028  | GPIO_PA_OVTDIS   | RW    | Over Voltage Disable for All Modes               |
| ...    | GPIO_Px_CTRL     | RW    | Port Control Register                            |
| ...    | GPIO_Px_MODEL    | RW    | Port Pin Mode Low Register                       |
| ...    | GPIO_Px_MODEH    | RW    | Port Pin Mode High Register                      |
| ...    | GPIO_Px_DOUT     | RW    | Port Data Out Register                           |
| ...    | GPIO_Px_DOUTTGL  | W1    | Port Data Out Toggle Register                    |
| ...    | GPIO_Px_DIN      | R     | Port Data in Register                            |
| ...    | GPIO_Px_PINLOCKN | RW    | Port Unlocked Pins Register                      |
| ...    | GPIO_Px_OVTDIS   | RW    | Over Voltage Disable for All Modes               |
| 0x210  | GPIO_PL_CTRL     | RW    | Port Control Register                            |
| 0x214  | GPIO_PL_MODEL    | RW    | Port Pin Mode Low Register                       |
| 0x218  | GPIO_PL_MODEH    | RW    | Port Pin Mode High Register                      |
| 0x21C  | GPIO_PL_DOUT     | RW    | Port Data Out Register                           |
| 0x228  | GPIO_PL_DOUTTGL  | W1    | Port Data Out Toggle Register                    |
| 0x22C  | GPIO_PL_DIN      | R     | Port Data in Register                            |
| 0x230  | GPIO_PL_PINLOCKN | RW    | Port Unlocked Pins Register                      |
| 0x238  | GPIO_PL_OVTDIS   | RW    | Over Voltage Disable for All Modes               |
| 0x400  | GPIO_EXTIPSELL   | RW    | External Interrupt Port Select Low Register      |
| 0x404  | GPIO_EXTIPSELH   | RW    | External Interrupt Port Select High Register     |
| 0x408  | GPIO_EXTIPINSELL | RW    | External Interrupt Pin Select Low Register       |
| 0x40C  | GPIO_EXTIPINSELH | RW    | External Interrupt Pin Select High Register      |
| 0x410  | GPIO_EXTIRISE    | RW    | External Interrupt Rising Edge Trigger Register  |
| 0x414  | GPIO_EXTIFALL    | RW    | External Interrupt Falling Edge Trigger Register |
| 0x418  | GPIO_EXTILEVEL   | RW    | External Interrupt Level Register                |
| 0x41C  | GPIO_IF          | R     | Interrupt Flag Register                          |
| 0x420  | GPIO_IFS         | W1    | Interrupt Flag Set Register                      |
| 0x424  | GPIO_IFC         | (R)W1 | Interrupt Flag Clear Register                    |
| 0x428  | GPIO_IEN         | RW    | Interrupt Enable Register                        |

| Offset | Name           | Type | Description                     |
|--------|----------------|------|---------------------------------|
| 0x42C  | GPIO_EM4WUEN   | RW   | EM4 Wake Up Enable Register     |
| 0x440  | GPIO_ROUTEPEN  | RW   | I/O Routing Pin Enable Register |
| 0x444  | GPIO_ROUTELOC0 | RW   | I/O Routing Location Register   |
| 0x448  | GPIO_ROUTELOC1 | RW   | I/O Routing Location Register 1 |
| 0x450  | GPIO_INSENSE   | RW   | Input Sense Register            |
| 0x454  | GPIO_LOCK      | RWH  | Configuration Lock Register     |

### 33.5 Register Description

#### 33.5.1 GPIO\_Px\_CTRL - Port Control Register

| Offset        | Bit Position |    |    |           |    |    |    |    |    |    |             |    |    |    |    |    |    |    |                  |    |    |    |   |   |   |        |   |   |   |   |    |   |          |  |  |  |               |
|---------------|--------------|----|----|-----------|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|------------------|----|----|----|---|---|---|--------|---|---|---|---|----|---|----------|--|--|--|---------------|
| 0x000         | 31           | 30 | 29 | 28        | 27 | 26 | 25 | 24 | 23 | 22 | 21          | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13               | 12 | 11 | 10 | 9 | 8 | 7 | 6      | 5 | 4 | 3 | 2 | 1  | 0 |          |  |  |  |               |
| <b>Reset</b>  |              |    |    | 0         |    |    |    |    |    |    | 0x5         |    |    |    |    |    |    |    | 0                |    |    |    |   |   |   | 0x5    |   |   |   |   | 0  |   |          |  |  |  |               |
| <b>Access</b> |              |    |    | RW        |    |    |    |    |    |    | RW          |    |    |    |    |    |    |    | RW               |    |    |    |   |   |   | RW     |   |   |   |   | RW |   |          |  |  |  |               |
| <b>Name</b>   |              |    |    | DINDISALT |    |    |    |    |    |    | SLEWRATEALT |    |    |    |    |    |    |    | DRIVESTRENGTHALT |    |    |    |   |   |   | DINDIS |   |   |   |   |    |   | SLEWRATE |  |  |  | DRIVESTRENGTH |

| Bit   | Name              | Reset  | Access              | Description   |
|-------|-------------------|--|---------------------|---|
| 31:29 | Reserved          | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |                     |   |
| 28    | DINDISALT         | 0  | RW                  | <b>Alternate Data in Disable</b><br>Data input disable for port pins using alternate modes.   |
| 27:23 | Reserved          | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |                     |   |
| 22:20 | SLEWRATEALT       | 0x5  | RW                  | <b>Alternate Slewrate Limit for Port</b><br>Slewrate limit for port pins using alternate modes. Higher values represent faster slewrates. |
| 19:17 | Reserved          | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |                     |   |
| 16    | DRIVESTRENGTH-ALT | 0  | RW                  | <b>Alternate Drive Strength for Port</b><br>Drive strength setting for port pins using alternate drive strength.                          |
|       | Value             | Mode   | Description         |   |
|       | 0                 | STRONG   | 10 mA drive current |   |
|       | 1                 | WEAK   | 1 mA drive current  |   |
| 15:13 | Reserved          | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |                     |   |
| 12    | DINDIS            | 0  | RW                  | <b>Data in Disable</b><br>Data input disable for port pins not using alternate modes.   |
| 11:7  | Reserved          | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |                     |   |
| 6:4   | SLEWRATE          | 0x5  | RW                  | <b>Slewrate Limit for Port</b><br>Slewrate limit for port pins not using alternate modes. Higher values represent faster slewrates.       |
| 3:1   | Reserved          | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |                     |   |

| Bit | Name          | Reset  | Access | Description   |
|-----|---------------|--------|--------|---|
| 0   | DRIVESTRENGTH | 0      | RW     | <b>Drive Strength for Port</b><br>Drive strength setting for port pins not using alternate modes. |
|     | Value         | Mode   |        | Description   |
|     | 0             | STRONG |        | 10 mA drive current   |
|     | 1             | WEAK   |        | 1 mA drive current  |

## 33.5.2 GPIO\_Px\_MODEL - Port Pin Mode Low Register

| Offset        | Bit Position |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |    |    |       |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|-------|----|----|-------|---|---|---|---|---|---|---|---|---|---|
| 0x004         | 31           | 30 | 29 | 28    | 27 | 26 | 25    | 24 | 23 | 22    | 21 | 20 | 19    | 18 | 17 | 16    | 15 | 14 | 13    | 12 | 11 | 10    | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0x0          |    |    | 0x0   |    |    | 0x0   |    |    | 0x0   |    |    | 0x0   |    |    | 0x0   |    |    | 0x0   |    |    | 0x0   |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> | RW           |    |    | RW    |    |    | RW    |    |    | RW    |    |    | RW    |    |    | RW    |    |    | RW    |    |    |       |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | MODE7        |    |    | MODE6 |    |    | MODE5 |    |    | MODE4 |    |    | MODE3 |    |    | MODE2 |    |    | MODE1 |    |    | MODE0 |   |   |   |   |   |   |   |   |   |   |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
|-----|------|-------|--------|-------------|

31:28 MODE7 0x0 RW **Pin 7 Mode**

Configure mode for pin 7.

| Value | Mode                     | Description  |
|-------|--------------------------|--|
| 0     | DISABLED                 | Input disabled. Pullup if DOUT is set.                           |
| 1     | INPUT                    | Input enabled. Filter if DOUT is set                             |
| 2     | INPUTPULL                | Input enabled. DOUT determines pull direction                    |
| 3     | INPUTPULLFILTER          | Input enabled with filter. DOUT determines pull direction        |
| 4     | PUSHPULL                 | Push-pull output   |
| 5     | PUSHPULLALT              | Push-pull using alternate control                                |
| 6     | WIREDOR                  | Wired-or output  |
| 7     | WIREDORPULLDOWN          | Wired-or output with pull-down                                   |
| 8     | WIREDAND                 | Open-drain output  |
| 9     | WIREDANDFILTER           | Open-drain output with filter                                    |
| 10    | WIREDANDPULLUP           | Open-drain output with pullup                                    |
| 11    | WIREDANDPULLUP-FILTER    | Open-drain output with filter and pullup                         |
| 12    | WIREDANDALT              | Open-drain output using alternate control                        |
| 13    | WIREDANDALTFILTER        | Open-drain output using alternate control with filter            |
| 14    | WIREDANDALTPULLUP        | Open-drain output using alternate control with pullup            |
| 15    | WIREDANDALTPULLUP-FILTER | Open-drain output using alternate control with filter and pullup |

27:24 MODE6 0x0 RW **Pin 6 Mode**

Configure mode for pin 6.

| Value | Mode            | Description   |
|-------|-----------------|---|
| 0     | DISABLED        | Input disabled. Pullup if DOUT is set.                    |
| 1     | INPUT           | Input enabled. Filter if DOUT is set                      |
| 2     | INPUTPULL       | Input enabled. DOUT determines pull direction             |
| 3     | INPUTPULLFILTER | Input enabled with filter. DOUT determines pull direction |

| Bit | Name | Reset                   | Access | Description  |
|-----|------|-------------------------|--------|--|
|     | 4    | PUSHPULL                |        | Push-pull output   |
|     | 5    | PUSHPULLALT             |        | Push-pull using alternate control                                |
|     | 6    | WIREDOR                 |        | Wired-or output  |
|     | 7    | WIREDORPULLDOWN         |        | Wired-or output with pull-down                                   |
|     | 8    | WIREDAND                |        | Open-drain output  |
|     | 9    | WIREDANDFILTER          |        | Open-drain output with filter                                    |
|     | 10   | WIREDANDPULLUP          |        | Open-drain output with pullup                                    |
|     | 11   | WIREDANDPULLUP-FILTER   |        | Open-drain output with filter and pullup                         |
|     | 12   | WIREDANDALT             |        | Open-drain output using alternate control                        |
|     | 13   | WIREDANDALTFILTER       |        | Open-drain output using alternate control with filter            |
|     | 14   | WIREDANDALTPULLUP       |        | Open-drain output using alternate control with pullup            |
|     | 15   | WIREDANDALTPULLUPFILTER |        | Open-drain output using alternate control with filter and pullup |

23:20 MODE5 0x0 RW **Pin 5 Mode**

Configure mode for pin 5.

| Value | Mode                    | Description  |
|-------|-------------------------|--|
| 0     | DISABLED                | Input disabled. Pullup if DOUT is set.                           |
| 1     | INPUT                   | Input enabled. Filter if DOUT is set                             |
| 2     | INPUTPULL               | Input enabled. DOUT determines pull direction                    |
| 3     | INPUTPULLFILTER         | Input enabled with filter. DOUT determines pull direction        |
| 4     | PUSHPULL                | Push-pull output   |
| 5     | PUSHPULLALT             | Push-pull using alternate control                                |
| 6     | WIREDOR                 | Wired-or output  |
| 7     | WIREDORPULLDOWN         | Wired-or output with pull-down                                   |
| 8     | WIREDAND                | Open-drain output  |
| 9     | WIREDANDFILTER          | Open-drain output with filter                                    |
| 10    | WIREDANDPULLUP          | Open-drain output with pullup                                    |
| 11    | WIREDANDPULLUP-FILTER   | Open-drain output with filter and pullup                         |
| 12    | WIREDANDALT             | Open-drain output using alternate control                        |
| 13    | WIREDANDALTFILTER       | Open-drain output using alternate control with filter            |
| 14    | WIREDANDALTPULLUP       | Open-drain output using alternate control with pullup            |
| 15    | WIREDANDALTPULLUPFILTER | Open-drain output using alternate control with filter and pullup |

| Bit   | Name  | Reset                    | Access | Description  |
|-------|-------|--------------------------|--------|--|
| 19:16 | MODE4 | 0x0                      | RW     | <b>Pin 4 Mode</b><br>Configure mode for pin 4.                   |
|       | Value | Mode                     |        | Description  |
|       | 0     | DISABLED                 |        | Input disabled. Pullup if DOUT is set.                           |
|       | 1     | INPUT                    |        | Input enabled. Filter if DOUT is set                             |
|       | 2     | INPUTPULL                |        | Input enabled. DOUT determines pull direction                    |
|       | 3     | INPUTPULLFILTER          |        | Input enabled with filter. DOUT determines pull direction        |
|       | 4     | PUSHPULL                 |        | Push-pull output   |
|       | 5     | PUSHPULLALT              |        | Push-pull using alternate control                                |
|       | 6     | WIREDOR                  |        | Wired-or output  |
|       | 7     | WIREDORPULLDOWN          |        | Wired-or output with pull-down                                   |
|       | 8     | WIREDAND                 |        | Open-drain output  |
|       | 9     | WIREDANDFILTER           |        | Open-drain output with filter                                    |
|       | 10    | WIREDANDPULLUP           |        | Open-drain output with pullup                                    |
|       | 11    | WIREDANDPULLUP-FILTER    |        | Open-drain output with filter and pullup                         |
|       | 12    | WIREDANDALT              |        | Open-drain output using alternate control                        |
|       | 13    | WIREDANDALTFILTER        |        | Open-drain output using alternate control with filter            |
|       | 14    | WIREDANDALTPULLUP        |        | Open-drain output using alternate control with pullup            |
|       | 15    | WIREDANDALTPULLUP-FILTER |        | Open-drain output using alternate control with filter and pullup |
| 15:12 | MODE3 | 0x0                      | RW     | <b>Pin 3 Mode</b><br>Configure mode for pin 3.                   |
|       | Value | Mode                     |        | Description  |
|       | 0     | DISABLED                 |        | Input disabled. Pullup if DOUT is set.                           |
|       | 1     | INPUT                    |        | Input enabled. Filter if DOUT is set                             |
|       | 2     | INPUTPULL                |        | Input enabled. DOUT determines pull direction                    |
|       | 3     | INPUTPULLFILTER          |        | Input enabled with filter. DOUT determines pull direction        |
|       | 4     | PUSHPULL                 |        | Push-pull output   |
|       | 5     | PUSHPULLALT              |        | Push-pull using alternate control                                |
|       | 6     | WIREDOR                  |        | Wired-or output  |
|       | 7     | WIREDORPULLDOWN          |        | Wired-or output with pull-down                                   |
|       | 8     | WIREDAND                 |        | Open-drain output  |
|       | 9     | WIREDANDFILTER           |        | Open-drain output with filter                                    |
|       | 10    | WIREDANDPULLUP           |        | Open-drain output with pullup                                    |
|       | 11    | WIREDANDPULLUP-FILTER    |        | Open-drain output with filter and pullup                         |

| Bit  | Name  | Reset                  | Access | Description  |
|------|-------|------------------------|--------|--|
|      | 12    | WIREDANDALT            |        | Open-drain output using alternate control                        |
|      | 13    | WIREDANDALTFILTER      |        | Open-drain output using alternate control with filter            |
|      | 14    | WIREDANDALTPULL-UP     |        | Open-drain output using alternate control with pullup            |
|      | 15    | WIREDANDALTPULL-FILTER |        | Open-drain output using alternate control with filter and pullup |
| 11:8 | MODE2 | 0x0                    | RW     | <b>Pin 2 Mode</b><br>Configure mode for pin 2.                   |
|      | Value | Mode                   |        | Description  |
|      | 0     | DISABLED               |        | Input disabled. Pullup if DOUT is set.                           |
|      | 1     | INPUT                  |        | Input enabled. Filter if DOUT is set                             |
|      | 2     | INPUTPULL              |        | Input enabled. DOUT determines pull direction                    |
|      | 3     | INPUTPULLFILTER        |        | Input enabled with filter. DOUT determines pull direction        |
|      | 4     | PUSHPULL               |        | Push-pull output   |
|      | 5     | PUSHPULLALT            |        | Push-pull using alternate control                                |
|      | 6     | WIREDOR                |        | Wired-or output  |
|      | 7     | WIREDORPULLDOWN        |        | Wired-or output with pull-down                                   |
|      | 8     | WIREDAND               |        | Open-drain output  |
|      | 9     | WIREDANDFILTER         |        | Open-drain output with filter                                    |
|      | 10    | WIREDANDPULLUP         |        | Open-drain output with pullup                                    |
|      | 11    | WIREDANDPULLUP-FILTER  |        | Open-drain output with filter and pullup                         |
|      | 12    | WIREDANDALT            |        | Open-drain output using alternate control                        |
|      | 13    | WIREDANDALTFILTER      |        | Open-drain output using alternate control with filter            |
|      | 14    | WIREDANDALTPULL-UP     |        | Open-drain output using alternate control with pullup            |
|      | 15    | WIREDANDALTPULL-FILTER |        | Open-drain output using alternate control with filter and pullup |
| 7:4  | MODE1 | 0x0                    | RW     | <b>Pin 1 Mode</b><br>Configure mode for pin 1.                   |
|      | Value | Mode                   |        | Description  |
|      | 0     | DISABLED               |        | Input disabled. Pullup if DOUT is set.                           |
|      | 1     | INPUT                  |        | Input enabled. Filter if DOUT is set                             |
|      | 2     | INPUTPULL              |        | Input enabled. DOUT determines pull direction                    |
|      | 3     | INPUTPULLFILTER        |        | Input enabled with filter. DOUT determines pull direction        |
|      | 4     | PUSHPULL               |        | Push-pull output   |
|      | 5     | PUSHPULLALT            |        | Push-pull using alternate control                                |
|      | 6     | WIREDOR                |        | Wired-or output  |

| Bit | Name  | Reset                    | Access | Description  |
|-----|-------|--------------------------|--------|--|
| 7   |       | WIREDORPULLDOWN          |        | Wired-or output with pull-down                                   |
| 8   |       | WIREDAND                 |        | Open-drain output  |
| 9   |       | WIREDANDFILTER           |        | Open-drain output with filter                                    |
| 10  |       | WIREDANDPULLUP           |        | Open-drain output with pullup                                    |
| 11  |       | WIREDANDPULLUP-FILTER    |        | Open-drain output with filter and pullup                         |
| 12  |       | WIREDANDALT              |        | Open-drain output using alternate control                        |
| 13  |       | WIREDANDALTFILTER        |        | Open-drain output using alternate control with filter            |
| 14  |       | WIREDANDALTPULLUP        |        | Open-drain output using alternate control with pullup            |
| 15  |       | WIREDANDALTPULLUP-FILTER |        | Open-drain output using alternate control with filter and pullup |
| 3:0 | MODE0 | 0x0                      | RW     | <b>Pin 0 Mode</b><br>Configure mode for pin 0.                   |
|     | Value | Mode                     |        | Description  |
|     | 0     | DISABLED                 |        | Input disabled. Pullup if DOUT is set.                           |
|     | 1     | INPUT                    |        | Input enabled. Filter if DOUT is set                             |
|     | 2     | INPUTPULL                |        | Input enabled. DOUT determines pull direction                    |
|     | 3     | INPUTPULLFILTER          |        | Input enabled with filter. DOUT determines pull direction        |
|     | 4     | PUSHPULL                 |        | Push-pull output   |
|     | 5     | PUSHPULLALT              |        | Push-pull using alternate control                                |
|     | 6     | WIREDOR                  |        | Wired-or output  |
|     | 7     | WIREDORPULLDOWN          |        | Wired-or output with pull-down                                   |
|     | 8     | WIREDAND                 |        | Open-drain output  |
|     | 9     | WIREDANDFILTER           |        | Open-drain output with filter                                    |
|     | 10    | WIREDANDPULLUP           |        | Open-drain output with pullup                                    |
|     | 11    | WIREDANDPULLUP-FILTER    |        | Open-drain output with filter and pullup                         |
|     | 12    | WIREDANDALT              |        | Open-drain output using alternate control                        |
|     | 13    | WIREDANDALTFILTER        |        | Open-drain output using alternate control with filter            |
|     | 14    | WIREDANDALTPULLUP        |        | Open-drain output using alternate control with pullup            |
|     | 15    | WIREDANDALTPULLUP-FILTER |        | Open-drain output using alternate control with filter and pullup |

### 33.5.3 GPIO\_Px\_MODEH - Port Pin Mode High Register

| Offset        | Bit Position |    |    |        |    |    |        |    |    |        |    |    |        |    |    |        |    |    |       |    |    |       |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|--------|----|----|--------|----|----|--------|----|----|--------|----|----|--------|----|----|-------|----|----|-------|---|---|---|---|---|---|---|---|---|---|
| 0x008         | 31           | 30 | 29 | 28     | 27 | 26 | 25     | 24 | 23 | 22     | 21 | 20 | 19     | 18 | 17 | 16     | 15 | 14 | 13    | 12 | 11 | 10    | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0x0          |    |    | 0x0    |    |    | 0x0    |    |    | 0x0    |    |    | 0x0    |    |    | 0x0    |    |    | 0x0   |    |    | 0x0   |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> | RW           |    |    | RW     |    |    | RW     |    |    | RW     |    |    | RW     |    |    | RW     |    |    | RW    |    |    |       |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | MODE15       |    |    | MODE14 |    |    | MODE13 |    |    | MODE12 |    |    | MODE11 |    |    | MODE10 |    |    | MODE9 |    |    | MODE8 |   |   |   |   |   |   |   |   |   |   |

| Bit | Name | Reset | Access | Description |
|-----|------|-------|--------|-------------|
|-----|------|-------|--------|-------------|

31:28 MODE15 0x0 RW **Pin 15 Mode**

Configure mode for pin 15.

| Value | Mode                     | Description  |
|-------|--------------------------|--|
| 0     | DISABLED                 | Input disabled. Pullup if DOUT is set.                           |
| 1     | INPUT                    | Input enabled. Filter if DOUT is set                             |
| 2     | INPUTPULL                | Input enabled. DOUT determines pull direction                    |
| 3     | INPUTPULLFILTER          | Input enabled with filter. DOUT determines pull direction        |
| 4     | PUSHPULL                 | Push-pull output   |
| 5     | PUSHPULLALT              | Push-pull using alternate control                                |
| 6     | WIREDOR                  | Wired-or output  |
| 7     | WIREDORPULLDOWN          | Wired-or output with pull-down                                   |
| 8     | WIREDAND                 | Open-drain output  |
| 9     | WIREDANDFILTER           | Open-drain output with filter                                    |
| 10    | WIREDANDPULLUP           | Open-drain output with pullup                                    |
| 11    | WIREDANDPULLUP-FILTER    | Open-drain output with filter and pullup                         |
| 12    | WIREDANDALT              | Open-drain output using alternate control                        |
| 13    | WIREDANDALTFILTER        | Open-drain output using alternate control with filter            |
| 14    | WIREDANDALTPULL-UP       | Open-drain output using alternate control with pullup            |
| 15    | WIREDANDALTPUL-LUPFILTER | Open-drain output using alternate control with filter and pullup |

27:24 MODE14 0x0 RW **Pin 14 Mode**

Configure mode for pin 14.

| Value | Mode            | Description   |
|-------|-----------------|---|
| 0     | DISABLED        | Input disabled. Pullup if DOUT is set.                    |
| 1     | INPUT           | Input enabled. Filter if DOUT is set                      |
| 2     | INPUTPULL       | Input enabled. DOUT determines pull direction             |
| 3     | INPUTPULLFILTER | Input enabled with filter. DOUT determines pull direction |

| Bit | Name | Reset                   | Access | Description  |
|-----|------|-------------------------|--------|--|
|     | 4    | PUSHPULL                |        | Push-pull output   |
|     | 5    | PUSHPULLALT             |        | Push-pull using alternate control                                |
|     | 6    | WIREDOR                 |        | Wired-or output  |
|     | 7    | WIREDORPULLDOWN         |        | Wired-or output with pull-down                                   |
|     | 8    | WIREDAND                |        | Open-drain output  |
|     | 9    | WIREDANDFILTER          |        | Open-drain output with filter                                    |
|     | 10   | WIREDANDPULLUP          |        | Open-drain output with pullup                                    |
|     | 11   | WIREDANDPULLUP-FILTER   |        | Open-drain output with filter and pullup                         |
|     | 12   | WIREDANDALT             |        | Open-drain output using alternate control                        |
|     | 13   | WIREDANDALTFILTER       |        | Open-drain output using alternate control with filter            |
|     | 14   | WIREDANDALTPULLUP       |        | Open-drain output using alternate control with pullup            |
|     | 15   | WIREDANDALTPULLUPFILTER |        | Open-drain output using alternate control with filter and pullup |

23:20 MODE13 0x0 RW **Pin 13 Mode**

Configure mode for pin 13.

| Value | Mode                    | Description  |
|-------|-------------------------|--|
| 0     | DISABLED                | Input disabled. Pullup if DOUT is set.                           |
| 1     | INPUT                   | Input enabled. Filter if DOUT is set                             |
| 2     | INPUTPULL               | Input enabled. DOUT determines pull direction                    |
| 3     | INPUTPULLFILTER         | Input enabled with filter. DOUT determines pull direction        |
| 4     | PUSHPULL                | Push-pull output   |
| 5     | PUSHPULLALT             | Push-pull using alternate control                                |
| 6     | WIREDOR                 | Wired-or output  |
| 7     | WIREDORPULLDOWN         | Wired-or output with pull-down                                   |
| 8     | WIREDAND                | Open-drain output  |
| 9     | WIREDANDFILTER          | Open-drain output with filter                                    |
| 10    | WIREDANDPULLUP          | Open-drain output with pullup                                    |
| 11    | WIREDANDPULLUP-FILTER   | Open-drain output with filter and pullup                         |
| 12    | WIREDANDALT             | Open-drain output using alternate control                        |
| 13    | WIREDANDALTFILTER       | Open-drain output using alternate control with filter            |
| 14    | WIREDANDALTPULLUP       | Open-drain output using alternate control with pullup            |
| 15    | WIREDANDALTPULLUPFILTER | Open-drain output using alternate control with filter and pullup |

| Bit   | Name   | Reset                    | Access | Description  |
|-------|--------|--------------------------|--------|--|
| 19:16 | MODE12 | 0x0                      | RW     | <b>Pin 12 Mode</b><br>Configure mode for pin 12.                 |
|       | Value  | Mode                     |        | Description  |
|       | 0      | DISABLED                 |        | Input disabled. Pullup if DOUT is set.                           |
|       | 1      | INPUT                    |        | Input enabled. Filter if DOUT is set                             |
|       | 2      | INPUTPULL                |        | Input enabled. DOUT determines pull direction                    |
|       | 3      | INPUTPULLFILTER          |        | Input enabled with filter. DOUT determines pull direction        |
|       | 4      | PUSHPULL                 |        | Push-pull output   |
|       | 5      | PUSHPULLALT              |        | Push-pull using alternate control                                |
|       | 6      | WIREDOR                  |        | Wired-or output  |
|       | 7      | WIREDORPULLDOWN          |        | Wired-or output with pull-down                                   |
|       | 8      | WIREDAND                 |        | Open-drain output  |
|       | 9      | WIREDANDFILTER           |        | Open-drain output with filter                                    |
|       | 10     | WIREDANDPULLUP           |        | Open-drain output with pullup                                    |
|       | 11     | WIREDANDPULLUP-FILTER    |        | Open-drain output with filter and pullup                         |
|       | 12     | WIREDANDALT              |        | Open-drain output using alternate control                        |
|       | 13     | WIREDANDALTFILTER        |        | Open-drain output using alternate control with filter            |
|       | 14     | WIREDANDALTPULLUP        |        | Open-drain output using alternate control with pullup            |
|       | 15     | WIREDANDALTPULLUP-FILTER |        | Open-drain output using alternate control with filter and pullup |
| 15:12 | MODE11 | 0x0                      | RW     | <b>Pin 11 Mode</b><br>Configure mode for pin 11.                 |
|       | Value  | Mode                     |        | Description  |
|       | 0      | DISABLED                 |        | Input disabled. Pullup if DOUT is set.                           |
|       | 1      | INPUT                    |        | Input enabled. Filter if DOUT is set                             |
|       | 2      | INPUTPULL                |        | Input enabled. DOUT determines pull direction                    |
|       | 3      | INPUTPULLFILTER          |        | Input enabled with filter. DOUT determines pull direction        |
|       | 4      | PUSHPULL                 |        | Push-pull output   |
|       | 5      | PUSHPULLALT              |        | Push-pull using alternate control                                |
|       | 6      | WIREDOR                  |        | Wired-or output  |
|       | 7      | WIREDORPULLDOWN          |        | Wired-or output with pull-down                                   |
|       | 8      | WIREDAND                 |        | Open-drain output  |
|       | 9      | WIREDANDFILTER           |        | Open-drain output with filter                                    |
|       | 10     | WIREDANDPULLUP           |        | Open-drain output with pullup                                    |
|       | 11     | WIREDANDPULLUP-FILTER    |        | Open-drain output with filter and pullup                         |

| Bit | Name | Reset                  | Access | Description  |
|-----|------|------------------------|--------|--|
|     | 12   | WIREDANDALT            |        | Open-drain output using alternate control                        |
|     | 13   | WIREDANDALTFILTER      |        | Open-drain output using alternate control with filter            |
|     | 14   | WIREDANDALTPULL-UP     |        | Open-drain output using alternate control with pullup            |
|     | 15   | WIREDANDALTPULL-FILTER |        | Open-drain output using alternate control with filter and pullup |

**11:8 MODE10 0x0 RW Pin 10 Mode**

Configure mode for pin 10.

| Value | Mode                   | Description  |
|-------|------------------------|--|
| 0     | DISABLED               | Input disabled. Pullup if DOUT is set.                           |
| 1     | INPUT                  | Input enabled. Filter if DOUT is set                             |
| 2     | INPUTPULL              | Input enabled. DOUT determines pull direction                    |
| 3     | INPUTPULLFILTER        | Input enabled with filter. DOUT determines pull direction        |
| 4     | PUSHPULL               | Push-pull output   |
| 5     | PUSHPULLALT            | Push-pull using alternate control                                |
| 6     | WIREDOR                | Wired-or output  |
| 7     | WIREDORPULLDOWN        | Wired-or output with pull-down                                   |
| 8     | WIREDAND               | Open-drain output  |
| 9     | WIREDANDFILTER         | Open-drain output with filter                                    |
| 10    | WIREDANDPULLUP         | Open-drain output with pullup                                    |
| 11    | WIREDANDPULLUP-FILTER  | Open-drain output with filter and pullup                         |
| 12    | WIREDANDALT            | Open-drain output using alternate control                        |
| 13    | WIREDANDALTFILTER      | Open-drain output using alternate control with filter            |
| 14    | WIREDANDALTPULL-UP     | Open-drain output using alternate control with pullup            |
| 15    | WIREDANDALTPULL-FILTER | Open-drain output using alternate control with filter and pullup |

**7:4 MODE9 0x0 RW Pin 9 Mode**

Configure mode for pin 9.

| Value | Mode            | Description   |
|-------|-----------------|---|
| 0     | DISABLED        | Input disabled. Pullup if DOUT is set.                    |
| 1     | INPUT           | Input enabled. Filter if DOUT is set                      |
| 2     | INPUTPULL       | Input enabled. DOUT determines pull direction             |
| 3     | INPUTPULLFILTER | Input enabled with filter. DOUT determines pull direction |
| 4     | PUSHPULL        | Push-pull output  |
| 5     | PUSHPULLALT     | Push-pull using alternate control                         |
| 6     | WIREDOR         | Wired-or output   |

| Bit | Name  | Reset                    | Access | Description  |
|-----|-------|--------------------------|--------|--|
| 7   |       | WIREDORPULLDOWN          |        | Wired-or output with pull-down                                   |
| 8   |       | WIREDAND                 |        | Open-drain output  |
| 9   |       | WIREDANDFILTER           |        | Open-drain output with filter                                    |
| 10  |       | WIREDANDPULLUP           |        | Open-drain output with pullup                                    |
| 11  |       | WIREDANDPULLUP-FILTER    |        | Open-drain output with filter and pullup                         |
| 12  |       | WIREDANDALT              |        | Open-drain output using alternate control                        |
| 13  |       | WIREDANDALTFILTER        |        | Open-drain output using alternate control with filter            |
| 14  |       | WIREDANDALTPULLUP        |        | Open-drain output using alternate control with pullup            |
| 15  |       | WIREDANDALTPULLUP-FILTER |        | Open-drain output using alternate control with filter and pullup |
| 3:0 | MODE8 | 0x0                      | RW     | <b>Pin 8 Mode</b><br>Configure mode for pin 8.                   |
|     | Value | Mode                     |        | Description  |
|     | 0     | DISABLED                 |        | Input disabled. Pullup if DOUT is set.                           |
|     | 1     | INPUT                    |        | Input enabled. Filter if DOUT is set                             |
|     | 2     | INPUTPULL                |        | Input enabled. DOUT determines pull direction                    |
|     | 3     | INPUTPULLFILTER          |        | Input enabled with filter. DOUT determines pull direction        |
|     | 4     | PUSHPULL                 |        | Push-pull output   |
|     | 5     | PUSHPULLALT              |        | Push-pull using alternate control                                |
|     | 6     | WIREDOR                  |        | Wired-or output  |
|     | 7     | WIREDORPULLDOWN          |        | Wired-or output with pull-down                                   |
|     | 8     | WIREDAND                 |        | Open-drain output  |
|     | 9     | WIREDANDFILTER           |        | Open-drain output with filter                                    |
|     | 10    | WIREDANDPULLUP           |        | Open-drain output with pullup                                    |
|     | 11    | WIREDANDPULLUP-FILTER    |        | Open-drain output with filter and pullup                         |
|     | 12    | WIREDANDALT              |        | Open-drain output using alternate control                        |
|     | 13    | WIREDANDALTFILTER        |        | Open-drain output using alternate control with filter            |
|     | 14    | WIREDANDALTPULLUP        |        | Open-drain output using alternate control with pullup            |
|     | 15    | WIREDANDALTPULLUP-FILTER |        | Open-drain output using alternate control with filter and pullup |

## 33.5.4 GPIO\_Px\_DOUT - Port Data Out Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x00C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DOUT   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description                            |
|-------|----------|--|--------|--|
| 31:16 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 15:0  | DOUT     | 0x0000   | RW     | <b>Data Out</b><br>Data output on pin. |

## 33.5.5 GPIO\_Px\_DOUTTGL - Port Data Out Toggle Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x018         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W1      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DOUTTGL |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description  |
|-------|----------|--|--------|--|
| 31:16 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 15:0  | DOUTTGL  | 0x0000   | W1     | <b>Data Out Toggle</b><br>Write bits to 1 to toggle corresponding bits in GPIO_Px_DOUT. Bits written to 0 will have no effect. |

## 33.5.6 GPIO\_Px\_DIN - Port Data in Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x01C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DIN    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description                        |
|-------|----------|--|--------|------------------------------------|
| 31:16 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |                                    |
| 15:0  | DIN      | 0x0000   | R      | <b>Data in</b><br>Port data input. |

## 33.5.7 GPIO\_Px\_PINLOCKN - Port Unlocked Pins Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x020         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0xFFFF   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PINLOCKN |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description  |
|-------|----------|--|--------|--|
| 31:16 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 15:0  | PINLOCKN | 0xFFFF   | RW     | <b>Unlocked Pins</b><br>Shows unlocked pins in the port. To lock pin n, clear bit n. The pin is then locked until reset. |

33.5.8 GPIO\_Px\_OVTDIS - Over Voltage Disable for All Modes

| Offset | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|--------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x028  | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reset  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Access |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Name   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | OVTDIS |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset   | Access | Description  |
|-------|----------|---|--------|--|
| 31:16 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 15:0  | OVTDIS   | 0x0000  | RW     | <b>Disable Over Voltage Capability</b><br>Disabling the Over Voltage capability will provide less distortion on analog inputs. |

## 33.5.9 GPIO\_EXTIPSELL - External Interrupt Port Select Low Register

| Offset        | Bit Position |    |    |           |    |    |           |    |    |           |    |    |           |    |    |           |    |    |           |    |    |           |   |   |     |   |   |   |   |   |   |   |
|---------------|--------------|----|----|-----------|----|----|-----------|----|----|-----------|----|----|-----------|----|----|-----------|----|----|-----------|----|----|-----------|---|---|-----|---|---|---|---|---|---|---|
| 0x400         | 31           | 30 | 29 | 28        | 27 | 26 | 25        | 24 | 23 | 22        | 21 | 20 | 19        | 18 | 17 | 16        | 15 | 14 | 13        | 12 | 11 | 10        | 9 | 8 | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0x0          |    |    | 0x0       |    |    | 0x0       |    |    | 0x0       |    |    | 0x0       |    |    | 0x0       |    |    | 0x0       |    |    | 0x0       |   |   | 0x0 |   |   |   |   |   |   |   |
| <b>Access</b> | RW           |    |    | RW        |    |    | RW        |    |    | RW        |    |    | RW        |    |    | RW        |    |    | RW        |    |    | RW        |   |   |     |   |   |   |   |   |   |   |
| <b>Name</b>   | EXTIPSEL7    |    |    | EXTIPSEL6 |    |    | EXTIPSEL5 |    |    | EXTIPSEL4 |    |    | EXTIPSEL3 |    |    | EXTIPSEL2 |    |    | EXTIPSEL1 |    |    | EXTIPSEL0 |   |   |     |   |   |   |   |   |   |   |

| Bit   | Name      | Reset | Access | Description  |
|-------|-----------|-------|--------|--|
| 31:28 | EXTIPSEL7 | 0x0   | RW     | <b>External Interrupt 7 Port Select</b><br>Select input port for external interrupt 7. |
|       | Value     | Mode  |        | Description  |
|       | 0         | PORTA |        | Port A group selected for external interrupt 7   |
|       | 1         | PORTB |        | Port B group selected for external interrupt 7   |
|       | 2         | PORTC |        | Port C group selected for external interrupt 7   |
|       | 3         | PORTD |        | Port D group selected for external interrupt 7   |
|       | 5         | PORTF |        | Port F group selected for external interrupt 7   |
| 27:24 | EXTIPSEL6 | 0x0   | RW     | <b>External Interrupt 6 Port Select</b><br>Select input port for external interrupt 6. |
|       | Value     | Mode  |        | Description  |
|       | 0         | PORTA |        | Port A group selected for external interrupt 6   |
|       | 1         | PORTB |        | Port B group selected for external interrupt 6   |
|       | 2         | PORTC |        | Port C group selected for external interrupt 6   |
|       | 3         | PORTD |        | Port D group selected for external interrupt 6   |
|       | 5         | PORTF |        | Port F group selected for external interrupt 6   |
| 23:20 | EXTIPSEL5 | 0x0   | RW     | <b>External Interrupt 5 Port Select</b><br>Select input port for external interrupt 5. |
|       | Value     | Mode  |        | Description  |
|       | 0         | PORTA |        | Port A group selected for external interrupt 5   |
|       | 1         | PORTB |        | Port B group selected for external interrupt 5   |
|       | 2         | PORTC |        | Port C group selected for external interrupt 5   |
|       | 3         | PORTD |        | Port D group selected for external interrupt 5   |
|       | 5         | PORTF |        | Port F group selected for external interrupt 5   |
| 19:16 | EXTIPSEL4 | 0x0   | RW     | <b>External Interrupt 4 Port Select</b><br>Select input port for external interrupt 4. |

| Bit   | Name      | Reset | Access | Description  |
|-------|-----------|-------|--------|--|
|       | Value     | Mode  |        | Description  |
|       | 0         | PORTA |        | Port A group selected for external interrupt 4   |
|       | 1         | PORTB |        | Port B group selected for external interrupt 4   |
|       | 2         | PORTC |        | Port C group selected for external interrupt 4   |
|       | 3         | PORTD |        | Port D group selected for external interrupt 4   |
|       | 5         | PORTF |        | Port F group selected for external interrupt 4   |
| 15:12 | EXTIPSEL3 | 0x0   | RW     | <b>External Interrupt 3 Port Select</b><br>Select input port for external interrupt 3. |
|       | Value     | Mode  |        | Description  |
|       | 0         | PORTA |        | Port A group selected for external interrupt 3   |
|       | 1         | PORTB |        | Port B group selected for external interrupt 3   |
|       | 2         | PORTC |        | Port C group selected for external interrupt 3   |
|       | 3         | PORTD |        | Port D group selected for external interrupt 3   |
|       | 5         | PORTF |        | Port F group selected for external interrupt 3   |
| 11:8  | EXTIPSEL2 | 0x0   | RW     | <b>External Interrupt 2 Port Select</b><br>Select input port for external interrupt 2. |
|       | Value     | Mode  |        | Description  |
|       | 0         | PORTA |        | Port A group selected for external interrupt 2   |
|       | 1         | PORTB |        | Port B group selected for external interrupt 2   |
|       | 2         | PORTC |        | Port C group selected for external interrupt 2   |
|       | 3         | PORTD |        | Port D group selected for external interrupt 2   |
|       | 5         | PORTF |        | Port F group selected for external interrupt 2   |
| 7:4   | EXTIPSEL1 | 0x0   | RW     | <b>External Interrupt 1 Port Select</b><br>Select input port for external interrupt 1. |
|       | Value     | Mode  |        | Description  |
|       | 0         | PORTA |        | Port A group selected for external interrupt 1   |
|       | 1         | PORTB |        | Port B group selected for external interrupt 1   |
|       | 2         | PORTC |        | Port C group selected for external interrupt 1   |
|       | 3         | PORTD |        | Port D group selected for external interrupt 1   |
|       | 5         | PORTF |        | Port F group selected for external interrupt 1   |
| 3:0   | EXTIPSEL0 | 0x0   | RW     | <b>External Interrupt 0 Port Select</b><br>Select input port for external interrupt 0. |
|       | Value     | Mode  |        | Description  |
|       | 0         | PORTA |        | Port A group selected for external interrupt 0   |
|       | 1         | PORTB |        | Port B group selected for external interrupt 0   |

| Bit | Name | Reset | Access | Description                                    |
|-----|------|-------|--------|--|
| 2   |      | PORTC |        | Port C group selected for external interrupt 0 |
| 3   |      | PORTD |        | Port D group selected for external interrupt 0 |
| 5   |      | PORTF |        | Port F group selected for external interrupt 0 |

### 33.5.10 GPIO\_EXTIPSELH - External Interrupt Port Select High Register

| Offset        | Bit Position |    |    |    |            |    |    |    |            |    |    |    |            |    |    |    |            |    |    |    |            |    |   |   |           |   |   |   |           |   |   |   |
|---------------|--------------|----|----|----|------------|----|----|----|------------|----|----|----|------------|----|----|----|------------|----|----|----|------------|----|---|---|-----------|---|---|---|-----------|---|---|---|
| 0x404         | 31           | 30 | 29 | 28 | 27         | 26 | 25 | 24 | 23         | 22 | 21 | 20 | 19         | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11         | 10 | 9 | 8 | 7         | 6 | 5 | 4 | 3         | 2 | 1 | 0 |
| <b>Reset</b>  | 0x0          |    |    |    | 0x0        |    |    |    | 0x0        |    |    |    | 0x0        |    |    |    | 0x0        |    |    |    | 0x0        |    |   |   | 0x0       |   |   |   |           |   |   |   |
| <b>Access</b> | RW           |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |    |    | RW         |    |   |   | RW        |   |   |   |           |   |   |   |
| <b>Name</b>   | EXTIPSEL15   |    |    |    | EXTIPSEL14 |    |    |    | EXTIPSEL13 |    |    |    | EXTIPSEL12 |    |    |    | EXTIPSEL11 |    |    |    | EXTIPSEL10 |    |   |   | EXTIPSEL9 |   |   |   | EXTIPSEL8 |   |   |   |

| Bit   | Name       | Reset | Access | Description  |
|-------|------------|-------|--------|--|
| 31:28 | EXTIPSEL15 | 0x0   | RW     | <b>External Interrupt 15 Port Select</b><br>Select input port for external interrupt 15. |
|       | Value      | Mode  |        | Description  |
|       | 0          | PORTA |        | Port A group selected for external interrupt 15  |
|       | 1          | PORTB |        | Port B group selected for external interrupt 15  |
|       | 2          | PORTC |        | Port C group selected for external interrupt 15  |
|       | 3          | PORTD |        | Port D group selected for external interrupt 15  |
|       | 5          | PORTF |        | Port F group selected for external interrupt 15  |
| 27:24 | EXTIPSEL14 | 0x0   | RW     | <b>External Interrupt 14 Port Select</b><br>Select input port for external interrupt 14. |
|       | Value      | Mode  |        | Description  |
|       | 0          | PORTA |        | Port A group selected for external interrupt 14  |
|       | 1          | PORTB |        | Port B group selected for external interrupt 14  |
|       | 2          | PORTC |        | Port C group selected for external interrupt 14  |
|       | 3          | PORTD |        | Port D group selected for external interrupt 14  |
|       | 5          | PORTF |        | Port F group selected for external interrupt 14  |
| 23:20 | EXTIPSEL13 | 0x0   | RW     | <b>External Interrupt 13 Port Select</b><br>Select input port for external interrupt 13. |
|       | Value      | Mode  |        | Description  |
|       | 0          | PORTA |        | Port A group selected for external interrupt 13  |
|       | 1          | PORTB |        | Port B group selected for external interrupt 13  |
|       | 2          | PORTC |        | Port C group selected for external interrupt 13  |
|       | 3          | PORTD |        | Port D group selected for external interrupt 13  |
|       | 5          | PORTF |        | Port F group selected for external interrupt 13  |
| 19:16 | EXTIPSEL12 | 0x0   | RW     | <b>External Interrupt 12 Port Select</b><br>Select input port for external interrupt 12. |

| Bit   | Name       | Reset | Access | Description  |
|-------|------------|-------|--------|--|
|       | Value      | Mode  |        | Description  |
|       | 0          | PORTA |        | Port A group selected for external interrupt 12  |
|       | 1          | PORTB |        | Port B group selected for external interrupt 12  |
|       | 2          | PORTC |        | Port C group selected for external interrupt 12  |
|       | 3          | PORTD |        | Port D group selected for external interrupt 12  |
|       | 5          | PORTF |        | Port F group selected for external interrupt 12  |
| 15:12 | EXTIPSEL11 | 0x0   | RW     | <b>External Interrupt 11 Port Select</b><br>Select input port for external interrupt 11. |
|       | Value      | Mode  |        | Description  |
|       | 0          | PORTA |        | Port A group selected for external interrupt 11  |
|       | 1          | PORTB |        | Port B group selected for external interrupt 11  |
|       | 2          | PORTC |        | Port C group selected for external interrupt 11  |
|       | 3          | PORTD |        | Port D group selected for external interrupt 11  |
|       | 5          | PORTF |        | Port F group selected for external interrupt 11  |
| 11:8  | EXTIPSEL10 | 0x0   | RW     | <b>External Interrupt 10 Port Select</b><br>Select input port for external interrupt 10. |
|       | Value      | Mode  |        | Description  |
|       | 0          | PORTA |        | Port A group selected for external interrupt 10  |
|       | 1          | PORTB |        | Port B group selected for external interrupt 10  |
|       | 2          | PORTC |        | Port C group selected for external interrupt 10  |
|       | 3          | PORTD |        | Port D group selected for external interrupt 10  |
|       | 5          | PORTF |        | Port F group selected for external interrupt 10  |
| 7:4   | EXTIPSEL9  | 0x0   | RW     | <b>External Interrupt 9 Port Select</b><br>Select input port for external interrupt 9.   |
|       | Value      | Mode  |        | Description  |
|       | 0          | PORTA |        | Port A group selected for external interrupt 9   |
|       | 1          | PORTB |        | Port B group selected for external interrupt 9   |
|       | 2          | PORTC |        | Port C group selected for external interrupt 9   |
|       | 3          | PORTD |        | Port D group selected for external interrupt 9   |
|       | 5          | PORTF |        | Port F group selected for external interrupt 9   |
| 3:0   | EXTIPSEL8  | 0x0   | RW     | <b>External Interrupt 8 Port Select</b><br>Select input port for external interrupt 8.   |
|       | Value      | Mode  |        | Description  |
|       | 0          | PORTA |        | Port A group selected for external interrupt 8   |
|       | 1          | PORTB |        | Port B group selected for external interrupt 8   |

| Bit | Name | Reset | Access | Description                                    |
|-----|------|-------|--------|--|
| 2   |      | PORTC |        | Port C group selected for external interrupt 8 |
| 3   |      | PORTD |        | Port D group selected for external interrupt 8 |
| 5   |      | PORTF |        | Port F group selected for external interrupt 8 |

### 33.5.11 GPIO\_EXTIPINSELL - External Interrupt Pin Select Low Register

| Offset        | Bit Position |    |             |    |    |    |             |    |    |    |             |    |    |    |             |    |    |    |             |    |    |    |             |   |   |   |             |   |   |   |             |   |
|---------------|--------------|----|-------------|----|----|----|-------------|----|----|----|-------------|----|----|----|-------------|----|----|----|-------------|----|----|----|-------------|---|---|---|-------------|---|---|---|-------------|---|
| 0x408         | 31           | 30 | 29          | 28 | 27 | 26 | 25          | 24 | 23 | 22 | 21          | 20 | 19 | 18 | 17          | 16 | 15 | 14 | 13          | 12 | 11 | 10 | 9           | 8 | 7 | 6 | 5           | 4 | 3 | 2 | 1           | 0 |
| <b>Reset</b>  |              |    | 0x3         |    |    |    | 0x2         |    |    |    | 0x1         |    |    |    | 0x0         |    |    |    | 0x3         |    |    |    | 0x2         |   |   |   | 0x1         |   |   |   | 0x0         |   |
| <b>Access</b> |              |    | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    | RW          |    |    |    | RW          |   |   |   | RW          |   |   |   | RW          |   |
| <b>Name</b>   |              |    | EXTIPINSEL7 |    |    |    | EXTIPINSEL6 |    |    |    | EXTIPINSEL5 |    |    |    | EXTIPINSEL4 |    |    |    | EXTIPINSEL3 |    |    |    | EXTIPINSEL2 |   |   |   | EXTIPINSEL1 |   |   |   | EXTIPINSEL0 |   |

| Bit   | Name        | Reset  | Access      | Description  |
|-------|-------------|--|-------------|--|
| 31:30 | Reserved    | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |             |  |
| 29:28 | EXTIPINSEL7 | 0x3  | RW          | <b>External Interrupt 7 Pin Select</b><br>Select the pin for external interrupt 7. |
|       | Value       | Mode   | Description |  |
|       | 0           | PIN4   | Pin 4       |  |
|       | 1           | PIN5   | Pin 5       |  |
|       | 2           | PIN6   | Pin 6       |  |
|       | 3           | PIN7   | Pin 7       |  |
| 27:26 | Reserved    | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |             |  |
| 25:24 | EXTIPINSEL6 | 0x2  | RW          | <b>External Interrupt 6 Pin Select</b><br>Select the pin for external interrupt 6. |
|       | Value       | Mode   | Description |  |
|       | 0           | PIN4   | Pin 4       |  |
|       | 1           | PIN5   | Pin 5       |  |
|       | 2           | PIN6   | Pin 6       |  |
|       | 3           | PIN7   | Pin 7       |  |
| 23:22 | Reserved    | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |             |  |
| 21:20 | EXTIPINSEL5 | 0x1  | RW          | <b>External Interrupt 5 Pin Select</b><br>Select the pin for external interrupt 5. |
|       | Value       | Mode   | Description |  |
|       | 0           | PIN4   | Pin 4       |  |
|       | 1           | PIN5   | Pin 5       |  |
|       | 2           | PIN6   | Pin 6       |  |
|       | 3           | PIN7   | Pin 7       |  |

| Bit   | Name            | Reset   | Access      | Description  |
|-------|-----------------|---|-------------|--|
| 19:18 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 17:16 | EXTIPINSEL4     | 0x0   | RW          | <b>External Interrupt 4 Pin Select</b><br>Select the pin for external interrupt 4. |
|       | Value           | Mode  | Description |  |
|       | 0               | PIN4  | Pin 4       |  |
|       | 1               | PIN5  | Pin 5       |  |
|       | 2               | PIN6  | Pin 6       |  |
|       | 3               | PIN7  | Pin 7       |  |
| 15:14 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 13:12 | EXTIPINSEL3     | 0x3   | RW          | <b>External Interrupt 3 Pin Select</b><br>Select the pin for external interrupt 3. |
|       | Value           | Mode  | Description |  |
|       | 0               | PIN0  | Pin 0       |  |
|       | 1               | PIN1  | Pin 1       |  |
|       | 2               | PIN2  | Pin 2       |  |
|       | 3               | PIN3  | Pin 3       |  |
| 11:10 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 9:8   | EXTIPINSEL2     | 0x2   | RW          | <b>External Interrupt 2 Pin Select</b><br>Select the pin for external interrupt 2. |
|       | Value           | Mode  | Description |  |
|       | 0               | PIN0  | Pin 0       |  |
|       | 1               | PIN1  | Pin 1       |  |
|       | 2               | PIN2  | Pin 2       |  |
|       | 3               | PIN3  | Pin 3       |  |
| 7:6   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 5:4   | EXTIPINSEL1     | 0x1   | RW          | <b>External Interrupt 1 Pin Select</b><br>Select the pin for external interrupt 1. |
|       | Value           | Mode  | Description |  |
|       | 0               | PIN0  | Pin 0       |  |
|       | 1               | PIN1  | Pin 1       |  |
|       | 2               | PIN2  | Pin 2       |  |
|       | 3               | PIN3  | Pin 3       |  |

| Bit | Name            | Reset   | Access | Description  |
|-----|-----------------|---|--------|--|
| 3:2 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 1:0 | EXTIPINSEL0     | 0x0   | RW     | <b>External Interrupt 0 Pin Select</b><br>Select the pin for external interrupt 0. |
|     | Value           | Mode  |        | Description  |
|     | 0               | PIN0  |        | Pin 0  |
|     | 1               | PIN1  |        | Pin 1  |
|     | 2               | PIN2  |        | Pin 2  |
|     | 3               | PIN3  |        | Pin 3  |

## 33.5.12 GPIO\_EXTIPINSELH - External Interrupt Pin Select High Register

| Offset        | Bit Position |    |              |    |    |    |              |    |    |    |              |    |    |    |              |    |    |    |              |    |    |    |              |   |   |   |             |   |   |   |             |   |
|---------------|--------------|----|--------------|----|----|----|--------------|----|----|----|--------------|----|----|----|--------------|----|----|----|--------------|----|----|----|--------------|---|---|---|-------------|---|---|---|-------------|---|
| 0x40C         | 31           | 30 | 29           | 28 | 27 | 26 | 25           | 24 | 23 | 22 | 21           | 20 | 19 | 18 | 17           | 16 | 15 | 14 | 13           | 12 | 11 | 10 | 9            | 8 | 7 | 6 | 5           | 4 | 3 | 2 | 1           | 0 |
| <b>Reset</b>  |              |    | 0x3          |    |    |    | 0x2          |    |    |    | 0x1          |    |    |    | 0x0          |    |    |    | 0x3          |    |    |    | 0x2          |   |   |   | 0x1         |   |   |   | 0x0         |   |
| <b>Access</b> |              |    | RW           |    |    |    | RW           |    |    |    | RW           |    |    |    | RW           |    |    |    | RW           |    |    |    | RW           |   |   |   | RW          |   |   |   | RW          |   |
| <b>Name</b>   |              |    | EXTIPINSEL15 |    |    |    | EXTIPINSEL14 |    |    |    | EXTIPINSEL13 |    |    |    | EXTIPINSEL12 |    |    |    | EXTIPINSEL11 |    |    |    | EXTIPINSEL10 |   |   |   | EXTIPINSEL9 |   |   |   | EXTIPINSEL8 |   |

| Bit   | Name            | Reset | Access | Description   |
|-------|-----------------|-------|--------|---|
| 31:30 | <i>Reserved</i> |       |        | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |
| 29:28 | EXTIPINSEL15    | 0x3   | RW     | <b>External Interrupt 15 Pin Select</b><br>Select the pin for external interrupt 15.  |
|       | Value           | Mode  |        | Description   |
|       | 0               | PIN12 |        | Pin 12  |
|       | 1               | PIN13 |        | Pin 13  |
|       | 2               | PIN14 |        | Pin 14  |
|       | 3               | PIN15 |        | Pin 15  |
| 27:26 | <i>Reserved</i> |       |        | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |
| 25:24 | EXTIPINSEL14    | 0x2   | RW     | <b>External Interrupt 14 Pin Select</b><br>Select the pin for external interrupt 14.  |
|       | Value           | Mode  |        | Description   |
|       | 0               | PIN12 |        | Pin 12  |
|       | 1               | PIN13 |        | Pin 13  |
|       | 2               | PIN14 |        | Pin 14  |
|       | 3               | PIN15 |        | Pin 15  |
| 23:22 | <i>Reserved</i> |       |        | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |
| 21:20 | EXTIPINSEL13    | 0x1   | RW     | <b>External Interrupt 13 Pin Select</b><br>Select the pin for external interrupt 13.  |
|       | Value           | Mode  |        | Description   |
|       | 0               | PIN12 |        | Pin 12  |
|       | 1               | PIN13 |        | Pin 13  |
|       | 2               | PIN14 |        | Pin 14  |
|       | 3               | PIN15 |        | Pin 15  |

| Bit   | Name            | Reset   | Access      | Description  |
|-------|-----------------|---|-------------|--|
| 19:18 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 17:16 | EXTIPINSEL12    | 0x0   | RW          | <b>External Interrupt 12 Pin Select</b><br>Select the pin for external interrupt 12. |
|       | Value           | Mode  | Description |  |
|       | 0               | PIN12   | Pin 12      |  |
|       | 1               | PIN13   | Pin 13      |  |
|       | 2               | PIN14   | Pin 14      |  |
|       | 3               | PIN15   | Pin 15      |  |
| 15:14 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 13:12 | EXTIPINSEL11    | 0x3   | RW          | <b>External Interrupt 11 Pin Select</b><br>Select the pin for external interrupt 11. |
|       | Value           | Mode  | Description |  |
|       | 0               | PIN8  | Pin 8       |  |
|       | 1               | PIN9  | Pin 9       |  |
|       | 2               | PIN10   | Pin 10      |  |
|       | 3               | PIN11   | Pin 11      |  |
| 11:10 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 9:8   | EXTIPINSEL10    | 0x2   | RW          | <b>External Interrupt 10 Pin Select</b><br>Select the pin for external interrupt 10. |
|       | Value           | Mode  | Description |  |
|       | 0               | PIN8  | Pin 8       |  |
|       | 1               | PIN9  | Pin 9       |  |
|       | 2               | PIN10   | Pin 10      |  |
|       | 3               | PIN11   | Pin 11      |  |
| 7:6   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 5:4   | EXTIPINSEL9     | 0x1   | RW          | <b>External Interrupt 9 Pin Select</b><br>Select the pin for external interrupt 9.   |
|       | Value           | Mode  | Description |  |
|       | 0               | PIN8  | Pin 8       |  |
|       | 1               | PIN9  | Pin 9       |  |
|       | 2               | PIN10   | Pin 10      |  |
|       | 3               | PIN11   | Pin 11      |  |

| Bit | Name            | Reset   | Access      | Description  |
|-----|-----------------|---|-------------|--|
| 3:2 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 1:0 | EXTIPINSEL8     | 0x0   | RW          | <b>External Interrupt 8 Pin Select</b><br>Select the pin for external interrupt 8. |
|     | Value           | Mode  | Description |  |
|     | 0               | PIN8  | Pin 8       |  |
|     | 1               | PIN9  | Pin 9       |  |
|     | 2               | PIN10   | Pin 10      |  |
|     | 3               | PIN11   | Pin 11      |  |

### 33.5.13 GPIO\_EXTIRISE - External Interrupt Rising Edge Trigger Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x410         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | EXTIRISE |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
| 31:16 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 15:0  | EXTIRISE        | 0x0000  | RW     | <b>External Interrupt N Rising Edge Trigger Enable</b><br>Set bit n to enable triggering of external interrupt n on rising edge. |
|       | Value           | Description   |        |  |
|       | EXTIRISE[n] = 0 | Rising edge trigger disabled  |        |  |
|       | EXTIRISE[n] = 1 | Rising edge trigger enabled   |        |  |

### 33.5.14 GPIO\_EXTIFALL - External Interrupt Falling Edge Trigger Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x414         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | EXTIFALL |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description |
|-------|----------|--|--------|-------------|
| 31:16 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |             |

|                 |          |                               |    |  |
|-----------------|----------|-------------------------------|----|--|
| 15:0            | EXTIFALL | 0x0000                        | RW | <b>External Interrupt N Falling Edge Trigger Enable</b><br>Set bit n to enable triggering of external interrupt n on falling edge. |
| <b>Value</b>    |          | <b>Description</b>            |    |  |
| EXTIFALL[n] = 0 |          | Falling edge trigger disabled |    |  |
| EXTIFALL[n] = 1 |          | Falling edge trigger enabled  |    |  |

## 33.5.15 GPIO\_EXTILEVEL - External Interrupt Level Register

| Offset        | Bit Position |    |    |         |    |    |        |        |    |    |    |        |    |    |        |        |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
|---------------|--------------|----|----|---------|----|----|--------|--------|----|----|----|--------|----|----|--------|--------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|--|
| 0x418         | 31           | 30 | 29 | 28      | 27 | 26 | 25     | 24     | 23 | 22 | 21 | 20     | 19 | 18 | 17     | 16     | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| <b>Reset</b>  |              |    |    | 0       |    |    | 0      | 0      |    |    |    | 0      |    |    | 0      | 0      |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| <b>Access</b> |              |    |    | RW      |    |    | RW     | RW     |    |    |    | RW     |    |    | RW     | RW     |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |
| <b>Name</b>   |              |    |    | EM4WU12 |    |    | EM4WU9 | EM4WU8 |    |    |    | EM4WU4 |    |    | EM4WU1 | EM4WU0 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |  |

| Bit   | Name     | Reset | Access | Description  |
|-------|----------|-------|--------|--|
| 31:29 | Reserved |       |        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |
| 28    | EM4WU12  | 0     | RW     | <b>EM4 Wake Up Level for EM4WU12 Pin</b>   |
| 27:26 | Reserved |       |        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |
| 25    | EM4WU9   | 0     | RW     | <b>EM4 Wake Up Level for EM4WU9 Pin</b>  |
| 24    | EM4WU8   | 0     | RW     | <b>EM4 Wake Up Level for EM4WU8 Pin</b>  |
| 23:21 | Reserved |       |        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |
| 20    | EM4WU4   | 0     | RW     | <b>EM4 Wake Up Level for EM4WU4 Pin</b>  |
| 19:18 | Reserved |       |        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |
| 17    | EM4WU1   | 0     | RW     | <b>EM4 Wake Up Level for EM4WU1 Pin</b>  |
| 16    | EM4WU0   | 0     | RW     | <b>EM4 Wake Up Level for EM4WU0 Pin</b>  |
| 15:0  | Reserved |       |        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |

## 33.5.16 GPIO\_IF - Interrupt Flag Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x41C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0x0000       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> | R            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | EM4WU        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | EXT    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name  | Reset                           | Access | Description  |
|-------|-------|---------------------------------|--------|--|
| 31:16 | EM4WU | 0x0000                          | R      | <b>EM4 Wake Up Pin Interrupt Flag</b><br>EM4 wake up Pin Interrupt flag. |
|       | Value | Description                     |        |  |
|       | 0     | Interrupt flag cleared          |        |  |
|       | 1     | Interrupt flag set              |        |  |
| 15:0  | EXT   | 0x0000                          | R      | <b>External Pin Interrupt Flag</b><br>Pin n external interrupt flag.     |
|       | Value | Description                     |        |  |
|       | 0     | External interrupt flag cleared |        |  |
|       | 1     | External interrupt flag set     |        |  |

## 33.5.17 GPIO\_IFS - Interrupt Flag Set Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x420         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0x0000       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> | W1           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W1     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | EM4WU        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | EXT    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name  | Reset  | Access | Description  |
|-------|-------|--------|--------|--|
| 31:16 | EM4WU | 0x0000 | W1     | <b>Set EM4WU Interrupt Flag</b><br>Write 1 to set the EM4WU interrupt flag |
| 15:0  | EXT   | 0x0000 | W1     | <b>Set EXT Interrupt Flag</b><br>Write 1 to set the EXT interrupt flag     |

## 33.5.18 GPIO\_IFC - Interrupt Flag Clear Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x424         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0x0000       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> | (R)W1        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | (R)W1  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | EM4WU        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | EXT    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name  | Reset  | Access | Description   |
|-------|-------|--------|--------|---|
| 31:16 | EM4WU | 0x0000 | (R)W1  | <b>Clear EM4WU Interrupt Flag</b><br>Write 1 to clear the EM4WU interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.). |
| 15:0  | EXT   | 0x0000 | (R)W1  | <b>Clear EXT Interrupt Flag</b><br>Write 1 to clear the EXT interrupt flag. Reading returns the value of the IF and clears the corresponding interrupt flags (This feature must be enabled globally in MSC.).     |

## 33.5.19 GPIO\_IEN - Interrupt Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x428         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0x0000       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | EM4WU        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | EXT    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name  | Reset  | Access | Description   |
|-------|-------|--------|--------|---|
| 31:16 | EM4WU | 0x0000 | RW     | <b>EM4WU Interrupt Enable</b><br>Enable/disable the EM4WU interrupt |
| 15:0  | EXT   | 0x0000 | RW     | <b>EXT Interrupt Enable</b><br>Enable/disable the EXT interrupt     |

## 33.5.20 GPIO\_EM4WUEN - EM4 Wake Up Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x42C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0x0000       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | EM4WUEN      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description   |
|-------|----------|--|--------|---|
| 31:16 | EM4WUEN  | 0x0000   | RW     | <b>EM4 Wake Up Enable</b><br>Write 1 to enable EM4 wake up request, write 0 to disable EM4 wake up request. |
|       | Value    |  |        | Description   |
|       | 0        |  |        | Disable EM4 wake up on pin  |
|       | 1        |  |        | Enable EM4 wake up on pin   |
| 15:0  | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |

## 33.5.21 GPIO\_ROUTEPEN - I/O Routing Pin Enable Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |           |           |           |           |            |    |    |    |    |    |   |   |   |   |   |   |   |        |        |        |             |             |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|-----------|-----------|-----------|-----------|------------|----|----|----|----|----|---|---|---|---|---|---|---|--------|--------|--------|-------------|-------------|
| 0x440         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19        | 18        | 17        | 16        | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2      | 1      | 0      |             |             |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    | 0         | 0         | 0         | 0         | 0          |    |    |    |    |    |   |   |   |   |   |   |   | 0      | 1      | 1      | 1           | 1           |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    | RW        | RW        | RW        | RW        | RW         |    |    |    |    |    |   |   |   |   |   |   |   | RW     | RW     | RW     | RW          | RW          |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    | ETMTD3PEN | ETMTD2PEN | ETMTD1PEN | ETMTD0PEN | ETMTCLKPEN |    |    |    |    |    |   |   |   |   |   |   |   | SWVPEN | TDIPEN | TDOPEN | SWDIOTMSPEN | SWCLKTCKPEN |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:21 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 20    | ETMTD3PEN       | 0   | RW     | <b>ETM Trace Data Pin Enable</b><br>Enable ETM Trace Data Output 3 connection to pin.   |
| 19    | ETMTD2PEN       | 0   | RW     | <b>ETM Trace Data Pin Enable</b><br>Enable ETM Trace Data Output 2 connection to pin.   |
| 18    | ETMTD1PEN       | 0   | RW     | <b>ETM Trace Data Pin Enable</b><br>Enable ETM Trace Data Output 1 connection to pin.   |
| 17    | ETMTD0PEN       | 0   | RW     | <b>ETM Trace Data Pin Enable</b><br>Enable ETM Trace Data Output 0 connection to pin.   |
| 16    | ETMTCLKPEN      | 0   | RW     | <b>ETM Trace Clock Pin Enable</b><br>Enable ETM Trace Clock Output connection to pin.   |
| 15:5  | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 4     | SWVPEN          | 0   | RW     | <b>Serial Wire Viewer Output Pin Enable</b><br>Enable Serial Wire Viewer connection to pin.   |
| 3     | TDIPEN          | 1   | RW     | <b>JTAG Test Debug Input Pin Enable</b><br>Enable JTAG TDI connection to pin.   |
| 2     | TDOPEN          | 1   | RW     | <b>JTAG Test Debug Output Pin Enable</b><br>Enable JTAG TDO connection to pin.  |
| 1     | SWDIOTMSPEN     | 1   | RW     | <b>Serial Wire Data and JTAG Test Mode Select Pin Enable</b><br>Enable Serial Wire Data and JTAG Test Mode Select connection to pin. WARNING: When this pin is disabled, the device can no longer be accessed by a debugger. A reset will set the pin back to a default state as enabled. If you disable this pin, make sure you have at least a 3 second timeout at the start of you program code before you disable the pin. This way, the debugger will have time to halt the device after a reset before the pin is disabled. |
| 0     | SWCLKTCKPEN     | 1   | RW     | <b>Serial Wire Clock and JTAG Test Clock Pin Enable</b><br>Enable Serial Wire and JTAG Clock connection to pin. WARNING: When this pin is disabled, the device can no longer be accessed by a debugger. A reset will set the pin back to a default state as enabled. If you disable this pin, make sure you have at least a 3 second timeout at the start of you program code before you disable the pin. This way, the debugger will have time to halt the device after a reset before the pin is disabled.                      |

### 33.5.22 GPIO\_ROUTELOC0 - I/O Routing Location Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |        |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|--------|---|---|---|---|---|---|---|
| 0x444         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | 0x00   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | RW     |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   | SWVLOC |   |   |   |   |   |   |   |

| Bit  | Name            | Reset   | Access      | Description  |
|------|-----------------|---|-------------|--|
| 31:6 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |             |  |
| 5:0  | SWVLOC          | 0x00  | RW          | <b>I/O Location</b><br>Decides the location of the SWV pins. |
|      | Value           | Mode  | Description |  |
|      | 0               | LOC0  | Location 0  |  |
|      | 1               | LOC1  | Location 1  |  |
|      | 2               | LOC2  | Location 2  |  |
|      | 3               | LOC3  | Location 3  |  |

### 33.5.23 GPIO\_ROUTELOC1 - I/O Routing Location Register 1

| Offset        | Bit Position |    |    |    |           |    |    |    |           |    |    |    |           |    |    |    |    |    |    |    |            |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|-----------|----|----|----|-----------|----|----|----|-----------|----|----|----|----|----|----|----|------------|----|---|---|---|---|---|---|---|---|---|---|
| 0x448         | 31           | 30 | 29 | 28 | 27        | 26 | 25 | 24 | 23        | 22 | 21 | 20 | 19        | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11         | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0x00         |    |    |    | 0x00      |    |    |    | 0x00      |    |    |    | 0x00      |    |    |    |    |    |    |    | 0x00       |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> | RW           |    |    |    | RW        |    |    |    | RW        |    |    |    | RW        |    |    |    |    |    |    |    | RW         |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | ETMTD3LOC    |    |    |    | ETMTD2LOC |    |    |    | ETMTD1LOC |    |    |    | ETMTD0LOC |    |    |    |    |    |    |    | ETMTCLKLOC |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name      | Reset | Access | Description  |
|-------|-----------|-------|--------|--|
| 31:26 | ETMTD3LOC | 0x00  | RW     | <b>I/O Location</b><br>Decides the location of ETM TD3 |
|       | Value     | Mode  |        | Description  |
|       | 0         | LOC0  |        | Location 0   |
|       | 1         | LOC1  |        | Location 1   |
|       | 2         | LOC2  |        | Location 2   |
|       | 3         | LOC3  |        | Location 3   |
| 25:20 | ETMTD2LOC | 0x00  | RW     | <b>I/O Location</b><br>Decides the location of ETM TD2 |
|       | Value     | Mode  |        | Description  |
|       | 0         | LOC0  |        | Location 0   |
|       | 1         | LOC1  |        | Location 1   |
|       | 2         | LOC2  |        | Location 2   |
|       | 3         | LOC3  |        | Location 3   |
| 19:14 | ETMTD1LOC | 0x00  | RW     | <b>I/O Location</b><br>Decides the location of ETM TD1 |
|       | Value     | Mode  |        | Description  |
|       | 0         | LOC0  |        | Location 0   |
|       | 1         | LOC1  |        | Location 1   |
|       | 2         | LOC2  |        | Location 2   |
|       | 3         | LOC3  |        | Location 3   |
| 13:8  | ETMTD0LOC | 0x00  | RW     | <b>I/O Location</b><br>Decides the location of ETM TD0 |
|       | Value     | Mode  |        | Description  |
|       | 0         | LOC0  |        | Location 0   |

| Bit | Name            | Reset   | Access | Description   |
|-----|-----------------|---|--------|---|
|     | 1               | LOC1  |        | Location 1  |
|     | 2               | LOC2  |        | Location 2  |
|     | 3               | LOC3  |        | Location 3  |
| 7:6 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 5:0 | ETMTCLKLOC      | 0x00  | RW     | <b>I/O Location</b><br>Decides the location of ETM TCLK |
|     | Value           | Mode  |        | Description   |
|     | 0               | LOC0  |        | Location 0  |
|     | 1               | LOC1  |        | Location 1  |
|     | 2               | LOC2  |        | Location 2  |
|     | 3               | LOC3  |        | Location 3  |

### 33.5.24 GPIO\_INSENSE - Input Sense Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |       |     |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-------|-----|
| 0x450         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0   |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | 1     | 1   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | RW    | RW  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | EM4WU | INT |

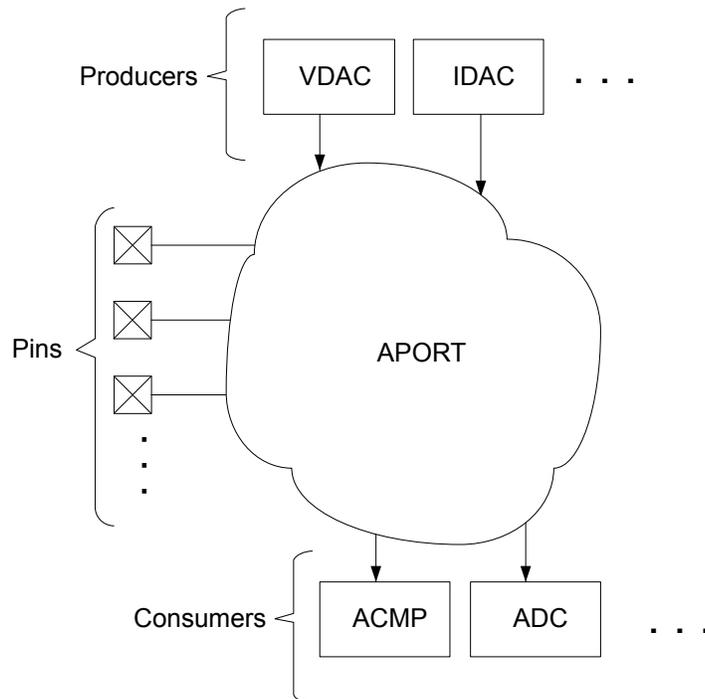
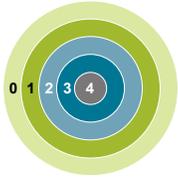
| Bit  | Name            | Reset   | Access | Description   |
|------|-----------------|---|--------|---|
| 31:2 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 1    | EM4WU           | 1   | RW     | <b>EM4WU Interrupt Sense Enable</b><br>Set this bit to enable input sensing for EM4WU interrupts. |
| 0    | INT             | 1   | RW     | <b>Interrupt Sense Enable</b><br>Set this bit to enable input sensing for interrupts.             |

## 33.5.25 GPIO\_LOCK - Configuration Lock Register

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x454         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LOCKKEY |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name            | Reset  | Access | Description   |
|-------|-----------------|--|--------|---|
| 31:16 | Reserved        | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |   |
| 15:0  | LOCKKEY         | 0x0000   | RWH    | <b>Configuration Lock Key</b><br>Write any other value than the unlock code to lock MODEL, MODEH, CTRL, PINLOCKN, OVTDIS, EXTIPSELL, EXTIPSELH, EXTIGSELL, EXTIGSELH, INSENSE, ROUTEPEN, and ROUTELOC0 from editing. Write the unlock code to unlock. When reading the register, bit 0 is set when the lock is enabled. |
|       | Mode            | Value  |        | Description   |
|       | Read Operation  |  |        |   |
|       | UNLOCKED        | 0  |        | GPIO registers are unlocked   |
|       | LOCKED          | 1  |        | GPIO registers are locked   |
|       | Write Operation |  |        |   |
|       | LOCK            | 0  |        | Lock GPIO registers   |
|       | UNLOCK          | 0xA534   |        | Unlock GPIO registers   |

## 34. APORT - Analog Port



### Quick Facts

#### What?

The Analog Port (APORT) is a set of analog buses which are used to connect I/O pins to analog peripheral signals.

#### Why?

The APORT gives on-chip analog resources access to a large number of I/O pins, and provides the system designer with a high degree of routing flexibility.

#### How?

An analog peripheral requests a pad by simply configuring its input/output to use a channel on APORT. That selection becomes an APORT request where the APORT control switches the pad and the analog signal onto a common bus.

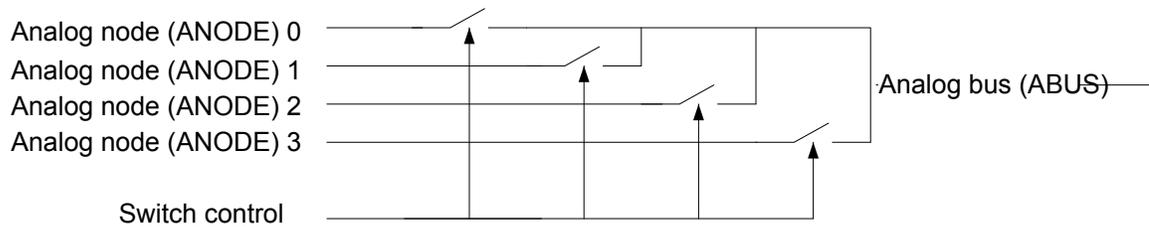
### 34.1 Introduction

APORT consists of wires, switches, and control logic needed to route signals between analog peripherals and I/O pins. On-chip clients can be either producers or consumers. Analog producers are active devices that drive current/voltage into an APORT, such as current or voltage DACs. Consumers are passive devices that monitor or react to the current/voltage routed to them via the APORT, such as ADCs or analog comparators (ACMP).

### 34.2 Features

- Pins are typically mapped to two different APORT buses
- Arbitration and conflict status provided to each APORT client

### 34.3 Functional Description



**Figure 34.1. Analog Bus (ABUS)**

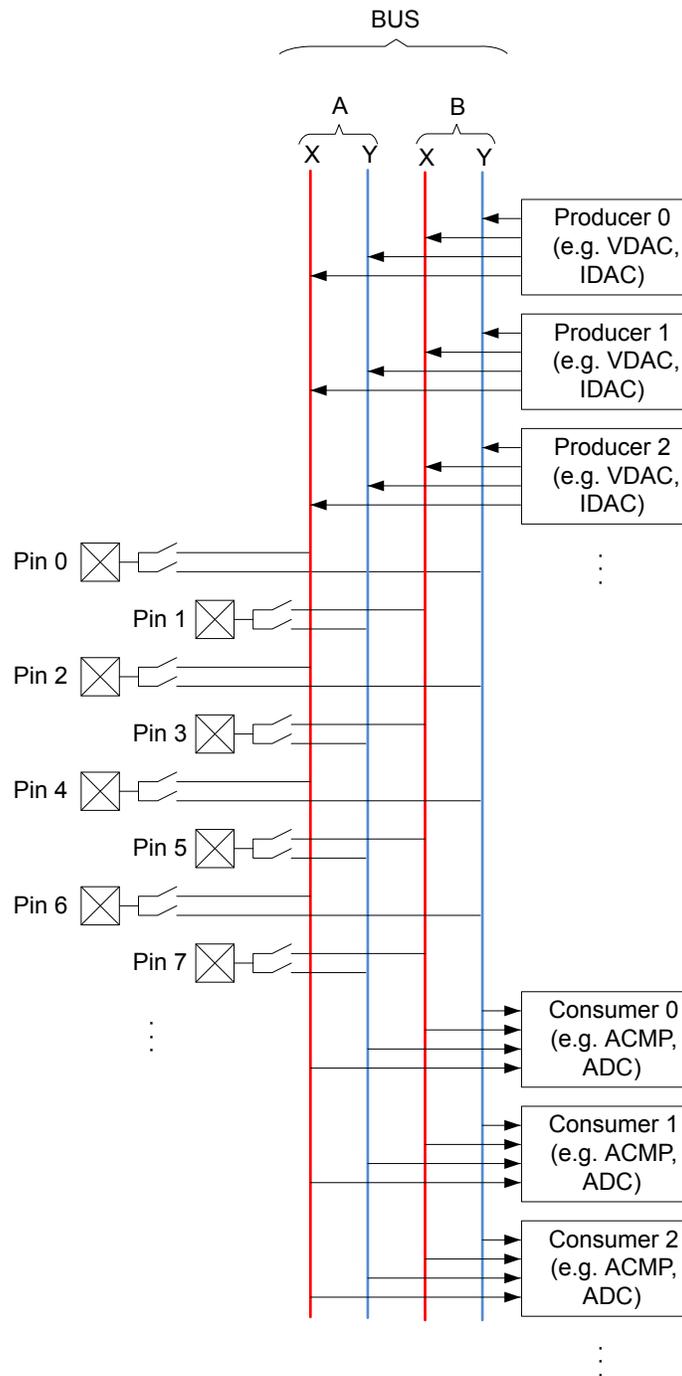
An analog bus (ABUS) consists of analog switches connected to a common wire as shown in [Figure 34.1 Analog Bus \(ABUS\) on page 1170](#). An APORT consists of multiple ABUSes. Since many clients can operate differentially, buses are grouped by pairs as X and Y. If a given client uses a single ABUS (e.g. single-ended ADC), X and Y are just labels to differentiate the two buses.

When operating differentially, most APORT clients require that one input be chosen from an X bus and the other from a Y bus. For example, the ACMP block will not allow both positive and negative inputs to be chosen from X buses.

#### 34.3.1 I/O Pin Considerations

For external analog signals routed through the APORT, the maximum supported analog I/O voltage will typically be limited to  $\text{MIN}(V_{\text{ANALOGSUPPLY}}, \text{IOVDD})$  (where  $V_{\text{ANALOGSUPPLY}}$  is the supply pin powering the analog module). Practically, this means that if  $\text{IOVDD}=1.8\text{ V}$ , the maximum supported analog IO voltage on APORT-routed signals will be limited to 1.8 V, regardless of the analog module supply voltage.

### 34.3.2 APORT ABUS Naming

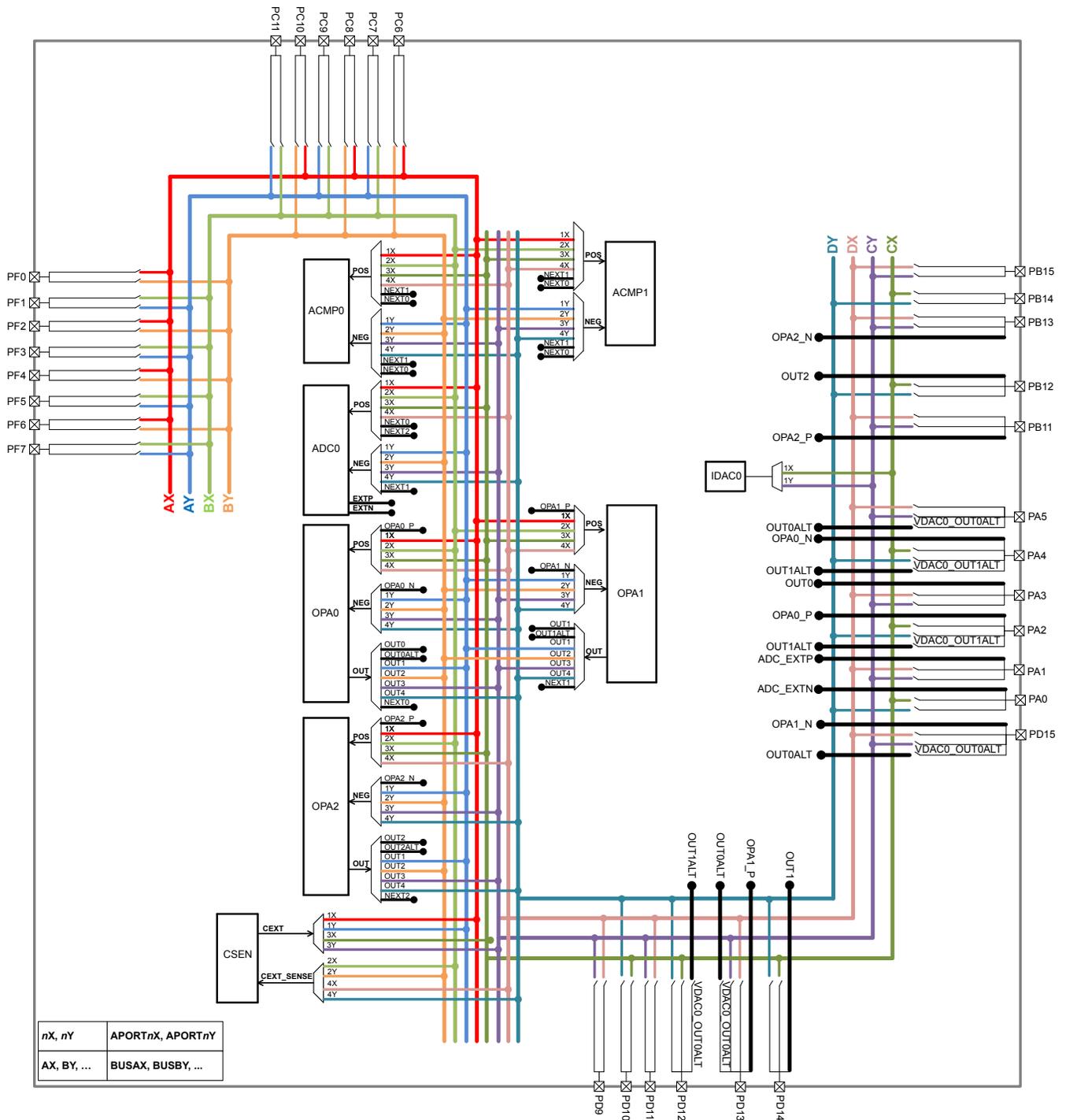


**Figure 34.2. Conceptual APORT Structure**

APORT ABUSes are prefixed with "BUS" and are grouped in pairs. Each pair is uniquely identified using a letter prefix ("A", "B", "C", etc.) followed by either a "X" or "Y" to identify the ABUS in the pair. For example, "BUSDX" decodes as: "BUS"=ABUS, "D"=pair, "X"=bus. [Figure 34.2 Conceptual APORT Structure on page 1171](#) illustrates this organization.

APORT clients are generally described once in this reference manual regardless of its number of instances. For example, the ACMP client is described once, but the device could contain multiple instances of the ACMP. Because of this, for APORT client descriptions in this reference manual, the ABUS connections are generalized with the prefix "APORT" followed by a number (instead of the "BUS"

followed by a letter). It is possible that different instances of an APORT client connect to different ABUSes. For example, ACMP0 APORT1X might connect to the ABUS BUSAX while ACMP1 APORT1X might connect to ABUS BUSCX. Refer to the APORT Client Map in the device data sheet to map the generalized APORT client bus name to an actual device ABUS. A given ABUS has multiple switches which need to be identified. The switches on a bus are specified with the ABUS connection ID followed by a channel ID. For example, channel switch 7 on a given APORT client might be given as APORT1XCH7. Not all APORT channels map to actual GPIO. Refer to the APORT Client Maps in the device data sheet for APORT to GPIO mapping.



**Figure 34.3. Detailed APORT Structure**

Figure 34.3 Detailed APORT Structure on page 1172 shows all the possible routes between different peripherals and different pins via APORT BUS for the largest package of the EFR32 device family. Note that, in the figure, the BUSxX and BUSxY are annotated as xX and xY, where x=A,B,C,D and the APORTnX and APORTnY are annotated as nX and nY, where n=1,2,3,4.

For example, the IDAC APORT output 1X can be routed to pin PB14 through BUSCX. The configuration required for this routing is as follows:

- Set `IDAC_CTRL_APORTOUTSEL = APORT1XCH30`. This selects the IDAC APORT output 1X and pin PB14.
- Set `IDAC_CTRL_APORTOUTEN = 1` and `IDAC_CTRL_APORTOUTENPRS = 0`. This enables the IDAC to ungate it's output to BUSCX.

Another example, when ADC is configured to operate in single channel mode for differential inputs (see [27.3.3.1 Single Channel Mode](#) for how to configure ADC in single channel mode), the positive ADC APORT input 2X and the negative ADC APORT input 2Y can be routed to pin PC9 and PC10 via BUSBX and BUSBY respectively with the following configuration:

- Set `ADCn_SINGLECTRL_POSSEL = APORT2XCH9`. This selects the pin PC9 for the positive input to the ADC.
- Set `ADCn_SINGLECTRL_NEGSEL = APORT2YCH10`. This selects the pin PC10 for the negative input to the ADC.

For smaller packages, not all GPIO pins are available. See the pinout sections of the device data sheet for pin availability on a specific device.

### 34.3.3 Managing ABUSes

The ABUSes of an APORT are shared resources. The user needs to be mindful of this in assigning I/O for different clients throughout the chip, as it is possible to have conflicts for a given ABUS. Each ABUS has an arbiter responsible for limiting the control over the ABUS to one and only one client. If multiple clients attempt to control an ABUS, the arbiter allows no client control over the ABUS and asserts a conflict signal to the clients. The user has the ability to check for such a conflict in each client's status, as well as generate an interrupt.

Having only one client control an ABUS is not the same as having only one user of an ABUS. It is possible for multiple clients to access a single ABUS, but requires all but one client to relinquish control of the ABUS. To do this, some clients have bits to disable bus master-ship which are 0 by default. One example is the APORTEXMASTERDIS bit in the ACMPn\_CTRL. When set to 1, the client will not assert control of the APORT X BUS switches, but may still connect to an APORT X BUS that is controlled by another client.

For example, the ADC and ACMP both want to use the same pin on a particular ABUS the user might set the bus master disable bit to 1 for the ACMP. The ADC is the sole master of the switch configuration on that ABUS, so switches are configured using the configuration set in the ADC. When the ACMP channel is chosen on that same bus, the actual pin connection is dictated by the ADC settings for that bus.

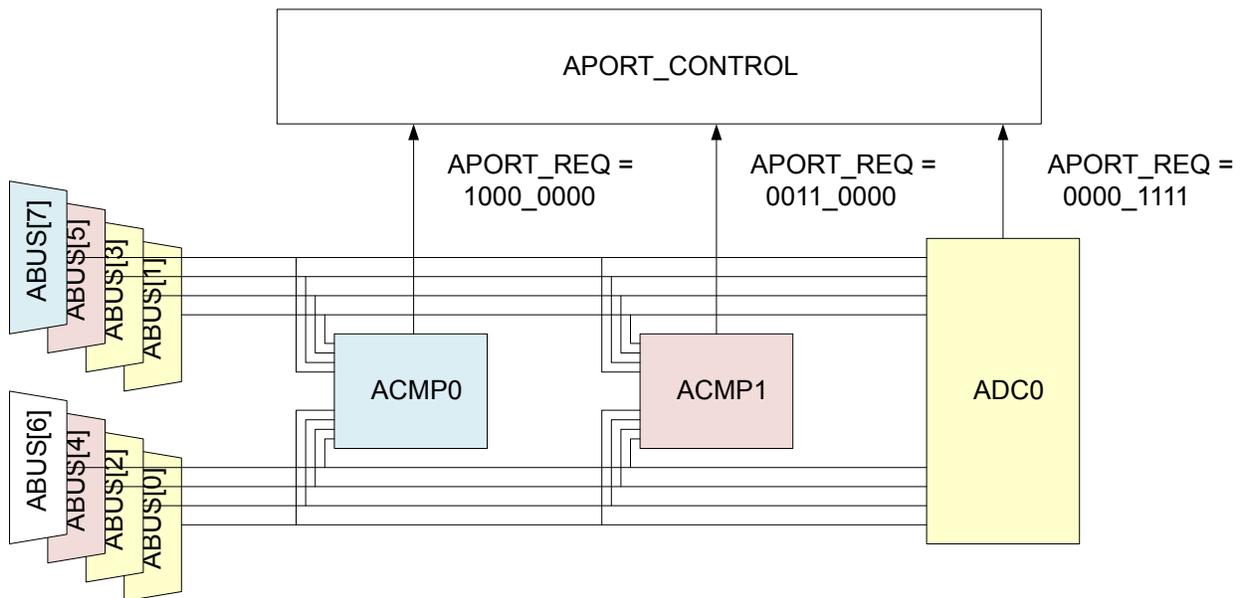


Figure 34.4. APORT Example 1

Figure 34.4 APORT Example 1 on page 1174 illustrates the sharing of APORT. For illustration purposes, each ABUS is identified by a numeric index (instead of BUSAX, BUSAY, BUSBX, etc.). Also, the requests from all the APORT clients are packed into a bit-vector named APORT\_REQ to illustrate the request from the APORT Clients (instead of by name such as APORT1XREQ, APORT1YREQ, APORT2XREQ, etc.). In Figure 34.4 APORT Example 1 on page 1174, ABUS and client are the same color if the client has been granted the ABUS.

In Figure 34.4 APORT Example 1 on page 1174 ADC0 has requested ABUS[3:0], ACMP1 has requested ABUS[5:4], ACMP0 has requested ABUS[7], and ABUS[6] is unused. No APORT Client has requested the same ABUS as another, so there is no conflict.

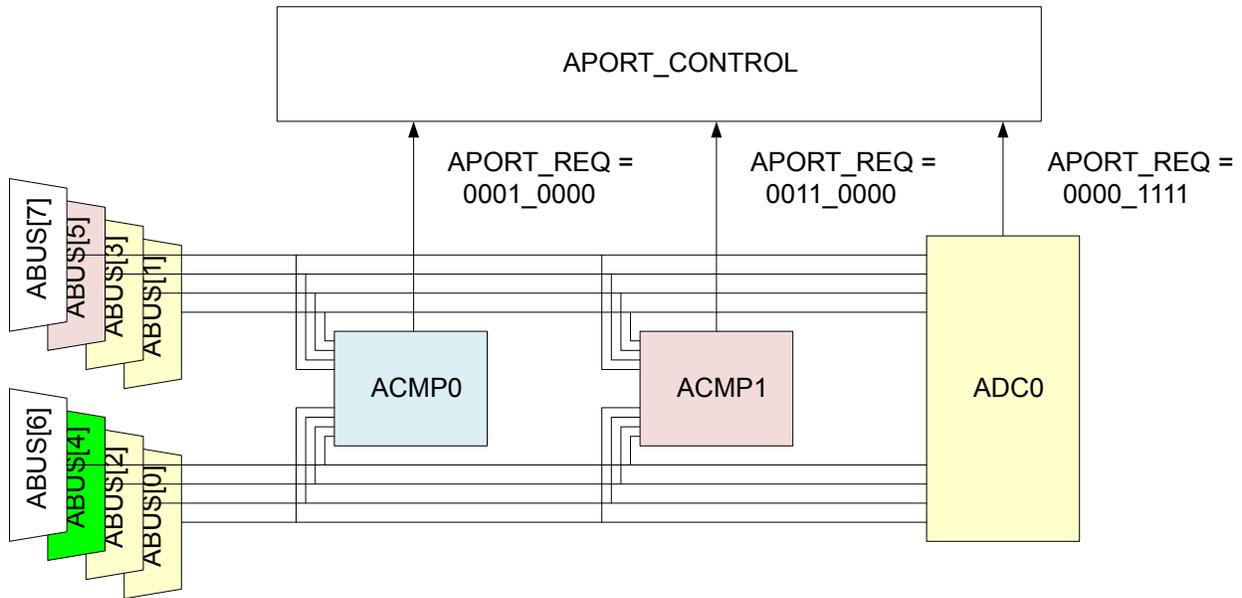


Figure 34.5. APORT Example 2: Bus Conflict

In Figure 34.5 APORT Example 2: Bus Conflict on page 1175 is a similar example to Figure 34.4 APORT Example 1 on page 1174, but now both ACMP0 and ACMP1 are requesting ABUS[4]. This is a configuration error, so APORT grants neither client ABUS[4]. The user must resolve the conflict before ABUS[4] is useable.

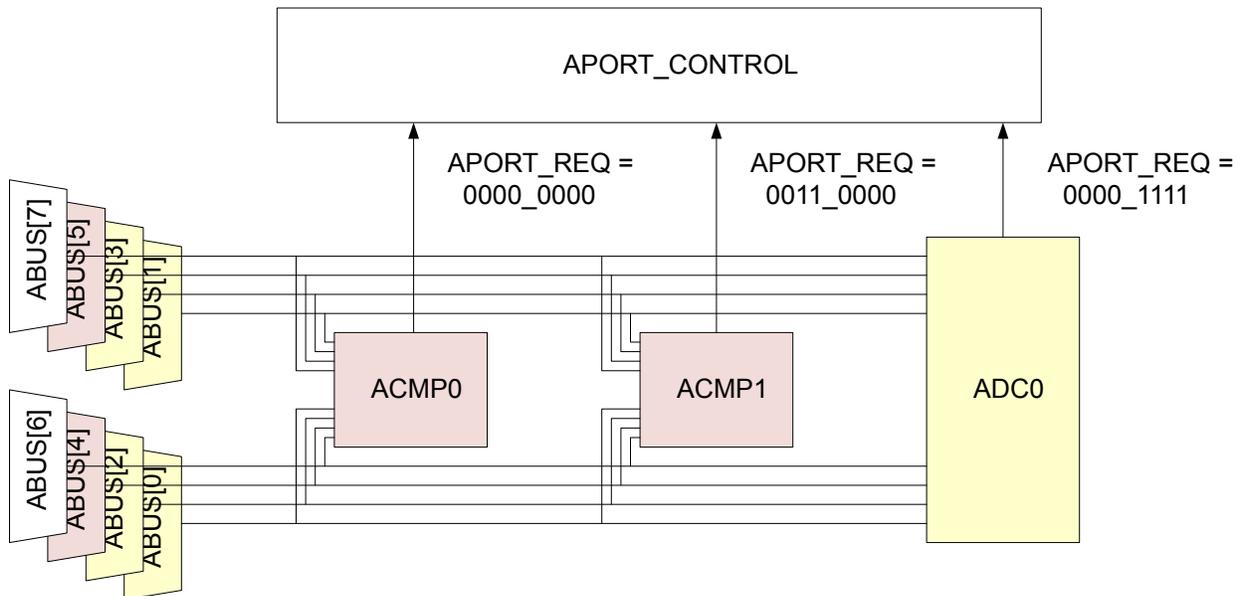
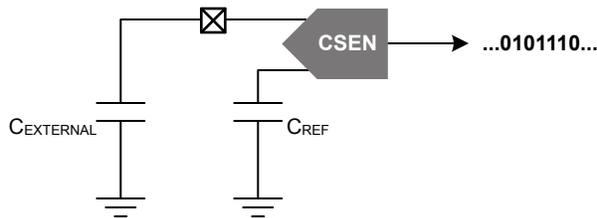
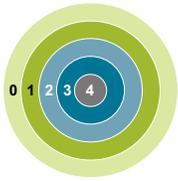


Figure 34.6. APORT Example 3: Sharing an ABUS

Figure 34.6 APORT Example 3: Sharing an ABUS on page 1175 illustrates ABUS sharing. Both ACMPs are configured identically, except ACMP0 has its APORTXMASTERDIS bit-field set to 1. There is only one APORT master for ABUS[5:4] in this case, so there is no conflict.

### 35. CSEN - Capacitive Sense Module



#### Quick Facts

##### What?

The capacitive sense (CSEN) module uses a capacitance-to-digital circuit to measure the capacitance of touch-sensitive switches. The module contains an advanced capacitance-to-digital converter that can be configured to take measurements on a single port pin or scan through a group of up to 64 port pins connected via the APORT buses. Port pins/channels can also be shorted together internally to measure the combined capacitance, lowering the required energy usage for wake-on-touch applications. Adjustable maximum capacitance allows for optimal dynamic range, while hardware accumulation and filtering reduce processor computation time. Interrupts can be generated when CSEN completes conversions or when the measured value crosses a threshold.

##### Why?

The CSEN module is designed to perform extremely low-power autonomous conversions of capacitive touch switches.

##### How?

The CSEN module uses charge timing techniques to compare external capacitance against internal reference capacitors.

#### 35.1 Introduction

The capacitive sensing (CSEN) module uses a capacitance-to-digital circuit to determine the capacitance on an input pin. The module can take measurements from different physical pins using the APORT multiplexer. In addition, the module can measure multiple pins in sequence using the scan modes, or multiple pins at the same time (bonded together) using the multiple-channel measurement feature. CSEN is available in EM0, EM1, EM2 and EM3.

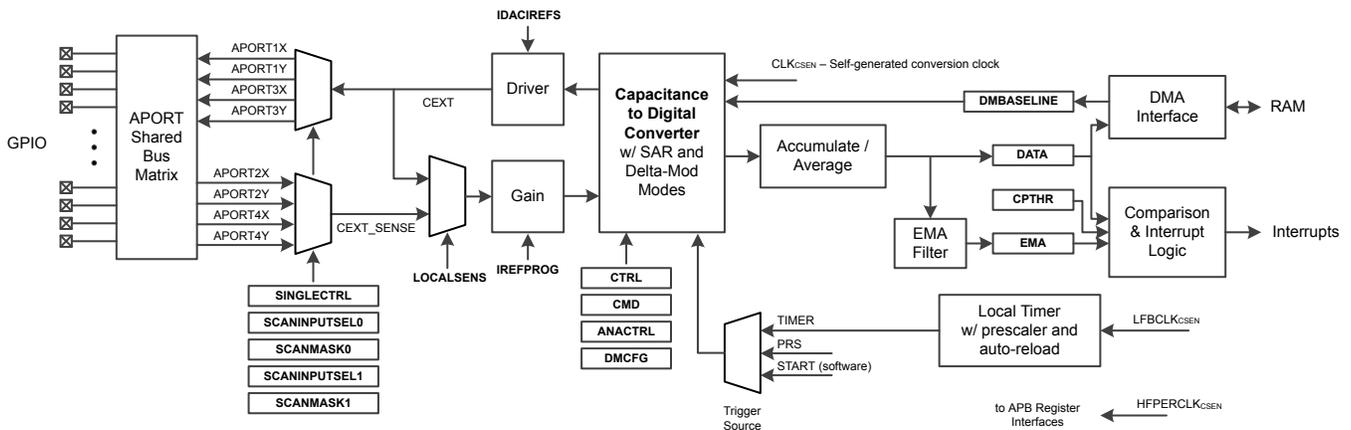


Figure 35.1. CSEN Overview

## 35.2 Features

- Up to 64 Channels, connected via APORT buses.
- Single sample, continuous single sample, single scan and continuous scan modes supported.
- Support for both SAR and Delta Modulation conversions.
  - SAR conversions are programmable to resolutions of 10, 12, 14, or 16 bits.
  - Delta Modulation conversions support dynamic or fixed gain, and are programmable to resolutions of 10, 12, 14, or 16 bits.
- Supports channel bonding to monitor multiple channels, shorted internally, with a single conversion. The maximum number of channels to be shorted is limited by the maximum capacitance that can be measured by the analog core.
- Conversions triggered by software, PRS, or dedicated timer running from LFXO, LFRCO, or ULFRCO.
- Hardware accumulation of 1, 2, 4, 8, 16, 32, or 64 samples. The result can be right-shifted to the desired resolution or collected in a 22-bit accumulator for further processing by software.
- Hardware exponential moving average (EMA) filter for candidate touch detection during low power autonomous operation.
- Automatic threshold comparison with programmable polarity.
- Low-frequency noise filter to reject noise sources such as 50/60 Hz.
- DMA interface to collect accumulated samples in on-chip RAM. The DMA interface can also be used to program starting values for delta-modulation conversions. The DMA interface can run down to EM2.

## 35.3 Timing

Conversion timing for the CSEN block is flexible, with access to several clocks and conversion trigger sources.

### 35.3.1 Clocks

The CSEN module takes two external clock sources as input. The register interface is driven by the HUPERCLK source, allowing for fast access to the control and data for the block. The local timer is driven by the LFBCLK source. The CSEN block also contains an internal, low-energy conversion clock source ( $CLK_{CSEN}$ ). Conversions are self-timed and the block only requires external clocks under certain circumstances.

For register access,  $HUPERCLK_{CSEN}$  must be enabled to the CSEN block in the  $CMU\_HUPERCLKEN0$  register. When register access is not required, this clock may be shut down for energy savings.

$LFBCLK_{CSEN}$  is used by the local CSEN timer. It should be enabled to the CSEN block in the  $CMU\_LFBCLKEN0$  register any time the CSEN local timer is used as a conversion trigger.

### 35.3.2 Conversion Triggers

CSEN conversions can be triggered from one of three different sources, selected by  $CTRL\_STM$ : a software register write, a PRS channel, or the local CSEN timer. The selected trigger source begins a conversion cycle. Depending on the selected conversion mode, one conversion trigger may generate one or many output words from the CSEN module. See [35.6 Conversion Modes](#) for more details on the CSEN output for each mode.

#### Software Triggered Conversions

When  $CTRL\_STM$  is set to START, conversions are triggered by software. Software triggering is typically used when operating the CSEN block in a continuous mode to gather conversions as quickly as the converter allows. Software triggering may also be used in applications where a single conversion or one scan cycle is needed infrequently and sporadically by different software processes. When configured for software triggering, a write of the  $CMD\_START$  bit to logic 1 initiates conversions.

#### PRS Triggered Conversions

When  $CTRL\_STM$  is set to PRS, conversions are triggered via a PRS event. PRS triggers are typically used when it is necessary to synchronize CSEN conversions with other events in the system. For example, the LETIMER may be used in EM2 to initiate a CSEN scan operation and other events at the same time. A number of different PRS channels may be configured as the trigger source. The specific PRS channel to be used as a trigger source is selected in the  $PRSEL$  register.

## CSEN Timer Triggered Conversions

When CTRL\_STM is set to TIMER, a local 8-bit CSEN timer is used to trigger conversions. The local timer is typically used in conjunction with non-continuous conversion modes to provide periodic conversion triggers at slow sampling rates. The local timer is clocked from LFBCLK<sub>CSEN</sub>, and configured with the TIMCTRL register. The CSEN timer has a local prescaler (set by the TIMCTRL\_PCPRESC field), which divides the LFBCLK<sub>CSEN</sub> further. The TIMCTRL\_PCTOP field sets the reload value for the CSEN timer. The CSEN timer counts down for the number of clocks specified in TIMCTRL\_PCTOP. When the counter reaches zero, a conversion cycle is triggered and the timer is reloaded.

### 35.3.3 Shutdown and Warmup

Many target applications for CSEN require low power operation and infrequent sampling. By default, the converter will power down when it is not in use to save energy. Upon receiving a conversion trigger, the CSEN block will power on and wait for (3 + TIMCTRL\_WARMPCNT) CLK<sub>CSEN</sub> clock cycles before starting conversions.

CTRL\_WARMUPMODE defines the behavior of the CSEN converter when it is not actively converting. Software may choose to keep the CSEN block powered on at all times by setting the CTRL\_WARMUPMODE bit to logic 1.

## 35.4 Conversion Types

The CSEN block offers two different types of conversions: SAR, and Delta Modulation.

### 35.4.1 SAR Conversion Type

SAR (successive approximation register) conversions are self-contained and do not depend on the results of any previous conversions. SAR conversions will be performed when CTRL\_CONVSEL is set to SAR. CTRL\_SARCR sets the SAR conversion resolution, and is selectable between 10, 12, 14, or 16 bits. SAR conversions last for N cycles of CLK<sub>CSEN</sub>, where N is the selected resolution (i.e. 12-bit conversions last for 12 CLK<sub>CSEN</sub> cycles).

Every SAR conversion consists of a set of tests, one for each bit of the converter. The MSB is tested first, followed by all other bits down to the LSB. Each test narrows the possible value by 1/2 until the final result is determined.

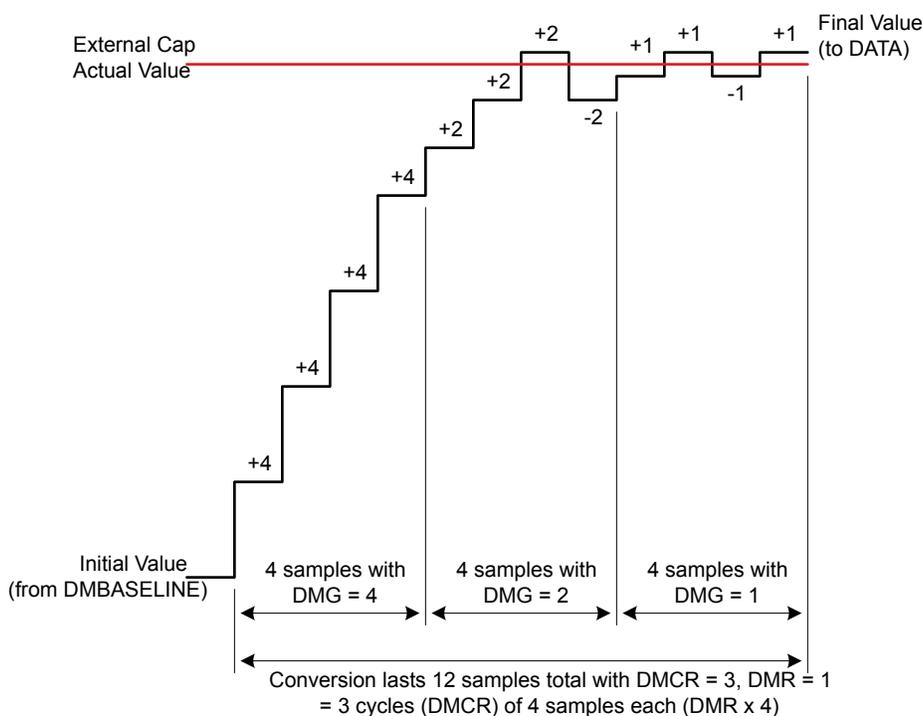
### 35.4.2 Delta Modulation Conversion Type

Delta modulation (DM) conversions provide significant noise, response time, and energy consumption improvements over SAR conversions. A DM conversion inherently takes longer than a SAR conversion to arrive at one result. However, it is much less susceptible to noise events in the system. Whereas a large number of SAR conversions may need to be averaged to produce a desired noise resolution, the same noise resolution can be achieved with few DM conversions. However, DM conversions require more specific knowledge of the underlying conversion process to implement effectively. Silicon Laboratories software libraries use delta modulation for the best possible performance. It is recommended to use the provided libraries in most applications. The information provided in this section is intended as a reference for CSEN module driver development.

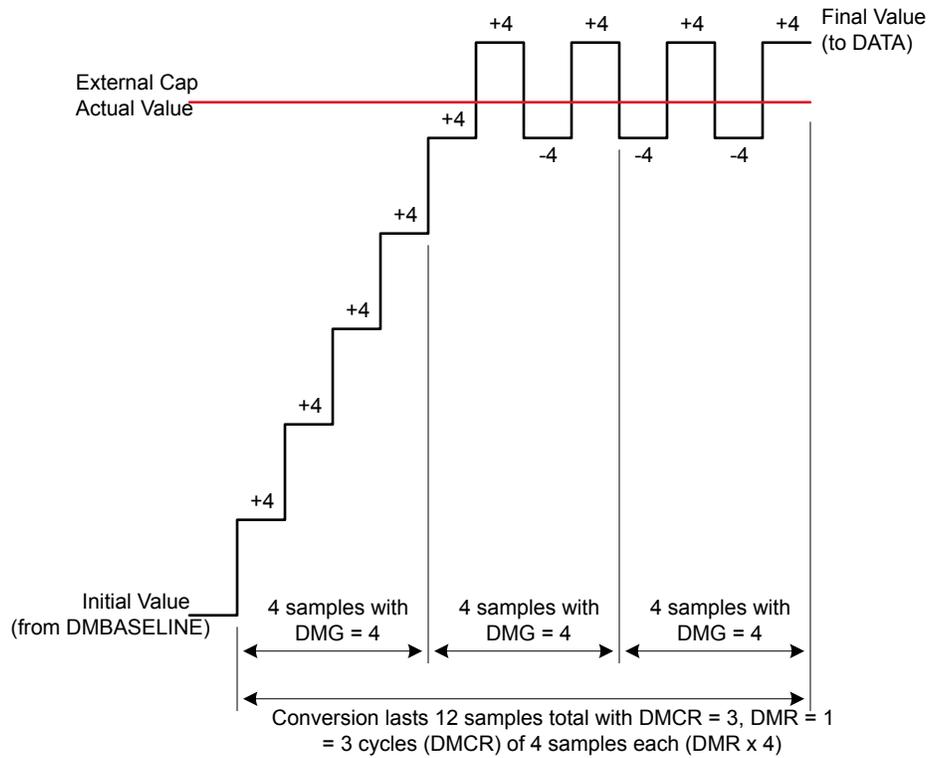
Delta modulation conversions are performed when CTRL\_CONVSEL is set to DM. DMCFG\_DMCR sets the DM conversion resolution, and is selectable between 10, 12, 14, or 16 bits. The selected resolution does not have an impact on conversion timing.

A delta modulated conversion begins with a test against a provided initial value, known as the baseline. If the comparison is high (the external capacitor is larger than the initial value), the comparison value is increased by a specified amount (the delta). If the comparison is low, the comparison value is decreased by the delta. The cycle then repeats, testing against the new value. Each subsequent test brings the test value closer to the external capacitance value, until the desired number of tests have been performed and an output result is produced. The converter may be configured to use a fixed delta value, or to reduce the value by a factor of two at specific intervals.

The DM state machine is configured using different fields in the DMCFG register. The DMG field sets the initial delta step to be used, between 0 and 255 codes at the selected resolution (specified by DMCFG\_CRMODE). The DMCFG\_DMR field specifies how many tests in a row are to be performed using each delta step. The converter will perform (4 x DMCFG\_DMR) tests at each delta step for DMCFG\_DMR > 0. For DMCFG\_DMR = 0, the converter will perform 64 tests at each delta step. The number of tests performed at each delta step is referred to here as a "cycle". The DMCFG\_DMCR field specifies how many cycles the state machine will take to produce one conversion output. For DMCFG\_DMCR = 0, the number of cycles will be 16. If the DMCFG\_DMGRDIS bit is cleared to 0, the delta step will be halved after each cycle. If DMCFG\_DMGRDIS is set to 1, all cycles will use a fixed delta step value. Each test performed by the converter requires one CLK\_CSEN, and so a full DM conversion requires number\_of\_cycles x tests\_per\_cycle clocks of CLK\_CSEN. [Figure 35.2 Delta Modulation Conversion With Gain Reduction \(DMCFG\\_DMGRDIS = 0\)](#) on page 1179 and [Figure 35.3 Delta Modulation Conversion With Fixed Delta Step \(DMCFG\\_DMGRDIS = 1\)](#) on page 1180 show how delta modulation conversions are performed with and without gain reduction.



**Figure 35.2. Delta Modulation Conversion With Gain Reduction (DMCFG\_DMGRDIS = 0)**



**Figure 35.3. Delta Modulation Conversion With Fixed Delta Step (DMCFG\_DMGDIS = 1)**

The initial test value (baseline) for a DM conversion can be written to the DMBASELINE register prior to the start of the conversion. DMBASELINE contains two fields: BASELINEUP and BASELINEDN. Only the BASELINEUP field is used when chopping is disabled (CTRL\_CHOPEN = 0). If chopping is enabled, software must maintain a second baseline value for the ramp-down phase, and write it to BASELINEDN.

### 35.5 Input Configuration

CSEN channel inputs are routed through the on-chip APORT bus matrix. Each APORT bus is a shared resource among certain analog peripherals on the device. Some knowledge of how the CSEN block utilizes the APORT buses is necessary to avoid conflicts with other peripherals.

Each time the CSEN module connects to an external pin to take a conversion, it uses one or two of the shared APORT buses. By default, the CSEN module charges the external capacitor through one APORT connection on the CEXT line, and senses the voltage at the capacitor through a different APORT connection on the CEXT\_SENSE line. This eliminates any errors introduced by series impedance of the APORT buses, particularly if the external capacitance is large. To conserve on-chip resources, it is possible to both charge and sense through the CEXT line, by setting CTRL\_LOCALSENS to logic 1. When CTRL\_LOCALSENS is set to 1, the CEXT\_SENSE line is not needed and the corresponding bus may be used by other peripherals.

The CSEN module has four APORT buses connected to the CEXT signal and four APORT buses connected to the CEXT\_SENSE signal. The specific buses used for each pin selection depend on the channel, according to [Table 35.1 CSEN APORT Bus Connectivity on page 1181](#). For example, if APORT1XCH4 (APORT1 channel 4) is selected in SINGLECTRL\_SINGLESEL, the CEXT signal will be connected to the shared BUSAX, channel 4. If CTRL\_LOCALSENS is set to DISABLE, then the CEXT\_SENSE signal will be connected to APORT2YCH4, and use the shared bus BUSBY, channel 4.

The same connections apply to scan mode conversions and bonded conversions. For scan mode conversions, the connection through the bus is only made on one channel at a time, when that channel is being converted in the scan. For bonded connections, all selected channel connections are made simultaneously.

**Table 35.1. CSEN APORT Bus Connectivity**

| Selected CSEN Channel | CEXT Routing          | CEXT_SENSE Routing<br>(LOCALSENS = 0) |
|-----------------------|-----------------------|---------------------------------------|
| APORT1, Even Channel  | APORT1XCHn / BUSAXCHn | APORT2YCHn / BUSBYCHn                 |
| APORT1, Odd Channel   | APORT1YCHn / BUSAYCHn | APORT2XCHn / BUSBXCHn                 |
| APORT3, Even Channel  | APORT3XCHn / BUSCXCHn | APORT4YCHn / BUSDYCHn                 |
| APORT3, Odd Channel   | APORT3YCHn / BUSCYCHn | APORT4XCHn / BUSDXCHn                 |

When the CSEN module requests an APORT bus that is already in use by another peripheral, an APORT conflict will occur. The IF\_APORTCONFLICT interrupt flag will be set to 1 (generating an interrupt if enabled), and the APORTCONFLICT register will reflect the bus(es) where the conflict occurred. Careful channel planning for the system will avoid APORT conflicts in most systems.

Channel selection for the CSEN module depends on the selected conversion mode. More details on how to select specific input pins are found in [35.6 Conversion Modes](#).

### 35.6 Conversion Modes

The CSEN module supports several conversion modes:

- Single Channel - A conversion trigger starts conversions on a single channel. One output result is produced, then the converter will halt.
- Scan - A conversion trigger starts a scan sequence, which converts a specified number of channels independently and in sequence. One output result is produced per channel, then the converter will halt.
- Bonded Channel - A conversion trigger starts conversions on a bonded channel. A bonded channel is several input channels which are shorted together internally. One output result is produced, then the converter will halt.
- Continuous Single Channel - A conversion trigger starts continuous conversions on a single channel. The single channel conversion will re-trigger automatically after each output result and repeat until halted.
- Continuous Scan - A conversion trigger starts continuous channel scanning. The scan sequence will re-trigger automatically at the end of each scan and repeat until halted.
- Continuous Bonded Channel - A conversion trigger starts continuous conversions on a bonded channel. The bonded channel conversion will re-trigger automatically after each output result and repeat until halted.

The conversion mode is selected by the CTRL\_CM and CTRL\_MCEN fields. Refer to [35.6.1 Single Channel Conversions](#), [35.6.2 Scan Conversions](#), and [35.6.3 Bonded Channel Conversions](#) for specific information on configuring the CSEN module to the desired conversion mode.

### 35.6.1 Single Channel Conversions

CSEN is configured for single channel mode when CTRL\_MCEN = DISABLE and CTRL\_CM = SGL. For continuous single channel mode, CTRL\_MCEN = DISABLE and CTRL\_CM = CONTSGL.

In single channel mode, SINGLECTRL\_SINGLESEL specifies the input channel to be converted. Firmware may select any of the pins connected to the CEXT signal via the APORT. Refer to the Analog Port (APORT) Client Maps section in the product data sheet for mapping of the CEXT signal to specific pins.

When a single channel conversion is triggered, the CSEN block will use the configured conversion type (SAR or DM) to convert the capacitance seen at the selected input pin to a digital value one or more times. The hardware accumulator setting (CTRL\_ACU) determines how many times the input pin will be sampled and accumulated before an output word is produced. The IF\_CONV interrupt flag will be set to 1 by hardware when an output word is available in the DATA register.

**Note:** The auto-ground feature is typically not used in single channel conversion mode and should be disabled by software. However, if auto-grounding is enabled, it will ground the unused channels specified by the SCANINPUTSEL0/1 and SCANMASKSEL0/1 registers. See the channel selection discussion in [35.6.2 Scan Conversions](#) for more details.

### 35.6.2 Scan Conversions

CSEN is configured for scan mode when CTRL\_MCEN = DISABLE and CTRL\_CM = SCAN. For continuous scan mode, CTRL\_MCEN = DISABLE and CTRL\_CM = CONTSCAN.

In scan mode, the input channels to be converted during the scan are determined by the SCANINPUTSEL0/1 and SCANMASK0/1 registers. There are 64 available channels in the scanner logic. SCANINPUTSEL0/1 allow software to route CSEN scan channels to APORT-capable GPIO in groups of 8. SCANMASK0/1 specify which channels on those groups are to be included in the scan.

**Note:** It is possible to include the same group of 8 in more than one place in the scan sequence. However, for the majority of use cases, the SCANINPUTSEL0 register should be written to 0x07060504, and SCANINPUTSEL1 should be written to 0x0F0E0D0C. This will configure the CSEN scan channels to match their order in bonded mode.

Individual channels are included in the scan based on their bit positions in the mask registers, SCANMASK0 and SCANMASK1. A '1' in the corresponding bit of the mask register will include that channel in the scan. Refer to the Analog Port (APORT) Client Maps section in the product data sheet for mapping of the CEXT signal to specific pins.

When a scan conversion is triggered, the CSEN block will convert each of the selected channels in turn, starting at channel 0 and working up to channel 63. If a channel is not configured for scan in the SCANMASK0/1 register (i.e. the bit for that channel is '0'), it will be skipped.

An example of how the scan logic progresses through channels is shown in [Figure 35.4 Scan Mode Sequencing on page 1183](#). In this simple example, SCANMASK0 = 0x00000318 and SCANMASK1 = 0x00000006, which selects channels 3, 4, 8, 9, 33, and 34 in turn.

|           | SCANMASK Values | CSEN Input Channel | DATA Output Order |  |
|-----------|-----------------|--------------------|-------------------|--|
| SCANMASK0 | 0               | 0                  |                   |  |
|           | 1               | 0                  |                   |  |
|           | 2               | 0                  |                   |  |
|           | 3               | 1                  | 3                 |  |
|           | 4               | 1                  | 4                 |  |
|           | 5               | 0                  |                   |  |
|           | 6               | 0                  |                   |  |
|           | 7               | 0                  |                   |  |
|           | 8               | 1                  | 8                 |  |
|           | 9               | 1                  | 9                 |  |
|           | 10              | 0                  |                   |  |
|           | 11              | 0                  |                   |  |
|           | 12              | 0                  |                   |  |
|           | 13              | 0                  |                   |  |
| •         | •               | •                  |                   |  |
| •         | •               | •                  |                   |  |
| •         | •               | •                  |                   |  |
| 27        | 0               | 27                 |                   |  |
| 28        | 0               | 28                 |                   |  |
| 29        | 0               | 29                 |                   |  |
| 30        | 0               | 30                 |                   |  |
| 31        | 0               | 31                 |                   |  |
| SCANMASK1 | 0               | 32                 |                   |  |
|           | 1               | 33                 | Channel 33        |  |
|           | 2               | 34                 | Channel 34        |  |
|           | 3               | 0                  |                   |  |
|           | 4               | 0                  |                   |  |
|           | •               | •                  |                   |  |
|           | •               | •                  |                   |  |
|           | •               | •                  |                   |  |
|           | 27              | 0                  | 59                |  |
|           | 28              | 0                  | 60                |  |
|           | 29              | 0                  | 61                |  |
|           | 30              | 0                  | 62                |  |
|           | 31              | 0                  | 63                |  |

**Figure 35.4. Scan Mode Sequencing**

An auto-grounding feature is available for scan mode conversions. This feature forces hardware to ground all of the non-active CSEN channels selected by SCANMASK0/1, to reduce bleed-through from measurements on other CSEN channels. Auto-grounding is enabled by setting the CTRL\_AUTOGND bit to logic 1.

CSEN will use the configured conversion type (SAR or DM) to convert the capacitance seen at each of the selected input pins to a digital value one or more times. The hardware accumulator setting (CTRL\_ACU) determines how many times each input pin will be sampled and accumulated before an output word is produced. The IF\_CONV interrupt flag will be set to 1 by hardware when each output word is available in the DATA register, and the IF\_EOS interrupt flag will be set to 1 by hardware at the completion of a scan cycle.

The DMBASELINE register provides the starting point for DM conversions. This starting point will be different for each channel in the scan, and the DMBASELINE register should be updated accordingly. This is typically done via DMA.

**Note:** DMA or software must read the output words from the DATA register before completion of the next conversion. New conversions will over-write the DATA register contents.

### 35.6.3 Bonded Channel Conversions

CSEN is configured for bonded mode when CTRL\_MCEN = ENABLE and CTRL\_CM = SGL. For continuous bonded mode, CTRL\_MCEN = ENABLE and CTRL\_CM = CONTSGL.

Bonded channel conversions are intended primarily for wake-on-touch applications where minimal power consumption is necessary. Bonded channel conversions operate similar to single channel conversions, except that multiple channels are shorted together and converted as a single capacitance value.

In bonded mode, the channels to be bonded are based on their bit positions in the mask registers SCANMASK0 and SCANMASK1, according to a fixed location, as shown in [Figure 35.5 CSEN Input Configuration in Bonded Mode on page 1184](#). SCANMASK0 selects channels from APORT1 and SCANMASK1 selects channels from APORT3. Even-numbered channels are connected through the X bus, and odd-numbered channels are connected through the Y bus. Channels with a '1' in the corresponding position of SCANMASK0/1 will be shorted together during the conversion and converted as a single channel. Refer to the Analog Port (APORT) Client Maps section in the product data sheet for mapping of the CEXT signal to specific pins.

|                  | CSEN Input Channel | APORT Connection | Shared Bus Channel |                  | CSEN Input Channel | APORT Connection | Shared Bus Channel |   |
|------------------|--------------------|------------------|--------------------|------------------|--------------------|------------------|--------------------|---|
| <b>SCANMASK0</b> | 0                  | APORT1XCH0       | BUSAX channel 0    | <b>SCANMASK1</b> | 32                 | APORT3XCH0       | BUSCX channel 0    |   |
|                  | 1                  | APORT1YCH1       | BUSAY channel 1    |                  | 33                 | APORT3YCH1       | BUSCY channel 1    |   |
|                  | 2                  | APORT1XCH2       | BUSAX channel 2    |                  | 34                 | APORT3XCH2       | BUSCX channel 2    |   |
|                  | 3                  | APORT1YCH3       | BUSAY channel 3    |                  | 35                 | APORT3YCH3       | BUSCY channel 3    |   |
|                  | 4                  | APORT1XCH4       | BUSAX channel 4    |                  | 36                 | APORT3XCH4       | BUSCY channel 4    |   |
|                  | •                  | •                | •                  |                  | •                  | •                | •                  | • |
|                  | •                  | •                | •                  |                  | •                  | •                | •                  | • |
|                  | •                  | •                | •                  |                  | •                  | •                | •                  | • |
|                  | •                  | •                | •                  |                  | •                  | •                | •                  | • |
|                  | 27                 | APORT1YCH27      | BUSAY channel 27   |                  | 27                 | APORT3YCH27      | BUSCY channel 27   |   |
|                  | 28                 | APORT1XCH28      | BUSAX channel 28   |                  | 28                 | APORT3XCH28      | BUSCX channel 28   |   |
|                  | 29                 | APORT1YCH29      | BUSAY channel 29   |                  | 29                 | APORT3YCH29      | BUSCY channel 29   |   |
|                  | 30                 | APORT1XCH30      | BUSAX channel 30   |                  | 30                 | APORT3XCH30      | BUSCX channel 30   |   |
|                  | 31                 | APORT1YCH31      | BUSAY channel 31   |                  | 31                 | APORT3YCH31      | BUSCY channel 31   |   |

**Figure 35.5. CSEN Input Configuration in Bonded Mode**

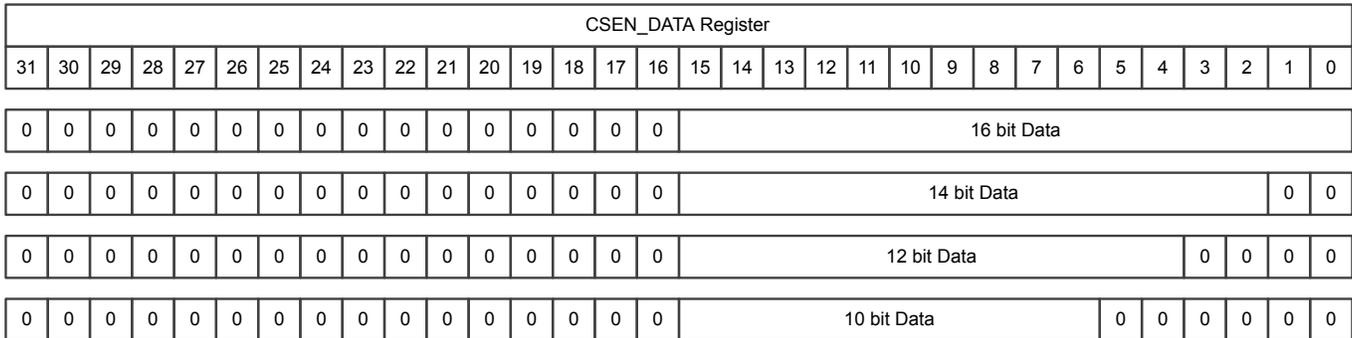
When a bonded conversion is triggered, the CSEN block will use the configured conversion type (SAR or DM) to convert the total capacitance seen at the selected input pins to a digital value one or more times. The hardware accumulator setting (CTRL\_ACU) determines how many times the input pins will be sampled and accumulated before an output word is produced. The IF\_CONV interrupt flag will be set to 1 by hardware when an output word is available in the DATA register.

**Note:** The auto-ground feature should not be used in bonded conversion mode. Software should clear CTRL\_AUTOGND to 0 when configuring CSEN for bonded conversions.

### 35.7 Output Data

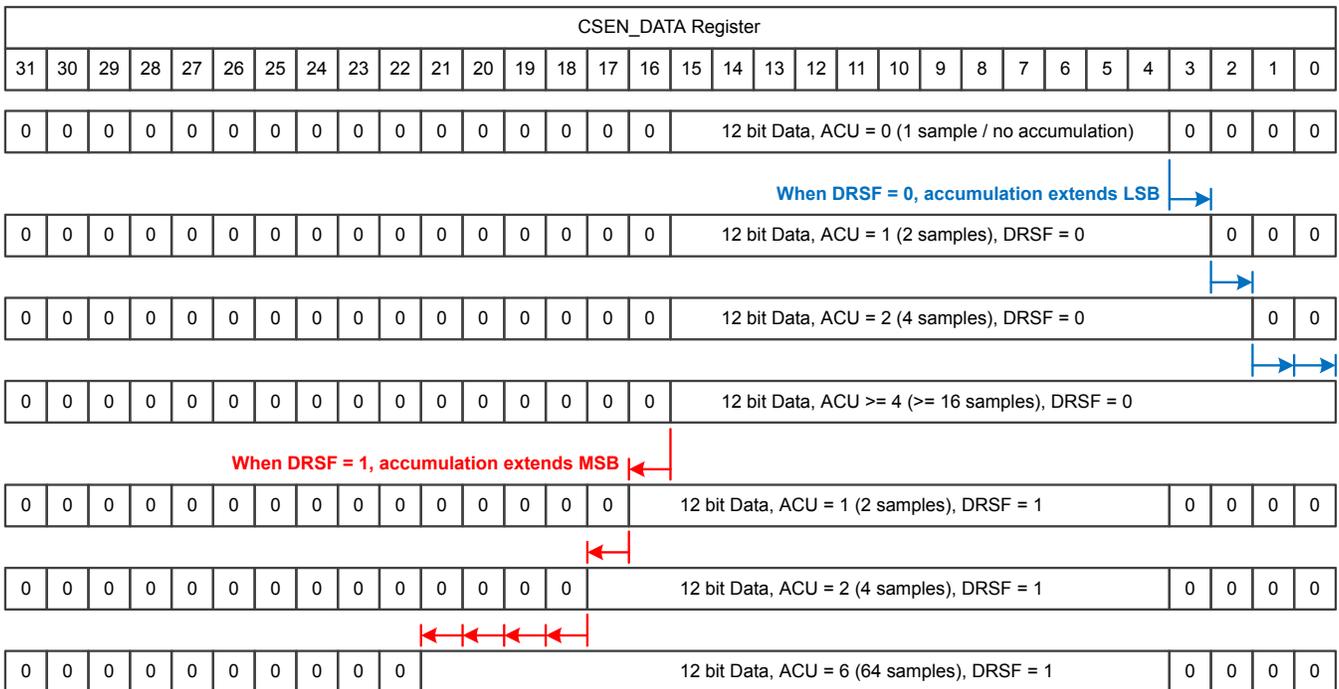
Output data from the CSEN module is posted to the DATA register. The data encoding can be affected by several configuration settings.

Figure 35.6 Data Encoding for Different Resolution Settings on page 1185 shows the effect that the resolution settings (CTRL\_SARCR for SAR conversions or DMCFG\_CRMODE for DM conversions) have on the output word. In this example, only one sample is accumulated. Regardless of the resolution setting, the MSB is always presented in bit position 15.



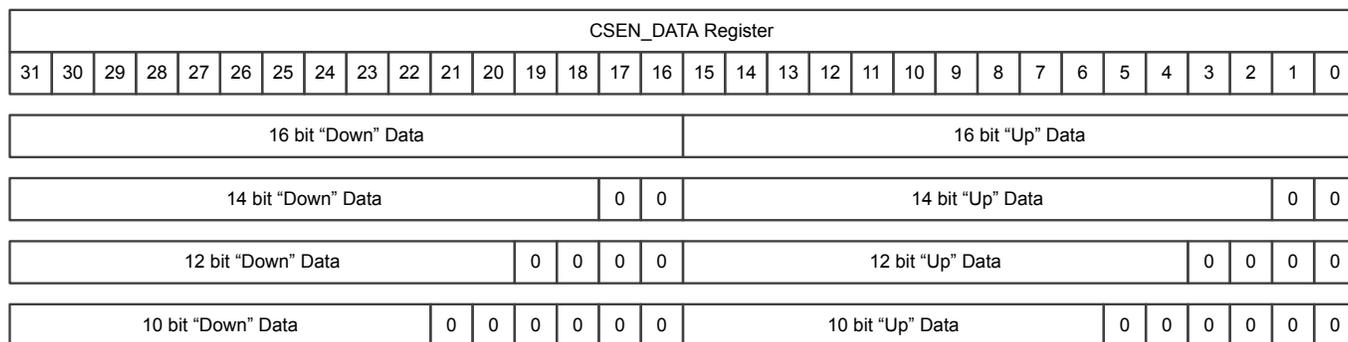
**Figure 35.6. Data Encoding for Different Resolution Settings**

A hardware accumulator allows the CSEN block to accumulate multiple samples on the same channel for each conversion data word produced, and automatically right-shift to normalize the data to 16 bits. This is effective as a simple noise filter. The CTRL\_ACU field sets the number of samples to be accumulated from 1, 2, 4, 8, 16, 32, or 64 samples. The right-shift operation can optionally be disabled by setting CTRL\_DRFSF to 1. Figure 35.7 Data Encoding for Different Accumulator Settings on page 1185 shows the effects of the accumulator, with and without right-shifting on the output data word. In this example, the sample resolution is fixed at 12 bits, but the same principles apply to any resolution setting.



**Figure 35.7. Data Encoding for Different Accumulator Settings**

When the conversion type is delta modulation (CTRL\_CONVSEL = DM) and chopping is enabled (CTRL\_CHOPEN = ENABLE), this is a special case for the output word. In this case, both the "up" and the "down" portions of the conversion must be stored. The DATA register will hold the "up" portion in the lower 16 bits and the "down" portion in the upper 16 bits as shown in Figure 35.8 Data Encoding for Delta Modulation With Chopping on page 1186.



**Figure 35.8. Data Encoding for Delta Modulation With Chopping**

### 35.8 Low Frequency Noise Filter (Chopping)

The CSEN module includes a low-frequency noise filter, which is implemented internally using a chopping mechanism. Chopping is enabled by setting CTRL\_CHOPEN to ENABLE. In a normal conversion cycle (CTRL\_CHOPEN = DISABLE), the charge timing is always performed on a positive (up) ramp. When chopping is enabled, the converter will alternate between using a positive (up) and negative (down) ramp for each sample. While the absolute capacitance value contributes the same amount for an up or a down conversion, any low-frequency offset artifacts due to supply changes will have opposite polarity. Averaging the results of an "up" and a "down" conversion taken back-to-back effectively eliminates the low-frequency offset differences.

When chopping is used with SAR type conversions, the accumulator performs the necessary averaging in hardware. The accumulator must be set to average at least two samples when chopping is enabled. Because the accumulator always works on multiples of two samples, an even number of "up" and "down" samples will be included in the average.

When chopping is used with DM type conversions, user software must maintain both an "up" and "down" portion of the baseline for the conversion separately. For this reason, the output word will contain both values when using DM conversions. In order to gain the benefits of chopping in DM mode, software should average the "up" and "down" results together.

### 35.9 Wake on Threshold and Exponential Moving Average

The CSEN module has the capability to operate in the energy-efficient EM2 or EM3 modes and autonomously wake the system when a predetermined threshold is crossed, either while doing single channel conversions or bonded channel conversions. This allows a system to monitor one or more input channels to implement low-energy "wait-for-touch" features. There are two different comparator threshold tests available for this purpose:

- Absolute - used to compare data outputs with "less than or equal" or "greater than" tests against a fixed value. This is useful for applications with short sleep durations, which simply want to wake quickly if a certain condition is met.
- Relative EMA - used to compare data outputs against a moving average window. This is extremely useful for applications with long-term sleep requirements. The relative comparison allows the CSEN module to adjust for slow changes in capacitance such as those due to environmental changes (temperature, supply) without waking the system.

The absolute test is used when CTRL\_CMPEN = ENABLE and CTRL\_EMACMP = DISABLE. In this mode, any output word written to the DATA register will be compared against the value in the CMPTHR register. The polarity of the comparison is configured with the CTRL\_CMPPOL field. Setting CTRL\_CMPPOL to GT means that the comparison will be true if DATA is greater than CMPTHR. Setting CTRL\_CMPPOL to LTE means that the comparison will be true if DATA is less than or equal to CMPTHR. On a true result, the IF\_CMP interrupt flag is set to 1, and any continuous conversion in progress will be halted.

The relative EMA test is used when CTRL\_EMACMP = ENABLE. In this mode, the exponential moving average (EMA) value is used to establish a low-noise average code reading. The EMA is a moving average that is re-calculated on every output data word from the converter, according to the following equation:

$$\text{EMA}[n] = \text{EMA}[n-1] - \text{EMA}[n-1]/N + \text{DATA}/N,$$

**Figure 35.9. CSEN Exponential Moving Average Calculation**

The EMA register stores the current EMA value. This register may be written by software to quickly establish a new baseline average. N in the equation above is the sample weighting of the EMA filter, and is controlled with the EMASAMPLE field. Lower values of EMASAMPLE mean less averaging, and quicker response time, while higher EMASAMPLE values will reject more noise at the expense of response time.

When relative EMA comparisons are enabled, every new sample is compared with a window around the EMA. The lower bound of this window is EMA - CMPTHR, and the upper bound of the window is EMA + CMPTHR. If the new sample written to DATA falls outside that window (lower than the lower bound or higher than the upper bound), the CMP interrupt flag is set to 1 and any continuous conversion in progress is halted. Using the EMA comparison, large jumps in the output data word will trip the comparator and wake the system, but gradual changes will not trigger false positives. [Figure 35.10 Wake on Threshold With Relative EMA on page 1188](#) shows an example of the EMA moving average filter and window.

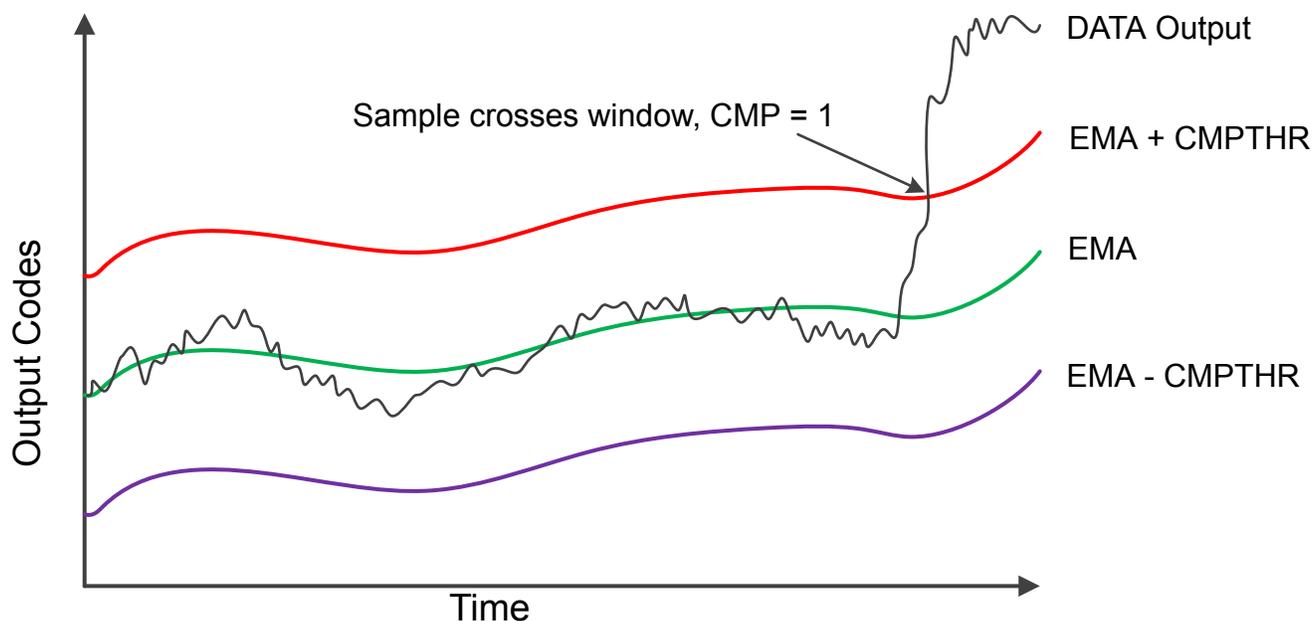


Figure 35.10. Wake on Threshold With Relative EMA

### 35.10 Analog Adjustments

The analog front-end of the CSEN module has some additional controls that may be useful in certain applications.

#### 35.10.1 Current Reference and Gain

The internal current source used for charging the reference capacitor can be adjusted using the ANACTRL\_IREFPROG field. This adjusts the ratio of the internal reference current source vs. the external drive current source, and thereby adjusts the effective gain of the converter. The lowest gain setting is when ANACTRL\_IREFPROG = 0, and the highest is with ANACTRL\_IREFPROG = 7. The difference between the lowest and highest setting is approximately 10x. High gain gives the best sensitivity and resolution for small capacitors, such as those typically implemented as touch-sensitive PCB features. Lower gain allows for larger capacitor values to be measured. It can also be useful to lower the gain when performing bonded channel conversions.

#### 35.10.2 Current Drive

The external capacitor is charged with a current-source DAC during conversions. The full scale output of the current DAC can be adjusted using the ANACTRL\_IDACIREFS field. When ANACTRL\_IDACIREFS is 0, the drive current is at its maximum setting. For ANACTRL\_IDACIREFS settings of 1-7, the drive current is reduced by a factor of ANACTRL\_IDACIREFS / 8. For most touch switch applications, the maximum (default) current drive (ANACTRL\_IDACIREFS = 0) should be used. Lower current drive may be useful when there is additional series impedance between the device pin and the capacitive sensor.

#### 35.10.3 Reset (Discharge) Timing

During a conversion, the external capacitance is charged and discharged multiple times. The amount of time used for the reset (discharge) phase is controlled by the ANACTRL\_TRSTPROG field. For most touch sensitive switch applications, the fastest (default) timing should be used. Extended reset timing may be useful in applications with additional series impedance between the device pin and the capacitive sensor.

### 35.11 DMA Interface

The CSEN module has DMA support for reads of the DATA register and writes to the DMBASELINE register. This enables the CSEN module to operate autonomously from software, either to free up software cycles during EM0 or to enable lower power operation in EM1 and EM2.

DMA transfers to and from the CSEN module are enabled by setting the CTRL\_DMAEN bit to 1. If the converter is used in SAR mode, only DMA reads (from the DATA register) are triggered. If the converter is used in delta modulation mode, both DMA reads from the DATA register and DMA writes to the DMBASELINE register are triggered.

Requests for a DATA register read occur at the end of a conversion cycle any time the CSEN module writes new output information to the DATA register. DMA may read half words (16 bits) or full words (32 bits) from the DATA register, depending on the specific CSEN configuration and the needs of the application. The CSEN module does not halt when the DMA read request is posted. It will immediately begin the next conversion. If the DMA read request is not serviced by the time the next conversion has completed, the IF\_DMAOF flag will be set to indicate an overflow event has occurred.

Requests for a data write to the DMBASELINE register occur only when using delta-modulation type conversions. The write request will be triggered at the start of a conversion, prior to the first sample comparison. The conversion will not begin until the DMA services this write request.

**Note:** If an absolute or EMA threshold interrupt is enabled when using the DMA, software must be aware that the converter will halt when the interrupt condition occurs. In this case it may be necessary to reconfigure portions of the DMA transfer before resuming conversions.

## 35.12 Register Map

The offset register address is relative to the registers base address.

| Offset | Name               | Type  | Description                        |
|--------|--------------------|-------|------------------------------------|
| 0x000  | CSEN_CTRL          | RW    | Control                            |
| 0x004  | CSEN_TIMCTRL       | RW    | Timing Control                     |
| 0x008  | CSEN_CMD           | W1    | Command                            |
| 0x00C  | CSEN_STATUS        | R     | Status                             |
| 0x010  | CSEN_PRSSEL        | RW    | PRS Select                         |
| 0x014  | CSEN_DATA          | RWH   | Output Data                        |
| 0x018  | CSEN_SCANMASK0     | RW    | Scan Channel Mask 0                |
| 0x01C  | CSEN_SCANINPUTSEL0 | RW    | Scan Input Selection 0             |
| 0x020  | CSEN_SCANMASK1     | RW    | Scan Channel Mask 1                |
| 0x024  | CSEN_SCANINPUTSEL1 | RW    | Scan Input Selection 1             |
| 0x028  | CSEN_APORTREQ      | R     | APOINT Request Status              |
| 0x02C  | CSEN_APORTCONFLICT | R     | APOINT Request Conflict            |
| 0x030  | CSEN_CMPTHR        | RW    | Comparator Threshold               |
| 0x034  | CSEN_EMA           | RWH   | Exponential Moving Average         |
| 0x038  | CSEN_EMACTRL       | RW    | Exponential Moving Average Control |
| 0x03C  | CSEN_SINGLECTRL    | RW    | Single Conversion Control          |
| 0x040  | CSEN_DMBASELINE    | RW    | Delta Modulation Baseline          |
| 0x044  | CSEN_DMCFG         | RW    | Delta Modulation Configuration     |
| 0x048  | CSEN_ANACTRL       | RW    | Analog Control                     |
| 0x054  | CSEN_IF            | R     | Interrupt Flag                     |
| 0x058  | CSEN_IFS           | W1    | Interrupt Flag Set                 |
| 0x05C  | CSEN_IFC           | (R)W1 | Interrupt Flag Clear               |
| 0x060  | CSEN_IEN           | RW    | Interrupt Enable                   |

### 35.13 Register Description

#### 35.13.1 CSEN\_CTRL - Control

| Offset        | Bit Position |    |    |            |           |            |          |      |         |        |         |       |      |       |     |      |    |     |     |    |    |    |       |     |   |   |    |     |   |        |    |    |  |
|---------------|--------------|----|----|------------|-----------|------------|----------|------|---------|--------|---------|-------|------|-------|-----|------|----|-----|-----|----|----|----|-------|-----|---|---|----|-----|---|--------|----|----|--|
| 0x000         | 31           | 30 | 29 | 28         | 27        | 26         | 25       | 24   | 23      | 22     | 21      | 20    | 19   | 18    | 17  | 16   | 15 | 14  | 13  | 12 | 11 | 10 | 9     | 8   | 7 | 6 | 5  | 4   | 3 | 2      | 1  | 0  |  |
| <b>Reset</b>  |              |    |    | 0          | 0         | 0          | 0        | 0    | 0       | 0      | 0       | 0     | 0    | 0     | 0x3 |      | 0  |     | 0x0 |    |    |    |       | 0x0 |   |   |    | 0x0 |   |        | 0  | 0  |  |
| <b>Access</b> |              |    |    | RW         | RW        | RW         | RW       | RW   | RW      | RW     | RW      | RW    | RW   | RW    | RW  | RW   | RW |     | RW  |    |    |    | RW    |     |   |   |    | RW  |   |        | RW | RW |  |
| <b>Name</b>   |              |    |    | CPACCURACY | LOCALSENS | WARMUPMODE | EMACMPEN | MXUC | AUTOGND | CHOPEN | CONVSEL | DMAEN | DRSF | CMPEN | STM | MCEN |    | ACU |     |    |    |    | SARCR |     |   |   | CM |     |   | CMPPOL | EN |    |  |

| Bit   | Name         | Reset  | Access | Description   |       |      |             |   |        |  |   |              |   |
|-------|--------------|--|--------|---|-------|------|-------------|---|--------|--|---|--------------|---|
| 31:29 | Reserved     | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i>  |        |   |       |      |             |   |        |  |   |              |   |
| 28    | CPACCURACY   | 0  | RW     | <b>Charge Pump Accuracy</b><br><br>This bit enables a more accurate reference for the APORT supply voltage. For the CSEN module, this bit has no effect on performance and should be written to 0.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>LO</td> <td>Request Low Accuracy Mode.</td> </tr> <tr> <td>1</td> <td>HI</td> <td>Request High Accuracy Mode.</td> </tr> </tbody> </table>   | Value | Mode | Description | 0 | LO     | Request Low Accuracy Mode.   | 1 | HI           | Request High Accuracy Mode.                             |
| Value | Mode         | Description  |        |   |       |      |             |   |        |  |   |              |   |
| 0     | LO           | Request Low Accuracy Mode.   |        |   |       |      |             |   |        |  |   |              |   |
| 1     | HI           | Request High Accuracy Mode.  |        |   |       |      |             |   |        |  |   |              |   |
| 27    | LOCALSENS    | 0  | RW     | <b>Local Sensing Enable</b><br><br>When cleared to 0, Kelvin sensing will be used. The external capacitor will be charged through the CEXT signal and the voltage at the pin will be monitored through a different APORT bus on the CEXT_CSEN signal. When this bit is set to 1, charging and sensing are both performed with the CEXT signal.  |       |      |             |   |        |  |   |              |   |
| 26    | WARMUPMODE   | 0  | RW     | <b>Select Warmup Mode for CSEN</b><br><br>Use this bit to keep the analog core enabled regardless of the conversion state.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>NORMAL</td> <td>CSEN analog core is shutdown after each operation completes. The next conversion trigger will incur a delay of (3 + WARMUPCNT) CSEN clock cycles before the conversion begins.</td> </tr> <tr> <td>1</td> <td>KEEPCSENWARM</td> <td>CSEN remains powered up, allowing continuous conversion</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | NORMAL | CSEN analog core is shutdown after each operation completes. The next conversion trigger will incur a delay of (3 + WARMUPCNT) CSEN clock cycles before the conversion begins. | 1 | KEEPCSENWARM | CSEN remains powered up, allowing continuous conversion |
| Value | Mode         | Description  |        |   |       |      |             |   |        |  |   |              |   |
| 0     | NORMAL       | CSEN analog core is shutdown after each operation completes. The next conversion trigger will incur a delay of (3 + WARMUPCNT) CSEN clock cycles before the conversion begins. |        |   |       |      |             |   |        |  |   |              |   |
| 1     | KEEPCSENWARM | CSEN remains powered up, allowing continuous conversion  |        |   |       |      |             |   |        |  |   |              |   |
| 25    | EMACMPEN     | 0  | RW     | <b>Greater and Less Than Comparison Using the Exponential Moving Average (EMA) is Enabled</b><br><br>The comparator flag (CMPIF) will be set if the accumulated result is greater than or equal to EMA+CMPTHR[8:0] or less than or equal to EMA-CMPTHR[8:0].  |       |      |             |   |        |  |   |              |   |
| 24    | MXUC         | 0  | RW     | <b>CSEN Mux Disconnect</b><br><br>CSEN Mux Disconnect.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>CONN</td> <td>The CSEN mux inputs are connected.</td> </tr> </tbody> </table>  | Value | Mode | Description | 0 | CONN   | The CSEN mux inputs are connected.   |   |              |   |
| Value | Mode         | Description  |        |   |       |      |             |   |        |  |   |              |   |
| 0     | CONN         | The CSEN mux inputs are connected.   |        |   |       |      |             |   |        |  |   |              |   |

| Bit | Name    | Reset   | Access | Description   |
|-----|---------|---------|--------|---|
|     | 1       | UNC     |        | The CSEN mux inputs unconnected.  |
| 23  | AUTOGND | 0       | RW     | <b>CSEN Automatic Ground Enable</b><br><br>Use this bit to enable automatic grounding of unused channels during scan conversions. For instance, if five channels are included in a scan, four channels will be grounded while one channel is being converted. This feature should be disabled when performing bonded conversions (MCE = 1). |
|     | Value   | Mode    |        | Description   |
|     | 0       | DISABLE |        | Auto grounding is disabled.   |
|     | 1       | ENABLE  |        | Auto grounding is enabled.  |
| 22  | CHOPEN  | 0       | RW     | <b>CSEN Chop Enable</b><br><br>Enables chopping for low-frequency noise filtering. When chopping is enabled, the ACU field must be set to a value greater than ACC1.  |
|     | Value   | Mode    |        | Description   |
|     | 0       | DISABLE |        | Chopping is disabled.   |
|     | 1       | ENABLE  |        | Chopping is enabled.  |
| 21  | CONVSEL | 0       | RW     | <b>CSEN Converter Select</b><br><br>This bit selects between SAR conversions and delta modulation conversions.  |
|     | Value   | Mode    |        | Description   |
|     | 0       | SAR     |        | The CSEN uses the SAR method for conversions.   |
|     | 1       | DM      |        | The CSEN uses the delta modulation method for conversions.  |
| 20  | DMAEN   | 0       | RW     | <b>CSEN DMA Enable Bit</b><br><br>Enables DMA transfers. DMA triggers are provided for DATA register reads of SAR and DM conversions. DMA triggers are also provided for DMBASELINE writes when DM conversions are performed.   |
|     | Value   | Mode    |        | Description   |
|     | 0       | DISABLE |        | CSEN DMA is disabled.   |
|     | 1       | ENABLE  |        | CSEN DMA is enabled.  |
| 19  | DRSF    | 0       | RW     | <b>CSEN Disable Right-Shift</b><br><br>Disables the hardware accumulator right-shift operation.   |
|     | Value   | Mode    |        | Description   |
|     | 0       | DISABLE |        | DATA[15:0] stores the last conversion (accumulated) result.   |
|     | 1       | ENABLE  |        | DATA[21:0] stores the last conversion (accumulated) result.   |
| 18  | CMPEN   | 0       | RW     | <b>CSEN Digital Comparator Enable</b><br><br>This bit enables the digital comparator which compares the accumulated CSEN conversions to the value stored in the CMPTHR register. When enabled, a comparator event will halt continuous conversions. Note that this bit is only effective when EMACMPEN = 0.                                 |
|     | Value   | Mode    |        | Description   |
|     | 0       | DISABLE |        | CSEN comparator is disabled.  |

| Bit   | Name            | Reset   | Access | Description  |
|-------|-----------------|---|--------|--|
|       | 1               | ENABLE  |        | CSEN comparator is enabled.  |
| 17:16 | STM             | 0x3   | RW     | <b>Start Trigger Select</b><br>Selects the start-of-conversion trigger to be used. Depending on the CSEN configuration, a single trigger may result in one or more conversions across multiple channels. |
|       | Value           | Mode  |        | Description  |
|       | 0               | PRS   |        | PRS Triggering. Conversions are triggered by the PRS channel selected in PRSSEL.   |
|       | 1               | TIMER   |        | Timer Triggering. Conversions are triggered by a local CSEN timer reload.  |
|       | 2               | START   |        | Software Triggering. Conversions are triggered by writing a 1 to the START field of the CMD register.  |
| 15    | MCEN            | 0   | RW     | <b>CSEN Multiple Channel Enable</b><br>This field enables bonded-channel conversions, where selected channels are shorted together. Use only with CM = SGL or CONTSGL.                                   |
|       | Value           | Mode  |        | Description  |
|       | 0               | DISABLE   |        | Multiple channel feature is disabled.  |
|       | 1               | ENABLE  |        | Selected channels are internally shorted together and the combined node is converted.  |
| 14:12 | ACU             | 0x0   | RW     | <b>CSEN Accumulator Mode Select</b><br>This field configures the hardware accumulator.   |
|       | Value           | Mode  |        | Description  |
|       | 0               | ACC1  |        | Accumulate 1 sample.   |
|       | 1               | ACC2  |        | Accumulate 2 sample.   |
|       | 2               | ACC4  |        | Accumulate 4 sample.   |
|       | 3               | ACC8  |        | Accumulate 8 sample.   |
|       | 4               | ACC16   |        | Accumulate 16 sample.  |
|       | 5               | ACC32   |        | Accumulate 32 sample.  |
|       | 6               | ACC64   |        | Accumulate 64 sample.  |
| 11:10 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 9:8   | SARCR           | 0x0   | RW     | <b>SAR Conversion Resolution.</b><br>This field selects the resolution of SAR type conversions.  |
|       | Value           | Mode  |        | Description  |
|       | 0               | CLK10   |        | Conversions last 10 internal CSEN clocks and are 10-bits in length.  |
|       | 1               | CLK12   |        | Conversions last 12 internal CSEN clocks and are 12-bits in length.  |
|       | 2               | CLK14   |        | Conversions last 14 internal CSEN clocks and are 14-bits in length.  |
|       | 3               | CLK16   |        | Conversions last 16 internal CSEN clocks and are 16-bits in length.  |

| Bit | Name            | Reset   | Access  | Description  |
|-----|-----------------|---|---|--|
| 7:6 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 5:4 | CM              | 0x0   | RW  | <b>CSEN Conversion Mode Select</b><br>This field is used to select a conversion method.  |
|     | Value           | Mode  | Description   |  |
|     | 0               | SGL   | Single Channel Mode: One conversion of a single channel (when MCE = 0) or set of bonded channels (when MCE = 1) per conversion trigger. |  |
|     | 1               | SCAN  | Scan Mode: Scans multiple selected channels once per conversion trigger.  |  |
|     | 2               | CONTSGL   | Continuous Single Channel: Continuous conversion of a single channel (when MCE = 0) or set of bonded channels (when MCE = 1).           |  |
|     | 3               | CONTSCAN  | Continuous Scan Mode: Continuously scans multiple selected channels.  |  |
| 3   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |
| 2   | CMPPOL          | 0   | RW  | <b>CSEN Digital Comparator Polarity Select</b><br>This bit determines the polarity of the digital comparator.  |
|     | Value           | Mode  | Description   |  |
|     | 0               | GT  | The digital comparator flag (CMPIF) is set if the conversion result is greater than the threshold.                                      |  |
|     | 1               | LTE   | The digital comparator flag (CMPIF) is set if the conversion result is less than or equal to the threshold.                             |  |
| 1   | EN              | 0   | RW  | <b>CSEN Enable</b><br>This bit enables the CSEN module. The CSEN module can be configured while disabled and then enabled when conversions are required. Clearing this bit to 0 will cancel any conversions in progress, but does not reset the configuration. |
|     | Value           | Mode  | Description   |  |
|     | 0               | DISABLE   | CSEN disabled.  |  |
|     | 1               | ENABLE  | CSEN enabled and ready to convert. Must be done before the start trigger.   |  |
| 0   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |  |

## 35.13.2 CSEN\_TIMCTRL - Timing Control

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |           |    |    |    |    |    |    |   |   |   |   |       |   |   |   |   |   |  |         |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------|----|----|----|----|----|----|---|---|---|---|-------|---|---|---|---|---|--|---------|
| 0x004         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16        | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5     | 4 | 3 | 2 | 1 | 0 |  |         |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0       |    |    |    |    |    |    |   |   |   |   | 0x00  |   |   |   |   |   |  | 0x0     |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW        |    |    |    |    |    |    |   |   |   |   | RW    |   |   |   |   |   |  | RW      |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    | WARMUPCNT |    |    |    |    |    |    |   |   |   |   | PCTOP |   |   |   |   |   |  | PCPRESC |

| Bit   | Name            | Reset   | Access  | Description   |
|-------|-----------------|---|---|---|
| 31:18 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |
| 17:16 | WARMUPCNT       | 0x0   | RW  | <b>Warmup Period Counter</b><br>Configures the warmup time for the converter when WARMUPMODE = NORMAL. The CSEN warmup time is defined as WARMUPCNT+3 CSEN clocks.  |
| 15:8  | PCTOP           | 0x00  | RW  | <b>Period Counter Top Value</b><br>This field contains the reload value for the period counter. If CTRL_STM = TIMER, the counter counts down and a start trigger is generated when the counter reaches zero. The counter is automatically reloaded from this field. |
| 7:3   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |   |   |
| 2:0   | PCPRESC         | 0x0   | RW  | <b>Period Counter Prescaler</b><br>This field sets the pre-scaler for local CSEN timer clock.   |
|       | Value           | Mode  | Description   |   |
|       | 0               | DIV1  | The period counter clock frequency is $\text{LFBCLK}_{\text{CSEN}}/1$   |   |
|       | 1               | DIV2  | The period counter clock frequency is $\text{LFBCLK}_{\text{CSEN}}/2$   |   |
|       | 2               | DIV4  | The period counter clock frequency is $\text{LFBCLK}_{\text{CSEN}}/4$   |   |
|       | 3               | DIV8  | The period counter clock frequency is $\text{LFBCLK}_{\text{CSEN}}/8$   |   |
|       | 4               | DIV16   | The period counter clock frequency is $\text{LFBCLK}_{\text{CSEN}}/16$  |   |
|       | 5               | DIV32   | The period counter clock frequency is $\text{LFBCLK}_{\text{CSEN}}/32$  |   |
|       | 6               | DIV64   | The period counter clock frequency is $\text{LFBCLK}_{\text{CSEN}}/64$  |   |
|       | 7               | DIV128  | The period counter clock frequency is $\text{LFBCLK}_{\text{CSEN}}/128$ |   |

## 35.13.3 CSEN\_CMD - Command

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------|
| 0x008         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0     |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0     |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | W1    |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | START |

| Bit  | Name     | Reset  | Access | Description  |
|------|----------|--|--------|--|
| 31:1 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |  |
| 0    | START    | 0  | W1     | <b>Start Software-Triggered Conversions</b><br>When CTRL_STM = START, writing a 1 to this bit will trigger CSEN conversions. |

## 35.13.4 CSEN\_STATUS - Status

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |          |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|----------|
| 0x00C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0        |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | 0        |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | R        |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | CSENBUSY |

| Bit  | Name     | Reset  | Access   | Description   |
|------|----------|--|--|---|
| 31:1 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |  |   |
| 0    | CSENBUSY | 0  | R  | <b>Busy Flag</b><br>This bit is set to 1 when a conversion is currently taking place. |
|      | Value    | Mode   | Description  |   |
|      | 0        | IDLE   | Conversion is complete or a conversion is not currently in progress. |   |
|      | 1        | BUSY   | Conversion is in progress.   |   |

### 35.13.5 CSEN\_PRSEL - PRS Select

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |       |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|-------|---|---|---|---|---|
| 0x010         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5     | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | 0x0   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | RW    |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | PRSEL |   |   |   |   |   |

| Bit  | Name     | Reset   | Access | Description |
|------|----------|---|--------|-------------|
| 31:4 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |             |

3:0 PRSEL 0x0 RW **PRS Channel Select**  
 Selects the PRS channel to be used as a conversion trigger when CTRL\_STM = PRS.

| Value | Mode    | Description                                  |
|-------|---------|--|
| 0     | PRSCH0  | PRS Channel 0 selected as the start trigger  |
| 1     | PRSCH1  | PRS Channel 1 selected as the start trigger  |
| 2     | PRSCH2  | PRS Channel 2 selected as the start trigger  |
| 3     | PRSCH3  | PRS Channel 3 selected as the start trigger  |
| 4     | PRSCH4  | PRS Channel 4 selected as the start trigger  |
| 5     | PRSCH5  | PRS Channel 5 selected as the start trigger  |
| 6     | PRSCH6  | PRS Channel 6 selected as the start trigger  |
| 7     | PRSCH7  | PRS Channel 7 selected as the start trigger  |
| 8     | PRSCH8  | PRS Channel 8 selected as the start trigger  |
| 9     | PRSCH9  | PRS Channel 9 selected as the start trigger  |
| 10    | PRSCH10 | PRS Channel 10 selected as the start trigger |
| 11    | PRSCH11 | PRS Channel 11 selected as the start trigger |

### 35.13.6 CSEN\_DATA - Output Data

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x014         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | DATA       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name | Reset      | Access | Description        |
|---|------|------------|--------|--------------------|
| 31:0  | DATA | 0x00000000 | RWH    | <b>Output Data</b> |
| <p>Output data words are written to the DATA register when sampling and accumulation for a channel have completed. Data encoding depends on the resolution, accumulator settings, and conversion type. See the chapter text for more details on data output encoding.</p> |      |            |        |                    |

### 35.13.7 CSEN\_SCANMASK0 - Scan Channel Mask 0

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x018         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x00000000  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | SCANINPUTEN |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name        | Reset      | Access | Description              |
|--|-------------|------------|--------|--------------------------|
| 31:0   | SCANINPUTEN | 0x00000000 | RW     | <b>Scan Channel Mask</b> |
| <p>Scan channel mask for CSEN channels CSEN_INPUT0 through CSEN_INPUT31. For scan mode conversions, a '1' in any bit position will include the channel specified by SCANINPUTSEL0 in a scan. For bonded channel conversions, a '1' in any bit position includes the corresponding channel from APORT1 / BUSA in the bonded conversion. If AUTOGND = ENABLE the scan mask also determines the pins that will be grounded when inactive, for both scan and single channel conversions.</p> |             |            |        |                          |

### 35.13.8 CSEN\_SCANINPUTSEL0 - Scan Input Selection 0

| Offset        | Bit Position |    |    |    |                |    |    |    |    |    |    |    |                |    |    |    |    |    |    |    |               |    |   |   |   |   |   |   |              |   |   |   |
|---------------|--------------|----|----|----|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|---------------|----|---|---|---|---|---|---|--------------|---|---|---|
| 0x01C         | 31           | 30 | 29 | 28 | 27             | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19             | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11            | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3            | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    | 0x0            |    |    |    |    |    |    |    | 0x0            |    |    |    |    |    |    |    | 0x0           |    |   |   |   |   |   |   | 0x0          |   |   |   |
| <b>Access</b> |              |    |    |    | RW             |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    | RW            |    |   |   |   |   |   |   | RW           |   |   |   |
| <b>Name</b>   |              |    |    |    | INPUT24TO31SEL |    |    |    |    |    |    |    | INPUT16TO23SEL |    |    |    |    |    |    |    | INPUT8TO15SEL |    |   |   |   |   |   |   | INPUT0TO7SEL |   |   |   |

| Bit   | Name            | Reset   | Access   | Description   |
|-------|-----------------|---|--|---|
| 31:28 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |   |
| 27:24 | INPUT24TO31SEL  | 0x0   | RW   | <b>CSEN_INPUT24-31 Select</b><br>Channels chosen for CSEN_INPUT24-CSEN_INPUT31 as referred in SCANMASK0 |
|       | Mode            | Value   | Description  |   |
|       | APORT1CH0TO7    | 4   | Select APORT1 CH0-CH7 as CSEN_INPUT24-CSEN_INPUT31   |   |
|       | APORT1CH8TO15   | 5   | Select APORT1 CH8-CH15 as CSEN_INPUT24-CSEN_INPUT31  |   |
|       | APORT1CH16TO23  | 6   | Select APORT1 CH16-CH23 as CSEN_INPUT24-CSEN_INPUT31 |   |
|       | APORT1CH24TO31  | 7   | Select APORT1 CH24-CH31 as CSEN_INPUT24-CSEN_INPUT31 |   |
|       | APORT3CH0TO7    | 12  | Select APORT3 CH0-CH7 as CSEN_INPUT24-CSEN_INPUT31   |   |
|       | APORT3CH8TO15   | 13  | Select APORT3 CH8-CH15 as CSEN_INPUT24-CSEN_INPUT31  |   |
|       | APORT3CH16TO23  | 14  | Select APORT3 CH16-CH23 as CSEN_INPUT24-CSEN_INPUT31 |   |
|       | APORT3CH24TO31  | 15  | Select APORT3 CH24-CH31 as CSEN_INPUT24-CSEN_INPUT31 |   |
| 23:20 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |   |
| 19:16 | INPUT16TO23SEL  | 0x0   | RW   | <b>CSEN_INPUT16-23 Select</b><br>Channels chosen for CSEN_INPUT16-CSEN_INPUT23 as referred in SCANMASK0 |
|       | Mode            | Value   | Description  |   |
|       | APORT1CH0TO7    | 4   | Select APORT1 CH0-CH7 as CSEN_INPUT16-CSEN_INPUT23   |   |
|       | APORT1CH8TO15   | 5   | Select APORT1 CH8-CH15 as CSEN_INPUT16-CSEN_INPUT23  |   |
|       | APORT1CH16TO23  | 6   | Select APORT1 CH16-CH23 as CSEN_INPUT16-CSEN_INPUT23 |   |
|       | APORT1CH24TO31  | 7   | Select APORT1 CH24-CH31 as CSEN_INPUT16-CSEN_INPUT23 |   |
|       | APORT3CH0TO7    | 12  | Select APORT3 CH0-CH7 as CSEN_INPUT16-CSEN_INPUT23   |   |
|       | APORT3CH8TO15   | 13  | Select APORT3 CH8-CH15 as CSEN_INPUT16-CSEN_INPUT23  |   |
|       | APORT3CH16TO23  | 14  | Select APORT3 CH16-CH23 as CSEN_INPUT16-CSEN_INPUT23 |   |
|       | APORT3CH24TO31  | 15  | Select APORT3 CH24-CH31 as CSEN_INPUT16-CSEN_INPUT23 |   |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 15:12 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 11:8  | INPUT8TO15SEL   | 0x0   | RW     | <b>CSEN_INPUT8-15 Select</b><br>Channels chosen for CSEN_INPUT8-CSEN_INPUT15 as referred in SCANMASK0 |
|       | Mode            | Value   |        | Description   |
|       | APORT1CH0TO7    | 4   |        | Select APORT1 CH0-CH7 as CSEN_INPUT8-CSEN_INPUT15   |
|       | APORT1CH8TO15   | 5   |        | Select APORT1 CH8-CH15 as CSEN_INPUT8-CSEN_INPUT15  |
|       | APORT1CH16TO23  | 6   |        | Select APORT1 CH16-CH23 as CSEN_INPUT8-CSEN_INPUT15   |
|       | APORT1CH24TO31  | 7   |        | Select APORT1 CH24-CH31 as CSEN_INPUT8-CSEN_INPUT15   |
|       | APORT3CH0TO7    | 12  |        | Select APORT3 CH0-CH7 as CSEN_INPUT8-CSEN_INPUT15   |
|       | APORT3CH8TO15   | 13  |        | Select APORT3 CH8-CH15 as CSEN_INPUT8-CSEN_INPUT15  |
|       | APORT3CH16TO23  | 14  |        | Select APORT3 CH16-CH23 as CSEN_INPUT8-CSEN_INPUT15   |
|       | APORT3CH24TO31  | 15  |        | Select APORT3 CH24-CH31 as CSEN_INPUT8-CSEN_INPUT15   |
| 7:4   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 3:0   | INPUT0TO7SEL    | 0x0   | RW     | <b>CSEN_INPUT0-7 Select</b><br>Channels chosen for CSEN_INPUT7-CSEN_INPUT0 as referred in SCANMASK0   |
|       | Mode            | Value   |        | Description   |
|       | APORT1CH0TO7    | 4   |        | Select APORT1 CH0-CH7 as CSEN_INPUT0-CSEN_INPUT7  |
|       | APORT1CH8TO15   | 5   |        | Select APORT1 CH8-CH15 as CSEN_INPUT0-CSEN_INPUT7   |
|       | APORT1CH16TO23  | 6   |        | Select APORT1 CH16-CH23 as CSEN_INPUT0-CSEN_INPUT7  |
|       | APORT1CH24TO31  | 7   |        | Select APORT1 CH24-CH31 as CSEN_INPUT0-CSEN_INPUT7  |
|       | APORT3CH0TO7    | 12  |        | Select APORT3 CH0-CH7 as CSEN_INPUT0-CSEN_INPUT7  |
|       | APORT3CH8TO15   | 13  |        | Select APORT3 CH8-CH15 as CSEN_INPUT0-CSEN_INPUT7   |
|       | APORT3CH16TO23  | 14  |        | Select APORT3 CH16-CH23 as CSEN_INPUT0-CSEN_INPUT7  |
|       | APORT3CH24TO31  | 15  |        | Select APORT3 CH24-CH31 as CSEN_INPUT0-CSEN_INPUT7  |

35.13.9 CSEN\_SCANMASK1 - Scan Channel Mask 1

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x020         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0x00000000   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | SCANINPUTEN  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit  | Name        | Reset      | Access | Description   |
|------|-------------|------------|--------|---|
| 31:0 | SCANINPUTEN | 0x00000000 | RW     | <b>Scan Channel Mask.</b><br><br>Scan channel mask for CSEN channels CSEN_INPUT32 through CSEN_INPUT63. For scan mode conversions, a '1' in any bit position will include the channel specified by SCANINPUTSEL1 in a scan. For bonded channel conversions, a '1' in any bit position includes the corresponding channel from APORT3 / BUSC in the bonded conversion. If AUTOGND = ENABLE the scan mask also determines the pins that will be grounded when inactive, for both scan and single channel conversions. |

### 35.13.10 CSEN\_SCANINPUTSEL1 - Scan Input Selection 1

| Offset        | Bit Position |    |    |    |                |    |    |    |    |    |    |    |                |    |    |    |    |    |    |    |                |    |   |   |   |   |   |   |                |   |   |   |
|---------------|--------------|----|----|----|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|----------------|----|---|---|---|---|---|---|----------------|---|---|---|
| 0x024         | 31           | 30 | 29 | 28 | 27             | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19             | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11             | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3              | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    | 0x0            |    |    |    |    |    |    |    | 0x0            |    |    |    |    |    |    |    | 0x0            |    |   |   |   |   |   |   | 0x0            |   |   |   |
| <b>Access</b> |              |    |    |    | RW             |    |    |    |    |    |    |    | RW             |    |    |    |    |    |    |    | RW             |    |   |   |   |   |   |   | RW             |   |   |   |
| <b>Name</b>   |              |    |    |    | INPUT56TO63SEL |    |    |    |    |    |    |    | INPUT48TO55SEL |    |    |    |    |    |    |    | INPUT40TO47SEL |    |   |   |   |   |   |   | INPUT32TO39SEL |   |   |   |

| Bit   | Name            | Reset   | Access   | Description   |
|-------|-----------------|---|--|---|
| 31:28 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |   |
| 27:24 | INPUT56TO63SEL  | 0x0   | RW   | <b>CSEN_INPUT56-63 Select</b><br>Channels chosen for CSEN_INPUT56-CSEN_INPUT63 as referred in SCANMASK1 |
|       | Mode            | Value   | Description  |   |
|       | APORT1CH0TO7    | 4   | Select APORT1 CH0-CH7 as CSEN_INPUT56-CSEN_INPUT63   |   |
|       | APORT1CH8TO15   | 5   | Select APORT1 CH8-CH15 as CSEN_INPUT56-CSEN_INPUT63  |   |
|       | APORT1CH16TO23  | 6   | Select APORT1 CH16-CH23 as CSEN_INPUT56-CSEN_INPUT63 |   |
|       | APORT1CH24TO31  | 7   | Select APORT1 CH24-CH31 as CSEN_INPUT56-CSEN_INPUT63 |   |
|       | APORT3CH0TO7    | 12  | Select APORT3 CH0-CH7 as CSEN_INPUT56-CSEN_INPUT63   |   |
|       | APORT3CH8TO15   | 13  | Select APORT3 CH8-CH15 as CSEN_INPUT56-CSEN_INPUT63  |   |
|       | APORT3CH16TO23  | 14  | Select APORT3 CH16-CH23 as CSEN_INPUT56-CSEN_INPUT63 |   |
|       | APORT3CH24TO31  | 15  | Select APORT3 CH24-CH31 as CSEN_INPUT56-CSEN_INPUT63 |   |
| 23:20 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |   |
| 19:16 | INPUT48TO55SEL  | 0x0   | RW   | <b>CSEN_INPUT48-55 Select</b><br>Channels chosen for CSEN_INPUT48-CSEN_INPUT55 as referred in SCANMASK1 |
|       | Mode            | Value   | Description  |   |
|       | APORT1CH0TO7    | 4   | Select APORT1 CH0-CH7 as CSEN_INPUT48-CSEN_INPUT55   |   |
|       | APORT1CH8TO15   | 5   | Select APORT1 CH8-CH15 as CSEN_INPUT48-CSEN_INPUT55  |   |
|       | APORT1CH16TO23  | 6   | Select APORT1 CH16-CH23 as CSEN_INPUT48-CSEN_INPUT55 |   |
|       | APORT1CH24TO31  | 7   | Select APORT1 CH24-CH31 as CSEN_INPUT48-CSEN_INPUT55 |   |
|       | APORT3CH0TO7    | 12  | Select APORT3 CH0-CH7 as CSEN_INPUT48-CSEN_INPUT55   |   |
|       | APORT3CH8TO15   | 13  | Select APORT3 CH8-CH15 as CSEN_INPUT48-CSEN_INPUT55  |   |
|       | APORT3CH16TO23  | 14  | Select APORT3 CH16-CH23 as CSEN_INPUT48-CSEN_INPUT55 |   |
|       | APORT3CH24TO31  | 15  | Select APORT3 CH24-CH31 as CSEN_INPUT48-CSEN_INPUT55 |   |

| Bit   | Name            | Reset   | Access   | Description   |
|-------|-----------------|---|--|---|
| 15:12 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |   |
| 11:8  | INPUT40TO47SEL  | 0x0   | RW   | <b>CSEN_INPUT40-47 Select</b><br>Channels chosen for CSEN_INPUT40-CSEN_INPUT47 as referred in SCANMASK1 |
|       | Mode            | Value   | Description  |   |
|       | APORT1CH0TO7    | 4   | Select APORT1 CH0-CH7 as CSEN_INPUT40-CSEN_INPUT47   |   |
|       | APORT1CH8TO15   | 5   | Select APORT1 CH8-CH15 as CSEN_INPUT40-CSEN_INPUT47  |   |
|       | APORT1CH16TO23  | 6   | Select APORT1 CH16-CH23 as CSEN_INPUT40-CSEN_INPUT47 |   |
|       | APORT1CH24TO31  | 7   | Select APORT1 CH24-CH31 as CSEN_INPUT40-CSEN_INPUT47 |   |
|       | APORT3CH0TO7    | 12  | Select APORT3 CH0-CH7 as CSEN_INPUT40-CSEN_INPUT47   |   |
|       | APORT3CH8TO15   | 13  | Select APORT3 CH8-CH15 as CSEN_INPUT40-CSEN_INPUT47  |   |
|       | APORT3CH16TO23  | 14  | Select APORT3 CH16-CH23 as CSEN_INPUT40-CSEN_INPUT47 |   |
|       | APORT3CH24TO31  | 15  | Select APORT3 CH24-CH31 as CSEN_INPUT40-CSEN_INPUT47 |   |
| 7:4   | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |  |   |
| 3:0   | INPUT32TO39SEL  | 0x0   | RW   | <b>CSEN_INPUT32-39 Select</b><br>Channels chosen for CSEN_INPUT32-CSEN_INPUT39 as referred in SCANMASK1 |
|       | Mode            | Value   | Description  |   |
|       | APORT1CH0TO7    | 4   | Select APORT1 CH0-CH7 as CSEN_INPUT32-CSEN_INPUT39   |   |
|       | APORT1CH8TO15   | 5   | Select APORT1 CH8-CH15 as CSEN_INPUT32-CSEN_INPUT39  |   |
|       | APORT1CH16TO23  | 6   | Select APORT1 CH16-CH23 as CSEN_INPUT32-CSEN_INPUT39 |   |
|       | APORT1CH24TO31  | 7   | Select APORT1 CH24-CH31 as CSEN_INPUT32-CSEN_INPUT39 |   |
|       | APORT3CH0TO7    | 12  | Select APORT3 CH0-CH7 as CSEN_INPUT32-CSEN_INPUT39   |   |
|       | APORT3CH8TO15   | 13  | Select APORT3 CH8-CH15 as CSEN_INPUT32-CSEN_INPUT39  |   |
|       | APORT3CH16TO23  | 14  | Select APORT3 CH16-CH23 as CSEN_INPUT32-CSEN_INPUT39 |   |
|       | APORT3CH24TO31  | 15  | Select APORT3 CH24-CH31 as CSEN_INPUT32-CSEN_INPUT39 |   |

## 35.13.11 CSEN\_APORTREQ - APORT Request Status

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |            |            |            |            |            |            |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|------------|------------|------------|------------|------------|------------|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x028         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11         | 10         | 9          | 8          | 7          | 6          | 5          | 4          | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R          | R          | R          | R          | R          | R          | R          | R          | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | APORT4YREQ | APORT4XREQ | APORT3YREQ | APORT3XREQ | APORT2YREQ | APORT2XREQ | APORT1YREQ | APORT1XREQ |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name       | Reset   | Access | Description  |
|-------|------------|---|--------|--|
| 31:10 | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 9     | APORT4YREQ | 0   | R      | <b>1 If the Bus Connected to APORT4Y is Requested</b><br>Reports if the bus connected to APORT4Y is being requested from the APORT |
| 8     | APORT4XREQ | 0   | R      | <b>1 If the Bus Connected to APORT4X is Requested</b><br>Reports if the bus connected to APORT4X is being requested from the APORT |
| 7     | APORT3YREQ | 0   | R      | <b>1 If the Bus Connected to APORT3Y is Requested</b><br>Reports if the bus connected to APORT3Y is being requested from the APORT |
| 6     | APORT3XREQ | 0   | R      | <b>1 If the Bus Connected to APORT3X is Requested</b><br>Reports if the bus connected to APORT3X is being requested from the APORT |
| 5     | APORT2YREQ | 0   | R      | <b>1 If the Bus Connected to APORT2Y is Requested</b><br>Reports if the bus connected to APORT2Y is being requested from the APORT |
| 4     | APORT2XREQ | 0   | R      | <b>1 If the Bus Connected to APORT2X is Requested</b><br>Reports if the bus connected to APORT2X is being requested from the APORT |
| 3     | APORT1YREQ | 0   | R      | <b>1 If the Bus Connected to APORT1X is Requested</b><br>Reports if the bus connected to APORT1X is being requested from the APORT |
| 2     | APORT1XREQ | 0   | R      | <b>1 If the Bus Connected to APORT2X is Requested</b><br>Reports if the bus connected to APORT1X is being requested from the APORT |
| 1:0   | Reserved   | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |

### 35.13.12 CSEN\_APORTCONFLICT - APORT Request Conflict

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                 |                 |                 |                 |                 |                 |                 |                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x02C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9               | 8               | 7               | 6               | 5               | 4               | 3               | 2               | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R               | R               | R               | R               | R               | R               | R               | R               | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | APORT4YCONFLICT | APORT4XCONFLICT | APORT3YCONFLICT | APORT3XCONFLICT | APORT2YCONFLICT | APORT2XCONFLICT | APORT1YCONFLICT | APORT1XCONFLICT |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name            | Reset   | Access | Description   |
|-------|-----------------|---|--------|---|
| 31:10 | Reserved        | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 9     | APORT4YCONFLICT | 0   | R      | <b>1 If the Bus Connected to APORT4Y is in Conflict With Another Peripheral</b><br><br>Reports if the bus connected to APORT4Y is is also being requested by another peripheral |
| 8     | APORT4XCONFLICT | 0   | R      | <b>1 If the Bus Connected to APORT4X is in Conflict With Another Peripheral</b><br><br>Reports if the bus connected to APORT4X is is also being requested by another peripheral |
| 7     | APORT3YCONFLICT | 0   | R      | <b>1 If the Bus Connected to APORT3Y is in Conflict With Another Peripheral</b><br><br>Reports if the bus connected to APORT3Y is is also being requested by another peripheral |
| 6     | APORT3XCONFLICT | 0   | R      | <b>1 If the Bus Connected to APORT3X is in Conflict With Another Peripheral</b><br><br>Reports if the bus connected to APORT3X is is also being requested by another peripheral |
| 5     | APORT2YCONFLICT | 0   | R      | <b>1 If the Bus Connected to APORT2Y is in Conflict With Another Peripheral</b><br><br>Reports if the bus connected to APORT2Y is is also being requested by another peripheral |
| 4     | APORT2XCONFLICT | 0   | R      | <b>1 If the Bus Connected to APORT2X is in Conflict With Another Peripheral</b><br><br>Reports if the bus connected to APORT2X is is also being requested by another peripheral |
| 3     | APORT1YCONFLICT | 0   | R      | <b>1 If the Bus Connected to APORT1Y is in Conflict With Another Peripheral</b><br><br>Reports if the bus connected to APORT1Y is is also being requested by another peripheral |
| 2     | APORT1XCONFLICT | 0   | R      | <b>1 If the Bus Connected to APORT1X is in Conflict With Another Peripheral</b><br><br>Reports if the bus connected to APORT1X is is also being requested by another peripheral |
| 1:0   | Reserved        | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |

### 35.13.13 CSEN\_CMPTHR - Comparator Threshold

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |        |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x030         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CMPTHR |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description |
|-------|----------|--|--------|-------------|
| 31:16 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |             |

| Bit  | Name   | Reset  | Access | Description   |
|------|--------|--------|--------|---|
| 15:0 | CMPTHR | 0x0000 | RW     | <b>Comparator Threshold.</b><br><br>When CMPEN is set to 1 and EMACMPEN is cleared to 0, a greater than or less than/equal (based on CMPPOL) comparison between the DATA register and CMPTHR value. If the desired condition is met, the CMPIF flag will be set. When EMACMPEN is set to 1, a comparison window is used instead. The DATA register will be compared against EMA +/- CMPTHR. The CMPIF flag is set any time the conversion result is above (EMA + CMPTHR) or below (EMA - CMPTHR). |

### 35.13.14 CSEN\_EMA - Exponential Moving Average

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x034         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x000000 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RWH      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | EMA      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name     | Reset  | Access | Description |
|-------|----------|--|--------|-------------|
| 31:22 | Reserved | To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a> |        |             |

| Bit  | Name | Reset    | Access | Description   |
|------|------|----------|--------|---|
| 21:0 | EMA  | 0x000000 | RWH    | <b>Calculated Exponential Moving Average</b><br><br>This register contains the current exponential moving average. The EMA is updated every time an accumulated sample is produced, according to the formula: $EMA[n] = EMA[n-1] - EMA[n-1]/N + DATA/N$ , where N is the EMA sample weight selected by EMASAMPLE. This register can be written to initialize the average. |

## 35.13.15 CSEN\_EMACTRL - Exponential Moving Average Control

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |           |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|-----------|---|---|---|---|---|
| 0x038         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5         | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | 0x0       |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | RW        |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | EMASAMPLE |   |   |   |   |   |

| Bit  | Name            | Reset   | Access | Description  |
|------|-----------------|---|--------|--|
| 31:3 | <i>Reserved</i> | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 2:0  | EMASAMPLE       | 0x0   | RW     | <b>EMA Sample Weight</b><br>This field specifies the sample weighting (N) for the exponential moving average filter. |
|      | Value           | Mode  |        | Description  |
|      | 0               | W1  |        | EMA weight (N) is 1.   |
|      | 1               | W2  |        | EMA weight (N) is 2.   |
|      | 2               | W4  |        | EMA weight (N) is 4.   |
|      | 3               | W8  |        | EMA weight (N) is 8.   |
|      | 4               | W16   |        | EMA weight (N) is 16.  |
|      | 5               | W32   |        | EMA weight (N) is 32.  |
|      | 6               | W64   |        | EMA weight (N) is 64.  |

### 35.13.16 CSEN\_SINGLECTRL - Single Conversion Control

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |           |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|-----------|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x03C         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20        | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    | 0x00      |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    | RW        |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    | SINGLESEL |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name        | Reset   | Access             | Description  |
|-------|-------------|---|--------------------|--|
| 31:11 | Reserved    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                    |  |
| 10:4  | SINGLESEL   | 0x00  | RW                 | <b>Single Channel Input Select</b><br>This field selects the channel to be sampled for single channel conversions. |
|       | Mode        | Value   | Description        |  |
|       | APOINT1XCH0 | 32  | Select APOINT1XCH0 |  |
|       | APOINT1YCH1 | 33  | Select APOINT1YCH1 |  |
|       | ...         | ...   | .....              |  |
|       | APOINT3XCH0 | 96  | Select APOINT3XCH0 |  |
|       | APOINT3YCH1 | 97  | Select APOINT3YCH1 |  |
|       | ...         | ...   | .....              |  |
| 3:0   | Reserved    | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |                    |  |

**35.13.17 CSEN\_DMBASELINE - Delta Modulation Baseline**

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0x040         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  | 0x0000       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0x0000     |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Access</b> | RW           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW         |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| <b>Name</b>   | BASELINEDN   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | BASELINEUP |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Bit   | Name       | Reset  | Access | Description  |
|-------|------------|--------|--------|--|
| 31:16 | BASELINEDN | 0x0000 | RW     | <b>Delta Modulator Integrator Initial Value</b><br>When CHOPEN = ENABLE, this field is used to initialize the ramp-down integrator. Unused if CHOPEN = DISABLE.          |
| 15:0  | BASELINEUP | 0x0000 | RW     | <b>Delta Modulator Integrator Initial Value</b><br>This field is used to initialize the integrator. When CHOPEN = ENABLE, this field is used for the ramp-up integrator. |

### 35.13.18 CSEN\_DMCFG - Delta Modulation Configuration

| Offset        | Bit Position |    |    |         |    |    |    |    |    |    |    |        |    |    |    |    |      |    |    |    |    |     |   |   |   |   |   |   |   |      |   |   |
|---------------|--------------|----|----|---------|----|----|----|----|----|----|----|--------|----|----|----|----|------|----|----|----|----|-----|---|---|---|---|---|---|---|------|---|---|
| 0x044         | 31           | 30 | 29 | 28      | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20     | 19 | 18 | 17 | 16 | 15   | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2    | 1 | 0 |
| <b>Reset</b>  |              |    |    | 0       |    |    |    |    |    |    |    | 0x0    |    |    |    |    | 0x0  |    |    |    |    | 0x0 |   |   |   |   |   |   |   | 0x00 |   |   |
| <b>Access</b> |              |    |    | RW      |    |    |    |    |    |    |    | RW     |    |    |    |    | RW   |    |    |    |    | RW  |   |   |   |   |   |   |   | RW   |   |   |
| <b>Name</b>   |              |    |    | DMGRDIS |    |    |    |    |    |    |    | CRMODE |    |    |    |    | DMCR |    |    |    |    | DMR |   |   |   |   |   |   |   | DMG  |   |   |

| Bit   | Name     | Reset   | Access | Description  |       |      |             |   |      |                        |   |      |                        |   |      |                        |   |      |                        |
|-------|----------|---|--------|--|-------|------|-------------|---|------|------------------------|---|------|------------------------|---|------|------------------------|---|------|------------------------|
| 31:29 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |      |                        |   |      |                        |   |      |                        |   |      |                        |
| 28    | DMGRDIS  | 0   | RW     | <b>Delta Modulation Gain Step Reduction Disable</b><br><br>If this bit set, the integrator uses a constant gain step for all cycles, given by DMG. Otherwise, at the end of each cycle, the gain step is divided by two and rounded up ( $DMG = DMG[7:1] + DMG[0]$ ).  |       |      |             |   |      |                        |   |      |                        |   |      |                        |   |      |                        |
| 27:22 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |      |                        |   |      |                        |   |      |                        |   |      |                        |
| 21:20 | CRMODE   | 0x0   | RW     | <b>Delta Modulator Conversion Resolution.</b><br><br>This field selects the resolution for DM conversions.<br><br><table border="1"> <thead> <tr> <th>Value</th> <th>Mode</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>DM10</td> <td>10-bit delta modulator</td> </tr> <tr> <td>1</td> <td>DM12</td> <td>12-bit delta modulator</td> </tr> <tr> <td>2</td> <td>DM14</td> <td>14-bit delta modulator</td> </tr> <tr> <td>3</td> <td>DM16</td> <td>16-bit delta modulator</td> </tr> </tbody> </table> | Value | Mode | Description | 0 | DM10 | 10-bit delta modulator | 1 | DM12 | 12-bit delta modulator | 2 | DM14 | 14-bit delta modulator | 3 | DM16 | 16-bit delta modulator |
| Value | Mode     | Description   |        |  |       |      |             |   |      |                        |   |      |                        |   |      |                        |   |      |                        |
| 0     | DM10     | 10-bit delta modulator  |        |  |       |      |             |   |      |                        |   |      |                        |   |      |                        |   |      |                        |
| 1     | DM12     | 12-bit delta modulator  |        |  |       |      |             |   |      |                        |   |      |                        |   |      |                        |   |      |                        |
| 2     | DM14     | 14-bit delta modulator  |        |  |       |      |             |   |      |                        |   |      |                        |   |      |                        |   |      |                        |
| 3     | DM16     | 16-bit delta modulator  |        |  |       |      |             |   |      |                        |   |      |                        |   |      |                        |   |      |                        |
| 19:16 | DMCR     | 0x0   | RW     | <b>Delta Modulator Conversion Rate</b><br><br>The DMCR field determines how many cycles the DM converter will use per conversion. For the case of DMCR = 0, the converter will perform 16 cycles. Each cycle will consist of between 4 and 64 tests as determined by the DMR field.  |       |      |             |   |      |                        |   |      |                        |   |      |                        |   |      |                        |
| 15:12 | Reserved | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |       |      |             |   |      |                        |   |      |                        |   |      |                        |   |      |                        |
| 11:8  | DMR      | 0x0   | RW     | <b>Delta Modulator Gain Reduction Interval</b><br><br>The DMR field determines how many tests are performed and integrated at each gain step setting. For DMR = 0, 64 tests will be performed per cycle (at the same gain step). For DMR = 1 to 15, (DMR x 4) tests will be performed per cycle.   |       |      |             |   |      |                        |   |      |                        |   |      |                        |   |      |                        |
| 7:0   | DMG      | 0x00  | RW     | <b>Delta Modulator Gain Step</b><br><br>This field sets the initial gain step size (the "delta") for the delta modulator. This field represents a number of codes at the resolution selected by CRMODE.  |       |      |             |   |      |                        |   |      |                        |   |      |                        |   |      |                        |

### 35.13.19 CSEN\_ANACTRL - Analog Control

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |          |    |    |    |    |    |    |    |    |    |    |    |           |   |   |   |           |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----------|----|----|----|----|----|----|----|----|----|----|----|-----------|---|---|---|-----------|---|---|---|---|---|
| 0x048         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21       | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9         | 8 | 7 | 6 | 5         | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    | 0x0      |    |    |    |    |    |    |    |    |    |    |    | 0x0       |   |   |   | 0x7       |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    | RW       |    |    |    |    |    |    |    |    |    |    |    | RW        |   |   |   | RW        |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    | TRSTPROG |    |    |    |    |    |    |    |    |    |    |    | IDACIREFS |   |   |   | IREFFPROG |   |   |   |   |   |

| Bit   | Name      | Reset   | Access | Description  |
|-------|-----------|---|--------|--|
| 31:23 | Reserved  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 22:20 | TRSTPROG  | 0x0   | RW     | <b>Reset Timing</b><br><br>This field adjusts the amount of time used to discharge the external capacitor during a conversion. Reset timing is increased for larger values of TRSTPROG.  |
| 19:11 | Reserved  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 10:8  | IDACIREFS | 0x0   | RW     | <b>Current DAC and Reference Current Scale</b><br><br>This field adjusts the currents used in the CSEN block. This directly affects the drive strength to the external capacitor. For IDACIREFS = 0, the maximum drive strength is used. For IDACIREFS = 1 to 7, the relative drive strength is (IDACIREFS / 8). |
| 7     | Reserved  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 6:4   | IREFFPROG | 0x7   | RW     | <b>Reference Current Control.</b><br><br>This field sets the relative magnitude of the current source that charges the internal reference cap. Lower settings allow for larger external capacitance, and higher settings allow for more precise measurements on smaller capacitors.                              |
| 3:0   | Reserved  | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |

### 35.13.20 CSEN\_IF - Interrupt Flag

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |       |   |     |   |      |   |     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|-------|---|-----|---|------|---|-----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|
| 0x054         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11            | 10 | 9     | 8 | 7   | 6 | 5    | 4 | 3   | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R             | 0  | R     | 0 | R   | 0 | R    | 0 | R   | 0 | R | 0 | R | 0 | R | 0 | R | 0 | R | 0 | R | 0 | R | 0 | R | 0 | R | 0 | R | 0 |   |  |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R             |    | R     |   | R   |   | R    |   | R   |   | R |   | R |   | R |   | R |   | R |   | R |   | R |   | R |   | R |   | R |   | R |  |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | APORTCONFLICT |    | DMAOF |   | EOS |   | CONV |   | CMP |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |

| Bit  | Name          | Reset   | Access | Description   |
|------|---------------|---|--------|---|
| 31:5 | Reserved      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 4    | APORTCONFLICT | 0   | R      | <b>APORT Conflict Interrupt Flag</b><br>1 if any of the BUSes being requested by the CSEN are also being requested by another peripheral                              |
| 3    | DMAOF         | 0   | R      | <b>DMA Overflow Interrupt Flag.</b><br>When DMAEN is 1, this flag will be set to 1 by hardware if DMA does not read the DATA register and a new conversion completes. |
| 2    | EOS           | 0   | R      | <b>End of Scan Interrupt Flag.</b><br>This flag is set to 1 at the end of a scan cycle, after all channels have been converted.                                       |
| 1    | CONV          | 0   | R      | <b>Conversion Done Interrupt Flag</b><br>This flag is set to 1 when a data conversion is complete and the result has been posted to DATA.                             |
| 0    | CMP           | 0   | R      | <b>Digital Comparator Interrupt Flag</b><br>This flag is set to 1 when a CSEN comparator event has happened.  |

## 35.13.21 CSEN\_IFS - Interrupt Flag Set

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |       |     |      |     |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|-------|-----|------|-----|---|---|---|---|---|---|---|
| 0x058         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11            | 10    | 9   | 8    | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0             | 0     | 0   | 0    | 0   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | W1            | W1    | W1  | W1   | W1  |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | APORTCONFLICT | DMAOF | EOS | CONV | CMP |   |   |   |   |   |   |   |

| Bit  | Name          | Reset   | Access | Description  |
|------|---------------|---|--------|--|
| 31:5 | Reserved      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |  |
| 4    | APORTCONFLICT | 0   | W1     | <b>Set APORTCONFLICT Interrupt Flag</b><br>Write 1 to set the APORTCONFLICT interrupt flag |
| 3    | DMAOF         | 0   | W1     | <b>Set DMAOF Interrupt Flag</b><br>Write 1 to set the DMAOF interrupt flag                 |
| 2    | EOS           | 0   | W1     | <b>Set EOS Interrupt Flag</b><br>Write 1 to set the EOS interrupt flag                     |
| 1    | CONV          | 0   | W1     | <b>Set CONV Interrupt Flag</b><br>Write 1 to set the CONV interrupt flag                   |
| 0    | CMP           | 0   | W1     | <b>Set CMP Interrupt Flag</b><br>Write 1 to set the CMP interrupt flag                     |



### 35.13.23 CSEN\_IEN - Interrupt Enable

| Offset        | Bit Position |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |       |     |      |     |   |   |   |   |   |   |   |
|---------------|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|-------|-----|------|-----|---|---|---|---|---|---|---|
| 0x060         | 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11            | 10    | 9   | 8    | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Reset</b>  |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 0             | 0     | 0   | 0    | 0   |   |   |   |   |   |   |   |
| <b>Access</b> |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RW            | RW    | RW  | RW   | RW  |   |   |   |   |   |   |   |
| <b>Name</b>   |              |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | APORTCONFLICT | DMAOF | EOS | CONV | CMP |   |   |   |   |   |   |   |

| Bit  | Name          | Reset   | Access | Description   |
|------|---------------|---|--------|---|
| 31:5 | Reserved      | <i>To ensure compatibility with future devices, always write bits to 0. More information in <a href="#">1.2 Conventions</a></i> |        |   |
| 4    | APORTCONFLICT | 0   | RW     | <b>APORTCONFLICT Interrupt Enable</b><br>Enable/disable the APORTCONFLICT interrupt |
| 3    | DMAOF         | 0   | RW     | <b>DMAOF Interrupt Enable</b><br>Enable/disable the DMAOF interrupt                 |
| 2    | EOS           | 0   | RW     | <b>EOS Interrupt Enable</b><br>Enable/disable the EOS interrupt                     |
| 1    | CONV          | 0   | RW     | <b>CONV Interrupt Enable</b><br>Enable/disable the CONV interrupt                   |
| 0    | CMP           | 0   | RW     | <b>CMP Interrupt Enable</b><br>Enable/disable the CMP interrupt                     |

## 36. Revision History

### Revision 1.1

May, 2019

- Restored PLFRCO and associated details throughout document (re-introduced with Rev -D OPNs).
- [Table 2.3 EFR32xG13 Wireless Gecko Timers Overview on page 38](#): Added low frequency clock sources for SysTick.
- [4.7.2 MODULEINFO - Module trace information](#) ; [4.7.3 MODXOCAL - Module Crystal Oscillator Calibration](#) : Added device identification entries for modules to the DI page.
- [7.3.2 Embedded Trace Macrocell V3.5 \(ETM\)](#): Clarified clock configuration requirements for enabling ETM.
- [8.2 Features](#): Updated flash zero wait-state access max frequency.
- [8.3.2 Lock Bits \(LB\) Page Description](#): Revised configuration lock word description to include default state.
- [Table 9.3 List of Peripherals Capable of Waking Up LDMA in EM2 Deep Sleep or EM3 Stop on page 204](#): Added table of peripherals that can wake LDMA.
- [11.3.9.2.1 EM2/EM3 Voltage Scaling Guidelines](#): Appended note regarding HFRCO clock default frequency when waking to EM0/EM1 while using EM2/EM3 voltage scaling.
- [Figure 24.1 VDAC Overview on page 796](#): Added HFPERCLK and prescaler block as VDAC clock source.
- [27.3.3.2 Scan Mode](#): Added note regarding the ADC conversion scan ID in continuous scan mode with no delay between repeated conversions.
- [27.3.10.2 Repetitive Mode](#): Added note regarding the ADC in SYNC mode with repetitive conversions when using a delay between repeated conversions.

### Revision 1.0

March, 2018

- Removed PLFRCO and associated details throughout document (removed from Rev -C OPNs).
- [Figure 4.3 System Address Space With Peripheral Listing on page 47](#): Fixed to show all peripheral mappings.
- [8.5.19 MSC\\_BOOTLOADERCTRL - Bootloader Read and Write Enable, Write Once Register](#) : Corrected descriptions of BLWDIS and BLRDIS.
- [10.3.3 Power-On Reset \(POR\)](#): Clarification of Power-On Reset supply connection (AVDD) and threshold (1.2V).
- Added information about analog peripheral power connections and VDDX\_ANA supply rail throughout document.
- Added information about IOVDD and AVDD restrictions on analog input signals throughout document.
- [11.3.11 Brown Out Detector \(BOD\)](#): Included missing BOD details in paragraph.
- [Table 11.2 EMU Energy Mode Overview on page 252](#): Added footnote for GPIO Pin State Retention in EM4 modes.
- [11.3.5.1 Bypass Mode](#): Added information on when bypass mode can be used and how to do so.
- [11.3.9.1 EM0/EM1 Voltage Scaling](#): Clarification of reset effects on voltage scaling operations in progress.
- [11.3.12 Voltage Monitor \(VMON\)](#): Added note about VMON hysteresis and rising/falling thresholds.
- [12. CMU - Clock Management Unit](#) : Removed erroneous information about DPLL.
- [12.3.2.4 HFXO Configuration](#): Clarified steady state timeout and state transition to ready.
- [12.3.2.5 LFXO Configuration](#): Added recommendations for GAIN setting.
- [16.3.1.3 Configurable PRS Logic](#): Clarified ANDNEXT and ORPREV behavior for first and last PRS channels.
- [16.3.2 Producers](#): Added more detail about GPIO producer source.
- [16.3.5 DMA Request on PRS](#): Fixed incorrect bit / register names and clarified signals for DMA are PRSRQE0 and PRSREQ1.
- [27.3.17 ADC Programming Model](#): Added note about changing to ASYNC clock mode with KEEPADCWARM.

### Revision 0.5

May 3rd, 2017

- [Section 7.3.1](#): Clarified default state of debug logic from power-on is JTAG.
- [Section 8.x](#): Added language to clarify that flash erase and write are only supported in high voltage modes (Voltage Scale Level 2).
- [Section 12.x](#): Added PLFRCO to low-frequency clocking diagram, and to discussions of LFnCLKs as needed.
- [Table 12.3](#): Changed maximum frequency condition for WS2 to 20 MHz.
- [TRNGn\\_FIFOLEVEL register](#): Marked as actionable reads, because the STATUS\_FULLIF flag is cleared upon reading this register.
- [Figure 34.3](#): Updated APORT diagram to include internal signal connections between analog peripherals.
- Removed *Confidential* watermark.

**Revision 0.1**

January 17th, 2017

Initial release.

**Appendix 1. Abbreviations**

This section lists abbreviations used in this document.

**Table 1.1. Abbreviations**

| Abbreviation | Description  |
|--------------|--|
| ADC          | Analog to Digital Converter  |
| AES          | Advanced Encryption Standard   |
| AFC          | Automatic Frequency Control  |
| AGC          | Automatic Gain Control   |
| AHB          | AMBA Advanced High-performance Bus. AMBA is short for "Advanced Microcontroller Bus Architecture". |
| APB          | AMBA Advanced Peripheral Bus. AMBA is short for "Advanced Microcontroller Bus Architecture".       |
| APC          | Automatic Power Control  |
| ASK          | Amplitude Shift Keying   |
| BLE          | Bluetooth Low Energy   |
| BLE-LR       | Bluetooth Low Energy Long Range  |
| BR           | Baud Rate  |
| BT           | Bandwidth Time product   |
| BUFC         | Buffer Controller  |
| BW           | Bandwidth  |
| CBC          | Cipher Block Chaining (AES mode of operation)  |
| CBC-MAC      | Cipher Block Chaining - Message Authentication Code (AES mode of operation)                        |
| CC           | Compare / Capture  |
| CCA          | Clear Channel Assessment   |
| CFB          | Cipher Feedback (AES mode of operation)  |
| CHF          | Channel Filter   |
| CLK          | Clock  |
| CM3          | ARM Cortex-M3  |
| CM4          | ARM Cortex-M4  |
| CMD          | Command  |
| CMU          | Clock Management Unit  |
| CRC          | Cyclic Redundancy Check  |
| CTR          | Counter mode (AES mode of operation)   |
| CTRL         | Control  |
| DBG          | Debug  |
| DC           | Direct Current   |
| DEC          | Decimator  |
| DEMOD        | Demodulator  |

| Abbreviation | Description                                  |
|--------------|--|
| DSA          | Detection of Signal Arrival                  |
| DSSS         | Direct Sequence Spread Spectrum              |
| ECB          | Electronic Code Book (AES mode of operation) |
| EFR32        | Wireless Gecko                               |
| EM           | Energy Mode                                  |
| EMU          | Energy Management Unit                       |
| FEC          | Forward Error Correction                     |
| FIR          | Finite Impulse Response                      |
| FRC          | Frame Controller                             |
| FSK          | Frequency Shift Keying                       |
| GFSK         | Gaussian Frequency Shift Keying              |
| GMSK         | Gaussian Minimum Shift Keying                |
| GPIO         | General Purpose Input / Output               |
| HFRCO        | High Frequency RC Oscillator                 |
| HFXO         | High Frequency Crystal Oscillator            |
| HW           | Hardware                                     |
| Hz           | Hertz  |
| IF           | Intermediate Frequency                       |
| ISR          | Interrupt Service Routine                    |
| LFRCO        | Low Frequency RC Oscillator                  |
| LFXO         | Low Frequency Crystal Oscillator             |
| LNA          | Low Noise Amplifier                          |
| LO           | Local Oscillator                             |
| MOD          | Modulator                                    |
| MODEM        | Modulator and Demodulator                    |
| MSK          | Minimum Shift Keying                         |
| NRZ          | Non Return to Zero                           |
| NVIC         | Nested Vector Interrupt Controller           |
| OFB          | Output Feedback Mode (AES mode of operation) |
| OOK          | On Off Keying                                |
| OQPSK        | Offset Quadrature Phase Shift Keying         |
| OSR          | Over-Sampling Ratio                          |
| PA           | Power Amplifier                              |
| PD           | Power Down                                   |
| PHY          | Physical Layer                               |
| PROTIMER     | Protocol Timer                               |
| PRS          | Peripheral Reflex System                     |

| Abbreviation | Description                        |
|--------------|------------------------------------|
| PWM          | Pulse Width Modulation             |
| RAC          | Radio Controller                   |
| RAM          | Random Access Memory               |
| RF           | Radio Frequency                    |
| RMU          | Reset Management Unit              |
| RSM          | Radio State Machine                |
| RSSI         | Received Signal Strength Indicator |
| RTC          | Real Time Counter                  |
| RX           | Receive                            |
| SEQ          | Radio Sequencer                    |
| SPI          | Serial Peripheral Interface        |
| SRC          | Sample Rate Converter              |
| STIMER       | Sequencer Timer                    |
| SW           | Software                           |
| SYNTH        | Synthesizer                        |
| TX           | Transmit                           |
| WOR          | Wake On Radio                      |
| XTAL         | Crystal                            |

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