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EFM32GG942 Errata, Chip Rev. E

F1024/F512

This document describes errata for the latest revision of EFM32GG942 devices.

ARM ZERO TINY GECKO LEOPARD GIANT WONDER

SILICON LABS

1 Errata

This document contains information on the errata of the latest revision of this device. For errata on older revisions, please refer to the errata history for the device. The device data sheet explains how to identify chip revisions, either from package markings or electronically.

In addition to the errata noted below, the errata for the ARM Cortex-M3 r2p1 (www.arm.com) also applies to this device.

1.1 Chip revision E

Table 1.1. Erratas

ID	Title/Problem	Effect	Fix/Workaround
ADC_E116	**Offset in ADC Temperature Sensor Calibration DataData** The ADC temperature sensor calibration value stored in the Device Information (DI) Page has an offset.	For devices with PROD_REV values of 16 or 17, the ADC0_TEMP_0_READ_1V25 register of the Device Information Page has an offset of 112. Using this value for calculating the absolute temperature gives an approximately 18 degrees too high value. Relative temperature measurements (temperature changes) are not affected by this offset.	For devices with PROD_REV values of 16 or 17, use ADC0_TEMP_0_READ_1V25 - 112 instead of ADC0_TEMP_0_READ_1V25 when calculating the temperature.
ADC_E117	**TIMEBASE not wide enough** For 48 MHz ADC clock, the ADC_CTRL_TIMEBASE is not wide enough.	For ADC warm-up, the user is required to set the ADC_CTRL_TIMEBASE to the number of ADC clock cycles in 1 µs. As this register is only 5 bits wide, it does not support frequencies above 32 MHz.	If an ADC clock above 32 MHz is required, the acquistion time should be increased to also account for too short warmup-time.
AES_E101	**BYTEORDER does not work in combination with DATASTART/XORSTART** When the BYTEORDER bit in AES_CTRL is set, an encryption or decryption should not be started through DATASTART or XORSTART.	If BYTEORDER is used in combination with DATASTART or XORSTART, the AES data and key are interpreted in the wrong order.	Do not use BYTEORDER in combination with DATASTART or XORSTART.
AES_E102	**AES_STATUS_RUNNING set one cycle late with BYTEORDER set** When the BYTEORDER bit in AES_CTRL is set, AES_STATUS_RUNNING is set one cycle late.	If BYTEORDER is used, it will take one cycle for the AES_STATUS_RUNNING flag to be set. This means that polling this status flag should be postponed at least one cycle after starting encryption/decryption.	If polling the AES_STATUS_RUNNING is preferred, insert a No Operation assembly instruction (NOP()) before starting to poll the status flag.
BURTC_E101	**BURTC LPMODE entry**	Counting error occurs if overflow on 7 LSBs happens when entering LPMODE with LPCOMP=7. This results in the	Avoid using LPMODE with LPCOMP=7.

ID	Title/Problem	Effect	Fix/Workaround
	Entering LPMODE with LPCOMP=7 causes counter error.	counter value being 256 less than it should be after the error. The error accumulates.	
BU_E105	**LFXO missing cycles during IOVDD ramping** LFXO missing cycles during IOVDD ramping when used in combination with Backup mode.	When IOVDD is ramped, the dc-level of the XTAL signal changes, resulting in missed LFXO cycles and possible glitches on the LFXO clock.	Set PRESC in BURTC_CTRL to greater then 0 when ramping IOVDD in combination with Backup mode to avoid glitches on the LFXO clock.
CMU_E112	**LFXO boost buffer current setting** LFXO boost buffer current must be disabled	LFXO will not work properly with LFXOBUFCUR in CMU_CTRL set.	Do not set LFXOBUFCUR in CMU_CTRL.
CMU_E113	**LFXO startup at high temperature** LFXO does not start at high temperature with default configuration.	For devices with PROD_REV = 16, LFXO may have startup issues with low capacitance crystals when using the default LFXO configuration.	Make this line of code part of your starup code, typically in the start of main(): *((volatile uint32_t*) 0x400c80C0) = (*((volatile uint32_t*) 0x400c80C0) & ~(1<<6)) | (1<<4);.
DAC_E109	**DAC output drift over lifetime** The voltage output of the DAC might drift over time.	When the device is powered and the DAC is disabled, stress on an internal circuit node can cause the output voltage of the DAC to drift over time, and in some cases may violate the $V_{DACOFFSET}$ specification. If the DAC is always enabled while the device is powered, this condition cannot occur.	Both in the startup initialization code and prior to disabling the DAC in application code, set the OPAnSHORT bit in DACn_OPACTRL to a '1' for the corresponding DAC(s) used by the application. This will prevent the output voltage drift over time effect.
DMA_E101	**EM2 with WFE and DMA** WFE does not work for the DMA in EM2.	In EM2, when sleeping with WFE (Wait for Event), an interrupt from the DMA will not wake up the system.	Use WFI (Wait for Interrupt) or EM1 instead.
PCNT_E102	**PCNT Pulse Width Filtering does not work**	The PCNT Pulse Width Filter does not work as intended.	Do not use the pulse width filter, i.e. ensure FILT = 0 in PCNTn_CTRL.
PRS_E101	**Edge detect on GPIO/ACMP** Edge detect on peripherals with asynchronous edges might be missed.	When using edge detect in PRS on signals from ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP and BURTC edges can be missed.	Do not use edge detect on ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP and BURTC.
TIMER_E103	**Capture/compare output is unreliable with RSSCOIST enabled** The TIMER capture/compare output is unreliable when RSSCOIST is enabled and the clock is prescaled.	When RSSCOIST is set and PRESC > 0 in TIMERn_CTRL, the capture/compare output value is not reliable.	Do not use a prescaled clock, i.e. ensure PRESC = 0 in TIMERn_CTRL when RSSCOIST is enabled.

ID	Title/Problem	Effect	Fix/Workaround
USART_E112	**USART AUTOTX continues to transmit even with full RX buffer** USART AUTOTX continues to transmit even with full RX buffer.	When AUTOTX in USARTn_CTRL or AUTOTXEN in USARTn_TRIGCTRL is set, the USART will continue to transmit data even after the RX buffer is full. This may cause the RX buffer to overflow if the data is not read out in time.	No known workaround.
USB_E103	**HNP Sequence fails if A-Device connects after 3.4ms**	The B-Device core only waits for up to 3.4ms before signalling HNP fail and reverting back to Peripheral mode. Therefore, the HNP sequence fails if the A-Device connects after 3.4ms.	No known workaround.
USB_E104	**USB A-Device delays the HNP switch back process** The D+ line disconnects after 200 ms, delaying the HNP switch back process.	The A-Device core delays the HNP switch back process. As per the USB-OTG 2.0 specification, the B-Device on the other side of the USB pipe either should wait for disconnect from the A-Device or should switch to Peripheral mode and wait for the A-Device to issue a USB reset. Hence, there is no significant impact on actual operation.	No known workaround.
USB_E105	**B-Device as Host driving K-J pairs during reset** The A-Device misinterprets the K-J pairs as Suspend after switching to High Speed mode.	If the B-Device as Host on the other side of the USB pipe drives K-J pairs for more than 200 ms during USB reset, the A-Device core exits peripheral state, causing the HNP process to fail. There is no significant impact since normally the host drives USB reset for a shorter time than 200 ms.	No known workaround.
USB_E109	**Missing USB_GINTSTS.SESSREQINT Interrupt with USB_PCGCCTL.STOPPCLK = 1** A Host-initiated Suspend, followed by a Host Disconnect and Host Connect will not result in a SessReq interrupt.	When USB_PCGCCTL.STOPPCLK is set and the device is acting as a B-peripheral, a Host-initated Suspend, followed by a Host Disconnect and Host Connect will not result in a SessReq interrupt.	If this is an expected use-case, USB_PCGCCTL.STOPPCLK should not be set. USB_PCGCCTL.GATEHCLK can still be used to save power.
USB_E110	**Unexpected USB_HCx_INT.CHHLTD interrupt** In some cases the USB_HCx_INT.CHHLTD interrupt might be incorrectly set.	In some cases, an unexpected USB_HCx_INT.CHHLTD interrupt might be received from another endpoint that does not have the USB_HCx_CHAR.CHDIS, USB_HCx_INT.XACTERR, USB_HCx_INT.BBLERR, USB_HCx_INT.DATATGLERR or USB_HCx_INT.XFERCOMPL interrupts enabled.	If such an interrupt is received, the application must re-enable the channel for which it received the unexpected USB_HCx_INT.CHHLTD interrupt.

1.2 Older Revisions

Erratas for older revisions can be found at the Silicon Laboratories homepage:

www.silabs.com/32bit-errata

2 Revision History

2.1 Revision 1.20

April 8th, 2016

Updated the latest revision to revision E.

Removed BURTC_E102, BU_E106, CMU_E114, DI_E101, EMU_107, and LES_E103 from revision E.

2.2 Revision 1.10

February 20th, 2015

Added DAC_E109.

Added EMU_E107.

Added TIMER_E103.

Added PCNT_E102.

Updated link to errata for older revisions.

Corrected typos.

Updated Trademark Information.

2.3 Revision 0.80

August 21st, 2013

Added ADC_E117.

Added AES_E102.

Added USB_E109.

Added USB_E110.

Updated disclaimer, trademark and contact information.

2.4 Revision 0.70

July 30th, 2013

Added AES_E101.

Added BURTC_E102.

Added CMU_E114.

Added DMA_E101.

Updated errata naming convention.

2.5 Revision 0.60

June 5th, 2012

Added ADC1.

Added DI1.

2.6 Revision 0.50

April 24th, 2012

Added BU6.

Added CMU4.

Added CMU5.

Added LES3.

Removed Erratas not valid for chip revision.

2.7 Revision 0.30

January 13th, 2012

Added USART1.

2.8 Revision 0.20

January 6th, 2012

Added CMU3.

Added CUR3.

Added CUR4.

Added USB7.

Added USB8.

Added MSC1.

Updated PRS1.

Removed Erratas not valid for chip revision.

2.9 Revision 0.10

November 4th, 2011

Initial preliminary release.

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B Contact Information

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701

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Table of Contents

List of Tables

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ZERO
ARM Cortex-M0+
TINY
ARM Cortex-M3
GECKO
ARM Cortex-M3
LEOPARD
ARM Cortex-M3
GIANT
ARM Cortex-M3
WONDER
ARM Cortex-M4