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EFM32GG900 Errata History

F1024/F512

This document describes known errata for all revisions of EFM32GG900 devices.

ARM ZERO TINY GECKO LEOPARD GIANT WONDER

SILICON LABS

1 Errata History

1.1 Errata Overview

Table 1.1 (p. 2) shows which erratum is applicable for each revision. The device datasheet explains how to identify chip revision, either from package marking or electronically.

In addition to the errata noted below, the errata for the ARM Cortex-M3 r2p1 (www.arm.com) also applies to all revisions of this device.

Table 1.1. Errata Overview

Erratum ID	Rev. E	Rev. D
ADC_E116	X	X
ADC_E117	X	X
AES_E101	X	X
AES_E102	X	X
BU_E105	X	X
BU_E106		X
BURTC_E101	X	X
BURTC_E102		X
CMU_E112	X	X
CMU_E113	X	X
CMU_E114		X
DAC_E109	X	X
DI_E101		X
DMA_E101	X	X
EBI_E103	X	X
EMU_E107		X
LES_E103		X

Erratum ID	Rev. E	Rev. D
PCNT_E102	X	X
PRS_E101	X	X
TIMER_E103	X	X
USART_E112	X	X
USB_E103	X	X
USB_E104	X	X
USB_E105	X	X
USB_E109	X	X
USB_E110	X	X

1.2 EFM32GG900 Errata Descriptions

Table 1.2. EFM32GG900 Errata Descriptions

ID	Title/Problem	Effect	Fix/Workaround
ADC_E116	**Offset in ADC Temperature Sensor Calibration DataData** The ADC temperature sensor calibration value stored in the Device Information (DI) Page has an offset.	For devices with PROD_REV values of 16 or 17, the ADC0_TEMP_0_READ_1V25 register of the Device Information Page has an offset of 112. Using this value for calculating the absolute temperature gives an approximately 18 degrees too high value. Relative temperature measurements (temperature changes) are not affected by this offset.	For devices with PROD_REV values of 16 or 17, use ADC0_TEMP_0_READ_1V25 - 112 instead of ADC0_TEMP_0_READ_1V25 when calculating the temperature.
ADC_E117	**TIMEBASE not wide enough** For 48 MHz ADC clock, the ADC_CTRL_TIMEBASE is not wide enough.	For ADC warm-up, the user is required to set the ADC_CTRL_TIMEBASE to the number of ADC clock cycles in 1 µs. As this register is only 5 bits wide, it does not support frequencies above 32 MHz.	If an ADC clock above 32 MHz is required, the acquisition time should be increased to also account for too short warmup-time.
AES_E101	**BYTEORDER does not work in combination with DATASTART/XORSTART** When the BYTEORDER bit in AES_CTRL is set, an encryption or de-	If BYTEORDER is used in combination with DATASTART or XORSTART, the AES data and key are interpreted in the wrong order.	Do not use BYTEORDER in combination with DATASTART or XORSTART.

ID	Title/Problem	Effect	Fix/Workaround
	cryption should not be started through DATASTART or XORSTART.		
AES_E102	**AES_STATUS_RUNNING set one cycle late with BYTEORDER set** When the BYTEORDER bit in AES_CTRL is set, AES_STATUS_RUNNING is set one cycle late.	If BYTEORDER is used, it will take one cycle for the AES_STATUS_RUNNING flag to be set. This means that polling this status flag should be postponed at least one cycle after starting encryption/decryption.	If polling the AES_STATUS_RUNNING is preferred, insert a No Operation assembly instruction (NOP()) before starting to poll the status flag.
BU_E105	**LFXO missing cycles during IOVDD ramping** LFXO missing cycles during IOVDD ramping when used in combination with Backup mode.	When IOVDD is ramped, the dc-level of the XTAL signal changes, resulting in missed LFXO cycles and possible glitches on the LFXO clock.	Set PRESC in BURTC_CTRL to greater then 0 when ramping IOVDD in combination with Backup mode to avoid glitches on the LFXO clock.
BU_E106	**Current leakage in Backup mode**	In Backup mode, when VDD > BU_VIN + 0.7, current will leak from VDD.	To avoid leakage, exit Backup mode before VDD exceeds the voltage where the leakage start by configuring the threshold in EMU_BUACT.
BURTC_E101	**BURTC LPMODE entry** Entering LPMODE with LPCOMP=7 causes counter error.	Counting error occurs if overflow on 7 LSBs happens when entering LPMODE with LPCOMP=7. This results in the counter value being 256 less than it should be after the error. The error accumulates.	Avoid using LPMODE with LPCOMP=7.
BURTC_E102	**BURTC_CNT read error** Software reads from BURTC_CNT might fail when LPMODE is activated	When LPMODE is active (i.e. BURTC_STATUS_LPMODEACT is high), software reads might result in wrong value being read from BURTC_CNT.	Before reading BURTC_CNT, disable LPMODE and wait for BURTC_STATUS_LPMODEACT to be cleared before reading BURTC_CNT.
CMU_E112	**LFXO boost buffer current setting** LFXO boost buffer current must be disabled	LFXO will not work properly with LFXOBUFCUR in CMU_CTRL set.	Do not set LFXOBUFCUR in CMU_CTRL.
CMU_E113	**LFXO startup at high temperature** LFXO does not start at high temperature with default configuration.	For devices with PROD_REV = 16, LFXO may have startup issues with low capacitance crystals when using the default LFXO configuration.	Make this line of code part of your starup code, typically in the start of main(): *((volatile uint32_t*) 0x400c80C0) = (*((volatile uint32_t*) 0x400c80C0) & ~(1<<6)) | (1<<4);.
CMU_E114	**Device not waking up from EM2 when using prescaled non-HFRCO oscillator as HFCLK**	If the device is running from any prescaled oscillator other than HFRCO as HFCLK and HFRCO is disabled, the device will not wake up from EM2.	Before entering EM2, clear CMU_CTRL_HFCLKDIV. Alternatively, enable HFRCO by setting CMU_OSCENCMD_HFRCOEN and wait until CMU_STATUS_HFRCORDY is set.

ID	Title/Problem	Effect	Fix/Workaround
DAC_E109	**DAC output drift over lifetime** The voltage output of the DAC might drift over time.	When the device is powered and the DAC is disabled, stress on an internal circuit node can cause the output voltage of the DAC to drift over time, and in some cases may violate the $V_{DACOFFSET}$ specification. If the DAC is always enabled while the device is powered, this condition cannot occur.	Both in the startup initialization code and prior to disabling the DAC in application code, set the OPAnSHORT bit in DACn_OPACTRL to a '1' for the corresponding DAC(s) used by the application. This will prevent the output voltage drift over time effect.
DI_E101	**Flash Page Size** The MEM_INFO_PAGE_SIZE value stored in Device Information (DI) Page is incorrect.	For devices with PROD_REV values lower than 18, the MEM_INFO_PAGE_SIZE register value in the Device Information Page is incorrect.	Use fixed flash page size of 4k bytes.
DMA_E101	**EM2 with WFE and DMA** WFE does not work for the DMA in EM2.	In EM2, when sleeping with WFE (Wait for Event), an interrupt from the DMA will not wake up the system.	Use WFI (Wait for Interrupt) or EM1 instead.
EBI_E103	**Page mode read in D16A16ALE mode** Page mode read in D16A16ALE mode skips RDSETUP stage for page mode accesses.	Page mode read in D16A16ALE mode skips RDSETUP stage for page mode accesses, making the read process go directly from ADDRSETUP to RDPA.	To compensate for the missing hold time related to the ALE address latch, the HALFALE field in EBI_ADDRTIMING can be enabled providing a 1/2 cycle hold time.
EMU_E107	**Interrupts during EM2 entry** An interrupt from a peripheral running from the high frequency clock that is received during EM2 entry will cause the EMU to ignore the SLEEPDEEP-flag.	During EM2 entry, the high frequency clocks that are disabled during EM2 will run for some clock cycles after WFI is issued to allow safe shutdown of the peripherals. If an enabled interrupt is requested from one of these non-EM2 peripherals during this shutdown period, the attempt to enter EM2 will fail, and the device will enter EM1 instead. As a result the pending interrupt will immediately wake the device to EM0.	Before entering EM2, disable all high frequency peripheral interrupts in the core.
LES_E103	**AUXHFRCO and LESENSE** LESENSE will not work properly at low AUXHFRCO frequencies.	LESENSE will not work properly when used with the AUXHFRCO running at the 1 or 7 MHz band.	Do not use a AUXHFRCO frequency band of 1 or 7 MHz when used in combination with LESENSE.
PCNT_E102	**PCNT Pulse Width Filtering does not work**	The PCNT Pulse Width Filter does not work as intended.	Do not use the pulse width filter, i.e. ensure FILT = 0 in PCNTn_CTRL.
PRS_E101	**Edge detect on GPIO/ACMP** Edge detect on peripherals with asynchronous edges might be missed.	When using edge detect in PRS on signals from ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP and BURTC edges can be missed.	Do not use edge detect on ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP and BURTC.

ID	Title/Problem	Effect	Fix/Workaround
TIMER_E103	**Capture/compare output is unreliable with RSSCOIST enabled** The TIMER capture/compare output is unreliable when RSSCOIST is enabled and the clock is prescaled.	When RSSCOIST is set and PRESC > 0 in TIMERn_CTRL, the capture/compare output value is not reliable.	Do not use a prescaled clock, i.e. ensure PRESC = 0 in TIMERn_CTRL when RSSCOIST is enabled.
USART_E112	**USART AUTOTX continues to transmit even with full RX buffer** USART AUTOTX continues to transmit even with full RX buffer.	When AUTOTX in USARTn_CTRL or AUTOTXEN in USARTn_TRIGCTRL is set, the USART will continue to transmit data even after the RX buffer is full. This may cause the RX buffer to overflow if the data is not read out in time.	No known workaround.
USB_E103	**HNP Sequence fails if A-Device connects after 3.4ms**	The B-Device core only waits for up to 3.4ms before signalling HNP fail and reverting back to Peripheral mode. Therefore, the HNP sequence fails if the A-Device connects after 3.4ms.	No known workaround.
USB_E104	**USB A-Device delays the HNP switch back process** The D+ line disconnects after 200 ms, delaying the HNP switch back process.	The A-Device core delays the HNP switch back process. As per the USB-OTG 2.0 specification, the B-Device on the other side of the USB pipe either should wait for disconnect from the A-Device or should switch to Peripheral mode and wait for the A-Device to issue a USB reset. Hence, there is no significant impact on actual operation.	No known workaround.
USB_E105	**B-Device as Host driving K-J pairs during reset** The A-Device misinterprets the K-J pairs as Suspend after switching to High Speed mode.	If the B-Device as Host on the other side of the USB pipe drives K-J pairs for more than 200 ms during USB reset, the A-Device core exits peripheral state, causing the HNP process to fail. There is no significant impact since normally the host drives USB reset for a shorter time than 200 ms.	No known workaround.
USB_E109	**Missing USB_GINTSTS.SESSREQINT Interrupt with USB_PCGCCTL.STOPPCLK = 1** A Host-initiated Suspend, followed by a Host Disconnect and Host Connect will not result in a SessReq interrupt.	When USB_PCGCCTL.STOPPCLK is set and the device is acting as a B-peripheral, a Host-initated Suspend, followed by a Host Disconnect and Host Connect will not result in a SessReq interrupt.	If this is an expected use-case, USB_PCGCCTL.STOPPCLK should not be set. USB_PCGCCTL.GATEHCLK can still be used to save power.
USB_E110	**Unexpected USB_HCx_INT.CHHLTD interrupt**	In some cases, an unexpected USB_HCx_INT.CHHLTD interrupt might be received from another endpoint that does not have the USB_HCx_CHAR.CHDIS, USB_HCx_INT.XACTERR, USB_HCx_INT.BBLERR,	If such an interrupt is received, the application must re-enable the channel for which it received the unexpected USB_HCx_INT.CHHLTD interrupt.

ID	Title/Problem	Effect	Fix/Workaround
	In some cases the USB_HCx_INT.CHHLTD interrupt might be incorrectly set.	USB_HCx_INT.DATATGLERR or USB_HCx_INT.XFERCOMPL interrupts enabled.	

2 Revision History

2.1 Revision 1.20

April 8th, 2016

Updated the latest revision to revision E.

Removed BURTC_E102, BU_E106, CMU_E114, DI_E101, EMU_107, and LES_E103 from revision E.

2.2 Revision 1.10

February 20th, 2015

Added DAC_E109.

Added TIMER_E103.

Added PCNT_E102.

Corrected typos.

2.3 Revision 1.00

Aug 8th, 2014

Initial release.

A Disclaimer and Trademarks

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