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EFM32GG880 Errata History

F1024/F512

This document describes known errata for all revisions of EFM32GG880 devices.

ARM ZERO TINY GECKO LEOPARD GIANT WONDER

SILICON LABS

1 Errata History

1.1 Errata Overview

Table 1.1 (p. 2) shows which erratum is applicable for each revision. The device datasheet explains how to identify chip revision, either from package marking or electronically.

In addition to the errata noted below, the errata for the ARM Cortex-M3 r2p1 (www.arm.com) also applies to all revisions of this device.

Table 1.1. Errata Overview

Erratum ID	Rev. E	Rev. D	Rev. C	Rev. B
ADC_E116	X	X		
ADC_E117	X	X	X	X
AES_E101	X	X	X	X
AES_E102	X	X	X	X
BU_E101				X
BU_E102				X
BU_E104				X
BU_E105	X	X	X	X
BU_E106		X		
BURTC_E101	X	X	X	X
BURTC_E102		X	X	X
CMU_E108				X
CMU_E110				X
CMU_E111			X	X
CMU_E112	X	X		
CMU_E113	X	X		

Erratum ID	Rev. E	Rev. D	Rev. C	Rev. B
CMU_E114		X	X	X
CUR_E103			X	
CUR_E105			X	X
DAC_E109	X	X	X	X
DI_E101		X	X	X
DMA_E101	X	X	X	X
EBI_E101				X
EBI_E102				X
EBI_E103	X	X	X	X
EMU_E105				X
EMU_E107		X	X	X
ETM_E101				X
GPIO_E101				X
LES_E101				X
LES_E102				X
LES_E103		X		
MSC_E101			X	X
OPA_E101				X
PCNT_E102	X	X	X	X
PRS_E101	X	X	X	X
TIMER_E103	X	X	X	X
USART_E112	X	X	X	X

1.2 EFM32GG880 Errata Descriptions

Table 1.2. EFM32GG880 Errata Descriptions

ID	Title/Problem	Effect	Fix/Workaround
ADC_E116	**Offset in ADC Temperature Sensor Calibration DataData** The ADC temperature sensor calibration value stored in the Device Information (DI) Page has an offset.	For devices with PROD_REV values of 16 or 17, the ADC0_TEMP_0_READ_1V25 register of the Device Information Page has an offset of 112. Using this value for calculating the absolute temperature gives an approximately 18 degrees too high value. Relative temperature measurements (temperature changes) are not affected by this offset.	For devices with PROD_REV values of 16 or 17, use ADC0_TEMP_0_READ_1V25 - 112 instead of ADC0_TEMP_0_READ_1V25 when calculating the temperature.
ADC_E117	**TIMEBASE not wide enough** For 48 MHz ADC clock, the ADC_CTRL_TIMEBASE is not wide enough.	For ADC warm-up, the user is required to set the ADC_CTRL_TIMEBASE to the number of ADC clock cycles in 1 µs. As this register is only 5 bits wide, it does not support frequencies above 32 MHz.	If an ADC clock above 32 MHz is required, the acquistion time should be increased to also account for too short warmup-time.
AES_E101	**BYTEORDER does not work in combination with DATASTART/XORSTART** When the BYTEORDER bit in AES_CTRL is set, an encryption or decryption should not be started through DATASTART or XORSTART.	If BYTEORDER is used in combination with DATASTART or XORSTART, the AES data and key are interpreted in the wrong order.	Do not use BYTEORDER in combination with DATASTART or XORSTART.
AES_E102	**AES_STATUS_RUNNING set one cycle late with BYTEORDER set** When the BYTEORDER bit in AES_CTRL is set, AES_STATUS_RUNNING is set one cycle late.	If BYTEORDER is used, it will take one cycle for the AES_STATUS_RUNNING flag to be set. This means that polling this status flag should be postponed at least one cycle after starting encryption/decryption.	If polling the AES_STATUS_RUNNING is preferred, insert a No Operation assembly instruction (NOP()) before starting to poll the status flag.
BU_E101	**Backup power increased power consumtion** Additional current consumption on BU_VIN approximately 100uA when VDD_DREG is between 0.3 BU_VIN to 0.7 BU_VIN.	Additional current consumption on BU_VIN approximately 100uA when VDD_DREG is between 0.3 BU_VIN to 0.7 BU_VIN.	Avoid having VDD_DREG in between 0.3 BU_VIN to 0.7 BU_VIN.
BU_E102	**EM4 GPIO retention in backup mode**	With GPIO retention enabled, GPIO pins will still drive in backup mode.	Do not use EM4 GPIO retention in combination with backup mode.

ID	Title/Problem	Effect	Fix/Workaround
	EM4 GPIO retention not shut off in backup mode.		
BU_E104	**EM4 with backup BODs** EM4 with backup BODs does not trigger reset.	EM4 with backup BODs does not trigger reset.	Avoid using backup BODs when entering EM4.
BU_E105	**LFXO missing cycles during IOVDD ramping** LFXO missing cycles during IOVDD ramping when used in combination with Backup mode.	When IOVDD is ramped, the dc-level of the XTAL signal changes, resulting in missed LFXO cycles and possible glitches on the LFXO clock.	Set PRESC in BURTC_CTRL to greater then 0 when ramping IOVDD in combination with Backup mode to avoid glitches on the LFXO clock.
BU_E106	**Current leakage in Backup mode**	In Backup mode, when VDD > BU_VIN + 0.7, current will leak from VDD.	To avoid leakage, exit Backup mode before VDD exceeds the voltage where the leakage start by configuring the threshold in EMU_BUACT.
BURTC_E101	**BURTC LPMODE entry** Entering LPMODE with LPCOMP=7 causes counter error.	Counting error occurs if overflow on 7 LSBs happens when entering LPMODE with LPCOMP=7. This results in the counter value being 256 less than it should be after the error. The error accumulates.	Avoid using LPMODE with LPCOMP=7.
BURTC_E102	**BURTC_CNT read error** Software reads from BURTC_CNT might fail when LPMODE is activated	When LPMODE is active (i.e. BURTC_STATUS_LPMODEACT is high), software reads might result in wrong value being read from BURTC_CNT.	Before reading BURTC_CNT, disable LPMODE and wait for BURTC_STATUS_LPMODEACT to be cleared before reading BURTC_CNT.
CMU_E108	**LFxCLKEN write** First write to LFxCLKEN can be missed.	For devices with PROD_REV < 15, enabling the clock for LFA/LFB after reset and then immediately writing LFACLKEN/LFBCLKEN, may cause the write to miss its effect.	For devices with PROD_REV < 15, make sure CMU_SYNCBUSY is not set before writing LFACLKEN/LFBCLKEN. Can temporarily switch to HFCORECLKLEDIV2 to speed up clearing synchbusy.
CMU_E110	**LFXO phase shift** Transients on pin D8 cause LFXO phase shift.	Transients on pin D8 can give a temporary phase shift on LFXO. Frequency is unchanged.	No known workaround.
CMU_E111	**LFXO configuration incorrect** LFXO configuration incorrect.	For devices with PROD_REV < 15, LFXOBUFCUR in CMU_CTRL is default 0 and LFXOBOOST in CMU_CTRL is default 1. However, these values are incorrect.	On devices with PROD_REV < 15, change LFXOBUFCUR to 1 and LFXOBOOST to 0.
CMU_E112	**LFXO boost buffer current setting**	LFXO will not work properly with LFXOBUFCUR in CMU_CTRL set.	Do not set LFXOBUFCUR in CMU_CTRL.

ID	Title/Problem	Effect	Fix/Workaround
	LFXO boost buffer current must be disabled		
CMU_E113	**LFXO startup at high temperature** LFXO does not start at high temperature with default configuration.	For devices with PROD_REV = 16, LFXO may have startup issues with low capacitance crystals when using the default LFXO configuration.	Make this line of code part of your starup code, typically in the start of main(): *((volatile uint32_t*) 0x400c80C0) = (*((volatile uint32_t*) 0x400c80C0) & ~(1<<6)) | (1<<4);.
CMU_E114	**Device not waking up from EM2 when using prescaled non-HFRCO oscillator as HFCLK**	If the device is running from any prescaled oscillator other than HFRCO as HFCLK and HFRCO is disabled, the device will not wake up from EM2.	Before entering EM2, clear CMU_CTRL_HFCLKDIV. Alternatively, enable HFRCO by setting CMU_OSCENCMD_HFRCOEN and wait until CMU_STATUS_HFRCORDY is set.
CUR_E103	**Increased EM2 current** Increased consumption in EM2	Current consumption in EM2 and EM3 has two stable states, the normal state (1200 nA and 900 nA for EM2 and EM3 respectively) and an error state. In the error state the current consumption in EM2 and EM3 is typically 4.5 uA at 25C (manufacturing test limits is set to 7 uA) but will increase with increased temperature. At 85C the error state EM2 and EM3 current consumption is typically 25 uA. It is unpredictable which state the device will go into on EM2/EM3 entry and it can also change state during operation.	No known workaround.
CUR_E105	**Increased current on AVDD2** Increased current on AVDD2	An increased current on AVDD2 can appear due to a floating internal node. This leakage is typically less than 10 uA, but can also rise to around 300 uA. The leakage is present in all energy modes.	To reduce this leakage to a few hundred nanoamps, set MODE10 and MODE11 in GPIO->P[5].MODEH to GPIO_P_MODEH_MODE10_PUSHPULL and GPIO_P_MODEH_MODE11_PUSHPULL respectively, and make sure bits 10 and 11 in GPIO->P[5].DOUT are set. To ensure GPIO->P[5] bits 10 and 11 stay set in EM4, set EM4RET in GPIO_CTRL to turn on GPIO retention before entering EM4.
DAC_E109	**DAC output drift over lifetime** The voltage output of the DAC might drift over time.	When the device is powered and the DAC is disabled, stress on an internal circuit node can cause the output voltage of the DAC to drift over time, and in some cases may violate the $V_{DACOFFSET}$ specification. If the DAC is always enabled while the device is powered, this condition cannot occur.	Both in the startup initialization code and prior to disabling the DAC in application code, set the OPAnSHORT bit in DACn_OPACTRL to a '1' for the corresponding DAC(s) used by the application. This will prevent the output voltage drift over time effect.
DI_E101	**Flash Page Size** The MEM_INFO_PAGE_SIZE value stored in Device Information (DI) Page is incorrect.	For devices with PROD_REV values lower than 18, the MEM_INFO_PAGE_SIZE register value in the Device Information Page is incorrect.	Use fixed flash page size of 4k bytes.
DMA_E101	**EM2 with WFE and DMA**	In EM2, when sleeping with WFE (Wait for Event), an interrupt from the DMA will not wake up the system.	Use WFI (Wait for Interrupt) or EM1 instead.

ID	Title/Problem	Effect	Fix/Workaround
	WFE does not work for the DMA in EM2.		
EBI_E101	**EBI masking functionality** EBI masking functionality is not limited to bank selected for TFT.	EBI masking functionality is not limited to the bank selected for TFT (by BANKSEL field in EBI_TFTCTRL). When masking is enabled, a mask match can be generated and suppress writes to any bank.	Disable masking when doing writes that should not be affected.
EBI_E102	**EBI access fails** Certain EBI accesses via the Cortex and Debug interface do not work.	Any access from the Cortex to the EBI not aligned to its size does not work. Also, only word accesses from the debug interface works.	Make sure all accesses via the Cortex are aligned to its size, and that all debug accesses are word accesses.
EBI_E103	**Page mode read in D16A16ALE mode** Page mode read in D16A16ALE mode skips RDSETUP stage for page mode accesses.	Page mode read in D16A16ALE mode skips RDSETUP stage for page mode accesses, making the read process go directly from ADDRSETUP to RDPA.	To compensate for the missing hold time related to the ALE address latch, the HALFALE field in EBI_ADDRTIMING can be enabled providing a 1/2 cycle hold time.
EMU_E105	**Debug unavailable during DMA processing from EM2** The debugger cannot access the system processing DMA request from EM2.	DMA requests from the LEUART can trigger a DMA operation from EM2. While waiting for the DMA to fetch data from the respective peripheral, the debugger cannot access the system. If such a DMA request is not handled by the DMA controller, the system will keep waiting for it while denying debug access.	Make sure DMA requests triggered from EM2 are handled.
EMU_E107	**Interrupts during EM2 entry** An interrupt from a peripheral running from the high frequency clock that is received during EM2 entry will cause the EMU to ignore the SLEEPDEEP-flag.	During EM2 entry, the high frequency clocks that are disabled during EM2 will run for some clock cycles after WFI is issued to allow safe shutdown of the peripherals. If an enabled interrupt is requested from one of these non-EM2 peripherals during this shutdown period, the attempt to enter EM2 will fail, and the device will enter EM1 instead. As a result the pending interrupt will immediately wake the device to EM0.	Before entering EM2, disable all high frequency peripheral interrupts in the core.
ETM_E101	**ETM Trace Clock** ETM Trace Clock needs to be delayed.	ETM trace clock is out of phase making the data transition occur at the same time as the ETM trace clock transitions.	ETM trace clock needs to be delayed between 10 ns and 1/4 of the trace clock period.
GPIO_E101	**GPIO wakeup from EM4** On GPIO wakeup from EM4 all cause bits for high-polarity wakeup pins are set.	All EM4 wakeup cause bits for EM4 wakeup pins with high polarity are set on wakeup.	Use low polarity if possible. For active high, slow changing inputs, a solution is to sample the inputs on wakeup.

ID	Title/Problem	Effect	Fix/Workaround
LES_E101	**LESENSE and Schmitt trigger** Schmitt trigger cannot be disabled on pins used for sensor excitation	When using LESENSE to excite a pin, the pin has to be configured in push-pull mode, which also enables the Schmitt trigger. If this pin has an input voltage somewhere in between 0.3*VDD and 0.7*VDD, the Schmitt trigger will consume a considerable ammount of current.	Keep the input voltage to pins configured as push-pull outside the range 0.3*VDD to 0.7*VDD when LESENSE is not interacting with the connected sensor.
LES_E102	**LESENSE and DAC CH1 configuration** LESENSE cannot control DAC CH1 if DACCH0CONV in LESENSE_PERCTRL is set to DISABLE.	LESENSE control of DAC CH1 cannot be enabled if DACCH0CONV in LESENSE_PERCTRL is set to DISABLE.	Configure DACCH0CONV in LESENSE_PERCTRL to anything but DISABLE, this enables DAC CH1 to be controlled properly. If DAC CH0 is not to be used, set DACCH0OUT in LESENSE_PERCTRL to DISABLE. This will disable LESENSE control of DAC CH0, but still allow LESENSE to control DAC CH1.
LES_E103	**AUXHFRCO and LESENSE** LESENSE will not work properly at low AUXHFRCO frequencies.	LESENSE will not work properly when used with the AUXHFRCO running at the 1 or 7 MHz band.	Do not use a AUXHFRCO frequency band of 1 or 7 MHz when used in combination with LESENSE.
MSC_E101	**Prefetch unreliable** Prefetch unreliable.	When prefetch is enabled, i.e. the PREFETCH bit (bit 8) is set in MSC_READCTRL, wrong instruction data can be prefetched causing system failure.	Do not enable prefetch. Prefetching is disabled by default.
OPA_E101	**Opamp 2 startup rampup** When OPA2 is started the output rampup is constant independent of bias setting.	When OPA2 is started the output rampup is constant independent of bias setting.	No known workaround.
PCNT_E102	**PCNT Pulse Width Filtering does not work**	The PCNT Pulse Width Filter does not work as intended.	Do not use the pulse width filter, i.e. ensure FILT = 0 in PCNTn_CTRL.
PRS_E101	**Edge detect on GPIO/ACMP** Edge detect on peripherals with asynchronous edges might be missed.	When using edge detect in PRS on signals from ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP and BURTC edges can be missed.	Do not use edge detect on ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP and BURTC.
TIMER_E103	**Capture/compare output is unreliable with RSSCOIST enabled** The TIMER capture/compare output is unreliable when RSSCOIST is enabled and the clock is prescaled.	When RSSCOIST is set and PRESC > 0 in TIMERn_CTRL, the capture/compare output value is not reliable.	Do not use a prescaled clock, i.e. ensure PRESC = 0 in TIMERn_CTRL when RSSCOIST is enabled.

ID	Title/Problem	Effect	Fix/Workaround
USART_E112	**USART AUTOTX continues to transmit even with full RX buffer** USART AUTOTX continues to transmit even with full RX buffer.	When AUTOTX in USARTn_CTRL or AUTOTXEN in USARTn_TRIGCTRL is set, the USART will continue to transmit data even after the RX buffer is full. This may cause the RX buffer to overflow if the data is not read out in time.	No known workaround.

2 Revision History

2.1 Revision 1.20

April 8th, 2016

Updated the latest revision to revision E.

Removed BURTC_E102, BU_E106, CMU_E114, DI_E101, EMU_107, and LES_E103 from revision E.

2.2 Revision 1.10

February 20th, 2015

Added DAC_E109.

Added EMU_E107.

Added TIMER_E103.

Added PCNT_E102.

Updated link to errata for older revisions.

Corrected typos.

2.3 Revision 0.70

March 26th, 2014

Corrected typos in document.

2.4 Revision 0.60

August 21st, 2013

Added ADC_E117.

Added AES_E102.

Updated disclaimer, trademark and contact information.

2.5 Revision 0.50

July 30th, 2013

Added AES_E101.

Added BURTC_E102.

Added CMU_E114.

Added DMA_E101.

Updated errata naming convention.

2.6 Revision 0.40

June 5th, 2012

Added ADC1.

Added DI1.

2.7 Revision 0.30

April 24th, 2012

Added BU6.

Added CMU4.

Added CMU5.

Added LES3.

Updated CMU3.

2.8 Revision 0.20

January 20th, 2012

Updated CUR5.

2.9 Revision 0.10

January 9th, 2012

Initial preliminary release.

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