Mighty Gecko
EFR32MG21 Errata

This document contains information on the EFR32MG21 errata. The latest available revision of this device is revision B.

For errata on older revisions, refer to the errata history section for the device. The revision information is typically specified in or near the trace code on the device. Refer to the package marking information in the data sheet for more information.

Errata effective date: April, 2019.

1. Active Errata Summary

These tables list all known errata for the EFR32MG21 and all unresolved errata in revision B of the EFR32MG21.

Table 1.1. Errata History Overview

Designator	Title/Problem	Exists on Revision:	
		A	B
CUR_E301	AVDD/IOVDD to DVDD Leakage Current	X	—
GPIO_E301	GPIO_PORTA_MODEL_MODE2 Write Affects SWDIO Pin During Active Debug	X	—
GPIO_E302	Increased Leakage Current When EM4WU Pins Are Enabled and the Pin State Is High	X	X
HFXO_E301	HFXO DISONDEMAND and FORCEEN Can Cause Device to Hang	X	X
I2C_E301	New Transfer Ignored if Bus Idle Timeout Occurs Between Start Detection and the Falling Edge of SCL	X	—
I2C_E302	Slave Holds SCL Low After Losing Arbitration	X	—
IADC_E301	Delta Sigma Modulator is Disabled in KEEPWARM Mode	X	—
IADC_E302	EM23ABORTERROR Interrupt Does Not Work	X	—
IADC_E303	Input Change Missed After Adjacent GND Conversions	X	—
IADC_E304	Possible Data Loss in EM2/EM3	X	X

Table 1.2. Active Errata Status Summary

Errata #	Designator	Title/Problem	Workaround Exists	Affected Revision	Resolution
1	GPIO_E302	Increased Leakage Current When EM4WU Pins Are Enabled and the Pin State Is High	Yes	B	—
2	HFXO_E301	HFXO DISONDEMAND and FORCEEN Can Cause Device to Hang	Yes	B	—
3	IADC_E304	Possible Data Loss in EM2/EM3	Yes	B	—

2. Detailed Errata Descriptions

2.1 GPIO_E302 – Increased Leakage Current When EM4WU Pins Are Enabled and the Pin State Is High

Description of Errata
When any of the EM4WU pins are used with the input path enabled and the pin state is high, an extra leakage current of approximately 15 µA per pin will be observed in EM0, EM1, EM2, and EM3.
Affected Conditions / Impacts
EM0, EM1, EM2, and EM3 current will be higher by approximately 15 µA per pin when any of the EM4WU pins are used with the input path enabled and the pin state is high.
Workaround
There are two workarounds for this issue: 1. If the input path on the pad is not required, disable the input path on that pad by setting the DINDIS or DINDISALT bits in the GPIO_PORTx_CTRL register. Thus, an EM4WU pin can still be used to drive an output without incurring the extra current leakage when the pin is configured as an output and DINDIS or DINDISALT is set. 2. If an input path is required (i.e. MODEn is any value other than DISABLED and DINDIS = 0 or DINDISALT = 0), assign it to a pin which does not have EM4 wakeup capability. Refer to the device data sheet to determine which pins have or do not have EM4 wake-up functionality.
Resolution
There is currently no resolution for this issue.

2.2 HFXO_E301 — HFXO DISONDEMAND and FORCEEN Can Cause Device to Hang

Description of Errata
When DISONDEMAND and FORCEEN in the HFXO_CTRL register are both 1, the HFXO causes a handshake between the EMU and the CMU to hang, which may prevent a system reset from being asserted.
Affected Conditions / Impacts
The device will hang waiting for the EMU/CMU handshake to complete, requiring a pin reset to recover.
Workaround
Do not set DISONDEMAND = 1 in HFXO_CTRL while the HFXO is enabled.
Resolution
There is currently no resolution for this issue.

2.3 IADC_E304 – Possible Data Loss in EM2/EM3

Description of Errata
When the IADC wakes from EM2 or EM3 and generates conversion results that the LDMA transfers to RAM, it is possible under very rare circumstances to lose data when the ratio of the bus clock (HCLK) is slow compared to the prescaled IADC clock (ADC_CLK).
Affected Conditions / Impacts
Data from IADC conversions in these cases can potentially be lost due to FIFO overflow.
Workaround
To prevent data loss when the IADC awakens from EM2 or EM3 and performs conversions that are serviced by the LDMA before re-entering the low-energy state, make sure that: • the rate at which the IADC takes samples in EM2 or EM3 is less than or equal to 125 kHz (samples are taken no faster than every 8 µs), and • the frequency of the HCLK (bus clock) is at least four times the frequency of the IADCCLK.
Resolution
There is currently no resolution for this issue.

3. Errata History

This section contains the errata history for EFR32MG21 devices.

For errata on the latest revision, refer to the beginning of this document. The device data sheet explains how to identify chip revision, either from package marking or electronically.

3.1 Errata History Summary

This table lists all resolved errata for the EFR32MG21.

Table 3.1. Errata History Status Summary

Errata #	Designator	Title/Problem	Workaround Exists	Affected Revision	Resolution
1	CUR_E301	AVDD/IOVDD to DVDD Leakage Current	Yes	A	B
2	GPIO_E301	GPIO_PORTA_MODEL_MODE2 Write Affects SWDIO Pin During Active Debug	Yes	A	B
3	I2C_E301	New Transfer Ignored if Bus Idle Timeout Occurs Between Start Detection and the Falling Edge of SCL	Yes	A	B
4	I2C_E302	Slave Holds SCL Low After Losing Arbitration	Yes	A	B
5	IADC_E301	Delta Sigma Modulator is Disabled in KEEPWARM Mode	Yes	A	B
6	IADC_E302	EM23ABORTERROR Interrupt Does Not Work	No	A	B
7	IADC_E303	Input Change Missed After Adjacent GND Conversions	No	A	B

3.2 Detailed Errata Descriptions

3.2.1 CUR_E301 – AVDD/IOVDD to DVDD Leakage Current

Description of Errata
Leakage from AVDD or IOVDD to DVDD is present when either supply voltage is higher than DVDD.
Affected Conditions / Impacts
When the AVDD or IOVDD supply voltage is higher than DVDD, a leakage current from AVDD or IOVDD to DVDD is present. This current has a diode like property, such that when the voltage difference is less than 700 mV, the leakage is less than 1 µA. If the difference is near the maximum (e.g. AVDD = 3.8V and DVDD = 1.8V), the leakage can be as high as 100 µA on a typical device at room temperature. In this case, there is also as much as 50 µA of added current from AVDD or IOVDD directly to ground.
Workaround
Enable the AVDD and/or IOVDD brownout detector via the EMU_BOD3SENSE register for the supply voltage(s) that is/are higher than DVDD. • Enable the AVDD monitor by performing a read-modify-write operation on the EMU_BOD3SENSE with 0x1 as the bit mask. • Enable the IOVDD monitor by performing a read-modify-write operation on the EMU_BOD3SENSE with 0x6 as the bit mask. Note that enabling the relevant brownout detector minimizes this leakage current, but it does not eliminate it completely.
Resolution
This issue is resolved in revision B devices.

3.2.2 GPIO_E301 – GPIO_PORTA_MODEL_MODE2 Write Affects SWDIO Pin During Active Debug

Description of Errata
When a debugger is connected to the device, software cannot clear GPIO_DBGROUTEPEN in order to prevent loss of communication with the host. However, changing the GPIO_PORTA_MODEL_MODE2 field, which corresponds to the SWDIO pin, to any of the wired-AND/wired-OR modes, effectively disables the debugger connection.
Affected Conditions / Impacts
Reconfiguring the SWDIO pin to a wired-AND/wired-OR output mode causes loss of debugger contact upon writing to the GPIO_PORTA_MODEL_MODE2 field.
Workaround
To prevent the debugger from losing its connection to the target device, do not change the state of the GPIO_PORTA_MODEL_MODE2 field.
Resolution
This issue is resolved in revision B devices.

3.2.3 I2C_E301 – New Transfer Ignored if Bus Idle Timeout Occurs Between Start Detection and the Falling Edge of SCL

Description of Errata
If a bus idle timeout occurs between detection of a start condition and the falling edge of SCL, the start condition detection logic is defeated, causing the I^2C state machine to indicate that bus is not busy (I2C_STATE_BUSY = 0).
Affected Conditions / Impacts
A transfer that meets the timing conditions cited above will be missed, causing the device not to respond to the master if it is the slave being addressed. Furthermore, because I2C_STATE_BUSY no longer reflects the actual state of the bus, the device can, if configured as a master, mistakenly attempt to use the bus, thus corrupting a transfer already in progress.
Workaround
To avoid corrupting bus activity, application software should implement the following before starting a transaction in systems where the bus timeout is used: • Wait for the I2C_IF_SSTOP flag, either by polling or by using the associated interrupt (I2C_IEN_SSTOP). • Impose a system-defined delay after all transfers that are independent of the bus timeout monitor to ensure that the bus is in idle state. When one of the above workarounds is met, the bus can be considered inactive and available for use.
Resolution
This issue is resolved in revision B devices.

3.2.4 I2C_E302 – Slave Holds SCL Low After Losing Arbitration

Description of Errata
If, while transmitting data as a slave, arbitration is lost, SCL is unintentionally held low for an indefinite period of time.
Affected Conditions / Impacts
The winner of arbitration cannot use the bus because SCL is never released.
Workaround
If the I^2C arbitration lost flag is asserted (I2C_IF_ARBLOST = 1) in slave mode (I2C_STATE_MASTER = 0), application software needs to wait for at least one SCL high time and then issue the transmission abort command (set I2C_CMD_ABORT = 1), thus releasing SCL.
Resolution
This issue is resolved in revision B devices.

3.2.5 IADC_E301 – Delta Sigma Modulator is Disabled in KEEPWARM Mode

Description of Errata
When IADC_CTRL_WARMUPMODE = KEEPWARM, the IADC delta sigma modulator is disabled between conversions.
Affected Conditions / Impacts
Because the delta sigma modulator is disabled before conversions restart, the results will be erroneous until the usual 1 µs required for warm-up has elapsed.
Workaround
Do not use IADC_CTRL_WARMUPMODE = KEEPWARM or discard the results received during the first 1 µs of operation after restarting the converter.
Resolution
This issue is resolved in revision B devices.

3.2.6 IADC_E302 – EM23ABORTERROR Interrupt Does Not Work

Description of Errata
When IADC_IEN_EM23ABORTERROR = 1, the IADC does not request an interrupt upon EM2 or EM3 entry when running from a clock that is not active in these energy modes.
Affected Conditions / Impacts
There is no way for the IADC to let application software know that the system has (erroneously) entered EM2 or EM3 with a converter clock source that is now disabled.
Workaround
There is currently no workaround for this issue.
Resolution
This issue is resolved in revision B devices.

3.2.7 IADC_E303 – Input Change Missed After Adjacent GND Conversions

Description of Errata
If the IADC is performing a scan that includes two adjacent GND conversions (IADC_SCAN[n]_PORTPOS = IADC_SCAN[n]_PORTNEG = GND and IADC_SCAN[n + 1]_PORTPOS = IADC_SCAN[n + 1]_PORTNEG = GND) such that the configuration for one GND conversion differs from the other (e.g. IADC_SCAN[n]_CFG = 0 and IADC_SCAN[n + 1]_CFG = 1 or vice versa), the inputs for conversion [n + 2] in the sequence after the two GND conversions will not be selected.
Affected Conditions / Impacts
Results for the first conversion after two adjacent GND conversions in a scan will be erroneous.
Workaround
Do not perform scans that include two adjacent GND conversions.
Resolution
This issue is resolved in revision B devices.

4. Revision History

Revision 0.3

April, 2019

- Added GPIO_E302 and HFXO_E301.

Revision 0.2

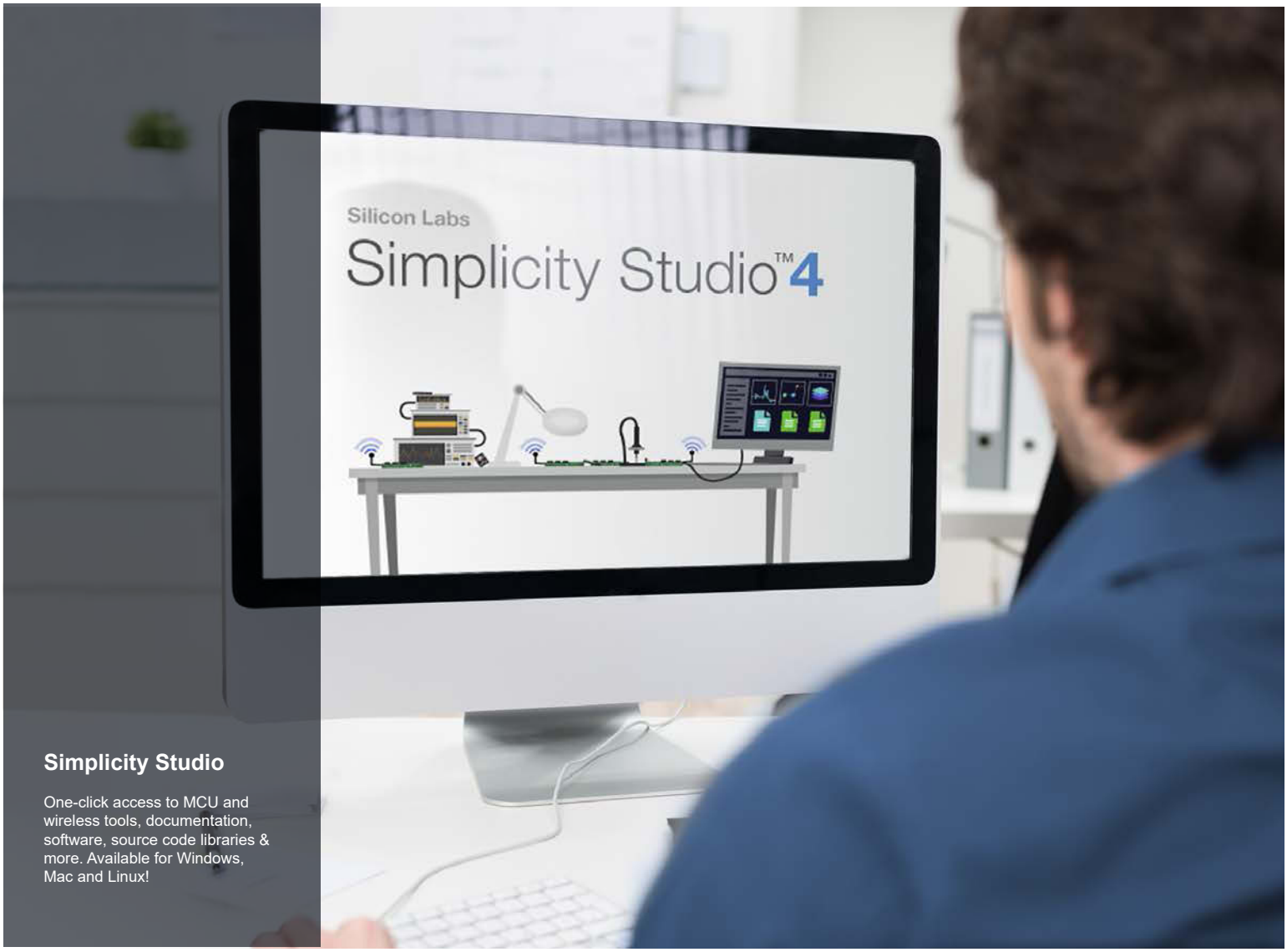
December, 2018

- Updated for device revision B.
- Added IADC_E303 and IADC_E304.
- CUR_E301, GPIO_E301, I2C_E301, I2C_E302, IADC_E301, IADC_E302, and IADC_E303 resolved and moved to Errata History.

Revision 0.1

May, 2018

- Initial release.



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