EM359x Reference Design With 0805 Ceramic Balun Front End, USB, 4-Layer

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1.	Cover Page
2.	Block Diagrams
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This design is intended for use as a reference for custom designs utilizing EM359x ZigBee radios which include the USB option and EM359x ZigBee radios which do not. Some of the connections shown in this design are different from other Silicon Labs EM35xx ZigBee reference designs which do not include USB. If you are unsure about use of the USB option or if you know your design will not require USB, please contact your region's Silicon Labs Sales Office for assistance with choosing the appropriate EM35xx ZigBee products, features and the corresponding reference design.

Click on the following links below for additional information regarding EM35xx ZigBee products and for the location of the nearest Silicon Labs Sales office;

EM35xx ZigBee Product Information

Silicon Labs Sales Office Locations

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MCU & Wireless WMN Support

Title: EM359x/0805 Ceramic Balun W/USB Reference Design	
Part Number: 130-0859-001	Rev: A0
Sheet Name: 1_EM359x-REF-DES-CER-USB_Cover.SchDoc	
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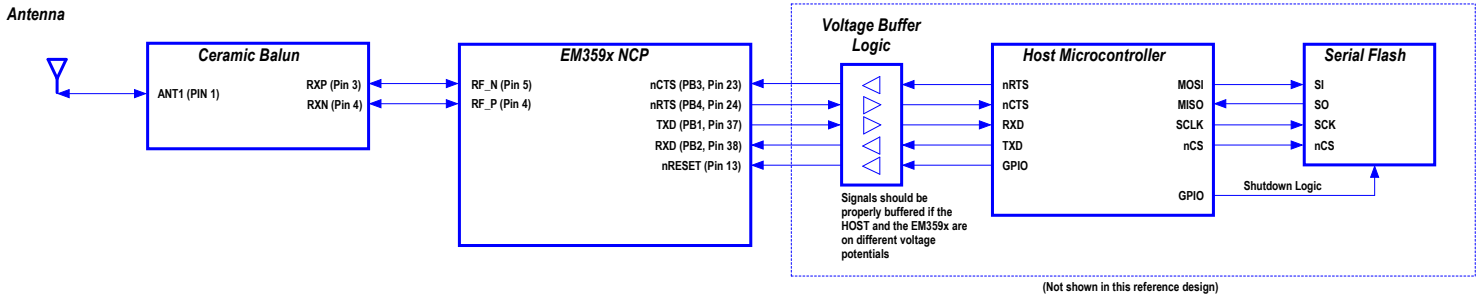
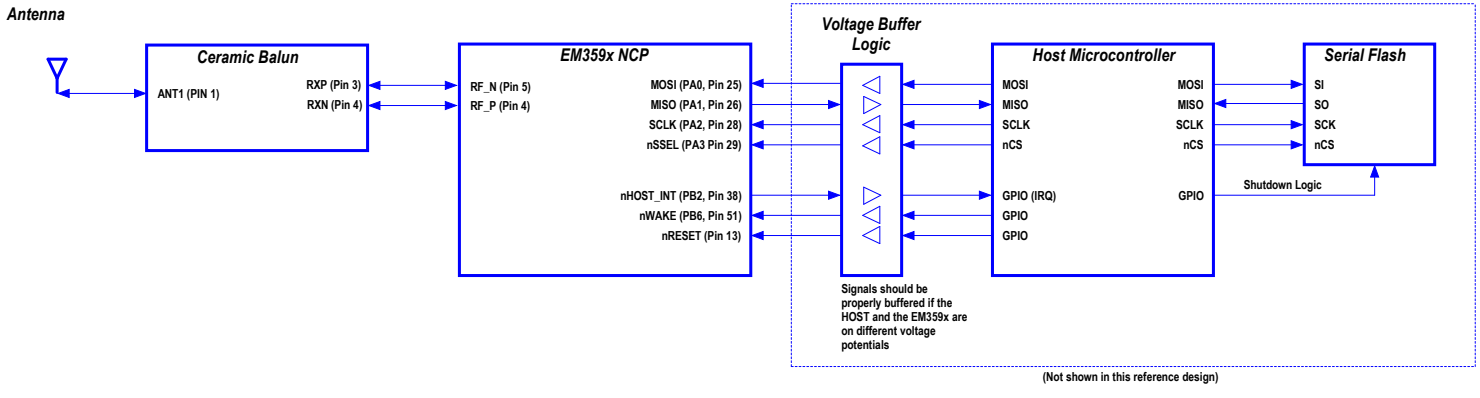
The schematics in this package can be used in both NCP & SOC designs involving the EM359x. Connect NCP to the HOST using either UART or SPI serial connection as shown below.

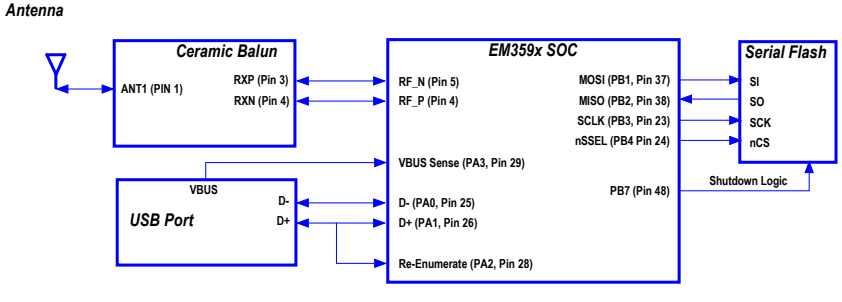
EM359x NCP with EZSP over Asynchronous Serial (UART)



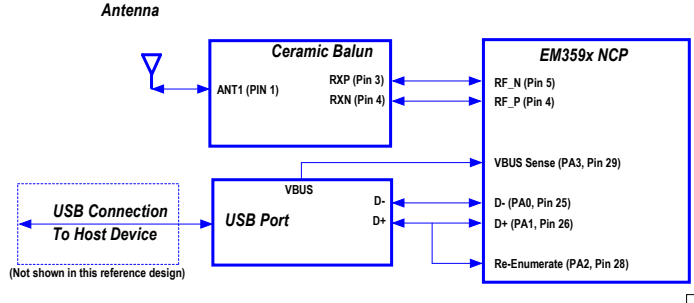
EM359x NCP with EZSP over Synchronous Serial (SPI)



EM359x SOC Reference Design, (USB Option Shown)



EM359x USB NCP Reference Design



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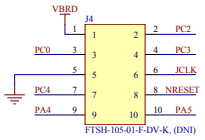
Packet Trace Port (Optional)

The J4 Packet Trace Port interface footprint, sized for a 10 pin dual row 0.05" pitch connector compatible with a Samtec FFSD series ribbon cable, (FFSD-05-D-12.00-01N), is required to make use of Ember Desktop software tools by enabling a direct connection to an Ember Debug Adapter (ISA3). This part can be optionally made 'Do Not Install' in production.



EM359x Zigbee SOC

High-Performance, Integrated ZigBee/802.15.4 System-on-Chip Solution with an internal 32-bit ARM CORTEX-M3 core processor with up to 64K of internal RAM and up to 512K of internal FLASH and AES128 encryption accelerator in a 8 x 8 mm QFN-56 package.

nRESET

nRESET (pin 12) has an internal glitch filter. External filter components are not required.

32.768KHz Clock source (Optional)

If precision sleep timing is not required, use the internal RC clock source. Designs requiring precision sleep timing use PC6 and PC7 for the 32.768 KHz clock. Populate Y2, C8 and C9 only for applications having a need for precise sleep timer requirements, or populate R14 and R15 for using PC6 and PC7 as GPIO. Alternately, a precision timer clock module can be utilized in place of the crystal, using PC7 as the input for the clock.

32.768KHz PCB Layout Note

In order to reduce crystal loop currents from coupling through the ground plane to the radio, Silicon Labs recommends the crystal shunt capacitors (C8 and C9) share a ground via and be geographically located close to each other and to Y2, thereby keeping loop current paths as short as possible.

0805 Zigbee Front End Ceramic Balun

The Ceramic Balun Reference Design incorporates a 100 ohm differential port with DC bias, to 50 ohm single ended port, ceramic balun in a standard 0805 package. An impedance tuning inductor, DC bias decoupling capacitor and harmonic filter are required elements in this design. The RF trace is a grounded coplanar waveguide, using a 29.67mil track width, 16mil gap width, and 16mil dielectric thickness. Given the dielectric constant of 4 at 2.4GHz, this yields a characteristic impedance of 53.12 ohms (close to 50 ohms).

Recomended Ceramic Balun Options

Balun Manufacturer	Balun Part Number	L3 Tuning Inductor
WURTH ELEKTRONIC	748421245	TBD
WURTH ELEKTRONIC	748420245	TBD
JOHANSON	2450BL15B100E	TBD
MURATA	LDB212G4010C-001	TBD
TDK	HHM1520	TBD

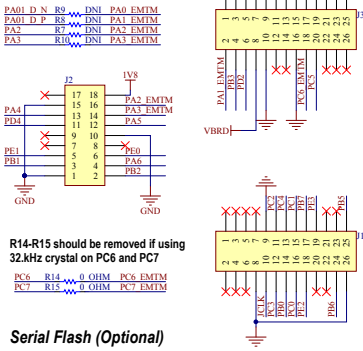
1V25_CORE Component Note

A ceramic capacitor (C3) with a minimum value of 1uF between pin 18 and ground is required for cost effective 1V25_CORE voltage regulator output stability.

Board to Board Interface (Optional)

The J1-J3 connector interface is not required for customer designs and is a through-hole 0.1" pitch header arrangement. J1, J2 and J3 can be optionally made 'Do Not Install', or replaced with a different board to board interface arrangement, or removed entirely to facilitate a merger into an already existing PCB layout design.

Install R7-R10 only if USB circuit is not installed and SC2 access is required via the board to board interface



Serial Flash (Optional)

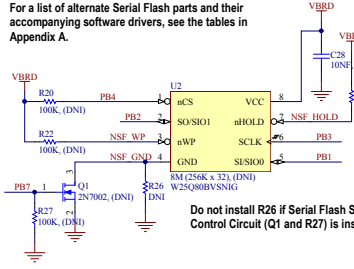
Serial Flash is required for Over The Air (OTA) Bootloader support as mandated by some applications of the ZigBee profiles but can be optionally made 'Do Not Install' for any end use application not requiring OTA Bootloader support.

This design uses 8 Mb Serial Flash to support 512 kB OTA. Smaller memory EM35xx devices can use smaller Serial Flash parts. For a list of alternate Serial Flash parts and their accompanying software drivers, see the tables in Appendix A.

For maximum power efficiency in custom application code, include firmware instructions to sleep the Serial Flash and any other peripherals prior to placing the EM359x in shutdown mode.

For applications utilizing the EM359x USB feature, connect the Serial Flash to Serial Controller 1, (SC1), as shown below. In applications where the USB feature is not utilized, the Serial Flash can be connected to Serial Controller 2, (SC2).

For a list of alternate Serial Flash parts and their accompanying software drivers, see the tables in Appendix A.



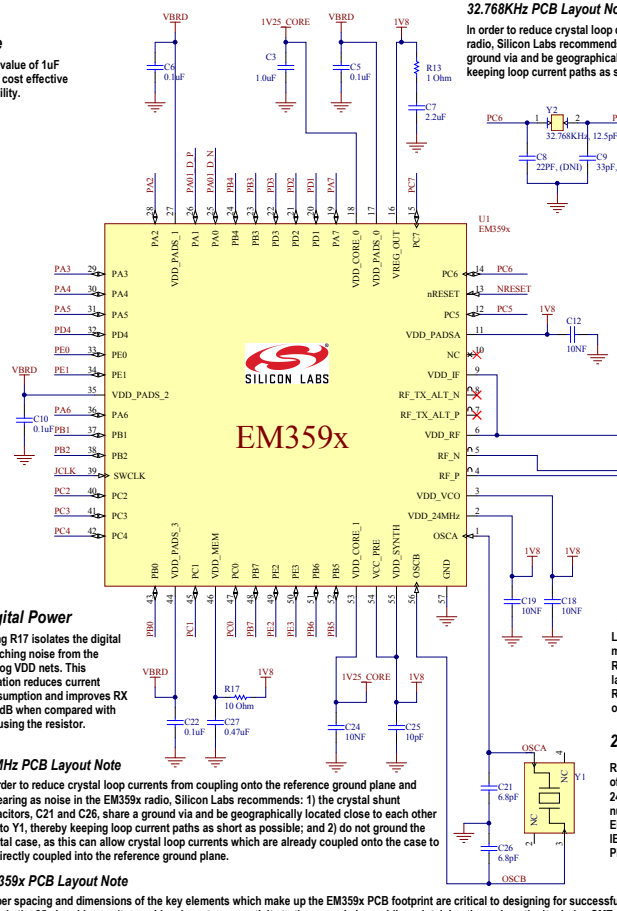
Do not install R26 if Serial Flash Shutdown Control Circuit (Q1 and R27) is installed.

Serial Flash Shutdown Control (Optional)

The EM359x SOC reference design uses PB7 to enable or disable Q1 for the purpose of controlling current consumed by the Serial Flash when not in use, however, any GPIO can be utilized for this purpose. Q1 and R27 can be optionally made "Do Not Install" if overall power efficiency is not a requirement.

Shutdown signaling for the Serial Flash and other peripherals can be tied to a single GPIO for applications not requiring a separate control signal for each.

A custom OTA Application Bootloader file with the command line EEPROM_USES_SHUTDOWN_CONTROL defined in the header file, is required for designs using the Serial Flash shutdown control.



Digital Power

Using R17 isolates the digital switching noise from the analog VDD nets. This isolation reduces current consumption and improves RX by 2dB when compared with not using the resistor.

24MHz PCB Layout Note

In order to reduce crystal loop currents from coupling onto the reference ground plane and appearing as noise in the EM359x radio, Silicon Labs recommends: 1) the crystal shunt capacitors, C21 and C26, share a ground via and be geographically located close to each other and to Y1, thereby keeping loop current paths as short as possible; and 2) do not ground the crystal case, as this can allow crystal loop currents which are already coupled onto the case to be directly coupled into the reference ground plane.

RF 1V8 PCB Layout Note

Keep 1V8 trace between EM359x RF pins 6 and 9, ceramic balun DC Bias pin 2 and all attached decoupling, as short as possible on a single layer.

Decoupling for the RF 1V8 trace (C14) should be placed close to the ceramic balun DC Bias pin 2.

RF Tuning Circuit

L3 is required for impedance matching between the EM359x and the RF Front End circuit. Changes in PCB layout between the EM359x and the RF Front End will result in a value other than shown here.

24MHz Clock Source

Refer to the tables in Appendix B of this schematic for a list of 24MHz crystal manufacturer part numbers known to work with the EM359x in compliance with the IEEE 802.15.4 symbol rate +/- 40 PPM specification.

EM359x PCB Layout Note

Proper spacing and dimensions of the key elements which make up the EM359x PCB footprint are critical to designing for successful manufacturability. These key elements include the 25 via grid array (to provide adequate connectivity to the ground plane while maintaining thermal continuity during SMT reflow), the paste mask array, the solder mask dimensions, and the package dimensions.

1. Refer to section 6.1, "Packaging", in the EM359x datasheet for PCB footprint mechanical details, which includes the Soldermask layer critical dimensions.
2. The EM359x is a QFN device which does not provide a direct ground pad connection to the PCB component layer. Instead, the ground connection is achieved through a 5 x 5 via grid array to a sub layer reference ground plane (layer 2 in this reference design).
3. For optimal noise suppression on VDD nets, each decoupling capacitor should be placed as close to its VDD pin as possible.
4. To further optimize noise suppression, route serially from the VDD source trace/via to the pad for the decoupling capacitor, then to the EM359x VDD pad.
5. Do not share ground vias between decoupling capacitors (note exception for crystal circuits).
6. The reference ground plane between EM359x ground pad vias and decoupling capacitor ground vias is to be kept unbroken by traces and/or other net vias.
7. Similarly, the reference ground plane between the EM359x ground pad vias and full RF path including balun and antenna circuit is to be kept unbroken by traces and/or other net vias.
8. Star route 1V8 target power pins from the EM359x VREG_OUT to take advantage of inductive filtering characteristics of copper traces.
9. Keep component layer ground plane pours disconnected from all parts of the EM35xx circuit to ensure AC noise is decoupled to the EM35xx reference ground plane and not to the component layer plane. Additionally, if stitching vias cannot be added between the component layer ground plane and the reference ground plane in any specific area, the component layer ground pour in this area should be removed as it will be a potential radiated noise generator otherwise.
10. Avoid creating ground "islands" for all ground plane pour areas to prevent localized impedances that may result in radiated emissions.
11. Avoid routing traces between the QFN component ground vias to prevent AC noise or ESD on the traces from coupling directly to the internal EM359x RF block.
12. Flood over instead of using thermals for the vias under the EM35xx to prevent the thermal spoke impedances from isolating the QFN device from the ground plane at radio frequencies.
13. Top layer ground pour areas are required to be tightly stitched to the reference ground, especially around the parameters and specifically at the pour area corners and uneven contours.

Ceramic Balun PCB Layout Notes

Duplicate as closely as possible all aspects of the Ceramic Balun Circuit PCB layout provided in the reference design .PcbDoc file and gerbers. Proper spacing and placement of key elements which make up the Ceramic Balun Circuit are necessary for successful manufacturability and for optimal RF performance. Key considerations include spacing of the balun from the EM359x, associated trace widths, ground plane layer to signal layer spacing, DC supply routing and via placement.

PCB Only

The symbols to the right list the PCB in the Bill of Materials and are used for identifying PCB silk screen and mechanical layer Logos within the Silicon Labs CAD tools. They are not required or intended for use in customer

Top Side Board Logo

Bottom Side Board Logo

Firmware Considerations

1. Refer to the EM359x Reference Manual, chapter 7, for GPIO configuration information.
2. Refer to Application Note AN710, Bringing Up Custom Devices for the EM359x SOC Platform, for setting the CIB tokens.
3. Set TOKEN_MFG_PHY_CONFIG value to 0xFFFE to enable the correct RF path and RX Boost mode for this reference design.

Harmonic Filter (Optional)

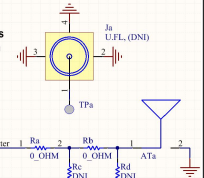
C15, C16, C17, L1, L2 make up a 5 element Harmonic filter which maximizes the conducted 2nd and 3rd order 802.15.4 band Harmonic margin for compliance with applicable governing regulatory requirements. Can be replaced with other types of filters, such as a ceramic band pass filter. Performance is sensitive to PCB parasitic impedances, therefore custom PCB layout should emulate the reference PCB layout attached to this design as closely as possible.

Typical RF Test Port with PCB Antenna Circuit Example

(for custom designs not utilizing the SMA RF connector interface)

Antenna Tuning Configuration:

Rb, Rc, and Rd are required for matching when the board impedances and antenna impedance are unknown or are not matched. Only two of the three elements will be required for matching, however the antenna impedance will determine whether or not Rc or Rd will be capacitive or inductively populated.



RF Test Port Configuration:

Normal operaton - Ra = 0 ohm

Radio Only - Ra.1 shorted to TPa

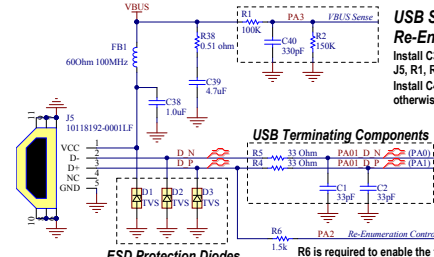
Antenna Tuning Only - Ra.2 shorted to TPa

RF Test Port (Optional)

An RF test port is required for characterization testing and tuning of the radio. This SMA connector can be replaced with a different RF test connector and/or antenna with pi structure matching circuit. Refer to other EM35xx reference designs for RF connector and antenna examples.

EM359x USB Application Circuit (Optional)

When USB is implemented, VBRD must always be equal to or greater than 3.0 volts.



R6 is required to enable the firmware to re-enumerate after deep sleep, a device Reset or a power cycling event.

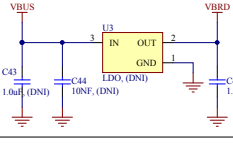
USB Self Powered Only Devices, Re-Enumeration

Install C38, C39, C40, C1, C2, D1, D2, D3, FB1, J5, R1, R38, R2, R4, R5, R6.

Install C40, R31, R2 for Self Powered only, otherwise DNI

EM359x USB Bus Powered Only Devices, Re-Enumeration

Install the Self Powered Only Circuit shown above, except for C40, R1, R2, and install the voltage regulator circuit, C43, C44, C45 and U3 shown below. C40, R37, R39 are not required for VBUS powered modules and should not be installed to prevent a potential power race condition on PA3.



USB PCB Layout Notes

1. Minimize trace lengths of the differential signals D+, D-.
2. Differential signal traces should be differentially impedance matched to 90 ohms.
3. Differential signals should have matching trace lengths.
4. Keep differential signal traces over the plane area of the ground plane layer.
5. Minimize the use of vias and corners when routing the differential signal traces.
6. If a 90 degree angle is necessary, use arcs or two 45 degree angles instead.
7. Keep differential signal traces isolated from any clock or similarly switching signals.
8. Follow rule of thumb keep-out by minimally maintaining 5 times trace width from all unrelated copper planes and traces.
9. Route terminating component pads in line or on top of the differential signal traces thereby avoiding trace stubs.
10. Differential signal termination components, C1, C2, R4, R5, should be placed as close as possible to the EM359x.
11. ESD and VBUS filter components should be placed as close as possible to the USB connector.

For additional information regarding using EM359x USB, refer to Application Note AN740, Using the Ember EM358x/EM359x USB.

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Appendix A: Approved Serial Flash Providers for the EM359x/0805 Ceramic Balun Front End 4-Layer Reference Design

Table 1 below provides details for Serial Flash devices intended for this Reference Design. Table 2 below provides details for Serial Flash devices which use an alternate pin-out different than the pin-out used in this reference design. For a complete list of Serial Dataflash devices supported by the Silicon Labs ZigBee software stack, refer to the Table 2. Supported Serial Dataflash/EEPROM Remote Memory Parts, in Application Note AN772, Using Application Bootloader.

Table 1: Silicon Labs Zigbee Serial Flash Vendor Parts List (Matching Pin-Out Used In This Design)

Manufacturer	Part Number	Description	Software Driver	Voltage Range
WinBond	W25X20BVSNIG	2M (256K x 8)	spiflash-class1.c	2.7-3.6V
WinBond	W25Q80BVSNIG	8M (256K x 32)	spiflash-class1.c	2.5-3.6V
Macronix	MX25L2006EM1I-12G	2M (2M x 1, 1M x 2)	spiflash-class1.c	2.7-3.6V
Macronix	MX25L8006EM1I-12G	8M (8M x 1, 4M x 2)	spiflash-class1.c	2.7-3.6V
Atmel/Adesto	AT25DF041A-SSH-B	4M (4M x 1, 2M x 2)	spiflash-class1.c	2.7-3.6V
Atmel/Adesto	AT25DF041A-SSHF-B	4M (4M x 1, 2M x 2)	spiflash-class1.c	2.3-3.6V
Atmel/Adesto	AT25DF081A-SSH-B	8M (8M x 1, 4M x 2)	spiflash-class1.c	2.7-3.6V
Atmel/Adesto	AT25DF081A-SSHF-B	8M (8M x 1, 4M x 2)	spiflash-class1.c	2.3-3.6V
Micron	M25P20-VMN6TPB	2M (2M x 1, 1M x 2)	spiflash-class1.c	2.3-3.6V
Micron	M25P40-VMN6TPB	4M (4M x 1, 2M x 2)	spiflash-class1.c	2.3-3.6V
Micron	M25P80-VMN6TPB	8M (8M x 1, 4M x 2)	spiflash-class1.c	2.7-3.6V
Micron	M25P16-VMN6TPB	16M (16M x 1, 8M x 2)	spiflash-class1.c	2.7-3.6V

Table 2: Silicon Labs Zigbee Serial Flash Vendor Parts List (Alternate Pin-Out Not Used in This Design)

Manufacturer	Part Number	Description	Software Driver	Voltage Range
Atmel/Adesto	AT45DB021E-SSHN-T	2M (256K x 8)	at45db021d.c	1.65-3.6V
Micron	M45PE20-VMN6TP	2M (256K x 8)	m45pe20.c	2.7-3.6V
Macronix	MX25L2006EM1I-12G	2M (2M x 1, 1M x 2)	spiflash-class1.c	2.7-3.6V
Macronix	MX25L8006EM1I-12G	8M (8M x 1, 4M x 2)	spiflash-class1.c	2.7-3.6V

Appendix B: Suggested 24MHz Crystal Providers for the EM359x/0805 Ceramic Balun Front End 4-Layer Reference Design

The tables below provide details for 24MHz crystal devices which can be used with EM359x series ZigBee products for the manufacture of ZigBee radio devices. Check with your preferred crystal vendor for the latest updates on their product offering or for additional information about crystals for the EM359x ZigBee products in your target application.

Table 3: Suggested 24MHz ZigBee Crystal Vendor Parts List for Crystal Packages Used in this design

Manufacturer	Part Number	Package Size	Frequency Tol	Temperature Stability	Aging	Total Frequency Tol	ESR	Load Capacitance	Tuning Capactor
Abracon	ABM8-24.000MHZ-R60-D-1-W-T	3.2 x 2.5 x 0.7mm	+/- 10 ppm	+/- 25 ppm (-40 +85)	+/- 3 ppm/First year max @ +25		60 ohms	18pF	22pF
Abracon	ABM8-24.000MHZ-R60-D-1-G-T	3.2 x 2.5 x 0.7mm	+/- 10 ppm	+/- 15 ppm (-40 +85)	+/- 3 ppm/First year max @ +25		60 ohms	18pF	22pF
Abracon	ABM8X-101-24.000MHZ	3.2 x 2.5 x 0.7mm	+/- 10 ppm	+/- 25 ppm (-40 +125)	+/- 5 ppm/10 years	+/- 40 ppm (-40 +125)/10 years max	60 ohms	10pF	6.8pF
Abracon	ABM8-177-24.000mHz	3.2 x 2.5 x 0.6mm	+/- 10 ppm	+/- 15 ppm (-40 +85)	+/- 15 ppm/20 years		60 ohms	18pF	22pF
AEL	X24M000000S037	3.2 x 2.5 x 0.6mm	+/- 10 ppm @25C	+/- 25 ppm (-40 +105)	+/- 3 ppm/year max		80 ohms	10pF	
AEL	X24M000000S050	3.2 x 2.5 x 0.6mm	+/- 10 ppm @25C	+/- 25 ppm (-40 +85)	+/- 3 ppm/year max		60 ohms	10pF	8.2pF
AEL	X24M000000S058	3.2 x 2.5 x 0.6mm	+/- 10 ppm @25C	+/- 15 ppm (-40 +85)	+/- 15 ppm/20 years max		60 ohms	10pF	
EPSON	TSX-3225 24.0000MF20G-C	3.2 x 2.5 x 0.6mm	+/- 10 ppm	+/- 20 ppm (-40 +105)	+/- 1 ppm/First year Max @ +25		60 ohms	18pF	
EPSON	TSX-3225 24.0000MF18X-C 18pF	3.2 x 2.5 x 0.7mm	+/- 10 ppm	+/- 18 ppm	+/- 1 ppm/First year max @ +25		60 ohms	18pF	27pF
ILSI	ILCX07-24.000000M-2392	3.2 x 2.5 x 0.9mm		(-40 +105)			60 ohms	18pF	
ILSI	ILCX13-24.000000M-2391	3.2 x 2.5 x 0.6mm		(-40 +85)			60 ohms	18pF	
KDS	1ZC224000ZZ0G	3.2 x 2.5 x 0.75mm				+/- 40 ppm (-40 +105)/10 years max	60 ohms	18pF	
KDS	1C324000ZZ0D	3.2 x 2.5 x 0.75mm	+/- 10 ppm			+/- 40 ppm (-40 +105)/10 years max	60 ohms	18pF	
Partron America Corp	CX5X24000FHVRG01	3.2 x 2.5 x 0.75mm	+/- 10 ppm	+/- 15 ppm (-40 +85)	+/- 2 ppm/ year @ +25		60 ohms	18pF	27pF
Precision Devices, Inc.	C324000XFAD13RX	3.2 x 2.5 x 0.7mm	+/- 10 ppm	+/- 20 ppm (-40 +70)	+/- 5 ppm/over life of the part		60 ohms	13pF	15pF
Suntsu	SCM18D48-24.000MHZ	3.2 x 2.5 x 0.65mm		+/- 15 ppm (-40 +85)	+/- 2 ppm/1st Year max, then +/- 1ppm/year		80 ohms	18pF	22pF
TXC Technology	7M-24.000MEEQ-T	3.2 x 2.5 x 0.7mm	+/- 10 ppm	+/- 10 ppm (-40 +85)	+/- 3 ppm/year max		60 ohms	18pF	
KDS	1B-1C-1H-1N22400AB0H	3.2 x 2.5 x 0.7mm							22pF

Table 4: Suggested 24MHz ZigBee Crystal Vendor Parts List for High Temperature Rated Crystals Having Alternate Package/PCB Dimensions than is Used in this Design

Manufacturer	Part Number	Package Size	Frequency Tol	Temperature Stability	Aging	Total Frequency Tol	ESR	Load Capacitance	Tuning Capactor
Abracon	ABM3Y-101-24.000MHZ-T	5.0 X 3.2 X 0.9mm	+/- 10 ppm	+/- 25 ppm (-40 +105)	+/- 10 ppm/5 years		30 ohms	10pF	
ILSI	ILCX07-24.000000M-2390	5.0 X 3.2 X 1.30mm		(-40 +105)			60 ohms	18pF	

Table 5: Suggested 24MHz ZigBee Crystal Vendor Parts List for Commercial and Industrial Rated Crystals Having Alternate Package/PCB Dimensions than is Used in this Design

Manufacturer	Part Number	Package Size	Frequency Tol	Temperature Stability	Aging	Total Frequency Tol	ESR	Load Capacitance	Tuning Capactor
Abracon	ABLS-24.000MHZ-D1X-T	HC/49US (AT49)	+/- 10 ppm	+/- 20 ppm (-40 +85)	+/- 10 ppm/5 years		40 ohms		
Abracon	ABLS-24.000MHZ-D-R60-1-W-T	HC/49US (AT49)	+/- 10 ppm	+/- 15 ppm (-40 +85)	+/-5 ppm/year		60 ohms	18pF	22pF
Abracon	ABLS-438-24.000MHZ-T	HC/49US (AT49)	+/- 10 ppm	+/- 15 ppm (-40 +85)	+/- 15 ppm/20 years		60 ohms	18pF	22pF
AEL	X24M000000S067	HC49S SM	+/- 10 ppm @25C	+/- 25ppm (-40 +105)	+/- 3 ppm/year max		80 ohms	10pF	
ILSI	HC49USM-24.000000M-2435	HC49US	+/- 10 ppm	(-40 +85)			30 ohms	18pF	
ILSI	ILCX07-24.000000M-2389	5.0 X 3.2 X 1.30mm		(-40 +85)			60 ohms	18pF	
KDS	1ZCA24000ZZ0C	2.5 x 2.0 x 0.75mm				+/- 40 ppm (-40 +105)/10 years max	80 ohms	18pF	
KDS	1ZCB24000ZZ0B	2.5 x 2.0 x 0.75mm				+/- 40 ppm (-40 +105)/10 years max	60 ohms	18pF	
TXC Technology	7B-24.000MEEQ-T	5.0 X 3.2 X 1.30mm	+/- 10 ppm	+/- 10 ppm (-40 +85)	+/- 3 ppm/year max		40 ohms	18pF	

EM359x-REF-DES-CER-USB

Schematic Notes:

-- Version A0--
***Released: March 25, 2015**
***Intial Release Version**

PCB Layout Notes:

-- Version A0 --
***Released: March 25, 2015**
***Intial Release Version**

SILICON LABS
343 Congress Street, 4th Fl,
Boston, MA 02210, USA
www.silabs.com
617-951-0200

MCU & Wireless WMN Support

Title:	EM359x/0805 Ceramic Balun W/USB Reference Design
Part Number: 130-0859-001	Rev: A0
Sheet Name: 5_EM359x-REF-DES-CER-USB_Rev_Notes.SchDoc	
Date: 3/25/2015 | Time: 6:36:51 PM	Sheet: 5 of 5 | Size: C