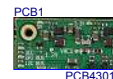





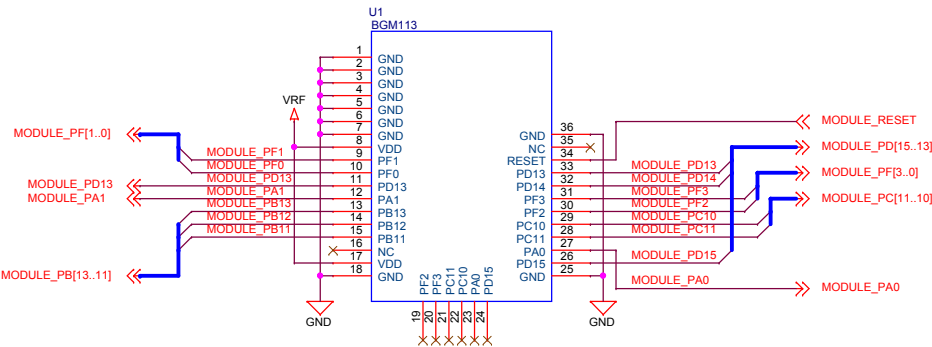
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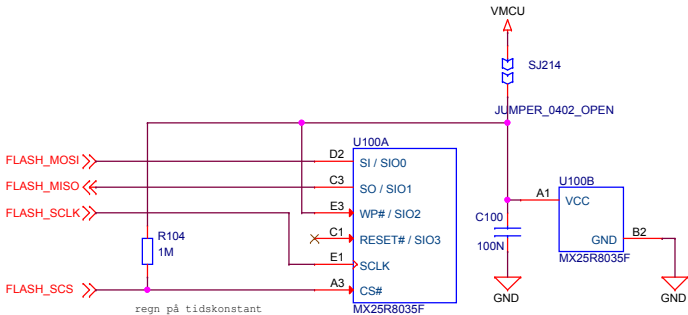
<Schematic Path>
SCHEMATIC1

 SILICON LABS		Schematic Title	
		BGM113 Module Carrier Board	
Designed: DDB		Approved: JNO	
Size A3	BOM Doc No: <Cage Code>	Document number BRD4301A	Revision A01
Design Created Date: Monday, April 02, 2012		Sheet Created Date Monday, April 02, 2012	Sheet Modified Date Monday, July 30, 2018
		Sheet 1 of 3	

Module Footprint



Serial Flash

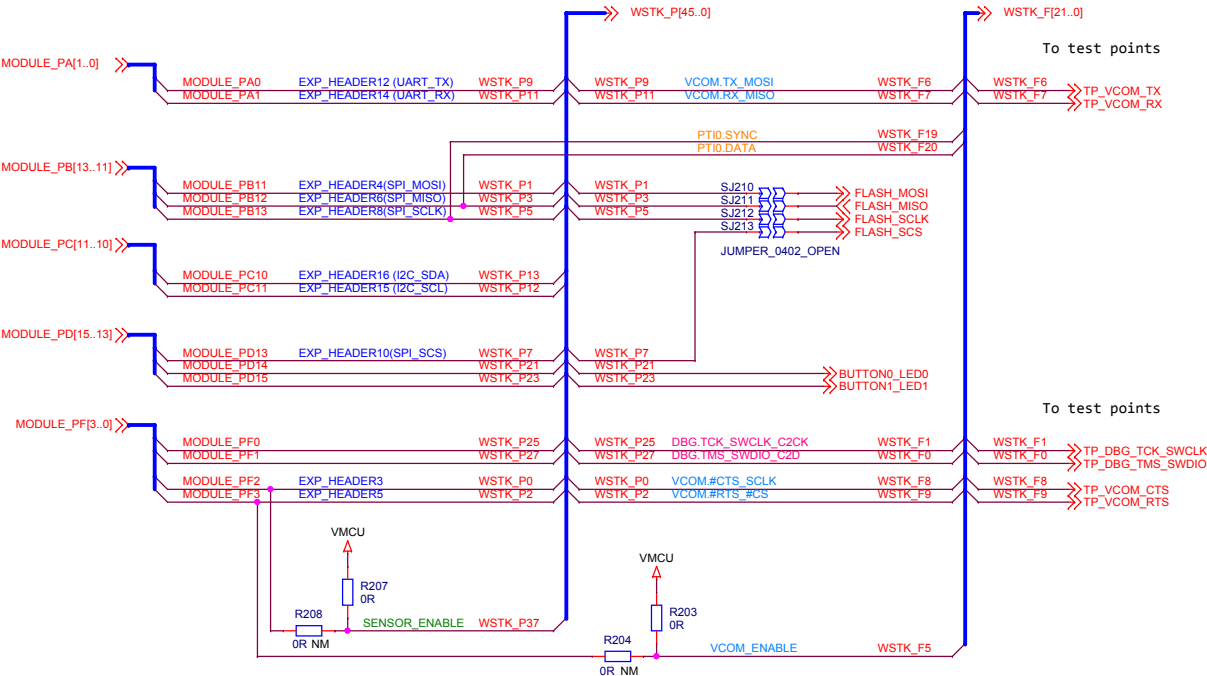


MX25R serial flash is always disabled.
Connect SJ210-SJ214 to enable.

Pin Assignments

Breakout connections

Functional Connections

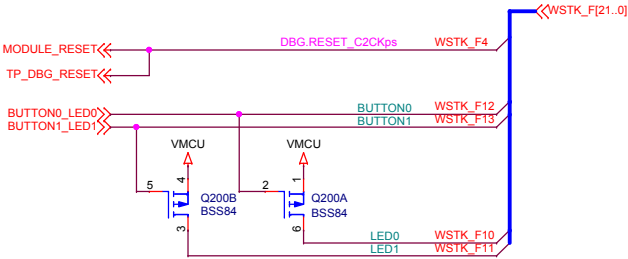


Humidity sensor on the mainboard is always enabled. Virtual COM port on the mainboard is always enabled.
Move R207 to R208 to connect PF2 with SENSOR_ENABLE. Move R203 to R204 connect PF3 with VCOM_ENABLE.

Note: Inserting R204 or R208 prevents using flow control on VCOM.

Additional Connections

Reset input from mainboard

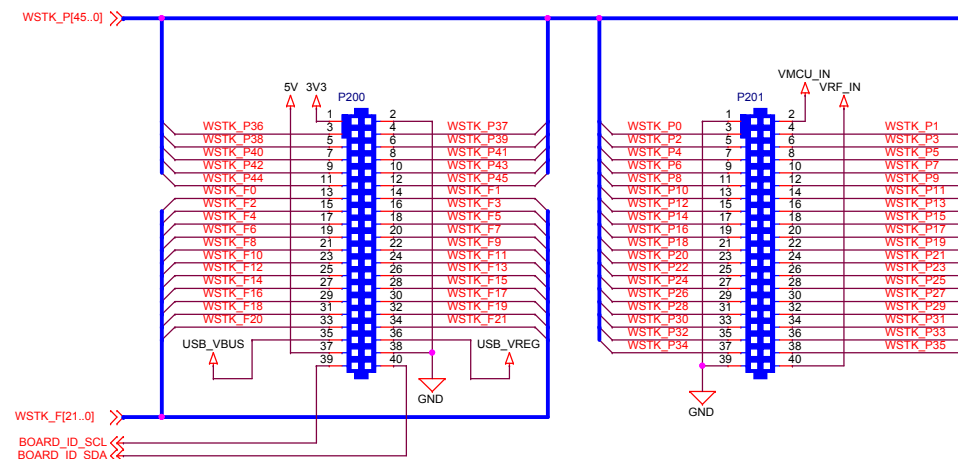


Buttons and leds connected to the same I/O pins:
Output: 0 = LED ON, 1 = LED OFF
Input: 0 = BUTTON PRESSED, 1 = BUTTON RELEASED

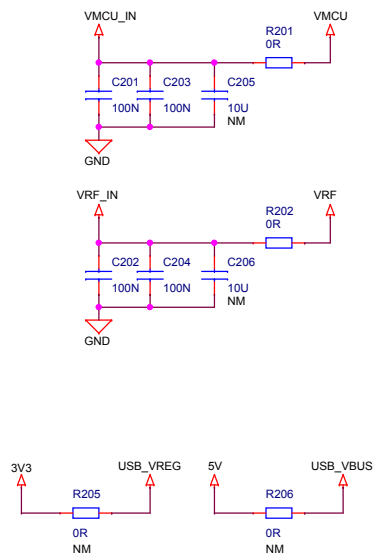
<Schematic Path>
SCHEMATIC1

 SILICON LABS		Schematic Title BGM113 Module Carrier Board	
Designed: DDB		Page Title RF, Antenna & Power	
Size A3		Document number BRD4301A	
Design Created Date: Monday, April 02, 2012		Sheet Created Date Monday, April 02, 2012	Sheet Modified Date Monday, July 30, 2018
Approved: JNO		Revision A01	Sheet 2 of 3

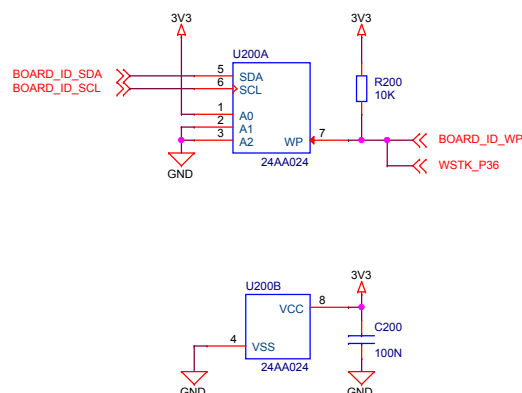
WSTK Connectors



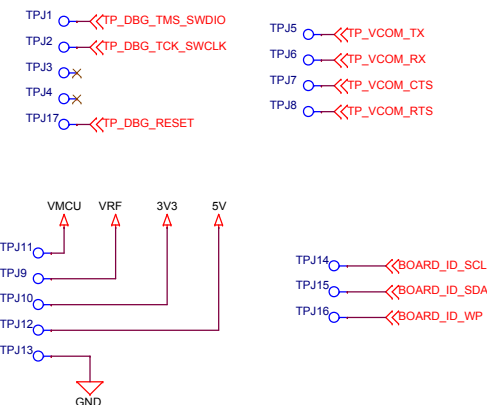
WSTK Power Decoupling



Board Identification



Test Points



<Schematic Path> SCHEMATIC1

		Schematic Title	
Designed: DDB		BGM113 Module Carrier Board	
Size: A3		Page Title	
BOM Doc No: <Cage Code>		WSTK Connectors & Board ID	
Design Created Date: Monday, April 02, 2012		Document number	Revision
		BRD4301A	A01
Sheet Created Date: Tuesday, April 03, 2012		Sheet Modified Date: Monday, July 30, 2018	Sheet 3 of 3