

1(2)

## \*\*\* PCB SPECIFICATION FOR BARE BOARD MANUFACTURING \*\*\*

PRODUCT OWNER : Silicon Labs  
 DOCUMENT/BOARD : PCB4302 Rev A00  
 Specification for PCB4302A  
 DATE : 2016-04-01  
 REVISION : A00

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PREPARED BY : Tamas Bodi  
 BOARDS pr PANEL: 12 (4 x 3)  
 PANEL SIZE : 210.2 x 205.4 mm  
 BOARD SIZE : 30.0 x 38.5 mm  
 BOARD THICKNESS: 1.6 mm +/- 10 %  
 NO OF LAYERS : 4  
 MATERIAL(S) : Glass Epoxy FR-4, NEMA Class 2, UL 94V-0, Tg min 150 C  
 Materials in compliance with the RoHS and WEEE directives  
 MARKINGS: Logo, Week/Year, UL (ON SECONDARY SIDE (BOT))  
 (Avoid areas reserved for DataMatrix, Barcodes or Labels)

QUALITY REQ. : IPC-A-600 (current revisions) Class 2, and IPC specifications  
 referred to by IPC-A-600

GENERAL REQ. : - Copper must not be added or removed from inside the board  
 outline(s), without written consent/approval.  
 If applicable, the following requirements are valid:  
 - Copper balancing may be applied on break-away-tabs,  
 or otherwise outside board outline(s), but must have  
 a minimum 1.5 mm clearance to possible fiducials.  
 - If Build-Up (Stack-Up) is specified, follow Build-Up,  
 otherwise use (board manufacturer) standard Build-Up.  
 - Break-away areas may be used for patterns, holes etc.  
 by manufacturer for QA purposes.  
 - If V-CUT, use angle 30 +/- 5 degrees.  
 V-CUT minimum remaining thickness 0.5 +/- 0.1 mm.  
 Use of V-CUT test pads is allowed.  
 - Inner radius (contour/outline) 1.2 mm, unless stated  
 otherwise.

COPPER THK. : SEE BUILD-UP  
 COPPER PASSIV. : ENIG to meet IPC-4552 requirements (current revision)  
 (Electroless Nickel/Immersion Gold)

RESIST MASK : Solder Mask Color: BLACK (NB! NON-STANDARD)  
 Photo Polymer wet film  
 to IPC-SM-840 Class T requirements (current revision)  
 Thickness minimum 8 um, maximum 20 um

VIA HOLES : PLUGGED/FILLED, IPC-4761 (current revision) Type IV-b  
 Plugged and Covered Both Sides, Low CTE Plugging Paste

LEGEND/SILKSCR.: WHITE, BOTH SIDES (TOP + BOT)

CONTROLLED IMP : Design has Controlled impedances. FOLLOW BUILD-UP STRICTLY!  
 Unless explicitly stated otherwise, controlled impedance  
 has been designed into the board. Use of test strip is  
 hence normally not required.  
 NOMINAL VALUES for width, Spacing and VIA Diameter:

Cu TRACK(TRACE): Minimum conductor width : 0.152 mm (6 mils)  
 Cu SPACING : Minimum conductor spacing: 0.152 mm (6 mils)  
 MINIMUM VIA : Minimum via pad diameter : 0.51 mm (20 mils)  
 Min via hole size: 0.254 mm (9.842 mils)  
 Min via hole may have more than one pad diameter.

(SPECIFICATION CONTINUED ON NEXT PAGE)

2(2)

BUILD UP :  
L1 ===== 35 um Cu (ca) After plating  
////////// C O R E ////////// 300 um  
L2 ===== 18 um Cu (0.5 oz)  
- - - - P R E P R E G - - - - 900 um (ca)  
L3 ===== 18 um Cu  
////////// C O R E ////////// 300 um  
L4 ===== 35 um Cu

Prepreg may be adjusted in order to reach correct board thickness

TEST : 100% Electrical Test  
Optical test, AOI (with automatic scanner)  
Visual inspection  
(Generate netlist from Gerber and Drill files)

Avoid use of 2125 Prepreg

If NB! is used in this specification, it means:  
abbreviation for nota bene!, a Latin expression meaning  
"note well!"

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NC DRILL - HOLE INFORMATION:  
WARNING: Drill dimensions must be taken from the Excellon (.DRL) file(s).  
NON-PLATED holes may have a small center marker in the Gerber files.  
Under no circumstance must these Gerber flashes be mistaken for the  
hole drill dimensions!

The drill data may contain slots (in a separate file).  
Dimensions for the finished board (after plating).  
Tolerances +/- 0.1 mm, unless specified differently.  
Via Holes +0.05 mm/-Via Size, unless specified differently.

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