EFM32 Development Kit

Revision History

Rev.	Description
PA18	Removed STM32 testADC connection Added OE signal to BC_SPI buffer Clamped DIR signal on BC_SPI buffer
A00	Changed ST1 and ST2 to NM Initial Release
A01	Fixed EFM32_A80 connection
A02	Set D11 to Not Mounted Changed capacitors on trace lines to 8.2 pF

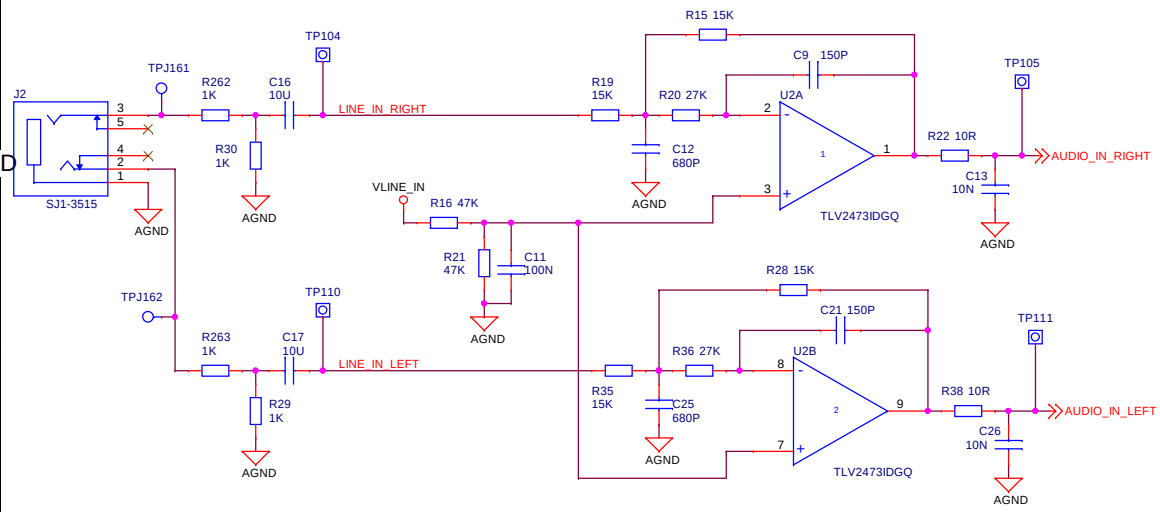
<Schematic Path>
TOP

PCB1

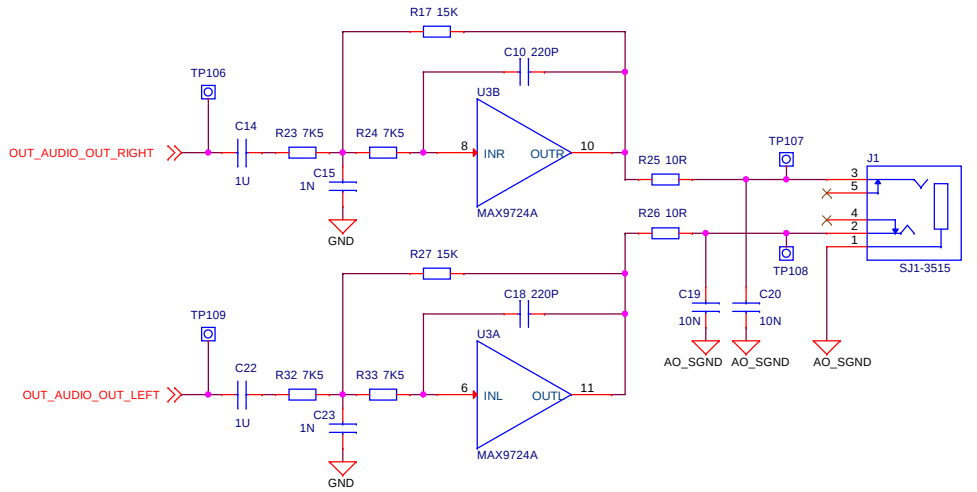
PCB3201

Schematic Title	EFM32 Development Kit - Mainboard
Page Title	Title Page
Designed: JNO / Approved: JNO	
Size: A3 / BOM Doc No: <Cage Code>	Document number: BRD3201A / Revision: A02
Design Created Date: Wednesday, December 03, 2008	Sheet Created Date: Saturday, March 21, 2009 / Sheet Modified Date: Thursday, September 08, 2011 / Sheet: 1 of 22

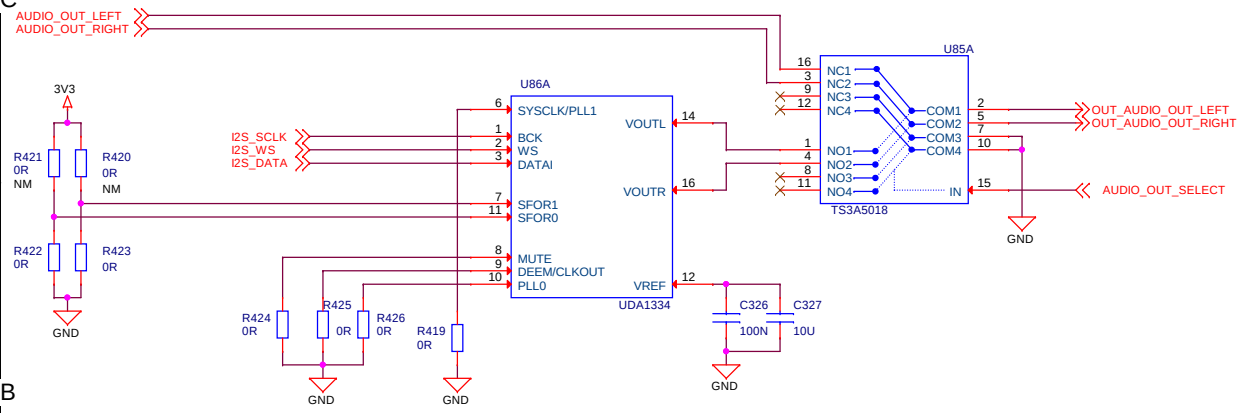
Line In Amplifier & Filter



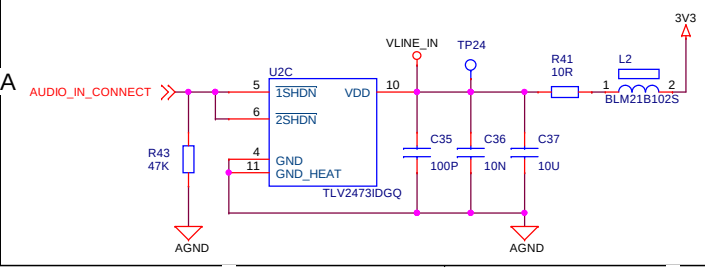
Line Out Driver & Filter

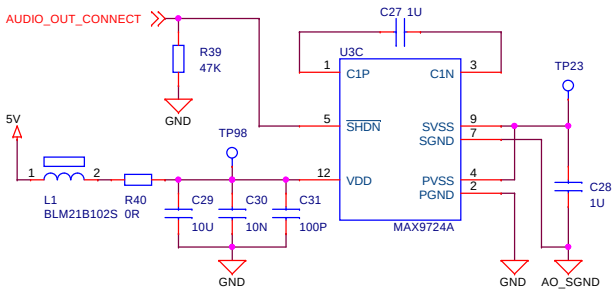


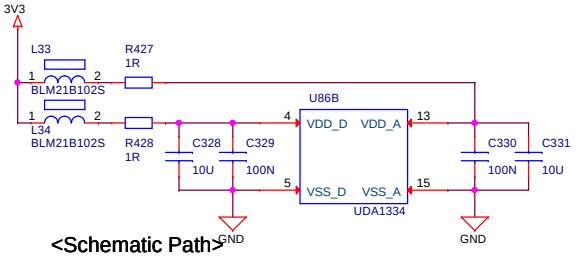
I2S DAC

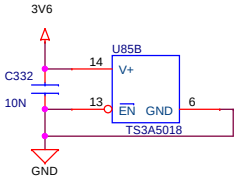


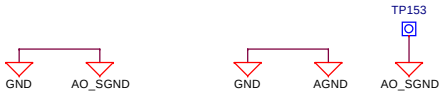
Power Supply and Decoupling











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Schematic Title	**EFM32 Development Kit - Mainboard**
Page Title	**Interface - Analog**
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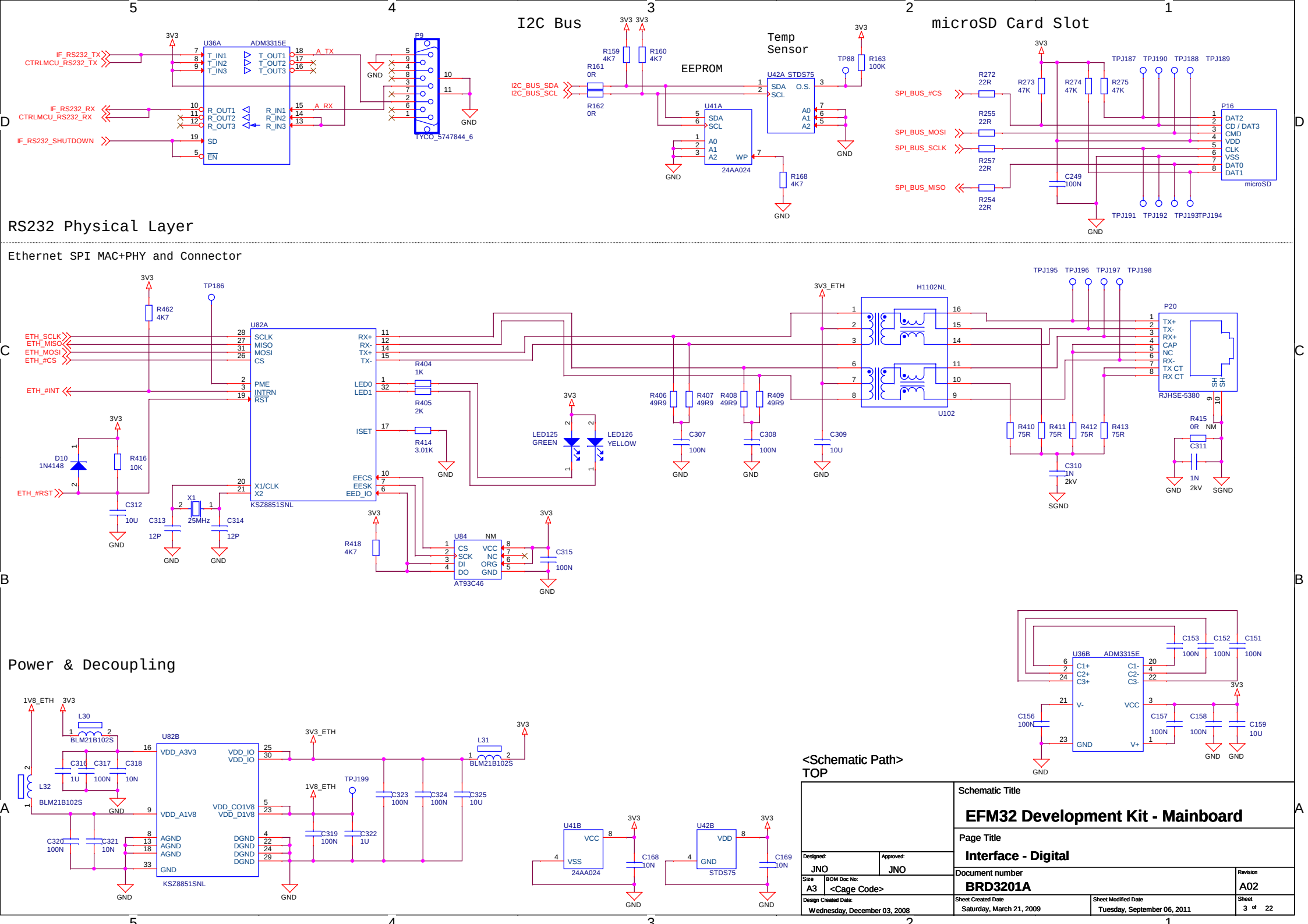
RS232 Physical Layer
I2C Bus
EEPROM
Temp Sensor
microSD Card Slot
Ethernet SPI MAC+PHY and Connector
Power & Decoupling
U36A ADM3315E
P9
TYCO_5747844_6
U41A
U42A STDS75
24AA024
TP88
R163 100K
R159 4K7
R160 4K7
R161 0R
R162 0R
R168 4K7
I2C_BUS_SDA
I2C_BUS_SCL
P16
microSD
SPI_BUS_#CS
SPI_BUS_MOSI
SPI_BUS_SCLK
SPI_BUS_MISO
R272 22R
R255 22R
R257 22R
R254 22R
R273 47K
R274 47K
R275 47K
C249 100N
TPJ187 TPJ190 TPJ188 TPJ189
TPJ191 TPJ192 TPJ193 TPJ194
IF_RS232_TX
CTRLMCU_RS232_TX
IF_RS232_RX
CTRLMCU_RS232_RX
IF_RS232_SHUTDOWN
A_TX
A_RX
U82A KSZ8851SNL
TP186
R462 4K7
ETH_SCLK
ETH_MISO
ETH_MOSI
ETH_#CS
ETH_#INT
ETH_#RST
R404 1K
R405 2K
R414 3.01K
R416 10K
D10 1N4148
X1 25MHz
C312 10U
C313 12P
C314 12P
LED125 GREEN
LED126 YELLOW
3V3_ETH
H1102NL
U102
R406 49R9
R407 49R9
R408 49R9
R409 49R9
C307 100N
C308 100N
C309 10U
R410 75R
R411 75R
R412 75R
R413 75R
C310 1N 2kV
P20
RJHSE-5380
R415 0R NM
C311 1N 2kV
U84 NM AT93C46
R418 4K7
C315 100N
L30 BLM21B102S
L31 BLM21B102S
L32 BLM21B102S
C316 1U
C317 100N
C318 10N
C320 100N
C321 10N
C322 1U
C323 100N
C324 100N
C325 10U
C319 100N
TPJ199
U41B 24AA024
U42B STDS75
C168 10N
C169 10N
U36B ADM3315E
C153 100N
C152 100N
C151 100N
C156 100N
C157 100N
C158 100N
C159 10U
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EFM32 Development Kit - Mainboard
Page Title
Interface - Digital
Document number
BRD3201A
Revision
A02
Designed: JNO
Approved: JNO
Size A3
BOM Doc No: <Cage Code>
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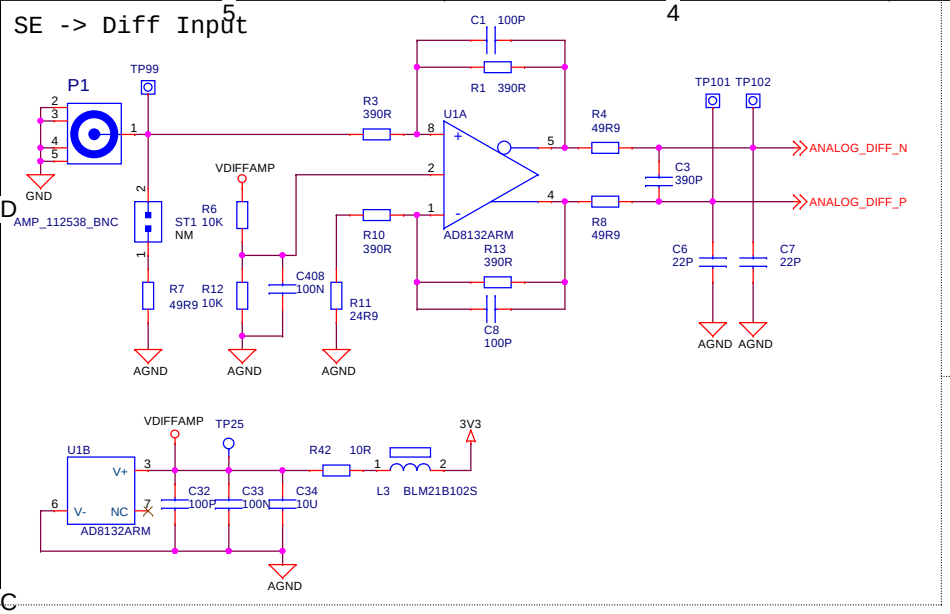
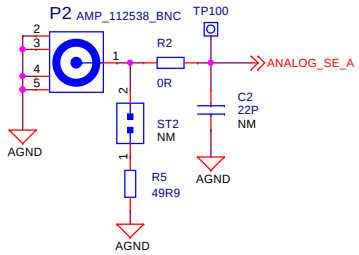
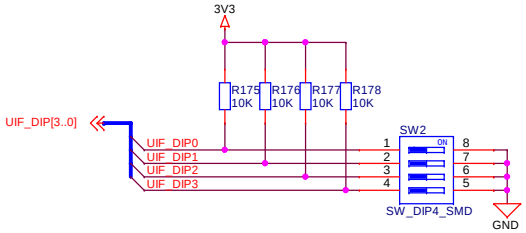
SE -> Diff Input



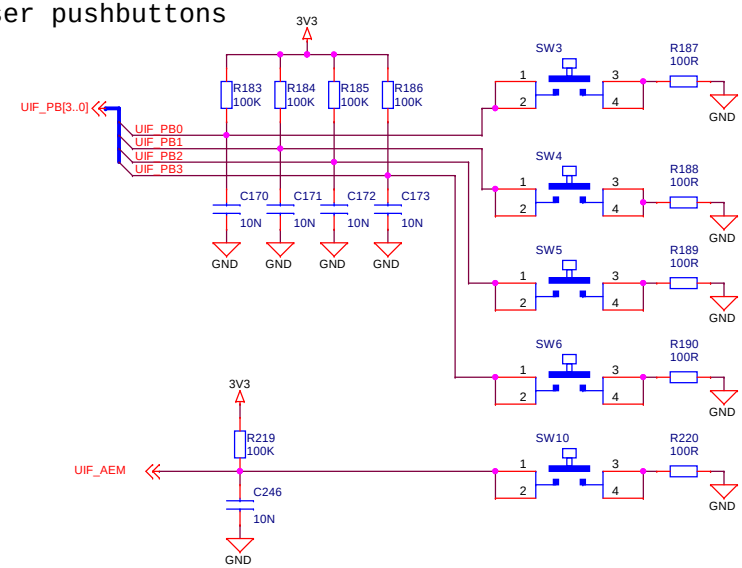
Single-Ended Input/Output



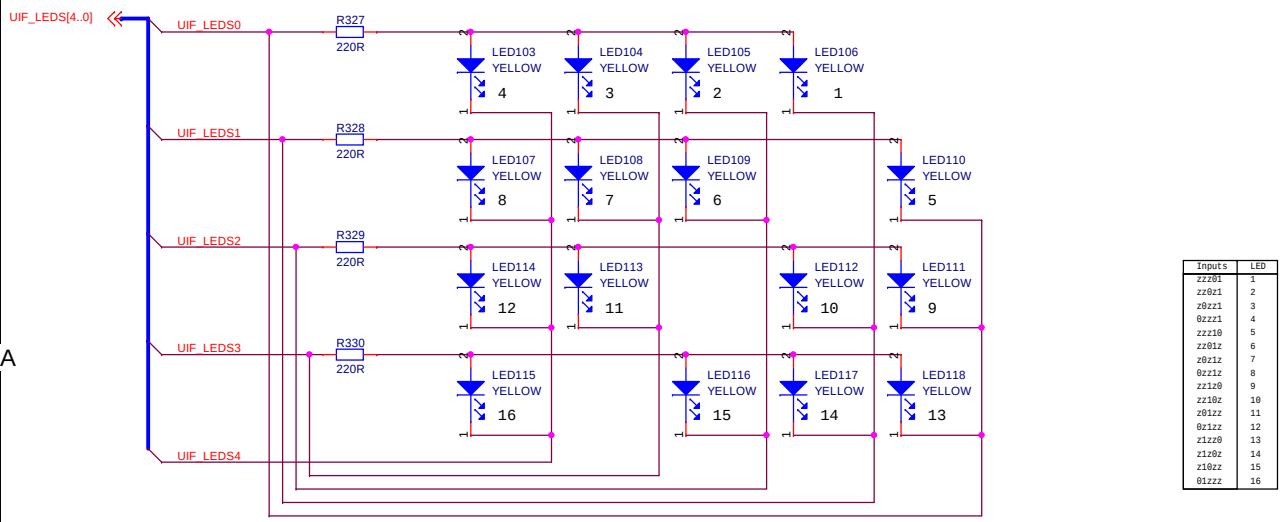
User switches



User pushbuttons

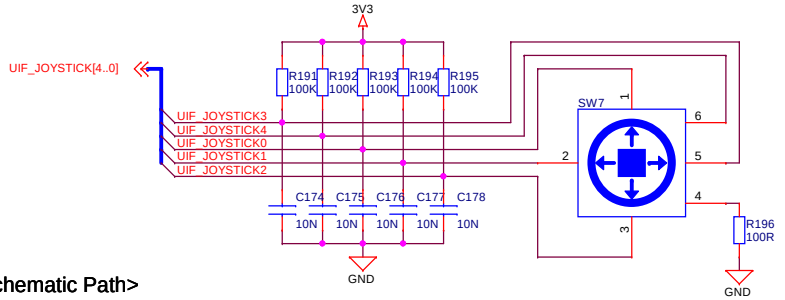


User LEDs



Inputs	LED
zzz01	1
zz0z1	2
z0zz1	3
0zzz1	4
zzz10	5
zz01z	6
z0z1z	7
0zz1z	8
zz1z0	9
zz10z	10
z01zz	11
0z1zz	12
z1zz0	13
z1z0z	14
z10zz	15
01zzz	16

Joystick



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Page Title	**Interface - Analog & UI**
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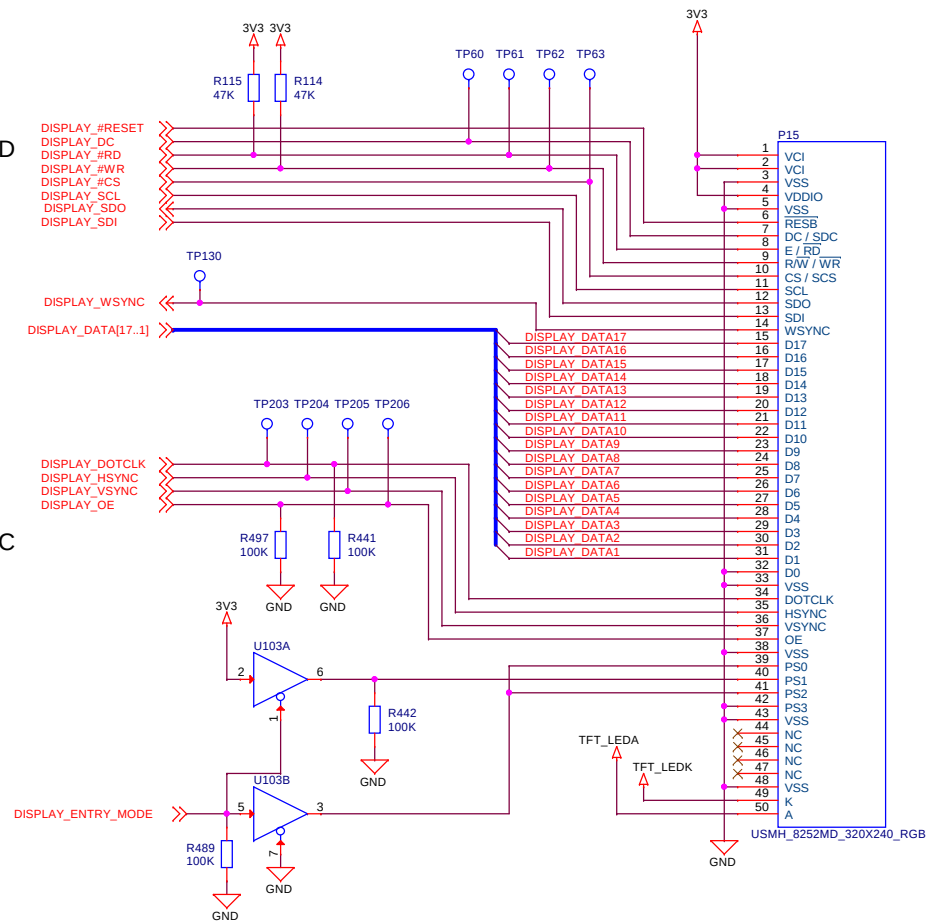
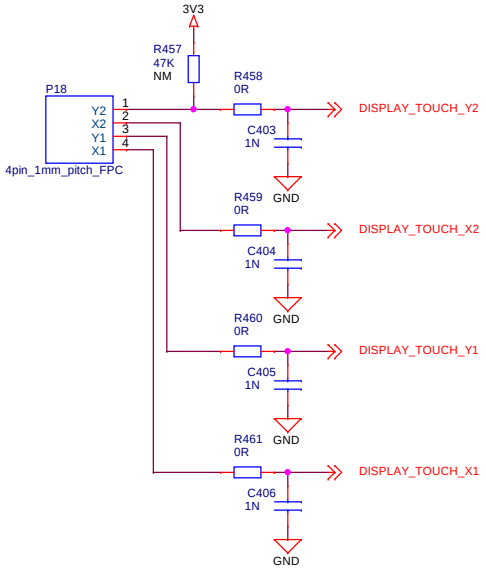
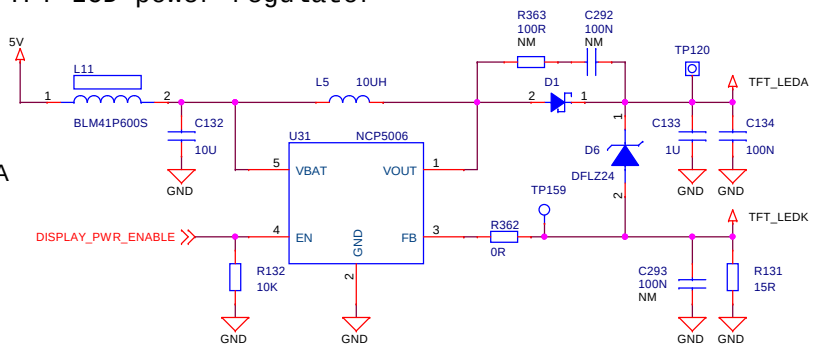
TFT-LCD Flat Panel Connector (FPC)

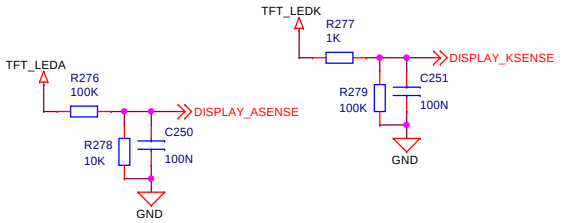




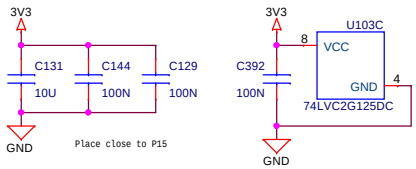
ENTRY_MODE	PS[3..0]	Description
0	0010	16 bit 8080 mode
1	0101	16 bit generic mode + SPI

TFT-LCD power regulator

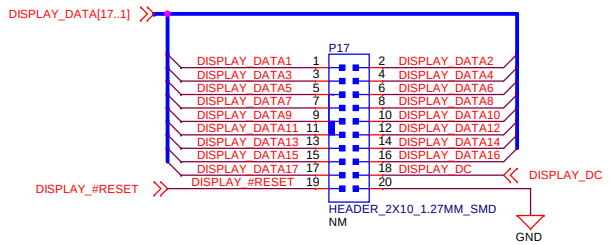




TFT-LCD decoupling



FPGA debug connector



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Schematic Title	EFM32 Development Kit - Mainboard
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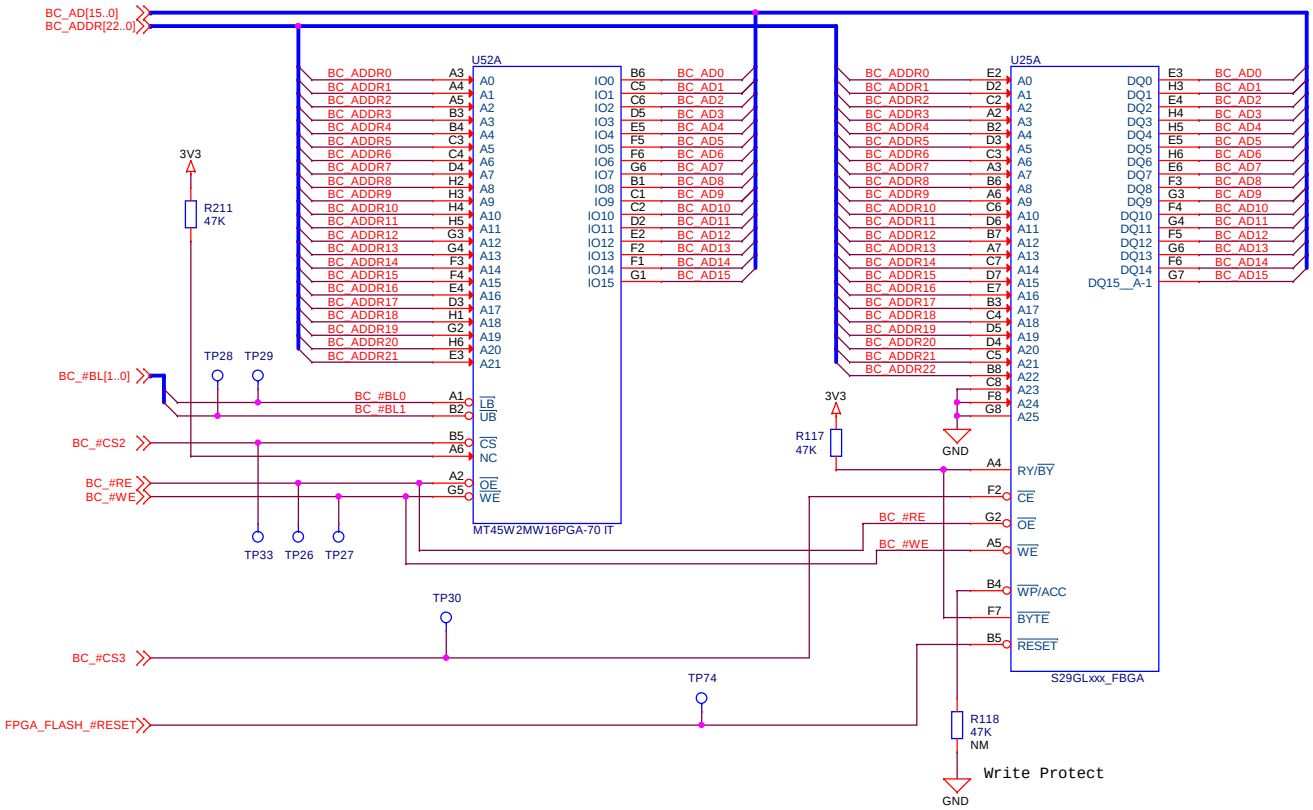
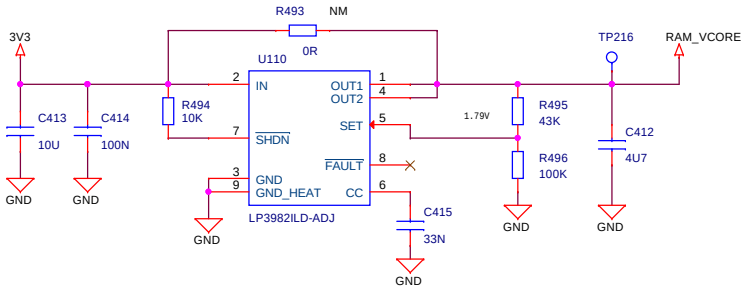
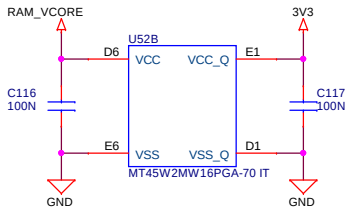
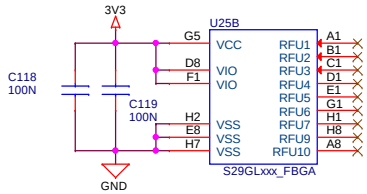


1.8V PSRAM regulator







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Schematic Title	**EFM32 Development Kit - Mainboard**
Page Title	**NOR Flash / SRAM**
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Size: A3 / BOM Doc No: <Cage Code>	Document number: **BRD3201A** / Revision: A02
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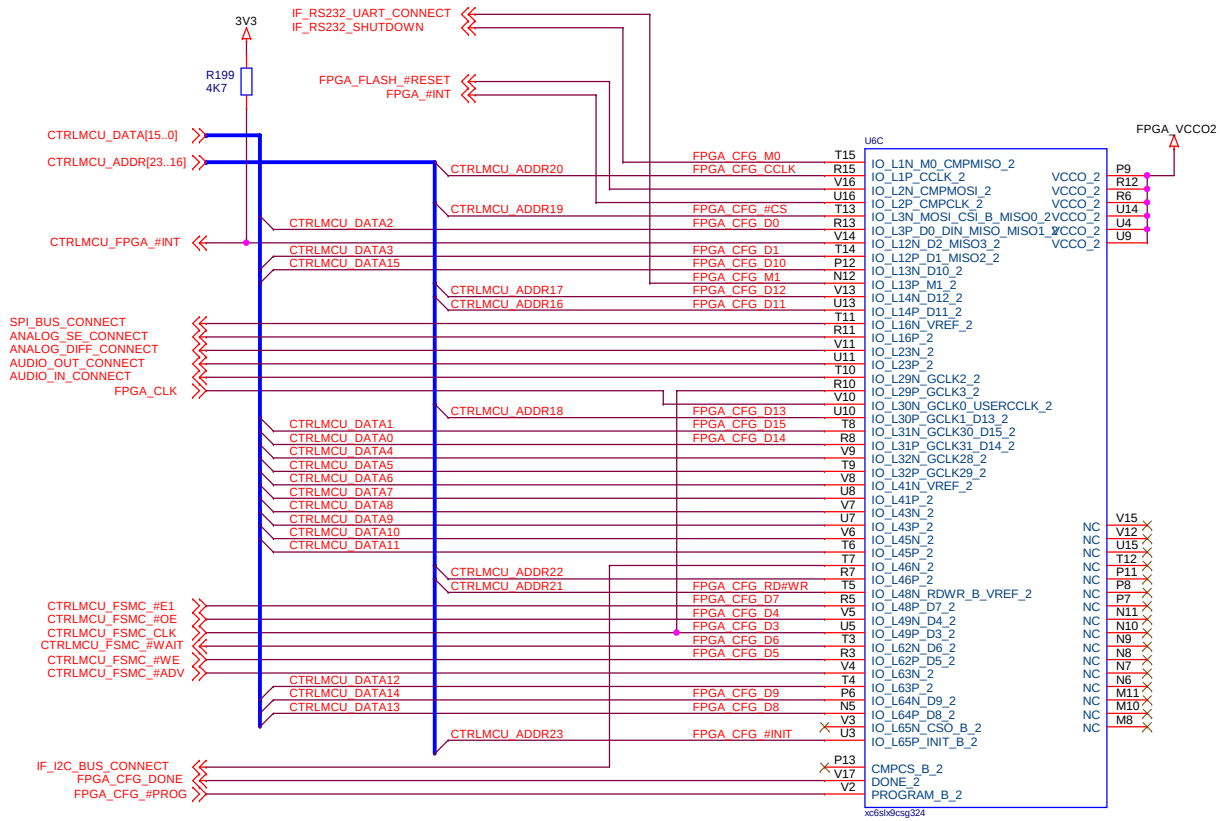
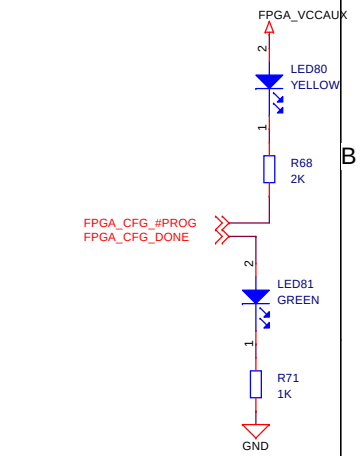
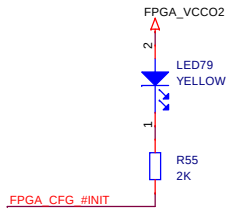
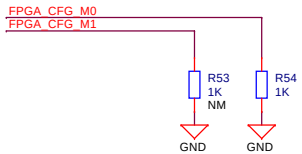




FPGA Init LED



FPGA Configuration Mode



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Schematic Title
EFM32 Development Kit - Mainboard

Page Title
Board Control - Control MCU Interface

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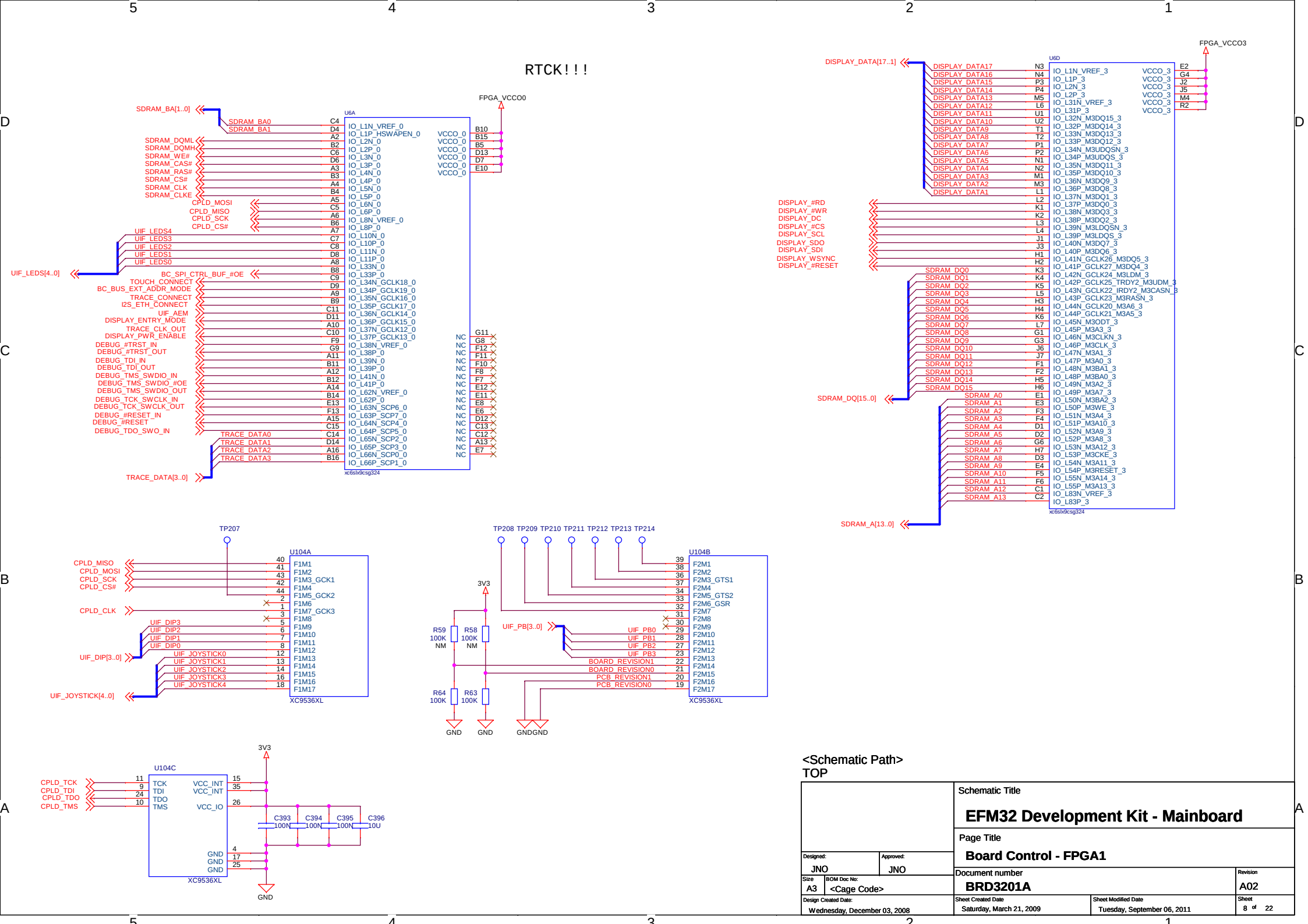

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Schematic Title	**EFM32 Development Kit - Mainboard**
Page Title	**Board Control - FPGA1**
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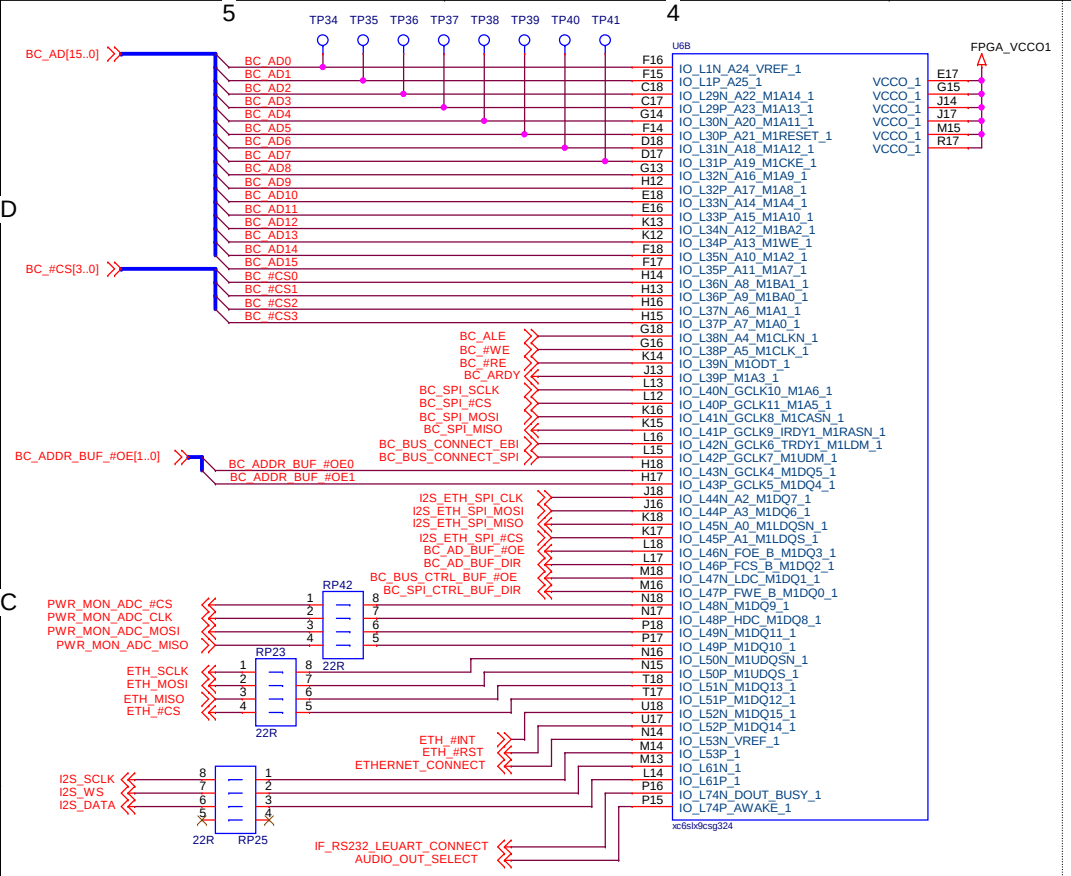

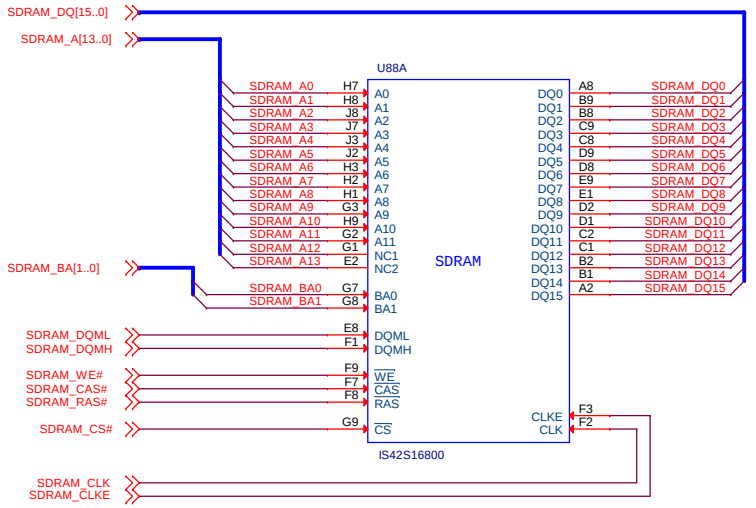

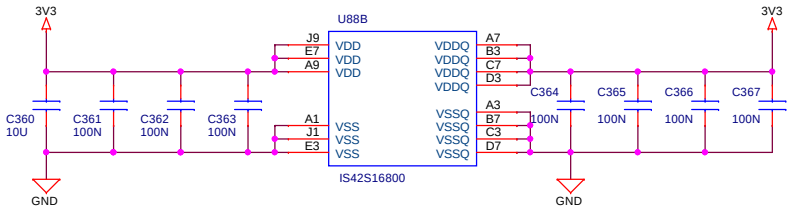

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Schematic Title	**EFM32 Development Kit - Mainboard**
Page Title	**Board Control - FPGA2**
Designed: JNO / Approved: JNO	Document number: **BRD3201A** / Revision: **A02**
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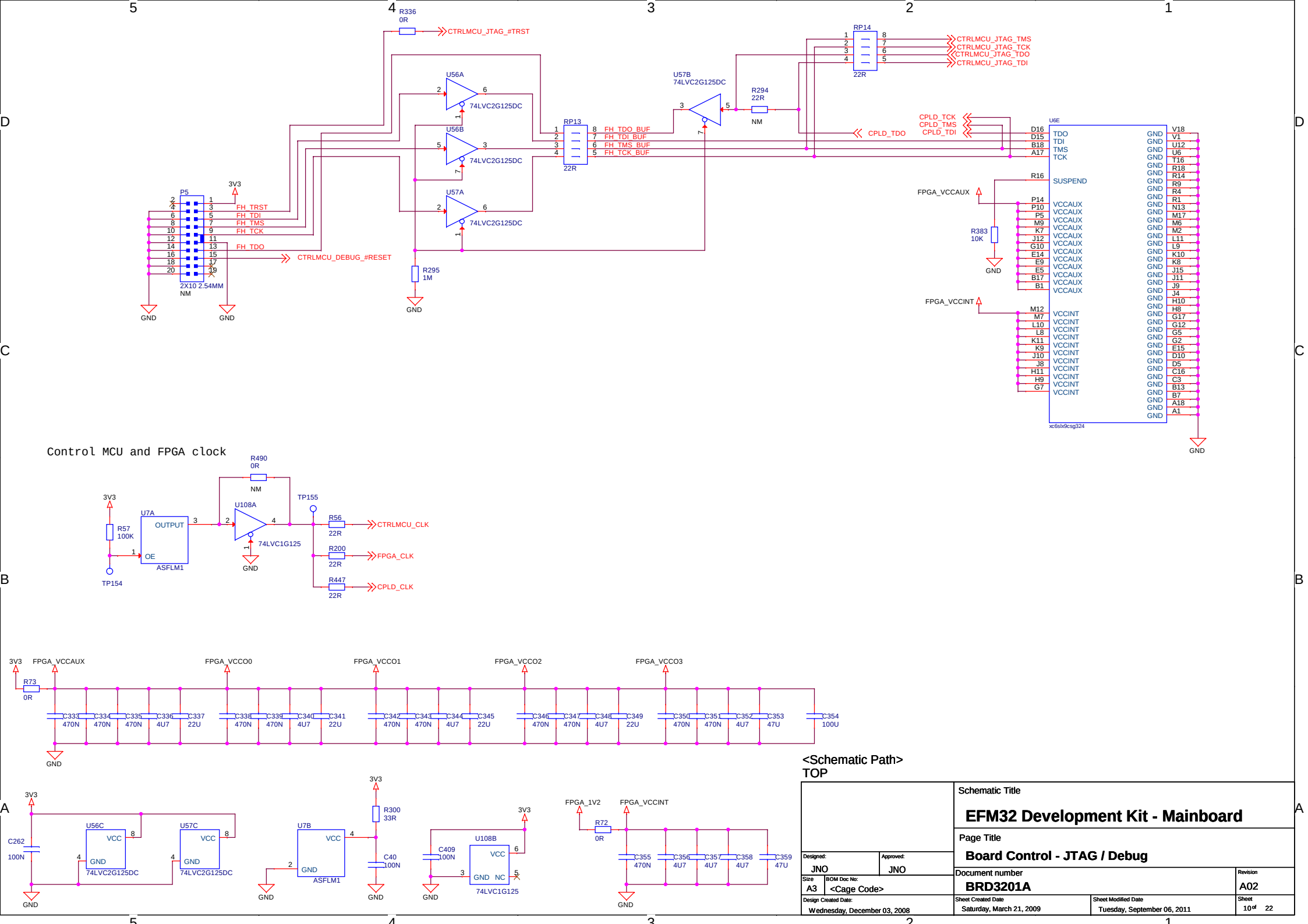
Design Created Date: Wednesday, December 03, 2008	Sheet Created Date: Saturday, March 21, 2009 / Sheet Modified Date: Tuesday, September 06, 2011


R336
0R
CTRLMCU_JTAG_#TRST
U56A
74LVC2G125DC
U56B
74LVC2G125DC
U57A
74LVC2G125DC
U57B
74LVC2G125DC
RP13
22R
FH_TDO_BUF
FH_TDI_BUF
FH_TMS_BUF
FH_TCK_BUF
RP14
22R
CTRLMCU_JTAG_TMS
CTRLMCU_JTAG_TCK
CTRLMCU_JTAG_TDO
CTRLMCU_JTAG_TDI
R294
22R
NM
CPLD_TDO
CPLD_TCK
CPLD_TMS
CPLD_TDI
P5
2X10 2.54MM
NM
FH_TRST
FH_TDI
FH_TMS
FH_TCK
FH_TDO
CTRLMCU_DEBUG_#RESET
3V3
GND
R295
1M
U6E
xc6slx9csg324
TDO
TDI
TMS
TCK
SUSPEND
VCCAUX
VCCINT
R16
R383
10K
FPGA_VCCAUX
FPGA_VCCINT
Control MCU and FPGA clock
R490
0R
NM
U108A
74LVC1G125
TP155
TP154
U7A
OUTPUT
OE
ASFLM1
R57
100K
R56
22R
R200
22R
R447
22R
CTRLMCU_CLK
FPGA_CLK
CPLD_CLK
R73
0R
FPGA_VCCO0
FPGA_VCCO1
FPGA_VCCO2
FPGA_VCCO3
C262
100N
U56C
U57C
74LVC2G125DC
U7B
ASFLM1
R300
33R
C40
100N
C409
100N
U108B
74LVC1G125
FPGA_1V2
R72
0R
C355
470N
C356
4U7
C357
4U7
C358
4U7
C359
47U
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EFM32 Development Kit - Mainboard
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Board Control - JTAG / Debug
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Approved: JNO
Size A3
BOM Doc No: <Cage Code>
Document number BRD3201A
Revision A02
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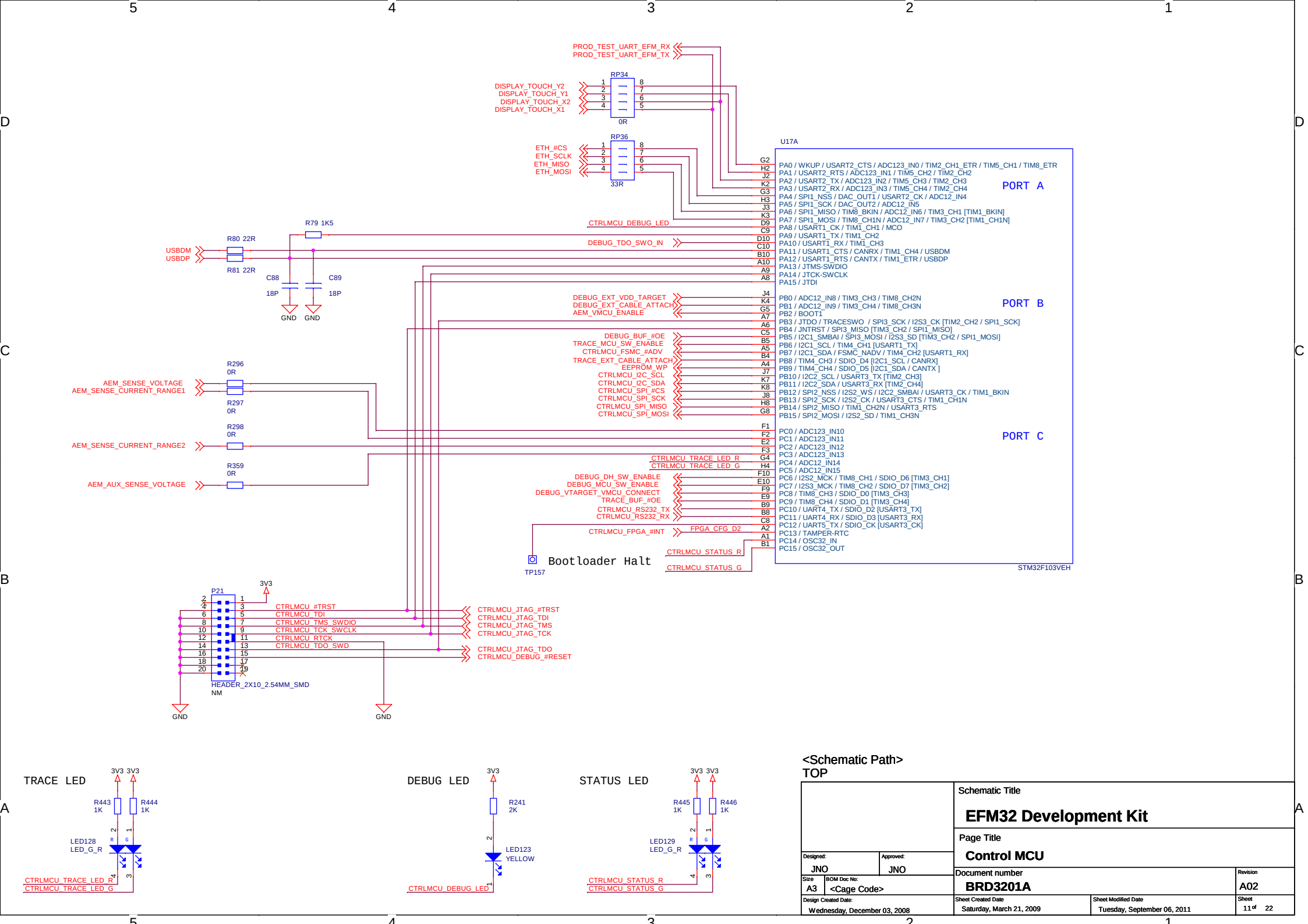

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Schematic Title	**EFM32 Development Kit**
Page Title	**Control MCU**
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Size: A3 / BOM Doc No: <Cage Code>	Document number: **BRD3201A** / Revision: A02
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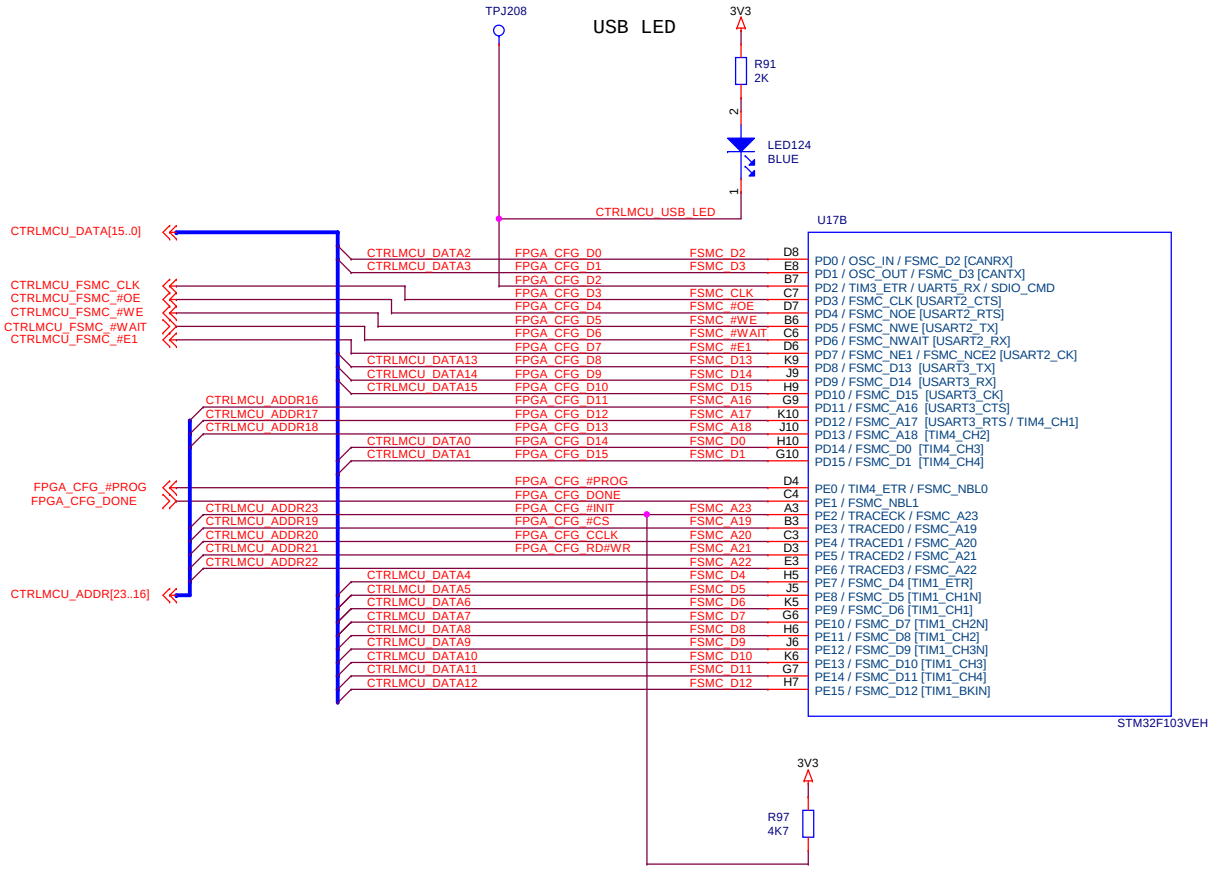
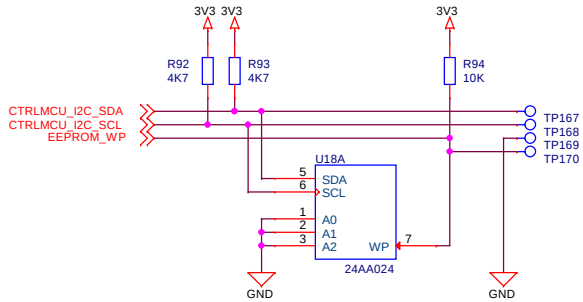
USB LED

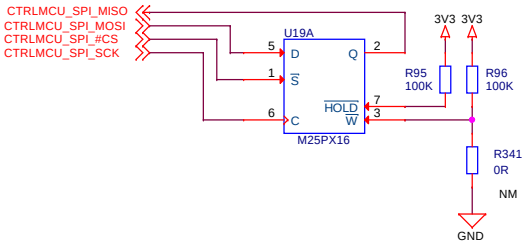


Control MCU EEPROM

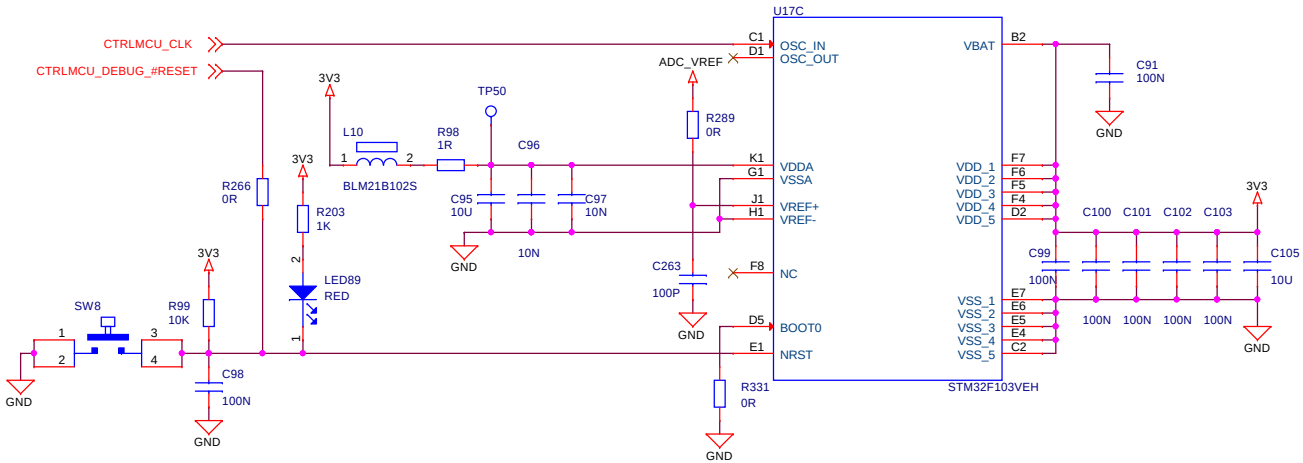


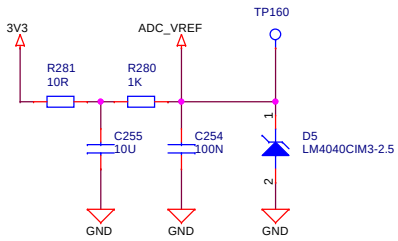
These test points must be placed exactly where the old header was.

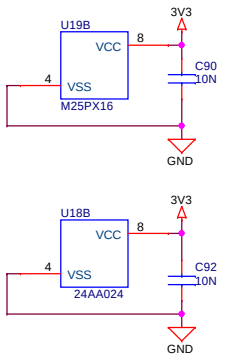
Control MCU SPI Flash



Control MCU Power & Bypass







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Schematic Title	**EFM32 Development Kit - Mainboard**
Page Title	**Control MCU - Board Control interface**
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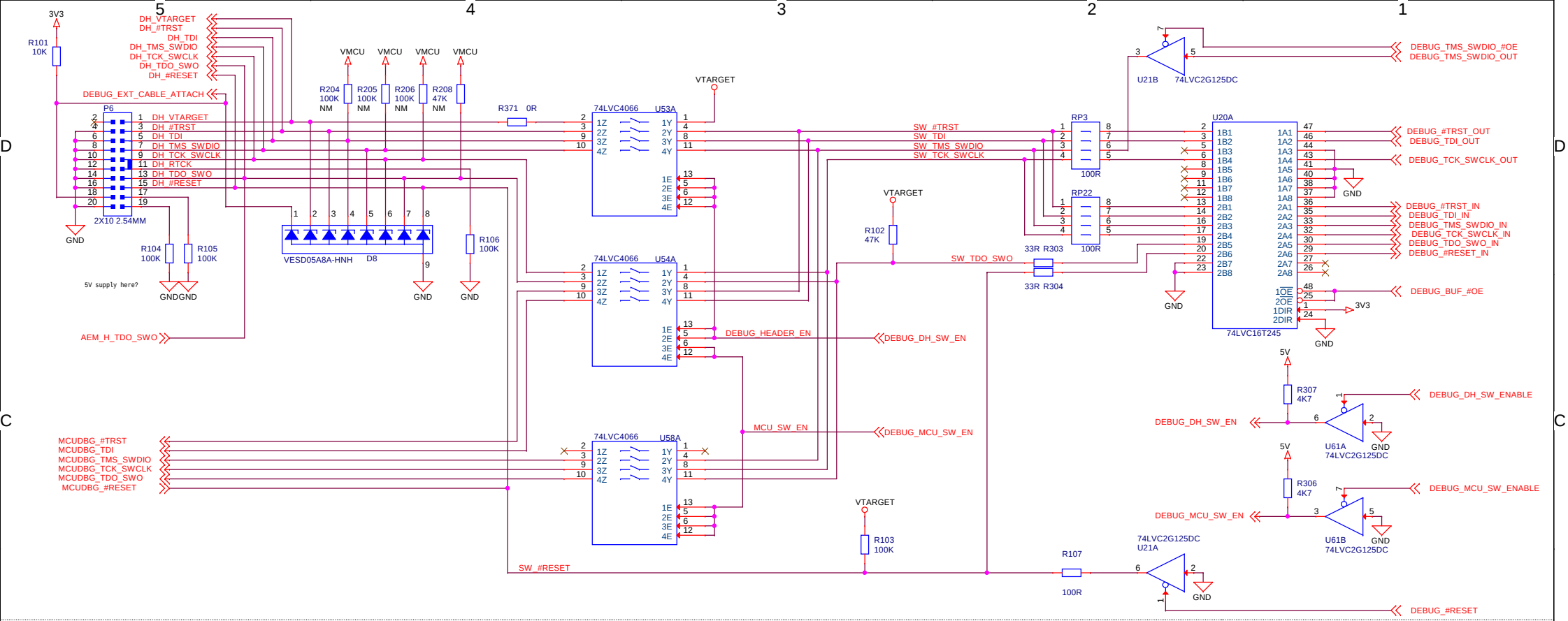
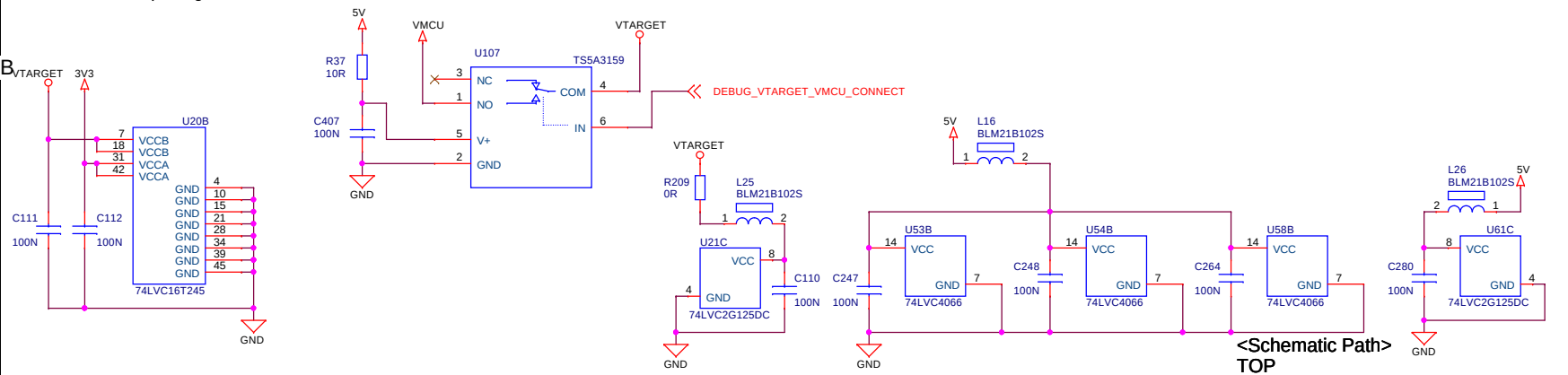
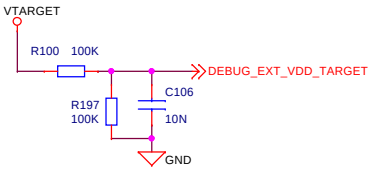


Power & Decoupling



Ext. Debug Voltage Measurement



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Mode	DEBUG_MCU_SW_ENABLE	DEBUG_DH_SW_ENABLE	DEBUG_BUF_#OE	DH_VTARGET	VTARGET
Debug Out	0	1	0	External voltage	External voltage
MCU Debug	1	0	0	Disconnected	VMCU
Debug In	1	1	1	VMCU	VMCU

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Debug Interface

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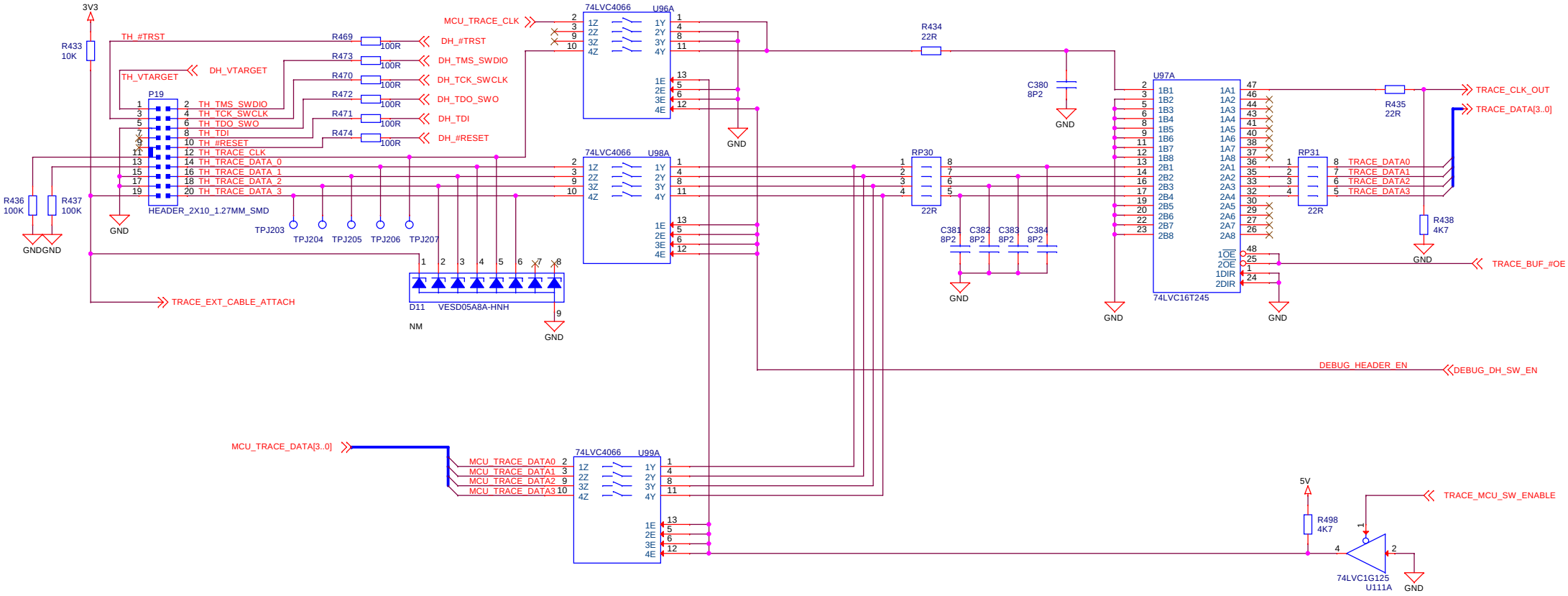
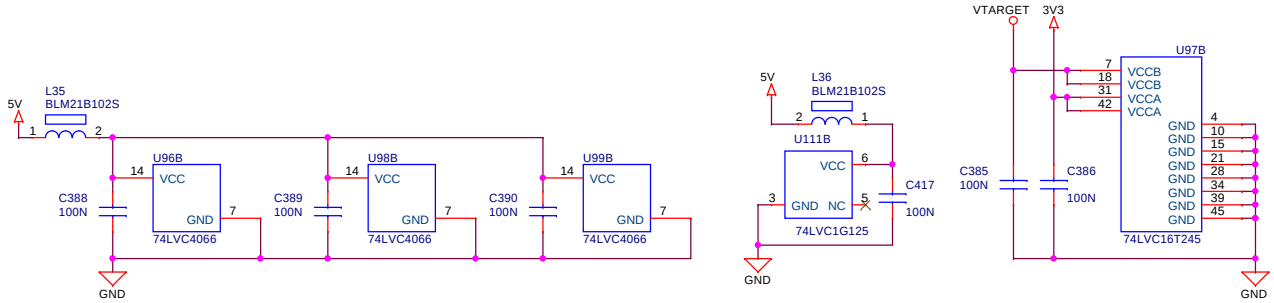


Mode	DEBUG_MCU_SW_ENABLE	DEBUG_TH_SW_ENABLE	TRACE_BUF_#OE
Trace OUT	0	1	0
MCU Trace	1	0	0
Trace IN	1	1	1



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	Schematic Title: **EFM32 Development Kit - Mainboard**
	Page Title: **Trace Interface**
Designed: AG / Approved: JNO	Document number: **BRD3201A** / Revision: **A02**
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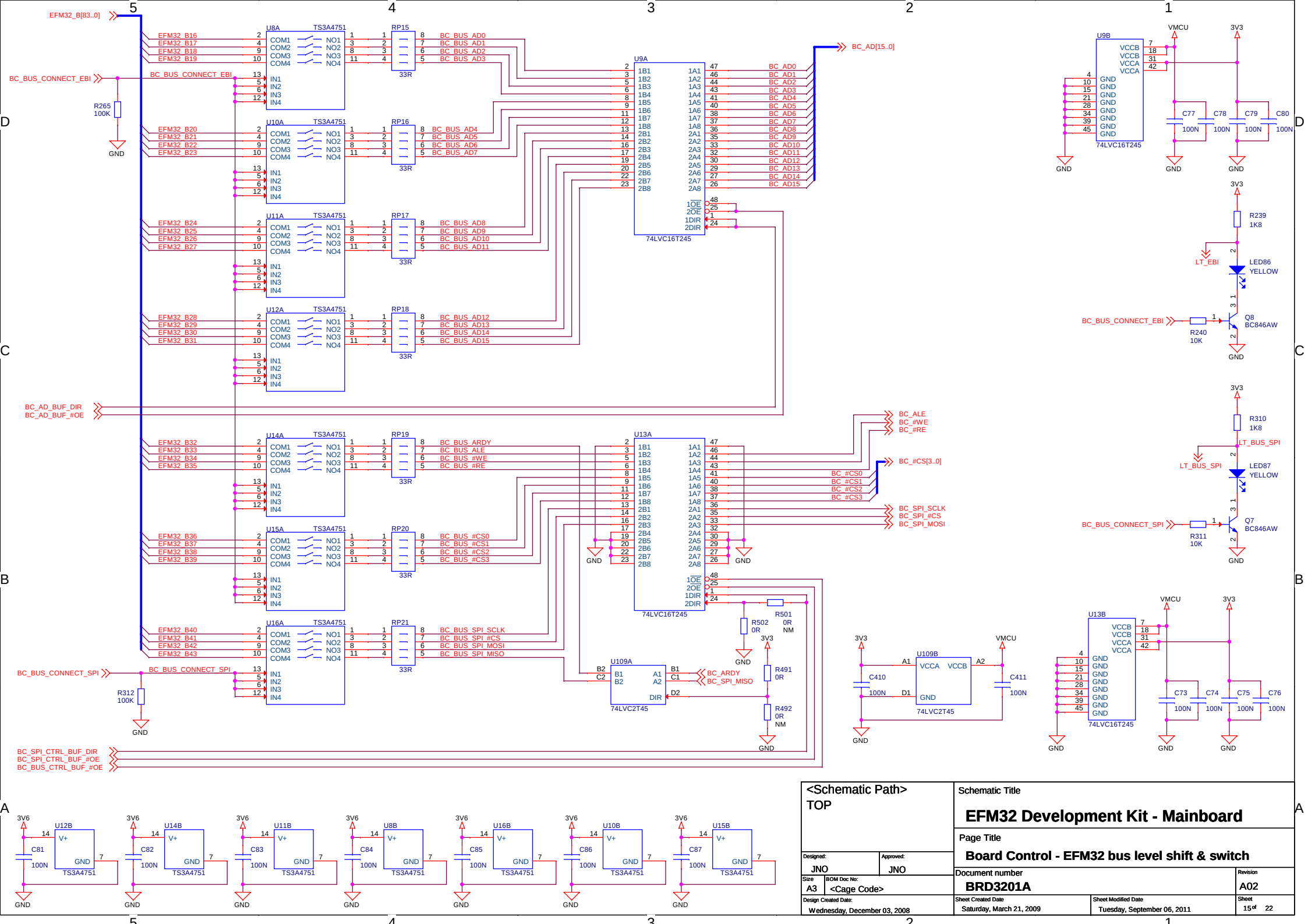
Design Created Date: Wednesday, December 03, 2008	Sheet Created Date: Monday, February 28, 2011 / Sheet Modified Date: Thursday, September 08, 2011 / Sheet: 14 of 22



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	Page Title: **Board Control - EFM32 bus level shift & switch**
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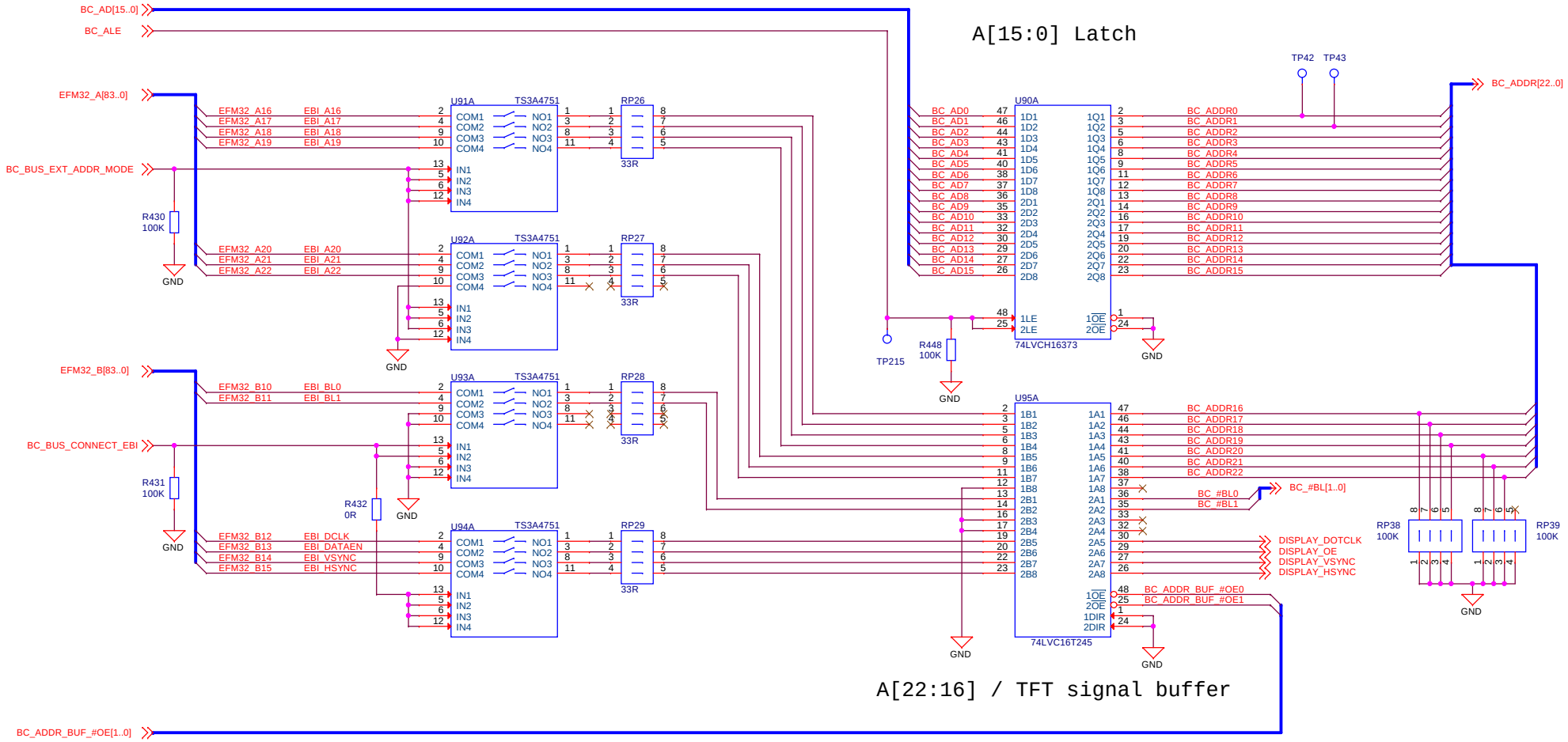
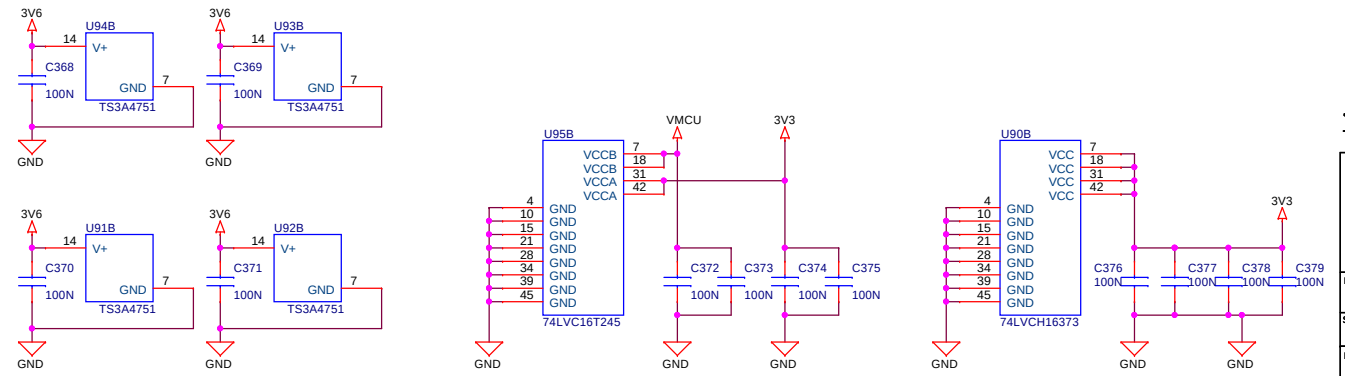


Power & Decoupling



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Page Title	**Board Control - EFM32 bus level shift & switch 2**
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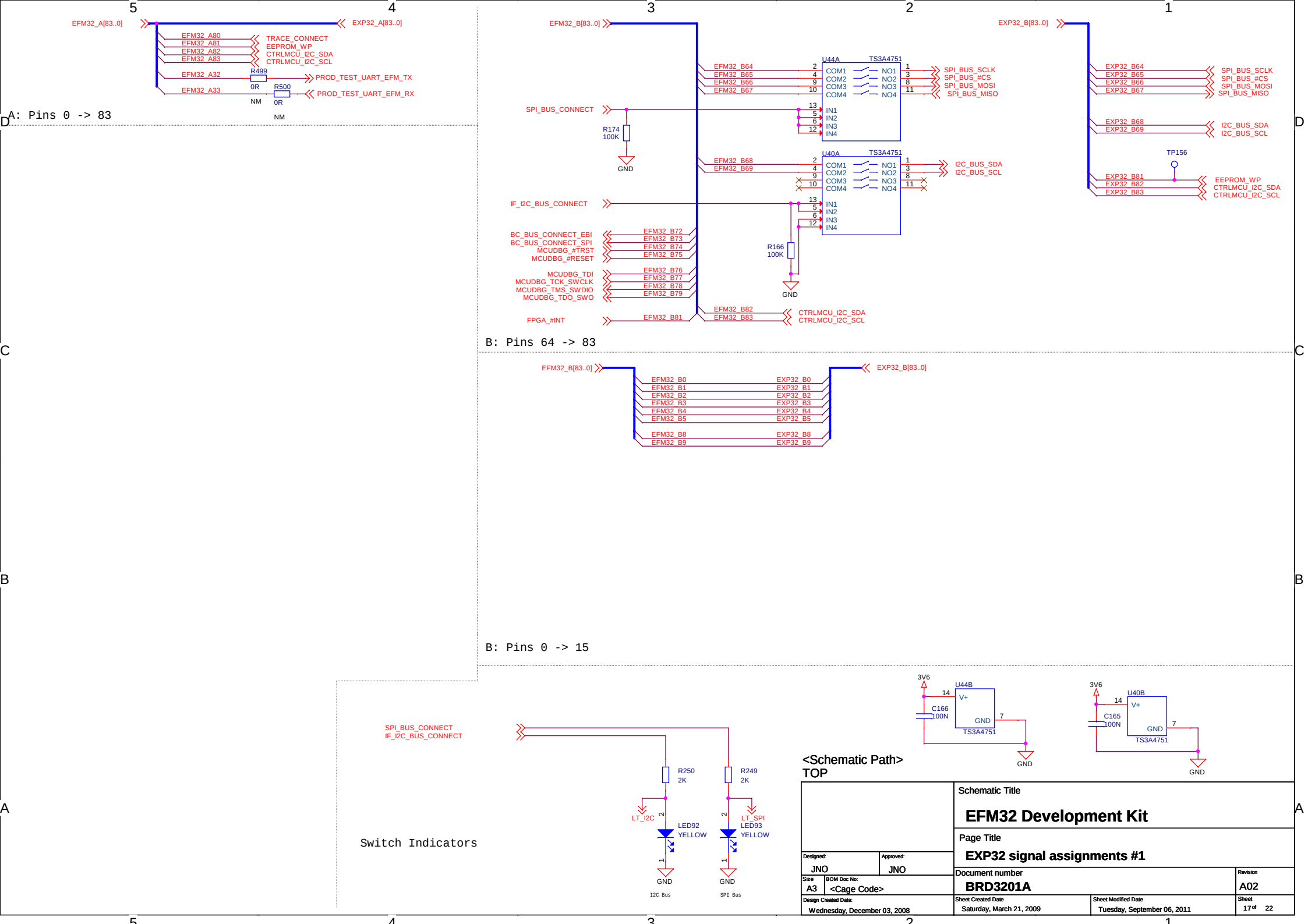
EFM32_A[83..0]
EXP32_A[83..0]
EFM32_A80
EFM32_A81
EFM32_A82
EFM32_A83
TRACE_CONNECT
EEPROM_WP
CTRLMCU_I2C_SDA
CTRLMCU_I2C_SCL
EFM32_A32
R499
0R
NM
PROD_TEST_UART_EFM_TX
EFM32_A33
R500
0R
NM
PROD_TEST_UART_EFM_RX
A: Pins 0 -> 83
EFM32_B[83..0]
EFM32_B64
EFM32_B65
EFM32_B66
EFM32_B67
U44A
TS3A4751
COM1
COM2
COM3
COM4
NO1
NO2
NO3
NO4
IN1
IN2
IN3
IN4
SPI_BUS_SCLK
SPI_BUS_#CS
SPI_BUS_MOSI
SPI_BUS_MISO
SPI_BUS_CONNECT
R174
100K
GND
EFM32_B68
EFM32_B69
U40A
I2C_BUS_SDA
I2C_BUS_SCL
IF_I2C_BUS_CONNECT
BC_BUS_CONNECT_EBI
BC_BUS_CONNECT_SPI
MCUDBG_#TRST
MCUDBG_#RESET
EFM32_B72
EFM32_B73
EFM32_B74
EFM32_B75
R166
100K
MCUDBG_TDI
MCUDBG_TCK_SWCLK
MCUDBG_TMS_SWDIO
MCUDBG_TDO_SWO
EFM32_B76
EFM32_B77
EFM32_B78
EFM32_B79
FPGA_#INT
EFM32_B81
EFM32_B82
EFM32_B83
CTRLMCU_I2C_SDA
CTRLMCU_I2C_SCL
B: Pins 64 -> 83
EXP32_B[83..0]
EXP32_B64
EXP32_B65
EXP32_B66
EXP32_B67
EXP32_B68
EXP32_B69
TP156
EXP32_B81
EXP32_B82
EXP32_B83
EEPROM_WP
CTRLMCU_I2C_SDA
CTRLMCU_I2C_SCL
EFM32_B0
EFM32_B1
EFM32_B2
EFM32_B3
EFM32_B4
EFM32_B5
EFM32_B8
EFM32_B9
EXP32_B0
EXP32_B1
EXP32_B2
EXP32_B3
EXP32_B4
EXP32_B5
EXP32_B8
EXP32_B9
B: Pins 0 -> 15
SPI_BUS_CONNECT
IF_I2C_BUS_CONNECT
R250
2K
R249
2K
LT_I2C
LT_SPI
LED92
LED93
YELLOW
GND
I2C Bus
SPI Bus
Switch Indicators
3V6
U44B
U40B
C166
100N
C165
100N
V+
GND
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EFM32 Development Kit
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EXP32 signal assignments #1
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Approved:
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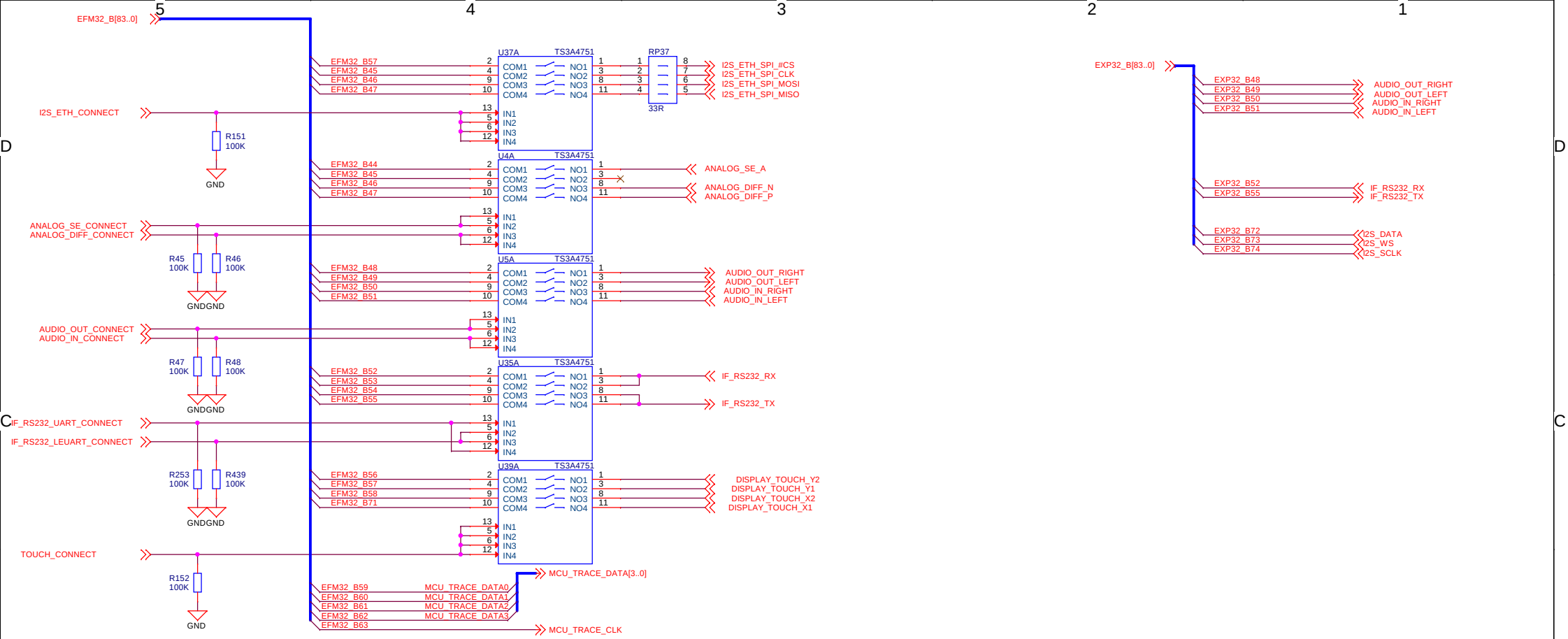
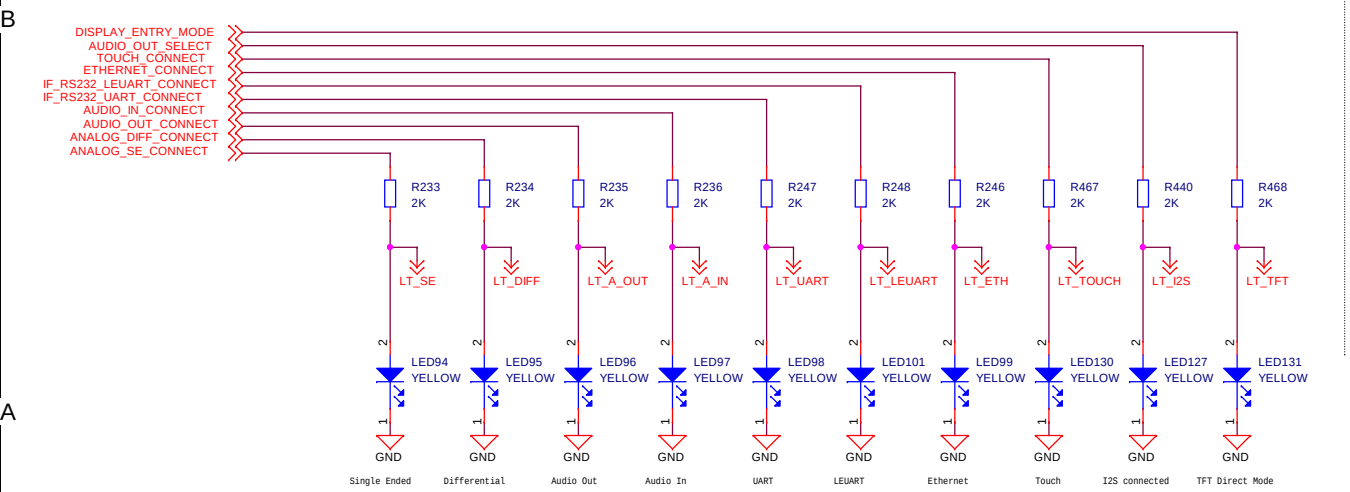
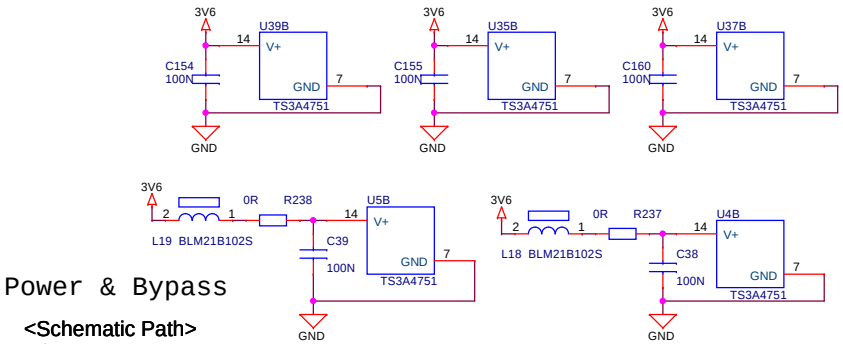


B: Pins 44 -> 63



Switch Indicators



Power & Bypass

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Schematic Title	**EFM32 Development Kit - Mainboard**
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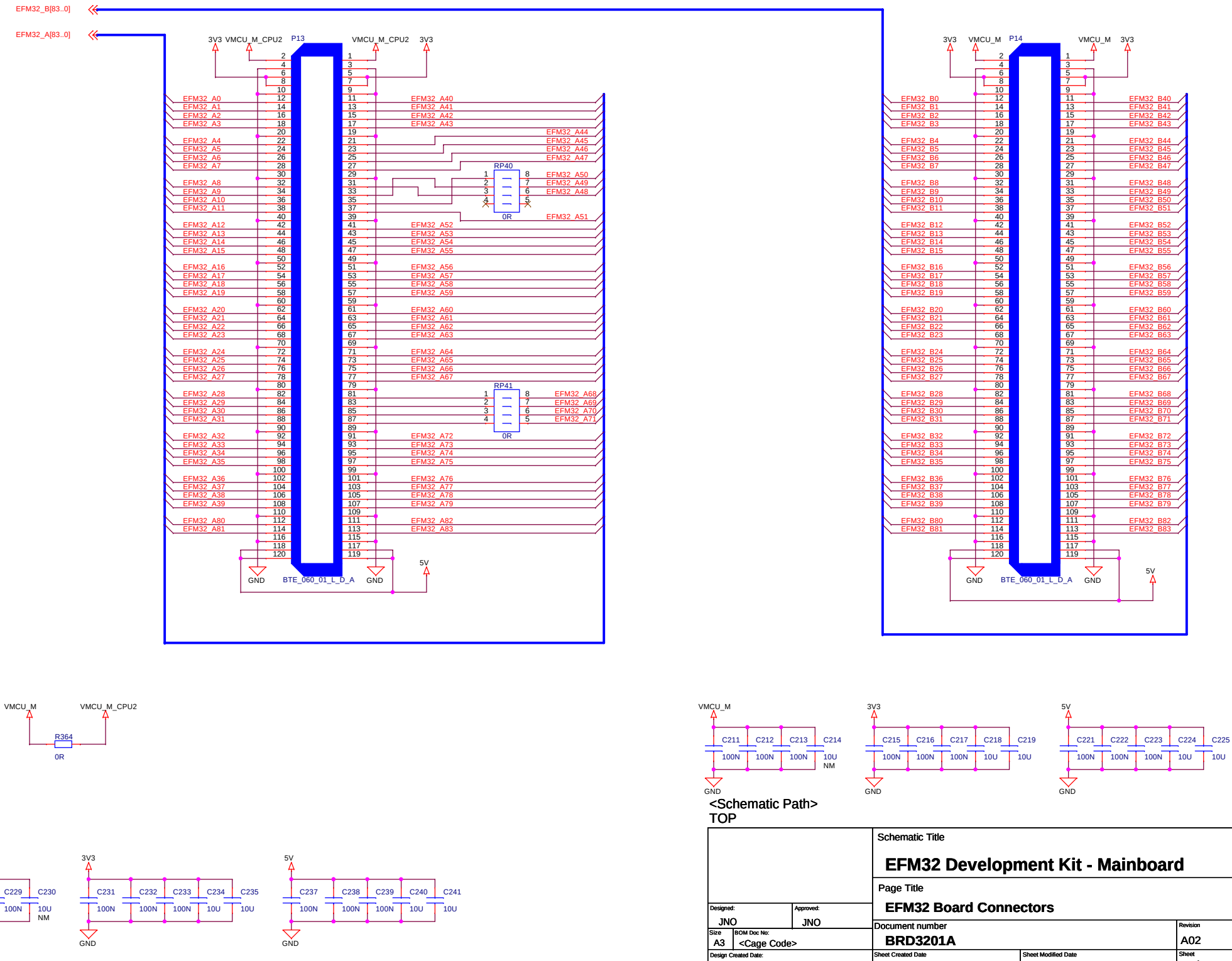

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Page Title	**EFM32 Board Connectors**
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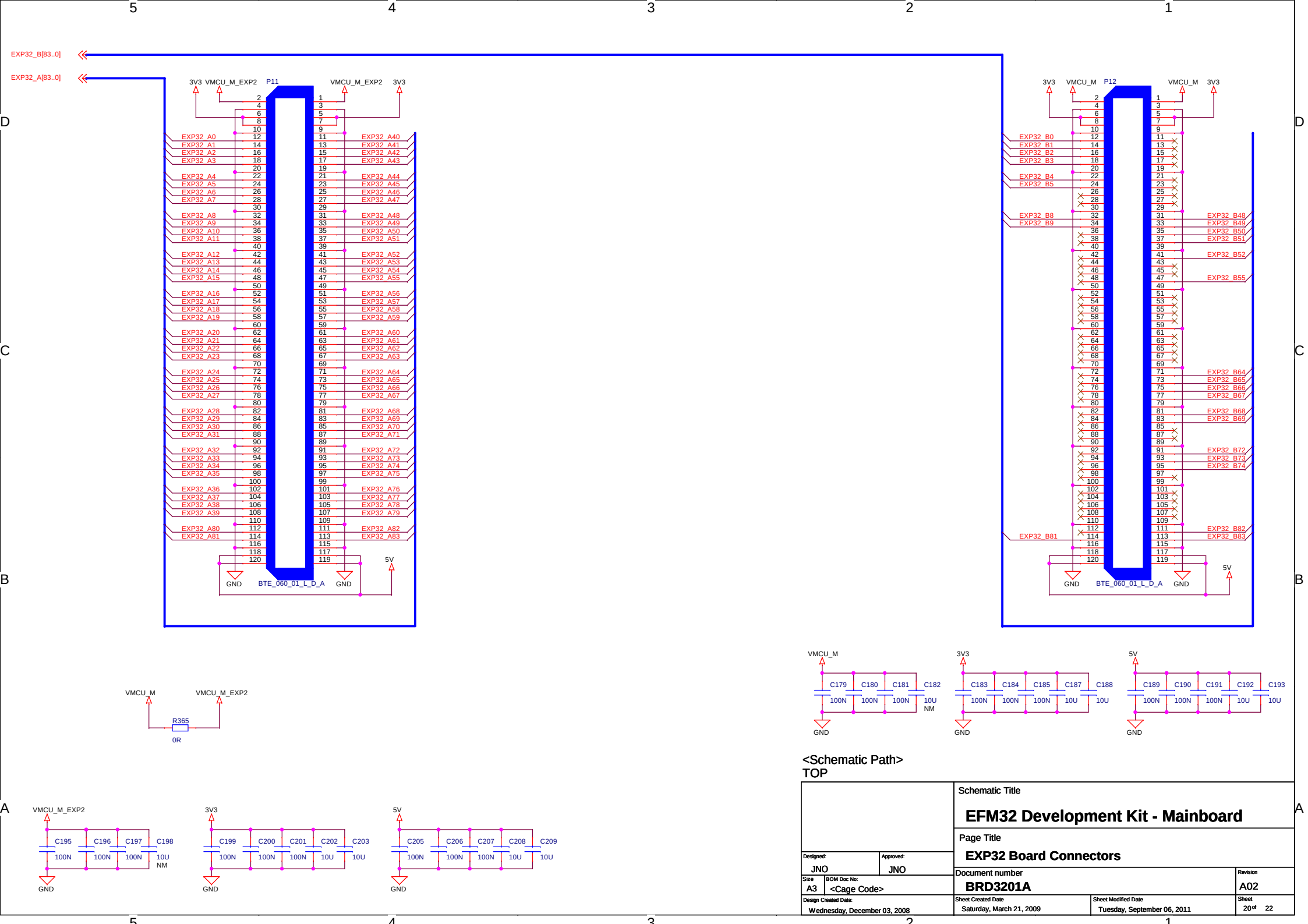

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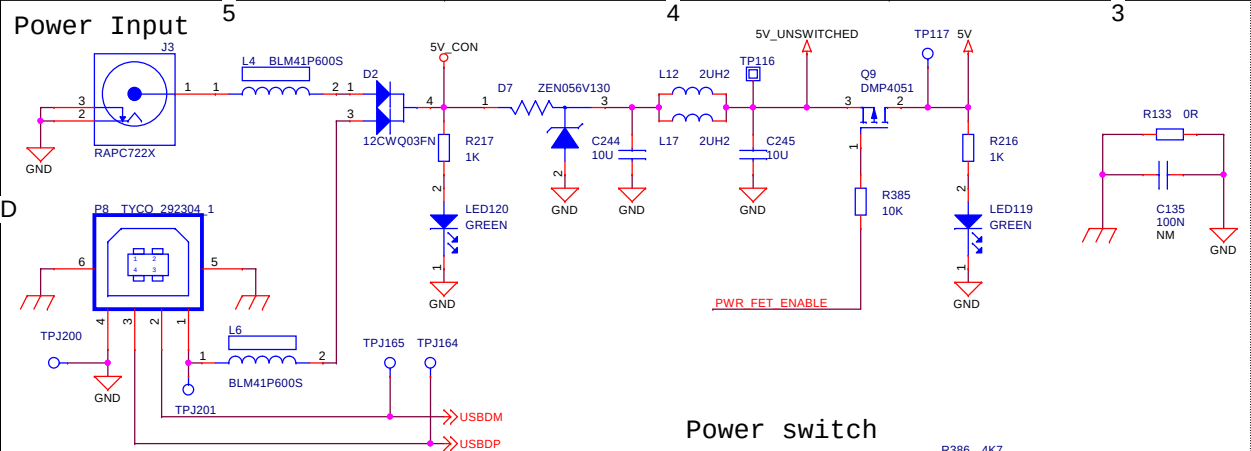
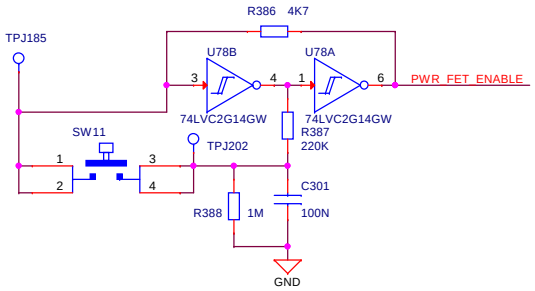
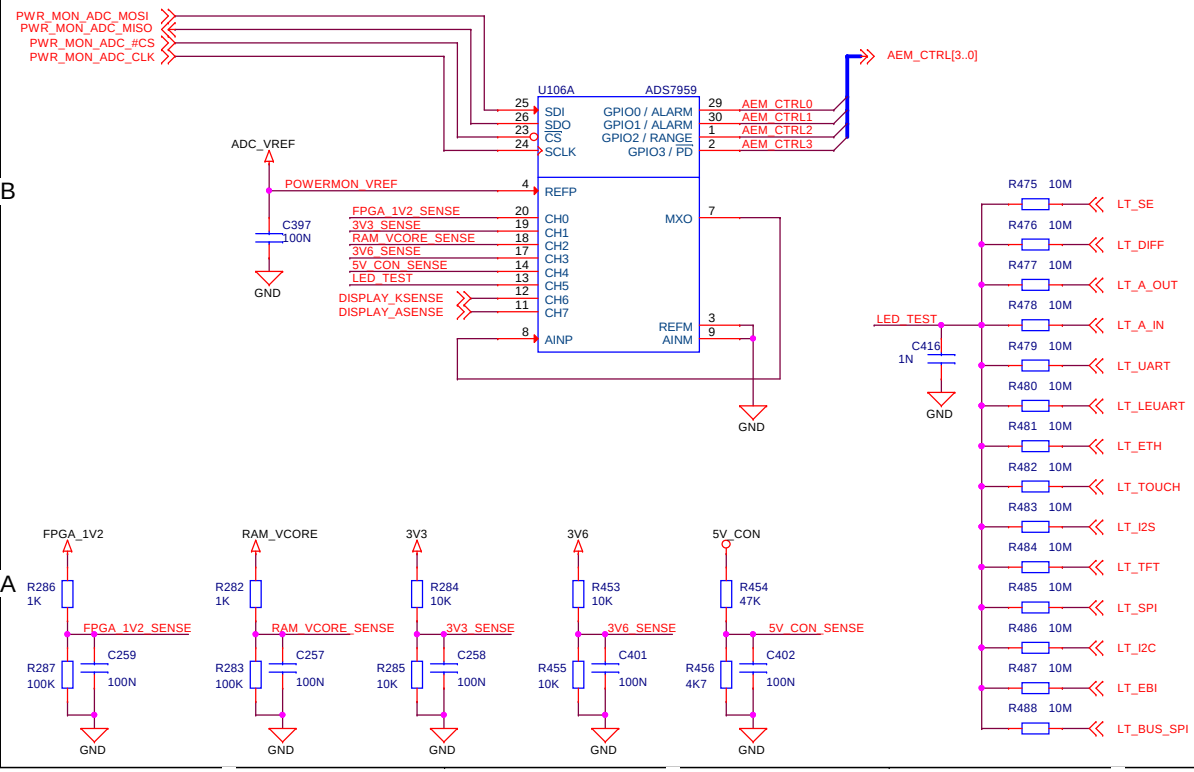
Power Input



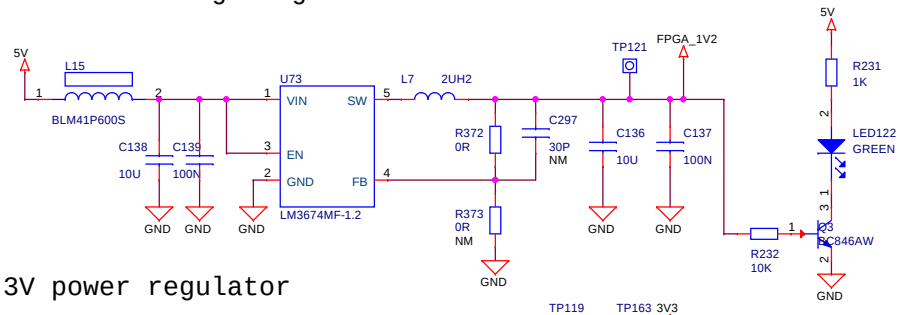
Power switch



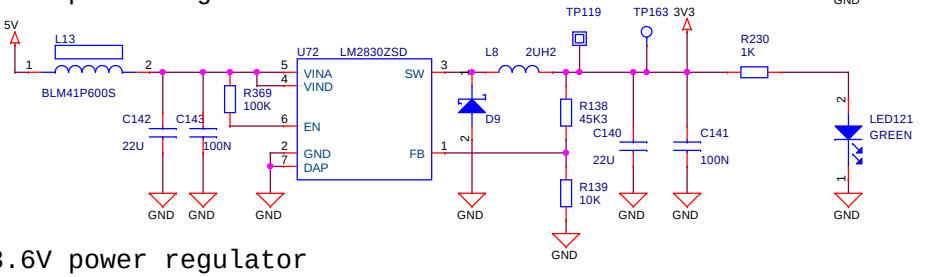
Power Monitoring



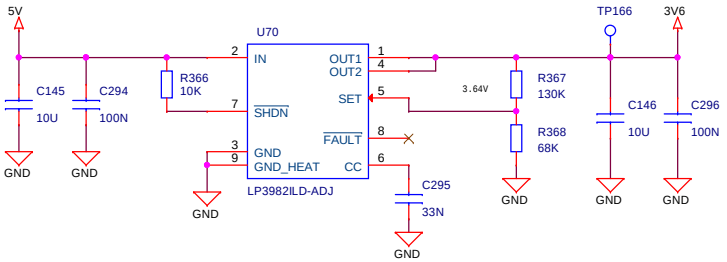
FPGA core voltage regulator



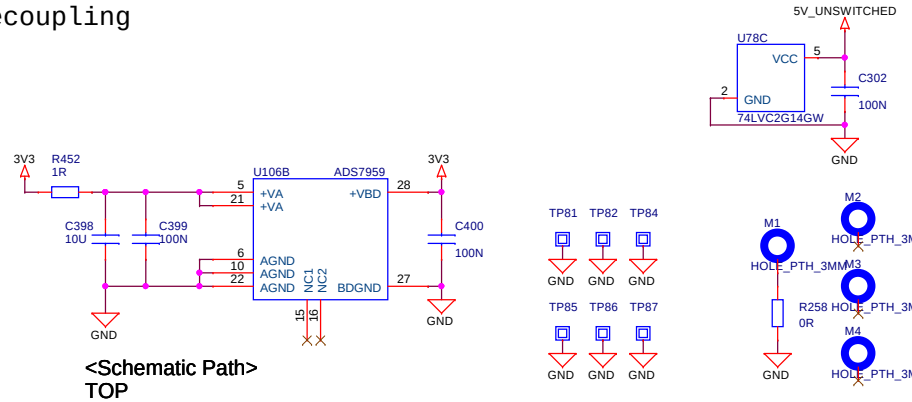
3.3V power regulator



3.6V power regulator



Decoupling



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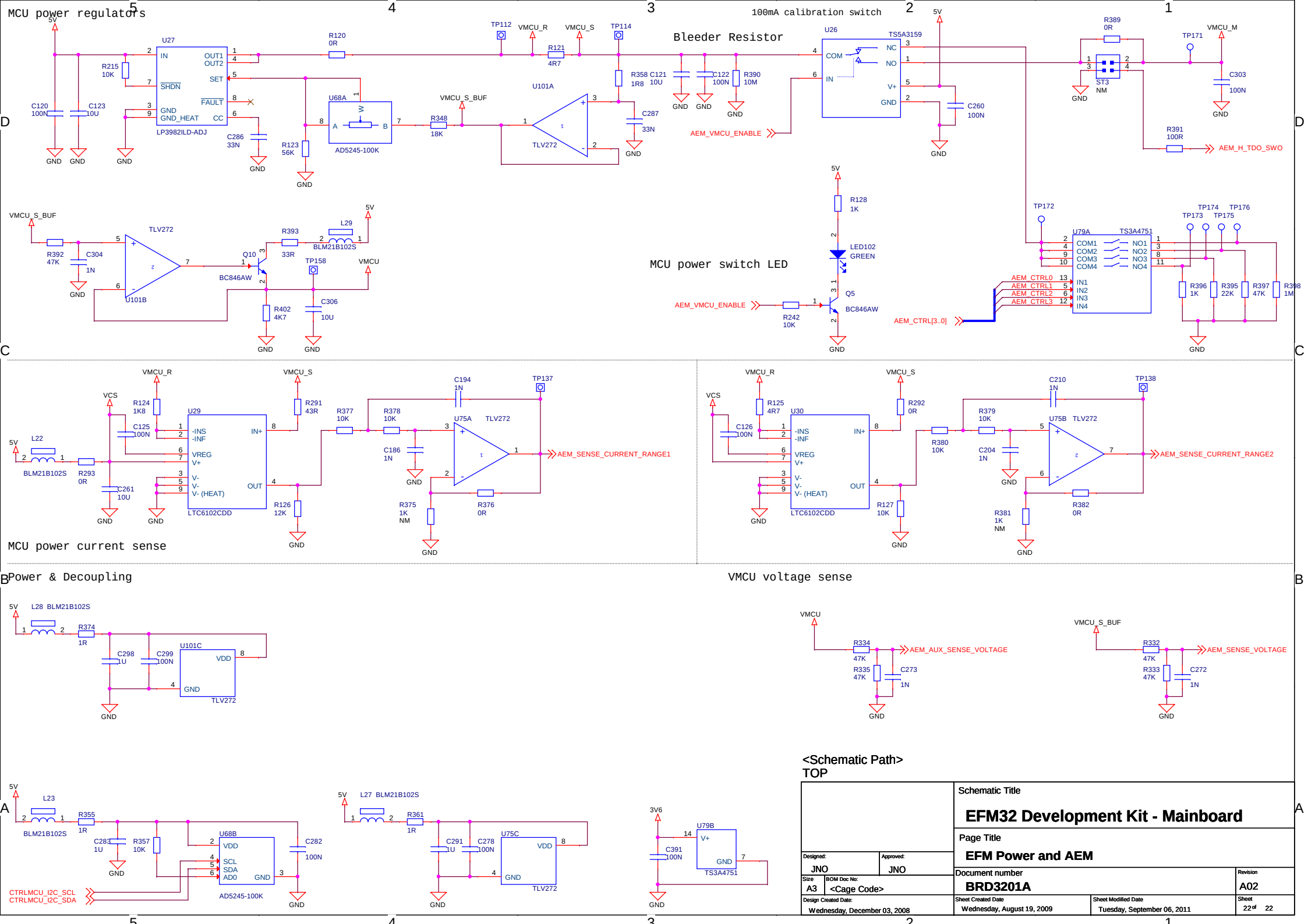

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