# RS9116 n-Link™ and WiSeConnect™ Wi-Fi® and Dual-Mode Bluetooth® 5 Wireless Connectivity B00 Module Solution

LGA Module (7.90 x 4.63) mm

## Overview

### 1.1 Features

**Wi-Fi**

- Compliant to single-spatial stream IEEE 802.11 b/g/n with single band support
- Support for 20 MHz channel bandwidth
- Transmit power up to +18 dBm with integrated PA
- Receive sensitivity as low as -96 dBm
- Data Rates: 802.11b: Up to 11 Mbps; 802.11g: Up to 54 Mbps; 802.11n: MCS0 to MCS7
- Operating Frequency Range: 2412 MHz – 2484 MHz

**Bluetooth**

- Transmit power up to +16 dBm with integrated PA
- Receive sensitivity: - LE: -92 dBm, LR 125 Kbps: -102 dBm
- Compliant to dual-mode Bluetooth 5
- <8 mA transmits current in Bluetooth 5 mode, 2 Mbps data rate
- Data rates: 125 Kbps, 500 Kbps, 1 Mbps, 2 Mbps, 3 Mbps
- Operating Frequency Range: 2.402 GHz - 2.480 GHz
- Bluetooth 2.1 + EDR, Bluetooth Low Energy 4.0 / 4.1 / 4.2 / 5.0
- Bluetooth Low Energy 1 Mbps, 2 Mbps and Long-Range modes
- Bluetooth Low Energy Secure connections
- Bluetooth Low Energy supports central role and peripheral role concurrently
- Bluetooth auto rate and auto TX power adaptation
- Scatternet* with two Secondary roles while still being visible

**RF Features**

- Integrated baseband processor with calibration memory, RF transceiver, high-power amplifier, balun, and T/R switch

**Power Consumption**

- Wi-Fi Standby Associated mode current: 55 uA @ 1 second beacon listen interval
- Wi-Fi 1 Mbps Listen current: 14 mA
- Wi-Fi LP chain Rx current: 19 mA
- Deep sleep current <1 uA, Standby current (RAM retention) < 10 uA

**Operating Conditions**

- Wide operating supply range: 1.75 V to 3.63 V
- RF Power Amplifier supports 3.0 V to 3.63 V
- Operating temperature: -40 ºC to +85 ºC (Industrial grade)

**Size**

- Small Form Factor: 7.90 x 4.63 x 0.9 mm

**Evaluation Kit**

- Single Band EVK: RS9116X-SB-EVK2

**Software Operating Modes**

- Hosted mode (n-Link™): Wi-Fi stack, Bluetooth stack and profiles and all network stacks reside on the host processor
- Embedded mode (WiSeConnect™): Wi-Fi stack, TCP/IP stack, IP modules, Bluetooth stack and some profiles reside in RS9116; Some of the Bluetooth profiles reside in the host processor

**Hosted Mode (n-Link™)**

- Available host interfaces: SDIO 2.0 and USB HS
- Application data throughput up to 50 Mbps (Hosted Mode) in 802.11n with 20MHz bandwidth.
- Host drivers for Linux
- Support for Client mode, Access point mode (Up to 16 clients), Concurrent Client and Access Point mode, Enterprise Security
- Support for concurrent Wi-Fi, dual-mode Bluetooth 5

**Embedded Mode (WiSeConnect™)**

- Available host interface: UART, SPI, and USB CDC, SDIO
- Support for Embedded Client mode, Access Point mode (Up to 8 clients), Concurrent Client and Access Point mode, and Enterprise Security

- Supports advanced security features: WPA2/WPA3 - Personal and WPA/WPA2 - Enterprise*
- Integrated TCP/IP stack, HTTP/HTTPS, SSL/TLS, MQTT
- Bluetooth inbuilt stack support for L2CAP, RFCOMM, SDP, SPP, GAP
- Bluetooth profile support for GAP, SDP, SPP, GATT, L2CAP, RFCOMM
- Wireless firmware update and provisioning
- Support for concurrent Wi-Fi, dual-mode Bluetooth 5

**Security**

- Accelerators: AES128/256 in Embedded Mode
- WPA2/WPA3 - Personal and WPA/WPA2 - Enterprise for Client*

**Software and Regulatory Certification**

- Wi-Fi Alliance*
- Bluetooth Qualification*
- Regulatory certifications (FCC, IC, CE/ETSI, MIC, and UKCA) *

* SW features depends on the firmware version. For a detailed list of software features and available profiles, refer to the Software Reference Manuals or contact Silicon Labs for availability.

All power and performance numbers are under ideal conditions.

## 1.2 Applications

**Wearables**

Smart Watches, Wristbands, Fitness Monitors, Smart Glasses, etc.

**Smart Home**

Smart Locks, Motion/Entrance Sensors, Water Leak Sensors, Smart Plugs/Switches, LED Lights, Door-Bell Cameras, Washers/Dryers, Refrigerators, Thermostats, Consumer Security Cameras, Voice Assistants, etc.

**Other Consumer Applications**

Toys, Anti-Theft Tags, Smart Dispensers, Weighing Scales, Blood Pressure Monitors, Blood Sugar Monitors, Portable Cameras, etc.

**Other Applications (Medical, Industrial, Retail, Agricultural, Smart City, etc.)**

Healthcare Tags, Medical Patches/Pills, Infusion Pumps, Sensors/Actuators in Manufacturing, Electronic Shelf Labels, Agricultural Sensors, Product Tracking Tags, Smart Meters, Parking Sensors, Street LED Lighting, Automotive After-Market, Security Cameras, etc.

## 1.3 Description

Silicon Labs' RS9116 single band B00 module provides a comprehensive multi-protocol wireless connectivity solution including 802.11 b/g/n (2.4 GHz), 802.11j, dual-mode Bluetooth 5. The module offers a high throughput and an extended range with power-optimized performance. The module is FCC, IC, MIC, ETSI/CE (including EN 300 328 v2.2.2), and UKCA certified.

## 1.4 Block Diagrams

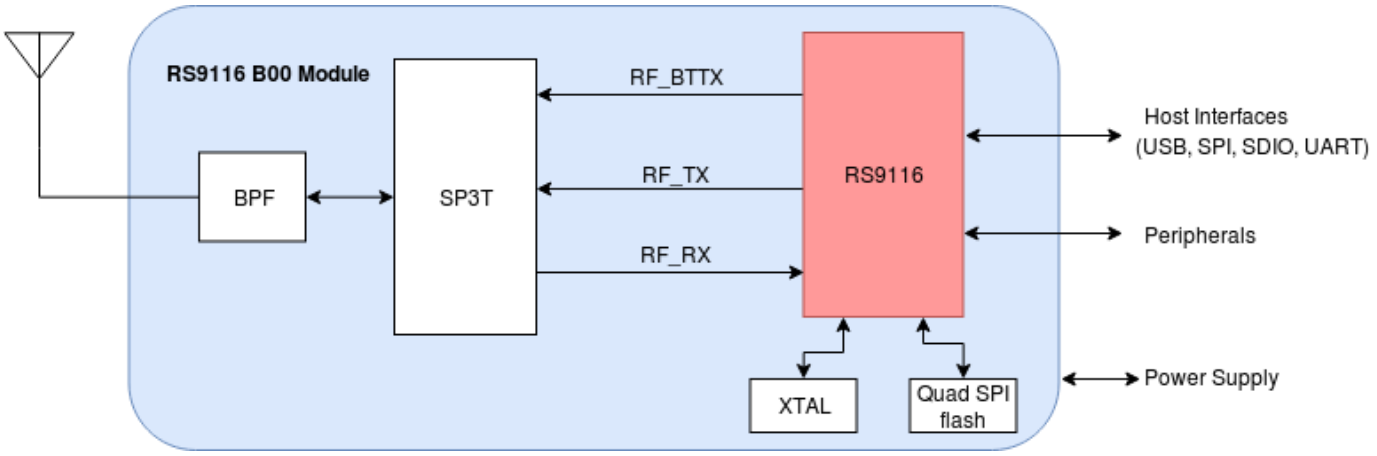


**Figure 1. B00 Module Block Diagram with Internal Flash**

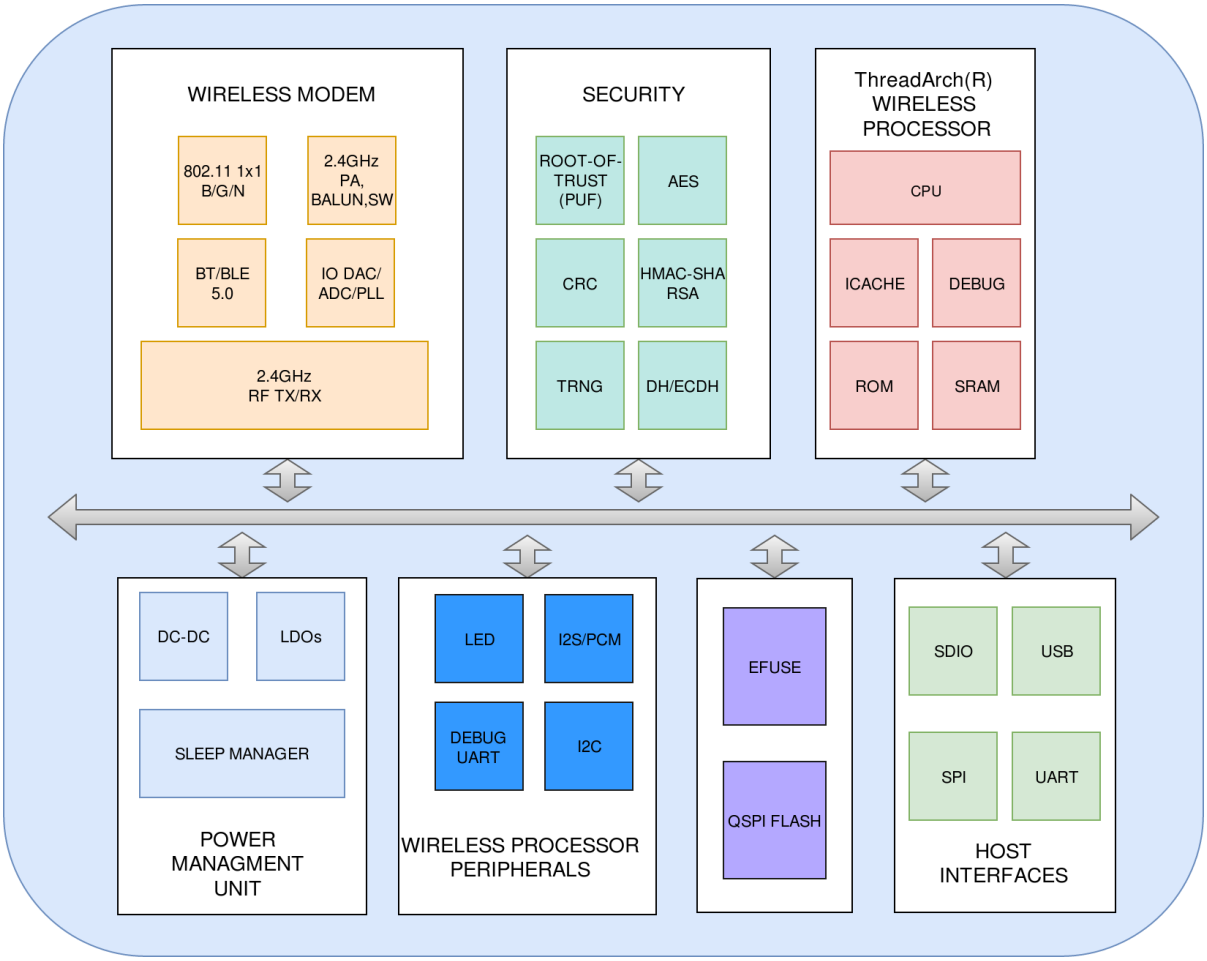


**Figure 2. RS9116 Connectivity Hardware Block Diagram**

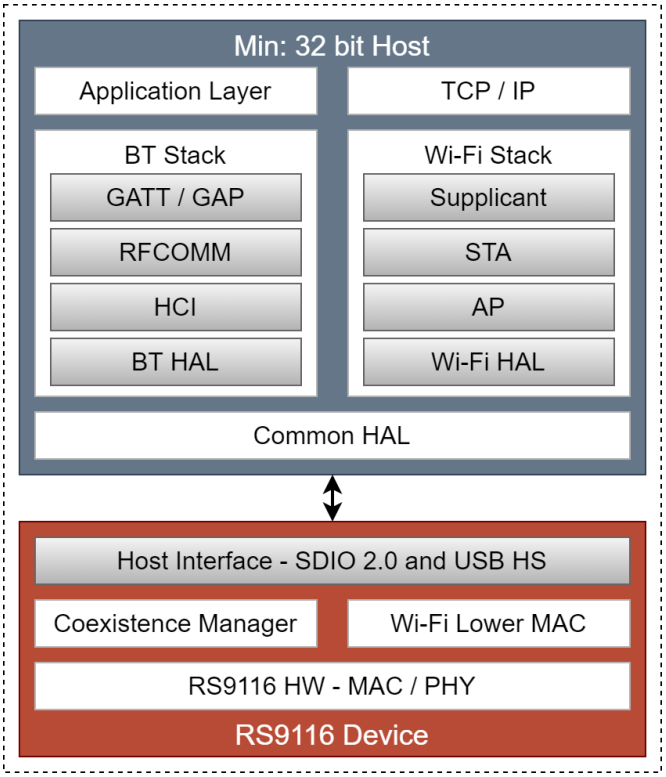


**Figure 3. Hosted Software Architecture**

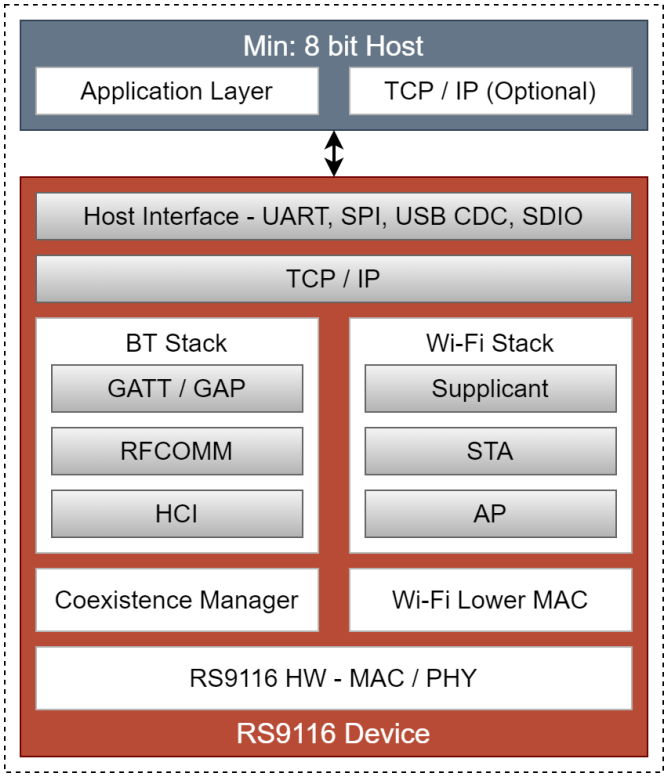


**Figure 4. Embedded Software Architecture**

Customer can connect multiple hosts, but only one host interface can be active after power-on.

**NOTE**: This content may contain offensive terminology that is now obsolete. Silicon Labs is replacing these terms with inclusive language wherever possible. For more information, visit www.silabs.com/about-us/inclusive-lexicon-project

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# 2 RS9116 B00 Module Pinout and Pin Description

## 2.1 Pin Diagram

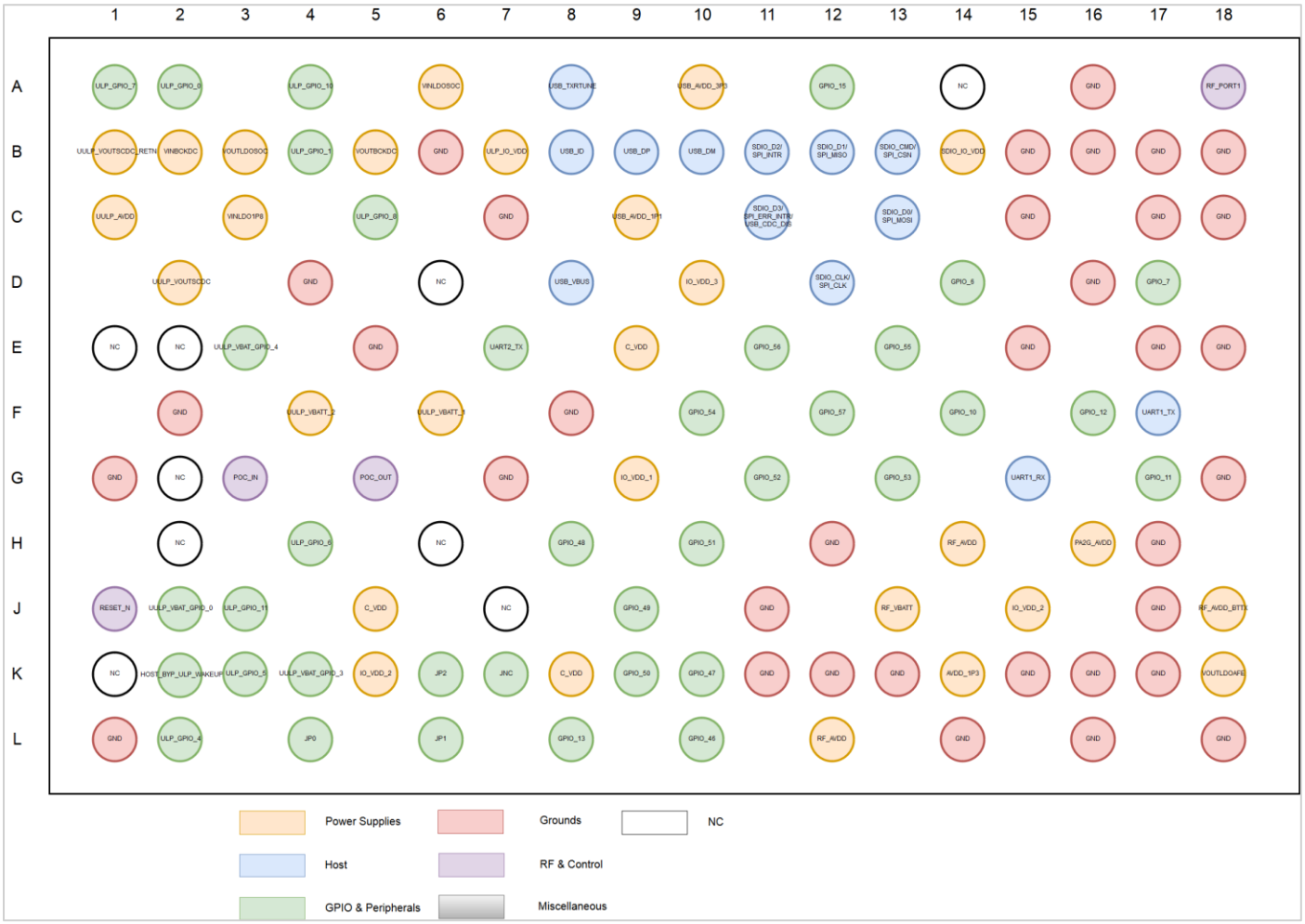



**Figure 5. RS9116 B00 Pin Diagram**

## 2.2 Pin Description

### 2.2.1 RF & Control Interfaces

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description |
|---|---|---|---|---|---|
| RF_PORT1 | A18 | NA | Inout | NA | Connect to Antenna with a 50 Ω impedance as per the Reference Schematics. |
| RESET_N | J1 | UULP_VBATT_1 | Input | NA | Active-low reset asynchronous reset signal. |
| POC_OUT | G5 | UULP_VBATT_1 | Output | NA | Power On Control Output.<br>This is internally generated. Initially, it is low. But it becomes high when the supplies (VBATT, UULP_VOUTSCDC) are valid. |
| POC_IN | G3 | UULP_VBATT_1 | Input | NA | Power On Control Input.<br>This is an input to the chip. It should be made high only after supplies are valid to ensure the IC is in safe state until valid power supply is available. |

**Table 1. RF & Control Interfaces**

### 2.2.2 Power & Ground Pins

| Pin Name | Type | Pin Number | Direction | Description |
|---|---|---|---|---|
| UULP_VBATT_1 | Power | F6 | Input | Always-on VBATT Power supply to the UULP domains |
| UULP_VBATT_2 | Power | F4 | Input | Always-on VBATT Power supply to the UULP domains |
| RF_VBATT | Power | J13 | Input | Always-on VBATT Power supply to the RF |
| VINBCKDC | Power | B2 | Input | Power supply for the on-chip Buck |
| VOUTBCKDC | Power | B5 | Output | Output of the on-chip Buck |

| Pin Name | Type | Pin Number | Direction | Description |
|---|---|---|---|---|
| VINLDOSOC | Power | A6 | Input | Power supply for SoC LDO. Connect to VOUTBCKDC as per the Reference Schematics |
| VOUTLDOSOC | Power | B3 | Output | Output of SoC LDO |
| VINLDO1P8 | Power | C3 | Input | Power supply for 1.8V LDO |
| VOUTLDOAFE | Power | K18 | Output | Output of AFE LDO |
| IO_VDD_1 | Power | G9 | Input | I/O Supply for GPIOs. Refer to the GPIOs section for details on which GPIOs have this as the I/O supply. |
| IO_VDD_2 | Power | J15, K5 | Input | I/O Supply for GPIOs. Refer to the GPIOs section for details on which GPIOs have this as the I/O supply. |
| IO_VDD_3 | Power | D10 | Input | I/O Supply for GPIOs. Refer to the GPIOs section for details on which GPIOs have this as the I/O supply. |
| SDIO_IO_VDD | Power | B14 | Input | I/O Supply for SDIO I/Os. Refer to the GPIOs section for details on which GPIOs have this as the I/O supply. |
| ULP_IO_VDD | Power | B7 | Input | I/O Supply for ULP GPIOs |
| PA2G_AVDD | Power | H16 | Input | Power supply for the 2.4 GHz RF Power Amplifier |
| RF_AVDD | Power | H14, L12 | Input | Power supply for the 2.4 GHz RF and AFE.Connect to VOUTBCKDC as per the Reference Schematics |
| RF_AVDD_BTTX | Power | J18 | Input | Power supply for Bluetooth Transmit circuit.Connect to VOUTLDOAFE as per the Reference Schematics. |
| AVDD_1P3 | Power | K14 | Input | Power supply for the 2.4 GHz RF.Connect to VOUTBCKDC as per the Reference Schematics. |
| UULP_VOUTSCDC | Power | D2 | Output | UULP Switched Cap DCDC Output |
| UULP_VOUTSCDC_RETN | Power | B1 | Output | UULP Retention Supply Output |
| UULP_AVDD | Power | C1 | Input | Power supply for the always-on digital and ULP peripherals. Connect to UULP_VOUTSCDC as per the Reference Schematics. |
| C_VDD | Power | E9, J5, K8 | Input | Power supply for the digital core. Connect to the VOUTLDOSOC as per the Reference Schematics. |

| Pin Name | Type | Pin Number | Direction | Description |
|---|---|---|---|---|
| USB_AVDD_3P3 | Power | A10 | Input | Power Supply for the USB interface |
| USB_AVDD_1P1 | Power | C9 | Input | Power supply for the USB core |
| GND | Ground | A16, B6, B15, B16, B17, B18, C7, C15, C17, C18, D4, D16, E5, E15, E17, E18, F2, F8, G1, G7, G18, H12, H17, J11, J17, K11, K12, K13, K15, K16, K17, L1, L14, L16, L18 | GND | Common ground pins |

**Table 2. Power and Ground Pins**

### 2.2.3 Host & Peripheral Interfaces

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description [1,2,3,4] |
|---|---|---|---|---|---|
| GPIO_6 | D14 | IO_VDD_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ<br>This pin can be configured by software to be any of the following<br>• I2S_DOUT - I2S interface output data.<br>• PCM_DOUT - PCM interface output data. |
| GPIO_7 | D17 | IO_VDD_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ<br>This pin can be configured by software to be any of the following<br>• I2S_CLK - I2S interface clock.<br>• PCM_CLK - PCM interface clock. |
| GPIO_8/UART1_RX | G15 | IO_VDD_1 | Inout | HighZ | **Host** / **Default** / **Sleep**<br>UART / UART1_RX - UART Host / HighZ |

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description [1,2,3,4] |
|---|---|---|---|---|---|
| | | | | | <table><tr><td></td><td>interface serial input.</td><td></td></tr><tr><td>Non UART</td><td>HighZ</td><td>HighZ</td></tr></table> The UART interface is supported only in WiSeConnect™. |
| GPIO_9/UART1_TX | F17 | IO_VDD_1 | Inout | HighZ | <table><tr><th>Host</th><th>Default</th><th>Sleep</th></tr><tr><td>UART</td><td>UART1_TX - UART Host interface serial output.</td><td>HighZ</td></tr><tr><td>Non UART</td><td>HighZ</td><td>HighZ</td></tr></table> The UART interface is supported only in WiSeConnect™. |
| GPIO_10 | F14 | IO_VDD_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ<br>This pin can be configured by software to be any of the following<br>• I2S_DIN: I2S interface input data.<br>• PCM_DIN - PCM interface input data. |
| GPIO_11 | G17 | IO_VDD_3 | Inout | HighZ | **Default:** HighZ.<br>**Sleep**: HighZ<br>This pin can be configured by software to be any of the following<br>• I2S_WS: I2S interface Word Select.<br>• PCM_FSYNC: PCM interface Frame Synchronization signal. |
| GPIO_12 | F16 | IO_VDD_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ |

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description [1,2,3,4] |
|---|---|---|---|---|---|
| | | | | | This pin can be configured by software to be any of the following<br>• UART1_RTS - UART interface Request to Send output, if UART Host Interface flow control is enabled.<br>The UART interface is supported only in WiSeConnect™. |
| GPIO_13 | L8 | IO_VDD_3 | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ<br>This pin can be configured by software to be any of the following<br>• EXT_FLASH_RESET - Reset signal to an external Flash IC, if connected |
| GPIO_15 | A12 | IO_VDD_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ<br>This pin can be configured by software to be any of the following<br>• UART1_CTS - UART interface Clear to Send input, if UART Host Interface flow control is enabled.<br>• UART1_TRANSPARENT_MODE - UART Host interface Transparent Mode, Indication that module has entered into TRANSPERENT_MODE<br>• TSF_SYNC - Transmit Synchronization Function signal to indicate to the Host when a packet is transmitted. The signal is toggled once at the end of every transmitted packet.<br>The UART interface is supported only in WiSeConnect™. |

<table>
<tr><th>Pin Name</th><th>Pin Number</th><th>I/O Supply Domain</th><th>Direction</th><th>Initial State (Power up, Active Reset)</th><th>Description [1,2,3,4]</th></tr>
<tr><td>SDIO_CLK/SPI_CLK</td><td>D12</td><td>SDIO_IO_VDD</td><td>Inout</td><td>HighZ</td><td>
<table>
<tr><th>Host</th><th>Default</th><th>Sleep</th></tr>
<tr><td>SDIO</td><td>SDIO_CLK - SDIO interface clock</td><td>HighZ</td></tr>
<tr><td>SPI</td><td>SPI_CLK - SPI Secondary interface clock</td><td>HighZ</td></tr>
<tr><td>Non SDIO, SPI</td><td>HighZ</td><td>HighZ</td></tr>
</table>
The SPI interface is supported only in WiSeConnect™.
</td></tr>
<tr><td>SDIO_CMD/SPI_CSN</td><td>B13</td><td>SDIO_IO_VDD</td><td>Inout</td><td>HighZ</td><td>
<table>
<tr><th>Host</th><th>Default</th><th>Sleep</th></tr>
<tr><td>SDIO</td><td>SDIO_CMD - SDIO interface CMD signal</td><td>HighZ</td></tr>
<tr><td>SPI</td><td>SPI_CSN - Active-low Chip Select signal of SPI Secondary interface</td><td>HighZ</td></tr>
<tr><td>Non SDIO, SPI</td><td>HighZ</td><td>HighZ</td></tr>
</table>
The SPI interface is supported only in WiSeConnect™.
</td></tr>
<tr><td>SDIO_D0/SPI_MOSI</td><td>C13</td><td>SDIO_IO_VDD</td><td>Inout</td><td>HighZ</td><td>
<table>
<tr><th>Host</th><th>Default</th><th>Sleep</th></tr>
<tr><td>SDIO</td><td>SDIO_D0 - SDIO</td><td>HighZ</td></tr>
</table>
</td></tr>
</table>

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description [1,2,3,4] |
|---|---|---|---|---|---|
| | | | | | interface Data0 signal |
| | | | | | SPI: SPI_MOSI - SPI Secondary interface Main-Out-Secondary - In signal; HighZ; HighZ |
| | | | | | Non SDIO, SPI: HighZ; HighZ |
| | | | | | The SPI interface is supported only in WiSeConnect™. |
| SDIO_D1/SPI_MISO | B12 | SDIO_IO_VDD | Inout | HighZ | **Host / Default / Sleep** |
| | | | | | SDIO: SDIO_D1 - SDIO interface Data1 signal; HighZ |
| | | | | | SPI: SPI_MISO - SPI Secondary interface Main-In-Secondary - Out signal; HighZ |
| | | | | | Non SDIO, SPI: HighZ; HighZ |
| | | | | | The SPI interface is supported only in WiSeConnect™. |
| SDIO_D2/SPI_INTR | B11 | SDIO_IO_VDD | Inout | HighZ | **Host / Default / Sleep** |
| | | | | | SDIO: SDIO_D2 - SDIO; HighZ |

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description [1,2,3,4] |
|---|---|---|---|---|---|
| | | | | | interface Data2 signal |
| | | | | | SPI: SPI_INTR - SPI Secondary interface Interrupt Signal to the Host; HighZ |
| | | | | | Non SDIO, SPI: HighZ; HighZ |
| | | | | | The SPI interface is supported only in WiSeConnect™. |
| SDIO_D3/ USB_CDC_DIS | C11 | SDIO_IO_VDD | Inout | Pullup | **Host / Default / Sleep** |
| | | | | | SDIO: SDIO_D3 - SDIO interface Data3 signal; HighZ |
| | | | | | USB: USB_CDC_DIS - USB-CDC Active-High Disable Signal; HighZ |
| | | | | | Non SDIO, SPI, USB: HighZ; HighZ |
| | | | | | The SPI interface is supported only in WiSeConnect™. |
| GPIO_46 | L10 | IO_VDD_1 | Inout | HighZ | **Part Number / Default / Sleep** |
| | | | | | RS9116W-SB00-B00-ABC: HighZ; HighZ |

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description [1,2,3,4] |
|---|---|---|---|---|---|
| GPIO_47 | K10 | IO_VDD_1 | Inout | HighZ | **Part Number** / **Default** / **Sleep**<br>RS9116W-SB00-B00-ABC / HighZ / HighZ |
| GPIO_48 | H8 | IO_VDD_1 | Inout | HighZ | **Part Number** / **Default** / **Sleep**<br>RS9116W-SB00-B00-ABC / HighZ / HighZ |
| GPIO_49 | J9 | IO_VDD_1 | Inout | HighZ | **Part Number** / **Default** / **Sleep**<br>RS9116W-SB00-B00-ABC / HighZ / HighZ |
| GPIO_50 | K9 | IO_VDD_1 | Inout | HighZ | **Part Number** / **Default** / **Sleep**<br>RS9116W-SB00-B00-ABC / HighZ / HighZ |
| GPIO_51 | H10 | IO_VDD_1 | Inout | HighZ | **Part Number** / **Default** / **Sleep**<br>RS9116W-SB00-B00-ABC / HighZ / HighZ |
| GPIO_52 | G11 | IO_VDD_1 | Inout | HighZ | **Default:** HighZ |

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description [1,2,3,4] |
|---|---|---|---|---|---|
| | | | | | **Sleep**: HighZ |
| GPIO_53 | G13 | IO_VDD_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ |
| GPIO_54 | F10 | IO_VDD_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ |
| GPIO_55 | E13 | IO_VDD_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ |
| GPIO_56 | E11 | IO_VDD_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ |
| GPIO_57 | F12 | IO_VDD_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ |
| ULP_GPIO_0 | A2 | ULP_IO_VDD | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ<br>This pin can be configured by software to be any of the following<br>• WLAN_ACTIVE*: Active-High signal to indicate to an external Bluetooth IC that WLAN transmission is active. Part of the 3-wire coexistence interface.<br>*This pin is intended to act as WLAN_ACTIVE for wireless coexistence. It is however not available in the current firmware. Please contact Silicon Labs to learn about availability in the future versions. |
| ULP_GPIO_1 | B4 | ULP_IO_VDD | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ<br>This pin can be configured by software to be any of the following |

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description [1,2,3,4] |
|---|---|---|---|---|---|
| | | | | | • BT_ACTIVE*: Active-High signal from an external Bluetooth IC that it is transmitting. Part of the 3-wire coexistence interface.<br>*This pin is intended to act as BT_ACTIVE for Bluetooth coexistence. It is however not available in the current firmware. Please contact Silicon Labs to learn about availability in the future versions. |
| ULP_GPIO_4 | L2 | ULP_IO_VDD | Inout | HighZ | **Default:** HighZ |
| ULP_GPIO_5 | K3 | ULP_IO_VDD | Inout | HighZ | **Default:** LP_WAKEUP_IN This is LP Powersave Wakeup indication from Device<br>**Sleep**: HighZ<br>This pin can be configured by software to be any of the following<br>• LP_WAKEUP_IN: This is LP Powersave Wakeup indication to Device from HOST<br>• HOST_WAKEUP_INDICATION: This is used as indication from Host to dev that host is ready to take the packet and Device can transfer the packet to host. This is supported only in UART host mode.<br>The UART interface is supported only in WiSeConnect™. |
| ULP_GPIO_6 | H4 | ULP_IO_VDD | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ<br>This pin can be configured by software to be any of the following<br>• WAKEUP_FROM_Dev* - Used as a wakeup indication to host from device |

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description [1,2,3,4] |
|---|---|---|---|---|---|
| | | | | | • BT_PRIORITY**: Active-high signal from an external Bluetooth IC that indicates that the Bluetooth transmissions are a higher priority.<br>*For Wake-on-Wireless, it is recommended to use an external weak pull-down or pull-up resistor. It is recommended to use weak pull-down resistor in new designs. Software has to be configured suitably for using either pull-down or pull-up resistor.<br>**This pin is intended to act as BT_PRIORITY for Bluetooth coexistence. It is however not available in the current firmware. Please contact Silicon Labs to learn about availability in the future versions. |
| ULP_GPIO_7 | A1 | ULP_IO_VDD | Inout | HighZ | **Default:** HighZ |
| ULP_GPIO_8 | C5 | ULP_IO_VDD | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ<br>This pin can be configured by software to be any of the following<br>• LED0: Control signal to an external LED.<br>• (*LED0 functionality currently not available in both, WiSeConnect™ and n-Link® modules) |
| ULP_GPIO_9/ UART2_TX | E7 | ULP_IO_VDD | Inout | HighZ | **Default:** UART2_TX- Debug UART Interface serial output<br>**Sleep**: HighZ<br>UART2_TX: Debug UART interface serial output. |
| ULP_GPIO_10 | A4 | ULP_IO_VDD | Inout | HighZ | **Default:** HighZ |

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description [1,2,3,4] |
|---|---|---|---|---|---|
| | | | | | **Sleep**: HighZ<br>This pin can be configured by software to be any of the following<br>• I2C_SCL: I2C interface clock. |
| ULP_GPIO_11 | J3 | ULP_IO_VDD | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ<br>This pin can be configured by software to be any of the following<br>• I2C_SDA: I2C interface data. |
| UULP_VBAT_GPIO_0 | J2 | UULP_VBATT_1 | Output | High | **Default:** EXT_PG_EN<br>**Sleep**: SLEEP_IND_FROM_DEV / EXT_PG_EN<br>This pin can be configured by software to be any of the following<br>• SLEEP_IND_FROM_DEV: This signal is used to send an indication to the Host processor. An indication is sent when the chip enters (logic low) and exits (logic high) the ULP Sleep mode.<br>• EXT_PG_EN: Active-high enable signal to an external power gate which can be used to control the power supplies other than Always-ON VBATT Power Supplies in ULP Sleep mode. |
| UULP_VBAT_GPIO_2/ HOST_BYP_ULP_WAKEUP | K2 | UULP_VBATT_1 | Input | HighZ | **Default:** HOST_BYP<br>**Sleep**: ULP_WAKEUP<br>This signal has two functionalities – one during the bootloading process and one after the bootloading. During bootloading, this signal is an active-high input to indicate that the bootloader should bypass any inputs from the Host processor and |

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description [1,2,3,4] |
|---|---|---|---|---|---|
| | | | | | continue to load the default firmware from Flash. After bootloading, this signal is an active-high input to indicate that the module should wakeup from its Ultra Low Power (ULP) sleep mode. The bootloader bypass functionality is supported only in WiSeConnect™. |
| UULP_VBAT_GPIO_3 | K4 | UULP_VBATT_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep**: XTAL_32KHZ_IN / SLEEP_IND_FROM_DEV<br>This pin can be configured by software to be any of the following<br>• XTAL_32KHZ_IN: This pin can be used to feed external clock from a host processor or from external crystal oscillator<br>• SLEEP_IND_FROM_DEV: This signal is used to send an indication to the Host processor. An indication is sent when the chip enters (logic low) and exits (logic high) the ULP Sleep mode. |
| UULP_VBAT_GPIO_4 | E3 | UULP_VBATT_1 | Inout | HighZ | **Default:** HighZ<br>**Sleep**: HighZ<br>This pin can be configured by software to be any of the following<br>• XTAL_32KHZ_IN: This pin can be used to feed external clock from a host processor or from external crystal oscillator |
| JP0 | L4 | VIN_3P3 | Input | Pullup | **Default:** JP0<br>**Sleep**: HighZ<br>JP0 - Reserved. Connect to a test point for debug purposes. |

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description [1,2,3,4] |
|---|---|---|---|---|---|
| JP1 | L6 | VIN_3P3 | Input | Pullup | **Default:** JP1<br>**Sleep**: HighZ<br>JP1 - Reserved. Connect to a test point for debug purposes. |
| JP2 | K6 | VIN_3P3 | Input | Pullup | **Default:** JP2<br>**Sleep**: HighZ<br>JP2 - Reserved. Connect to a test point for debug purposes. |
| JNC | K7 | VIN_3P3 | NC | Pullup | **Default:** JNC<br>**Sleep**: HighZ<br>JNC - Reserved. Connect to a test point for debug purposes. |
| USB_DP | B9 | USB_AVDD_3P3 | Inout | NA | Positive data channel from the USB connector. |
| USB_DM | B10 | USB_AVDD_3P3 | Inout | NA | Negative data channel from the USB connector. |
| USB_ID | B8 | USB_AVDD_3P3 | Input | NA | ID signal from the USB connector.<br>If USB_ID pin is not connected to the host, then use a weak-pull down resistor on this pin. |
| USB_VBUS | D8 | USB_AVDD_3P3 | Input | NA | 5V USB VBUS signal from the USB connector. This pin is used just for detecting USB. |
| USB_TXRTUNE | A8 | USB_AVDD_3P3 | Input | NA | USB Transmitter resistor tune analog signal which needs to be connected to an external 200 Ω resistor to adjusts the USB's high-speed source impedance |

**Table 3. Host and Peripheral Interfaces**

1. **"Default"** state refers to the state of the device after initial boot loading and firmware loading is complete.
2. **"Sleep"** state refers to the state of the device after entering Sleep state which is indicated by Active-Low "SLEEP_IND_FROM_DEV" signal.
3. Please refer to **" RS9116N Open-Source Driver Technical Reference Manual "** for software programming information in hosted mode.
4. Please refer to **" RS9116W SAPI Programming Reference Manual "** for software programming information in embedded mode.
5. There are some functionalities, such as SLEEP_IND_FROM_DEV, that are available on multiple pins. However, these pins have other multiplexed functionalities. Any pin can be used based on the required functionality. Customer must note the default states before using appropriate pin.
6. In the application, wherever RS9116 is connected to external host, during power-off state, the host should ensure that all the pins (analog or digital) connected to the RS9116 are not driven. Else, the pins must be grounded.
7. JP0, JP1, JP2 and JNC are reserved. Connect these pins to test points for debug purposes. Do not drive these pins.

### 2.2.4 Miscellaneous Pins

| Pin Name | Pin Number | I/O Supply Domain | Direction | Initial State (Power up, Active Reset) | Description |
|---|---|---|---|---|---|
| NC | A14, D6, E1, E2, H2, H6, G2, J7, K1 | NA | NA | NA | No connect. |

**Table 4. Miscellaneous Pins**

# 3 RS9116 B00 Module Specifications

## 3.1 Absolute Maximum Ratings

Functional operation above maximum ratings are not guaranteed and may damage the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{store}$ | Storage temperature | -40 | +125 | ºC |
| $T_{j(max)}$ | Maximum junction temperature | - | +125 | ºC |
| UULP_VBATT_1 | Always-on VBATT supply to the UULP Domains | -0.5 | 3.63 | V |
| UULP_VBATT_2 | Always-on VBATT supply to the UULP Domains | -0.5 | 3.63 | V |
| RF_VBATT | Always-on VBATT Power supply to the RF | -0.5 | 3.63 | V |
| VINBCKDC | Power supply for the on-chip Buck | -0.5 | 3.63 | V |
| FBDC1P3 | Feedback signal for on-chip Buck | -0.5 | 1.8 | V |
| VINLDOSOC | Power supply for SoC LDO | -0.5 | 1.8 | V |
| VINLDO1P8 | Power supply for 1.8V LDO | -0.5 | 3.63 | V |
| IO_VDD_1 | I/O supplies for GPIOs | -0.5 | 3.63 | V |
| IO_VDD_2 | I/O supplies for GPIOs | -0.5 | 3.63 | V |
| IO_VDD_3 | I/O supplies for GPIOs | -0.5 | 3.63 | V |
| SDIO_IO_VDD | I/O supplies for SDIO I/Os | -0.5 | 3.63 | V |
| ULP_IO_VDD | I/O supplies for ULP GPIOs | -0.5 | 3.63 | V |
| PA2G_AVDD | Power supply for the 2.4 GHz RF Power Amplifier | -0.5 | 3.63 | V |
| RF_AVDD_BTTX | Power supply for Bluetooth Transmit circuit. | -0.5 | 1.22 | V |
| RF_AVDD | Power supply for the 2.4 GHz RF and AFE | -0.5 | 1.98 | V |
| AVDD_1P3 | Power supply for the 2.4 GHz RF | -0.5 | 1.98 | V |
| UULP_AVDD | Power supply for the always-on digital and ULP peripherals | -0.5 | 1.21 | V |
| EFUSE_AVDD | Power supply for the on-chip eFuse | -0.5 | 2.3 | V |
| C_VDD | Power supply for the digital core | -0.5 | 1.26 | V |
| DDR_IO_VDD | I/O supply for the DDR interface pins | -0.5 | 1.98 | V |
| USB_AVDD_3P3 | Power supply for the USB interface | -0.5 | 3.63 | V |
| USB_AVDD_1P1 | Power supply for the USB core | -0.5 | 1.26 | V |
| USB_VBUS | USB VBUS signal from the USB connector | -0.5 | 5.25 | V |
| $I_{max}$ | Maximum Current consumption in TX mode | - | 400 | mA |
| $P_{max}$ | RF Power Level Input to the chip | - | 10 | dBm |
| $I_{Pmax}$ | Peak current rating for power supply | - | 500 | mA |

**Table 5. Absolute Maximum Ratings**

## 3.2 Recommended Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $T_{ambient}$ | Ambient temperature | -40 | 25 | 85 | °C |
| UULP_VBATT_1 | Always-on VBATT supply to the UULP Domains | 1.75/3.0 | 1.85/3.3 | 1.98/3.63 | V |
| UULP_VBATT_2 | Always-on VBATT supply to the UULP Domains | 1.75/3.0 | 1.85/3.3 | 1.98/3.63 | V |
| RF_VBATT | Always-on VBATT Power supply to the RF | 1.75/3.0 | 1.85/3.3 | 1.98/3.63 | V |
| VINBCKDC | Power supply for the on-chip Buck | 1.75/3.0 | 1.85/3.3 | 1.98/3.63 | V |
| VINLDOSOC | Power supply for SoC LDO | 1.1 | 1.35 | 1.55 | V |
| VINLDO1P8 | Power supply for 1.8V LDO | 1.75/3.0 | 1.85/3.3 | 1.98/3.63 | V |
| IO_VDD_1 | I/O supply for GPIOs | 1.75/3.0 | 1.85/3.3 | 1.98/3.63 | V |
| IO_VDD_2 | I/O supply for GPIOs | 1.75/3.0 | 1.85/3.3 | 1.98/3.63 | V |
| IO_VDD_3 | I/O supply for GPIOs | 1.75/3.0 | 1.85/3.3 | 1.98/3.63 | V |
| ULP_IO_VDD | I/O supply for ULP GPIOs | 1.75/3.0 | 1.85/3.3 | 1.98/3.63 | V |
| SDIO_IO_VDD | I/O supply for SDIO I/Os | 1.75/3.0 | 1.85/3.3 | 1.98/3.63 | V |
| PA2G_AVDD | Power supply for the 2.4 GHz RF Power Amplifier | 3.0 | 3.3 | 3.63 | V |
| RF_AVDD_BTTX | Power supply for Bluetooth Transmit circuit. | 1.0 | 1.1 | 1.22 | V |
| RF_AVDD | Power supply for the 2.4 GHz RF and AFE | 1.3 | 1.4 | 1.8 | V |
| AVDD_1P3 | Power supply for the 2.4 GHz RF | 1.3 | 1.4 | 1.8 | V |
| UULP_AVDD | Power supply for the always-on digital and ULP peripherals | 0.95 | 1.0 | 1.21 | V |
| EFUSE_AVDD | Power supply for the on-chip eFuse | 1.75 | 1.85 | 1.98 | V |
| C_VDD | Power supply for the digital core (Low Power Mode)<br>Power supply for the digital core (High Performance Mode) | 0.95<br>0.99 | 1.0<br>1.1 | 1.05<br>1.21 | V<br>V |
| USB_AVDD_3P3 | Power supply for the USB interface | 3.0 | 3.3 | 3.63 | V |
| USB_AVDD_1P1 | Power supply for the USB core | 0.99 | 1.1 | 1.21 | V |
| USB_VBUS | USB VBUS signal from the USB connector | 4.75 | 5 | 5.25 | V |

**Table 6. Recommended Operating Conditions**

## 3.3 DC Characteristics

### 3.3.1 Reset Pin

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | High level input voltage @ 3.3 V | 0.8 * VDD | - | - | V |
| | High level input voltage @ 1.8 V | 1.17 | - | - | V |
| $V_{IL}$ | Low level input voltage @ 3.3 V | - | - | 0.3 * VDD | V |
| | Low level input voltage @ 1.8 V | - | - | 0.63 | V |
| $V_{hys}$ | Hysteresis voltage | 0.05 * VDD | - | - | V |

**Table 7. Reset Pin**

All numbers are at typical operating conditions unless otherwise stated.

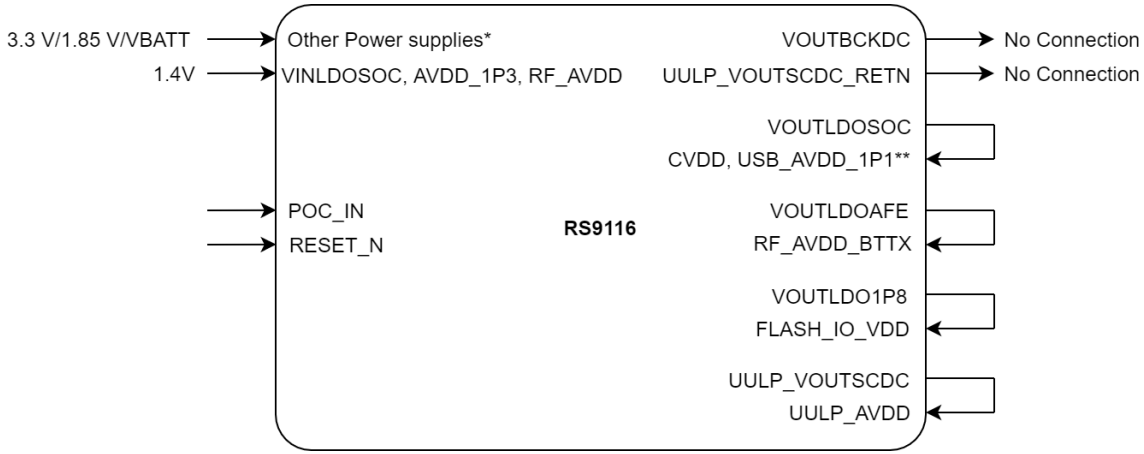
### 3.3.2 Power Sequence

The POC_IN and RESET_N signals should be controlled from external sources such as R/C circuits, and/or other MCU's GPIOs. Below waveforms show power sequence (Up & Down) requirements under various application needs. Note that below waveforms are not to scale.

#### 3.3.2.1 Power-Up and Down Sequence with External 1.4V supply and POC_IN

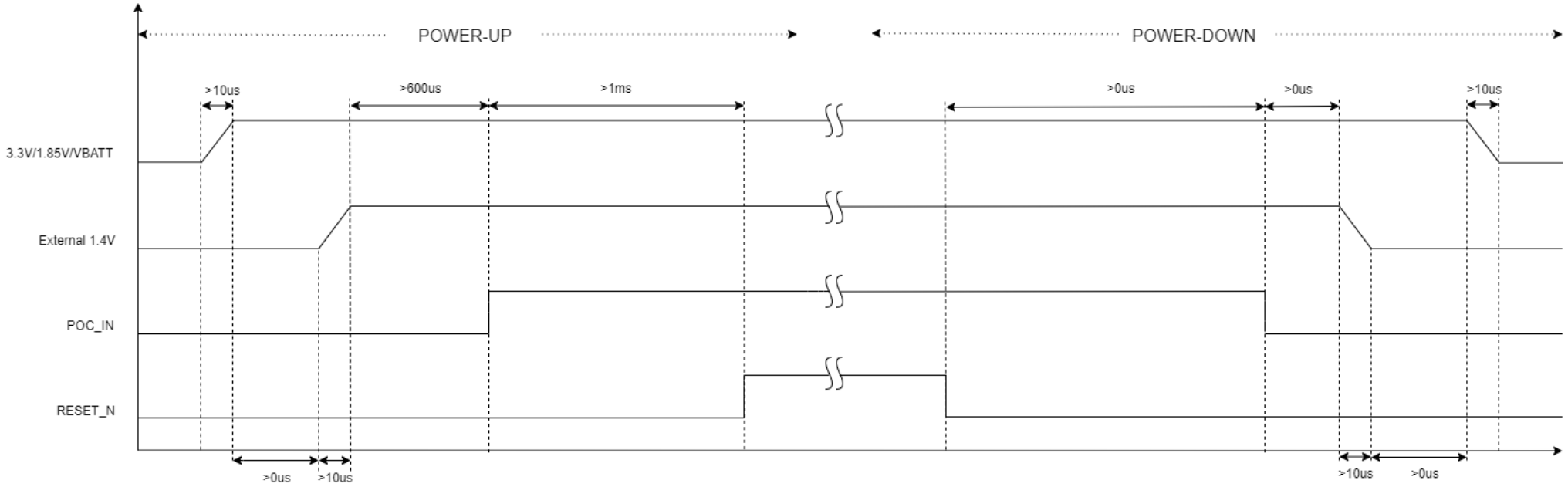
The diagram below shows connections of various power supply voltages, POC_IN and RESET_N. These connections can be used when:

- System PMU (outside RS9116) can provide 1.4V supply, and hence the internal Buck regulator in RS9116 can be disabled.
- The 1.1V supply is still derived from LDO SoC (internal to RS9116).
- POC_IN is controlled externally.




NOTE:

1. A typical connection diagram is shown above. Some of the supply pins shown above may or may not be present in the IC/Module. Check the Pinout table in this datasheet and connect accordingly.
2. * = Provide the supply voltages as per the specifications mentioned in this datasheet.
3. ** = USB power supply input connection is required if USB interface is present and used. Otherwise, follow the connection as shown in Reference Schematics.



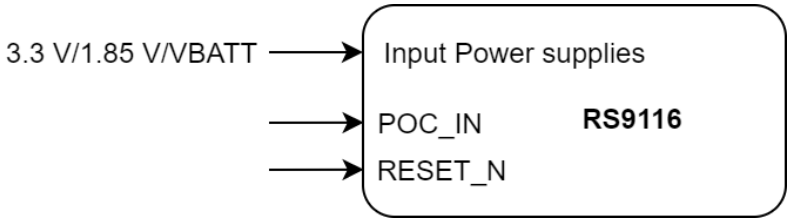

NOTE:

1. 3.3 V/1.85 V/VBATT supply shown above must be connected to the power supply pins of IC/Module. For example, SDIO_IO_VDD, ULP_IO_VDD, UULP_VBATT_1, etc.
2. Above POC_IN waveform is applicable if it is externally driven. Otherwise, that particular waveform can be ignored, and the RESET_N timing can be considered after/before external power supplies ramp-up/down.

### 3.3.2.2 Power-Up and Down Sequence with External POC_IN

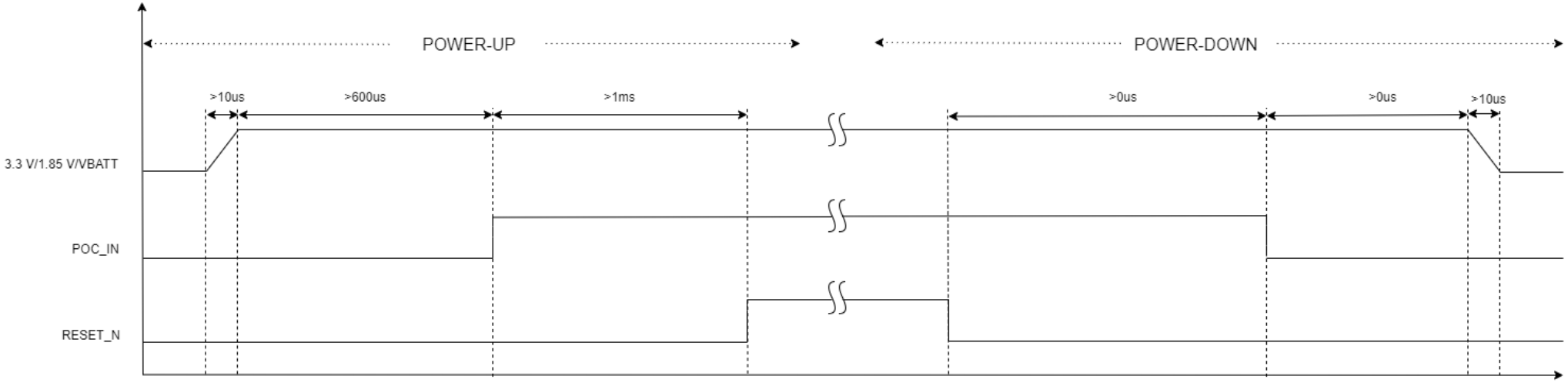
The diagram below shows connections of various power supply voltages, POC_IN and RESET_N. These connections can be used when:

- System PMU cannot provide 1.4 V or 1.1 V supplies and the internal buck and LDO of RS9116 are used.
- POC_IN is controlled externally.



NOTE:

1. A typical connection diagram is shown above. Check the Reference Schematics for connections of other power supplies.



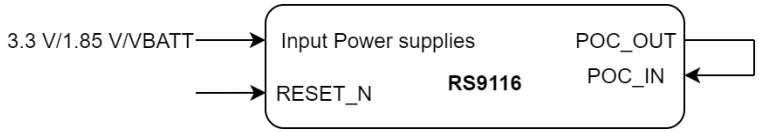

NOTE:

1. 3.3 V/1.85 V/VBATT supply shown above must be connected to the power supply pins of IC/Module. For example, SDIO_IO_VDD, ULP_IO_VDD, UULP_VBATT_1, etc.

### 3.3.2.3 Power-Up and Down Sequence with POC_IN connected internally

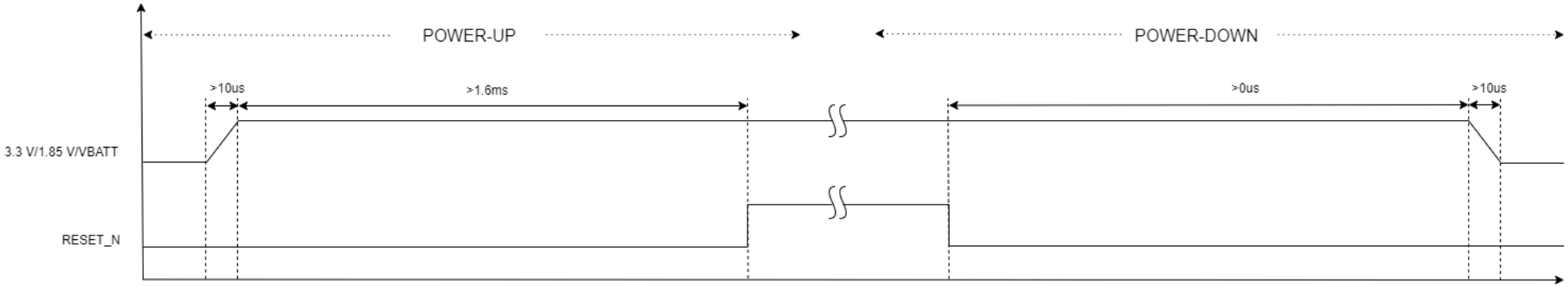
The diagram below shows connections of various power supply voltages, POC_IN and RESET_N. The typical applications of this connection can be as follows. This connection is **Not Recommended for New Design**.

- System cannot provide external 1.4 V & 1.1 V supplies and the internal buck and LDO of RS9116 are used.
- POC_IN is looped back from POC_OUT.




NOTE:

1. 1. A typical connection diagram is shown above. Check the Reference Schematics for connections of other power supplies.
2. POC_OUT can be connected to POC_IN if the supply voltage is 3.3 V only. Else, POC_IN must be driven externally.
3. This connection is **Not Recommended for New Design**, and it is recommended to drive POC_IN externally as shown in the above section. If POC_IN cannot be driven externally, then an RC circuit delay can be provided in between POC_IN and POC_OUT, for delaying the POC_OUT signal reaching POC_IN.

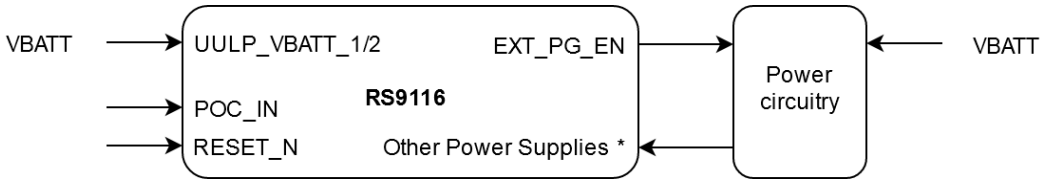



NOTE:

1. 3.3 V/1.85 V/VBATT supply shown above must be connected to the power supply pins of IC/Module. For example, SDIO_IO_VDD, ULP_IO_VDD, UULP_VBATT_1, etc.

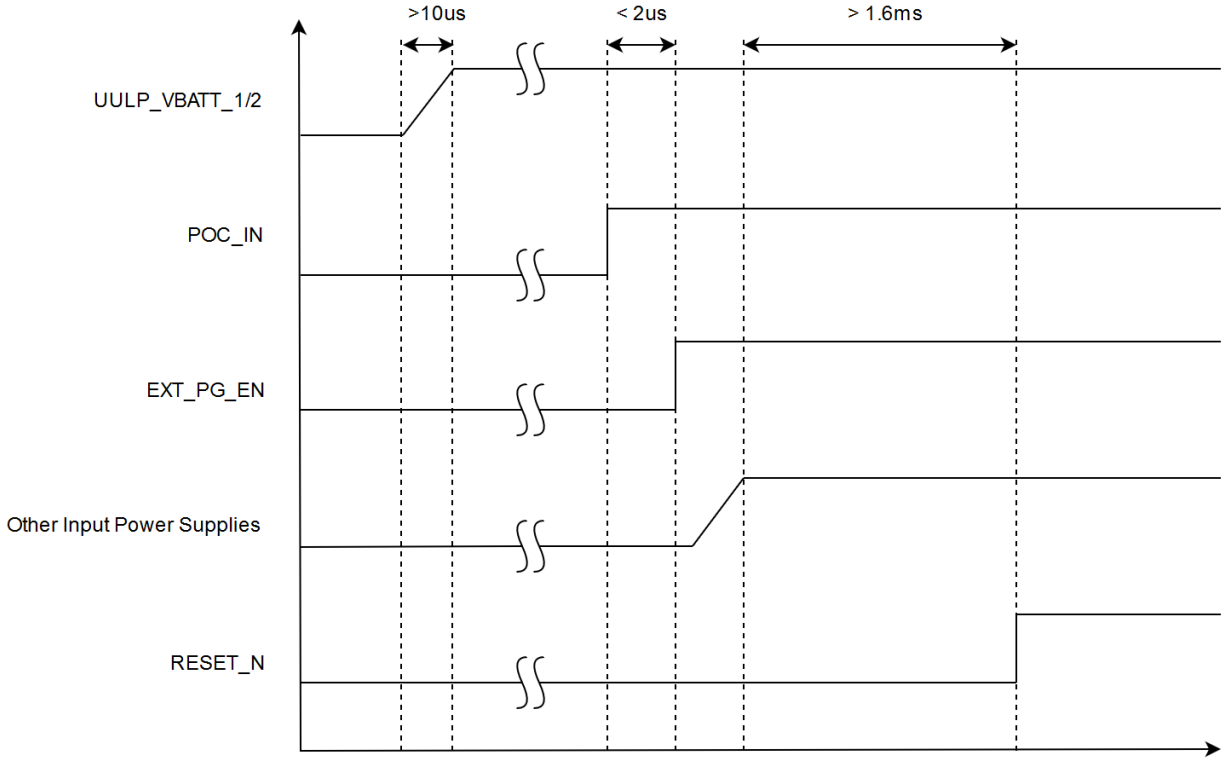
### 3.3.2.4 Power-Up Sequence with EXT_PG_EN used to Control Supply Voltages

The EXT_PG_EN functionality (available on one of the pins) can be used to control supply voltages other than UULP_VBATT supplies (Always-ON VBATT Power supplies). If EXT_PG_EN functionality is enabled, it will be '1' by default immediately after power-on. The diagram below shows typical connections of EXT_PG_EN and UULP_VBATT pins. Use one of the application connections shown above in conjunction to the below. The main purpose of this connection diagram and waveform is to show the EXT_PG_EN connection and its waveform in relation to the others.




NOTE:

1. 1. A typical connection diagram is shown above. Some of the supply pins shown above may not be present in the SoC/module. Check the Pin Out table in this datasheet and connect accordingly.
2. * = Provide the supply voltages as per the specifications mentioned in the datasheet.
3. Typical Power circuitry can be a Power Gate (Transistor or IC based), or a Voltage Regulator.

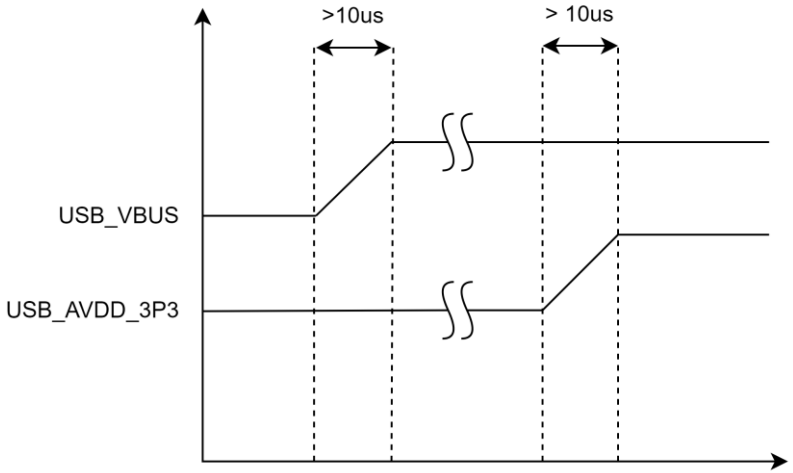



NOTE:

1. The waveform shown above is for a typical connection. POC_IN can be connected based on one of the above application diagrams, and its waveform/timing depends on the connection.
2. As per the EXT_PG_EN signaling, other power supplies ramp-up as per the power circuitry implementation. Hence, the start and ramp-up timing of other power supplies does not have any timing requirement.

#### 3.3.2.5 Power-Up Sequence with USB as Host Interface

The timing waveform below is for the case when USB is used as the host interface. USB_VBUS should be supplied at 5 V, and it should follow this timing waveform with respect to USB_AVDD_3P3.




NOTE:

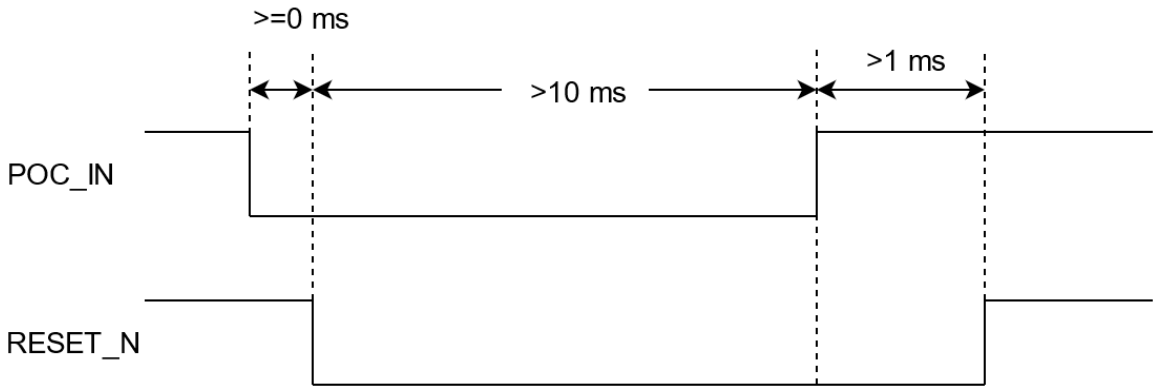
USB_AVDD_3P3 is part of the input power supply to RS9116.

This waveform should be followed in conjunction with the applicable waveform given in the above sections.

### 3.3.3 Hardware Resetting Sequence after Power On

During power-up of the RS9116, a power-up sequence must be followed as per the requirements mentioned in the above section. In some applications, there is a need to reset the RS9116 for a second time or beyond after power-up. Follow the below timing diagram in such cases. Because the POC_IN and RESET_N are applied externally, the present state of the device will be lost.

If POC_IN cannot be applied externally or POC_OUT is looped back to POC_IN, then a second reset (or beyond) cannot be applied.



### 3.3.4 Digital Input Output Signals

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | High level input voltage @3.3 V | 2.0 | - | - | V |
| | High level input voltage @1.8 V | 1.17 | - | - | V |
| $V_{IL}$ | Low level input voltage @3.3 V | - | - | 0.8 | V |
| | Low level input voltage @1.8 V | - | - | 0.63 | V |
| $V_{hys}$ | Hysteresis voltage | 0.1 VDD | - | - | V |
| $V_{OL}$ | Low level output voltage | - | - | 0.4 | V |
| $V_{OH}$ | High level output voltage | VDD-0.4 | - | - | V |
| $I_{OL}$ | Low level output current | - | 4.0 | - | mA |
| $I_{OH}$ | High level output current | - | 4.0 | - | mA |

**Table 8. Digital I/O Signals**

- All numbers are at typical operating conditions unless otherwise stated.
- SDIO signals will be at 8 mA drive strength.

### 3.3.5 USB

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Vcm DC (DC level measured at receiver connector) | HS Mode<br>LS/FS Mode | -0.05<br>0.8 | - | 0.5<br>2.5 | V |
| Crossover Voltages | LS Mode<br>FS Mode | 1.3<br>1.3 | - | 2<br>2 | V |
| Power supply ripple noise (Analog 3.3V) | < 160 MHz | -50 | - | 50 | mV |

**Table 9. USB**

### 3.3.6 Pin Capacitances

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{io}$ | Input/output capacitance, digital pins only | - | - | 2.0 | pF |

**Table 10. Pin Capacitances**

## 3.4 AC Characteristics

### 3.4.1 Clock Specifications

RS9116 chipsets require two primary clocks:

- Low frequency 32 kHz clock for sleep manager and RTC
  - Internal 32 kHz RC clock is used for applications with low timing accuracy requirements
  - 32 kHz crystal clock is used for applications with high timing accuracy requirements
- High frequency 40 MHz clock for the ThreadArch® processor, baseband subsystem and the radio
  - 40 MHz clock is integrated inside the module, and no external clock needs to be provided

The chipsets have integrated internal oscillators including crystal oscillators to generate the required clocks. Integrated crystal oscillators enable the use of low-cost passive crystal components. Additionally, in a system where

an external clock source is already present, the clock can be reused. The following are the recommended options for the clocks for different functionalities:

| Functionality | Default Clock option | Other Clock option | Comments |
|---|---|---|---|
| Wi-Fi or Wi-Fi + BLE Connectivity | Internal 32 kHz RC oscillator calibrated to <200ppm | 32 kHz XTAL oscillator input on UULPGPIO. | 32 kHz XTAL Oscillator clock is optional. No significant power consumption impact on connected power numbers (<10uA). |
| Wi-Fi + BT or Wi-Fi + BT + BLE Connectivity with low power Audio Streaming operation (A2DP Source) | 32 kHz XTAL oscillator input on UULPGPIO | Internal 32 kHz RC oscillator calibrated to <200ppm | 32 kHz XTAL Oscillator clock is important for Low-power Audio Streaming operation (A2DP Source). |

There is no impact on sleep/deep-sleep power consumption with/without 32 kHz XTAL oscillator clock

**32 kHz XTAL sources:**

**Option 1:** From Host MCU/MPU LVCMOS rail to rail clock input on UULPGPIO

**Option 2:** External Xtal oscillator providing LVCMOS rail to rail clock input on UULPGPIO (Nano-drive clock should not be supplied).

#### 3.4.1.1 32 kHz Clock

The 32 kHz clock selection can be done through software. RC oscillator clock is not suited for high timing accuracy applications and can increase system current consumption in duty-cycled power modes.

##### 3.4.1.1.1 RC Oscillator

| Parameter | Parameter Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $F_{osc}$ | Oscillator Frequency | | 32.0 | | kHz |
| $F_{osc\_Acc}$ | Frequency Variation with Temp and Voltage | | 1.2 | | % |
| Jitter | RMS value of Edge jitter (TIE) | | 91 | | ns |
| Peak Period Jitter | Peak value of Cycle Jitter with 6σ variation | | 789 | | ns |

**Table 11. 32 kHz RC Oscillator**

##### 3.4.1.1.2 32 kHz External Oscillator

An external 32 kHz low-frequency clock can be fed through the XTAL_32KHZ_IN functionality.

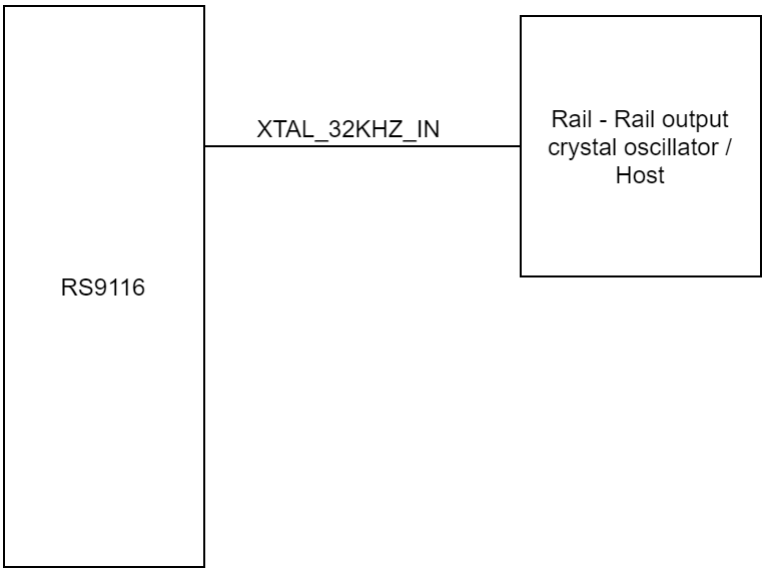



**Figure 6. External 32 kHz Oscillator - Rail to Rail**

| Parameter | Parameter Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $F_{osc}$ | Oscillator Frequency | | 32.768 | | kHz |
| $F_{osc\_Acc}$ | Frequency Variation with Temp and Voltage | -100 | | 100 | ppm |
| Duty cycle | Input duty cycle | 30 | 50 | 70 | % |
| $V_{AC}$ | Input AC peak-peak voltage swing at input pin. | -0.3 | - | VBATT +/- 10% | Vpp |

**Table 12. 32 kHz External Oscillator Specifications**

### 3.4.2 SDIO 2.0 Secondary

#### 3.4.2.1 Full Speed Mode

| Parameter | Parameter Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{sdio}$ | SDIO_CLK | - | - | 25 | MHz |
| $T_s$ | SDIO_DATA/SDIO_CMD, input setup time | 4 | - | - | ns |
| $T_h$ | SDIO_DATA/SDIO_CMD, input hold time | 1 | - | - | ns |
| $T_{od}$ | SDIO_DATA/SDIO_CMD, clock to output delay | - | - | 13 | ns |
| $C_L$ | Output Load | 5 | - | 10 | pF |

**Table 13. AC Characteristics - SDIO 2.0 Secondary Full Speed Mode**

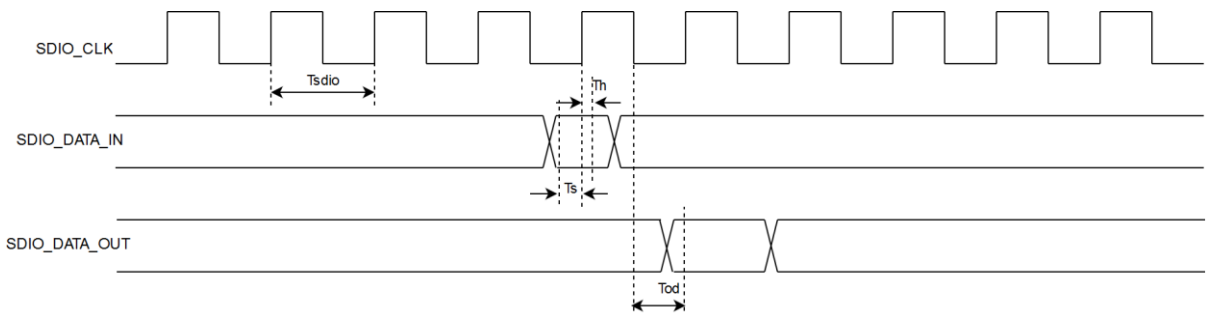



**Figure 7. Interface Timing Diagram for SDIO 2.0 Secondary Full Speed Mode**

#### 3.4.2.2 High Speed Mode

| Parameter | Parameter Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{sdio}$ | SDIO_CLK | 25 | - | 50 | MHz |
| $T_s$ | SDIO_DATA/SDIO_CMD, input setup time | 4 | - | - | ns |
| $T_h$ | SDIO_DATA/SDIO_CMD, input hold time | 1 | - | - | ns |
| $T_{od}$ | SDIO_DATA/SDIO_CMD, clock to output delay | 2.5 | - | 13 | ns |
| $C_L$ | Output Load | 5 | - | 10 | pF |

**Table 14. AC Characteristics - SDIO 2.0 Secondary High-Speed Mode**

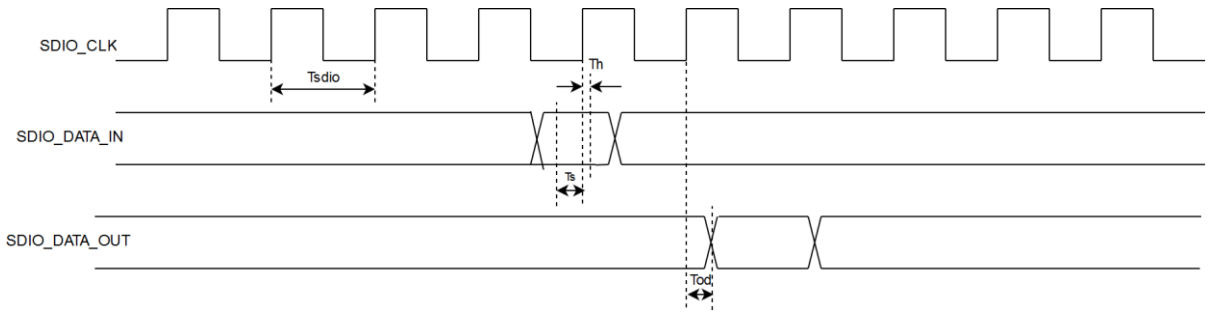



**Figure 8. Interface Timing Diagram for SDIO 2.0 Secondary High Speed Mode**

### 3.4.3 SPI Secondary

#### 3.4.3.1 Low Speed Mode

| Parameter | Parameter Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{spi}$ | SPI_CLK | 0 | - | 25 | MHz |
| $T_{cs}$ | SPI_CSN to output delay | - | - | 7.5 | ns |
| $T_{cst}$ | SPI CSN to input setup time | 4.5 | - | - | - |
| $T_s$ | SPI_MOSI, input setup time | 1.33 | - | - | ns |
| $T_h$ | SPI_MOSI, input hold time | 1.2 | - | - | ns |
| $T_{od}$ | SPI_MISO, clock to output delay | - | - | 8.75 | ns |
| $C_L$ | Output Load | 5 | - | 10 | pF |

**Table 15. AC Characteristics - SPI Secondary Low Speed Mode**

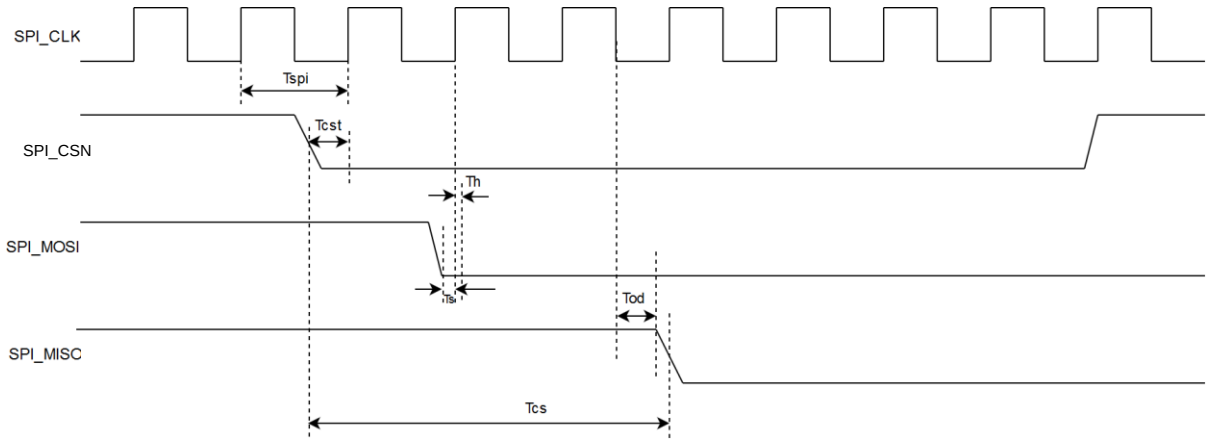



**Figure 9. Interface Timing Diagram for SPI Secondary Low Speed Mode**

### 3.4.3.2 High Speed Mode

| Parameter | Parameter Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{spi}$ | SPI_CLK | 25 | - | 80 | MHz |
| $T_{cs}$ | SPI_CSN to output delay | - | - | 7.5 | ns |
| $T_{cst}$ | SPI CSN to input setup time | 4.5 | - | - | - |
| $T_s$ | SPI_MOSI, input setup time | 1.33 | - | - | ns |
| $T_h$ | SPI_MOSI, input hold time | 1.2 | - | - | ns |
| $T_{od}$ | SPI_MISO, clock to output delay | 2.5 | - | 8.75 | ns |
| $C_L$ | Output Load | 5 | - | 10 | pF |

**Table 16. AC Characteristics - SPI Secondary High Speed Mode**

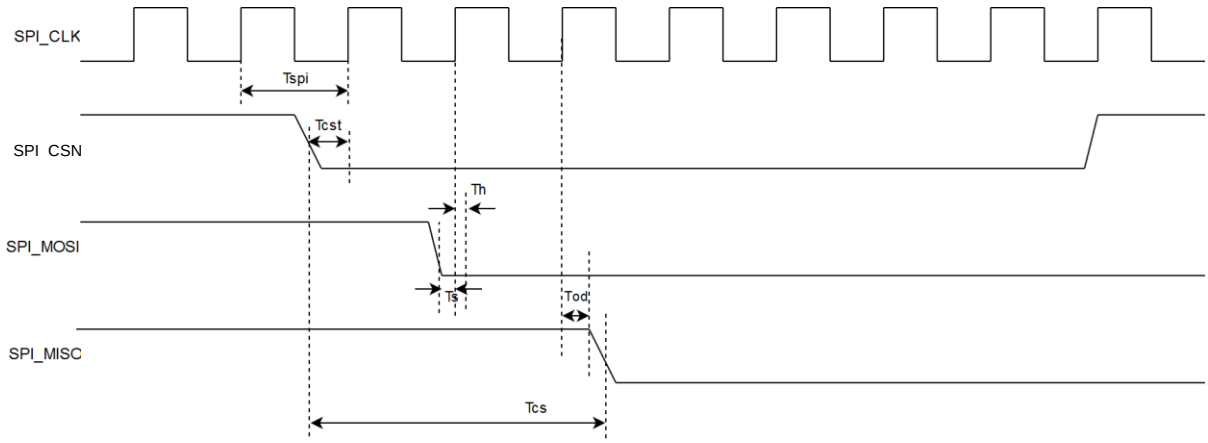



**Figure 10. Interface Timing Diagram for SPI Secondary High Speed Mode**

### 3.4.3.3 Ultra-High-Speed Mode

| Parameter | Parameter Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{spi}$ | SPI_CLK | - | - | 100 | MHz |
| $T_s$ | SPI_MOSI, input setup time | 1.33 | - | - | ns |
| $T_h$ | SPI_MOSI, input hold time | 1.2 | - | - | ns |
| $T_{od}$ | SPI_MISO, clock to output delay | 1.5 | - | 8.75 | ns |

| Parameter | Parameter Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_L$ | Output Load | 5 | - | 10 | pF |

**Table 17. AC Characteristics - SPI Secondary Ultra-High-Speed Mode**

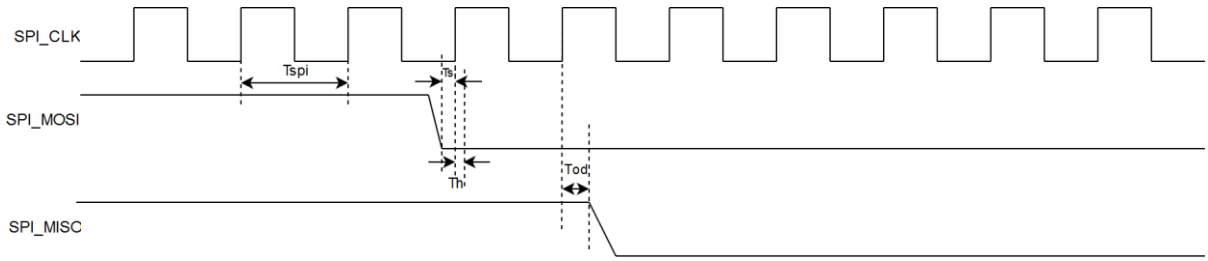



**Figure 11. Interface Timing Diagram for SPI Secondary Ultra-High-Speed Mode**

## 3.4.4 USB

### 3.4.4.1 Low Speed Mode

| Parameter | Parameter Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_r$ | Rise Time | 75 | - | 300 | ns |
| $T_f$ | Fall Time | 75 | - | 300 | ns |
| Jitter | Jitter | - | - | 10 | ns |

**Table 18. AC Characteristics - USB Low Speed Mode**

### 3.4.4.2 Full Speed Mode

| Parameter | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_r$ | Rise Time | 4 | - | 20 | ns |
| $T_f$ | Fall Time | 4 | - | 20 | ns |
| Jitter | Jitter | - | - | 1 | ns |

**Table 19. AC Characteristics - USB Full Speed Mode**

### 3.4.4.3 High Speed Mode

| Parameter | Parameter Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_r$ | Rise Time | 0.5 | - | - | ns |
| $T_f$ | Fall Time | 0.5 | - | - | ns |
| Jitter | Jitter | - | - | 0.1 | ns |

**Table 20. AC Characteristics - USB High Speed Mode**

## 3.4.5 UART

| Parameter | Parameter Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{uart}$ | CLK | 0 | - | 20 | MHz |
| $T_{od}$ | Output delay | 0 | - | 10 | ns |
| $T_s$ | Input setup time | 0 | - | 5 | ns |

| Parameter | Parameter Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_L$ | Output load | 5 | - | 25 | pF |

**Table 21. AC Characteristics - UART**

## 3.4.6 I2C Main and Secondary

### 3.4.6.1 Fast Speed Mode

| Parameter | Parameter Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{i2c}$ | SCL | 100 | - | 400 | KHz |
| $T_{low}$ | clock low period | 1.3 | - | - | us |
| $T_{high}$ | clock high period | 0.6 | - | - | us |
| $T_{sstart}$ | start condition, setup time | 0.6 | - | - | us |
| $T_{hstart}$ | start condition, hold time | 0.6 | - | - | us |
| $T_s$ | data, setup time | 100 | - | - | ns |
| $T_{sstop}$ | stop condition, setup time | 0.6 | - | - | us |
| $C_L$ | Output Load | 5 | - | 10 | pF |

**Table 22. AC Characteristics - I2C Fast Speed Mode**

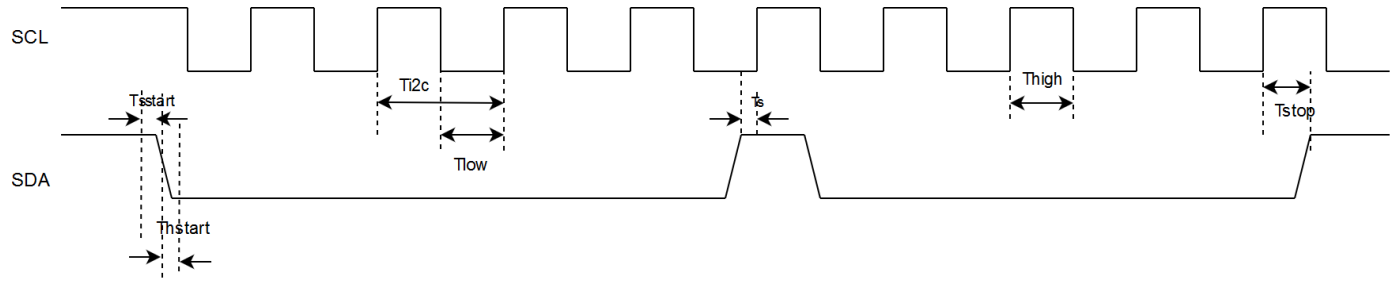



**Figure 12. Interface Timing Diagram for I2C Fast Speed Mode**

### 3.4.6.2 High Speed Mode

| Parameter | Parameter Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{i2c}$ | SCL | 0.4 | - | 3.4 | MHz |
| $T_{low}$ | clock low period | 160 | - | - | ns |
| $T_{high}$ | clock high period | 60 | - | - | ns |
| $T_{sstart}$ | start condition, setup time | 160 | - | - | ns |
| $T_{hstart}$ | start condition, hold time | 160 | - | - | ns |
| $T_s$ | data, setup time | 10 | - | - | ns |
| $T_h$ | data, hold time | 0 | - | 70 | ns |
| $T_{sstop}$ | stop condition, setup time | 160 | - | - | ns |
| $C_L$ | Output Load | 5 | - | 10 | pF |

**Table 23. AC Characteristics - I2C High Speed Mode**

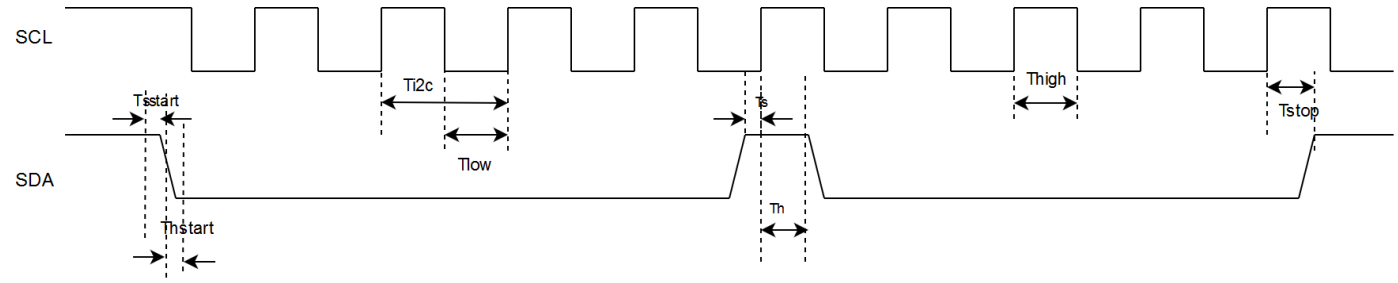



**Figure 13. Interface Timing Diagram for I2C High Speed Mode**

### 3.4.7 I2S/PCM Main and Secondary

#### 3.4.7.1 Main Mode

Negedge driving and posedge sampling for I2S
Posedge driving and negedge sampling for PCM

| Parameter | Parameter Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{i2s}$ | i2s_clk | 0 | - | 25 | MHz |
| $T_s$ | i2s_din, i2s_ws setup time | 10 | - | - | ns |
| $T_h$ | i2s_din, i2s_ws hold time | 0 | - | - | ns |
| $T_{od}$ | i2s_dout output delay | 0 | - | 12 | ns |
| $C_L$ | i2s_dout output load | 5 | - | 10 | pF |

**Table 24. AC Characteristics – I2S/PCM Main Mode**

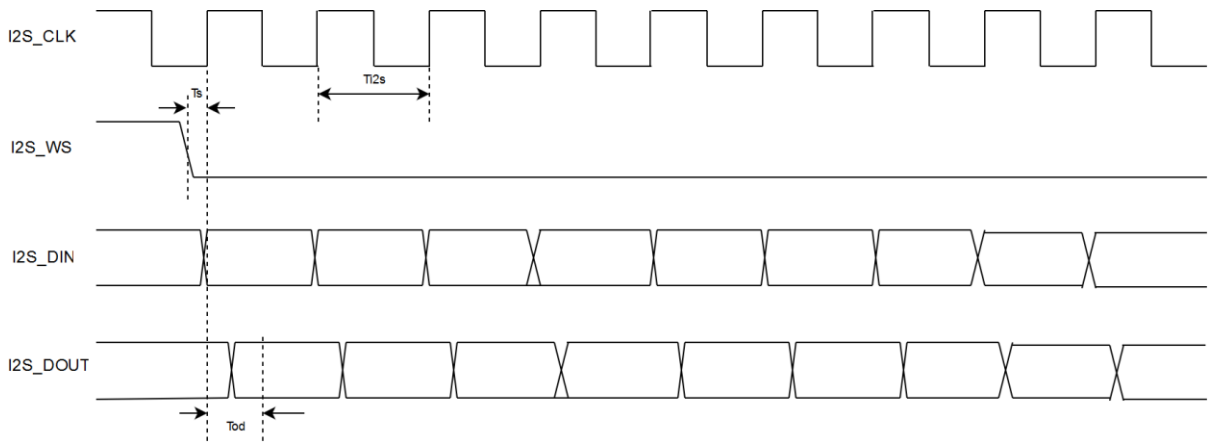



**Figure 14. Interface Timing Diagram for I2S Main Mode**

#### 3.4.7.2 Secondary Mode

Negedge driving and posedge sampling for I2S
Posedge driving and negedge sampling for PCM

| Parameter | Parameter Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{i2s}$ | i2s_clk | 0 | - | 25 | MHz |
| $T_s$ | i2s_din, i2s_ws setup time | 8 | - | - | ns |
| $T_h$ | i2s_din, i2s_ws hold time | 0 | - | - | ns |
| $T_{od}$ | i2s_dout output delay | 0 | - | 17 | ns |

| Parameter | Parameter Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_L$ | i2s_dout output load | 5 | - | 10 | pF |

**Table 25. AC Characteristics - I2S/PCM Secondary Mode**

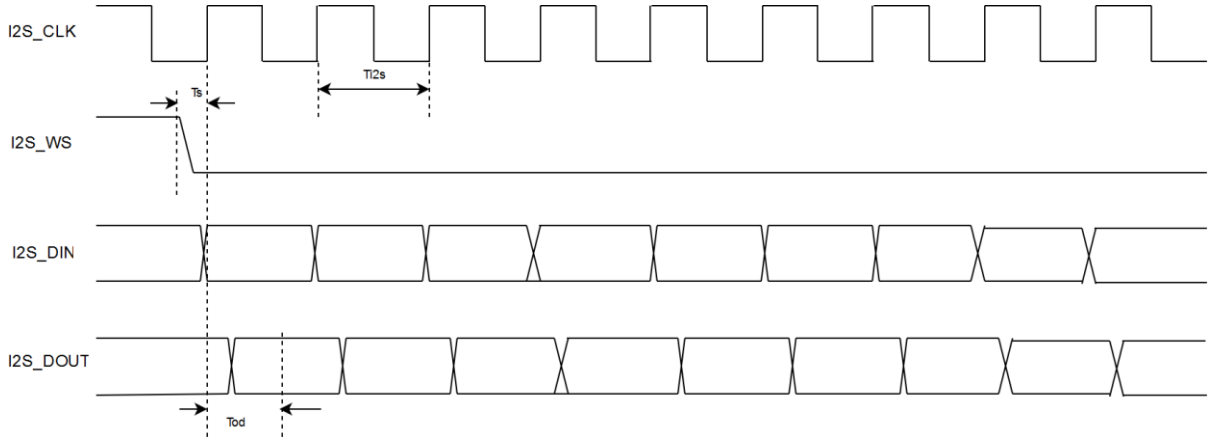



**Figure 15. Interface Timing Diagram for I2S Secondary Mode**

### 3.4.8 GPIO Pins

| Parameter | Parameter Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_{rf}$ | Rise time | Pin configured as output; SLEW = 1(fast mode) | 1.0 | - | 2.5 | ns |
| $T_{ff}$ | Fall time | Pin configured as output; SLEW = 1(fast mode) | 0.9 | - | 2.5 | ns |
| $T_{rs}$ | Rise time | Pin configured as output; SLEW = 0(standard mode) | 1.9 | - | 4.3 | ns |
| $T_{fs}$ | Fall time | Pin configured as output; SLEW = 0(standard mode) | 1.9 | - | 4.0 | ns |
| $T_r$ | Rise time | Pin configured as input | 0.3 | - | 1.3 | ns |
| $T_f$ | Fall time | Pin configured as input | 0.2 | - | 1.2 | ns |

**Table 26. AC Characteristics - GPIO Pins**

## 3.5 RF Characteristics

All specifications are subject to change. Contact Silicon Labs for final numbers.

In the sub-sections below, all numbers are measured at typical operating conditions unless otherwise stated.

### 3.5.1 WLAN 2.4 GHz Transmitter Characteristics

#### 3.5.1.1 Transmitter Characteristics with 3.3 V Supply

- TA = 25 °C, PA2G_AVDD/VINBCKDC = 3.3V. Remaining supplies are at typical operating conditions.
- The transmit power numbers are based on average performance across all channels.

| Parameter | Condition | Notes | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Transmit Power for 20 MHz Bandwidth, compliant with IEEE mask and EVM | DSSS - 1 Mbps | EVM< -9 dB | - | 17 | - | dBm |
| | DSSS - 2 Mbps | EVM< -9 dB | - | 16.5 | - | dBm |
| | CCK- 5.5 Mbps | EVM< -9 dB | - | 16.5 | - | dBm |
| | CCK - 11 Mbps | EVM< -9 dB | - | 16.5 | - | dBm |
| | OFDM - 6 Mbps | EVM< -5 dB | - | 17.5 | - | dBm |
| | OFDM - 9 Mbps | EVM< -8 dB | - | 17.5 | - | dBm |
| | OFDM - 12 Mbps | EVM< -10 dB | - | 17.5 | - | dBm |
| | OFDM - 18 Mbps | EVM< -13 dB | - | 16.5 | - | dBm |
| | OFDM - 24 Mbps | EVM< -16 dB | - | 15.5 | - | dBm |
| | OFDM - 36 Mbps | EVM< -19 dB | - | 13.5 | - | dBm |
| | OFDM - 48 Mbps | EVM< -22 dB | - | 13.5 | - | dBm |
| | OFDM - 54 Mbps | EVM< -25 dB (See note section) | - | 13.5 | - | dBm |
| | MCS0 Mixed Mode | EVM< -5 dB | - | 16.5 | - | dBm |
| | MCS1 Mixed Mode | EVM< -10 dB | - | 16.5 | - | dBm |
| | MCS2 Mixed Mode | EVM< -13 dB | - | 16.5 | - | dBm |
| | MCS3 Mixed Mode | EVM< -16 dB | - | 15.5 | - | dBm |
| | MCS4 Mixed Mode | EVM< -19 dB | - | 14 | - | dBm |
| | MCS5 Mixed Mode | EVM< -22 dB | - | 13 | - | dBm |
| | MCS6 Mixed Mode | EVM< -25 dB (See note section) | - | 13 | - | dBm |
| | MCS7 Mixed Mode | (See note section) | - | 10.5 | - | dBm |
| Transmitter Emissions (6 Mbps @ Maximum Power) | 776-794 MHz | CDMA2000 | - | -158 | - | dBm/Hz |
| | 869–960 MHz | CDMAOne, GSM850 | - | -158 | - | dBm/Hz |
| | 1450–1495 MHz | DAB | - | -158 | - | dBm/Hz |
| | 1570–1580 MHz | GPS | - | -145 | - | dBm/Hz |
| | 1592–1610 MHz | GLONASS | - | -120 | - | dBm/Hz |

| Parameter | Condition | Notes | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | 1710–1800 MHz | DSC-1800-Uplink | - | -128 | - | dBm/Hz |
| | 1805–1880 MHz | GSM 1800 | - | -111 | - | dBm/Hz |
| | 1850–1910 MHz | GSM 1900 | - | -125 | - | dBm/Hz |
| | 1910–1930 MHz | TDSCDMA, LTE | - | -134 | - | dBm/Hz |
| | 1930–1990 MHz | GSM1900, CDMAOne, WCDMA | - | -132 | - | dBm/Hz |
| | 2010–2075 MHz | TDSCDMA | - | -134 | - | dBm/Hz |
| | 2110–2170 MHz | WCDMA | - | -130 | - | dBm/Hz |
| | 2305–2370 MHz | LTE Band 40 | - | -110 | - | dBm/Hz |
| | 2370–2400 MHz | LTE Band 40 | - | -95 | - | dBm/Hz |
| | 2496–2530 MHz | LTE Band 41 | - | -115 | - | dBm/Hz |
| | 2530–2560 MHz | LTE Band 41 | - | -121 | - | dBm/Hz |
| | 2570–2690 MHz | LTE Band 41 | - | -127 | - | dBm/Hz |
| | 5000–5900 MHz | WLAN 5G | - | -148 | - | dBm/Hz |
| Harmonic Emissions (1 Mbps @ Maximum Power) | 4.8-5.0 GHz | 2nd Harmonic | - | -48 | - | dBm/MHz |
| | 7.2-7.5 GHz | 3rd Harmonic | - | -43 | - | dBm/MHz |

**Table 27. WLAN 2.4 GHz Transmitter Characteristics (3.3V)**

1. There is a variation of up to +/-1dB in power across channels.
2. To meet FCC emission limits, band edge channels (1 and 11) TX power has to be reduced up to 6 dB in lower data rates and up to 3 dB in higher data rates. The radiated power in band edge is a strong function of the antenna properties. Refer to the AN1337 application note for more details on the certifications.
3. Across the temperature range of -40 °C to +85 °C, the output power may degrade by up to 2 dB at -40 °C and by up to 5 dB at +85 °C.
4. There may be a reduction in EVM of up to 1 dB in 54 Mbps data rate, and 2 dB in MCS6 data rate.
5. EVM for MCS7 data rate may not meet IEEE spec of -27dB.
6. IEEE spectral mask limits may be crossed in lower data rates in some channels, and if required power may be backed off by 1-2dB.
7. There is a +/-2dB of 3 sigma (99.7%) part-to-part power variation.

### 3.5.2 WLAN 2.4 GHz Receiver Characteristics on High-Performance (HP) RF Chain

TA = 25 °C. Parameters are measured at antenna port on channel 1 (2412 MHz)

- All WLAN receiver sensitivity numbers and adjacent channel numbers are at < 10% PER limit. Packet sizes are 1024 bytes for 802.11 b/g data rates and 4096 bytes for 802.11 n data rates.
- For WLAN ACI cases, the desired signal power is 3 dB above standard defined sensitivity level.

| Parameter | Condition/Notes | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Sensitivity for 20 MHz Bandwidth (1) | 1 Mbps DSSS | - | -95 | - | dBm |
| | 2 Mbps DSSS | - | -89.5 | - | dBm |
| | 5.5 Mbps CCK | - | -87.5 | - | dBm |
| | 11 Mbps CCK | - | -85.5 | - | dBm |
| | 6 Mbps OFDM | - | -89 | - | dBm |
| | 9 Mbps OFDM | - | -88 | - | dBm |
| | 12 Mbps OFDM | - | -88.5 | - | dBm |
| | 18 Mbps OFDM | - | -86.5 | - | dBm |
| | 24 Mbps OFDM | - | -82.5 | - | dBm |
| | 36 Mbps OFDM | - | -78.5 | - | dBm |
| | 48 Mbps OFDM | - | -75 | - | dBm |
| | 54 Mbps OFDM | - | -73 | - | dBm |
| | MCS0 Mixed Mode | - | -88 | - | dBm |
| | MCS1 Mixed Mode | - | -85.5 | - | dBm |
| | MCS2 Mixed Mode | - | -83 | - | dBm |
| | MCS3 Mixed Mode | - | -80.5 | - | dBm |
| | MCS4 Mixed Mode | - | -77 | - | dBm |
| | MCS5 Mixed Mode | - | -72 | - | dBm |
| | MCS6 Mixed Mode | - | -70 | - | dBm |
| | MCS7 Mixed Mode | - | -69.5 | - | dBm |
| Maximum Input Level for PER below 10% | 802.11 b | - | 0 | - | dBm |
| | 802.11g | - | -10 | - | dBm |
| | 802.11n | - | -10 | - | dBm |
| RSSI Accuracy Range | | -3 | - | 3 | dB |
| Blocking level for 3 dB RX Sensitivity Degradation (Data rate 6Mbps OFDM, Desired signal at -79dBm) | 776–794 MHz | - | -4 | - | dBm |
| | 824–849 MHz | - | -4 | - | dBm |
| | 880–915 MHz | - | -4 | - | dBm |
| | 1710–1785 MHz | - | -14 | - | dBm |
| | 1850–1910 MHz | - | -13 | - | dBm |
| | 1920–1980 MHz | - | -15 | - | dBm |
| | 2300–2400 MHz | - | -60 | - | dBm |
| | 2570–2620 MHz | - | -23 | - | dBm |
| | 2545–2575 MHz | - | -22 | - | dBm |
| Return Loss | | -10 | - | - | dB |
| Adjacent Channel Interference | 1 Mbps DSSS | - | 36 | - | dB |

| Parameter | Condition/Notes | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| | 11 Mbps DSSS | - | 37 | - | dB |
| | 6 Mbps OFDM | - | 38 | - | dB |
| | 54 Mbps OFDM | - | 22 | - | dB |
| | MCS0 Mixed Mode | - | 38 | - | dB |
| | MCS7 Mixed Mode | - | 20 | - | dB |
| Alternate Adjacent Channel Interference | 1 Mbps DSSS | - | 44 | - | dB |
| | 11 Mbps DSSS | - | 35 | - | dB |
| | 6 Mbps OFDM | - | 46 | - | dB |
| | 54 Mbps OFDM | - | 30 | - | dB |
| | MCS0 Mixed Mode | - | 46 | - | dB |
| | MCS7 Mixed Mode | - | 28 | - | dB |

**Table 28. WLAN 2.4 GHz Receiver Characteristics on HP RF Chain**

1. Receiver sensitivity may be degraded by up to 6.5 dB for channels 5,6,7,8,13 & 14 due to the desensitization of the receiver by harmonics of the system clock (40 MHz).
2. There may be a degradation of up to 2 dB across the operating temperature range of -40 °C to +85 °C.

### 3.5.3 WLAN 2.4 GHz Receiver Characteristics on Low-Power (LP) RF Chain

TA = 25 °C. Parameters are measured at antenna port on channel 1 (2412 MHz)

| Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Sensitivity for 20 MHz Bandwidth (1) | 1 Mbps DSSS | - | -93 | - | dBm |
| | 2 Mbps DSSS | - | -86.5 | - | dBm |
| | 5.5 Mbps CCK | - | -84.5 | - | dBm |
| | 11 Mbps CCK | - | -81.5 | - | dBm |
| | 6 Mbps OFDM | - | -86.5 | - | dBm |
| | 9 Mbps OFDM | - | -86 | - | dBm |
| | 12 Mbps OFDM | - | -85.5 | - | dBm |
| | 18 Mbps OFDM | - | -83 | - | dBm |
| | 24 Mbps OFDM | - | -80.5 | - | dBm |
| | 36 Mbps OFDM | - | -76.5 | - | dBm |
| | MCS0 Mixed Mode | - | -85.5 | - | dBm |
| | MCS1 Mixed Mode | - | -83.5 | - | dBm |
| | MCS2 Mixed Mode | - | -81 | - | dBm |

| Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| | MCS3 Mixed Mode | - | -78 | - | dBm |
| | MCS4 Mixed Mode | - | -74 | - | dBm |
| Maximum Input Level for PER below 10% | 802.11 b | - | 5 | - | dBm |
| | 802.11g | - | -10 | - | dBm |
| | 802.11n | - | -10 | - | dBm |
| RSSI Accuracy Range | | -3 | - | 3 | dB |
| Blocking level for 3 dB RX Sensitivity Degradation (Data rate 6Mbps OFDM, Desired signal at -79dBm) | 776–794 MHz | - | -4 | - | dBm |
| | 824–849 MHz | - | -4 | - | dBm |
| | 880–915 MHz | - | -4 | - | dBm |
| | 1710–1785 MHz | - | -14 | - | dBm |
| | 1850–1910 MHz | - | -13.5 | - | dBm |
| | 1920–1980 MHz | - | -18 | - | dBm |
| | 2300–2400 MHz | - | -60 | - | dBm |
| | 2570–2620 MHz | - | -25 | - | dBm |
| | 2545–2575 MHz | - | -26 | - | dBm |
| Return Loss | | -10 | - | - | dB |
| Adjacent Channel Interference | 1 Mbps DSSS | - | 40 | - | dB |
| | 11 Mbps DSSS | - | 36 | - | dB |
| | 6 Mbps OFDM | - | 42 | - | dB |
| | 36 Mbps OFDM | - | 30 | - | dB |
| | MCS0 Mixed Mode | - | 40 | - | dB |
| | MCS4 Mixed Mode | - | 30 | - | dB |
| Alternate Adjacent Channel Interference | 1 Mbps DSSS | - | 50 | - | dB |
| | 11 Mbps DSSS | - | 38 | - | dB |
| | 6 Mbps OFDM | - | 48 | - | dB |
| | 36 Mbps OFDM | - | 38 | - | dB |
| | MCS0 Mixed Mode | - | 48 | - | dB |
| | MCS4 Mixed Mode | - | 36 | - | dB |

**Table 29. WLAN 2.4 GHz Receiver Characteristics on LP RF Chain**

1. Receiver sensitivity may be degraded by up to 6.5 dB for channels 5,6,7,8,13 & 14 due to the desensitization of the receiver by harmonics of the system clock (40 MHz).
2. There may be a degradation of up to 2 dB across the operating temperature range of -40 °C to +85 °C.

### 3.5.4 Bluetooth Transmitter Characteristics on High-Performance (HP) RF Chain

#### 3.5.4.1 Transmitter Characteristics with 3.3 V Supply

TA = 25 °C, PA2G_AVDD/VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are measured at antenna port. (1)

- For Bluetooth C/I cases, the desired signal power is 3 dB above standard defined sensitivity level.

| Parameter | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Transmit Power | BR | | - | 12 | - | dBm |
| | EDR 2Mbps | | - | 12 | - | dBm |
| | EDR 3Mbps | | - | 11 | - | dBm |
| | LE 1Mbps | | - | 18 | - | dBm |
| | LE 2Mbps | | - | 18 | - | dBm |
| | LR 500 Kbps | | - | 18 | - | dBm |
| | LR 125 Kbps | | - | 18 | - | dBm |
| Power Control Step | BR, EDR | | - | 3 | - | dB |
| Adjacent Channel Power \|M-N\| = 2 | BR | | - | - | -20 | dBm |
| | EDR | | - | - | -20 | dBm |
| | LE | | - | - | -20 | dBm |
| | LR | | - | - | -20 | dBm |
| Adjacent Channel Power \|M-N\| > 2 | BR | | - | - | -40 | dBm |
| | EDR | | - | - | -40 | dBm |
| | LE | | - | - | -30 | dBm |
| | LR | | - | - | -30 | dBm |
| BR Modulation Characteristics | DH1 | | -25 | - | 25 | kHz |
| | DH3 | | -40 | - | 40 | kHz |
| | DH5 | | -40 | - | 40 | kHz |
| | Drift Rate | | -20 | - | 20 | kHz/50 us |
| | Δf1 Avg | | 140 | - | 175 | kHz |
| | Δf2 Max | | 115 | - | | kHz |
| EDR Modulation Characteristics | RMS DEVM, EDR2 | | - | 10 | - | % |
| | RMS DEVM, EDR3 | | - | 6 | - | % |
| | 99% DEVM, EDR2 | | - | 17 | - | % |
| | 99% DEVM, EDR3 | | - | 12 | - | % |

| Parameter | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | peak DEVM, EDR2 | | - | 22 | - | % |
| | peak DEVM, EDR3 | | - | 16 | - | % |
| BLE Modulation Characteristics | Δf1 Avg | | 225 | - | 275 | kHz |
| | Δf2 Max | | 185 | - | - | kHz |
| | Δf2 Avg/Δf1 Avg | | 0.8 | - | - | - |
| Transmitter Emissions (BR @Maximum output power) | 776-794 MHz | CDMA2000 | - | -160 | - | dBm/Hz |
| | 869–960 MHz | CDMAOne, GSM850 | - | -160 | - | dBm/Hz |
| | 1450–1495 MHz | DAB | - | -160 | - | dBm/Hz |
| | 1570–1580 MHz | GPS | - | -160 | - | dBm/Hz |
| | 1592–1610 MHz | GLONASS | - | -160(2) | - | dBm/Hz |
| | 1710–1800 MHz | DSC-1800-Uplink | - | -115 | - | dBm/Hz |
| | 1805–1880 MHz | GSM 1800 | - | -148 | - | dBm/Hz |
| | 1850–1910 MHz | GSM 1900 | - | -148 | - | dBm/Hz |
| | 1910–1930 MHz | TDSCDMA, LTE | - | -135 | - | dBm/Hz |
| | 1930–1990 MHz | GSM1900, CDMAOne, WCDMA | - | -101 | - | dBm/Hz |
| | 2010–2075 MHz | TDSCDMA | - | -148 | - | dBm/Hz |
| | 2110–2170 MHz | WCDMA | - | -115 | - | dBm/Hz |
| | 2305–2370 MHz | LTE Band 40 | - | -140 | - | dBm/Hz |
| | 2370–2400 MHz | LTE Band 40 | - | -134 | - | dBm/Hz |
| | 2496–2530 MHz | LTE Band 41 | - | -125 | - | dBm/Hz |
| | 2530–2560 MHz | LTE Band 41 | - | -138 | - | dBm/Hz |
| | 2570–2690 MHz | LTE Band 41 | - | -138 | - | dBm/Hz |
| | 5000–5900 MHz | WLAN 5G | - | -148 | - | dBm/Hz |

**Table 30. Bluetooth Transmitter Characteristics on HP RF Chain 3.3 V**

1. There is a variation of up to +/-1 dB in power across channels.
2. Noise-floor is -160 dBm/Hz with spurious tone power of -66 dBm at 1601.33 MHz when transmitted signal is at 2402 MHz.
3. Across the temperature range of -40 °C to +85 °C, the output power may degrade by up to 2 dB at -40 °C and by up to 5 dB at +85 °C.
4. There is a +/-2 dB of 3 sigma (99.7%) part-to-part power variation.

### 3.5.5 Bluetooth Transmitter Characteristics on Low-Power (LP) 0 dBm RF Chain

TA = 25 °C. Parameters are measured at antenna port and applicable to PA2G_AVDD/VINBCKDC=3.3V

- For Bluetooth C/I cases, the desired signal power is 3 dB above standard defined sensitivity level.

| Parameter | Condition/Notes | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Transmit Power | LE 1Mbps | - | - | -3.5 | dBm |
| | LE 2Mbps | - | - | -3.5 | dBm |
| | LR 500 Kbps | - | - | -3.5 | dBm |
| | LR 125 kbps | - | - | -3.5 | dBm |
| Adjacent Channel Power \|M-N\| = 2 | LE | - | - | -20 | dBm |
| | LR | - | - | -20 | dBm |
| Adjacent Channel Power \|M-N\| > 2 | LE | - | - | -30 | dBm |
| | LR | - | - | -30 | dBm |
| BR Modulation Characteristics | DH1 | -25 | - | 25 | kHz |
| | DH3 | -40 | - | 40 | kHz |
| | DH5 | -40 | - | 40 | kHz |
| | Drift Rate | -20 | - | 20 | kHz |
| | Δf1 Avg | 140 | - | 175 | kHz |
| | Δf2 Max | 115 | - | - | kHz |
| BLE Modulation Characteristics | Δf1 Avg | 225 | - | 275 | kHz |
| | Δf2 Max | 185 | - | - | kHz |
| | Δf2 Avg/Δf1 Avg | 0.8 | - | - | - |

**Table 31. Bluetooth Transmitter Characteristics on LP 0 dBm RF Chain**

1. There is a variation of up to 2 dB in power across parts and channels.
2. Noise-floor is -160 dBm/Hz with spurious tone power of -66 dBm at 1601.33 MHz when transmitted signal is at 2402 MHz.
3. Across the temperature range of -40 °C to +85 °C, the output power may degrade by up to 2 dB at -40 °C and by up to 5 dB at +85 °C.

### 3.5.6 Bluetooth Receiver Characteristics on High-Performance (HP) RF Chain

TA = 25 °C. Parameters are measured at antenna port and applicable to PA2G_AVDD/VINBCKDC=3.3 V

| Parameter | Condition/Notes | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Sensitivity, Dirty TX off (1), (2) | BR (1 Mbps), 339 bytes, DH5 Packet, BER= 0.1% | - | -90 | - | dBm |

| Parameter | Condition/Notes | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| | EDR2 (2 Mbps), 679 bytes, 2-DH5 Packet, BER= 0.01% | - | -91 | - | dBm |
| | EDR3 (3 Mbps), 1020 bytes, 3-DH5 Packet, BER= 0.01% | - | -85 | - | dBm |
| | LE (1 Mbps), 37 bytes, PER=30.8% | - | -92 | - | dBm |
| | LE (2 Mbps), 37 bytes, PER=30.8% | - | -90 | - | dBm |
| | LR (500 Kbps), 37 bytes, PER=30.8% | - | -99 | - | dBm |
| | LR (125 Kbps), 37 bytes, PER=30.8% | - | -103 | - | dBm |
| Maximum Input Level | BR, EDR2, EDR3, BER= 0.1% | - | -16 | - | dBm |
| | LE 1Mbps, 2Mbps, PER=30.8% | - | 10 | - | dBm |
| | LR 500kps, 125kbps, PER=30.8% | - | 10 | - | dBm |
| C/I Performance | BR, co-channel, BER=0.1% | 9 | - | - | dB |
| | BR, adjacent +1/-1 MHz, BER=0.1% | -2 | - | - | dB |
| | BR, adjacent +2/-2 MHz BER=0.1% | -19 | - | - | dB |
| | BR, adjacent >=\|±3\| MHz BER=0.1% | -19 | - | - | dB |
| | BR, Image channel BER=0.1% | -11 | - | - | dB |
| | BR, adjacent to Image channel BER=0.1% | -22 | - | - | dB |
| | EDR2, co-channel BER=0.1% | 11 | - | - | dB |
| | EDR2, adjacent +1/-1 MHz BER=0.1% | -2 | - | - | dB |
| | EDR2, adjacent +2/-2 MHz BER=0.1% | -17 | - | - | dB |
| | EDR2, adjacent >=\|±3\| MHz BER=0.1% | -17 | - | - | dB |
| | EDR2, Image channel BER=0.1% | -9 | - | - | dB |
| | EDR2, adjacent to Image channel BER=0.1% | -22 | - | - | dB |
| | EDR3, co-channel BER=0.1% | 19 | - | - | dB |
| | EDR3, adjacent +1/- MHz BER=0.1% | 3 | - | - | dB |
| | EDR3, adjacent +2/-2 MHz BER=0.1% | -12 | - | - | dB |
| | EDR3, adjacent >=\|±3\| MHz BER=0.1% | -12 | - | - | dB |
| | EDR3, Image channel BER=0.1% | -2 | - | - | dB |

| Parameter | Condition/Notes | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| | EDR3, adjacent to Image channel BER=0.1% | -15 | - | - | dB |
| | LE 1Mbps, co-channel PER=30.8% | - | 11 | - | dB |
| | LE 1Mbps, adjacent +1 MHz PER=30.8% | - | 1 | - | dB |
| | LE 1Mbps, adjacent -1 MHz PER=30.8% | - | -1 | - | dB |
| | LE 1Mbps, adjacent +2 MHz PER=30.8% | - | -22 | - | dB |
| | LE 1Mbps, adjacent -2 MHz PER=30.8% | - | -21 | - | dB |
| | LE 1Mbps, adjacent +3 MHz PER=30.8% | - | -20 | - | dB |
| | LE 1Mbps, adjacent -3 MHz PER=30.8% | - | -27 | - | dB |
| | LE 1Mbps, adjacent >= \|±4\| MHz PER=30.8% | - | -33 | - | dB |
| | LE 1Mbps, Image channel PER=30.8% | - | -22 | - | dB |
| | LE 1Mbps, +1MHz adjacent to Image channel PER=30.8% | - | -31 | - | dB |
| | LE 1Mbps, -1MHz adjacent to Image channel PER=30.8% | - | -20 | - | dB |
| | LE 2Mbps, co-channel PER=30.8% | - | 11 | - | dB |
| | LE 2Mbps, adjacent +2 MHz PER=30.8% | - | -4 | - | dB |
| | LE 2Mbps, adjacent -2 MHz PER=30.8% | - | -4 | - | dB |
| | LE 2Mbps, adjacent +4 MHz PER=30.8% | - | -13 | - | dB |
| | LE 2Mbps, adjacent -4 MHz PER=30.8% | - | -16 | - | dB |
| | LE 1Mbps, adjacent >= \|±6\| MHz PER=30.8% | - | -32 | - | dB |
| | LE 1Mbps, Image channel PER=30.8% | - | -13 | - | dB |
| | LE 1Mbps, +2MHz adjacent to Image channel PER=30.8% | - | -24 | - | dB |
| | LE 1Mbps, -2MHz adjacent to Image channel PER=30.8% | - | -4 | - | dB |

**Table 32. Bluetooth Receiver Characteristics on HP RF Chain**

1. **BR, EDR:** Receiver sensitivity is degraded by up to 9 dB for channels 38,78 due to the desensitization of the receiver by harmonics of the system clock (40MHz)
2. **BLE, LR:** Receiver sensitivity is degraded by up to 11.5 dB for channels 19,29,30,39 due to the desensitization of the receiver by harmonics of the system clock (40MHz)
3. There may be a degradation of up to 2 dB across the operating temperature range of -40 °C to +85 °C.

### 3.5.7 Bluetooth Receiver Characteristics on Low-Power (LP) RF Chain

TA = 25 °C. Parameters are measured at antenna port and applicable to PA2G_AVDD/VINBCKDC=3.3 V

| Parameter | Condition/Notes | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Sensitivity, Dirty TX off (1), (2) | BR (1 Mbps), 339 bytes, DH5 Packet BER= 0.1% | - | -85 | - | dBm |
| | EDR2 (2 Mbps), 679 bytes, 2-DH5 Packet, BER= 0.01% | - | -83 | - | dBm |
| | LE (1 Mbps), 37 bytes, PER=30.8% | - | -89 | - | dBm |
| | LE (2 Mbps), 37 bytes, PER=30.8% | - | -87 | - | dBm |
| | LR (500 Kbps), 37 bytes, PER=30.8% | - | -97 | - | dBm |
| | LR (125 Kbps), 37 bytes, PER=30.8% | - | -101 | - | dBm |
| Maximum Input Level | BR, EDR2 BER= 0.1% | - | -16 | - | dBm |
| | LE 1Mbps, 2Mbps PER=30.8% | - | 3 | - | dBm |
| | LR 500kps, 125kbps PER=30.8% | - | 10 | - | dBm |
| BER Floor | | - | 1e-4 | - | % |
| C/I Performance | BR, co-channel BER= 0.1% | 9 | - | - | dB |
| | BR, adjacent +1/-1 MHz, BER=0.1% | -2 | - | - | dB |
| | BR, adjacent +2/-2 MHz BER=0.1% | -19 | - | - | dB |
| | BR, adjacent >=\|±3\| MHz BER=0.1% | -19 | - | - | dB |
| | BR, Image channel BER=0.1% | -11 | - | - | dB |
| | BR, adjacent to Image channel BER=0.1% | -22 | - | - | dB |
| | EDR2, co-channel BER=0.1% | 11 | - | - | dB |
| | EDR2, adjacent +1/-1 MHz BER=0.1% | -2 | - | - | dB |
| | EDR2, adjacent +2/-2 MHz BER=0.1% | -17 | - | - | dB |

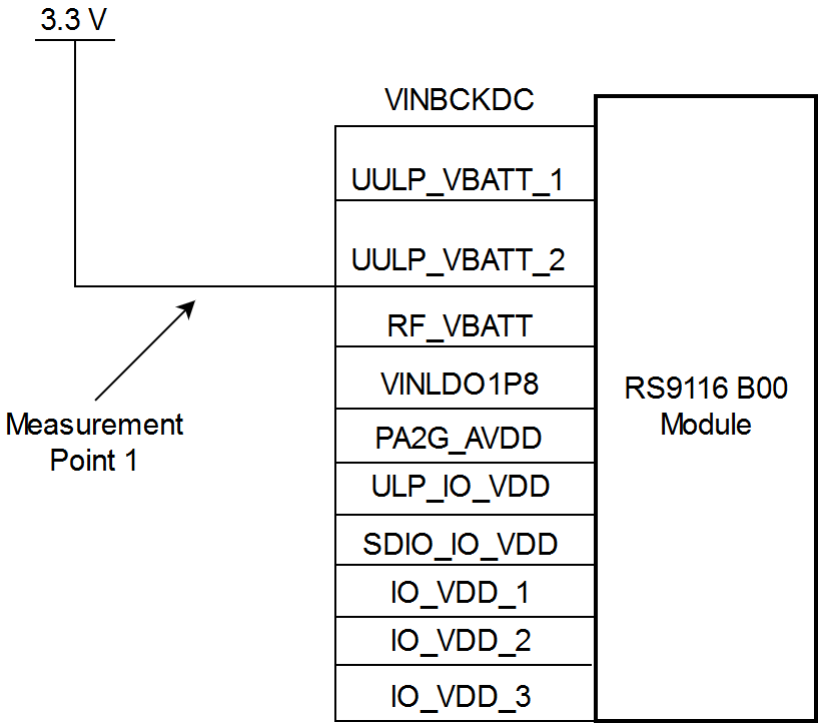
| Parameter | Condition/Notes | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| | EDR2, adjacent >=\|±3\| MHz BER=0.1% | -17 | - | - | dB |
| | EDR2, Image channel BER=0.1% | -9 | - | - | dB |
| | EDR2, adjacent to Image channel BER=0.1% | -22 | - | - | dB |
| | LE 1Mbps, co-channel PER=30.8% | - | 11 | - | dB |
| | LE 1Mbps, adjacent +1 MHz PER=30.8% | - | 0 | - | dB |
| | LE 1Mbps, adjacent -1 MHz PER=30.8% | - | -2 | - | dB |
| | LE 1Mbps, adjacent +2 MHz PER=30.8% | - | -22 | - | dB |
| | LE 1Mbps, adjacent -2 MHz PER=30.8% | - | -23 | - | dB |
| | LE 1Mbps, adjacent +3 MHz PER=30.8% | - | -21 | - | dB |
| | LE 1Mbps, adjacent -3 MHz PER=30.8% | - | -25 | - | dB |
| | LE 1Mbps, adjacent >= \|±4\| MHz PER=30.8% | - | -32 | - | dB |
| | LE 1Mbps, Image channel PER=30.8% | - | -26 | - | dB |
| | LE 1Mbps, +1MHz adjacent to Image channel PER=30.8% | - | -34 | - | dB |
| | LE 1Mbps, -1MHz adjacent to Image channel PER=30.8% | - | -21 | - | dB |
| | LE 2Mbps, co-channel PER=30.8% | - | 10 | - | dB |
| | LE 2Mbps, adjacent +2 MHz PER=30.8% | - | -4 | - | dB |
| | LE 2Mbps, adjacent -2 MHz PER=30.8% | - | 0 | - | dB |
| | LE 2Mbps, adjacent +4 MHz PER=30.8% | - | -12 | - | dB |
| | LE 2Mbps, adjacent -4 MHz PER=30.8% | - | -16 | - | dB |
| | LE 2Mbps, adjacent >= \|±6\| MHz PER=30.8% | - | -33 | - | dB |
| | LE 2Mbps, Image channel PER=30.8% | - | -12 | - | dB |
| | LE 2Mbps, 2MHz adjacent to Image channel PER=30.8% | - | -23 | - | dB |
| | LE 2Mbps, -2MHz adjacent to Image channel PER=30.8% | - | -4 | - | dB |

**Table 33. Bluetooth Receiver Characteristics on LP RF Chain**

1. **BR, EDR:** Receiver sensitivity is degraded by up to 9 dB for channels 38,78 due to the desensitization of the receiver from harmonics of the system clock (40MHz)
2. **BLE, LR:** Receive sensitivity is degraded by up to 11.5 dB for channels 19,29,30,39 due to the desensitization of the receiver from harmonics of the system clock (40MHz)
3. There may be a degradation of up to 2 dB across the operating temperature range of -40 °C to +85 °C.

## 3.6 Typical Current Consumption

### 3.6.1 3.3 V




#### 3.6.1.1 WLAN

| Parameter | Description | Value | Units |
|---|---|---|---|
| 1 Mbps Listen | LP Chain | 13.82 | mA |
| 1 Mbps RX Active | LP Chain | 19.67 | mA |
| 6 Mbps RX Active | HP Chain | 48.2 | mA |
| 72 Mbps RX Active | HP Chain | 48.2 | mA |
| 11 Mbps TX Active | Tx Power = Maximum (18dBm)<br>Tx Power = 8dBm | 270<br>130 | mA<br>mA |
| 6 Mbps TX Active | Tx Power = Maximum (18dBm)<br>Tx Power = 8dBm | 285<br>130 | mA<br>mA |
| 54 Mbps TX Active | Tx Power = Maximum (15dBm)<br>Tx Power = 8dBm | 200<br>130 | mA<br>mA |
| 72 Mbps TX Active | Tx Power = Maximum (12dBm) | 180 | mA |

| Parameter | Description | Value | Units |
|---|---|---|---|
| | Tx Power = 8dBm | 130 | mA |
| Deep Sleep | GPIO Wake up | 0.9 | uA |
| Standby | State retained | 13.1 | uA |
| Standby Associated, DTIM = 1 | | 293 | uA |
| Standby Associated, DTIM = 3 | | 119 | uA |
| Standby Associated, DTIM = 10 | | 51 | uA |

#### 3.6.1.2 Bluetooth BR and EDR

| Parameter | Description | Value | Units |
|---|---|---|---|
| TX Active Current, 1 Mbps BR | LP chain, Tx Power = -2 dBm<br>HP chain, Tx Power = Maximum (12 dBm) | 9.9<br>130 | mA<br>mA |
| RX Active Current, 1 Mbps BR | LP chain<br>HP chain | 10.2<br>26.7 | mA<br>mA |
| TX Active Current, 2 Mbps EDR | HP chain, Tx Power = Maximum (12 dBm) | 130 | mA |
| RX Active Current, 2 Mbps EDR | LP chain<br>HP chain | 10.2<br>26.7 | mA<br>mA |
| TX Active Current, 3 Mbps EDR | HP chain, Tx Power = Maximum (12 dBm) | 140 | mA |
| RX Active Current, 3 Mbps EDR | HP chain | 26.7 | mA |
| Deep Sleep | GPIO Wake up | 0.9 | uA |
| Standby | State RAM retained | 13.1 | uA |

#### 3.6.1.3 Bluetooth LE

| Parameter | Description | Value | Units |
|---|---|---|---|
| TX Active Current | LP chain, Tx Power = -2 dBm<br>LP Chain, Tx Power = 2 dBm<br>HP Chain, Tx Power = Maximum (18 dBm) | 8.9<br>-<br>190 | mA<br>mA<br>mA |
| RX Active Current | LP chain<br>HP chain | 10.9<br>26.7 | mA<br>mA |
| Deep Sleep | GPIO Wakeup | 0.9 | uA |
| Standby | State retained | 13.1 | uA |
| Advertising, Unconnectable | Advertising on all 3 channels<br>Advertising Interval = 1.28s<br>Tx Power = -2 dBm, LP chain | 22.4 | uA |
| Advertising, Connectable | Advertising on all 3 channels<br>Advertising Interval = 1.28s<br>Tx Power = -2 dBm, LP chain | 30.1 | uA |
| Connected | Connection Interval = 1.28s | 21.8 | uA |

| Parameter | Description | Value | Units |
|---|---|---|---|
| | No Data<br>Tx Power = -2 dBm, LP chain | | |
| Connected | Connection Interval = 200ms<br>No Data<br>Tx Power = -2 dBm, LP chain | 72 | uA |

# 4 RS9116 B00 Module Detailed Description

## 4.1 Overview

RS9116 B00 module is based on Silicon Labs' RS9116 ultra-low-power, single spatial stream, 802.11n + BT/BLE5.0 Convergence SoC. The RS9116 B00 module provides low-cost CMOS integration of a multi-threaded MAC processor (ThreadArch®), baseband digital signal processing, analog front-end, crystal oscillator, calibration eFuse, 2.4GHz RF transceiver, integrated power amplifier, match, bandpass filters (BPF), antenna diversity switch (DPDT) and Quad-SPI Flash thus providing a fully integrated solution for a range of hosted and embedded wireless applications. With Silicon Labs embedded four-threaded processor and on-chip ROM and RAM, these chipsets enable integration into low-cost and zero host load applications. With an integrated PMU and support for a variety of digital peripherals, RS9116 enables very low-cost implementations for wireless hosted and embedded applications. It can be connected to a host processor through SDIO, USB, SPI or UART interfaces. Wireless firmware upgrades and provisioning are supported.

## 4.2 Module Features

### 4.2.1 WLAN

- Compliant to single-spatial stream IEEE 802.11 b/g/n with single band support
- Support for 20 MHz channel bandwidth
- Transmit power up to +18 dBm with integrated PA
- Receive sensitivity as low as -96 dBm
- Data Rates: 802.11b: Up to 11 Mbps; 802.11g: Up to 54 Mbps; 802.11n: MCS0 to MCS7
- Operating Frequency Range: 2412 MHz – 2484 MHz

#### 4.2.1.1 MAC

- Conforms to IEEE 802.11b/g/n/j standards for MAC
- Dynamic selection of fragment threshold, data rate, and antenna depending on the channel statistics
- Hardware accelerators for WEP 64/128-bit and AES
- WPA, WPA2, and WMM support
- AMPDU and AMSDU aggregation for high performance
- Firmware downloaded from host based on application
- Hardware accelerators for DH (for WPS)

#### 4.2.1.2 Baseband Processing

- Supports DSSS for 1, 2 Mbps and CCK for 5.5, 11 Mbps
- Supports all OFDM data rates (6, 9, 12, 18, 24, 36, 48, 54 Mbps, MCS0 to MCS7), and Short GI in Hosted mode
- Supports IEEE 802.11n single-stream modes with data rates up to 72 Mbps
- Supports long, short, and HT preamble modes
- High-performance multipath compensation in OFDM, DSSS, and CCK modes

### 4.2.2 Bluetooth

- Transmit power up to +16 dBm with integrated PA
- Receive sensitivity: - LE: -92 dBm, LR 125 Kbps: -102 dBm
- Compliant to dual-mode Bluetooth 5
- <8 mA transmits current in Bluetooth 5 mode, 2 Mbps data rate
- Data rates: 125 Kbps, 500 Kbps, 1 Mbps, 2 Mbps, 3 Mbps

- Operating Frequency Range: 2.402 GHz - 2.480 GHz
- Bluetooth 2.1 + EDR, Bluetooth Low Energy 4.0 / 4.1 / 4.2 / 5.0
- Bluetooth Low Energy 1 Mbps, 2 Mbps and Long-Range modes
- Bluetooth Low Energy Secure connections
- Bluetooth Low Energy supports central role and peripheral role concurrently
- Bluetooth auto rate and auto TX power adaptation
- Scatternet* with two Secondary roles while still being visible

* For a detailed list of software features and available profiles, refer to the Software Reference Manuals or contact Silicon Labs for availability.

#### 4.2.2.1 MAC

##### 4.2.2.1.1 Link Manager

- Creation, modification & release of logical links
- Connection establishment between Link managers of two Bluetooth devices
- Link supervision is implemented in Link Manager
- Link power control is done depending on the inputs from Link Controller
- Enabling & disabling of encryption & decryption on logical links
- Services the data transport requests from L2CAP and provides required QOS
- Support for security using ECDH hardware accelerator

##### 4.2.2.1.2 Link Controller

- Encodes and decodes header of BT packets
- Manages flow control, acknowledgment, retransmission requests, etc.
- Stores the last packet status for all logical transports
- Chooses between SCO & ACL buffers depending on the control information coming from BBP resource manager
- Indicates the success status of packet transmission to upper layers
- Indicates the link quality to the LMP layer

##### 4.2.2.1.3 Host Controller

- Receives & decodes commands received from the Bluetooth Host.
- Propagates the decoded commands to respective modules
- Responsible for transmitting and receiving packets from and to Host
- Formats the responses coming from other modules of Bluetooth Controller as events and sends them to the Host.

##### 4.2.2.1.4 Device Manager

- Controls Scan & Connection processes
- Controls all BT Device operations except data transport operations
- Storing link keys
- BT Controller state transition management
- Slot synchronization & management
- Access contract management

- Scheduler

#### 4.2.2.2 Baseband Processing

- Supports GFSK (1 Mbps), EDR-DQPSK, EDR-D8PSK
- Supports BLE and Bluetooth long range
- Supports Data rates up to 3 Mbps

### 4.2.3 RF Transceiver

- Integrated 2.4 GHz transceiver with highly programmable operating modes
- Internal oscillator with 40 MHz crystal
- Inbuilt automatic boot up and periodic calibration enables ease of integration

### 4.2.4 Host Interfaces

- SDIO
    - Version 2.0-compatible
    - Supports 1-bit and 4-bit SDIO modes
    - Operation up to a maximum clock speed of 50 MHz
- SPI Interface
    - Operation up to a maximum clock speed of 100 MHz
- USB 2.0
    - Supports 480Mbps “High Speed” (HS), 12Mbps “Full Speed” (FS) and 1.5Mbps “Low Speed” (LS) serial data transmission
    - Support USB CDC and device mode
- UART
    - Supports variable baud rates between 9600 and 3686400 bps
    - AT command interface for configuration and data transmission/reception

**NOTE**: Hosted mode (n-Link) supports USB 2.0 and SDIO. Embedded Mode (WiSeConnect) supports SPI, USB CDC, SDIO, and UART.

#### 4.2.4.1 Auto Host Detection

RS9116 detects the host interface automatically after connecting to respective host controllers like SDIO, SPI, UART, USB and USB-CDC. SDIO/SPI host interface is detected through the hardware packet exchanges. UART host interface is detected through the software based-on the received packets on the UART interface. USB-Device mode interface is detected through the hardware based-on VBUS signal level. The host interface detection between USB & USB-CDC will be taken care by the firmware based on the USB_CDC_DIS GPIO. This Host configuration is stored in always-on domain registers after detection (on power up) and reused this information at each wakeup.

### 4.2.5 Wireless Coexistence Manager

- Arbitration between Wi-Fi, Bluetooth, and Bluetooth Low Energy
- Application aware arbitration
- Adaptive frequency hopping (AFH) in Bluetooth is based on WLAN channel usage
- Pre inter thread interrupts generation for radio switching
- QoS assurance across different traffics

### 4.2.6 Software

The RS9116 software package supports 802.11 b/g/n Client, Access Point (Up to 16 clients), Concurrent Client and Access Point mode, Enterprise Security, dual-mode BT 5.0 functionality on a variety of host platforms and operating

systems. The software package includes complete firmware, reference drivers, application profiles and configuration graphical user interface (GUI) for Linux operating systems. The Wi-Fi driver has support for a simultaneous access point, and client mode. Bluetooth host driver utilizes Opensource host stacks like BlueZ for Linux. The application layer supports all profiles supported by BlueZ on Linux. It has a wireless coexistence manager to arbitrate between protocols.

The RS9116 software package is available in two flavors

- **Hosted mode (n-Link™):** Wi-Fi stack, Bluetooth stack and profiles, and all network stacks reside on the host processor. Support for multiple Virtual Access Points available.
- **Embedded mode (WiSeConnect™):** Wi-Fi stack, TCP/IP stack, IP modules, Bluetooth stack and some profiles reside in RS9116; Some of the Bluetooth profiles reside in the host processor

**NOTE**: Please refer to the Software Manuals (TRM and PRM) in RS9116 Document Library for more details.

#### 4.2.6.1 Hosted Mode (n-Link™)

- Available host interfaces: SDIO 2.0 and USB HS
- Application data throughput up to 50 Mbps (Hosted Mode) in 802.11n with 20MHz bandwidth.
- Host drivers for Linux
- Support for Client mode, Access point mode (Up to 16 clients), Concurrent Client and Access Point mode, Enterprise Security
- Support for concurrent Wi-Fi, dual-mode Bluetooth 5

#### 4.2.6.2 Embedded Mode (WiSeConnect™)

- Available host interface: UART, SPI, SDIO, and USB CDC
- Support for Embedded Client mode, Access Point mode (Up to 8 clients), Concurrent Client and Access Point mode, and Enterprise Security
- Supports advanced security features: WPA/WPA2-Personal and Enterprise
- Integrated TCP/IP stack, HTTP/HTTPS, SSL/TLS, MQTT
- Bluetooth inbuilt stack support for L2CAP, RFCOMM, SDP, SPP, GAP
- Bluetooth profile support for GAP, SDP, SPP, GATT, L2CAP, RFCOMM
- Wireless firmware update and provisioning
- Support for concurrent Wi-Fi, dual-mode Bluetooth 5

> * For a detailed list of software features and available profiles, refer to the Software Reference Manuals or contact Silicon Labs for availability.

### 4.2.7 Security

RS9116 supports multiple levels of security capabilities available for the development of IoT devices.

- Accelerators: AES128/256 in Embedded Mode
- WPA/WPA2-Personal, WPA/WPA2 Enterprise for Client

> * For a detailed list of software features and available profiles, refer to the Software Reference Manuals or contact Silicon Labs for availability.

### 4.2.8 Power Management

The RS9116 chipsets have an internal power management subsystem, including DC-DC converters and linear regulators. This subsystem generates all the voltages required by the chipset to operate from a wide variety of input sources.

- LC DC-DC switching converter for RF and Digital blocks
    - Wide input voltage range (1.85 to 3.6V) on pin VINBCKDC
    - Output - 1.4V and 300mA maximum load on pin VOUTBCKDC
- SC DC-DC - Switching converter for Always-ON core logic domain
    - Wide input voltage range (1.85 to 3.6V) on pin UULP_VBATT_1 and UULP_VBATT_2
    - Output - 1.05V
- LDO SOC - Linear regulator for digital blocks
    - Input - 1.4V from LC DC-DC or external regulated supply on pin VINLDOSOC
    - Output - 1.15V and 300mA maximum load on pin VOUTLDOSOC
- LDO RF and AFE - Linear regulator for RF and AFE
    - Input - 1.4V from LC DC-DC or external regulated supply on pin RF_AVDD
    - Output - 1.1V and 20mA maximum load on pin VOUTLDOAFE

#### 4.2.8.1 Output Voltage Ranges

| Pin Description | Supply Voltage (V) | |
|---|---|---|
| | Min | Max |
| VOUTLDOSOC | 1.05 | 1.21 |
| VOUTBCKDC | 1.25 | 1.55 |
| VOUTLDOAFE | 1.0 | 1.22 |
| UULP_VOUTSCDC | 1.0 | 1.21 |
| UULP_VOUTSCDC_RETN | 0.715 | 1.21 |

**Table 34. Min and Max Specifications of Various Output Voltages**

The output voltages from the IC/module will be reflected as per specifications only after the firmware is loaded.

VOUTLDOAFE specifications are applicable whenever RF is initialized, and its maximum value can vary up to ±3% across temperature range.

### 4.2.9 Low Power Modes

It supports Ultra-low power consumption with multiple power modes to reduce the system energy consumption.

- Dynamic Voltage and Frequency Scaling
- Low Power (LP) mode with only the host interface active
- Deep sleep (ULP) mode with only the sleep timer active – with and without RAM retention
- Wi-Fi standby associated mode with automatic periodic wake-up
- Automatic clock gating of the unused blocks or transit the system from Normal to LP or ULP modes

#### 4.2.9.1 ULP Mode

In Ultra Low Power mode, the deep sleep manager has control over the other subsystems and processors and controls their active and sleep states. During deep sleep, the always-on logic domain operates on a lowered supply and a 32 kHz low-frequency clock to reduce power consumption. The ULP mode supports the following wake-up options:

- Timeout wakeup - Exit sleep state after programmed timeout value.
- GPIO Based Wakeup: Exit sleep state when GPIO goes High/Low based on programmed polarity.
- Analog Comparator Based wakeup - Exit sleep state on an event at the analog comparator.

- RTC Timer wakeup - Exit Sleep state on timeout of RTC timer
- WatchDog Interrupt based wakeup - Exit Sleep state upon watchdog interrupt timeout.

ULP mode is not supported in the USB interface mode

#### 4.2.9.2 LP Mode

In Low Power mode, Network processor maintains system state and gate all internal high frequency clocks. But host interface is ready to accept any command from host controller.

The LP mode supports the following wake-up options:

- Host Request - Exit sleep state on a command from HOST controller. whenever a command from the host is received, the processor serves the request with minimum latency and the clock is gated immediately after the completion of the operation to reduce power consumption
- GPIO based wakeup - Wakeup can be initiated through a GPIO pin
- Timeout wakeup - Exit sleep state after the programmed timeout value

### 4.2.10 Memory

#### 4.2.10.1 On-chip Memory

The ThreadArch® processor has the following memory:

- On-chip 384Kbytes SRAM for the wireless stack.
- 512Kbytes of ROM which holds the Secure primary bootloader, Network Stack, Wireless stacks, and security functions.
- 16Kbytes of Instruction cache enabling eXecute In Place (XIP) with quad SPI flash memory.
- eFuse of 512 bytes (used to store primary boot configuration, security, and calibration parameters)

#### 4.2.10.2 Serial Flash

The RS9116 utilizes a serial Flash to store processor instructions and other data. The SPI Flash Controller is a 1/2/4-wired interface for serial access of data from Flash. It can be used in either Single, Dual or Quad modes. Instructions are read using the Direct Fetch mode while data transfers use the Indirect Access mode. The SPI Flash Controller in RS9116 has been designed with programmable options for most of the single and multi-bit operations. RS9116 B00 module has 4 Mbytes internal flash memory.

User cannot use Flash for application code, but certificates can be loaded. For more details about loading certificates, refer to following documents:

- SAPI Reference Guide
- AT Command Reference Manual

# 5 RS9116 B00 Module Reference Schematics, BOM and Layout Guidelines

1. Customers should include provision for programming or updating the firmware at manufacturing.
2. If using UART, we recommend bringing out the SPI lines to test points, so designers could use the faster interface for programming the firmware as needed.
3. If using SPI as host interface, then firmware programming or update can be done through the host MCU, or if designer prefers to program standalone at manufacturing, then it is recommended to have test points on the SPI signals.
4. If SDIO/SPI/UART interface is not used, then their respective IO domains must still be connected to the power supply.

NOTE:

Refer and follow AN1345 Hardware Design checklist application note.

## 5.1 SDIO/SPI/UART

### 5.1.1 Schematics

The below diagram shows the typical schematic with SDIO/SPI/UART Host Interface and Internal Flash.

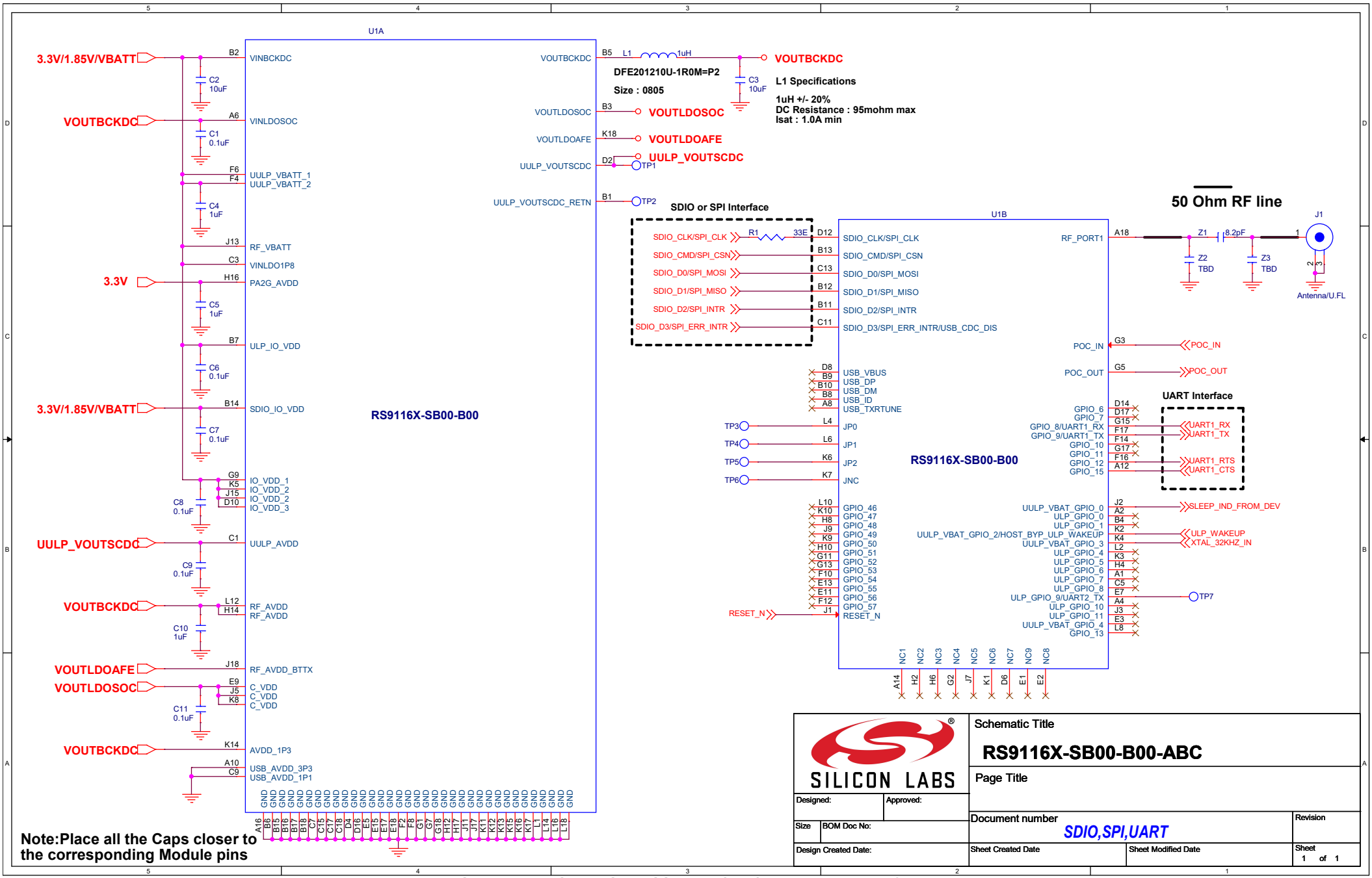



**Figure 16. Schematics with SDIO/SPI/UART Host Interface**

1. PA2G_AVDD can be driven by 3.3V source irrespective of other sources for Maximum Transmit Output power.
2. The supplies can be driven by different voltage sources within the recommended operating conditions specified in Specifications section.
3. SDIO_IO_VDD can be driven by a different source irrespective of other sources to support different interfaces.
4. In SDIO mode, pull-up resistors should be present on SDIO_CMD & SDIO Data lines as per the SDIO physical layer specification, version 2.0.
5. In SPI mode, ensure that the input signals, SPI_CSN and SPI_CLK are not floating when the device is powered up and reset is deasserted. This can be done by ensuring that the host processor configures its signals (outputs) before deasserting the reset. SPI_INTR is the interrupt signal driven by the Secondary device. This signal may be configured as Active-high or Active-low. If it is active-high, an external pull-down resistor is required. If it is active-low, an external pull-up resistor is required. The following action can be carried out by the host processor during power-up of the device, and before/after ULP Sleep mode.
    a. To use the signal in the Active-high or Active-low mode, ensure that, during the power up of the device, the Interrupt is disabled in the Host processor before deasserting the reset. After deasserting the reset, the Interrupt needs to be enabled only after the SPI initialization is done and the Interrupt mode is programmed to either Active-high or Active-low mode as required.
    b. The Host processor needs to disable the interrupt before the ULP Sleep mode is entered and enable it after SPI interface is reinitialized upon wakeup from ULP Sleep.
6. In UART mode, ensure that the input signals, UART_RX and UART_CTS are not floating when the device is powered up and reset is deasserted. This can be done by ensuring that the host processor configures its signals (outputs) before deasserting the reset.
7. Resistor "**R1**" should not be populated if UART is used as Host Interface.

### 5.1.2 Bill of Materials

| S.No. | Quantity | Reference | Value | Description | JEDEC | Manufacturer | Part Number |
|---|---|---|---|---|---|---|---|
| 1 | 2 | C2, C3 | 10uF | CAP CER 10UF 10V X5R 0805 | 0805 | Murata | GRM21BR61A106KE19L |
| 2 | 3 | C4, C5, C10 | 1uF | CAP CER 1UF 10V 10% X5R 0402 | 0402 | Murata | GRM155R61A105KE15D |
| 3 | 6 | C1, C6, C7, C8, C9, C11 | 0.1uF | CAP CER 0.1UF 10V X5R 0402 | 0402 | Murata | GRM155R61A104KA01D |
| 4 | 1 | Z1 | 8.2pF | CER CHP 8.2P +/-0.25P C0G 0201 25V | 0201 | Murata | GRM0335C1E8R2CD01D |
| 5 | 1 | J1 | | Antenna/U.FL | | | |

| S.No. | Quantity | Reference | Value | Description | JEDEC | Manufacturer | Part Number |
|---|---|---|---|---|---|---|---|
| 6 | 1 | L1 | 1uH | FIXED IND 1UH 2.0A 95 MOHM SMD | 0805 | Murata | DFE201210U-1R0M=P2 |
| 7 | 1 | R1 | 33E | RES SMD 33 OHM 5% 1/10W | 0402 | Panasonic | ERJ-2GEJ330X |
| 8 | 1 | U1 | | Wireless Single Band Module | | Silicon Labs | RS9116N-SB00-B00-B00 / RS9116W-SB00-B00-B24 / RS9116W-SB00-B00-B2A |
| 9 | 2 | Z2, Z3 | | Optional Capacitors for Antenna Matching | 0201 | | |

**Table 35. Bill of Materials with SDIO/SPI/UART Host Interface**

## 5.2 USB/USB-CDC

### 5.2.1 Schematics

The below diagram shows the typical schematic with USB/USB-CDC Host Interface and Internal Flash.

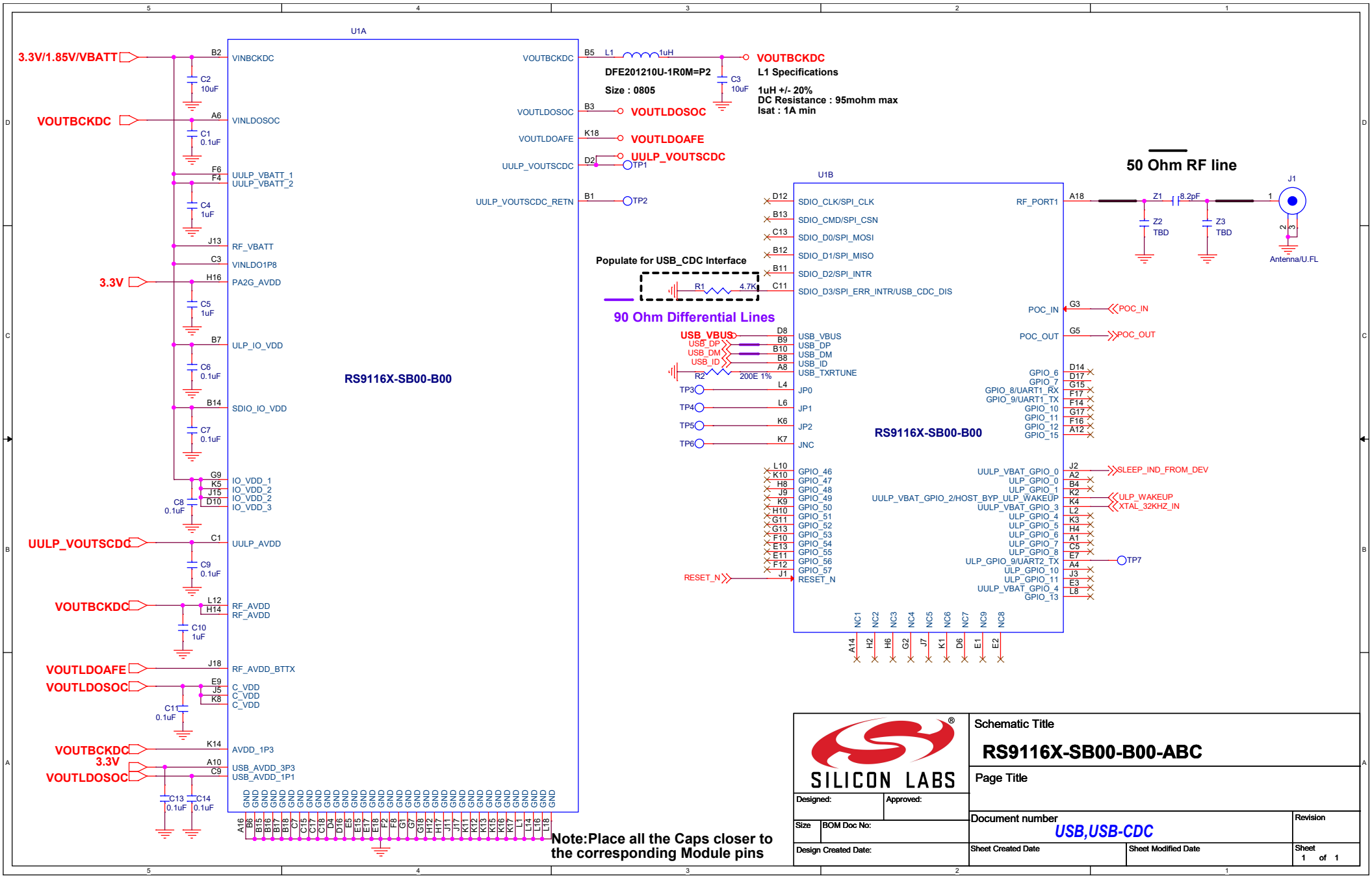



**Figure 17. Schematics with USB/USB-CDC Host Interface**

1. PA2G_AVDD can be driven by 3.3V source irrespective of other sources for Maximum Transmit Output power.
2. The supplies can be driven by different voltage sources within the recommended operating conditions specified in Specifications section.
3. Ensure that the pin USB_CDC_DIS is left unconnected to ensure normal USB functionality.
4. Resistor "**R1**" should not be populated if normal USB is used as Host Interface.

### 5.2.2 Bill of Materials

| S.No. | Quantity | Reference | Value | Description | JEDEC | Manufacturer | Part Number |
|---|---|---|---|---|---|---|---|
| 1 | 2 | C2, C3 | 10uF | CAP CER 10UF 10V X5R 0805 | 0805 | Murata | GRM21BR61A106KE19L |
| 2 | 3 | C4, C5, C10 | 1uF | CAP CER 1UF 10V 10% X5R 0402 | 0402 | Murata | GRM155R61A105KE15D |
| 3 | 8 | C1, C6, C7, C8, C9, C11, C13, C14 | 0.1uF | CAP CER 0.1UF 10V X5R 0402 | 0402 | Murata | GRM155R61A104KA01D |
| 4 | 1 | Z1 | 8.2pF | CER CHP 8.2P +/-0.25P C0G 0201 25V | 0201 | Murata | GRM0335C1E8R2CD01D |
| 5 | 1 | J1 | | Antenna/U.FL | | | |
| 6 | 1 | L1 | 1uH | FIXED IND 1UH 2.0A 95 MOHM SMD | 0805 | Murata | DFE201210U-1R0M=P2 |
| 7 | 1 | R1 | 4.7K | RES SMD 4.7K OHM 1% 1/16W 0402 | 0402 | Yageo | RC0402FR-074K7L |
| 8 | 1 | R2 | 200E | RES SMD 200 OHM 1% 1/20W 0201 | 0201 | Yageo | RC0201FR-07200RL |
| 9 | 1 | U1 | | Wireless Single Band Module | | Silicon Labs | RS9116N-SB00-B00-B00 / RS9116W-SB00-B00-B24 / RS9116W-SB00-B00-B2A |
| 10 | 2 | Z2, Z3 | | Optional Capacitors for Antenna Matching | 0201 | | |

**Table 36. Bill of Materials with USB/USB-CDC Host Interface**

## 5.3 Layout Guidelines

1. The following Supply Pins needs to be STAR routed from the Supply Source
    a. VINBCKDC
    b. UULP_VBATT_1
    c. UULP_VBATT_2
    d. RF_VBATT
    e. VINLDO1P8
    f. PA2G_AVDD
    g. ULP_IO_VDD
    h. SDIO_IO_VDD
    i. IO_VDD_1, IO_VDD_2, IO_VDD_3
2. The RF_PORT1 (Module Pin No. A18) signal may be directly connected to an on-board chip antenna or terminated in an RF connector of any form factor for enabling the use of external antennas.
3. There need to be DC blocking capacitors (8.2pF) on RF_PORT1 if they are connected to Antenna
4. The RF trace on RF_PORT1 should have a characteristic impedance of 50 Ohms. Any standard 50 Ohms RF trace (Microstrip or Coplanar wave guide) may be used. The width of the 50 Ohms line depends on the PCB stack, e.g., the dielectric of the PCB, thickness of the copper, thickness of the dielectric and other factors. Consult the PCB fabrication unit to get these factors right.
5. To evaluate transmit and receive performance like Tx Power and EVM, Rx sensitivity and the like, an RF connector would be required. A suggestion is to place a ‘microwave coaxial connector with switch’ between RF_PORT1 and the antenna.
6. The layout Guidelines for the BUCK are as follows: -
    a. Minimize the loop area formed by inductor switching node, output capacitors & input capacitors. This helps keep high current paths as short as possible. Keeping high current paths shorter and wider would help decrease trace inductance & resistance. This would significantly help increase the efficiency in high current applications. This reduced loop area would also help in reducing the radiated EMI that may affect nearby components.
    b. VINBCKDC Capacitor should be very close to the Module Pin & the Ground Pad of the capacitor should have direct vias to the Ground Plane underneath.
    c. Buck Inductor should be close to Module VOUTBCKDC pin and buck capacitor should be placed closed to the Inductor; the Ground Pad of the capacitor should have direct vias to the Ground Plane underneath.
    d. The Ground Plane underneath the Buck Inductor in the Top Layer should be made as an isolated copper patch and should descend down to the Second Layer (Main Ground) through multiple Vias.
    e. The path from VOUTBCKDC to VINLDOSOC is a high current path. The Trace should be as short & wide as possible and is recommended to run a Grounded Shield Traces on either side of this High Current Trace
    f. The Capacitor on VINLDOSOC should be very close to the Module Pin & the Ground Pad of the capacitor should have direct vias to the Ground Plane underneath.
7. For USB, it is recommended that the components and their values in the BoM be adhered to.
8. It is highly recommended that the two USB differential signals (USB_DP and USB_DN) be routed in parallel with a spacing (say, a) which achieves 90 Ω of differential impedances, 45 Ω for each trace.

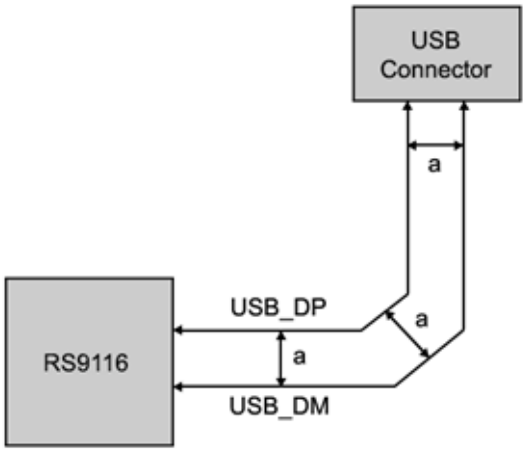



**Figure 18 Spacing between USB_DP and USB_DM**

9. To minimize crosstalk between the two USB differential signals (USB_DP and USB_DN) and other signal traces routed close to them, it is recommended that a minimum spacing of 3 x a be maintained for low-speed non-periodic signals and a minimum spacing of 7 x a be maintained for high-speed periodic signals.

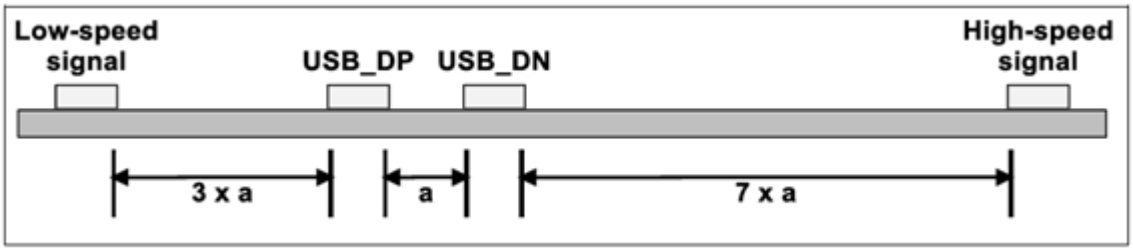



**Figure 19 Spacing for Low-speed and High-speed signals around USB_DP/USB_DN**

10. It is recommended that the total trace length of the signals between the RS9116 module and the USB connector be less than 450mm.
11. If the USB high-speed signals are routed on the Top layer, best results will be achieved if Layer2 is a ground plane. Furthermore, there must be only one ground plane under high-speed signals to avoid the high-speed signals crossing to another ground plane.

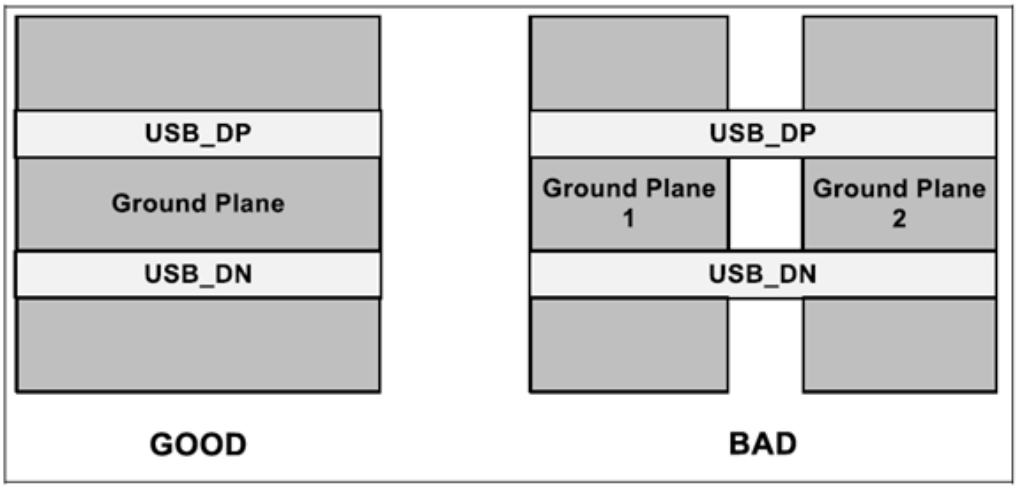


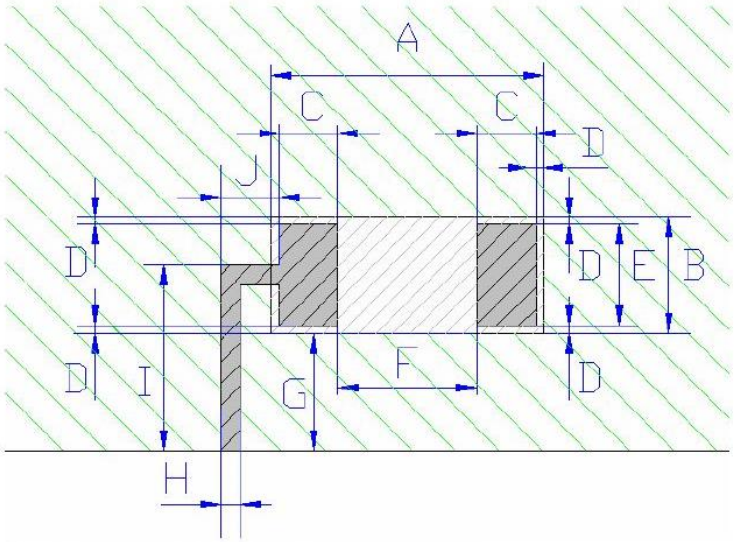

**Figure 20 Signals and the Ground Plane**

12. Each GND pin must have a separate GND via.
13. All decoupling capacitors placement must be as much close as possible to the corresponding power pins, and the trace lengths as short as possible.
14. Ensure all power supply traces widths are sufficient enough to carry corresponding currents.
15. Add GND copper pour underneath IC/Module in all layers, for better thermal dissipation.

The antenna layout guidelines for single band modules without antenna are below: -

The choice of antenna depends on the application. However, if an on-chip antenna is to be used, we recommend the Fractus FR05-S1-N-0-102.

There should be no metal planes or traces in the region under the PCB antenna. The Ground plane should be removed from under and both sides of the antenna. Follow the rules listed in the figure below while doing the layout for the chip antenna.




| Letter | Meas. |
|---|---|
| A | 7.00 |
| B | 3.00 |
| C | 1.50 |
| D | 0.20 |
| E | 2.60 |
| F | 3.60 |
| G | 3.00 |
| H | 0.50 |
| I | 4.75 |
| J | 1.50 |

*All dimensions are in millimetres.*

**Figure 21. Antenna Layout Recommendations**

- The above figure shows the antenna footprint details for 0.8 mm thickness FR4 PCB.
- This layout guidelines are as per antenna part guidelines. For more details, please refer to the antenna datasheet.

The recommended Chip Antennas are λ/4 antennas. They require an external ground plane for proper functioning. The length of the ground plane behind the antenna (from the feed point of antenna to backwards) should be at least 25mm – the longer the ground plane the better the performance.

It is recommended to characterize the antenna portion using a Network Analyzer. Electrical performance of any chip antenna is influenced by the physical characteristics of the surrounding ground plane, feed line, other devices, and materials. This can be used as an advantage by manipulating certain parameters to affect resonant frequency and matching.

These parameters are listed below:

1. Ground plane configuration
2. Distance from antenna
3. Topology around antenna
4. Feed point transmission line impedance
5. Trace width
6. Trace length
7. Matching Network
8. PCB substrate thickness
9. PCB substrate dielectric constant.

NOTE:

Refer and follow AN1343 B00 Board Layout Guidelines Application Note.

# 6 RS9116 B00 Module Package Description

## 6.1 Dimensions

| Parameter | Value (LxWxH) | Units |
|---|---|---|
| Module Dimensions | 7.9 x 4.63 x 0.9 | mm |
| Tolerance | ±0.1 | mm |

**Table 37 Module Dimensions**

## 6.2 Package Outline

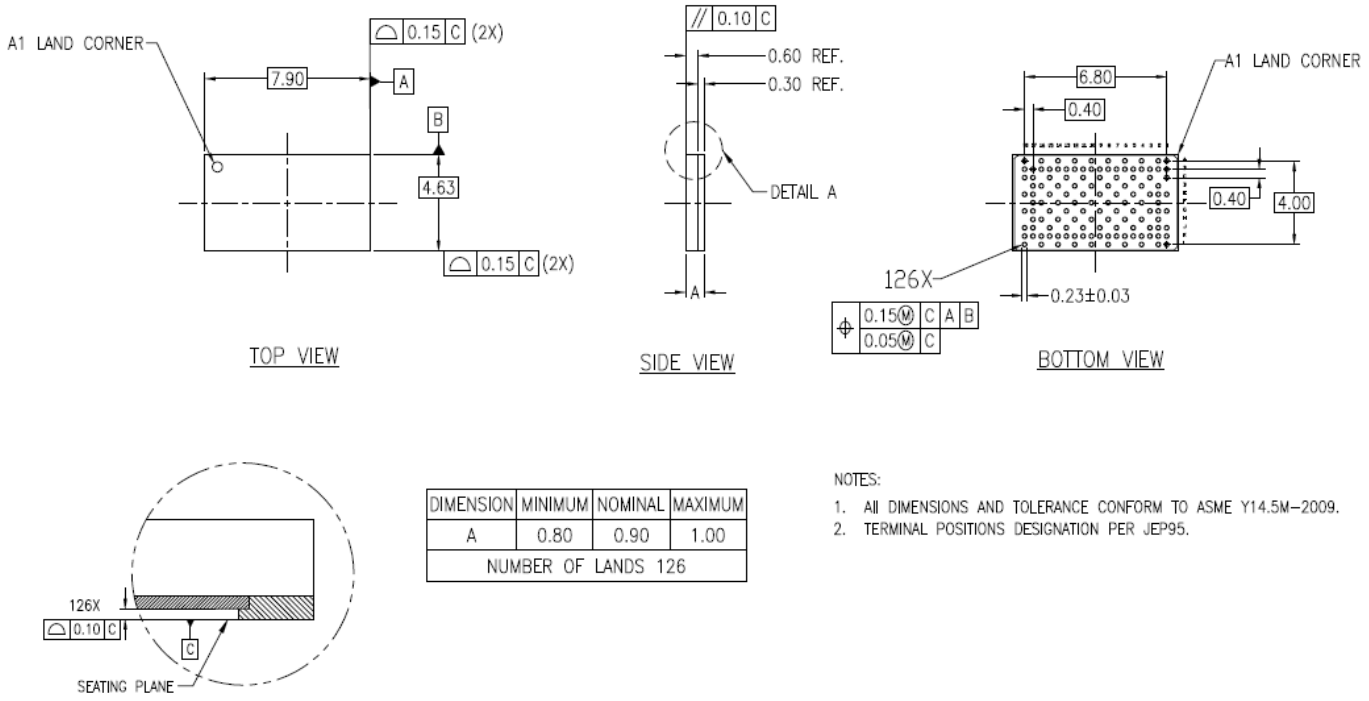



**Figure 22. Module Dimensions**

## 6.3 Pin Locations

All coordinates in the table below are in millimeters, and in TOP VIEW.

| Pin Number | X-Coordinate | Y-Coordinate | Pin Number | X-Coordinate | Y-Coordinate | Pin Number | X-Coordinate | Y-Coordinate | Pin Number | X-Coordinate | Y-Coordinate |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 | -3.4 | 2 | C9 | -0.2 | 1.2 | F14 | 1.8 | 0 | J17 | 3 | -1.2 |
| A2 | -3.0 | 2 | C11 | 0.6 | 1.2 | F16 | 2.6 | 0 | J18 | 3.4 | -1.2 |
| A4 | -2.2 | 2 | C13 | 1.4 | 1.2 | F17 | 3 | 0 | K1 | -3.4 | -1.6 |
| A6 | -1.4 | 2 | C15 | 2.2 | 1.2 | G1 | -3.4 | -0.4 | K2 | -3.0 | -1.6 |

| Pin Number | X-Coordinate | Y-Coordinate | Pin Number | X-Coordinate | Y-Coordinate | Pin Number | X-Coordinate | Y-Coordinate | Pin Number | X-Coordinate | Y-Coordinate |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A8 | -0.6 | 2 | C17 | 3 | 1.2 | G2 | -3.0 | -0.4 | K3 | -2.6 | -1.6 |
| A10 | 0.2 | 2 | C18 | 3.4 | 1.2 | G3 | -2.6 | -0.4 | K4 | -2.2 | -1.6 |
| A12 | 1 | 2 | D2 | -3.0 | 0.8 | G5 | -1.8 | -0.4 | K5 | -1.8 | -1.6 |
| A14 | 1.8 | 2 | D4 | -2.2 | 0.8 | G7 | -1.0 | -0.4 | K6 | -1.4 | -1.6 |
| A16 | 2.6 | 2 | D6 | -1.4 | 0.8 | G9 | -0.2 | -0.4 | K7 | -1.0 | -1.6 |
| A18 | 3.4 | 2 | D8 | -0.6 | 0.8 | G11 | 0.6 | -0.4 | K8 | -0.6 | -1.6 |
| B1 | -3.4 | 1.6 | D10 | 0.2 | 0.8 | G13 | 1.4 | -0.4 | K9 | -0.2 | -1.6 |
| B2 | -3.0 | 1.6 | D12 | 1 | 0.8 | G15 | 2.2 | -0.4 | K10 | 0.2 | -1.6 |
| B3 | -2.6 | 1.6 | D14 | 1.8 | 0.8 | G17 | 3 | -0.4 | K11 | 0.6 | -1.6 |
| B4 | -2.2 | 1.6 | D16 | 2.6 | 0.8 | G18 | 3.4 | -0.4 | K12 | 1 | -1.6 |
| B5 | -1.8 | 1.6 | D17 | 3 | 0.8 | H2 | -3.0 | -0.8 | K13 | 1.4 | -1.6 |
| B6 | -1.4 | 1.6 | E1 | -3.4 | 0.4 | H4 | -2.2 | -0.8 | K14 | 1.8 | -1.6 |
| B7 | -1.0 | 1.6 | E2 | -3.0 | 0.4 | H6 | -1.4 | -0.8 | K15 | 2.2 | -1.6 |
| B8 | -0.6 | 1.6 | E3 | -2.6 | 0.4 | H8 | -0.6 | -0.8 | K16 | 2.6 | -1.6 |
| B9 | -0.2 | 1.6 | E5 | -1.8 | 0.4 | H10 | 0.2 | -0.8 | K17 | 3 | -1.6 |
| B10 | 0.2 | 1.6 | E7 | -1.0 | 0.4 | H12 | 1 | -0.8 | K18 | 3.4 | -1.6 |
| B11 | 0.6 | 1.6 | E9 | -0.2 | 0.4 | H14 | 1.8 | -0.8 | L1 | -3.4 | -2.0 |
| B12 | 1 | 1.6 | E11 | 0.6 | 0.4 | H16 | 2.6 | -0.8 | L2 | -3.0 | -2.0 |
| B13 | 1.4 | 1.6 | E13 | 1.4 | 0.4 | H17 | 3 | -0.8 | L4 | -2.2 | -2.0 |
| B14 | 1.8 | 1.6 | E15 | 2.2 | 0.4 | J1 | -3.4 | -1.2 | L6 | -1.4 | -2.0 |
| B15 | 2.2 | 1.6 | E17 | 3 | 0.4 | J2 | -3.0 | -1.2 | L8 | -0.6 | -2.0 |
| B16 | 2.6 | 1.6 | E18 | 3.4 | 0.4 | J3 | -2.6 | -1.2 | L10 | 0.2 | -2.0 |
| B17 | 3 | 1.6 | F2 | -3.0 | 0 | J5 | -1.8 | -1.2 | L12 | 1 | -2.0 |
| B18 | 3.4 | 1.6 | F4 | -2.2 | 0 | J7 | -1.0 | -1.2 | L14 | 1.8 | -2.0 |
| C1 | -3.4 | 1.2 | F6 | -1.4 | 0 | J9 | -0.2 | -1.2 | L16 | 2.6 | -2.0 |
| C3 | -2.6 | 1.2 | F8 | -0.6 | 0 | J11 | 0.6 | -1.2 | L18 | 3.4 | -2.0 |
| C5 | -1.8 | 1.2 | F10 | 0.2 | 0 | J13 | 1.4 | -1.2 | | | |
| C7 | -1.0 | 1.2 | F12 | 1 | 0 | J15 | 2.2 | -1.2 | | | |

**Table 38. Pin Locations**

### 6.3.1 PCB Landing Pattern

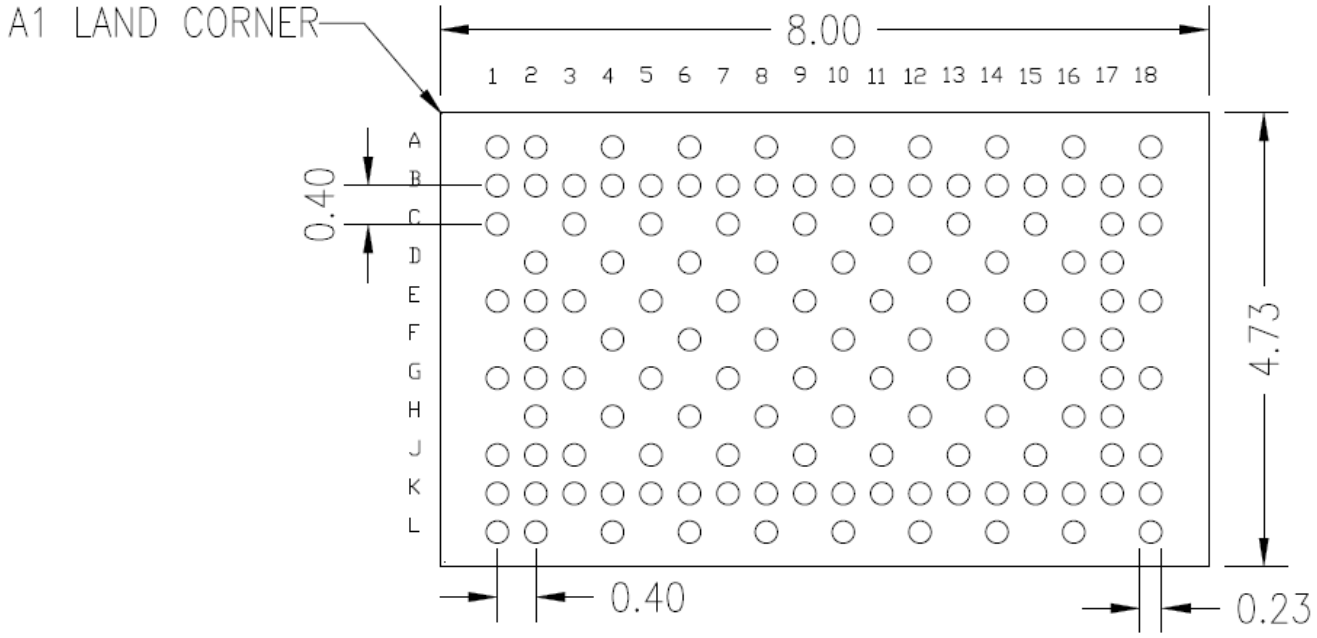



**Figure 23. PCB Landing Pattern**

# 7 RS9116 B00 Module Certification and Ordering Information

## 7.1 Certification Information

This section will outline the regulatory certification information for the RS9116 modules for the countries listed below. This information will be updated when available.

1. United States
2. Canada
3. Europe
4. Japan
5. United Kingdom
6. Other Regulatory Jurisdictions

The RS9116 single band B00 module from Silicon Labs has undergone modular certification for FCC, IC, MIC, CE/ETSI (including EN 300 328 v2.2.2), and UKCA. Note that any changes to the module's configuration including (but not limited to) the programming values of the RF Transceiver and Baseband can cause the performance to change beyond the scope of the certification. These changes, if made, may result in the module having to be certified afresh.

## 7.2 Compliance and Certification

RS9116 - B0014 module is FCC/IC/CE/MIC/UKCA certified. This section outlines the regulatory information for the RS9116 - B0014 module. This allows integrating the module in an end product without the need to obtain subsequent and separate approvals from these regulatory agencies. This is valid in the case no other intentional or un-intentional radiator components are incorporated into the product and no change in the module circuitry. Without these certifications, an end product cannot be marketed in the relevant regions. RF Testing Software is provided for any end product certification requirements.

### 7.2.1 Federal Communication Commission Statement

This device complies with FCC Rules Part 15. Operation is subject to the following two conditions:

• This device may not cause harmful interference.

• This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a class B digital device, pursuant to Part 15 of the Federal Communications Commission (FCC) rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by doing one or more of the following measures:

• Reorient or relocate the receiving antenna.

• Increase the separation between the equipment and receiver.

• Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

• Consult the dealer or an experienced radio/TV technician for help.

#### 7.2.1.1 FCC Caution

Any changes or modifications not expressly approved by the party responsible for compliance could void the user‘s authority to operate the equipment.

The antenna(s) used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

#### 7.2.1.2 Radiation Exposure Statements

This equipment must be installed and operated in accordance with provided instructions and the antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

#### 7.2.1.3 FCC Label Instructions

The outside of final products that contains this module device must display a label referring to the enclosed module. This exterior label can use wording such as: “Contains Transmitter Module FCC ID: XF6-B001P4V2P1”, or

“Contains FCC ID: XF6-B001P4V2P1”, Any similar wording that expresses the same meaning may be used.

### 7.2.2 Industry Canada / ISED Statement

This product meets the applicable Innovation, Science and Economic Development Canada technical specifications.

Ce produit repond aux specifications techniques applicables a l'innovation, Science et Developpement economique Canada.

#### 7.2.2.1 Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Déclaration d’exposition aux radiations:

Cet équipement est conforme aux limites d’exposition aux rayonnements IC établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

1) This device may not cause interference, and

2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le present appareil est conforme aux CNR d’Industrie Canada applicables aux appareils radio exempts de licence. L’exploitation est autorisee aux deux conditions suivantes:

1) l’appareil ne doit pas produire de brouillage;

2) l’utilisateur de l’appareil doit accepter tout brouillage radioelectrique subi, meme si le brouillage est susceptible d’en compromettre le fonctionnement.

#### 7.2.2.2 Labeling and User Information

**Innovation, Science and Economic Development Canada ICES003 Compliance Label**: CAN ICES-3 (B)/NMB-3(B)

The RS9116 - B0014 module has been labeled with its own IC ID number (8407A-B001P4V2P1) and if the IC ID is not visible when the module is installed inside another device, then the outside of the finished product into which the module is installed must also display a label referring to the enclosed module. This exterior label can use following wording: Contains Transmitter Module IC: 8407A-B001P4V2P1 or Contains IC: 8407A-B001P4V2P1 User manuals for license-exempt radio apparatus shall contain the above mentioned statement or equivalent notice in a conspicuous location in the user manual or alternatively on the device or both

Le module RS9116 - B0014 a été étiqueté avec son propre numéro d’ID IC (8407A-B001P4V2P1) et si l’ID IC n’est pas visible lorsque le module est installé dans un autre périphérique, alors l’extérieur du produit fini dans lequel le module est installé doit également afficher une étiquette faisant référence au module inclus. Cette étiquette extérieure peut être libellée comme suit: Contient le module émetteur IC: 8407A-B001P4V2P1 ou contient IC: 8407A-B001P4V2P1. Les manuels d'utilisation d'appareils radio exemptés de licence doivent contenir l'énoncé susmentionné ou une notification équivalente à un endroit bien en évidence dans le manuel d'utilisation. ou alternativement sur l'appareil ou les deux

### 7.2.3 Regulatory Module Integration Instructions

#### 7.2.3.1 List of Applicable FCC Rules

This device complies with part 15.247 of the FCC Rules.

#### 7.2.3.2 Summarize the Specific Operational Use Conditions

This module can be used in household electrical appliances as well as lighting equipment(s). The input voltage to the module should be nominally 1.8-3.3 Vdc, typical and the ambient temperature of the module should not exceed 85℃. This module using two kinds of antennas, PCB antenna with maximum gain is 1.00 dBi. Other antenna arrangement is not covered

#### 7.2.3.3 Limited Module Procedures

Not applicable

#### 7.2.3.4 Trace Antenna Designs

Not applicable

#### 7.2.3.5 RF Exposure Considerations

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator and your body. If the device built into a host as a portable usage, the additional RF exposure evaluation may be required as specified by§ 2. 1093.by this certification. The antenna is not field replaceable. If the antenna needs to be changed, the certification should be re-applied.

#### 7.2.3.6 Antennas

Provision for Chip Antenna or other Antennae

#### 7.2.3.7 Label and Compliance Information

Already in the manual

#### 7.2.3.8 Information on Test Modes and Additional Testing Requirements

a) The modular transmitter has been fully tested by the module grantee on the required number of channels, modulation types, and modes, it should not be necessary for the host installer to re-test all the available transmitter modes or settings. It is recommended that the host product manufacturer, installing the modular transmitter, perform some investigative measurements to confirm that the resulting composite system does not exceed the spurious emissions limits or band edge limits (e.g., where a different antenna may be causing additional emissions).

b) The testing should check for emissions that may occur due to the intermixing of emissions with the other transmitters, digital circuitry, or due to physical properties of the host product (enclosure). This investigation is especially important when integrating multiple modular transmitters where the certification is based on testing each of them in a stand-alone configuration. It is important to note that host product manufacturers should not assume that because the modular transmitter is certified that they do not have any responsibility for final product compliance.

c) If the investigation indicates a compliance concern the host product manufacturer is obligated to mitigate the issue. Host products using a modular transmitter are subject to all the applicable individual technical rules as well as to the general conditions of operation in Sections 15.5, 15.15, and 15.29 to not cause interference. The operator of the host product will be obligated to stop operating the device until the interference has been corrected

#### 7.2.3.9 Additional Testing, Part 15 Sub Part B Disclaimer

The final host / module combination needs to be evaluated against the FCC Part 15Bcriteria for unintentional radiators in order to be properly authorized for operation as a Part15 digital device.

#### 7.2.3.10 Steps for TX Verification

Already in the manual

#### 7.2.3.11 Other in User Manual

The host integrator installing this module into their product must ensure that the final composite product complies with the FCC requirements by a technical assessment or evaluation to the FCC rules, including the transmitter operation and should refer to guidance in KDB 996369.

#### 7.2.3.12 Frequency Spectrum to be Investigated

For host products with certified modular transmitter, the frequency range of investigation of the composite system is specified by rule in Sections 15.33(a)(1) through (a)(3), or the range applicable to the digital device, as shown in Section 15.33(b)(1), whichever is the higher frequency range of investigation.

#### 7.2.3.13 Operating the Host Product

When testing the host product, all the transmitters must be operating. The transmitters can be enabled by using publicly available drivers and turned on, so the transmitters reactive. In certain conditions it might be appropriate to use a technology-specific call box (test set) where accessory devices or drivers are not available. When testing for emissions from the unintentional radiator, the transmitter shall be placed in the receive mode or idle mode, if possible. If receive mode only is not possible then, the radio shall be passive (preferred) and/or active scanning. In these cases, this would need to enable activity on the communication BUS (i.e., PCIe, SDIO, USB) to ensure the unintentional radiator circuitry is enabled. Testing laboratories may need to add attenuation or filters depending on the signal strength of any active beacons (if applicable) from the enabled radio(s). See ANSI C63.4, ANSI C63.10 and ANSI C63.26 for further general testing details.

### 7.2.4 MIC

Telefication, operating as Conformity Assessment Body (CAB ID Number:211) with respect to Japan, declares that the RS9116 – B0014 complies with Technical Regulations Conformity Certification of specified Radio equipment (ordinance of MPT Nº 37,1981)

- The validity of this Certificate is limited to products, which are equal to the one examined in the type-examination
- When the manufacturer (or holder of this certificate) is placing the product on the Japanese market, the product must be affixed with the following Specified Radio Equipment marking R211-210209 for RS9116 – B0014.

### 7.2.5 Qualified Antenna Types

This device has been designed to operate with the antennas listed below. Antennas not included in this list or having a gain greater than listed gains in each region are strictly prohibited for use with this device. The required antenna impedance is 50 ohms.

Any antenna that is of the same type and of equal or less directional gain can be used without a need for retesting. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that permitted for successful communication. Using an antenna of a different type or gain more than certified gain will require additional testing.

| Brand | Antenna Model | Antenna Type | Gain (2.4 GHz) | Qualified Region |
|---|---|---|---|---|
| Fractus | FR05-S1-N-0-102 | PCB Trace Antenna | 1.70 dBi | FCC/IC, CE, MIC, UKCA |
| Taoglas | GW.34.5153 | Dipole Antenna | 5.89 dBi | FCC/IC, CE, MIC, UKCA |
| Walsin | RFPCA500609IMAB301 | PCB Antenna | 4.53 dBi | MIC |

**Table 39. Qualified Antenna Types for B00 Module**

## 7.3 Marking Information

### 7.3.1 Certification Marking

The following certification markings will be provided on the shipment package of the RS9116 – B0014 module.

| Marking | | Description |
|---|---|---|
| Compliance Marks | | FCC Compliance Mark |
| | | CE Compliance Mark |
| | | MIC Compliance Mark |
| | | UKCA Compliance Mark |

### 7.3.2 Module Marking

The figure and table below illustrate the marking on the Single band module and explains the marking on the module.


**Figure 24. Module Marking Information**

| Marking | | Description |
|---|---|---|
| Part Number | PPPPPPPPPPP | Part Number Designation. |
| Lot Code Information | TTTTTT<br>YYWW | TTTTTT – A trace or manufacturing code. The first letter is the device revision (B = Silicon Rev 1.4).<br>YY – Last two digits of the assembly year<br>WW – Two-digit work week when the device was assembled |

## 7.4 Module Package

| Package Code | Package Type, Pins | Dimensions (mm) | Frequency Band | Integrated Antenna |
|---|---|---|---|---|
| B00 | LGA, 126 | 7.8 x 4.63 x 0.9 | Single Band (2.4 GHz) | No |

**Table 40. B00 Module Package**

## 7.5 Ordering Information

| Model Number | Part Number | Wireless and Memory |
|---|---|---|
| **Hosted Connectivity (n-Link)** | | |
| RS9116-B0014 | RS9116N-SB00-B00-B00 | SBW + BT 5 with internal flash; Rev 1.4 Silicon |
| **Embedded Connectivity (WiSeConnect)** | | |
| RS9116-B0014 | RS9116W-SB00-B00-B24 | SBW + BT 5 with internal flash; Rev 1.4 Silicon; Firmware version: 1.2.24 |
| RS9116-B0014 | RS9116W-SB00-B00-B2A | SBW + BT 5 with internal flash; Rev 1.4 Silicon; Firmware version: 2.0 or higher |

**Table 41. Part Ordering Options**

- SBW: Single Band Wi-Fi (2.4 GHz).
- Customer should include provision for programming or updating the firmware at manufacturing.

# 8 RS9116 B00 Module Documentation and Support

Silicon Labs offers a set of documents which provide further information required for evaluating and developing products and applications using RS9116. These documents are available in RS9116 Document Library on the Silicon Labs website. The documents include information related to Software releases, Evaluation Kits, User Guides, Programming Reference Manuals, Application Notes, and others.

For further assistance, you can contact Silicon Labs Technical Support here.

## 8.1 Resource Location

RS9116 Document Library: https://docs.silabs.com/rs9116/

Technical Support: http://www.silabs.com/support/

# 9 RS9116 B00 Module Revision History

| Revision No. | Version No. | Date | Changes |
|---|---|---|---|
| 1 | 1.0 | April, 2019 | Initial version |
| 2 | 1.0.1 | May, 2019 | • Updated host-based schematics. Combined SDIO, SPI & UART host interfaces into one schematic. Combined USB and USB-CDC host interfaces into one schematic<br>• Updated 32 KHz external oscillator specifications<br>• Updated antenna layout recommendations for single band antenna<br>• Updated the Schematics for UART_RTS and UART_CTS Pin correction. |
| 3 | 1.0.2 | May, 2019 | Renamed VOUTLDO1P8 as VINLDO1P8 in Pinout Description<br>Removed 32KHz XTAL Pins and used UULP GPIO for feeding in the External Clock. Updated the below sections for the same<br>• Pinout Description.<br>• Specifications<br>• Reference Schematics |
| 4 | 1.0.3 | July, 2019 | • Corrected the description of 32KHz external clock in Specifications section<br>• Added external control for POC_IN in Specifications<br>• Renamed LP_WAKEUP to LP_WAKEUP_IN and changed its description in Pinout table.<br>• Added host detection details and updated network processor memory details in Detailed description.<br>• Updated PCB landing pattern in Package Description<br>• Removed PLL_AVDD from Absolute Maximum Ratings and Recommended Operating conditions section<br>• Corrected the initial state of SDIO_D3 to pullup and SDIO_D2 to HighZ. |
| 5 | 1.0.4 | November, 2019 | Bluetooth ACI specs corrected (earlier version shows under Typ - should have been under “Min”) |
| 6 | 1.0.5 | July, 2020 | • Added note about voltage applied on external Buck Regulator for Typical Current Consumption at 1.85V.<br>• Updated Applications section.<br>• Updated 40 MHz Clock specifications.<br>• Updated LED0 software configuration note for ULP_GPIO_8 under Pin Description.<br>• Mentioned need for weak pull up resistor under Pin Description to use Wake-on-Wireless feature on ULP_GPIO_6.<br>• Updated "Digital Input Output Signals" to separate readings at 3.3V and 1.8V.<br>• Wireless Updated Co-Existence modes in Features list.<br>• The number of center roles supported by BLE changed from 8 to 6.<br>• Added a note under Pin Description regarding functionalities that are available on multiple Pins, and their proper usage. Eg. SLEEP_IND_FROM_DEV |

| Revision No. | Version No. | Date | Changes |
|---|---|---|---|
| | | | • Updated Generic PCB Layout Guidelines.<br>• Updated Power Sequence Diagrams under DC Characteristics for POC_IN and POC_OUT.<br>• Features list updated.<br>• Reflow profile diagram updated.<br>• Updated Typical values for BLE ACI characteristics.<br>• Updated GPIO pin descriptions.<br>• Updated Bluetooth EDR 2 Mbps LP Chain Receiver specification.<br>• Removed Legacy Bluetooth Tx on LP Chain.<br>• Updated WLAN 2.4 GHz 3.3V/1.85V Transmitter specifications. |
| 7 | 1.0.6 | August, 2020 | • Updated Features List removed redundant information.<br>• Updated Applications, and Software Architecture Diagrams.<br>• Updated pin descriptions - ULP_GPIO_0 and ULP_GPIO_6.<br>• Updated Software section with latest information.<br>• Rebranded to Silicon Labs. |
| 8 | 1.0.7 | September, 2020 | • Updated Device Information with new nomenclature to include Silicon revision, and firmware version.<br>• Updated nomenclature in Pinout diagram, and Pin descriptions.<br>• Updated schematics to include the new nomenclature.<br>• SoC Ordering information updated with new OPNs; Device Nomenclature diagram updated. |
| 9 | 1.0.8 | June, 2021 | • Module image updated with Silicon Labs logo.<br>• Added note under Software Architecture diagram on connecting and using multiple hosts at the same time.<br>• Included EN 300 328-v2.2.2 certification info.<br>• Removed redundant section ‘Device Information’. Same information is available in section ‘Ordering Information’.<br>• Pin names updated for consistency; included actual pin names along with signals; updated pins: UART1_RX, UART1_TX, UART2_TX, HOST_BYP_ULP_WAKEUP<br>• ULP_GPIOs in Pin Description referenced to ULP_IO_VDD instead of IO_VDD_1.<br>• Updated note on Wake-on-Wireless feature, under Description for pin ULP_GPIO_6.<br>• Removed ESD and Latch Up information from Absolute Ratings table.<br>• Updated Min and Max values for RF related pins to reflect only 3.3 V in Recommended Operating Conditions.<br>• Updated Min and Max values for IO pins to reflect both 1.8 V and 3.3 V related minimum (1.65/3.0), and maximum (1.98/3.6) values in Recommended Operating Conditions.<br>• Power-Up and Down Sequence with POC_IN connected internally. Included statement that this connection is NRND. |

| Revision No. | Version No. | Date | Changes |
|---|---|---|---|
| | | | • Updated $V_{IH}$, $V_{OH}$ to show only Min values; $V_{IL}$, $V_{OL}$ to show only Max values; $I_{OL}$, $I_{OH}$ to show only Typ values.<br>• Updated 32 kHz External Crystal Oscillator specifications to reflect correct Min and Max values for $V_{ac}$.<br>• Removed 40 MHz crystal specification because the crystal is integrated inside the module. Added a note under Clock Specifications.<br>• Timing data included for SDIO_CMD.<br>• Recommended Operating Conditions for PA2G_AVDD pin updated.<br>• Added caveats to the RF Characteristics.<br>• Updated RF Specification section to include numbers at 3.3 V only.<br>• Updated Note for IEEE spectral mask effects. Added mention of AN1337 application note for certification details.<br>• Included output voltage power ranges under Power Management.<br>• Typical Current Consumption section updated to include values at 3.3 V only.<br>• Removed section on Serial Flash; B00 does not support External Flash.<br>• Schematics updated to reflect correct voltage for PA2G_AVDD pin.<br>• Reference Schematics updated to show DC Resistance at 95mohm max (from 70), and Isat at 1.0A min (from 1.5).<br>• Updated Murata's 1uH inductor part in Schematics and BOM from DFE201210**S**-1R0M=P2 to DFE201210**U**-1R0M=P2.<br>• Updated description for DFE201210S-1R0M=P2 in BOM to FIXED IND 1UH 2.0A 95 MOHM SMD (from 2.3A 70 MOHM SMD).<br>• Updated Reference Schematics to reflect only 3.3 V input to RF pins.<br>• Removed External Flash Reference schematics.<br>• Updated Antenna Layout guidelines for Fractus FR05-S1-N-0-102.<br>• Removed Device Nomenclature.<br>• Appended B0014 Certification information.<br>• Removed Reflow Profile, Soldering and Baking instructions. Information available through the web based RFI system.<br>• Datasheet updated from Preliminary to Full Production. |
| 10 | 1.0.9 | December, 2022 | • Added UKCA certification details |
| 11 | 1.0.10 | March 2023 | • Added a brief description for POC_IN and POC_OUT<br>• Added conditions for the status of signals when they are driven by an external host<br>• Added description on status of USB_ID pin when not in use<br>• Added Power Up Sequence with EXT_PG_EN<br>• Provided Hardware Resetting sequence information<br>• Updated Absolute Max Rating & Recommended Operating Condition for RF_AVDD_BTTX pin |

| Revision No. | Version No. | Date | Changes |
|---|---|---|---|
| | | | • Updated Digital Input Output Signals and added a note for SDIO signal<br>• Added a note under Reference Schematics regarding power supply to IO domain when any interface/signal is not used<br>• Updated Recommended Operating Conditions: UULP_VBATT_1/2, RF_VBATT, VINBCKDC, VINLDO1P8 pins to have supply voltages at both 1.85/3.3 V; Reference Schematics updated to reflect this information<br>• Output Voltage Specs updated for VOUTLDOSOC, VOUTLDOAFE, UULP_VOUTSCDC, and UULP_VOUTSCDC_RETN pins. Added a note for VOUTLDOAFE under the specifications<br>• Corrected Operating Voltage range and Temperature range under Features section<br>• Included SDIO interface support for WiSeConnect.<br>• Updated Baseband processing data rate up to 72 Mbps for 802.11n single stream modes<br>• Minimum voltage rating for SDIO_IO_VDD, ULP_IO_VDD, and IO_VDD_1,2,3 pins updated to 1.75 V under Recommended Operating Conditions<br>• Certification symbols mentioned where applicable<br>• Added information about MIC certification<br>• Added Module Marking Information<br>• Updated Notes in RF Characteristics section regarding Power variation across channels and part-to-part<br>• Updated EVM-related notes for MCS7<br>• Added RAM size and certificates loading into Flash<br>• Added Power-Up Sequence with USB as host interface<br>• Replaced TELEC with MIC in all relevant sections<br>• Removed SPI_ERR_INTR from Section 2.2.3<br>• Notes added for JP0, JP1, JP2, and JNC pins<br>• Replaced CS to CSN in all relevant sections<br>• Removed SD-SPI from Section 4.2.4<br>• Added a column for model number in Section 7.5 |

**Table 42. Revision History**

# Simplicity Studio

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**400 West Cesar Chavez**
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