This test setup consists of one transmitter and two receivers ("Receiver" and "Clock"). "Receiver" signals refer to my non-working Si4432 receiver, and "Clock" signals refer to the working RFM12B.
Decoded data received at "Clock" receiver. This is the original receiver, and the data here is correct. A new packet is received every 4 seconds. Frequency hopping occurs between packets every 4 seconds with 3 frequencies used. Clear channel indicators on my Si4432 "Receiver" seem to be aligned with the 915MHZ markers.

"Receiver" signals refer to my non-working Si4432 receiver, and "Clock" signals refer to the working receiver (believed to be a RFM12B).
Valid, decoded data from the "Clock" receiver.

5.34mS

The 1 byte preamble, 2 byte sync, and 5 decoded data bytes shown above should have been received by my "Receiver" within this clear channel window. But it can be seen that the data is nonsense. The width of the clear channel window is sufficiently wide to have received the 8 bytes described above (8 x (1/19.2K) x 10 = 4.17mS minimum).

It is believed that the "Clock" receiver is a RFM12B module. It is a Chip On Board with glob top.