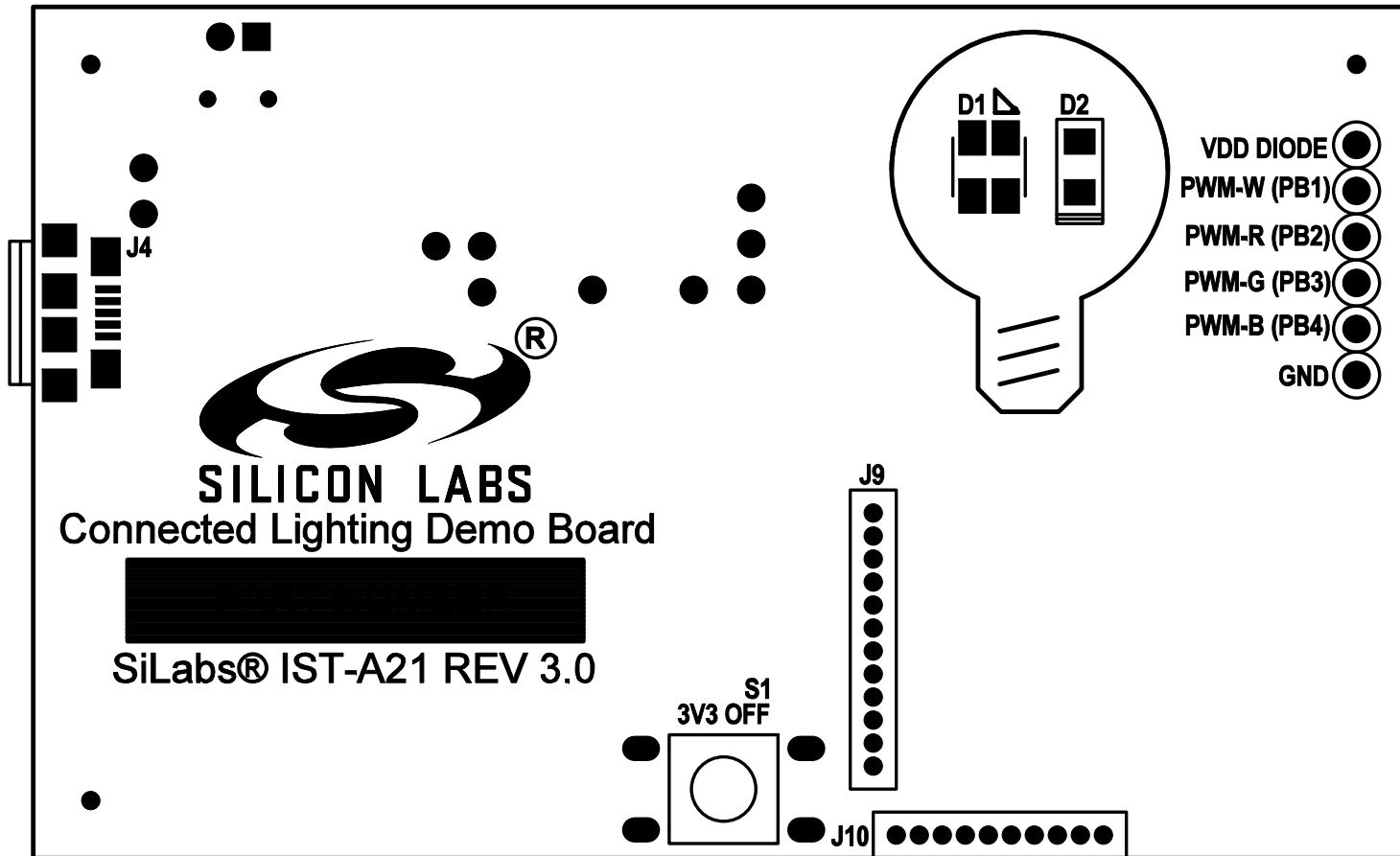
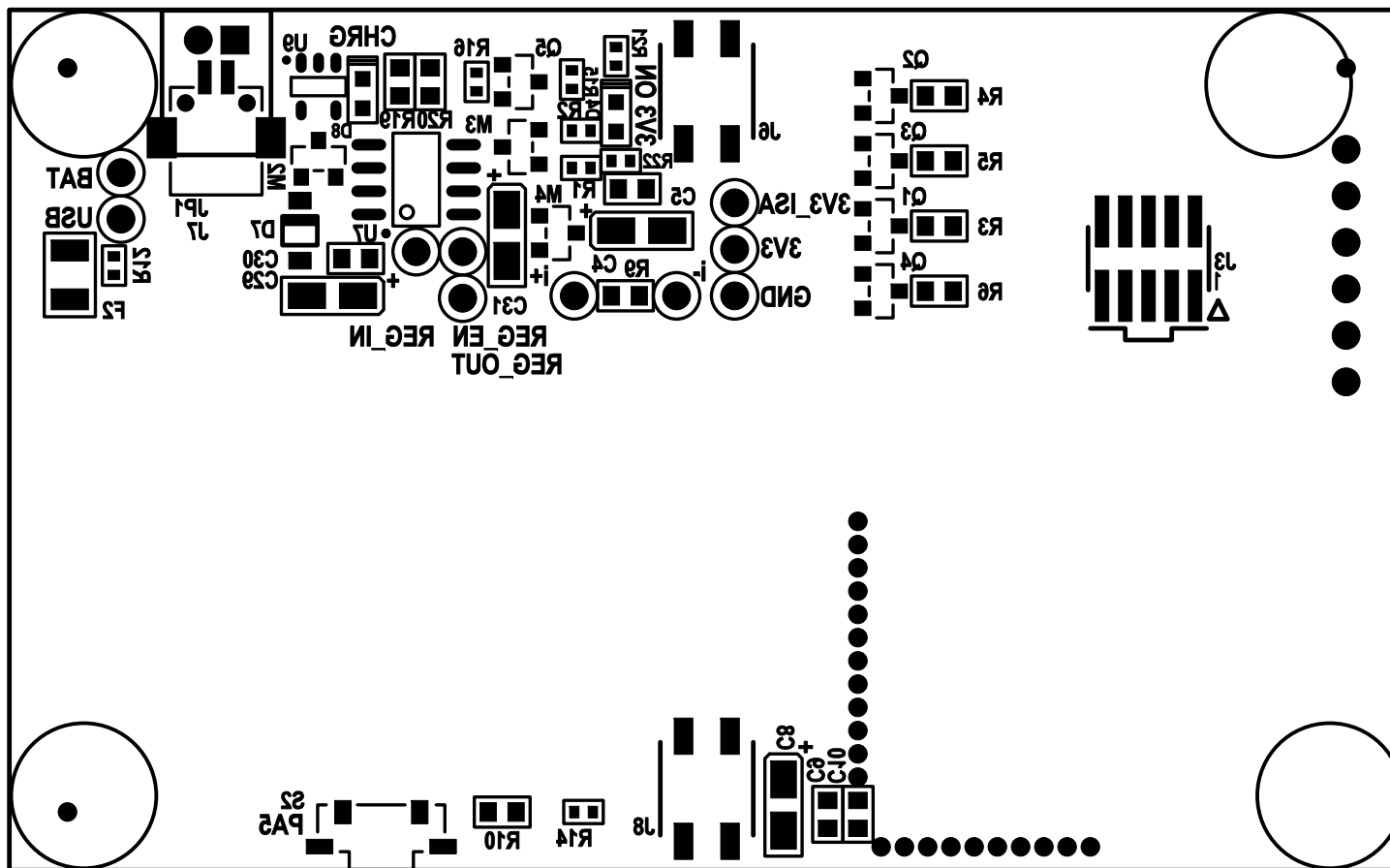


PRIMARY SILKSCREEN



SECONDARY SILKSCREEN



PRIMARY SILKSCREEN



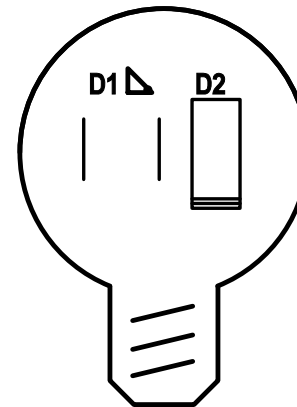
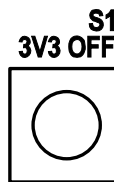
J4



SILICON LABS
Connected Lighting Demo Board



SiLabs® IST-A21 REV 3.0



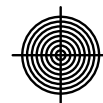
- VDD DIODE
- PWM-W (PB1)
- PWM-R (PB2)
- PWM-G (PB3)
- PWM-B (PB4)
- GND

J9

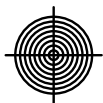
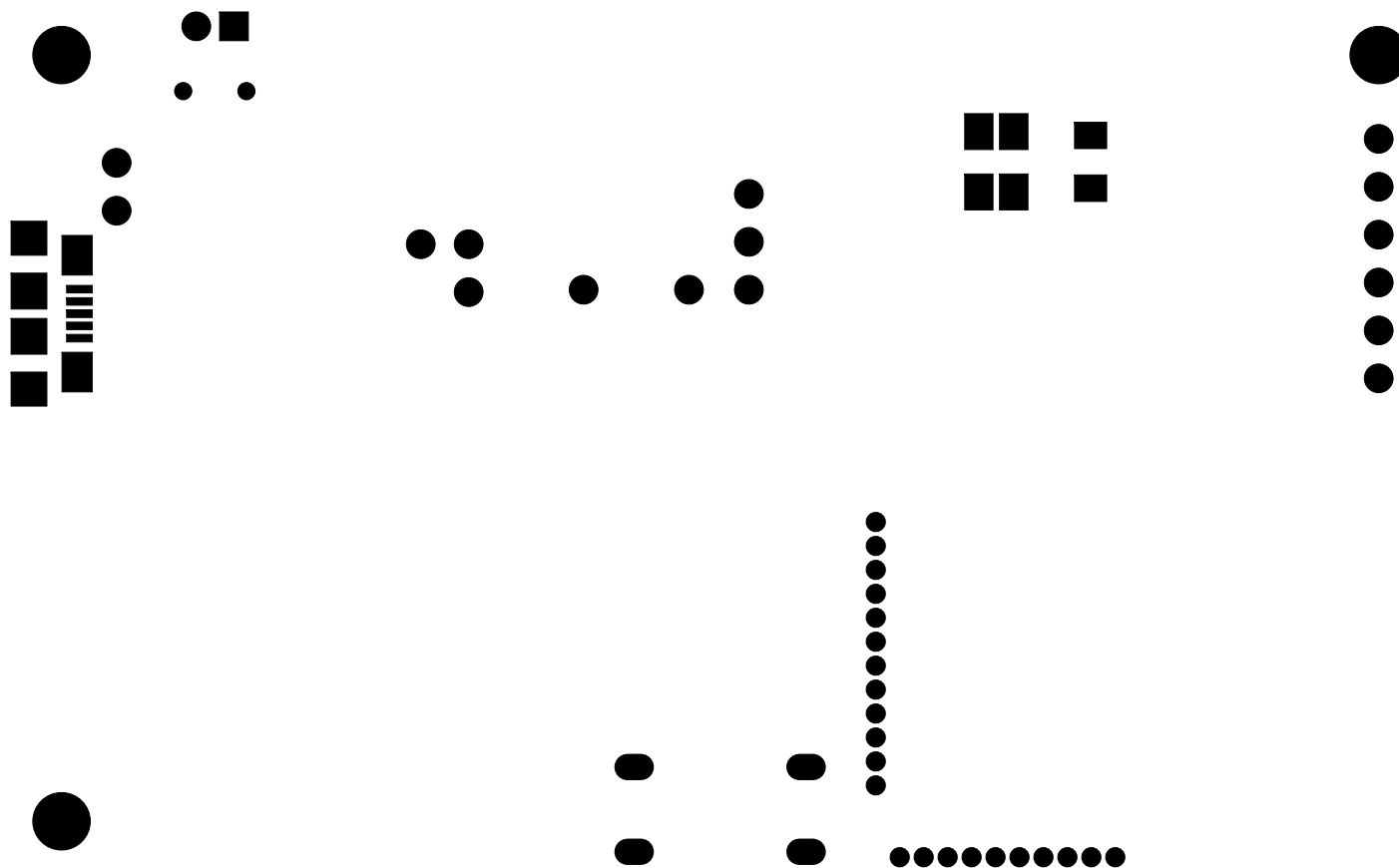


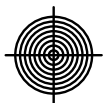
J10



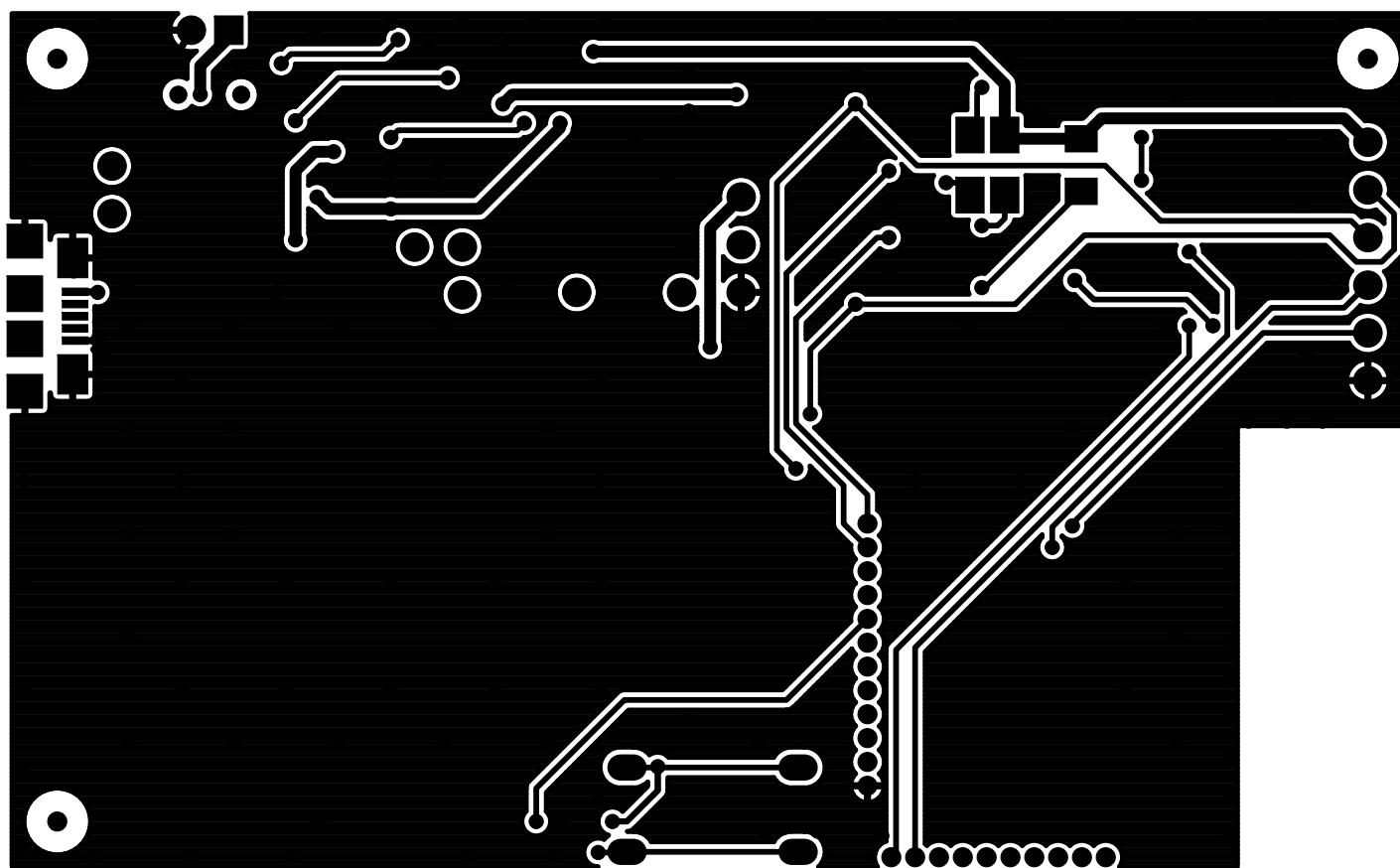
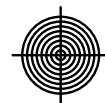


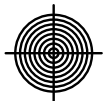
PRIMARY SOLDER MASK



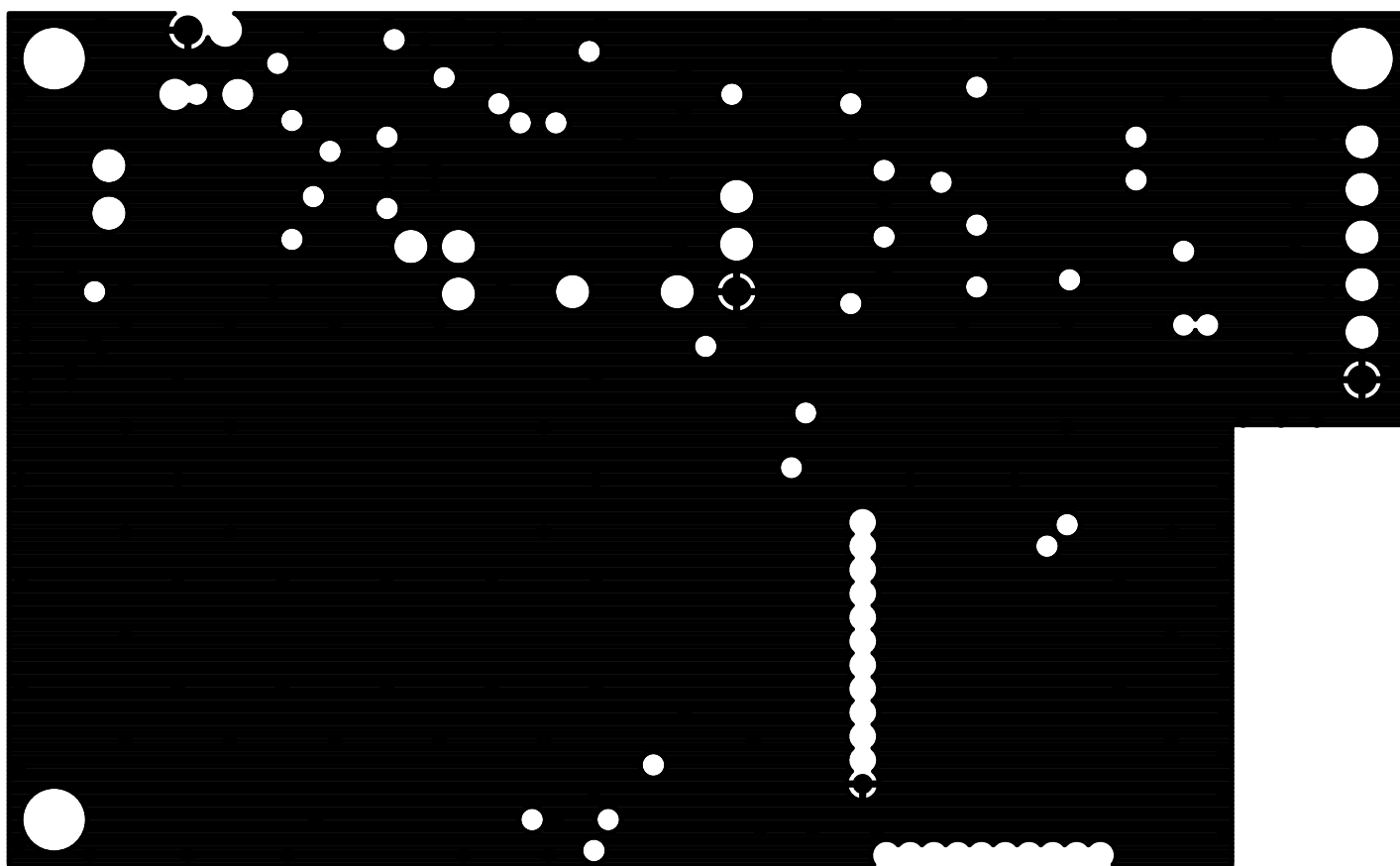
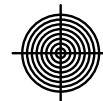


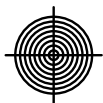
PRIMARY SIDE





GROUND PLANE 1



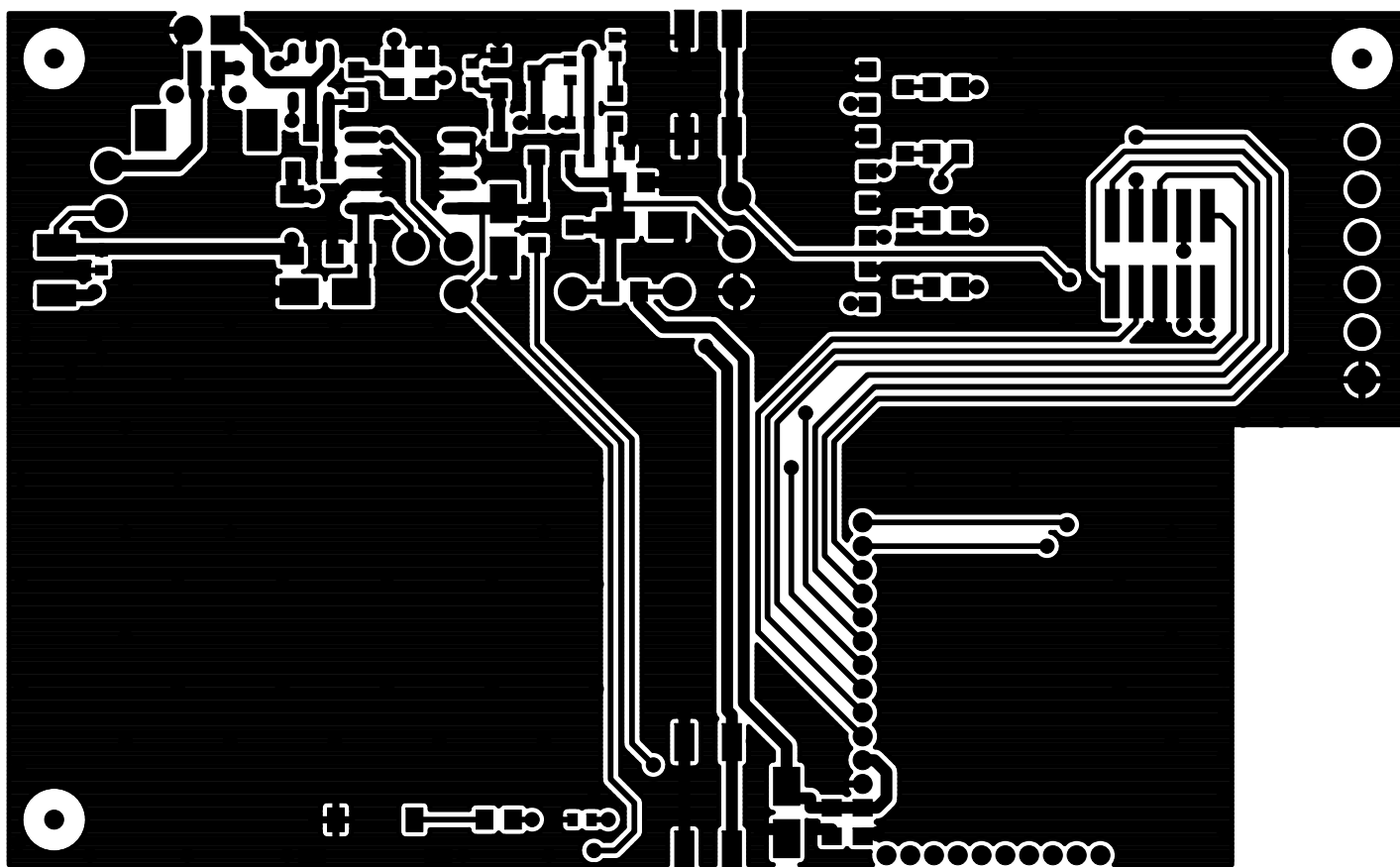
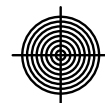


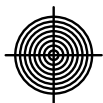
GROUND PLANE 2



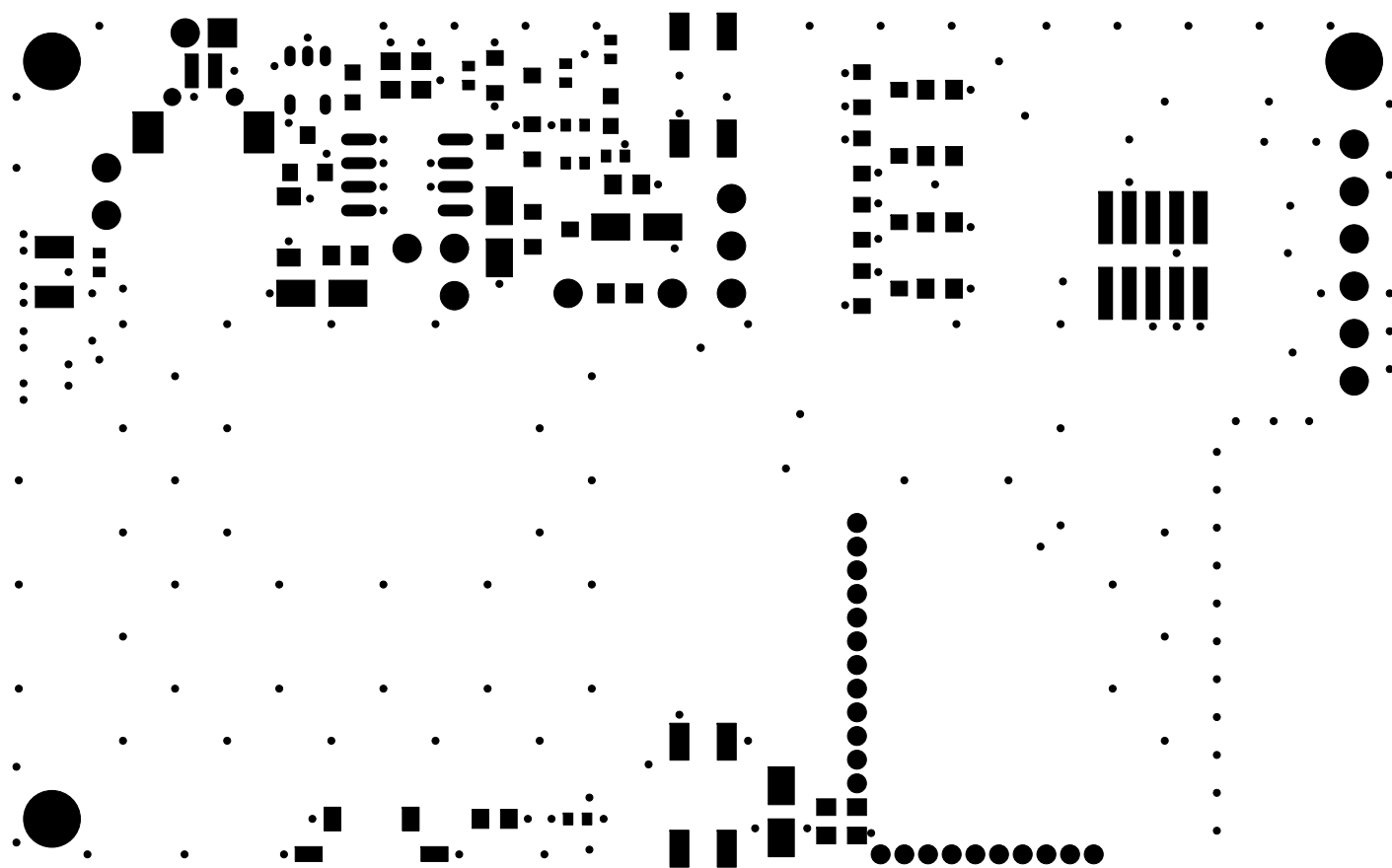


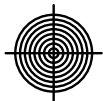
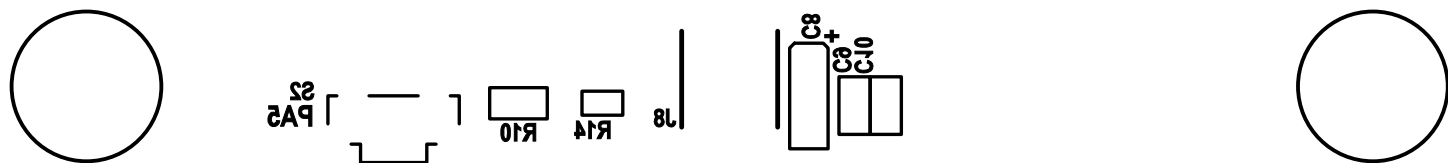
SECONDARY SIDE

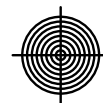
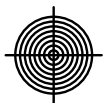




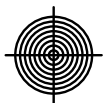
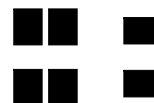
SECONDARY SOLDER MASK

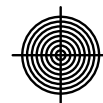




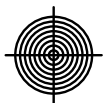
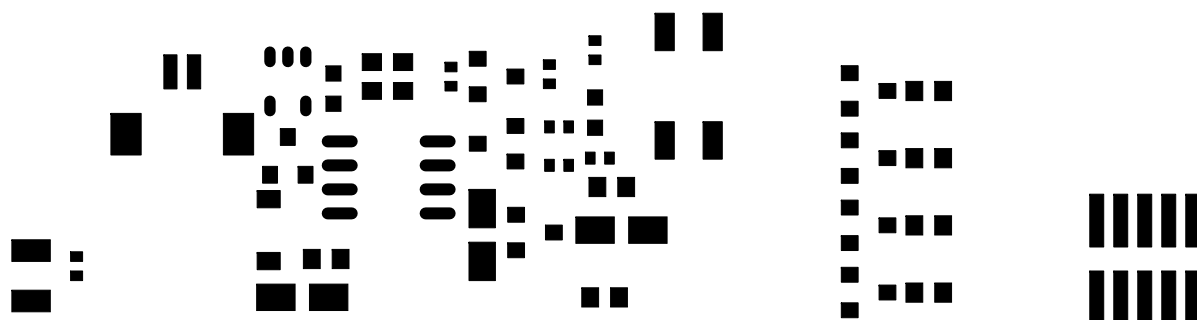


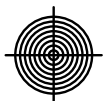
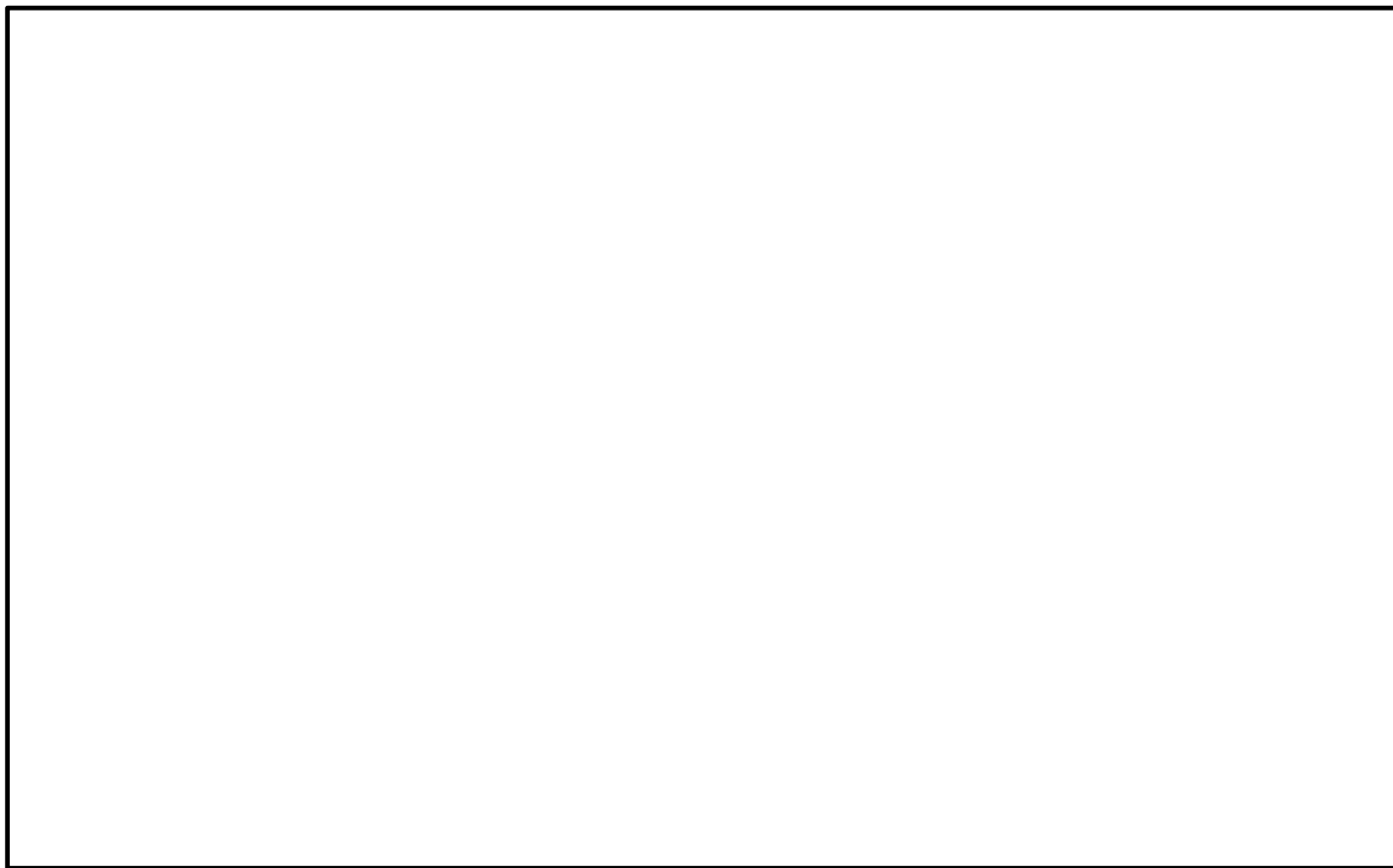
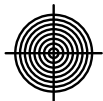
PRIMARY SOLDER PASTE

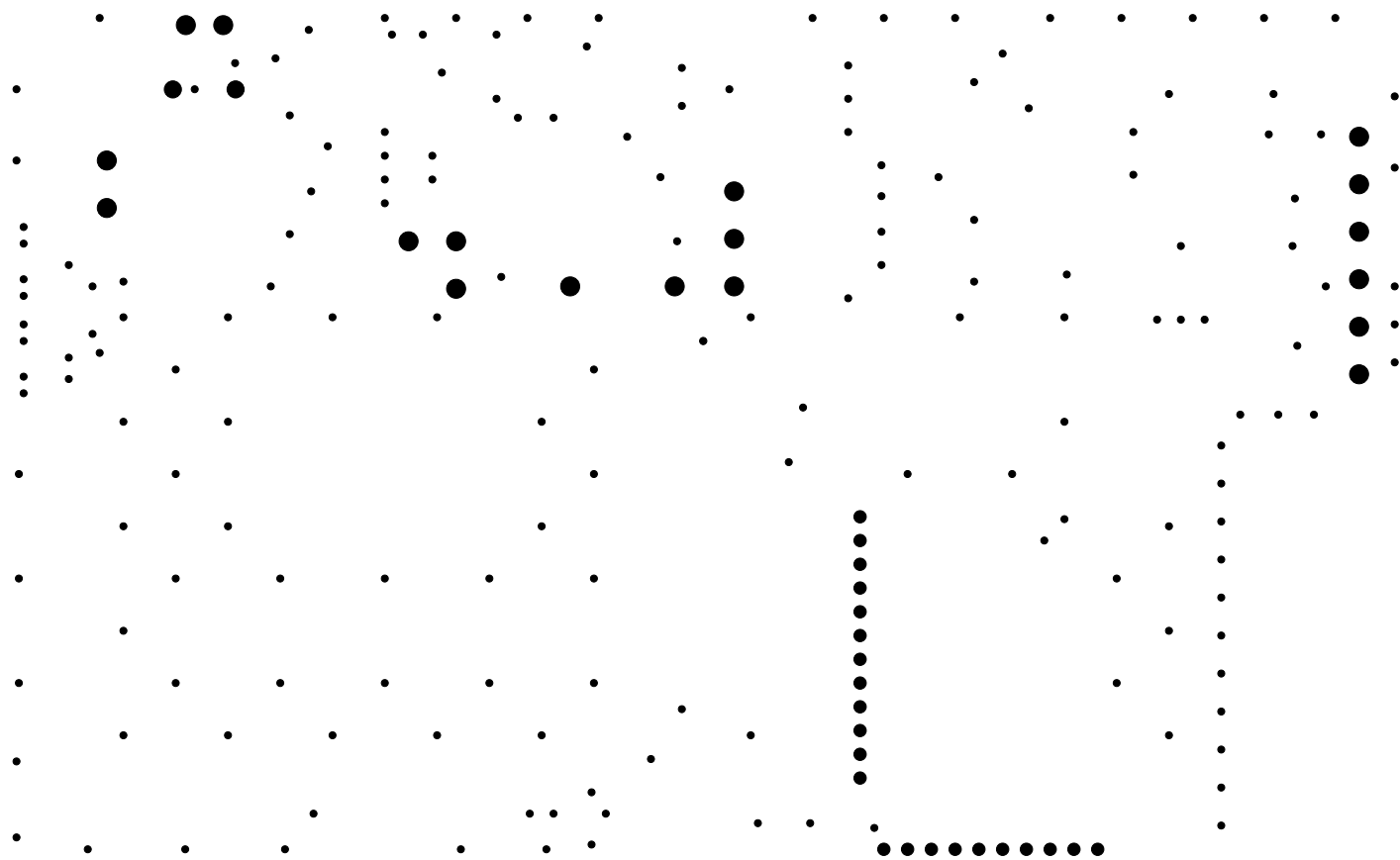




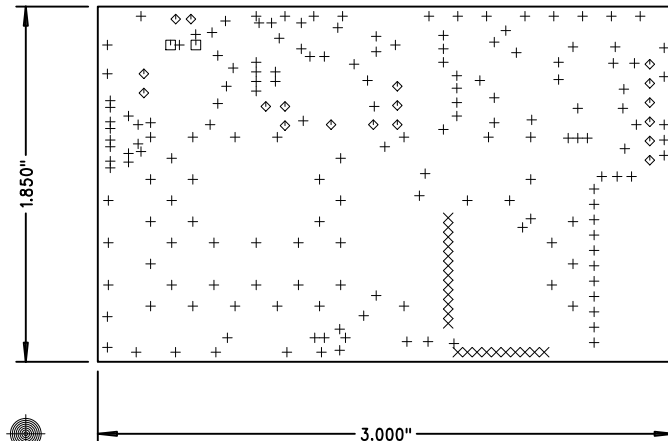
SECONDARY SOLDER PASTE







PRIMARY DRILL



NOTES : UNLESS OTHERWISE SPECIFIED

1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. MATERIAL SHALL BE COPPER CLAD FR-4, NEMA GRADE PER IPC-4101/26, COLOR NATURAL.
4. COPPER WEIGHT SHALL BE 0.5 OZ./SQ. FT. BEFORE PLATING.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE ± 0.003 ".
7. MINIMUM ANNULAR RING SHALL BE 0.001".
8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE 0.062" $\pm 10\%$.
10. WARP/TWIST SHALL NOT EXCEED 1.0%
11. FINISH SHALL BE LPI, BLACK SMOBC, ENIG BOTH SIDES.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. REFERENCE ADDITIONAL FAB NOTES IN FILE README.TXT


LAYER STACKUP

FILE NAMES

PRIMARY SILKSCREEN	A21_PSS.PHO
PRIMARY SOLDERMASK	A21_PSM.PHO
PRIMARY SIDE	A21_PRI.PHO
GROUND PLANE	A21_L02.PHO
GROUND PLANE	A21_L03.PHO
SECONDARY SIDE	A21_SEC.PHO
SECONDARY SOLDERMASK	A21_SSM.PHO
SECONDARY SILKSCREEN	A21_SSS.PHO

SCALE: NONE

SIZE	QTY	SYM	PLT	TOOL	TOL
0.015	176	+	P	1	+0/-0.015
0.026	22	X	P	2	+/-0.003
0.036	2	□	N	3	+/-0.003
0.040	18	◇	P	4	+/-0.003

UNLESS OTHERWISE SPECIFIED			THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART, WITHOUT THE WRITTEN CONSENT OF SILICON LABORATORIES, INC..			COMPANY:  400 W Cesar Chavez AUSTIN, TX 78701 (512)416-8500 www.silabs.com			
DIMENSIONS ARE IN INCHES AND APPLY AFTER FINISH DIMENSIONS IN BRACKETS [] ARE IN MILLIMETERS INTERPRET DRAWING PER MIL-D-1000			DESIGN CD 27MAR2015 LAYOUT CT 03APR2015			NAME: IST-A21			REV : 3.0
TOLERANCES HOLE TOLERANCES PER 78027						PART NUMBER:			
DECIMALS .XX +/- .XXX +/-	ANGLES +/-	SURFACES MICROINCHES	PART TO BE FREE OF BURRS			SCALE 1:1			FABRICATION DRAWING
BREAK EDGES MAX			BEND RADIUS MAX			BEND RELIEF MAX			SHEET 1 OF 1
DO NOT SCALE DRAWING									

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IST-A21 REV 3.0
Size:
Array: 7.9 x 3.0
Part: 1.85 x 3.0
Parts On Array:
4 Parts
Matrix:
4 x 1
Spacing:
0.0 x NA
Array Borders:
Left: 0.25 Right: 0.25
Top: 0.0 Bottom: 0.0

Notes:

Please add 4, 0.125" NP tooling holes located 0.125" from tab corners and 3, 40/120 fiduials to each side of array located 0.25" from tooling holes.