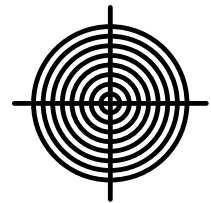
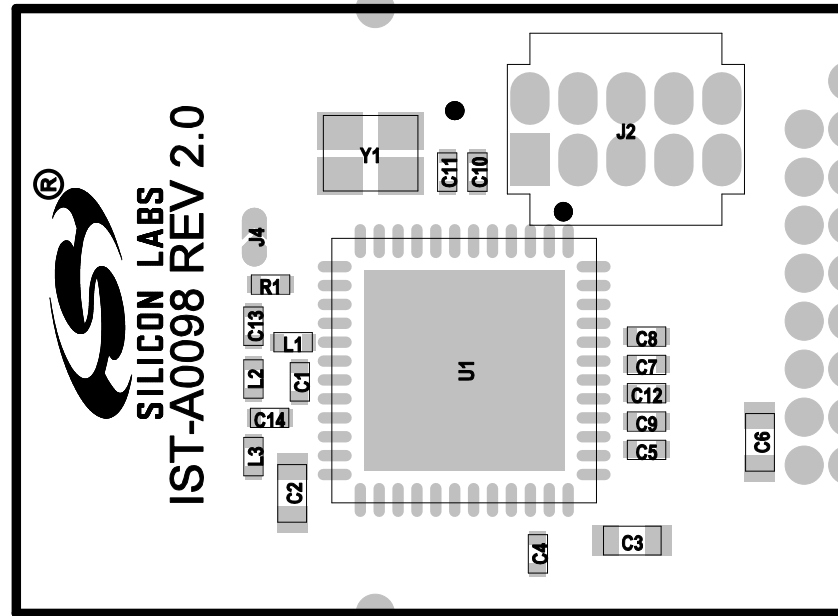
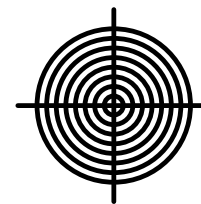
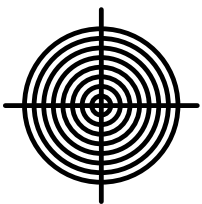
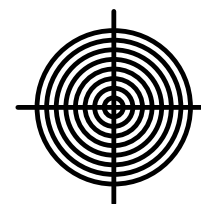
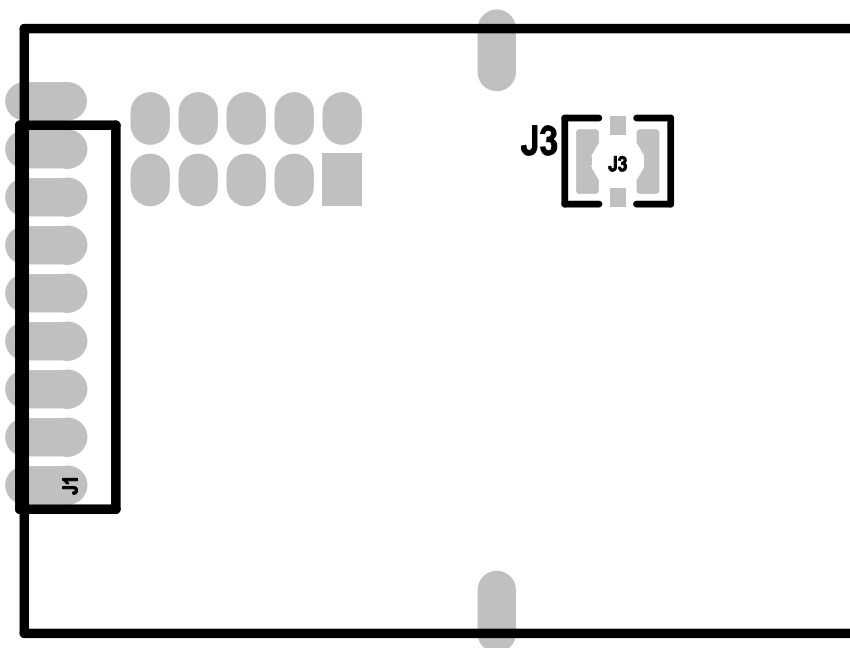


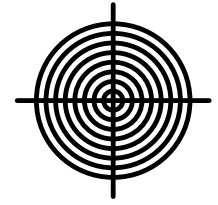
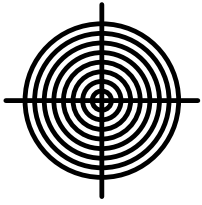
PRIMARY SILKSCREEN



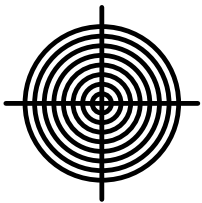
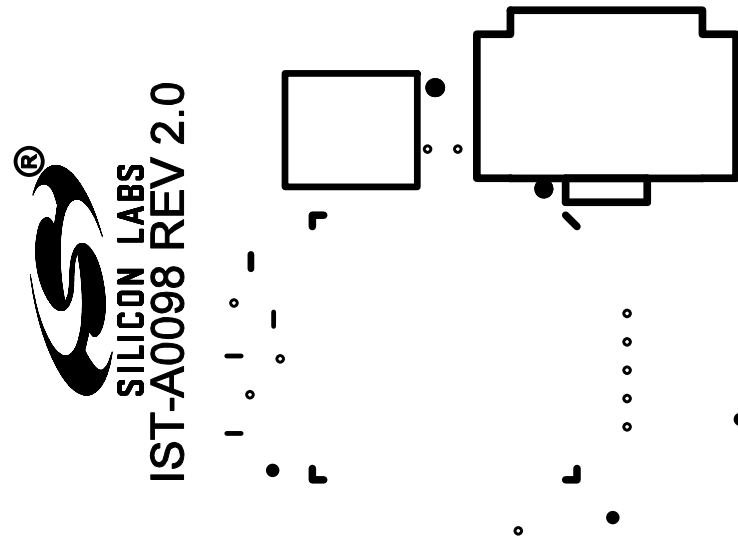


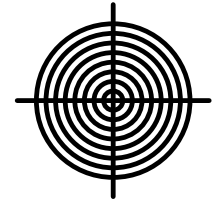
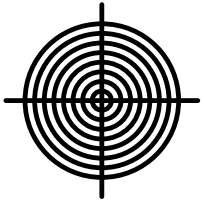
SECONDARY SILKSCREEN



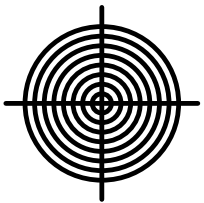
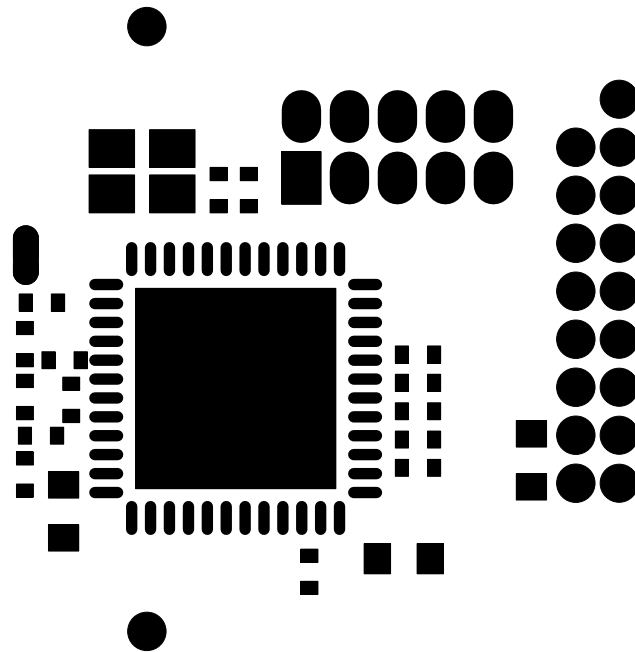


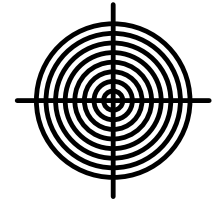
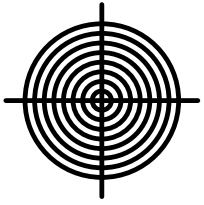
PRIMARY SILKSCREEN



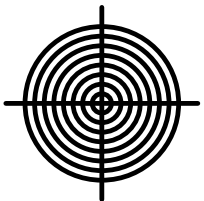
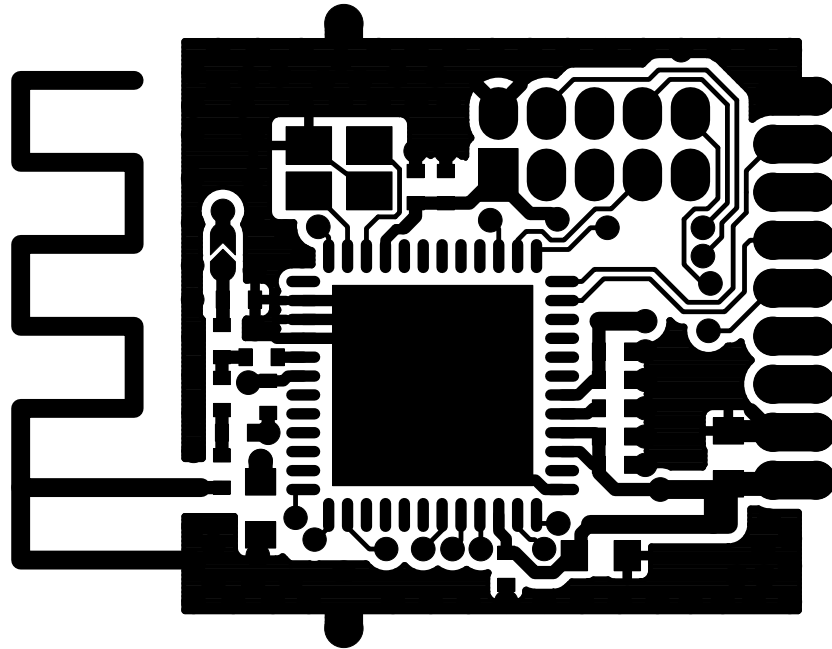


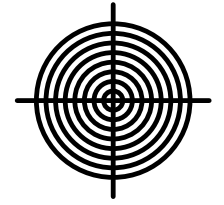
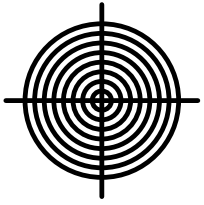
PRIMARY SOLDER MASK



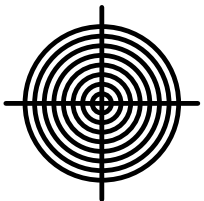
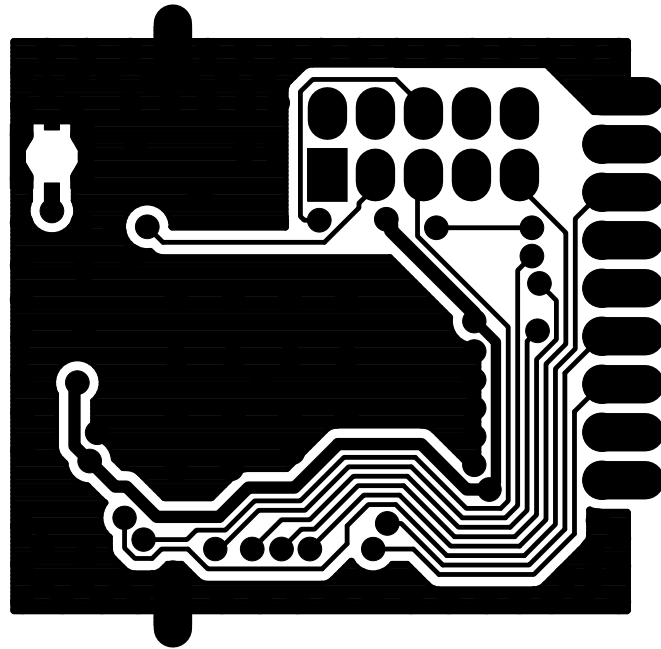


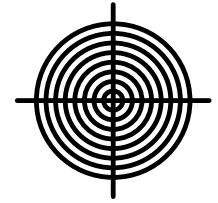
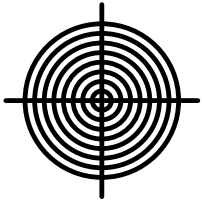
PRIMARY SIDE



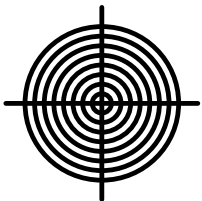
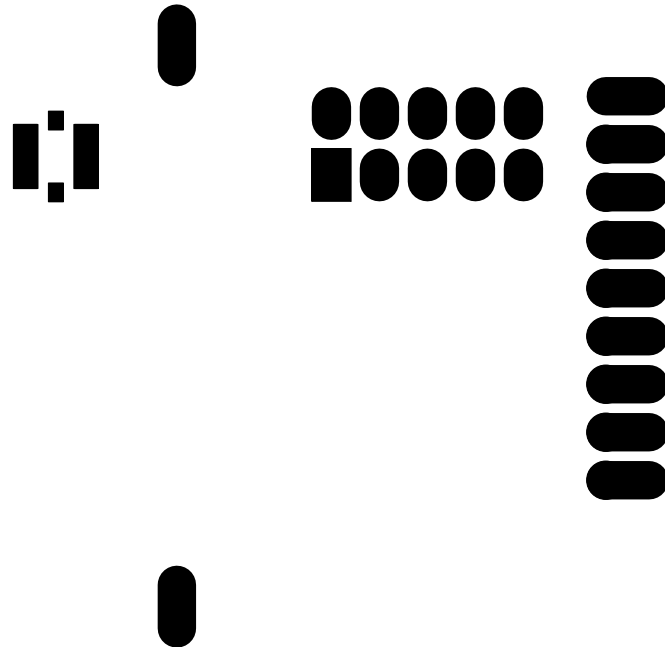


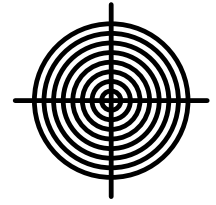
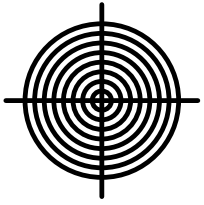
SECONDARY SIDE





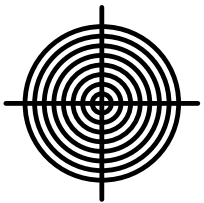
SECONDARY SOLDER MASK

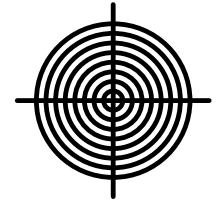
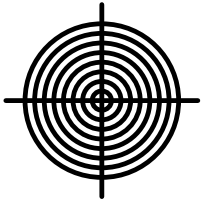




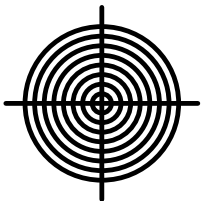
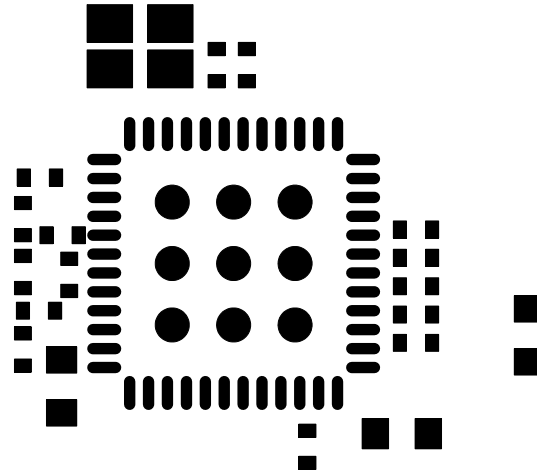
SECONDARY SILKSCREEN

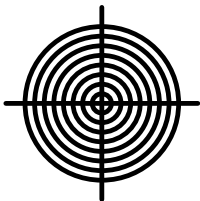
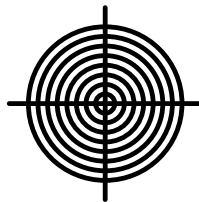
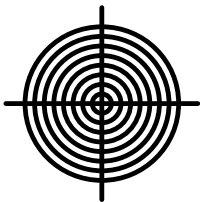
[]_{εL}

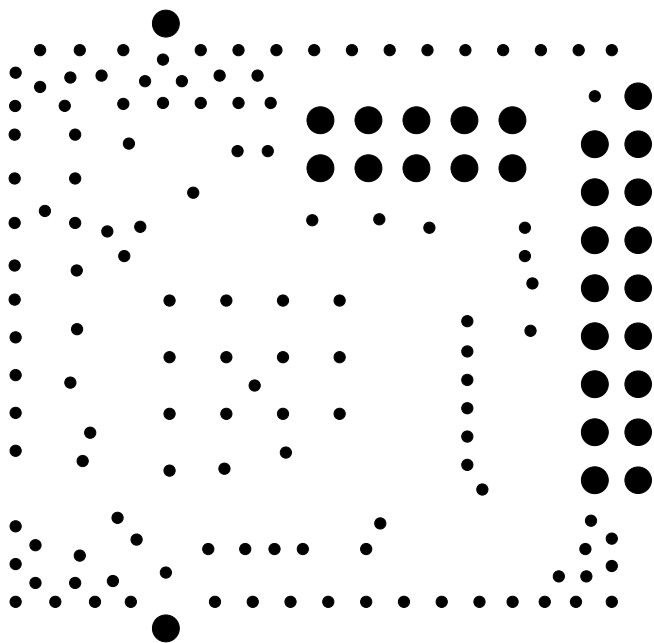




PRIMARY SOLDER PASTE

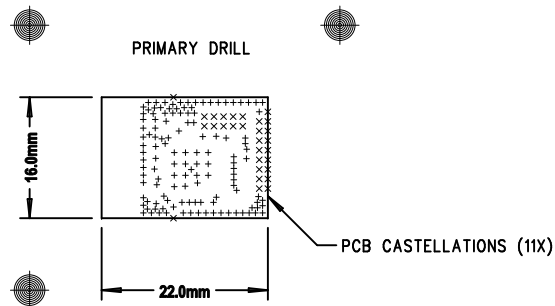






NOTES : UNLESS OTHERWISE SPECIFIED

1. MANUFACTURE IN ACCORDANCE WITH IPC-6012, TYPE 3, CLASS 2.
2. END PRODUCT FEATURES SHALL NOT VARY MORE THAN 20% FROM ARTWORK ORIGINALS.
3. LAMINATE AND PREPREG SHALL BE AS PER IPC-4101/26,83,98 WITH A DECOMPOSITION TEMPERATURE $\geq 345^{\circ}\text{C}$, COLOR, NATURAL.
4. COPPER WEIGHT SHALL BE 0.5 OZ./SQ. FT. BEFORE PLATING.
5. ALL PLATED THROUGH HOLES SHALL HAVE A MINIMUM OF 0.001" COPPER.
6. DRILL HOLE TOLERANCE AFTER PLATING SHALL BE ± 0.003 ".
7. MINIMUM ANNULAR RING SHALL BE 0.001".
8. MINIMUM ANNULAR RING AT EMERGENT CONDUCTORS SHALL BE 0.003".
9. FINAL PCB THICKNESS SHALL BE 0.031" $\pm 10\%$.
10. WARP/TWIST SHALL NOT EXCEED 1.0%.
11. FINISH SHALL BE LPI, BLACK SMOBC, BALANCE ENIG.
12. SILKSCREEN WITH NONCONDUCTIVE WHITE EPOXY INK.
13. REFERENCE ADDITIONAL FAB NOTES IN FILE README.TXT




LAYER STACKUP

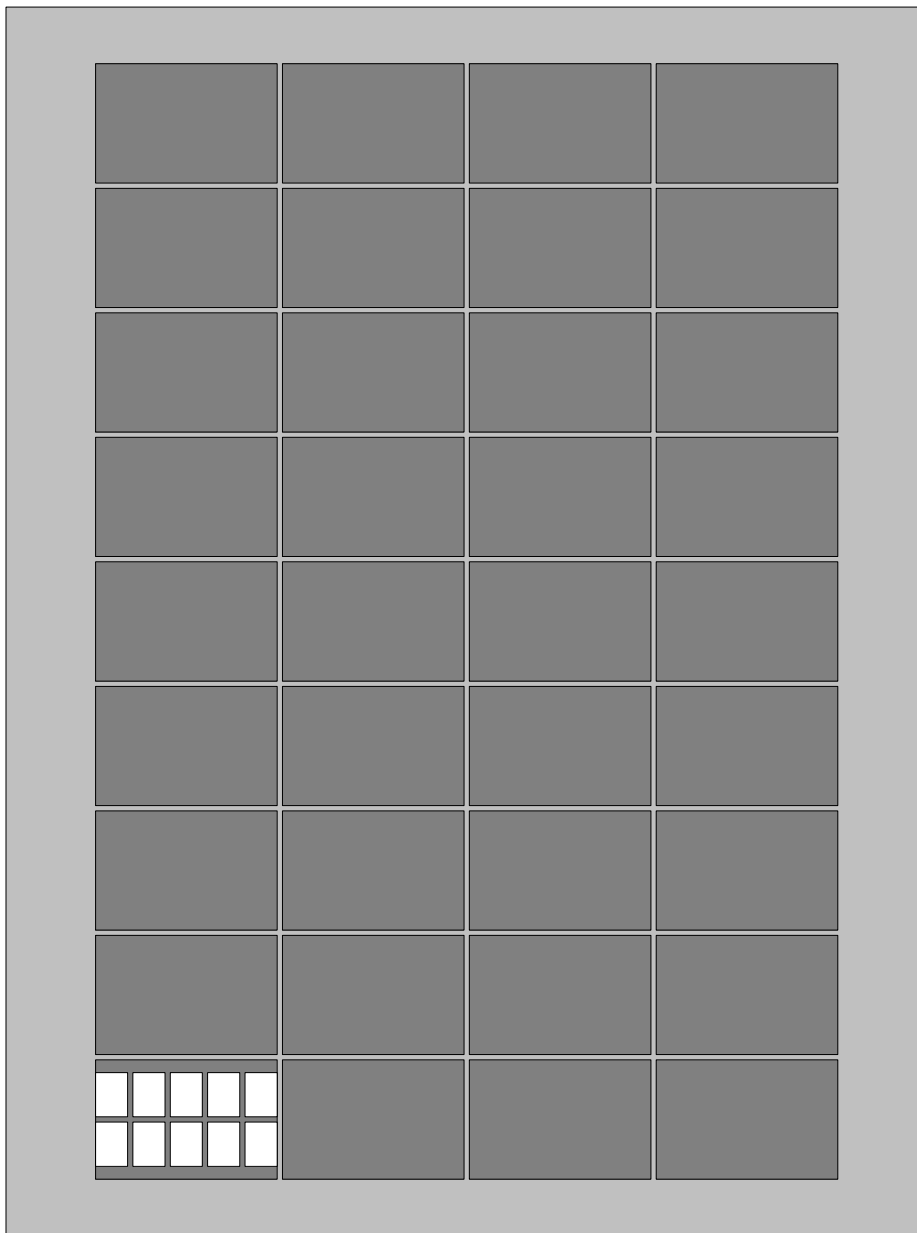
FILE NAMES

PRIMARY SILKSCREEN	A98_PSS.PHO
PRIMARY SOLDERMASK	A98_PSM.PHO
PRIMARY SIDE	A98_PRI.PHO
SECONDARY SIDE	A98_SEC.PHO
SECONDARY SOLDERMASK	A98_SSM.PHO
SECONDARY SILKSCREEN	A98_SSS.PHO

SCALE: NONE

SIZE	QTY	SYM	PLT	TOOL	TOL
0.300	125	+	P	1	+0/-0.300
0.710	29	X	P	2	+/-0.075

UNLESS OTHERWISE SPECIFIED			THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND SHALL NOT BE DUPLICATED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED IN WHOLE OR IN PART, WITHOUT THE WRITTEN CONSENT OF SILICON LABORATORIES, INC..			COMPANY:		 SILICON LABS 400 W Cesar Chavez AUSTIN, TX 78701 (512)416-8500 www.silabs.com		
DIMENSIONS ARE IN INCHES AND APPLY AFTER FINISH										
INTERPRET DRAWING PER MIL-D-1000										
TOLERANCES										
HOLE TOLERANCES PER 78027			NAME:			IST-A0098		REV : 2.0		
DECIMALS	ANGLES	SURFACES	DESIGN	YAS	16AUG2017	SIZE	PART NUMBER:			
.XX +/-			LAYOUT	CT	16AUG2017	A				
.XXX +/-	+/-	MICROINCHES								
PART TO BE FREE OF BURRS										
BREAK EDGES	BEND RADIUS	BEND RELIEF	DO NOT SCALE DRAWING							
MAX	MAX	MAX	SCALE 1:1		FABRICATION DRAWING			SHEET 1 OF 1		



IST-A0098 REV 2.0

Size:

Panel: 18.0 x 24.0

Array: 3.55 x 2.332

Part: 0.63 x 0.866

Panel Yield:

36 Arrays of 10 Parts

360 Parts Total

69.0% Material Utilization

Matrix:

On Panel: 4 x 9, Origin: X1.75 Y1.106

On Array: 5 x 2

Spacing:

On Panel: 0.1 x 0.1

On Array: 0.1 x 0.1

Panel Borders:

Left: 1.75 Right: 1.75

Top: 1.106 Bottom: 1.106

Array Borders:

Left: 0.0 Right: 0.0

Top: 0.25 Bottom: 0.25

Notes:

Please add 4, 0.125" NP tooling holes located 0.125" from tab corners and 3, 40/120 fiduials to each side of array located 0.25" from tooling holes.