UG384: WGM160P Hardware Design User’s Guide

The purpose of this guide is to help users design WiFi applications using the WGM160P.

This guide includes information for schematics and layout. Some options available with WGM160P hardware are not available with all software architectures, so the pin features versus software are detailed.

KEY FEATURES

- Schematic guidelines
- Package information
- Layout guidelines

Table of Contents

1. WGM160P Pinout

WGM160P is a 23.8 mm x 14.2 mm x 2.3 mm PCB module.

The diagram below describes pinout (top view)

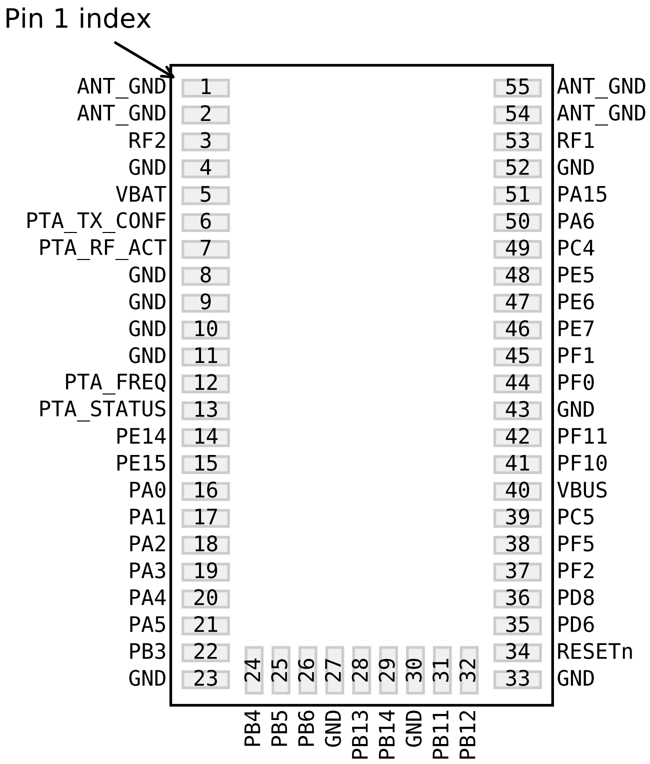


Figure 1.1. WGM160P Device Pinout

2. WGM160P Pin Description

2.1 Pin Table

Table 2.1. WGM160P Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
ANT_GND	1 2 54 55	Antenna ground.	RF2	3	External antenna connection for diversity antenna. Terminate to ground with 47-51 Ohms if not connected to an antenna.
GND	4 8 9 10 11 23 27 30 33 43 52	Ground. Connect all ground pins to ground plane.	VBAT	5	Module power supply
PTA_TX_CONF	6	PTA TX_CONF pin. These pins can be used to manage co-existence with another 2.4 GHz radio.	PTA_RF_ACT	7	PTA RF_ACT pin. These pins can be used to manage co-existence with another 2.4 GHz radio.
PTA_FREQ	12	PTA FREQ pin. These pins can be used to manage co-existence with another 2.4 GHz radio.	PTA_STATUS	13	PTA STATUS pin. These pins can be used to manage co-existence with another 2.4 GHz radio.
PE14	14	GPIO	PE15	15	GPIO
PA0	16	GPIO	PA1	17	GPIO
PA2	18	GPIO	PA3	19	GPIO
PA4	20	GPIO	PA5	21	GPIO
PB3	22	GPIO	PB4	24	GPIO
PB5	25	GPIO	PB6	26	GPIO
PB13	28	GPIO	PB14	29	GPIO
PB11	31	GPIO	PB12	32	GPIO
RESETn	34	Reset input, active low. This pin is internally pulled up to VBAT. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PD6	35	GPIO
PD8	36	GPIO	PF2	37	GPIO
PF5	38	GPIO	PC5	39	GPIO
VBUS	40	USB VBUS signal and auxiliary input to 5 V regulator. May be left disconnected if USB is unused.	PF10	41	GPIO (5V)
PF11	42	GPIO (5V)	PF0	44	GPIO (5V)
PF1	45	GPIO (5V)	PE7	46	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE6	47	GPIO	PE5	48	GPIO
PC4	49	GPIO	PA6	50	GPIO
PA15	51	GPIO	RF1	53	External antenna connection on WGM160P22N. Not connected on WGM160P22A.
Note: 1. GPIO with 5V tolerance are indicated by (5V).					

2.2 Power Pin

The WGM160P module is supplied through the VBAT pin. There is no need for external bypass capacitors as the ICs decoupling is performed within the module. Note that, although the VBAT supply is variable, the maximum TX output power can be achieved only when the supply is set to 3.3 V or higher.

Note that pin VBUS cannot be used to supply the module.

2.3 RESETn Pin

The WGM160P module is reset by driving the RESETn pin low. A weak internal pull-up resistor holds the RESETn pin high allowing it to be left unconnected if no external reset source is required.

Note that when WGM160P is not powered, RESETn must not be connected to an active supply through an external pull-up resistor as this could damage the device.

Note also that the WGM160P features Power On Reset to keep WGM160P in reset mode until VBAT is high enough. For more details, refer to the MCU EFM32GG11 reference manual.

2.4 RF Pins

The WGM160P module is available with two RF configurations.

Table 2.2. WGM160P RF Configuration

Part Numbers	RF1	RF2
WGM160PX22KGA2 WGM160P022KGA2	Internal antenna. Pin RF1 is not connected.	RF port
WGM160PX22KGN2 WGM160P022KGN2	RF port	RF port

RF ports are internally matched to 50 Ω. It is recommended to connect any unused RF port to ground through a 50 Ω resistor. Any of the RF ports can be used in a similar way. However, performance obtained on RF1 is slightly better, so it is preferable to use this one.

Only one RF port is active at a given time, but the module can also achieve antenna diversity if the application requires it. Port selection and antenna diversity enablement are achieved through software configuration.

2.5 Clocks

The WGM160P module is available with two clock configurations.

Table 2.3. WGM160P Low Power Clock Configuration

Part Numbers	Low Frequency Crystal
WGM160PX22KGA2 WGM160PX22KGN2	Internal 32.768 kHz crystal
WGM160P022KGA2 WGM160P022KGN2	No crystal

A 32.768 kHz clock source is required to enable the lowest power operation in WiFi power save modes. 32.768 kHz can be generated using either an internal Low Frequency RC oscillator or an internal crystal. As the frequency tolerance of this clock affects wake-up scheduling, power consumption in DTIM modes is optimized when using the WGM160P with an integrated 32.768 kHz crystal.

For WGM160P applications requiring Ethernet, a 50 MHz reference clock is required. This can be achieved either by connecting a 50 MHz external clock to module pin PB14 or by connecting a 50 MHz crystal oscillator between pins PB13 (HFXTAL_P) and PB14 (HFXTAL_N). For more details, refer to the MCU EFM32GG11 reference manual.

Table 2.4. WGM160P 50 MHz High-Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXO}	No clock doubling	4	—	50	MHz
		Clock doubler enabled	4	—	25	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO}	50 MHz crystal	—	—	50	Ω
		24 MHz crystal	—	—	150	Ω
		4 MHz crystal	—	—	180	Ω
Nominal on-chip tuning cap range[1]	C_{HFXO_T}	On each of HFXTAL_N and HFXTAL_P pins	8.7	—	51.7	pF
On-chip tuning capacitance step	SS_{HFXO}		—	0.084	—	pF
Startup time	t_{HFXO}	50 MHz crystal, ESR = 50 Ω, C_L = 8 pF	—	350	—	µs
		24 MHz crystal, ESR = 150 Ω, C_L = 6 pF	—	700	—	µs
		4 MHz crystal, ESR = 180 Ω, C_L = 18 pF	—	3	—	ms
Current consumption after startup	I_{HFXO}	50 MHz crystal	—	880	—	µA
		24 MHz crystal	—	420	—	µA
		4 MHz crystal	—	80	—	µA

Note:

1. The effective load capacitance seen by the crystal will be C_{HFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.

2.6 PTA Pins

If an RF transceiver using the same 2.4 GHz band (e.g. Bluetooth) is located next to WGM160P, a Packet Transfer Arbitration (PTA) interface can be used to avoid mutual interference. In this case, the PTA pins are connected to the other transceiver. The PTA interface is highly programmable and can use 1, 2, 3, or 4 pins upon configuration. PTA signal names can vary by manufacturer, so the table below shows their alternative names.

Table 2.5. WGM160P PTA Configuration

WGM160P Pin #	WGM160P Pin Name	Alternative Name
6	PTA_TX_CONF	GRANT
7	PTA_RF_ACT	REQUEST
13	PTA_STATUS	PRIORITY
12	PTA_FREQ	RHO

PTA interface configuration is achieved through software configuration. PTA operation will be detailed in an upcoming application note.

2.7 Multifunction Pins

The multifunction pins refer to the WGM160P pins directly connected to the embedded MCU, EFM32GG11.

2.7.1 Software Architecture Considerations

As described in the data sheet, the WGM160P module has considerable flexibility regarding the configuration of MCU pins, but not all software architectures support all functions.

2.7.1.1 Bootloader

All devices come preprogrammed with a UART bootloader. This bootloader resides in flash and can be erased if it is not needed. More information about the bootloader protocol and usage can be found in *AN0003: UART Bootloader*. Application notes can be found on the Silicon Labs website (www.silabs.com/32bit-appnotes) or within Simplicity Studio in the [**Documentation**] area.

WGM160P pin 44 (GG11 PF0) and pin 45 (GG11 PF1) provide the bootloader with TX and RX access, respectively.

2.7.1.2 Implementation with GG11 Open Software

Full flexibility can be achieved when using the source software based on the Full MAC driver provided by Silicon Labs. The configuration of multifunction pins is accomplished within Simplicity Studio similar to the software development for the EFM32GG11. For more details regarding these pins, refer to tables 6.2 and 6.3 of the WGM160P data sheet.

2.7.1.3 Implementation with Gecko OS

The following table provides details on the various multifunction pin features supported through Gecko OS 4.0. Features such as SPI slave and USB will be supported in future releases of the Gecko OS.

Table 2.6. WGM160P Multifunction Pin Configuration With GeckoOS

WGM160P Pin	GG11 Port	Default Function	GPIO[1] (GOS_GPIO_x)	UART[2] (GOS_UART_x)	SPI[3] (GOS_SPI_x)	I2C (GOS_I2C_x)	ADC (GOS_ADC_x)	PWM (GOS_PWM_x)	Ethernet (RMII)
14	PE14	GPIO	0				0	0	TXD1
15	PE15	GPIO	1				-	1	TXD0
16	PA0	SPI Master MOSI	2		SPI0 MOSI		6	2	TXEN
17	PA1	SPI Master MISO	3		SPI0 MISO		-	3	RXD1
18	PA2	SPI Master CLK	4		SPI0 CLK		10	4	RXD0
19	PA3	GPIO	5				-	5	REFCLK
20	PA4	GPIO	6				11	6	CRSDV
21	PA5	GPIO	7				-	7	RXER
22	PB3	Bulk sflash MOSI or [4] UART TX (logging)	8	UART1 TX	SPI1 MOSI		-	8	
24	PB4	Bulk sflash MISO or 4 UART RX (logging)	9	UART1 RX	SPI1 MISO		12	9	
25	PB5	UART RTS (Commands)	10	UART0 RTS			-	10	
26	PB6	UART CTS (Commands)	11	UART0 CTS			1	11	
28	PB13	GPIO	12				-	-	
29	PB14	GPIO	13				2	-	
31	PB11	I2C Master SDA	14			I2C0 SDA	-	12	
32	PB12	I2C Master SCL	15			I2C0 SCL	3	13	
35	PD6	Factory Reset[5] GPIO	16	UART1 CTS			4	14	
36	PD8	GPIO	17	UART1 RTS			-	15	
37	PF2	GPIO	18				5	16	

WGM160P Pin	GG11 Port	Default Function	GPIO[1] (GOS_GPIO_x)	UART[2] (GOS_UART_x)	SPI[3] (GOS_SPI_x)	I2C (GOS_I2C_x)	ADC (GOS_ADC_x)	PWM (GOS_PWM_x)	Ethernet (RMII)
38	PF5	GPIO	19				-	17	
39	PC5	GPIO	20				-	18	
41	PF10	USB DM	21				7	-	
42	PF11	USB DP	22				-	-	
46	PE7	UART TX (Commands)	23	UART0 TX			-	19	
47	PE6	UART RX (Commands)	24	UART0 RX			8	20	
48	PE5	GPIO	25				-	21	
49	PC4	Bulk sflash SCLK	26		SPI1 CLK		-	22	
50	PA6	GPIO	27				9	23	MDC
51	PA15	GPIO	28				-	24	MDIO

Note:

1. The prefix _x in GOS_GPIO_x is replaced with the numbers in the column: GOS_GPIO_1, GOS_GPIO_2, etc. SDK have all those symbols defined in header files.
2. All UART IO's are relevant to WGM160P, so when RX is used it means WGM160P receives, and TX means WGM160P transmits.
3. SPI can be configured as master or slave. At the moment, only SPI master is supported in Gecko OS. SPI slave is coming in a future release. SPI interface does not define fixed SPI_CS pin. CS is configurable and any unused GPIO can be used for this function.
4. PB3 and PB4 showing 2 default functions means that those pins can be assigned using Gecko OS command API (variables and command) to one of those functions. For example, "set bus.data_bus uart1" or "set system.bflash.port spi1". Once one of these variables is assigned, the other one will give an error that pins are already in use. UART (logging) is used to print Gecko OS log messages: https://docs.silabs.com/gecko-os/4/standard/latest/cmd/variables/bus#bus-log-bus
5. WGM160P PAD 35 is used as factory reset pin and resets all Gecko OS variables to defaults. Any of the spare GPIOs is expected to be configured as factory reset pin, default being GOS_GPIO_16. More about factory reset at https://docs.silabs.com/gecko-os/4/standard/latest/getting-started#performing-a-factory-reset.

3. Application Schematic Recommendations

3.1 Power Supply

The WGM160P consists of two main blocks, the microcontroller (EFM32GG11) and the Wi-Fi network co-processor (WF200). The microcontroller contains an internal dc-dc converter that powers both the microcontroller core and the WiFi chip with a lower supply voltage to reduce overall power consumption. All the internal supplies are connected together and supplied by module pin VBAT.

Care should be taken that the supply source is capable of supplying enough current for the load peaks of the power amplifier (which can go momentarily up to 200 mA), so it is recommended to select a regulator capable of supplying 300 mA. The peaks can be very fast, and the power supply for the module should be capable of reacting to load changes within 5 µs.

External high-frequency bypass capacitors are not needed because the module contains the required supply filter capacitors. However, care should be taken to prevent strong switching noise from being superimposed on the supply lines. Such noise can be generated, for example, by the onboard charge pump converters used in RS232 level shifters.

Note that there is a total of about 15 µF of low ESR ceramic capacitors inside the module connected directly on the supply input. When using external regulators to generate regulated supplies for the module, the stability of the regulator with the low ESR provided by these capacitors should be checked. Some low-drop linear regulators and some older switched mode regulators are not stable when ceramic output capacitors are used. The data sheet of the regulator typically lists recommendations concerning suitable capacitors, including data on ESR range and/or stability curves. A regulator should include the statement "stable with ceramic capacitors".

3.2 RF Part

When using the WGM160P with an antenna external to the module, be they connectorized off-the-shelf antennas or PCB trace antennas, antenna impedance must be well matched to 50 Ω, achieving better than -10 dB return loss throughout the 2.4-2.48 GHz band to reduce distortion in the module power amplifier due to impedance mismatch.

The matching should be verified in the final enclosure, and it is recommended to reserve SMD placeholders for external antenna tuning. The suggested external antenna matching structure is a 3-element PI network.

Unused RF ports (RF2 on both variants or RF1 on the variant without the chip antenna assembled) must be terminated to ground with a resistor of between 47 and 51 Ω.

4. Typical Application Schematics

The diagrams below show a simple application schematic with WGM160P and its internal antenna.

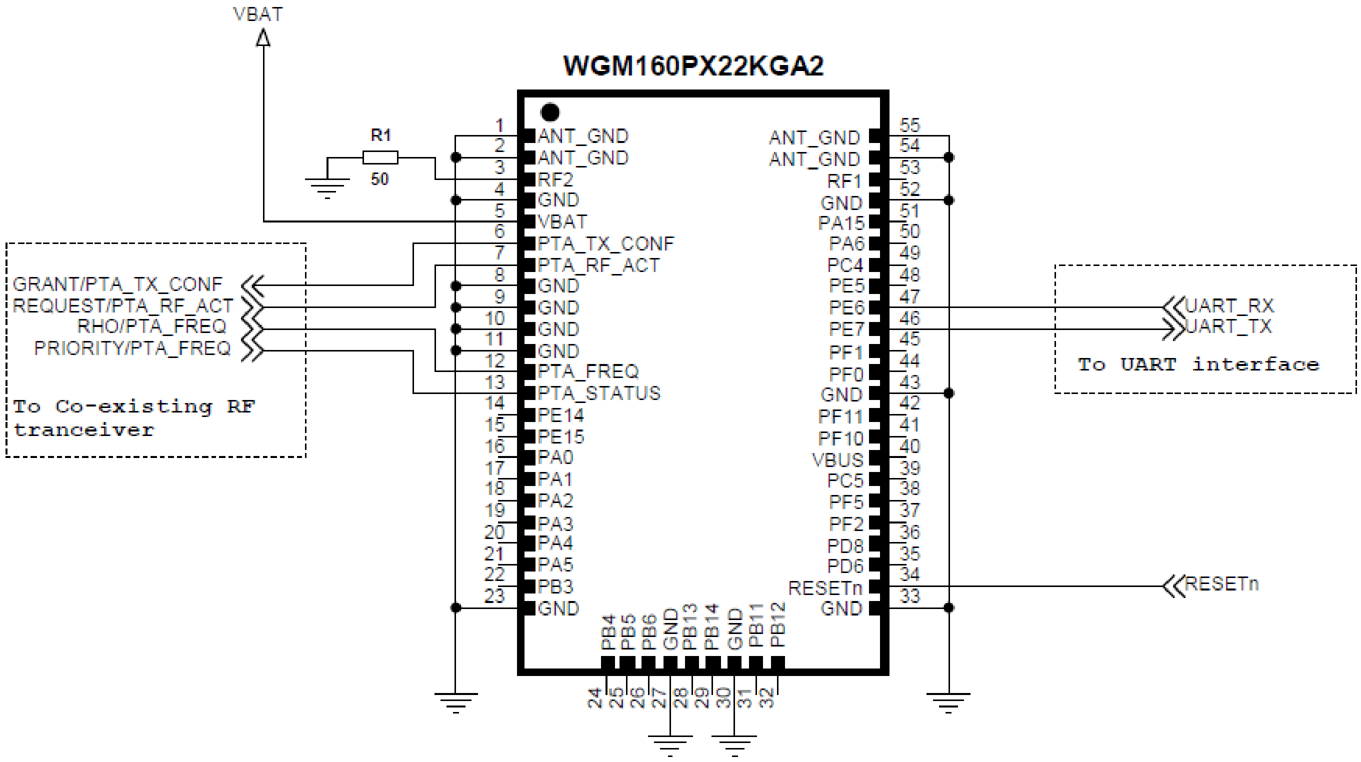


Figure 4.1. WFM160PX22KGA2 Schematics

5. Layout Recommendations

5.1 Generic RF Layout Considerations

For custom designs, use the same number of PCB layers as are present in the reference design whenever possible. Deviation from the reference PCB layer count can cause different PCB parasitic capacitances, which can detune the matching network from its optimal form. If a design with a different number of layers than the reference design is necessary, make sure that the distance between the top layer and the first inner layer is similar to that found in the reference design because this distance determines the parasitic capacitance value to ground. Otherwise, detuning of the matching network is possible, and fine tuning of the component values may be required. The Silicon Labs development kit uses a 1.6 mm thick FR4 PCB with the following board stack-up.

```
BOARD THICKNESS     : 1.6 mm +/-10%
NO OF LAYERS        : 4
MATERIAL(S)         : Glass Epoxy FR-4, NEMA Class 2, UL 94V-0, Tg min 150 C
                      Materials in compliance with the RoHS and WEEE directives
MARKINGS            : Logo, Week/Year, UL (ON SECONDARY SIDE (BOT))
                      (Avoid areas reserved for DataMatrix, Barcodes or Lables)
                      All PCB manufacturerÆs markings (Logo, Week/Year, UL)
                      shall be put in the PCB frame. No marking on the boards
                      is allowed
QUALITY REQ.        : IPC-A-600 (current revisions) Class 2, and IPC specifications
                      refered to by IPC-A-600
GENERAL REQ.        : - Copper must not be added or removed from inside the board
                        outline(s), without written consent/approval.
                      Use the balancing of the panel that comes with the
                      Gerber files (without alterations)
                      If applicable, the following requirements are valid:
                      - If Build-Up (Stack-Up) is specified, follow Build-Up,
                        otherwise use (board manufacturer) standard Build-Up.
                      - Break-away areas may be used for patterns, holes etc.
                        by manufacturer for QA purposes.
                      - If V-CUT, use angle 30 +/- 5 degrees.
                        V-CUT minimum remaining thickness 0.5 +/- 0.1 mm.
                        Use of V-CUT test pads is allowed.
                      - Inner radius (contour/outline) 1.2 mm, unless stated
                        otherwise.
COPPER THK.         : SEE BUILD-UP
COPPER PASSIV.      : ENIG to meet IPC-4552 requirements (current revision)
                      (Electroless Nickel/Immersion Gold)
RESIST MASK         : Solder Mask Color: BLACK (NB! NON-STANDARD)
                      Photo Polymer Wet film
                      to IPC-SM-840 Class T requirements (current revision)
                      Thickness minimum 8 um, maximum 20 um
VIA HOLES           : PLUGGED/FILLED, IPC-4761 (current revision) Type IV-b
                      Plugged and Covered Both Sides, Low CTE Plugging Paste
                      If Type IV-b is not available as a process, then Type IV-a
                      for the Top Side, and Overprinted (Tented) Bot Side is OK
LEGEND/SILKSCR.     : WHITE, BOTH SIDES (TOP + BOT)
CONTROLLED IMP      : Design has Controlled impedances. FOLLOW BUILD-UP STRICTLY!
                      Unless explicitly stated otherwise, controlled impedance
                      has been designed into the board. Use of test strip is
                      hence normally not required.
NOMINAL VALUES for Width, Spacing and VIA Diameter:
Cu TRACK(TRACE)     : Minimum conductor width      : 0.125 mm (5 mils)
Cu TRACK(TRACE)     : Minimum conductor spacing    : 0.125 mm (5 mils)
MINIMUM VIA         : Minimum via pad diameter     : 0.5 mm ( 20 mils)
                      Minimum via hole diameter    : 0.25 mm (10 mils)
                      Min via hole may have more than one pad diameter.

BUILD UP            :
                    L1  ==== | |========================= 38 um Cu (ca) After plating
                       ///// | |///////// PREPREG //////// 300 um *)
                    L2 ===== | |========================= 18 um Cu (0.5 Oz)
                       - - - | | - - - - - - CORE - - - - -  **)
                    L3 ===== | |========================= 18 um Cu (0.5 Oz)
                       ///// | |///////// PREPREG ////////
                    L4 ====  | |========================= 38 um Cu (ca) After plating

                    *)
                    The distance from bottom of L1 to top of L2 should be
                    as close to 300 um as possible!

                    **)
                    Select Core and Prepreg thickness in order to reach specified
                    board thickness


TEST                : 100% Electrical Test
                      Optical test, AOI (with automatic scanner)
                      Visual inspection
                      (Generate netlist from Gerber and Drill files)

                      Avoid use of 2125 Prepreg

                      If NB! is used in this specification, it means:
                      abbreviation for nota bene!, a Latin expression meaning
                      note well!


--------------------------------------------------------------------------------
NC DRILL - HOLE INFORMATION:
WARNING   : Drill dimensions must be taken from the Excellon (.DRL) file(s), and
            the drill report file(s) (.DRR).
            NON-PLATED holes may have a small center marker in the Gerber files.
            Under no circumstance must these Gerber flashes be mistaken for the
            hole drill dimensions!
The drill data may contain slots (in a separate file).
Dimensions for the finished board (after plating).
Tolerances +/- 0.1 mm, unless specified differently.
Via Holes +0.05 mm/-Via Size, unless specified differently.
```

Figure 5.1. Reference Design PCB Specification

Use as much continuous and unified ground plane metallization as possible, especially on the top and bottom layers.

Use as many ground stitching vias, especially near the GND pins, as possible to minimize series parasitic inductance between the ground pours of different layers and between the GND pins.

Use a series of GND stitching vias along the PCB edges and internal GND metal pouring edges. The maximum distance between the vias should be less than lambda/10 of the 10th harmonic (the typical distance between vias on a reference design is 1 mm). This distance is required to reduce the PCB radiation at higher harmonics caused by the fringing field of these edges.

For designs with more than two layers, it is recommended to put as many traces (even the digital traces) as possible in an inner layer and ensure large, continuous GND pours on the top and bottom layers, while keeping the GND pour metallization unbroken beneath the RF areas (between the antenna, matching network and module). To benefit from parasitic decoupling capacitance, the inner layer can be used to route the power supply with a wide VBAT sub-plane and traces to increase parasitic capacitance with nearby ground layers.

Avoid using long and/or thin transmission lines to connect the RF-related components. Otherwise, due to their distributed parasitic inductance, some detuning effects can occur. Also, shorten the interconnection lines as much as possible to reduce the parallel parasitic caps to the ground. However, couplings between neighbor discretes may increase in this way.

Route traces (especially the supply and digital lines) on inner layers for boards with more than two layers.

To achieve good RF ground on the layout, it is recommended to add large, continuous GND metallization on the top layer in the area of the RF section (at a minimum). Better performance may be obtained if this is applied to the entire PCB. To provide a good RF ground, the RF voltage potentials should be equal along the entire GND area as this helps maintain good VBAT filtering. Any gap on each PCB layer should ideally be filled with GND metal and the resulting sections on the top and bottom layers should be connected with as many vias as possible. The reason for not using vias on the entire GND section is due to layout restrictions, such as traces routed on other layers or components on the bottom side.

Use tapered lines between transmission lines with different widths (i.e., different impedances) to reduce internal reflections.

Avoid using loops and long wires to obviate their resonances. They also work well as unwanted radiators, especially at the harmonics.

Avoid routing GPIO lines close or beneath the RF lines, antenna or crystal, or in parallel with a crystal signal. Use the lowest slew rate possible on GPIO lines to decrease crosstalk to RF or crystal signals.

Use as many parallel grounding vias at the GND metal edges as possible, especially at the edge of the PCB and along the VBAT traces, to reduce their harmonic radiation caused by the fringing field.

Place any high-frequency (MHz-ranged) crystal as close to the module as possible. External crystal load capacitors are not needed since there is an on-chip capacitance bank for this purpose. Thus, it is suggested that one select crystals with load capacitance requirements that can be supported by the module. This way, the crystal can be placed close to the chip pins, and external capacitors are not needed. Connect the crystal case to the ground using many vias to avoid radiation of the ungrounded parts. Do not leave any metal unconnected and floating that may be an unwanted radiator. Avoid leading supply traces close or beneath the crystal or parallel with a crystal signal or clock trace. If possible, use an isolating ground metal between the crystal and any nearby supply traces to avoid any detuning effects on the crystal and to avoid the leakage of the crystal/clock signal and its harmonics to the supply lines. If possible, route traces between crystal and module pins as differential signals to minimize the trace loop area.

5.2 RF-Pads Including the Diversity Port and External Antennas

With WGM160P variants without a chip antenna, the important properties are mainly to ensure that WGM160P ground pads are well connected to the PCB ground plane in order to optimize thermal conductivity and prevent unwanted emissions due to ground currents.

The RF pads and RF traces conducting the RF signal should be dimensioned to have a characteristic impedance of 50 Ω. It is vital that proper RF design principles be used when designing an application using the RF pads.

Antennas external to the module, be they connectorized off-the-shelf antennas or PCB trace antennas, must be well-matched to 50 Ω.

PCB size and layout recommendations from the antenna manufacturer must be followed. Board size, ground plane size, plastic enclosures, metal shielding, and components in close proximity to the antenna can affect the antenna impedance and radiation pattern. Therefore, antenna matching should be verified in the final enclosure. Better than 10 dB return loss throughout the 2.4–2.48 GHz band is recommended to prevent distortion in the module power amplifier due to impedance mismatch. PA distortion can cause significant packet loss and poor overall performance.

5.3 Module Chip Antenna

As is common for very small antennas, the antenna on WGM160P uses the ground plane edge to radiate, rather than just the antenna chip itself. The antenna on WGM160P is robust to the detuning effect of the proximity of various objects and makes the module easy to use with a consistent and reliable performance. All the antenna needs is a small patch free from copper under the antenna end of the module and a solid ground plane covering the whole PCB on at least one layer, especially the edge of the application board where the antenna is placed. To prevent the RF signal coupling to other, sensitive parts of the design, it is recommended to have a solid, board-wide ground plane.

For optimal performance of the WGM160P Module, please follow these guidelines:

1. Place the Module at the edge of the PCB with the antenna end flush against the application board edge. If it is necessary to place the module some distance from the edge, limit the copper plane edges to the level of the module antenna end.
2. Place the module close to the center of the edge of the board.
3. Do not place any metal (traces, components, battery, etc.) within the clearance area of the antenna.
4. Connect all ground pads directly to a solid ground plane covering the whole PCB. The grounds closest to the antenna end conduct strong RF currents and are critical for good performance, while the rest of the ground pads are important for thermal conductivity.
5. Place multiple ground vias as close to the ground pads as possible. If possible, fill every unused area in all layers with ground-connected copper to improve thermal conductivity.
6. Terminate unused RF ports to ground with a resistor between 47 and 51 ohms

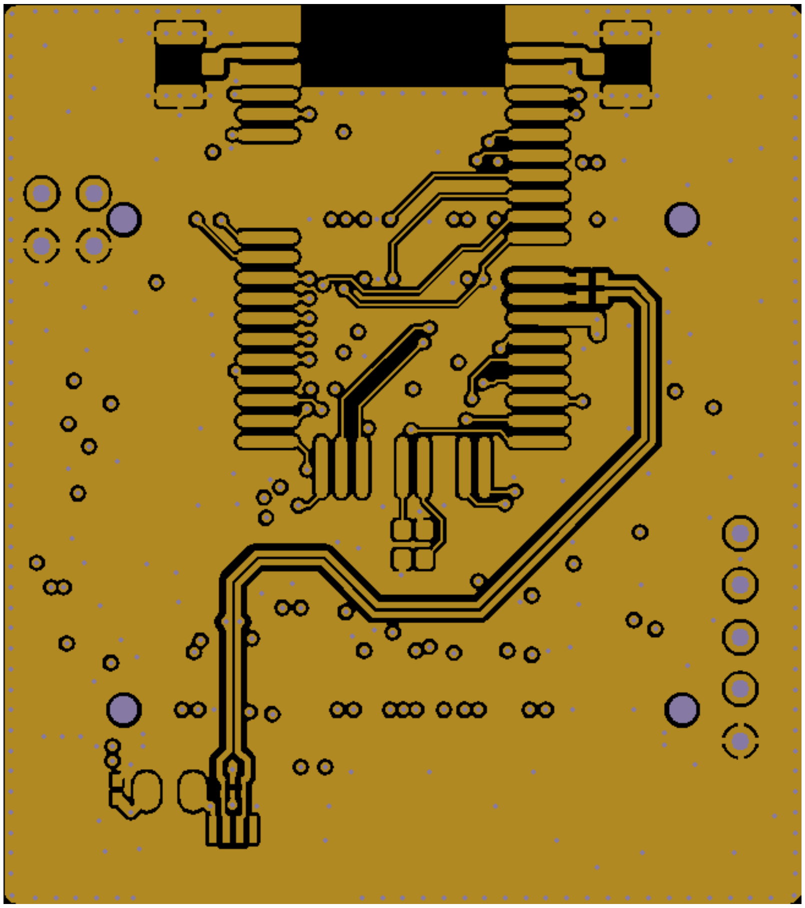


Figure 5.2. Top Layer Layout of WGM160P Reference Design

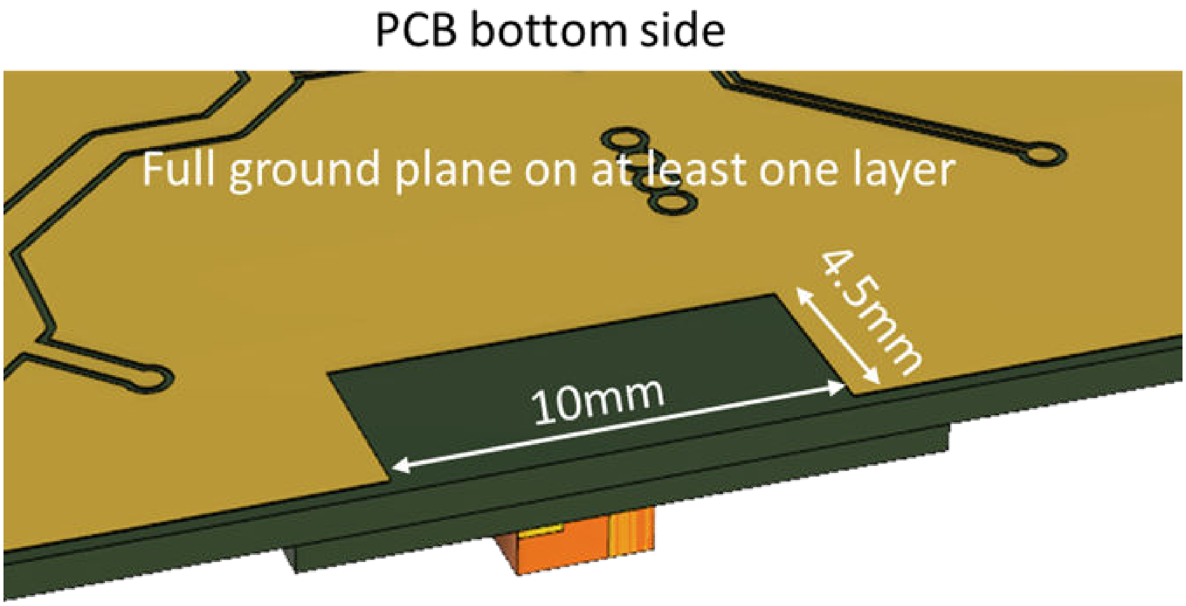


Figure 5.3. Details of Antenna Ground Clearance

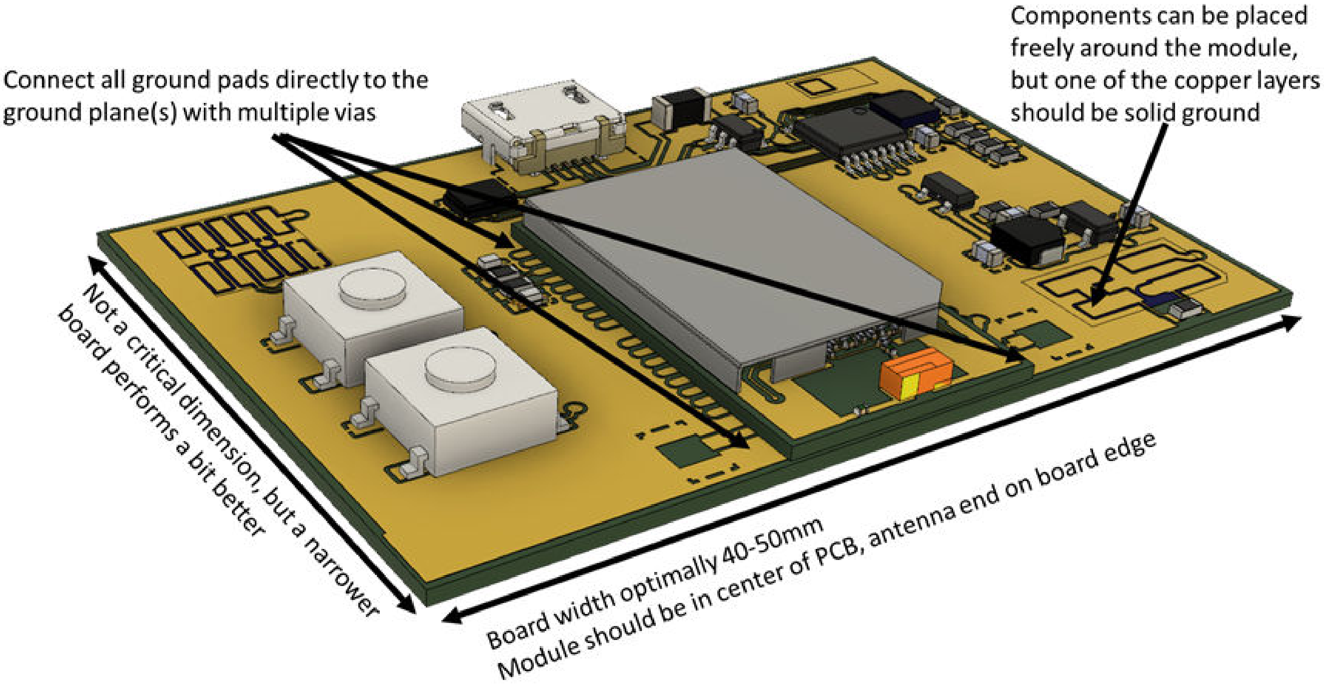


Figure 5.4. Details about Board Dimensions and Module Placement

Any metallic objects in close proximity to the antenna will distort the antenna's electromagnetic fields and cause the antenna center frequency to shift, reducing performance. The minimum recommended distance of metallic and/or conductive objects is 10 mm in any direction from the antenna, except in the directions of the application PCB ground planes. Please note that even if nearby metallic objects do not shift the antenna's center frequency, they will still distort the radiation pattern and prevent the antenna from radiating freely. Metals are opaque to radio frequencies and may create the equivalent of a shadow, a region of weaker performance, in the direction covered by the metal.

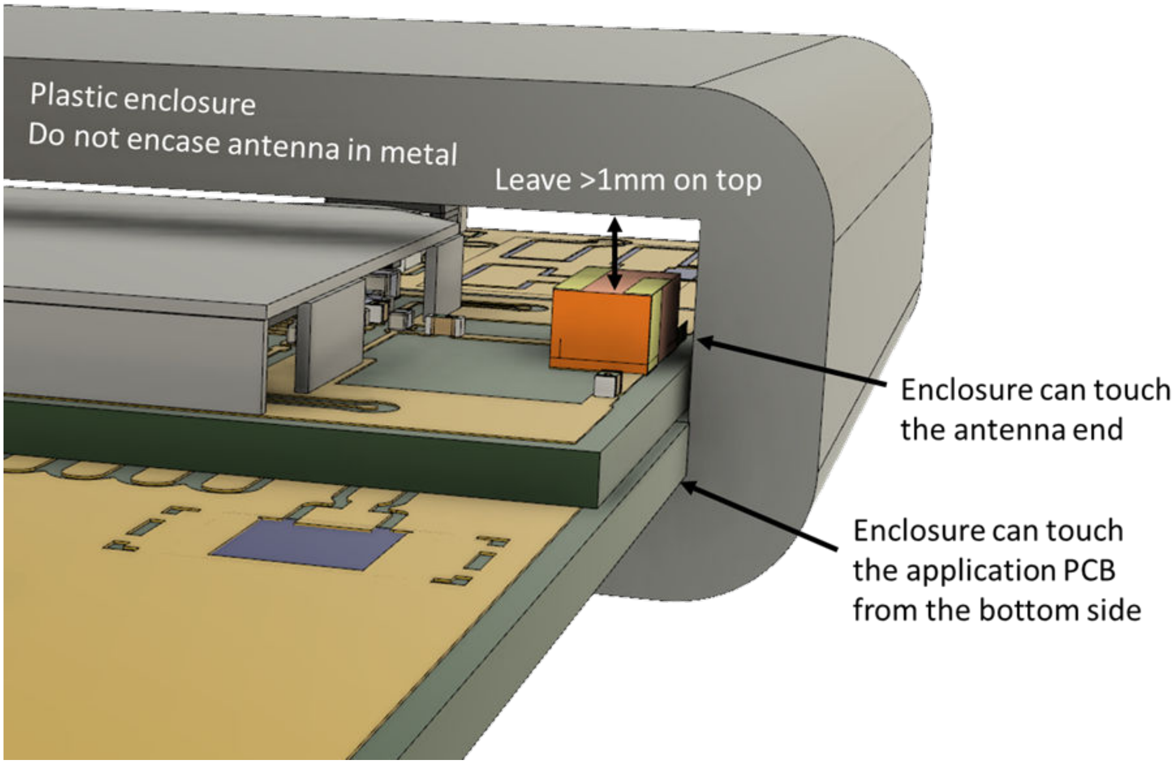


Figure 5.5. Enclosure Clearance Recommendations

Because the application board is part of the antenna circuit, its dimensions affect the antenna's efficiency and thus its achievable range. Narrower ground planes can be used but will result in compromised RF performance.

The following two-dimensional radiation pattern plots have been measured on the BRD4321A board:

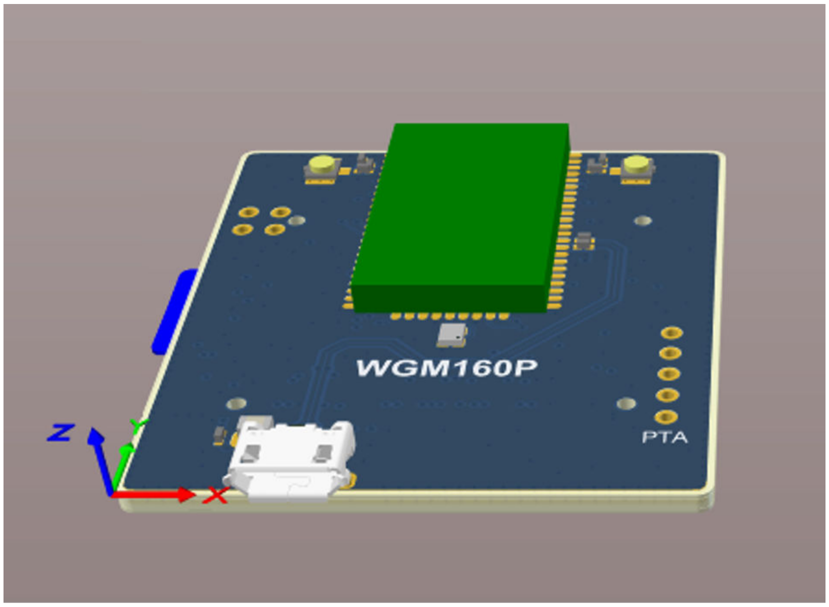


Figure 5.6. WGM160P Radio Board BRD4321A with XYZ Axis Added

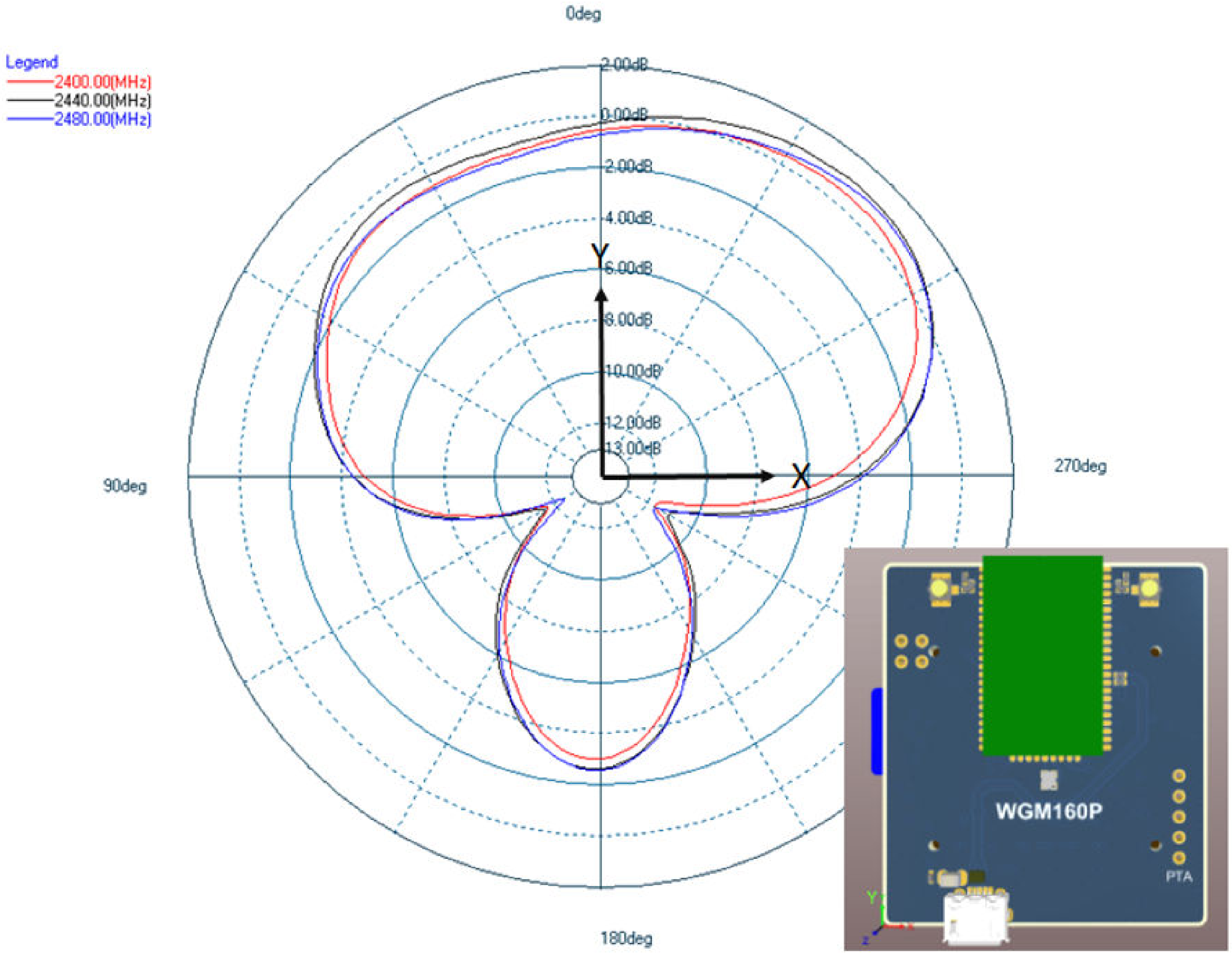


Figure 5.7. Typical 2D Radiation Pattern—Top View

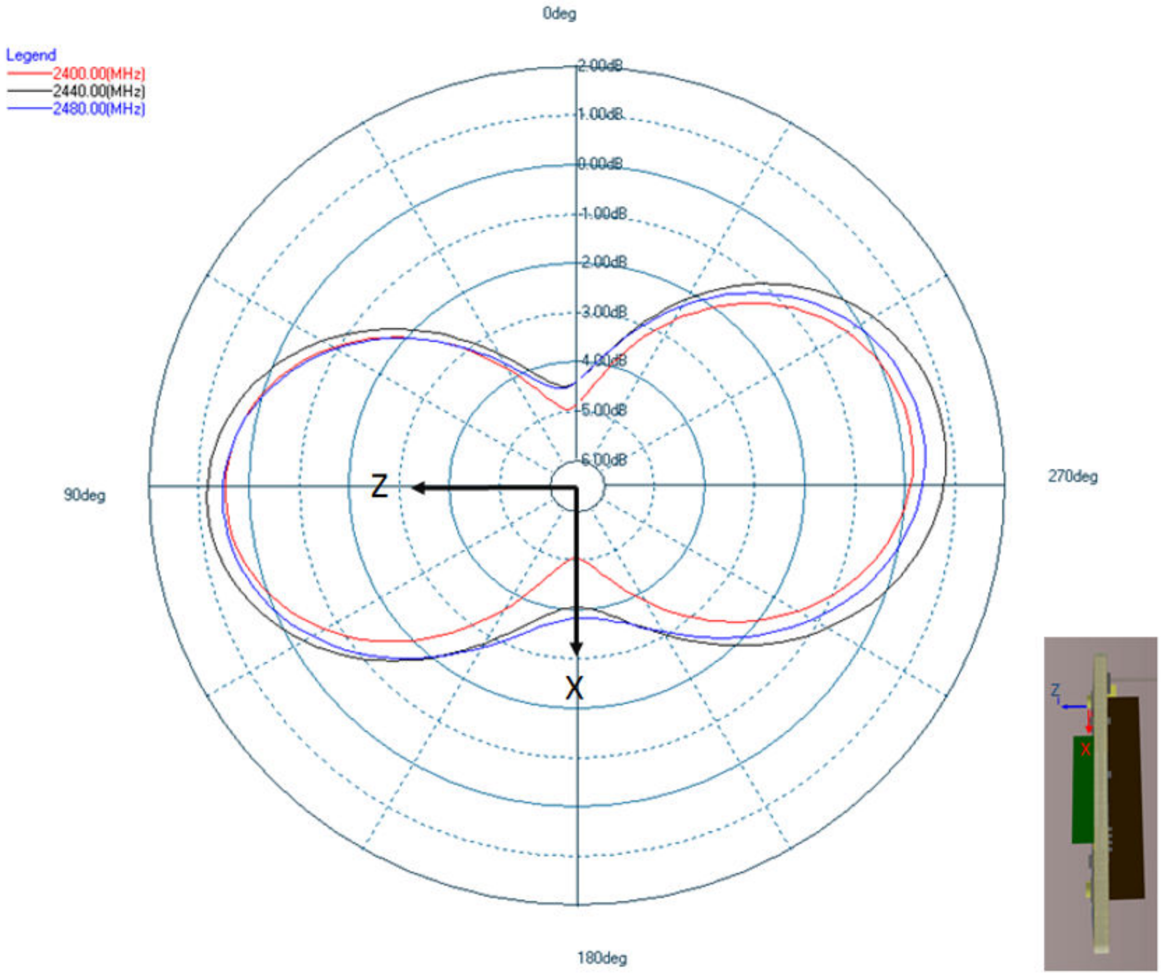


Figure 5.8. Typical 2D Radiation Pattern—Front View

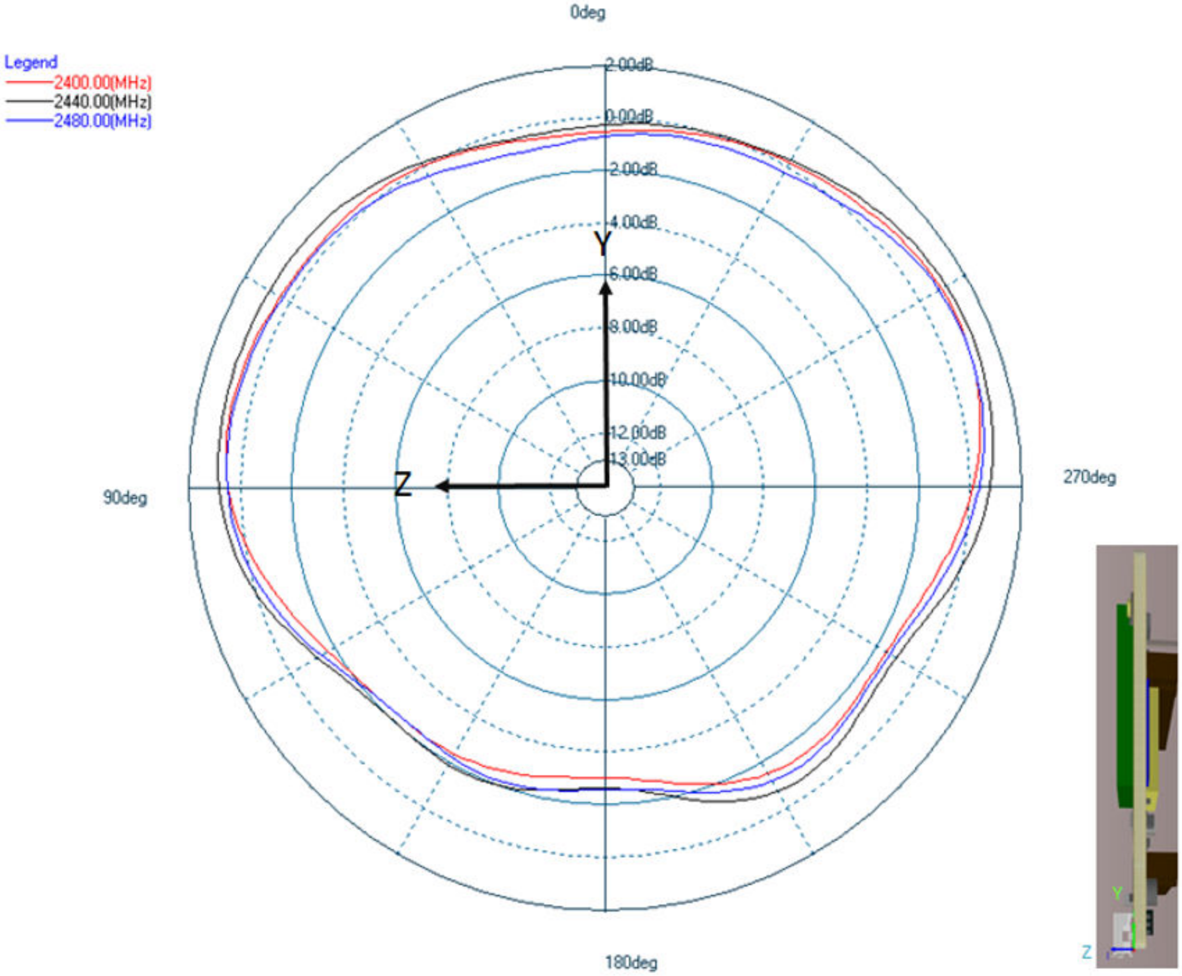


Figure 5.9. Typical 2D Radiation Pattern—Side View

6. Recommendations for Certification

Customers should refer to the datasheet for detailed recommendations about certification.

7. Package Outline

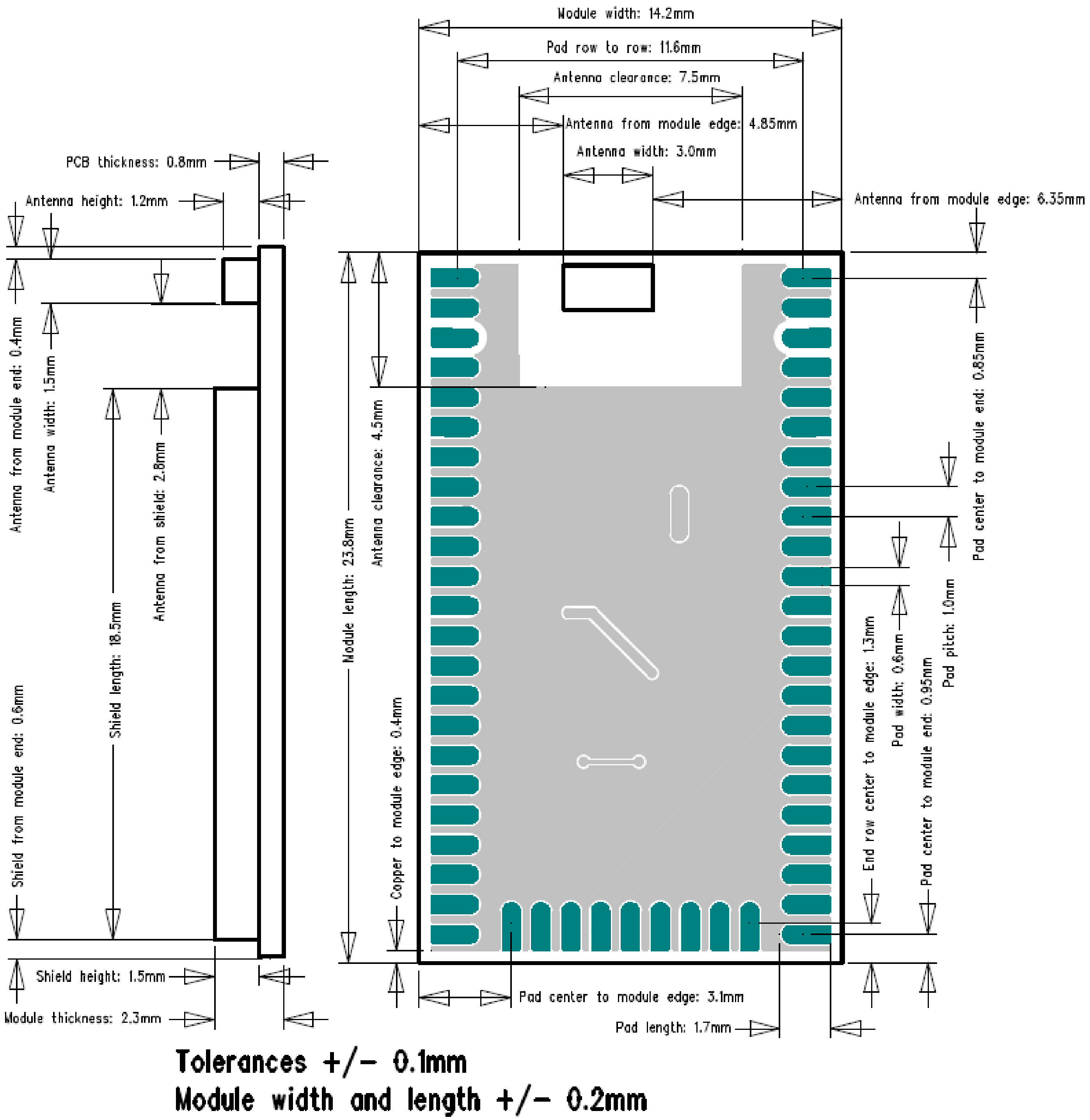


Figure 7.1. WGM160PX22KGA2 Package Outline

8. Recommended PCB Land Pattern

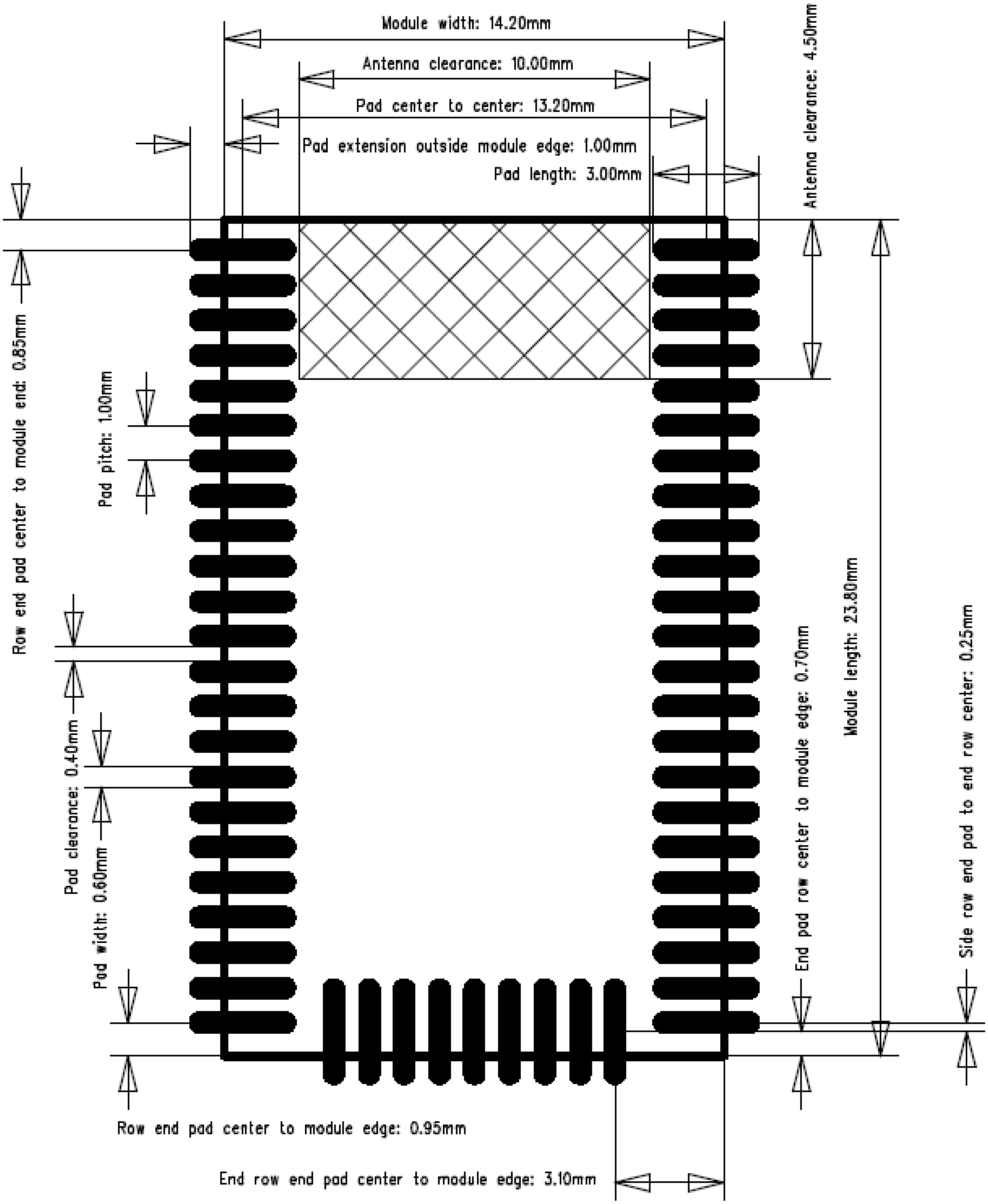


Figure 8.1. WGM160PX22KGA2/ WGM160P022KGA2 Recommended Land Footprint

For WGM160P modules without antenna, there is no need for PCB antenna clearance.

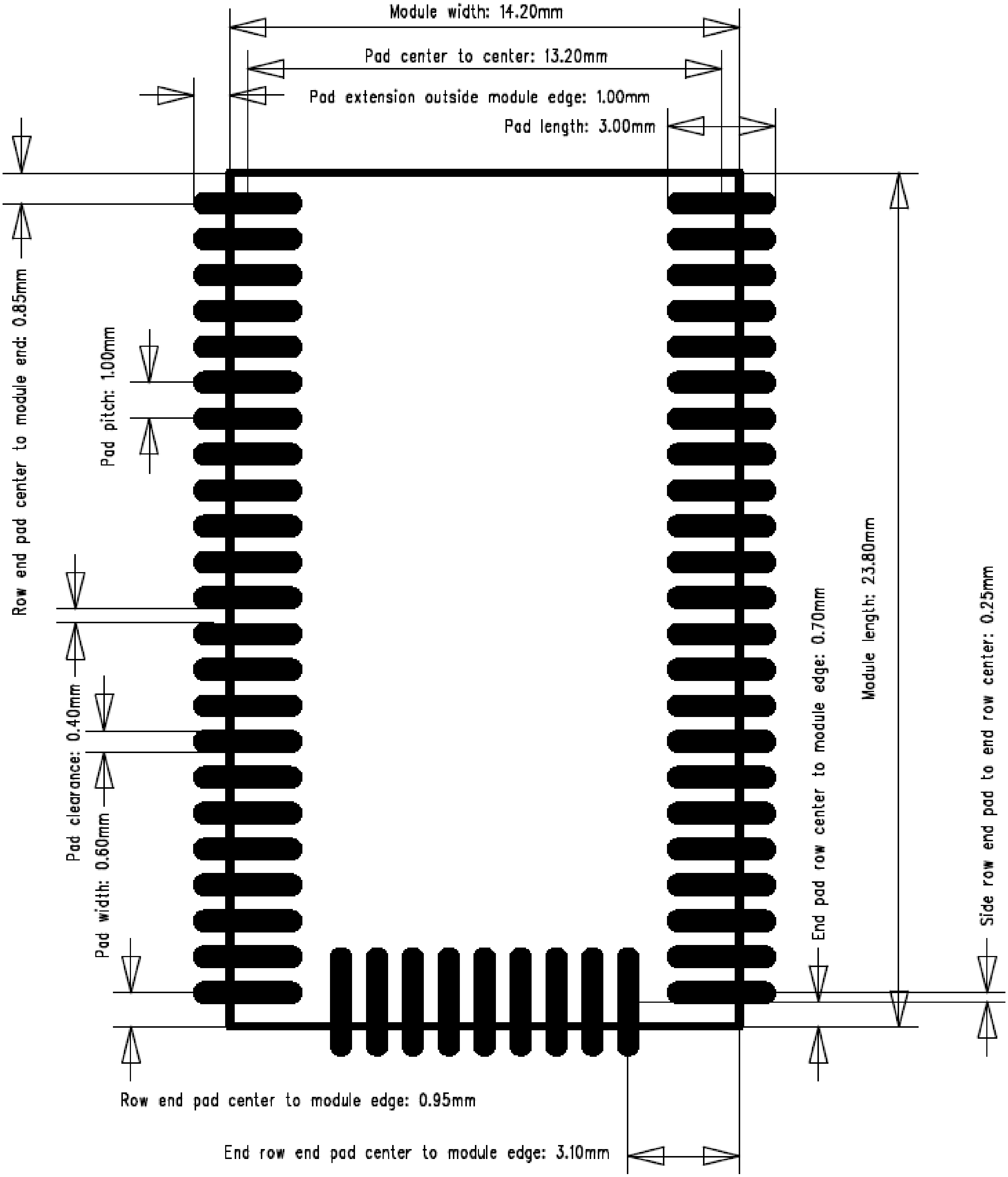
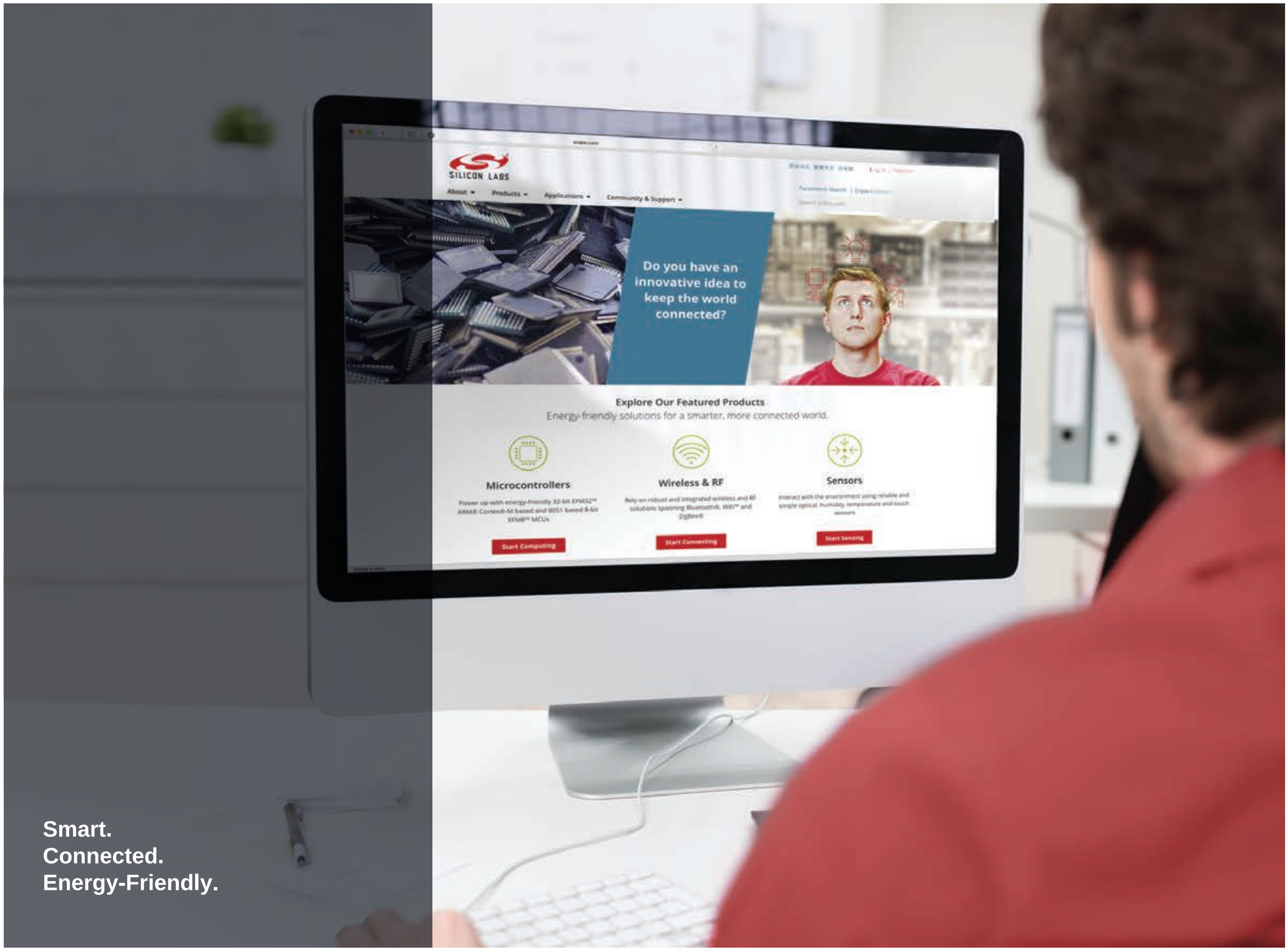


Figure 8.2. WGM160PX22KGN2/ WGM160P022KGN2 Recommended Land Footprint



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