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Backup Power Domain

AN0041 - Application Note

This application note describes how to use the EFM32 Backup Power Domain and Backup Real Time Counter. Included software examples demonstrate how to configure and use these features for time-keeping while running on backup power.

This application note includes:

- This PDF document
- Source files (zip)
  - Example C code
  - Multiple IDE projects

ARM ZERO TINY GECKO LEOPARD GIANT WONDER

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1 Backup Mode

1.1 Introduction

Some EFM32 devices feature the possibility to be powered by a backup/reserve power source. If a main power brownout should occur, the MCU can switch to a backup power source that can power 512 bytes of retention memory and a Backup Real-Time Counter (BURTC).

Backup Mode is a low energy mode equivalent to Energy Mode 4 (EM4), except that power is sourced from a backup power supply.

This Application Note includes software examples which shows how Backup Mode can be used to keep track of time during an MCU main power shut-down on a Giant Gecko Development Kit (EFM32GG-DK3750) and a Giant Gecko Starter Kit (EFM32GG-STK3750). All source files are included.

2 Backup Power Domain

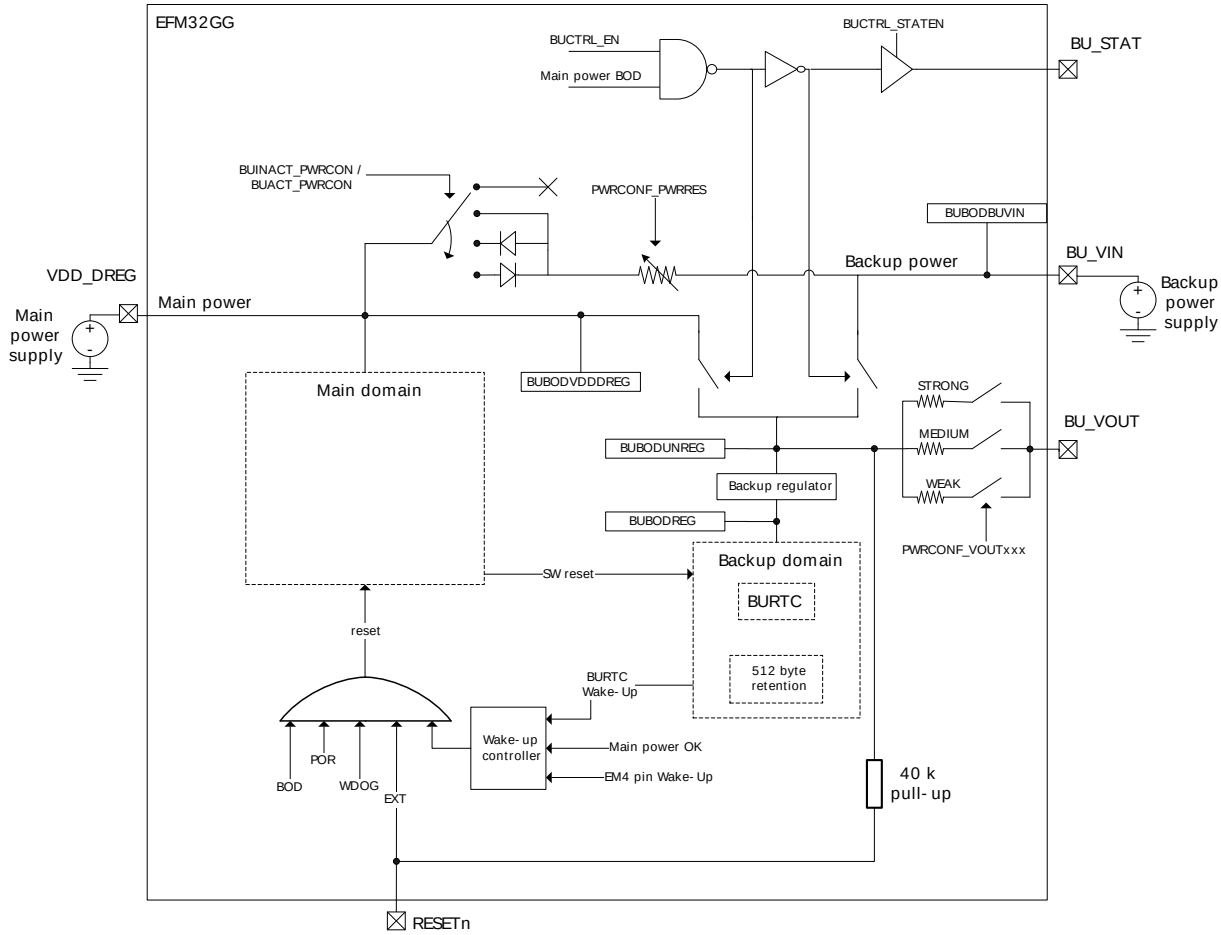
2.1 Overview

During normal operation, the CPU core and the digital peripherals are powered by the main power supply, VDD_DREG. Chip voltages are continuously monitored by several brownout detectors (BOD) that will trigger if the input voltage level is below a specified threshold.

In normal operation a voltage drop on VDD will trigger the main BOD which then will trigger a system reset. The power-on reset circuitry will hold the MCU in reset until main power reaches a voltage level that enables safe operation. When backup mode is enabled, four additional backup BODs are enabled. Now a similar voltage drop on VDD will trigger the backup brownout detector (BUBODVDDDREG) before the main BOD. This trigger will cause the MCU to go into backup mode, and source the backup power domain from a secondary power supply connected to the BU_VIN pin(Figure 2.1 (p. 3)).

Note that RESETn is pulled towards BU_VIN when the device is in backup mode. This means that one should take care if connecting the RESETn pin to any external circuitry.

Figure 2.1. Backup power domain overview



Backup mode is in practice the same as Energy Mode 4 (EM4). The difference being that the MCU is powered from the backup power pin (BU_VIN). This means that features available in backup mode is the same as in EM4, and that functionality that is used in backup mode must be configured to be enabled in EM4.

The backup real-time counter can be clocked by one of three clock sources. Which clock source is used will affect current consumption in backup mode. If current consumption is the prime concern, the

ULFRCO at 1 or 2 kHz should be used. The ULFRCO is, however, not very precise. The internal LFRCO offers better precision, but for time-keeping purposes, the LFXO which requires an external crystal should be used.

The backup mode features, such as the BURTC and retention RAM, can also be used in EM4 without utilizing a backup power source. This enables the MCU to be put in a state with very low current consumption while still being able to keep the system clock or to wake on a timer.

2.2 Configuration

This is a quick overview of the necessary settings for the backup functionality to work. For further details, please consult the reference manual.

- The first step in configuring the Backup Domain is to set the enable (EN) bit in the Backup Power configuration register (EMU_BUCTRL).
- To use a backup power source, the backup in (BU_VIN) pin must be enabled by setting the BUVINPEN bit in EMU_ROUTE.
- Memory retention and the backup real time counter requires voltage regulators to be enabled in backup mode. Enable the VREGEN bit in EMU_EM4CONF.
- If another oscillator than ULFRCO should be enabled in EM4, configure this by setting the bit field EMU_EM4CONF_OSC accordingly.
- Optionally, the backup mode status pin (BU_STAT) can be enabled by setting the STATEN bit in EMU_BUCTRL. During normal operation, this pin is low. In backup mode, it is pulled up to the backup voltage.
- Before backup mode is ready, the backup domain brown out detectors must warm up. Wait until the backup mode ready (BURDY) flag in EMU_STATUS is set.
- Finally, to prevent these settings to be overwritten during power on, set the configuration lock (LOCKCONF) bit in EMU_EM4CONF.

In the software example these steps are done in the *BUD_setup()* function.

2.2.1 Power Routing

The main power domain and the backup power domain can be connected through the MCU, either with a direct connection or through a diode. This can be used to charge a backup voltage source from the main voltage source. This connection is controlled by the PWRCON bit field in the EMU_BUACT and EMU_BUINACT registers so the setting can be different from normal operation to backup mode.

As shown in Figure 2.1 (p. 3) PWRCON can be set in four ways:

- NONE: No connection
- NODIODE: Direct connection
- BUMAIN: Diode allows current flow towards main power source
- MAINBU: Diode allows current flow towards backup power source

There should not be current flowing from the backup voltage source to the main voltage source when the device is in backup mode, as this may cause the device to get stuck in a loop going in and out of backup mode. This happens when the backup voltage is exposed to the main BOD, which will be misinterpret it as main power is restored. When the device tries to recover from backup mode the connection between the main BOD and the backup voltage source is broken and the device will go back to backup mode and so forth. To prevent this, avoid setting BUACT_PWRCON to BUMAIN or NODIODE.

Under certain circumstances, a device can be stuck in backup mode in a way that it will not start up when main power is restored. To prevent this, BUACT_PWRCON should be set to MAINBU. On Wonder Gecko devices, setting BUMODEBODEN in EMU_BUCTRL will also prevent this from happening.

To limit the output current there is a configurable series resistor between the two power domains. The PWRRES bit field in EMU_PWRCONF selects one of four discrete values. The resistor configuration is the same for backup mode and for normal operation.

2.2.2 Backup Voltage Output

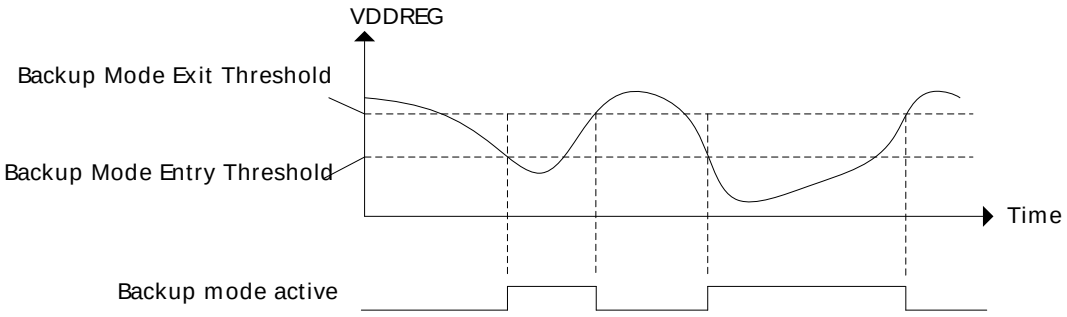
To enable external devices to operate in backup mode, the MCU can be configured to output the backup voltage on the BU_VOUT pin, and effectively extend the backup power domain outside the MCU. This will allow external devices to be powered from the backup source during a main power drop out, and using the same mechanisms to configure the power source.

2.3 Brownout Detectors

The backup functionality uses four brownout detectors to monitor voltage levels at different locations in the MCU, see Figure 2.1 (p. 3) .

The main power backup brownout detector, BUBODVDDDREG, senses on VDD after the internal voltage regulator. This BOD controls when to enter and exit backup mode. There is an amount of hysteresis implemented, as this BOD uses two different threshold levels. In normal mode it uses the Backup Mode Entry Threshold to determine when to enter backup mode. While in backup mode the Backup Mode Exit Threshold is used to decide when to resume normal operation.

Figure 2.2. Brownout detector thresholds



The BOD on the backup power pin, BUBODBUVIN, is used to prevent an entry to backup mode when the backup voltage is too low. If this BOD is triggered, the MCU will not enter backup mode on a voltage drop on main power, even if backup mode is configured.

BUBODUNREG and BUBODREG are located on respectively the unregulated and the regulated power domain internally on the MCU. A trigger on one of these BODs will just set the corresponding flag in RMU_RSTCAUSE.

All BOD trigger events will set the corresponding bit in RMU_RSTCAUSE. RSTCAUSE is not cleared at power up and can be used to determine if the MCU is resuming from backup mode. Thus, it is important that this register is cleared at start-up.

2.3.1 Brownout Levels

The thresholds for the backup brownout detectors are calibrated during production tests. Most important are the enter and exit thresholds on main power (BUBODVDDDREG), and the sensing on backup power (BUBODBUVIN). The factory calibrated thresholds are:

- Backup mode entry threshold: 2.10 V

- Backup mode exit threshold: 1.95 V
- BUBODBUVIN threshold: 1.90 V

3 Backup Real Time Counter

3.1 Overview

The Backup Real Time Counter (BURTC) is a real time counter that is available in all energy modes including backup mode. To facilitate this counter, the MCU keeps one oscillator available into Energy Mode 4 and in backup mode. By default this is the ULFRCO, but for higher precision BURTC can also be clocked by either the LFRCO or LFXO down to EM4.

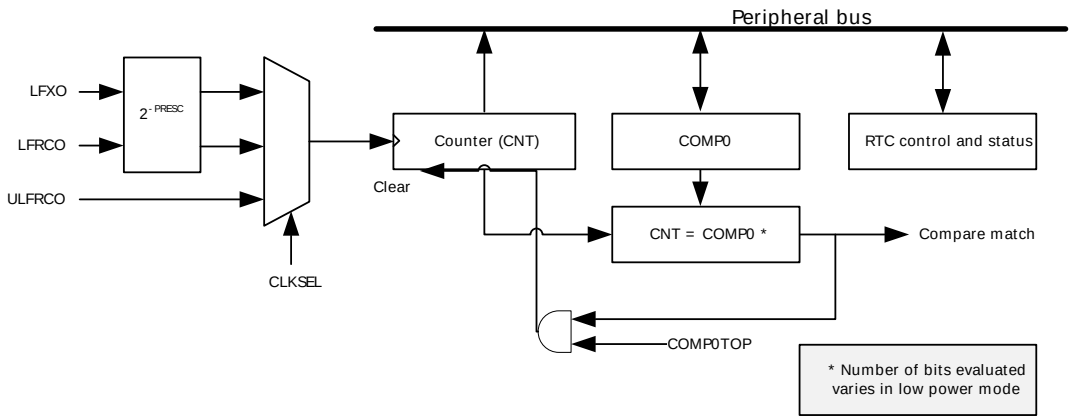
The backup real time counter has a time-stamp feature. On transition to backup mode, the BURTC value is automatically written to the BURTC_TIMESTAMP register.

The BURTC has one compare register, BURTC_COMP0. When the counter value is equal to the compare value, an interrupt will be set. In combination with setting the BURTC wake-up (BURTCWU) bit in EMU_EM4CONF , a timed wake-up from EM4 is possible. Note that enabling BURTCWU will cause a wake-up on any BURTC interrupt.

As opposed to many other registers, the BURTC registers are not reset on system reset, ensuring that the counter value and time-stamp are valid when waking up from backup mode. This also means that the one must take special care to initialize these registers when used for the first time.

Note that if an application is using the BURTC to keep track of time in Backup Mode it has to take special care of overflow. The BURTC cannot trigger an interrupt on overflow in this case (there is no main power) and therefore the application must manually check if an overflow occurred, for instance by comparing BURTC_TIMESTAMP and the counter value.

Figure 3.1. Backup Real Time Counter



3.2 Configuration

This is a quick walk-through of the configuration of the BURTC:

- First, reset the Backup Real Time Counter during configuration. Set the RESETEN bit in BURTC_CTRL.
- Select a clock source. The example uses LFXO as clock source to ensure accurate time keeping. Set the CLKSEL bit field in BURTC_CTRL to the desired source. For the BURTC to run in energy modes below EM2, EMU_EM4OSC must be configured accordingly.
- Set the clock pre-scaler. When using LFRCO or LFXO, the clock can be divided down by a factor from 1 to 128 in powers of 2. In the example, the clock is divided by 128 to allow the maximum time before the counter overflows. This results in a counter frequency of 256 Hz and that the counter can run for 194 days before overflowing.

- By default the BURTC is disabled. To make it available in backup mode, it must be enabled in all energy modes down to EM4. Set the MODE bit-field in BURTC_CTRL.
- Enable BURTC time-stamp upon backup mode entry. Set BUMODETSEN in BURTC_CTRL.
- In the example, the BURTC is used to keep track of time while the MCU is in backup mode. Configure the counter to not wrap around when it reaches the compare value in BURTC_COMP0. Clear the COMP0TOP bit in BURTC_CTRL.
- Finally, release reset bit for BURTC. This will clear the counter value and start the counter.

In the software example this is done by the *BURTC_setup()* function.

3.3 Retention Registers

The Backup RTC includes 128 32-bit registers, in total 512 bytes, that can offer retention in all energy modes. The registers are accessible through the BURTC_RET[0:127]_REG registers. Retention is by default enabled in all energy modes. The registers can be shut off to save power by setting the RAM bit in BURTC_POWERDOWN.

The retention registers are mapped to a RAM instance and have undefined state out of reset. If the system should lose main power and enter backup mode while writing to the retention registers, the RAM write error flag, RAMWERR, in BURTC_STATUS will be set. The flag is cleared by writing a 1 to CLRSTATUS in BURTC_CMD.

Note that the retention registers cannot be accessed when RSTEN in BURTC_CTRL is set.

3.4 Register Synchronization

The BURTC registers use the synchronization schemes that are described in the device family specific reference manuals. Most registers use immediate synchronizaton, except COMP0 and LPMODE which are asynchronous and use delayed synchronization.

The BURTC contains validation logic on the clock signals from the LFRCO and the LFXO. This validation logic is disabled when RSTEN in the CTRL register is set. This means that the asynchronous registers will not be synchronized while RSTEN is set, and subsequent writes to one of these registers may cause emlib to hang in a while-loop waiting for the corresponding SYNCBUSY flag to be released.

The clock signal from ULFRCO does not pass through this validation logic. So when ULFRCO is configured as BURTC clock source, the asynchronous registers will be synchronized even when BURTC_CTRL_RSTEN is set.

4 Software Example

4.1 BURTC Calendar Clock for Development Kit

The attached software example consists of a calendar application that demonstrates the features of the Backup Power Domain and the Backup RTC. A basic configuration of the backup power domain and the backup real time counter is shown. The Backup RTC is used as a system clock, and the capabilities of the backup power domain and the retention memory are used to maintain a correct clock during a main power brownout.

In the example, the Backup RTC is used for two separate purposes. At a regular interval (by default 1 second), the BURTC Comparator generates an interrupt that triggers an update of the TFT display. Separate from the display update, the Backup RTC is also used to keep track of system time. A *time()* function is implemented. This function calculates the system time based on the BURTC counter value, and outputs it as Unix time number. This the number of seconds passed since the Unix epoch which is (midnight UTC on January 1, 1970). C Standard library functions defined in *time.h* are used to convert Unix time to a human readable calendar format.

Two backup retention registers are used to store the necessary clock data to enable the correct system time to be restored in case of a main power brownout. This data is the start time and the BURTC overflow counter.

The example uses DVK GLIB to display date and time on the TFT display.

Between display updates, the MCU goes sleep. Normally, EM2 or EM3 would be used to keep the current consumption to a minimum. However, this would result in the current consumption being so low that the MCU would keep running for several seconds after VMCU is shut off just on the charge stored in the decoupling capacitors. For demonstration purposes, a more instant entry to backup mode is desired, so EM1 is used instead.

4.1.1 Instructions

Insert a 6.8 mm cell battery (not provided with kit) in the backup battery holder on the MCU board. If this is not available, a capacitor or another backup source can also be used. It is also possible to connect a strap from one of the 3.3 V test points to the positive part of the battery holder.

Compile the example, power up the DK and download the program to the MCU.

Press the AEM-button (rightmost button below TFT display) to toggle display control between the on-board DK controller (AEM mode) or the MCU (EFM mode). One press should set the display in EFM mode. When MCU is not using the TFT, three letters in top right hand corner of the TFT will indicate the mode.

Now, press reset on the MCU board. The display will show the calendar clock and some debug information.

To adjust the clock, use the push buttons below the TFT display in combination with the 4-way joystick:

- Year: Press and hold PB1 while moving joystick up or down
- Month: Press and hold PB2 while moving joystick up or down
- Day: Press and hold PB2 while moving joystick left or right
- Hour: Press and hold PB3 while moving joystick up or down
- Minute: Press and hold PB3 while moving joystick left or right
- Seconds are reset to zero whenever PB1-PB3 is pressed

The clock should now be running as normal. To use backup mode, press the AEM button once to switch display control to the AEM, then press PB2 to enter the CFG menu. To avoid the MCU to be back-

powered by DVK peripherals that are powered by 3.3 V, make sure that Debug Control is set to OFF and also that all DVK peripherals found in the PERI menu are OFF.

Now set VMCU to OFF to shut off MCU main power. The MCU now enters backup mode.

How long the MCU can stay in backup mode depends on the capacity of the backup power source. Switch VMCU back on before the backup source drains out.

When display control is transferred back to the MCU, the display should show the restored calendar clock. Verify that RMU_RSTCAUSE and BURTC_SATUS have reasonable values.

Please note that when the AEM is used to set the VMCU Level, the DK always resets the MCU between each step. This function can therefore not be used to gradually decrease VMCU until backup mode is entered. Also, a main power out or reset on the Development Kit will reset the MCU and time info will be lost.

4.2 BURTC Calendar Clock for Starter Kit

A software example for the Giant Gecko Starter Kit, EFM32GG-STK3700, is also included. This example shares the same backup functionality as the Development Kit example, but the user interface is much simpler.

The Segment LCD is used to display a 24 hour clock only. No date information is shown. The two push buttons on the kit are used to set the time. The left push button adds 1 hour to the time while the right push button adds one minute.

The starter kit features a 30 mF super capacitor that is used to power the EFM32 while in backup mode.

5 Revision History

5.1 Revision 1.26

2014-05-07

Added information on BOD thresholds

RESETn internal pull-up described

Added description of issue where device in some cases will not start-up after a brown-out on BU_VIN

Added warning about setting BUACT_PWRCONF to MAINBU

Better check of RMU->RSTCAUSE in software examples

General clean-up of software examples

Updated example code to CMSIS 3.20.5

Changed to Silicon Labs license on code examples

Added project files for Simplicity IDE

Removed makefiles for Sourcery CodeBench Lite

5.2 Revision 1.25

2013-10-14

New cover layout

5.3 Revision 1.24

2013-05-08

Added software projects for ARM-GCC and Atollic TrueStudio.

Fixed a bug where the application would be stuck if reset was pressed during backup mode.

5.4 Revision 1.23

2012-11-12

Adapted software projects to new kit-driver and BSP structure.

5.5 Revision 1.22

2012-08-13

Updated file paths for glib

5.6 Revision 1.21

2012-06-11

Disabled BU_STAT pin on EFM32GG-STK3700 example. On the STK, this pin is also connected to a LED, causing an unwanted increase in the backup mode current consumption.

5.7 Revision 1.20

2012-06-11

Added software project for EFM32GG-STK3700.

5.8 Revision 1.11

2012-04-20

Adapted software projects to new peripheral library naming and CMSIS_V3.

5.9 Revision 1.10

2012-03-29

Example updated to use efm32lib library functions.

Fixed an issue with time recovery was wrong when restoring clock from Backup Mode if BURTC overflow had occurred before Backup Mode was entered.

Fixed an issue with very high current consumption in Backup Mode because the clock divider for the BURTC was outside of specifications.

5.10 Revision 1.00

2012-02-08

Initial revision.

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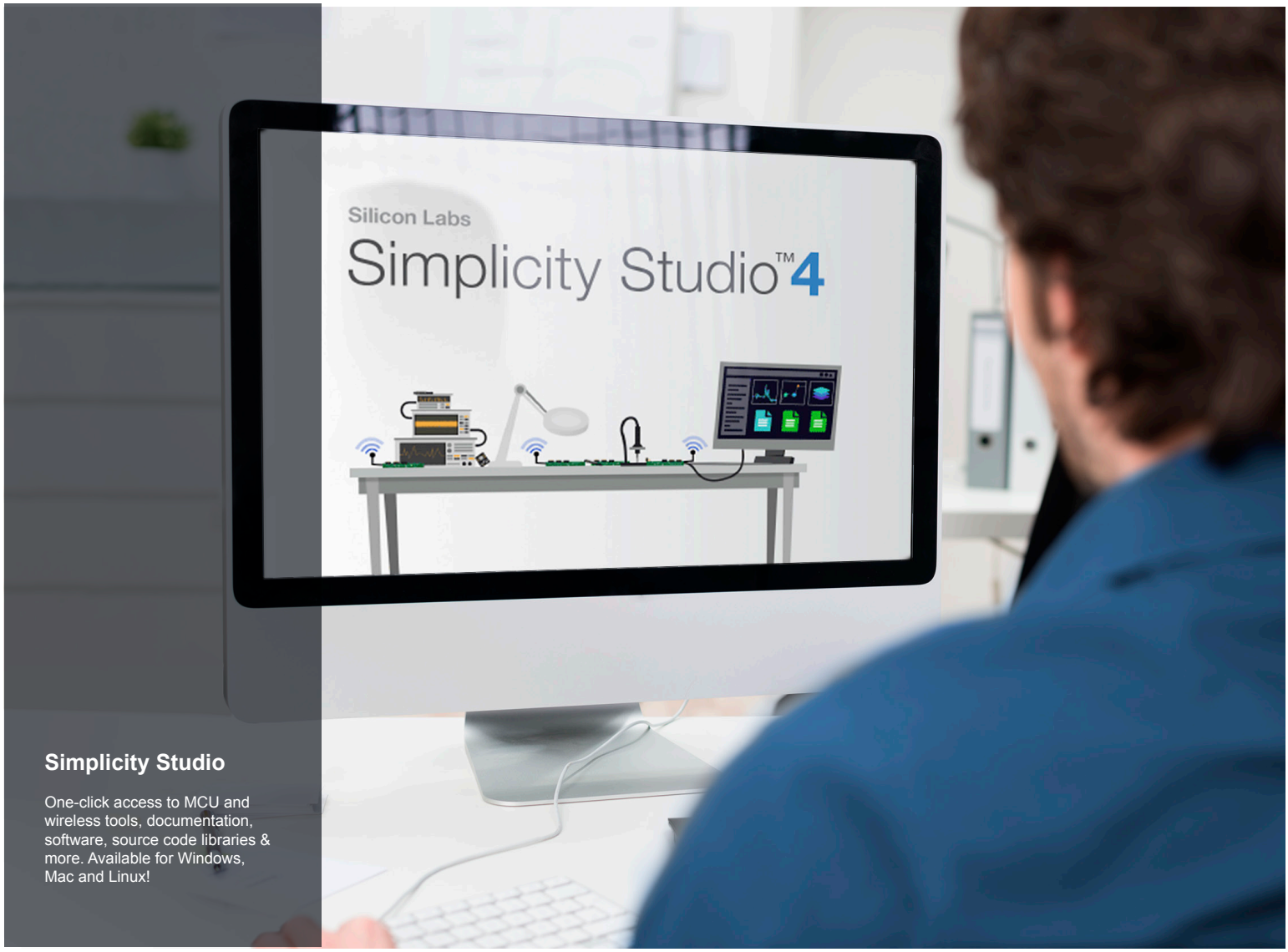

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