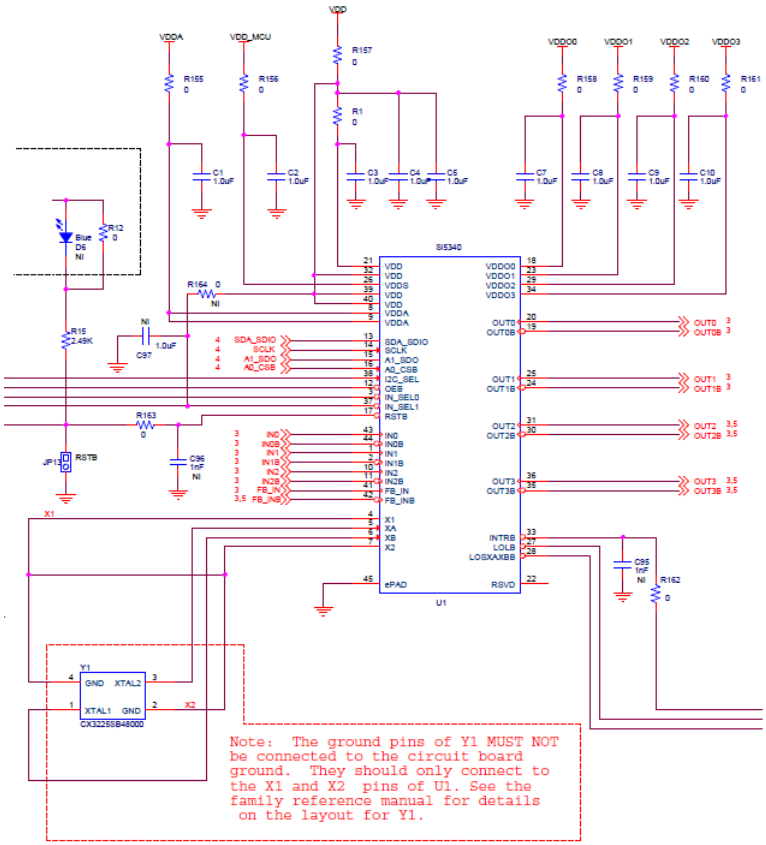
AN1051: Si534x/7x/8x/9x Schematic Review Checklist Application Note

This application note contains a schematic review checklist, which can be used as an initial step in evaluating a Si534x/7x/8x/9x schematic design. Considering the items listed in this document before committing to layout will contribute to a successful design.

Illustrated below is an excerpt from the Si5340-D-EB evaluation board schematic.



KEY POINTS

- This schematic review checklist application note applies to Silicon Labs Si534x/7x/8x/9x clock generators and jitter attenuators.
- This document addresses these topics:
  - Internal/External Crystal Reference
  - External XO/TCXO/OCXO Reference
  - Input Clocks
  - Output Clocks
  - Power Supply Distribution Network
  - Serial Communication
  - Digital I/O

1. Introduction

This schematic review checklist application note applies to Silicon Labs Si534x/7x/8x/9x devices. Examples of such devices are the Si5348, Si5372, Si5386 and Si5395.

Please review this checklist and consider each of the listed topics in your board's schematic design.

It is a good idea when getting started to make sure you have the latest documentation, especially the data sheet and reference manuals. These documents are all available from http://www.silabs.com. Evaluation board documentation such as for the Si5395-A-EVB are available at https://www.silabs.com/documents/public/user-guides/ug335-si5395evb.pdf.

Note that there are 2 reference documents that apply to every Si534x/7x/8x/9x device. The first is a Reference Manual (RM) or Family Reference Manual (FRM) that contains technical application details such as register programming and layout considerations for each device or device family. Examples are the *https://www.silabs.com/documents/login/reference-manuals/si5395-94-92-family.pdf* and the *https://www.silabs.com/documents/public/reference-manuals/si5348-e-family.pdf*. Unless otherwise noted, the terms RM or Reference Manual will refer to the device-specific reference document.

The second is a stand-alone crystal reference document that applies to *all* Si534x/7x/8x/9x devices. This is the Si534x/8x Jitter Attenuators Recommended Crystal, TCXO, and OCXOs Reference Manual. It is essentially a list of approved crystals and crystal oscillators.

2. Checklist

The following is a checklist of items every designer should review in the schematic and layout.

- Output Clocks
- Input Clocks
- References
- Power Supply Distribution Network
- Serial Communication
- Digital I/O
- CBPro Project File

2.1 Output Clocks

The primary considerations here are proper output terminations, signal integrity, supporting ZDM (Zero Delay Mode) if necessary, and optimizing output clock placement. Please consider using the "Clock Placement Wizard" in CBPro to ensure the output placement is optimized to minimize crosstalk.

1. LVDS Format Output Termination

- LVDS output clocks may be AC coupled or DC coupled
- A 100 ohm differential termination must be used, according to Figure 2.1 DC Coupled LVDS on page 4 and Figure 2.2 AC Coupled LVDS/LVPECL/Custom Differential on page 4. The termination may either be internal to the destination device or an external resistor.

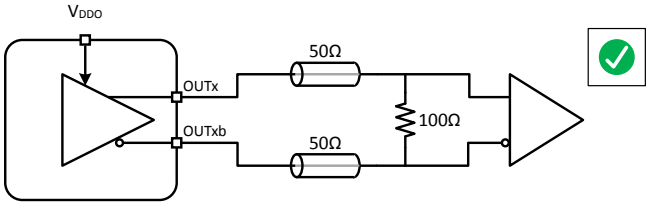


Figure 2.1. DC Coupled LVDS

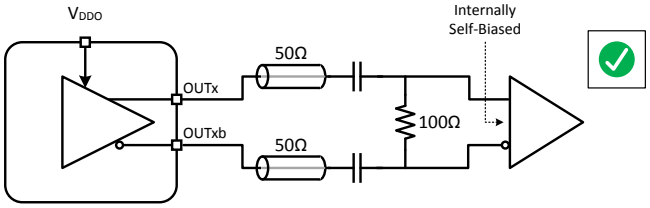


Figure 2.2. AC Coupled LVDS/LVPECL/Custom Differential

2. LVPECL Format Output Termination

- LVPECL output clocks must be AC coupled
- 100 ohm differential termination should be used, according to Figure 2.2 AC Coupled LVDS/LVPECL/Custom Differential on page 4. The termination may either be internal to the destination device or an external resistor.
- Shunt resistors to ground or series resistors should NOT be added, according to Figure 2.3 Shunt Resistors at Source Should NOT Be Used on page 4.

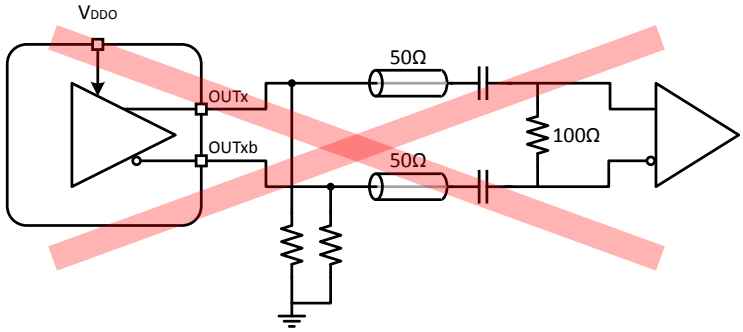


Figure 2.3. Shunt Resistors at Source Should NOT Be Used

3. CML Format Output Termination

- CML output clocks must be AC coupled.
- 50 ohm termination resistors should be applied to each leg, according to Figure 2.4 AC Coupled CML Termination on page 5.

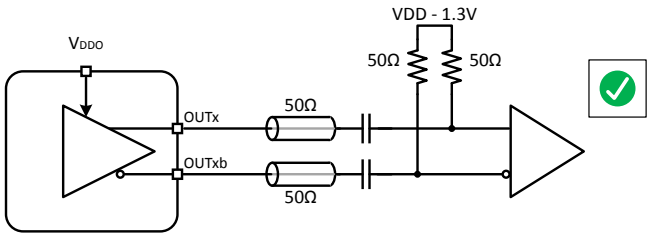


Figure 2.4. AC Coupled CML Termination

- Pull-up resistors at the source should NOT be added, according to Figure 2.5 Incorrect CML Termination on page 5.

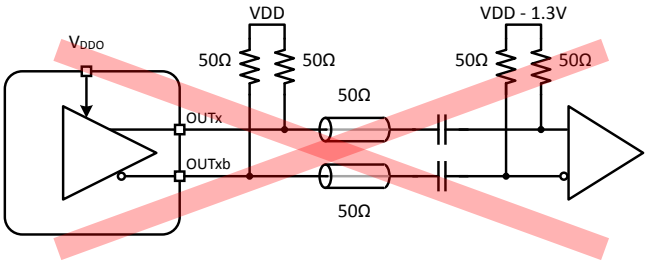
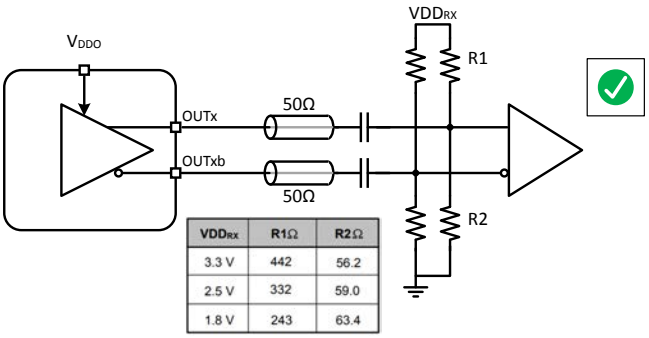


Figure 2.5. Incorrect CML Termination

4. HCSL Format Output Termination

- HCSL output clocks must be AC coupled.
- The resistor divider termination network in Figure 2.6 AC Coupled HCSL on page 5 should be used. This serves to (1) provide 50 ohm termination to each leg and (2) bias the common-mode level of the HCSL signal to the desired level.



VDDRX	R1Ω	R2Ω
3.3 V	442	56.2
2.5 V	332	59.0
1.8 V	243	63.4

Figure 2.6. AC Coupled HCSL

- Shunt resistors to ground or series resistors at the source should NOT be added, according to Figure 2.7 Incorrect HCSL Terminations on page 6.
- DC coupling the output clock with 50 ohms to ground should NOT be done, according to Figure 2.7 Incorrect HCSL Terminations on page 6.

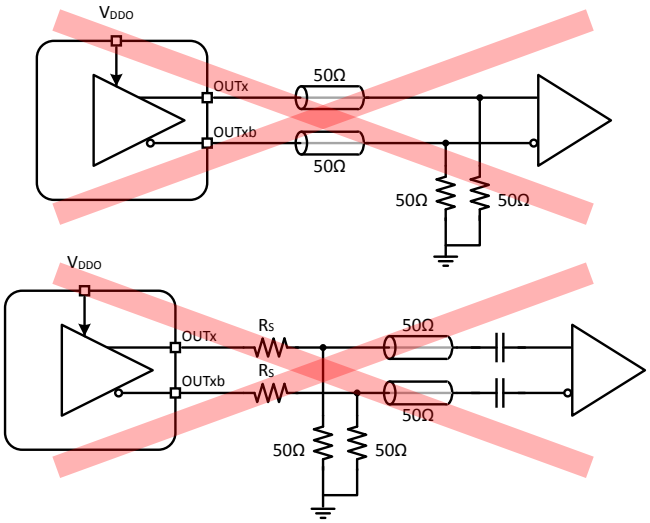


Figure 2.7. Incorrect HCSL Terminations

5. Custom Differential Format Output Termination

- Custom differential output clocks must be AC coupled.
- 100 ohm differential termination should be used, according to Figure 2.2 AC Coupled LVDS/LVPECL/Custom Differential on page 4. The termination may either be internal to the destination device or an external resistor.

6. CMOS Format Output Termination

- Series or near end source termination may be required for CMOS outputs. Please see the Reference Manual for the recommended resistor value.
- Differential clocks provide higher performance than CMOS clocks. Please see application note *AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems*.

7. ZDB Mode

- If the device supports ZDB mode, route the nearest shortest route output clock fed back to IN3/FB_IN. Input and output pin polarities are such that no vias are needed to make this connection. The application must get polarity correct.

2.2 Input Clocks

The primary considerations here are signal integrity and optimizing input clock placement.

1. AC-coupling caps per RM recommendations? Ensure that AC coupling capacitors have <5 ohms capacitive reactance at the input clock frequency.
2. Review input terminations per RM recommendations?
3. Input clock connections correct for CMOS? Make sure the Project File selects the Standard input buffer. The Pulsed LVCMOS buffer is only used by exception for low frequency (≤ 1 MHz) low duty cycle single-ended DC-coupled LVCMOS. Refer to the RM for the recommended termination network to keep the signal at INx within the absolute maximum voltage levels: -1V<INx<3.8V.
4. Please consider the use of a "split termination" for input differential clock signals if the board may be noisy and there is room to do so. A split termination for input clocks is a conservative approach to common-mode (CM) noise suppression. It is a modification of the standard textbook terminations described in the Reference Manual and is discussed in the Knowledge Base article, "Terminating Differential Transmission Lines to Minimize CM Noise." Below is an illustration modified after the diagram cited in that article.

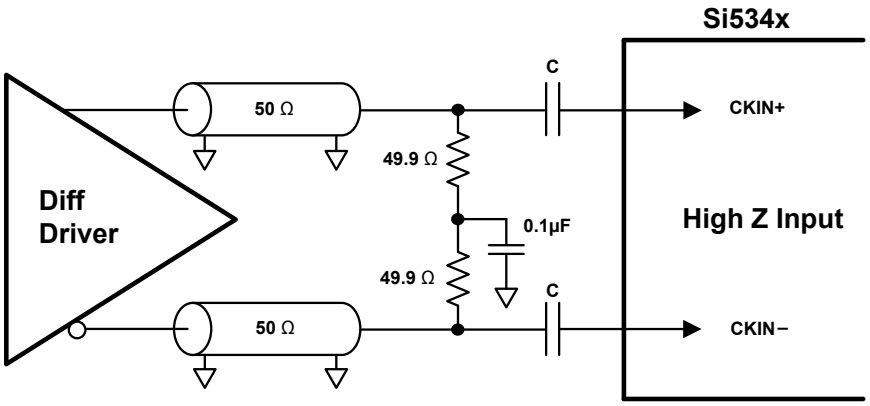
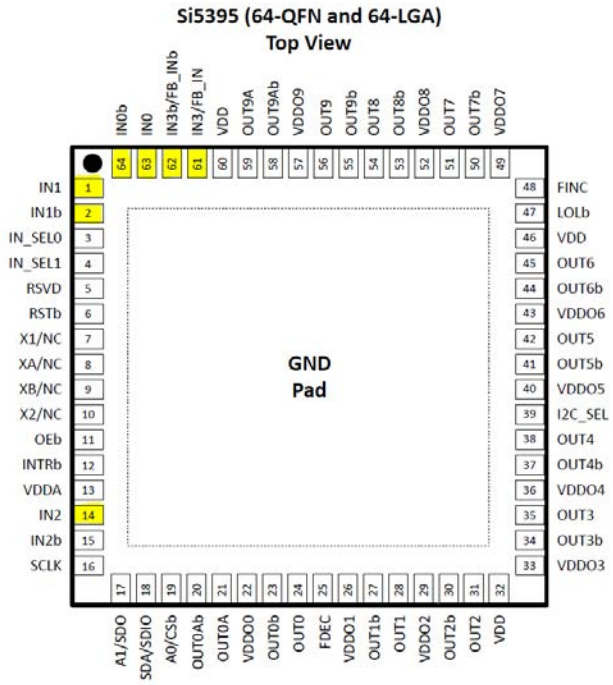


Figure 2.8. Example Split Termination

5. Connection to the single-pin CMOS clock inputs on Si5348 IN3/IN4 correct per RM?
6. In general, input clock selections are preferred based on maximum distance from XA/XB pins. This reduces the possibility of XA/XB crosstalk to input clock traces in the PCB. For example, see the following figure taken from the Si5395 data sheet.



In this specific example, proximity and orthogonality to the XA and XB pins suggest the preferred input clocks in order would be IN3, IN0, IN1, IN2.

7. If the unused input clocks are declared as being unused in the CBPro project file, their pins can be left as "no connect". AC coupling the unused inputs to ground is also permissible but not required.

8. If the unused input clocks are not declared as being unused in the CBPro project file, then one side of the pair should be pulled up with a resistor, and the other side of the pair should be pulled low with a resistor. But it is always preferable to declare the unused input clocks as unused in the CBPro project file.

2.3 External Crystal/ OCXO,TCXO,XO External Reference/ Internal Reference Device

A crystal or external reference clock is required to be connected at the XA/XB pins for all the jitter attenuators and independent (i.e., no output clock) clock generators. The crystal or external reference determines the close-in phase noise of the output clocks. The items listed here are intended to ensure that the crystal operates properly and that external noise is minimized.

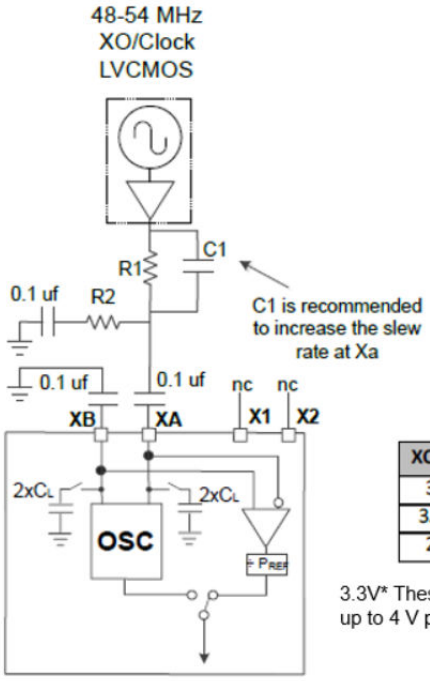
2.3.1 External Crystal Reference

1. Does the crystal selected as the external reference meet the datasheet parameters such as frequency, equivalent series resistance, and shunt capacitance? For a list of suitable crystals, see the *Si534x/8x Jitter Attenuators Recommended Crystal, TCXO and OCXOs Reference Manual* https://www.silabs.com/documents/public/reference-manuals/si534x-8x-9x-recommended-crystals-rm.pdf
2. Crystal connected directly to the device's XA and XB pins? Please see the applicable device reference manual for layout details.
3. Make sure that the crystal pins designated X1 and X2 are **not** connected to PCB GND. The guard ring around the crystal connects to the device's X1 and X2 pins only.
4. Make sure there are no crystal external load capacitors.

2.3.2 OCXO/TCXO/XO External Reference Applied to XA/XB Pins

An OCXO, TCXO, or XO can be connected to the device's XA or XA and XB pins instead of a crystal.

1. Selection appropriate? Any oscillator applied to the crystal input pins should have the correct frequency and low enough phase noise and jitter to achieve output clock jitter requirements. See application note *AN905: Si534x External References: Optimizing Performance* for guidance at http://www.silabs.com/support%20documents/technicaldocs/an905.pdf. For a list of suitable oscillators, please see the *Si534x/8x Jitter Attenuators Recommended Crystal, TCXO and OCXOs Reference Manual* at https://www.silabs.com/documents/public/reference-manuals/si534x-8x-9x-recommended-crystals-rm.pdf
2. AC-coupling caps per RM recommendations?
3. Terminations correct per RM recommendations?
4. Split termination for differential clock signals at XA and XB? (Please see explanation of this approach under Input Clocks.)
5. Leave pins X1 and X2 unconnected in this case unlike the crystal case.
6. Single-ended reference oscillators should be connected to XA and not XB in order to obtain LOSXAXB support. The unused XB pin should be bypassed to ground with a capacitor that is as close to the XB pin as possible.
7. Because of slow rise/fall times, it is always preferable to avoid using clipped sine wave XOs and TCXOs. Instead, the outputs should be CMOS.
8. When the XA pin is being driven by a CMOS signal, it is important to include a feed forward cap in the attenuator circuit, as shown in the below example circuit.
9. Place the external reference close to the XA/XB pins.
10. Ensure that the external reference's CMOS voltage applied to XA is less than 2V pp_se. The figure below provides an example when the CMOS signal applied may be up to 4V pp_se. The feed forward capacitor C1 is optional but recommended to improve the slew rate and, therefore, the phase noise performance.



XO VDD	R1	R2	C1
3.3V	453 Ω	549 Ω	12 pf
3.3V *	665 Ω	549 Ω	10 pf
2.5V	274 Ω	732 Ω	30 pf

3.3V* These settings should be done if the CMOS level is up to 4 V pp to limit the input at XA to less than 2 V ppse

2.3.3 External Reference Applied to REF/REFb Pins

An external reference may be applied to the REF/REFb pins of the Si5348/88/89 devices.

1. Selection appropriate? The external reference applied to the REF/REFb pins should have the necessary accuracy, wander, and stability for the required application. See application note *AN905: Si534x External References: Optimizing Performance* for guidance at http://www.silabs.com/support%20documents/technicaldocs/an905.pdf. For a list of suitable TCXOs/OCXOs, please see the *Si534x/8x Jitter Attenuators Recommended Crystal, TCXO and OCXOs Reference Manual* at https://www.silabs.com/documents/public/reference-manuals/si534x-8x-9x-recommended-crystals-rm.pdf
2. AC-coupling caps per RM recommendations?
3. Terminations correct per RM recommendations?
4. Single-ended external references should be connected to the REF pin and not the REFb pin. The unused REFb pin should be bypassed to ground with a capacitor.
5. Because of slow rise/fall times, it is always preferable to avoid using clipped sine wave TCXOs and OCXOs. Instead, the outputs should be CMOS.
6. When the REF pin is being driven by a CMOS signal, it is important to include a feed forward cap in the attenuator circuit, per RM recommendation.
7. When the REF pin is being driven by a CMOS signal, the TCXO/OCXO should be placed close to the REF pin.

2.3.4 Embedded Crystal Devices

Using one of the embedded crystal devices (grades J/K/L/M/E) simplify the schematic and layout since the crystal is internal to the chip. There are no external components required.

If one of the devices on the PCB is an embedded crystal device (e.g. Si5395J-A), be sure that the X1, XA, XB and X2 pins are "no connect" For the Si5395J, these are pins 7, 8, 9 and 10.

2.4 Power Supply Distribution Network

1. 1.8 V to VDD?
2. 3.3 V to VDDA?
3. 1.8, 2.5, or 3.3 V to VDDOn?

   Note: "VDDOn" here refers to the VDDO for each output clock buffer. For example, the Si5345 has VDDO0, VDDO1, ... VDDO9.

4. Bypass Capacitors are, generally, not critical. Here are some guidelines:
   a. VDD: 1 µF per pin, as close as possible. (The customer EVB uses 1 µf//0.1 µF//series to an inductor and shunt 0.1 µF.)
   b. VDDA: 1 µF per pin, as close as possible.
   c. VDDOn: 1 µF per pin, as close as possible.
5. Ferrite Bead or Inductor
   a. Series connected ferrite beads and inductors are usually not needed. However, including zero ohm resistors in the PCB layout to isolate the power supply pins is prudent. The suggested resistor size is 0603 so that a ferrite bead can be accommodated in the footprint if necessary.
   b. If you have a series ferrite bead or inductor, you may want to consider adding additional bulk capacitance.
   c. The CEVB 30 Ω inductor on VDD is not needed.

2.5 Serial Communication

1. Are the connections correct for I^2C, 3-wire, or 4-wire SPI?
2. If I^2C is used, are the bus pull-up resistors present? Only 1 set of resistors should be used (no duplicates with same bus on different schematic pages.)
3. Verify A0/A1 connections are unique for each Silicon Labs device on an I^2C bus.
4. Consider including provisions for a male 10-pin header to support the Field Programmer. (Optional but recommended for Field Programmer support.)
5. Ensure that voltage level of the serial interface matches the bit IO_VDD_SEL, which is at addr 0x0943[0]. When the bit equals 0 the external connection should be 1.8V, and when the bit equals 1 the external connection should be 3.3V.

2.6 Digital I/O

1. External pullups and pulldowns:
   a. Any digital inputs that must be pulled or tied externally? The following cannot be left floating when unused and must be pulled high or low when unused. Refer to the datasheet for further details.
      i. Si5397: FDEC & OE1b
      ii. Si5348: FDEC
      iii. Si5347: FDEC & OE1b
   b. To be conservative, an external pull-up or pull-down resistor can be added even if the device already has one, since the internal pull-ups and pull-downs are relatively weak. Refer to the datasheet for further details.
   c. Any unnecessary and just waste power? GPIO outputs (e.g. LOLb, INTRb) are always actively driven high unless they are asserted, so pull-up/down resistors on these pins are unnecessary. Refer to the datasheet for details on each GPIO pin.
2. Recommend that even unused digital I/O be connected to at least a test pad, pin, or via just in case.
3. The status output signals (e.g., LOL) are capable of driving 2 mA. Check to be sure that their load does not demand more current.
4. Most digital inputs (e.g., OEb) have internal pull up/down resistors. Check the data sheet and if the correct pull up/down is in place, the pins can be "no connect".

2.7 CBPro Project File

The assignment of clock I/O, serial port, XAXB reference, etc, in the schematic should be checked against the CBPro project file(s) that will be used on the board.

ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

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