# AN111: Using 8-Bit MCUs in 5 Volt Systems

This document describes how to incorporate Silicon Lab's 8-bit EFM8 and C8051 families of devices into existing 5 V systems.

When using a 3 V device in a 5 V system, the user must consider:

- A 3 V power supply must be provided.
- A 5 V device driving a 3 V input.
- A 3 V device driving a 5 V input.

KEY POINTS

- Two solutions for interfacing a 3 V MCU with a 5 V system are using logic gates or pull-up resistors.
- If using pull-up resistors, the size of the resistor must be carefully considered to address rise time and power consumption concerns.
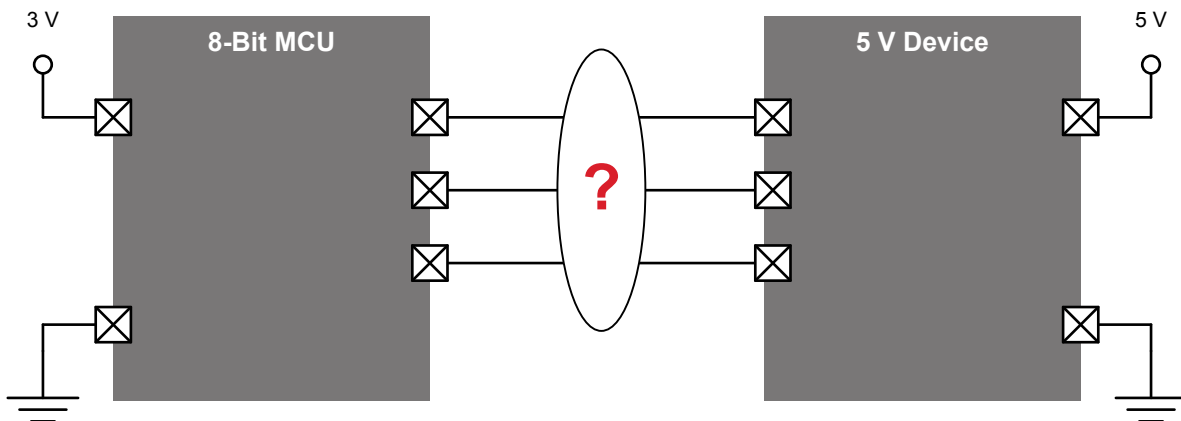
1. Power Supply

There are several factors in determining what method should be used to provide the 3 V power supply from the existing 5 V power supply. Among these is the reliability of the 5 V power supply and the source of power to the system (i.e., battery or ac with rectifier). Conditioning the 5 V power supply to provide 3 V will increase the number of components in the design and will cost some additional power, which is especially important in low power applications using a battery.

1.1 Rectified Line Power Supply

Power may be supplied from a commercial power supply. This supply is typically poorly regulated. To provide a clean and stable 3 V power supply, we recommend a Low Dropout Regulator (LDO).

The LDO must be able to supply the specified current for the given part and other 3 V peripherals that may be in use in the application. These specifications may be found in the appropriate data sheets. For example, the typical current specified in Silicon Lab's C8051F001 data sheet is 12 mA @ 20 MHz with analog peripherals active (10 mA digital supply current with CPU active and 2 mA for analog peripherals). Additionally, if other devices are in use such as LED's, the design must account for the additional current needed.

Some example LDO's available that convert 5 V to 3 V are:
- National Semiconductor's LM3940
- Texas Instrument's TPS769xx Family

1.2 Battery Power Supply

Batteries generally provide a clean power supply. However, applications using batteries must be low power, so dc-dc converters should be used as they are more efficient than LDOs.

The device must be able to provide the proper voltage for the application's required maximum current. Some dc-dc converters available are:
- National Semiconductor's LM2825
- C&D Technologies' LME305D and LME305S
- Texas Instrument's TPS769xx family of LDOs is also optimized for battery applications
Unlike LDOs, dc-dc converters can provide an output voltage that is higher than the input voltage.

2. 5 V Tolerant Inputs

Connecting a 5 V driver to a standard 3 V input can cause damage or reduce component life due to current flow into ESD protection devices. Many of the Silicon Labs 8-bit MCUs (EFM8 and C8051) use input structures that are 5 V tolerant. In these cases, the designer may connect 5 V devices directly to digital input pins without causing harmful current flow. Consult the Absolute Maximum Ratings table in the Electrical Specifications chapter of the device data sheet for more information.

3. Driving a 5 V Input with a 3 V Driver

Even though an MCU's digital inputs are 5 V tolerant, the outputs can only drive as high as VDD (up to 3.6 V). If the 5 V device requires an input voltage higher than VDD to operate, then additional configuration is necessary. The two main methods of driving a 5 V input are using logic gates and pull-up resistors.

3.1 Interfacing Using Logic Gates

Logic gates in the 74VHCTxx family can be used to interface 3 V to 5 V systems. The figure below shows how the 74VHCTxx device takes in a 3 V signal and drives a 5 V signal. Interfacing with logic gates is recommended for applications with high-speed signals. The main drawbacks are the cost and board space used by the 74VHCTxx device.
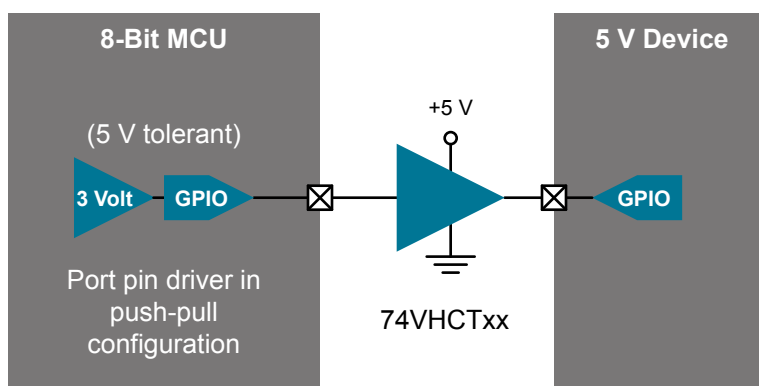

Figure 3.1. Interfacing with Logic Gates

3.2 Interfacing Using Pull-up Resistors

A low cost alternative to logic gates that requires less board space is a pull-up resistor. A pull-up resistor can be used to supply voltages greater than VDD. To accomplish this, we set the output mode of the port pin to open-drain. In open-drain mode, a logic 1 on the port latch makes the port high impedance, and a logic 0 causes it to drive a low signal. When connected to a 5 V device through a pull-up resistor, as shown in the figure below, a logic 1 output from the 8-bit MCU will rise to 5 V, and a logic 0 will go to ground.
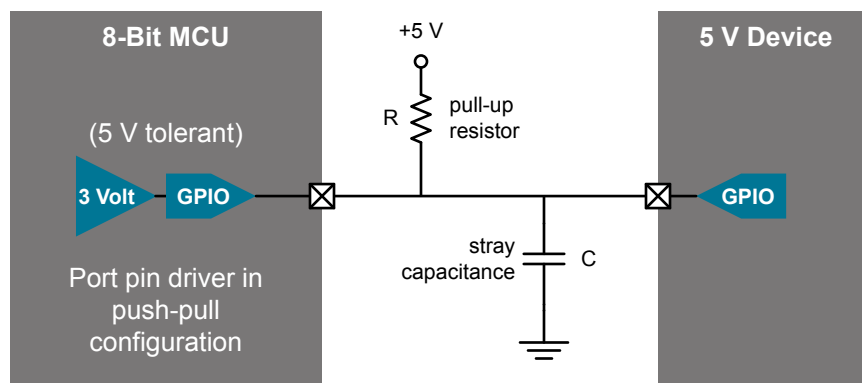

Figure 3.2. Driving a 5 V Device Input with a Pull-Up Resistor

3.2.1 Choosing a Pull-Up Resistor

When the port pin is a logic 0, the output voltage will be near ground. In this state, current will flow to ground through the pull-up resistor and port driver. To save power, a large value resistor is needed to minimize this current flow.

When the port pin is set to logic 1, the output driver turns off and the voltage at the port output is pulled high through the pull-up resistor. The rise time of this signal can be quite long and is determined by the value of the pull-up resistor and the amount of stray capacitance due to the connecting trace and input circuitry. In the circuit in Figure 3.2 Driving a 5 V Device Input with a Pull-Up Resistor on page 3, the stray capacitance is charged from the 5 V power supply through the pull-up resistor with a time constant equal to the product of the stray capacitance and pull-up resistance as follows:

$$V(t) = 5 \text{ V} \times \left(1 - e^{\frac{-t}{RC}}\right)$$

Stray capacitance is negligible if timing is not important (e.g., a push button or chip select signals). However, if the timing is important (e.g., serial communications, clock signal synchronization), then the charge time must be considered, and this will limit the maximum size of the pull-up resistor. A pull-up resistor that is large will result in a large time to charge the stray capacitance, and a long time to get the port pin voltage high enough to realize a logic 1. See Figure 3.3 Square Wave with Charge Time Due to Stray Capacitance on page 4, where T is the time it takes to charge above the voltage required for the 5 V device to realize a logic 1 (commonly referred to as V_{IH}).
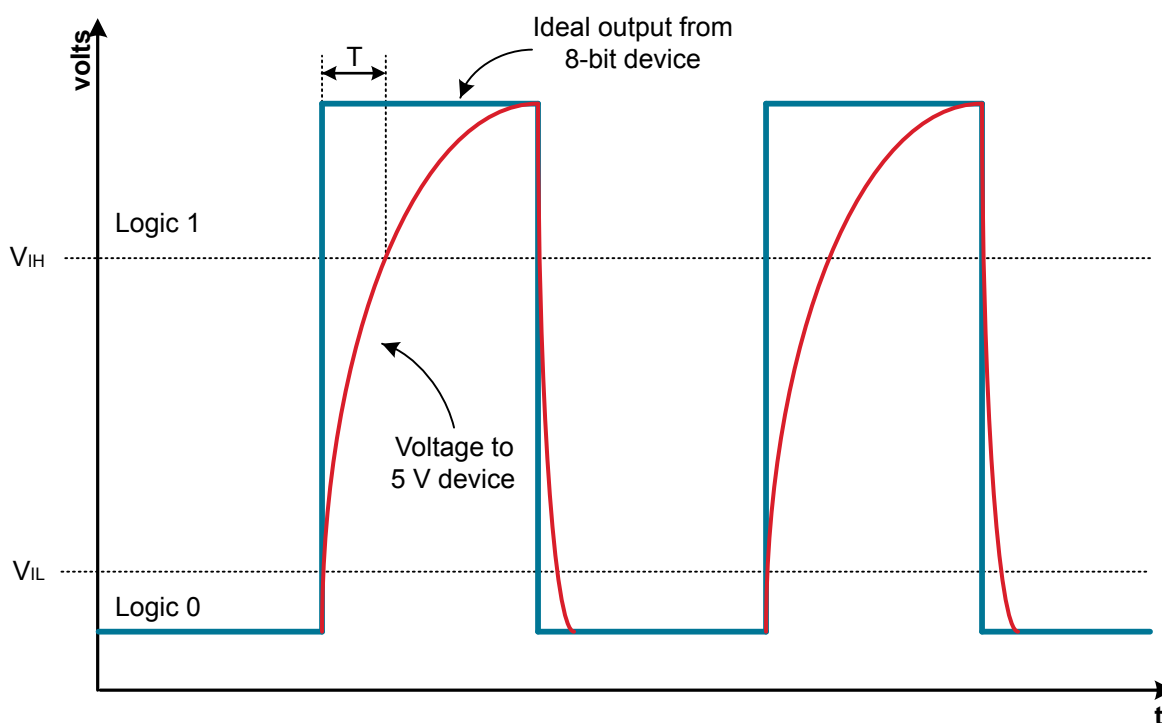

Figure 3.3. Square Wave with Charge Time Due to Stray Capacitance

This voltage will depend on the application, as will the value of the stray capacitance. If the time constant is too large, the 5 V device may never receive a high enough voltage to realize a logic 1 at a given square wave frequency. For this reason, the chosen pull-up resistance (R) must be low enough for proper input, but the R must not be so low that excessive power is dissipated in the pull-up resistor during logic low state. Once the maximum acceptable rise time (T) is determined for a given application, the value of the pull-up resistor (R) can be calculated by solving for R:

$$R = \frac{T}{C \times \ln\left(\frac{5}{5 - V_{IH}}\right)}$$

Even though there is a slight delay in the output voltage dropping from high to low (1 to 0), this time is insignificant when compared to the rise time. This delay is illustrated (although exagerated) in Figure 3.3 Square Wave with Charge Time Due to Stray Capacitance on page 4 to show the small decay time. The charge in the stray capacitance discharges through the 8-bit MCU port driver with a small voltage drop to ground.

As previously mentioned, if the resistance is low, large amounts of power may be consumed as current flows from the 5 V power supply to ground in logic 0 state. Additionally, if the value of the resistor is too low, the low state voltage may be too high to realize a logic 0 (V_{OL}) due to the voltage drop across the port driver. For example, the V_{OL} specification for the C8051F0xx devices is 0.6 V at 8.5 mA. A small resistance may result in higher currents and thus a higher voltage input to the 5 V device.

In summary, a pull-up resistor must be:

1. Large enough to prevent excessive current flow and power consumption in the logic 0 state.
2. Large enough to keep the voltage below the V_{IL} specification of the 5 V device to realize a logic 0 state.
3. Small enough to provide acceptable rise times based on the amount of stray capacitance and the requirements of the application.

3.2.2 Pull-Up Example

The following is an example of calculating a proper pull-up resistor value (R) for a given stray capacitance (C), required voltage level for a logic 1 (V_{IH}), and frequency of state change to determine maximum allowable rise time (T). Additionally, we will investigate the power consumption in the pullup resistor and voltage level when in the logic 0 state. From this calculation, we will determine a value for the pull-up resistor (R).

In this example application, we will consider an application using the SMBus which uses an open-drain synchronizing clock signal (SCL) output from an EFM8 or C8051 in Master Mode (supplying the SCL signal to other devices). This signal will output to a 5 V device, and so the configuration in Figure 3.2 Driving a 5 V Device Input with a Pull-Up Resistor on page 3 will be used to ensure proper voltage supplied. Ensure port pins used in this method are configured as open-drain (see associated data sheets). EFM8 and C8051 port pins default to open-drain configuration upon reset.

A proper pull-up resistor value (R) must be calculated to ensure:

• Minimal current/power loss when in a logic low (0) state (R too low).
• Performance specifications are not violated due to the rise time associated with the stray capacitance and pull-up resistance. (R too high).
• In a logic low state, voltage is not too high due to the voltage drop across the port driver (R too low).

Ideally, a high resistance would be used in order to minimize power loss which can be critical in low power applications (i.e., when using a battery power supply). We will calculate the highest resistance we can use while meeting voltage rise time specifications. For this application, the voltage should be high enough to realize a logic 1 for CMOS logic in the 5 V device within 5% of the clock period. We assume a V_{IH} of 0.8*VDD, or 4 V. Choosing a SCL frequency of 400 kHz, our voltage should rise to 4 V within 125 ns.

Thus, referring to the second equation, T = 125 ns and V_{IH} = 4 V. We will assume the stray capacitance to be 10 pF with one slave device connected to the SCL line.
Note: This will vary for different applications, depending on the number of devices connected and amount of wiring and traces used to connect these devices.

Using this equation, we calculate R = 7.77 kΩ. This is the maximum resistor value that can be used at the specified SCL frequency and specification we set for the CMOS input logic. If the SCL frequency were lower, then a higher resistance could be used.

Now that we have a desired maximum pull-up resistance, we can calculate the current flowing through the circuit when at a logic 0 to see if this is acceptable for a given application. In the worst case condition, we calculate the current flow with a 5 V power supply and negligible voltage drop in the port pin to ground. The current through the 7.77 kΩ resistor is then 644 µA. The power dissipation in the pull-up resistor at 644 µA of current is approximately 3.2 mW.

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