DIFFERENCES BETWEEN THE C8051F310 AND THE C8051T61X DEVICE FAMILY

1. Introduction

The C8051T61x devices are low-cost, byte-programmable EPROM code memory microcontrollers based on the Silicon Laboratories CIP-51 microcontroller core. As with Silicon Laboratories' C8051F-series Flash-based microcontrollers, the C8051T61x are highly-integrated, mixed-signal devices incorporating communication peripherals as well as analog-to-digital converter (ADC) technology. Also included is the C2 2-wire debugging and programming interface, allowing designers to rapidly develop and debug firmware.

Because the devices in the C8051T61x family cannot be erased, a new device is required for testing every time the firmware changes. This could make the code development process more difficult and time consuming. Fortunately, the features found in the C8051T61x family are closely related to the features of the Flash-based C8051F31x family. In most cases, this allows the C8051F310 to be used for the entire code development process, and the firmware image will be interchangeable between the two device families. For systems that take advantage of the additional features found in the C8051T61x family, the majority of the firmware can still be developed on the C8051F310 device and then ported to the C8051T61x during the final stages of code development.

This document details the hardware differences between the two device families and provides some guidelines for using the C8051F310 to develop code for the C8051T61x.

2. Key Points

- Although the majority of device features are identical between the C8051F310 and the C8051T61x, there are some hardware differences.
- When developing code for the C8051T61x device family, the majority of the code development process can be done on the Flash-based C8051F310.
- Each device has a set of unique features that are not present on the other family. Recognizing these differences is the key to successfully developing common code (code that works on either family) as well as code that uses some of the additional features found on the C8051T61x.

3. Code Memory Storage

The most obvious difference between the C8051F31x and the C8051T61x devices is the code memory storage technology. On the C8051F31x devices, Flash memory is used, while on the C8051T61x devices, an EPROM code memory architecture is used. Table 1 details some parameters of interest related to the code storage technology.

Table 1. Code Memory Storage

Feature	C8051F310	C8051T61x
Code memory can be programmed multiple times	Yes	No
Programming voltage (V_{PP}) required to program code memory	No	Yes
Code memory can be written or erased from firmware on the device	Yes	No
Code memory can be read from firmware on the device	Yes	

The impact of the code storage technology on the development of C8051T61x firmware is minimal. When developing firmware for the C8051T61x on the C8051F310 or porting an existing design, make certain that there are no firmware routines intended to write or erase areas of code memory, as they will not have any effect on the C8051T61x.

4. Special Function Registers

The special function register (SFR) memory map of the C8051T61x is very similar to the SFR memory map of the C8051F310. However, there are a few differences related to functionality and features found on only one of the two device families. Fortunately, SFRs that exist in one family but not the other can be safely written and read on the other device family without causing a problem. Likewise, certain registers have additional bits defined that are not present on both devices. In these cases, the default bit settings are safe to write, and the read values of those bits are defined in the datasheet. Figure 1 shows the combined SFR map of the two device families. The locations of SFRs that differ between the two families and those with only bitwise differences are highlighted.

F8	SPI0CN	PCA0L	PCA0H	PCA0CPL0	PCA0CPH0	PCA0CPL4	PCA0CPH4	VDM0CN
F0	B	P0MDIN	P1MDIN	P2MDIN	P3MDIN		EIP1	
E8	ADC0CN	PCA0CPL1	PCA0CPH1	PCA0CPL2	PCA0CPH2	PCA0CPL3	PCA0CPH3	RSTSRC
E0	ACC	XBR0	XBR1		IT01CF		EIE1	
D8	PCA0CN	PCA0MD	PCA0CPM0	PCA0CPM1	PCA0CPM2	PCA0CPM3	PCA0CPM4	
D0	PSW	REF0CN			P0SKIP	P1SKIP	P2SKIP	
C8	TMR2CN		TMR2RLL	TMR2RH	TMR2L	TMR2H		
C0	SMB0CN	SMB0CF	SMB0DAT	ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH	REG0CN
B8	IP		**AMX0N**	AMX0P	ADC0CF	ADC0L	ADC0H	
B0	P3	OSCXCN	OSCICN	OSCICL			**FLSCL**	**FLKEY**
A8	IE	CLKSEL	EMI0CN					
A0	P2	SPI0CFG	SPI0CKR	SPI0DAT	P0MDOUT	P1MDOUT	P2MDOUT	P3MDOUT
98	SCON0	SBUF0	CPT1CN	CPT0CN	CPT1MD	CPT0MD	CPT1MX	CPT0MX
90	P1	TMR3CN	TMR3RLL	TMR3RLH	TMR3L	TMR3H		
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	**PSCTL**
80	P0	SP	DPL	DPH		TOFFL	TOFFH	PCON
	0(8) Bit-Addressable	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)

C8051F310 Registers | **C8051T61x Registers** | **Registers with Bit Differences**

Figure 1. SFR Memory Map Differences

5. ADC and Temperature Sensor

The ADC peripheral is different between the two device families. The C8051F310 features a 10-bit, 200 ksps SAR, while the C8051T61x family has a 10-bit, 500 ksps SAR. A list of ADC differences that may affect the system and code design are detailed in Table 2.

Table 2. ADC and Temperature Sensor

Feature	C8051F310	C8051T61x
Output Word Resolution	10 bits	10 bits
Throughput (Sampling Rate)	200 ksps	500 ksps
Minimum Tracking Time	300 ns	300 ns
Conversion time in SAR clocks	10 Clocks	11 or 13 Clocks*
Maximum SAR Clock Speed	3 MHz	8.33 MHz
Gain Settings	1x	0.5x, 1x
Differential Inputs (AIN+ and AIN-)	Yes	No
Calibrated Temperature Sensor Offset	No	Yes
Voltage Reference (V_{REF}) Options	VDD, External Pin	VDD, External Pin, LDO Output

5.1. Analog Multiplexer and Gain Settings

The ADC on the C8051T61x contains a subset of the multiplexing features found on the C8051F310. On the C8051T61x, only the positive channel (AIN+) of the ADC is available, meaning that only single-ended measurements are possible (from AIN+ to GND). When developing code for the C8051T61x on the C8051F310, the five LSBs of the AMX0N register should always be written to 11111b (binary). This will select GND as the negative input on the C8051F310's ADC and perform a single-ended measurement. In addition to the 1x gain setting of the C8051F310's ADC, C8051F61x devices have a gain setting of 0.5x.

5.2. SAR Timing

During a conversion, the SAR ADC is normally in one of two different phases, "tracking" or "converting", as shown in Figure 2.

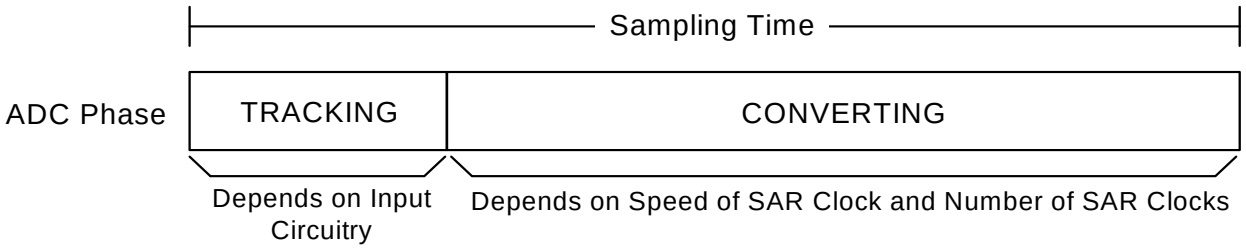


Figure 2. ADC Sampling Phases: Tracking and Converting

Establishing the same conversion time between the 'T61x and 'F31x requires programming the 'T61x to a faster SAR clock frequency. During the tracking phase, the ADC's sampling capacitor is connected to the external pin input through the analog multiplexer. When a conversion is initiated by the selected start-of-conversion source, the sampling capacitor is disconnected from the input, and the SAR conversion is performed. The number of SAR clocks required for the conversion phase in 10-bit mode on the C8051T61x is larger than the number required for the C8051F310. At a given SAR clock frequency, this leaves less of the total sampling time for tracking.

The ADC on both devices requires a minimum 300 ns tracking time before each conversion, and additional tracking time may be necessary depending on the nature of the front-end circuitry (see the "Settling Time Requirements" section of the data sheet for more details). Fortunately, the C8051T61x SAR can operate with a faster SAR clock than the C8051F310 to compensate for the extra SAR clocks needed to complete a 10-bit conversion and to provide comparable tracking/settling time at the same sampling rate. If the application requires the C8051T61x's SAR clock speed to be faster than the C8051F310 SAR clock specification, the switch to the faster SAR clock should be implemented as one of the final development steps after the majority of other code development is completed on the C8051F310.

5.3. Temperature Sensor

Use of the temperature sensor on the C8051T61x is very similar to that on the C8051F310. However, the transfer function of the two temperature sensors is different. Different values for the offset and slope of the temperature sensor are necessary to accurately calculate the temperature on each device family. Additionally, to help remove some of the error due to part-to-part variations, the C8051T61x temperature sensor output has been measured during production test for each device. The results of the measurement are stored in the registers, TOFFH and TOFFL. These register values represent the output of the temperature sensor at an ambient temperature of zero degrees Celsius as measured by the ADC, using the internal regulator as a reference voltage.

5.4. Voltage Reference Options

On the C8051F310, the ADC can use one of two different voltage reference options: the VDD supply pin or an external reference applied to the VREF pin. On the C8051T61x, an additional voltage reference option is available. By setting the REGOVR bit in the REF0CN register, the ADC can use the internal regulator as the voltage reference for the ADC.

5.5. External Conversion Start (CNVSTR) Timing

If the CNVSTR pin is used to begin conversions on the ADC, it is important to note the differences in timing between the C8051F310 and the C8051T61x family. On the C8051F310, the rising edge of CNVSTR always ends tracking mode and begins a conversion. On the C8051T61x family, when the AD0TM bit is set to “0”, conversions are initiated on the rising edge of CNVSTR, and tracking occurs when CNVSTR is low. On the C8051T61x, if AD0TM is set to “1”, tracking occurs any time a conversion is not in progress and lasts an additional three SAR clocks after the rising edge of CNVSTR.

6. Supply and I/O Pin Voltages

The C8051T61x is implemented in a different process technology than the C8051F31x. Consequently, there are some additional features and restrictions related to the supply voltage and allowable I/O pin voltages; these are detailed in Table 3.

Table 3. Supply and I/O Pin Voltages

Feature	C8051F310	C8051T61x
Supply Voltage Range	2.7–3.6 V	1.8–3.6 V
LDO Regulator for Internal Core Voltage	NO	YES
Maximum Voltage on any I/O Pin	5.8 V	V_{DD} + 3.6 V*
***Note:** Up to a maximum of 5.8 V		

The internal LDO regulator included on the C8051T61x family is used to regulate the V_{DD} supply voltage down to 1.7 V for the controller core. The regulated core voltage is only used internally. All external voltages and analog circuits on the device are powered from the V_{DD} voltage, so the I/O logic levels and the allowable ADC and comparator input ranges are all relative to V_{DD}. The LDO regulator can be bypassed if the external supply to the device is from a 1.8 V power source. The regulator output to the internal circuitry may also be turned off when the device enters Stop mode to conserve power.

6.1. In-System Code Development for Lower Voltage Systems (Below 2.7 V)

In a system that uses a 2.7–3.6 V supply voltage, the C8051F310 can be used as a substitute for the C8051T61x for in-system code development. However, if the supply voltage in the final system using the C8051T61x is less than 2.7 V, it may be necessary to add additional circuitry to the prototype board when using the C8051F310 to prevent damage to other devices in the system. Any required additional circuitry will be dictated by the specifications of the other circuits in the system:

1. If all of the other circuitry in the system can also operate at 2.7 V or higher, raising the supply voltage for the entire system during development is an easy solution.
2. If the other devices cannot operate at a higher supply voltage, but the I/O pins connected to the C8051F310 are tolerant of higher voltages, simply using a separate regulator for the C8051F310 may be an option.
3. If the I/O pins of the other devices in the system also cannot tolerate higher voltages, level-shifting circuitry may be necessary. An alternative to level shifters would be to use the C8051F310's outputs in open-drain mode with an external pull-up resistor to the lower supply voltage. Be aware that this will result in extra supply current on the C8051F310, as well as slower rise times of the C8051F310 output signals.

6.2. Special Considerations for Higher Voltage Systems (Above 3.6 V)

The C8051T61x devices can interface to logic levels that are higher than its supply voltage. However, special care must be taken in any system where the C8051T61x interfaces to logic that uses a supply voltage higher than 3.6 V. The C8051T61x I/O pins can only tolerate up to 3.6 V above the voltage present at the V_{DD} pin, or 5.8 V, whichever is lower. This means that when the device is powered off, and V_{DD} is 0 V, the maximum voltage on any I/O pin is 3.6 V. When VDD is 2.2 V or higher, the maximum voltage at any I/O pin is 5.8 V. It may be necessary to either control the order in which power supplies turn on in the system or add external protection circuitry to ensure that the pin voltages remain within tolerable limits at all times.

6.3. Regulator Control

The internal LDO regulator is an additional feature of the C8051T61x that is not found on the C8051F310. The special function register, REG0CN, is used to control some of the regulator's features. The REG0CN register is located at address 0xC7 in the C8051T61x devices. On the C8051F310, register location 0xC7 is not used, and it will not cause any harm to write to this location on a C8051F310 device. This allows the user to run code intended for a C8051T61x device on a C8051F310 device without modification.

If the V_{DD} supply voltage to the C8051T61x is regulated externally with a 1.8 V regulator, the internal regulator may be placed in bypass mode for power savings. The BYPASS bit in REG0CN can be set to “1” by firmware to use an external regulator. It is very important that the BYPASS function only be used if the external V_{DD} supply voltage is within the limits for “Voltage on V_{DD} / Regulator in Bypass Mode” specified in the “Absolute Maximum Ratings” table in the datasheet. The device will be damaged if bypass mode is used when V_{DD} is higher than this specification.

For slower clock frequencies (<2 MHz), the amount of current consumed by the device can be reduced by setting the Memory Power Control bit (MPCE) in register REG0CN to “1”. This setting allows the device to save power by only turning on the read buffers for the amount of time necessary to read the memory contents. Note that when this feature is enabled, the ADC should use a SAR clock divider of 2 or more for proper operation.

On the C8051T61x devices, there are two versions of Stop mode (as opposed to one on the C8051F31x). The normal Stop mode leaves the internal regulator on and is identical to the C8051F31x Stop mode in that any reset source will be accepted and bring the device back out of Stop mode. The contents of RAM are retained if the regulator is left on in Stop mode. However, for additional power savings, the output of the regulator may also be disabled when the device enters Stop mode. Writing a “1” to the STOPCF bit in the REG0CN register enables this feature. Only a reset initiated by the /RST pin or a power-on reset can wake the device from this mode. Note that the contents of RAM are lost if this option is used since power to the internal RAM is supplied by the regulator.

6.4. VDD Monitor/Brown-Out Detector

The VDD monitor on the C8051T61x behaves in the same way as the VDD monitor for the C8051F310, with two exceptions. The C8051F310’s VDD monitor threshold is set to operate below 2.7 V, while the C8051T61x’s VDD monitor threshold is set to operate below 1.8 V. The VDD monitor on the C8051F310 is disabled by default, and the VDD monitors on the C8051F61x devices are enabled by default.

7. Clocking Options

The clocking options on the C8051T61x are very similar to those offered on the C8051F310. The only exception, as shown in Table 4, is that the C8051F310 includes an external crystal oscillator option, which is not available on the C8051T61x.

Table 4. Clocking Options

Feature	C8051F310	C8051T61x
Internal Calibrated 24.5 MHz Oscillator (divided by 1, 2, 4, or 8)	YES	YES
External CMOS clock (digital input)	YES	YES
External Oscillator in RC or Capacitor Mode	YES	YES
External Oscillator in Crystal Oscillator Mode	YES	NO

Because the external crystal oscillator option is not offered on the C8051T61x, any port of an existing C8051F310 design that relies on the precision of a crystal oscillator should be modified to use an external CMOS oscillator instead.

8. Other Peripherals

All other peripherals and features not discussed in the previous sections are functionally the same between the two device families. Code written for these peripherals will operate the same way on either device family; so, there are no special considerations when developing code for the other peripherals.

9. Code Example

A simple code example highlighting some of the differences in the ADC modules between the C8051F310 and the C8051T61x is included in this section. In the code example, the ADC is configured to read the temperature sensor, average a number of samples, and calculate the temperature from the result in tenths of a degree Celsius. The main differences to be noted are in the setup of the ADC and the calculation of temperature from the ADC result. Some portions of code are conditionally compiled based on the processor being used. There are two definitions for the processor selection: C8051F310 and C8051T610. The code can be compiled for either processor by commenting out the opposite processor's definition.

To compile for the C8051F310:

```
#define C8051F310
//#define C8051T610
```

To compile for the C8051T610:

```
//#define C8051F310
#define C8051T610
```

There are only two places in code that use the above constants to conditionally compile code. These are in the ADC and VREF setup routine and in the precompiler definitions for the temperature sensor offset and slope values.

9.1. ADC and VREF Setup Differences

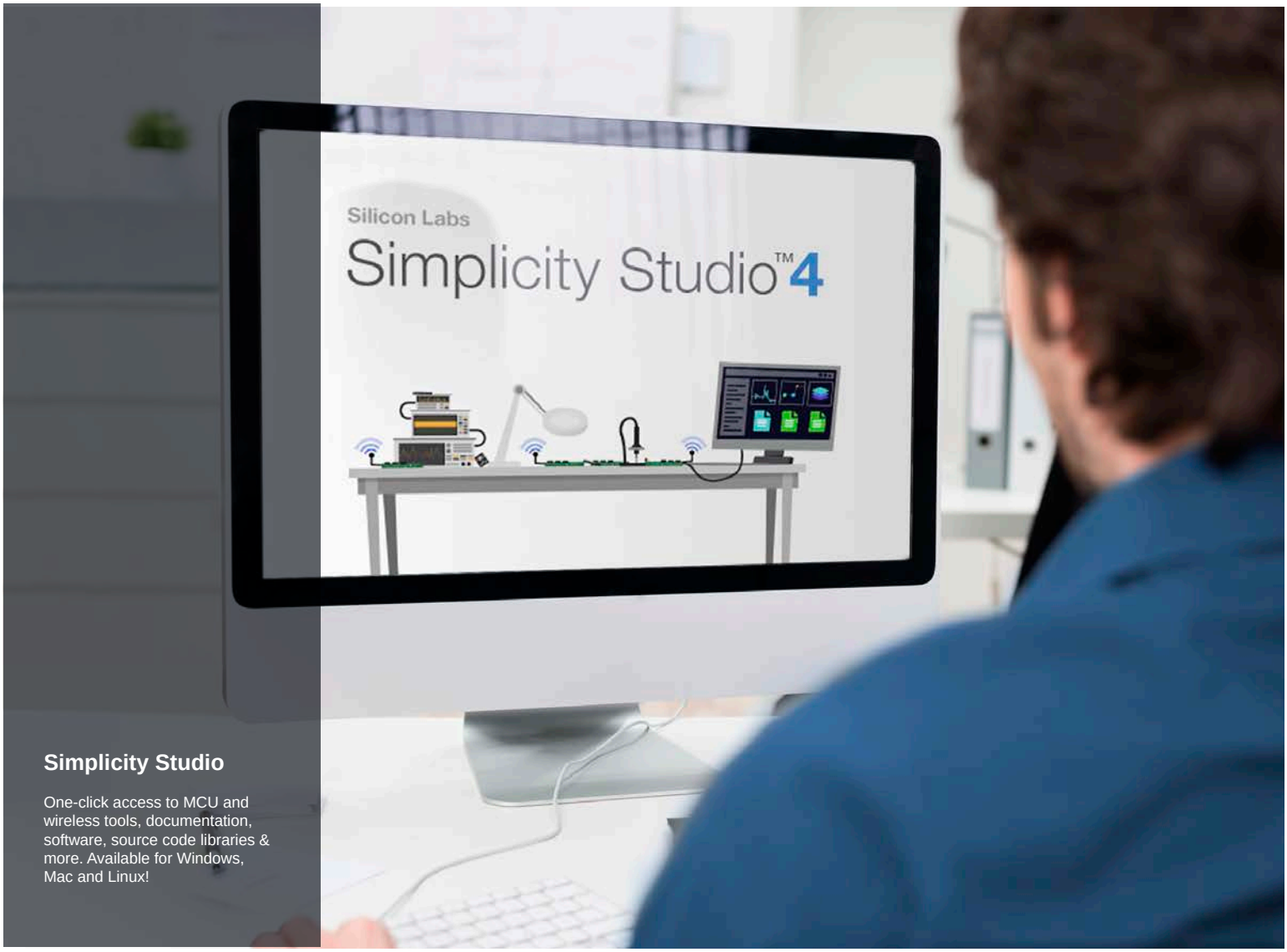
On the C8051F310, the VDD supply is used as the ADC's voltage reference. It is assumed that the code is running on a board that supplies 3.3 V for the VDD supply.

In the C8051T61x family of devices, the temperature sensor offset at 0 °C has been calculated in production test under the condition that the ADC is using the internal 1.8 V regulator as VREF and the 1x gain range. This value is stored in the TOFFH and TOFFL registers in the C8051T61x devices. To take advantage of this premeasured temperature sensor value, the internal 1.8 V regulated supply is used as the voltage reference, and the 1x gain range is used. Thus, the input range for the ADC on the C8051T61x is 0 to 1.8 V.

9.2. Temperature Calculation Differences

The C8051F310 and C8051T61x temperature sensors have slightly different characteristics for offset and slope. When compiling the source code for the C8051F310, the offset and slope values are calculated by the precompiler and stored as constants. When compiling the source code for the C8051T61x, the slope value is calculated and stored as a constant, but the offset value is read from the TOFFH and TOFFL registers.

In both cases, the offset value used by the code represents the output of the ADC when measuring the temperature sensor at 0 °C, to an accuracy of 10 bits. The slope value used by the code represents the temperature sensor slope per 100 °C, also assuming a 10-bit ADC output word.



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