DIFFERENCES BETWEEN THE C8051F33X AND THE C8051T63X DEVICE FAMILIES

1. Introduction

The C8051T63x devices are low-cost, electrically-programmable read-only memory (EPROM) microcontrollers based on the Silicon Laboratories CIP-51 microcontroller core. As with Silicon Laboratories' C8051F-series Flash-based microcontrollers, the C8051T63x are highly-integrated, mixed-signal devices incorporating communication peripherals as well as analog-to-digital converter (ADC) technology. Also included is the C2 2-wire debugging and programming interface, allowing designers to rapidly develop and debug firmware.

Because the devices in the C8051T63x family cannot be erased, a new device is required for testing every time the firmware changes. This could make the code development process more difficult and time consuming. Fortunately, the features found in the C8051T63x family are closely related to the features of two other Flash-based device families: the C8051F330-5, and the C8051F336-9. The most closely-related of these devices is the C8051F336, which is included on an "emulation daughter card" in the C8051T630-DK. In most cases, the C8051F336 can be used for the entire code development process, and the firmware image will be interchangeable between the two device families. For systems that take advantage of the additional features found in the C8051T63x family, the majority of the firmware can still be developed on the C8051F336 device and then ported to the C8051T63x during the final stages of code development.

This document details the hardware differences between the EPROM and Flash device families and provides some guidelines for using the C8051F336 to develop code for the C8051T63x.

2. Key Points

- Although the majority of device features are identical between the C8051F330–5, the C8051F336–9, and the C8051T63x, there are some hardware differences.
- When developing code for the C8051T63x device family, the majority of the code development process can be done on one of the Flash-based counterparts, and the C8051F336 is the closest Flash-based relative.
- Each device family has a set of unique features that are not present on the other families. Recognizing these differences is the key to successfully developing common code (code that works across all families) or code that uses some of the additional features found on the C8051T63x.

3. Special Function Registers

The special function register (SFR) memory map of the C8051T63x is very similar to the SFR memory map of the C8051F336-9 and the C8051F330-5. However, there are a few differences related to functionality and features found on only certain devices. Fortunately, SFRs that exist in one family but not another can be safely written and read on the other devices without causing a problem. Likewise, certain registers have additional bits defined that are not present on all devices. In these cases, the default bit settings are safe to write, and the read values of those bits are defined in the data sheet. Figure 1 shows the combined SFR map of these three device families. The locations of SFRs that differ between the families and those with only bitwise differences are highlighted.

F8	SPI0CN	PCA0L	PCA0H	PCA0CPL0	PCA0CPH0	P0MAT *3	P0MASK *3	VDM0CN
F0	B	P0MDIN	P1MDIN	P2MDIN *4			EIP1	PCA0PWM *3
E8	ADC0CN	PCA0CPL1	PCA0CPH1	PCA0CPL2	PCA0CPH2	P1MAT *3	P1MASK *3	RSTSRC
E0	ACC	XBR0	XBR1	OSCLCN	IT01CF		EIE1	SMB0ADM *3
D8	PCA0CN	PCA0MD	PCA0CPM 0	PCA0CPM 1	PCA0CPM 2			
D0	PSW	REF0CN *5			P0SKIP	P1SKIP	P2SKIP *4	SMB0ADR *3
C8	TMR2CN		TMR2RLL	TMR2RH	TMR2L	TMR2H		
C0	SMB0CN	SMB0CF	SMB0DAT	ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH	REG0CN *2
B8	IP	IDA0CN	AMX0N *1	AMX0P	ADC0CF *5	ADC0L	ADC0H	
B0		OSCXCN *5	OSCICN *5	OSCICL			FLSCL *1	FLKEY *1
A8	IE	CLKSEL	EMI0CN					
A0	P2	SPI0CFG	SPI0CKR	SPI0DAT	P0MDOUT	P1MDOUT	P2MDOUT	
98	SCON0	SBUF0		CPT0CN		CPT0MD		CPT0MX
90	P1	TMR3CN *5	TMR3RLL	TMR3RLH	TMR3L	TMR3H	IDA0L	IDA0H
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	PSCTL *1
80	P0	SP	DPL	DPH		TOFFL *2	TOFFH *2	PCON
	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)

Bit-Addressable

*1 C8051F33x Only	*3 C8051F336-9 C8051T60x Only	*5 Registers with Bit Differences Between Device Families
*2 C8051T61x Only	*4 C8051F336-9 Only	

Figure 1. SFR Memory Map Differences

4. Code Memory Storage

The most obvious difference between the C8051F33x and the C8051T63x devices is the code memory storage technology. On the C8051F33x devices, Flash memory is used, while on the C8051T63x devices, a byte-programmable EPROM code memory architecture is used. EPROM memory can be programmed one byte at a time, but cannot be erased. Table 1 details some parameters of interest related to the code storage technology.

Table 1. Code Memory Storage

Feature	C8051F33x	C8051T63x
Code memory can be erased and reprogrammed	Yes	No
Programming voltage (V_{PP}) required to program code memory	No	Yes
Code memory can be written or erased from firmware on the device	Yes	No
Code memory can be read from firmware on the device	Yes	

The impact of the code storage technology on the development of C8051T63x firmware is minimal. When developing firmware for the C8051T63x on the C8051F336 or porting an existing design from any C8051F33x device, make certain that there are no firmware routines intended to write or erase areas of code memory, as they will not have any effect on the C8051T63x.

5. ADC and Temperature Sensor

The ADC peripheral is different between the Flash and EPROM devices. The C8051F33x features a 10-bit, 200 ksps SAR, while the C8051T63x family has a 10-bit, 500 ksps SAR. A list of ADC differences that may affect the system and code design are detailed in Table 2.

Table 2. ADC and Temperature Sensor

Feature	C8051F33x	C8051T63x
Output Word Resolution	10 bits	10 bits
Throughput (Sampling Rate)	200 ksps	500 ksps
Minimum Tracking Time	300 ns	300 ns
Maximum SAR Clock Speed	3.125 MHz	8.33 MHz
Gain Settings	1x	0.5x, 1x
Differential Inputs (AIN+ and AIN-)	Yes	No
Calibrated Temperature Sensor Offset	No	Yes
Voltage Reference (V_{REF}) Options	VDD, External Pin, On-chip 2.4 V	VDD, External Pin, LDO Output, On-chip 2.4 V to 1.2 V

5.1. Analog Multiplexer and Gain Settings

The ADC on the C8051T63x contains a subset of the multiplexing features found on the C8051F33x. On the C8051T63x, only the positive channel (AIN+) of the ADC is available, meaning that only single-ended measurements are possible (from AIN+ to GND). When developing code for the C8051T63x on the C8051F33x, the five LSBs of the AMX0N register should always be written to 10001b (binary). This will select GND as the negative input on the C8051F33x's ADC and perform a single-ended measurement. In addition to the 1x gain setting of the C8051F33x's ADC, C8051T63x devices have a gain setting of 0.5x.

5.2. SAR Timing

During a conversion, the SAR ADC is normally in one of two different phases, “tracking” or “converting”, as shown in Figure 2.

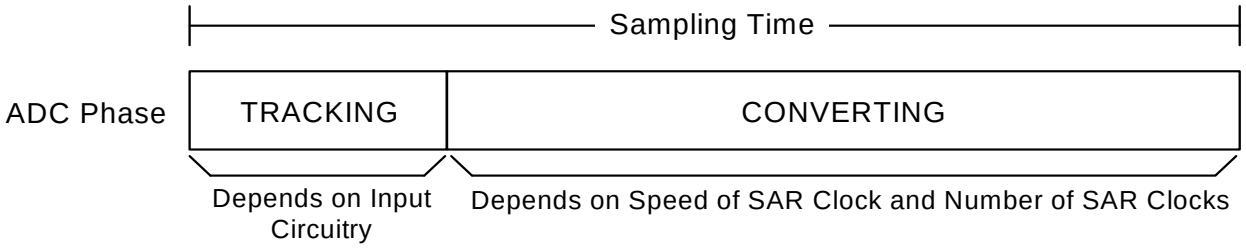


Figure 2. ADC Sampling Phases: Tracking and Converting

Establishing the faster conversion rate available on the 'T63x requires programming the 'T63x to a faster SAR clock frequency. During the tracking phase, the ADC's sampling capacitor is connected to the external pin input through the analog multiplexer. When a conversion is initiated by the selected start-of-conversion source, the sampling capacitor is disconnected from the input, and the SAR conversion is performed. To speed up the conversion time and allow enough tracking time, the SAR clock must be set to a higher rate.

The ADC on both devices requires a minimum 300 ns tracking time before each conversion, and additional tracking time may be necessary depending on the nature of the front-end circuitry (see the “Settling Time Requirements” section of the data sheet for more details). The C8051T63x SAR can operate with a faster SAR clock than the C8051F33x to accommodate the higher sampling rate available. If the application requires the C8051T63x's SAR clock speed to be faster than the C8051F33x SAR clock specification, the switch to the faster SAR clock should be implemented as one of the final development steps after the majority of other code development is completed on the C8051F33x.

5.3. Temperature Sensor

Use of the temperature sensor on the C8051T63x is very similar to that on the C8051F33x. However, the transfer function of the temperature sensors on each device family is different. Different values for the offset and slope of the temperature sensor are necessary to accurately calculate the temperature on each device family. Additionally, to help remove some of the error due to part-to-part variations, the C8051T63x temperature sensor output has been measured during production test for each device. The results of the measurement are stored in the registers, TOFFH and TOFFL. These register values represent the output of the temperature sensor at an ambient temperature of zero degrees Celsius, if measured with the ADC using the internal regulator as a reference voltage.

5.4. Voltage Reference Options

On the C8051F33x, the ADC can use one of three different voltage reference options: the VDD supply pin, an external reference applied to the VREF pin, or the on-chip 2.4 V reference voltage routed to the VREF pin. On the C8051T63x, two additional voltage reference options are available. By setting the REGOVR bit in the REF0CN register, the ADC can use the internal regulator as the voltage reference for the ADC. If using the on-chip reference voltage generator, the REFBGS bit can also be used to switch between 1.2 V and 2.4 V.

5.5. External Conversion Start (CNVSTR) Timing

If the CNVSTR pin is used to begin conversions on the ADC, it is important to note the differences in timing between the C8051F33x and the C8051T63x family. On the C8051F33x, the rising edge of CNVSTR always ends tracking mode and begins a conversion. On the C8051T63x family, when the AD0TM bit is set to 0, conversions are initiated on the rising edge of CNVSTR, and tracking occurs when CNVSTR is low. On the C8051T63x, if AD0TM is set to 1, tracking occurs any time a conversion is not in progress and lasts an additional three SAR clocks after the rising edge of CNVSTR.

6. Supply and I/O Pin Voltages

The C8051T63x is implemented in a different process technology than the C8051F33x. Consequently, there are some additional features and restrictions related to the supply voltage and allowable I/O pin voltages; these are detailed in Table 3.

Table 3. Supply and I/O Pin Voltages

Feature	C8051F33x	C8051T63x
Supply Voltage Range	2.7–3.6 V	1.8–3.6 V
LDO Regulator for Internal Core Voltage	NO	YES
Maximum Voltage on any I/O Pin	5.8 V	V_{DD} + 3.6 V*
***Note:** Up to a maximum of 5.8 V		

The internal LDO regulator included on the C8051T63x family is used to regulate the V_{DD} supply voltage down to 1.7 V for the controller core. The regulated core voltage is only used internally. All external voltages and analog circuits on the device are powered from the V_{DD} voltage, so the I/O logic levels and the allowable ADC and comparator input ranges are all relative to V_{DD}. The LDO regulator can be bypassed if the external supply to the device is from a 1.8 V power source. The regulator output to the internal circuitry may also be turned off when the device enters Stop mode to conserve power.

6.1. In-System Code Development for Lower Voltage Systems (Below 2.7 V)

In a system that uses a 2.7–3.6 V supply voltage, the C8051F33x can be used as a substitute for the C8051T63x for in-system code development. However, if the supply voltage in the final system using the C8051T63x is less than 2.7 V, it may be necessary to add additional circuitry to the prototype board when using the C8051F33x to prevent damage to other devices in the system. Any required additional circuitry will be dictated by the specifications of the other circuits in the system:

1. If all of the other circuitry in the system can also operate at 2.7 V or higher, raising the supply voltage for the entire system during development is an easy solution.
2. If the other devices cannot operate at a higher supply voltage, but the I/O pins connected to the C8051F33x are tolerant of higher voltages, simply using a separate regulator for the C8051F33x may be an option.
3. If the I/O pins of the other devices in the system also cannot tolerate higher voltages, level-shifting circuitry may be necessary. An alternative to level shifters would be to use the C8051F33x's outputs in open-drain mode with an external pull-up resistor to the lower supply voltage. Be aware that this will result in extra supply current on the C8051F33x, as well as slower rise times of the C8051F33x output signals.

6.2. Special Considerations for Higher Voltage Systems (Above 3.6 V)

The C8051T63x devices can interface to logic levels that are higher than its supply voltage. However, special care must be taken in any system where the C8051T63x interfaces to logic that uses a supply voltage higher than 3.6 V. The C8051T63x I/O pins can only tolerate up to 3.6 V above the voltage present at the V_{DD} pin, or 5.8 V, whichever is lower. This means that when the device is powered off, and V_{DD} is 0 V, the maximum voltage on any I/O pin is 3.6 V. When VDD is 2.2 V or higher, the maximum voltage at any I/O pin is 5.8 V. It may be necessary to either control the order in which power supplies turn on in the system or add external protection circuitry to ensure that the pin voltages remain within tolerable limits at all times.

6.3. Regulator Control

The internal LDO regulator is an additional feature of the C8051T63x that is not found on the C8051F33x. The special function register, REG0CN, is used to control some of the regulator's features. The REG0CN register is located at address 0xC7 in the C8051T63x devices. On the C8051F33x, register location 0xC7 is not used, and it will not cause any harm or malfunction to write to this location on a C8051F33x device. This allows the user to run code intended for a C8051T63x device on a C8051F33x device without modification.

If the V_{DD} supply voltage to the C8051T63x is regulated externally with a 1.8 V regulator, the internal regulator may be placed in bypass mode for power savings. The BYPASS bit in REG0CN can be set to 1 by firmware to use an external regulator. It is very important that the BYPASS function only be used if the external V_{DD} supply voltage is within the limits for "Voltage on V_{DD} / Regulator in Bypass Mode" specified in the "Absolute Maximum Ratings" table in the datasheet. The device will be damaged if bypass mode is used when V_{DD} is higher than this specification.

For slower clock frequencies (<2 MHz), the amount of current consumed by the device can be reduced by setting the Memory Power Control bit (MPCE) in register REG0CN to 1. This setting allows the device to save power by only turning on the read buffers for the amount of time necessary to read the memory contents. Note that when this feature is enabled, the ADC should use a SAR clock divider of 2 or more for proper operation.

On the C8051T63x devices, there are two versions of Stop mode (as opposed to one on the C8051F33x). The normal Stop mode leaves the internal regulator on and is identical to the C8051F33x Stop mode in that any reset source will be accepted and bring the device back out of Stop mode. The contents of RAM are retained if the regulator is left on in Stop mode. However, for additional power savings, the output of the regulator may also be disabled when the device enters Stop mode. Writing a 1 to the STOPCF bit in the REG0CN register enables this feature. Only a reset initiated by the /RST pin or a power-on reset can wake the device from this mode. Note that the contents of RAM are lost if this option is used since power to the internal RAM is supplied by the regulator.

6.4. VDD Monitor/Brown-Out Detector

The VDD monitor behaves in the same way across device families, but the state of the VDD monitor out of a power-on reset is different between device families, and the voltage level at which the VDD monitor trips is lower on the EPROM devices. Details of these differences are shown in Table 4.

Table 4. VDD Monitor Differences

Parameter	C8051F330-5	C8051F336-9	C8051T63x
Upper VDD Monitor Threshold	2.7 V	2.7 V	1.8 V
VDD Monitor ON after Power-on Reset	NO	YES	YES

7. Suspend Mode and Related Features

The C8051T63x and C8051F336-9 device families have one additional power-saving mode, named suspend mode, which is not available on the C8051F330-5 devices. The suspend mode on these devices is a function of the internal 24.5 MHz oscillator, and is entered by setting the SUSPEND bit in the OSCICN register to '1'. When placed into suspend mode, the 24.5 MHz oscillator reverts to a very low-power state where it is no longer oscillating, but can wake quickly and begin clocking the device again on three different events. One wake-up event is the new port match feature, which allows the device to wake on specified logic states of Port 0 and Port 1 pins. If Timer 3 is running from an external oscillator source or the internal low-frequency oscillator, a Timer 3 overflow can also wake the device from suspend mode. The final suspend wake event is a logic low output from Comparator 0.

The C8051F330-5 devices do not implement the oscillator suspend feature, the port match feature, or the ability to run Timer 3 from the internal low-frequency oscillator.

8. Clocking Options

The clocking options on the C8051T63x are very similar to those offered on the C8051F33x. The only exception, as shown in Table 5, is that the C8051F33x includes an external crystal oscillator option, which is not available on the C8051T63x.

Table 5. Clocking Options

Feature	C8051F33x	C8051T63x
Internal Calibrated 24.5 MHz Oscillator (divided by 1, 2, 4, or 8)	YES	YES
Internal 80 kHz Oscillator (divided by 1, 2, 4, or 8)	YES	YES
External CMOS clock (digital input)	YES	YES
External Oscillator in RC or Capacitor Mode	YES	YES
External Oscillator in Crystal Oscillator Mode	YES	NO

Because the external crystal oscillator option is not offered on the C8051T63x, any port of an existing C8051F33x design that relies on the precision of a crystal oscillator should be modified to use an external CMOS oscillator instead.

9. SMBus, PCA, and Timer 3

The C8051T63x and C8051F336-9 device families also implement some digital peripheral enhancements not found on the C8051F330-5 device family. Specifically, the SMBus, PCA, and Timer 3 peripherals all have additional features.

The SMBus peripheral additions are an optional hardware address recognition and automatic ACK feature, using the SMB0ADR and SMB0ADM registers. Using these features, the firmware required to handle SMBus transfers is reduced, and the software overhead associated with accepting or rejecting slave addresses is eliminated.

The PCA enhancements include more options for PWM generation, using the PCA0PWM register. In addition to the standard 8 or 16-bit PWM options found on the C8051F330-5 family, the C8051T63x and C8051F336-9 families include 9, 10, and 11-bit PWM options in hardware.

Timer 3 has also been enhanced on the C8051T63x and C8051F336-9 families. It supports operation from the internal low-frequency oscillator while the device is running from a different clock. If Timer 3 is configured to run from the external oscillator circuit or from the internal low-frequency oscillator, it will continue to run if the 24.5 MHz oscillator is placed in suspend, and the overflow can be used as a wake-up source for the device.

All of these enhancements are backwards-compatible, meaning that code written to operate on the C8051F330-5 family will work the same way on the C8051T63x or C8051F336-9 families.

10. Other Peripherals

All other peripherals and features not discussed in the previous sections are functionally the same between these device families. Code written for these peripherals will operate the same way on all device families, so there are no special considerations when developing code to utilize the other features.

11. Code Example

A simple code example highlighting some of the differences in the ADC modules between the C8051F33x and the C8051T63x is included in this section. In the code example, the ADC is configured to read the temperature sensor, average a number of samples, and calculate the temperature from the result in tenths of a degree Celsius. The main differences to be noted are in the setup of the ADC and the calculation of temperature from the ADC result. Some portions of code are conditionally compiled based on the processor being used. There are two definitions for the processor selection: C8051F336 and C8051T630. The code can be compiled for either processor by commenting out the opposite processor's definition.

To compile for the C8051F336:

```
#define C8051F336
//#define C8051T630
```

To compile for the C8051T630:

```
//#define C8051F336
#define C8051T630
```

There are only two places in code that use the above constants to conditionally compile code. These are in the ADC and VREF setup routine and in the precompiler definitions for the temperature sensor offset and slope values.

11.1. ADC and VREF Setup Differences

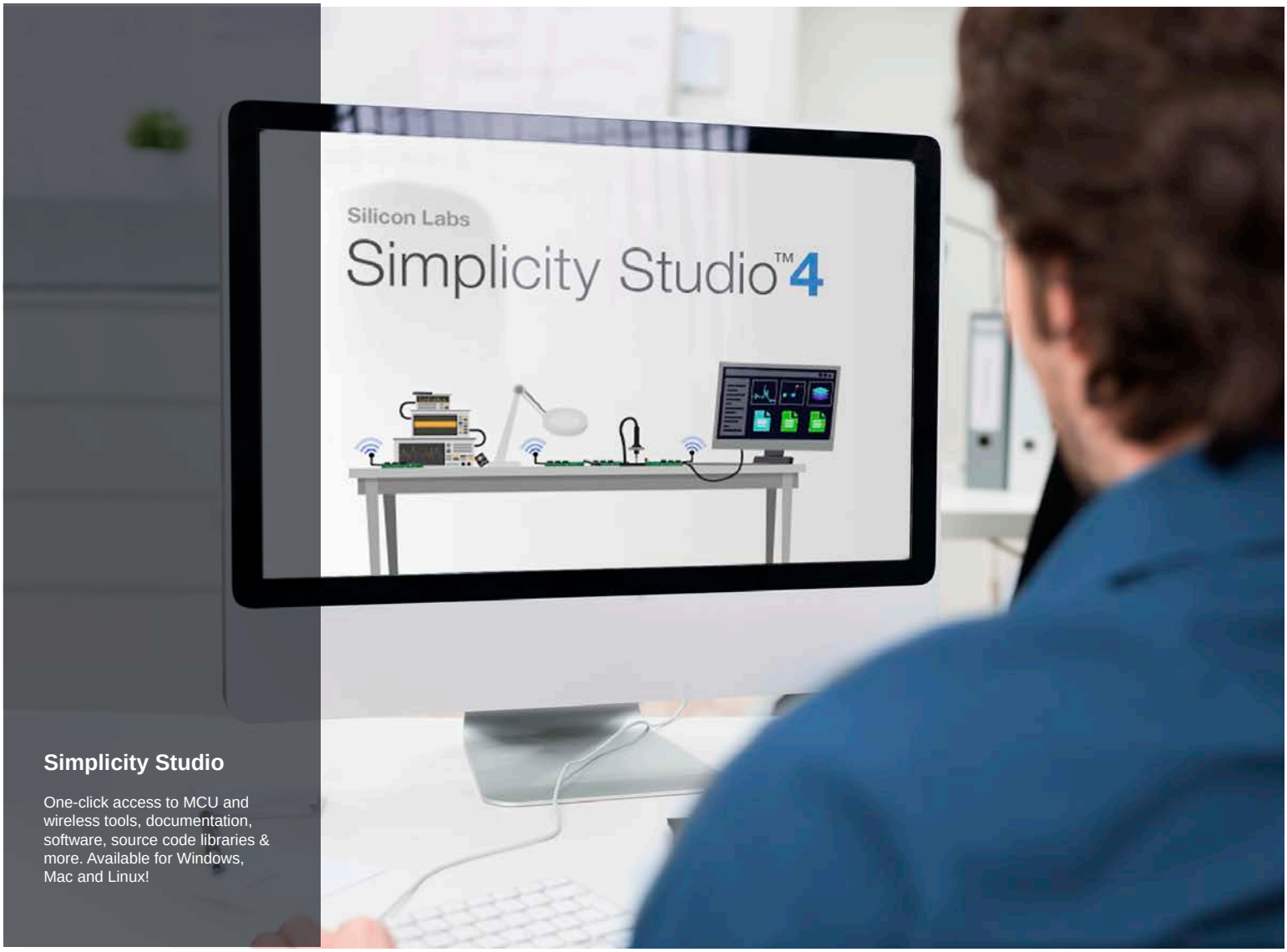
On the C8051F336, the VDD supply is used as the ADC's voltage reference. It is assumed that the code is running on a board that supplies 3.3 V for the VDD supply.

In the C8051T63x family of devices, the temperature sensor offset at 0 °C has been calculated in production test under the condition that the ADC is using the internal 1.8 V regulator as VREF and the 1x gain range. This value is stored in the TOFFH and TOFFL registers in the C8051T63x devices. To take advantage of this pre-measured temperature sensor offset value, the internal 1.8 V regulated supply is used as the voltage reference, and the 1x gain range is used. Thus, the input range for the ADC on the C8051T63x is 0 to 1.8 V.

11.2. Temperature Calculation Differences

The C8051F336 and C8051T63x temperature sensors have slightly different characteristics for offset and slope. When compiling the source code for the C8051F336, the offset and slope values are calculated by the precompiler and stored as constants. When compiling the source code for the C8051T63x, the slope value is calculated and stored as a constant, but the offset value is read from the TOFFH and TOFFL registers.

In both cases, the offset value used by the code represents the output of the ADC when measuring the temperature sensor at 0 °C, to an accuracy of 10 bits. The slope value used by the code represents the temperature sensor slope per 100 °C, also assuming a 10-bit ADC output word.



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