Si4030/4031/4430/4431 PA MATCHING

1. Introduction

This application note provides a description of the matching of the power amplifier (PA) on the Si4030/4031/4430/4431 family of RFICs. (As these chips do not differ in the design and functionality of the PA, the remainder of this document will refer to the Si4431 as representative of the entire group.) Specifically, this document does not address the matching procedure for the PA on the Si4032/4432 RFIC. Since the output power level on the Si4032/4432 RFIC is considerably higher than the Si4431 RFIC, the matching procedure is somewhat different.

We wish to simultaneously achieve several goals with the matching network:

- Maximize RF output power
- Minimize current consumption (i.e., maximize efficiency)
- Constrain the peak voltage at the drain of the output devices
- Comply with ETSI and FCC specifications for spurious emissions

The matching procedure outlined in this document will allow for achieving the above-listed goals and is applicable for two different types of board configurations: one with separate antennas for the TX and RX paths and one with a single antenna and with the TX and RX paths tied directly together (without use of an RF switch). The differences in the matching procedure required for the two board configurations are discussed in detail.

Tables 1, 2, and 3 are provided for users more interested in quickly obtaining matching component values than in the methodology used to develop the matching network. The component values shown in these tables are appropriate for a supply voltage of V_{DD} = 3.3 V; the value of resistor R_{DC} will require modification if other supply voltages are used. Refer to "3.3.4. Step #4: Calculate the Required Value for Voltage-Limiting Resistor RDC" on page 13 for further details on the calculation of the value of R_{DC}.

1.1. Brief Overview of Matching Procedure

This application note discusses the matching philosophy and procedure for the Si4431 RFIC in great detail. However, some users may be interested in quickly gaining a high-level overview of the procedure before getting into the fine details. For those readers, the main points of the matching procedure are summarized below:

- Choose L_{CHOKE} (pull-up inductor) for high impedance at Fo
- Calculate required value of Z_{LOAD}, given Fo
- Calculate required value of R_{DC}, given V_{DD} and desired output power
- Choose value for C_0 (series capacitor)
- Calculate L_0 (series inductor) and required matching component values L_X and C_X
- Design a Chebyshev LPF (for attenuation of harmonics)

1.2. Summary of Matching Network Component Values

Some users are not greatly interested in the theoretical development of the matching network; rather, they are concerned with quickly obtaining a set of component values for a given desired frequency of operation. For those users, the resulting component values for the PA matching network for multiple frequencies across the operating range of the Si4431 RFIC are summarized in this section.

The matching networks may be realized with either wire-wound SMD inductors or with multi-layer SMD inductors. The cost of a multi-layer inductor is significantly lower than that of a wire-wound inductor, and thus in cost sensitive applications the multi-layer solution is preferred. However, a circuit realization using only multi-layer SMD inductors is more challenging, especially for the Direct Tie solution.

The primary reason is that multi-layer SMD inductors are often available only in coarser-spaced inductance values. In a Direct Tie solution, it is necessary to perform fine adjustments of the value of L0 in order to avoid degradation to RX sensitivity; this may be more difficult with only the set of values available for a multi-layer series of inductors. In such a case, the target value of L0 may be realized by using two series-connected multi-layer inductors of the appropriate values; this often remains a cheaper solution than one single wire-wound inductor.

A secondary issue with multi-layer inductors is the increased loss; they tend to have lower Qs and greater ohmic losses than wire-wound inductors of equivalent value. Fortunately, in most cases the resulting degradation in output power may be compensated by an appropriate modification in value of resistor R_{DC}. This effect may be observed in the tables below. In the case of a Split TX/RX board configuration, this is the only difference in component values between the wire-wound inductor realization and the multi-layer inductor realization. However, due to the increased loss, a realization using multi-layer inductors typically exhibits a slight increase in current consumption for the same amount of output power.

1.2.1. Component Values for Split TX/RX Board Configuration (V_{DD} = 3.3 V)

Table 1 provides the component values required for the Split TX/RX board configuration shown in Figure 1 for a supply voltage of V_{DD} = 3.3 V. Two possible values for resistor R_{DC} are provided, depending upon whether wire-wound or multi-layer inductors are used in the circuit realization. The value of R_{DC} is the only difference between the wire-wound and multi-layer realizations, except at 315 MHz where the value of pull-up inductor L_{CHOKE} must be chosen as 270 nH; this is the largest value of inductance available in a multi-layer inductor series in 0603-size. Also, the maximum allowed output power in the Japanese 950 MHz band is +10 dBm; for this reason, the output power state of the Si4431 RFIC is commanded to txpow[2:0]=3'b110 and the value of R_{DC} is deliberately increased to target the lower output power level.

Table 1. Match Network Component Values vs. Frequency (Split TX/RX Board, V_{DD} = 3.3 V)

	R_{DC}										
Freq Band	**wire-wound**	**multi-layer**	**Lchoke**	**C0**	**L0**	**CM**	**LM**	**CM2**	**LM2**	**CM3**	**LM3**
315 MHz	110 Ω	68 Ω	390 nH	10 pF	68 nH	15 pF	22 nH	15 pF	0 Ω	N/F	0 Ω
434 MHz	68 Ω	47 Ω	220 nH	8.2 pF	39 nH	15 pF	22 nH	12 pF	18 nH	N/F	0 Ω
868 MHz	47 Ω	36 Ω	100 nH	4.3 pF	15 nH	8.2 pF	9.1 nH	3.6 pF	0 Ω	N/F	0 Ω
915 MHz	47 Ω	36 Ω	100 nH	4.7 pF	12 nH	5.1 pF	8.2 nH	3.9 pF	15 nH	3.9 pF	8.2 nH
950 MHz	120 Ω	100 Ω	100 nH	5.1 pF	12 nH	6.2 pF	7.5 nH	3.9 pF	12 nH	3.9 pF	7.5 nH

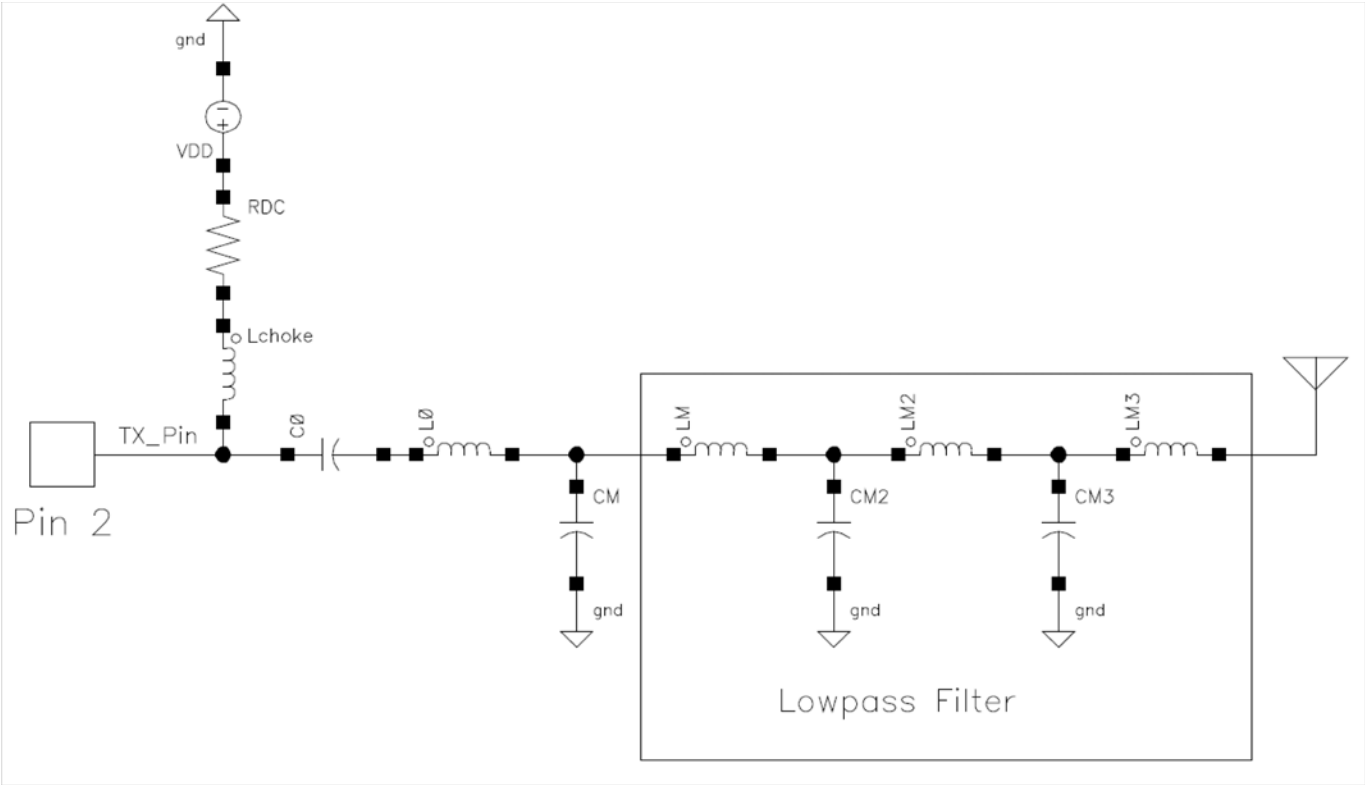

Figure 1. Matching Topology for Split TX/RX Board Configuration

1.2.2. Component Values for Direct Tie Board Configuration (V_{DD} = 3.3 V)

Table 2 provides the component values required for the Single Antenna with Direct Tie board configuration of Figure 2 for a supply voltage of V_{DD} = 3.3 V, assuming wire-wound inductors are used in the circuit realization. Table 3 provides the required component values assuming multi-layer inductors are used in the circuit realization.

Table 2. Match Network Component Values vs. Frequency (Direct Tie Board, Wire-Wound Inductors, V_{DD} = 3.3 V)

Freq Band	RX Side				TX Side									
	LR	LR2	CR1	CR2	RDC	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	LM3
315 MHz	68 nH	51 nH	6.0 pF	4.3 pF	110 Ω	270 nH	10.0 pF	68 nH	15.0 pF	22 nH	15.0 pF	0 Ω	N/F	0 Ω
434 MHz	33 nH	33 nH	8.2 pF	3.0 pF	68 Ω	220 nH	8.2 pF	39 nH	15.0 pF	22 nH	12.0 pF	18 nH	N/F	0 Ω
868 MHz	15 nH	15 nH	4.3 pF	2.2 pF	39 Ω	100 nH	4.3 pF	18 nH	6.0 pF	9.1 nH	3.6 pF	0 Ω	N/F	0 Ω
915 MHz	10 nH	9.1 nH	4.7 pF	2.2 pF	18 Ω	100 nH	3.9 pF	19 nH	4.3 pF	8.2 nH	4.3 pF	9.5 nH	3.3 pF	0 Ω
950 MHz	10 nH	11 nH	4.3 pF	2.2 pF	100 Ω	100 nH	5.1 pF	15 nH	4.3 pF	7.5 nH	3.9 pF	13 nH	3.9 pF	7.5 nH

Table 3. Match Network Component Values vs. Frequency (Direct Tie Board, Multilayer Inductors, V_{DD} = 3.3 V)

Freq Band	RX Side				TX Side									
	LR	LR2	CR1	CR2	RDC	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	LM3
315 MHz	68 nH	56 nH	6.0 pF	4.3 pF	110 Ω	270 nH	10.0 pF	68 nH	15.0 pF	22 nH	15.0 pF	0 Ω	N/F	0 Ω
434 MHz	33 nH	33 nH	8.2 pF	3.0 pF	68 Ω	220 nH	8.2 pF	39 nH	15.0 pF	22 nH	12.0 pF	18 nH	N/F	0 Ω
868 MHz	15 nH	15 nH	4.3 pF	2.2 pF	39 Ω	100 nH	4.3 pF	18 nH	6.0 pF	9.1 nH	3.6 pF	0 Ω	N/F	0 Ω
915 MHz	10 nH	9.1 nH	4.7 pF	2.2 pF	10 Ω	100 nH	3.9 pF	18 nH	4.3 pF	8.2 nH	4.3 pF	10 nH	3.3 pF	0 Ω
950 MHz	10 nH	10 nH	4.3 pF	2.2 pF	56 Ω	100 nH	5.1 pF	15 nH	4.3 pF	7.5 nH	3.9 pF	12 nH	3.9 pF	7.5 nH

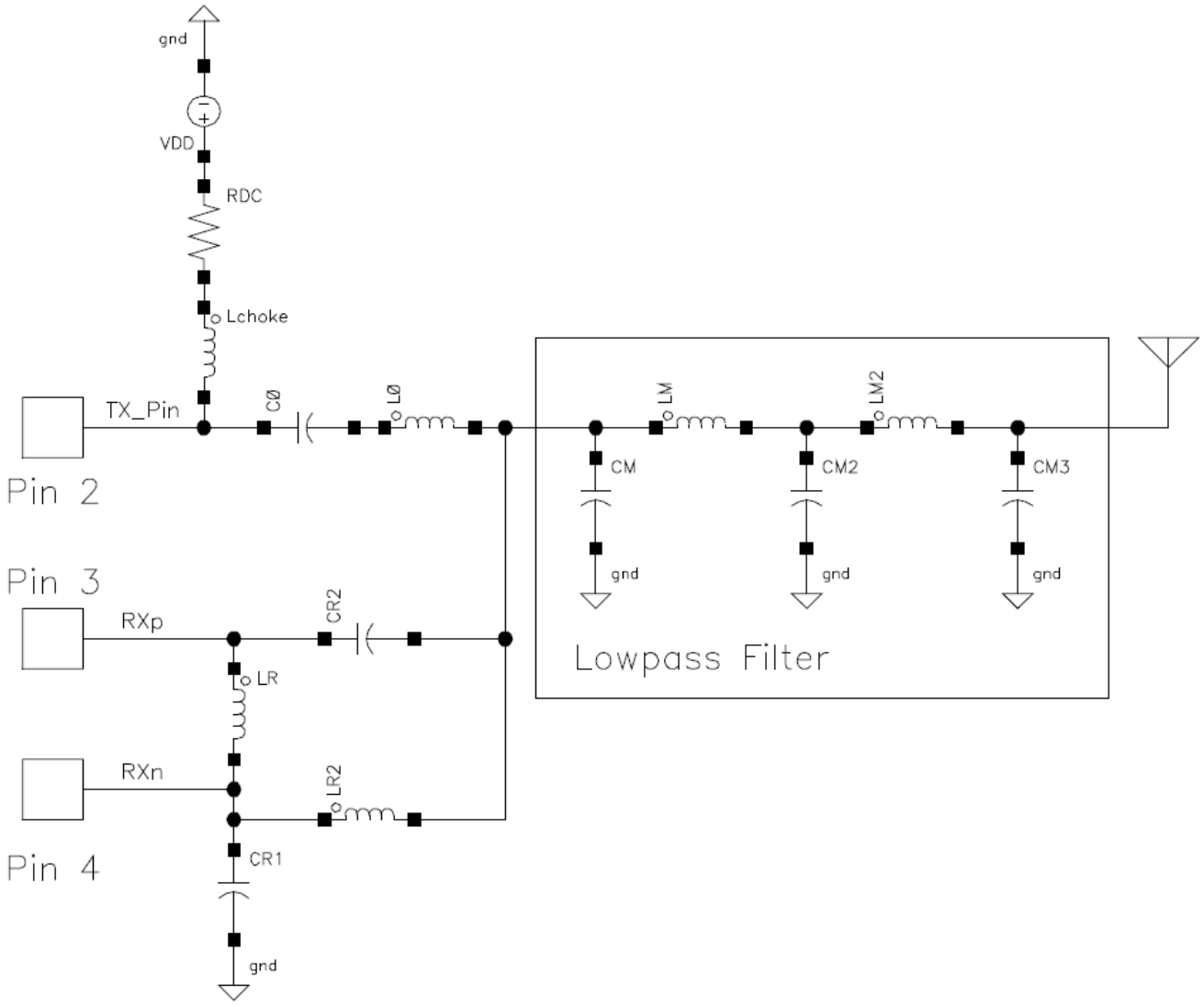

Figure 2. Matching Topology for Single Antenna with Direct Tie Board Configuration

Surface-mount 0603-size or 0402-size components themselves contain parasitic elements that modify their effective values at the frequency of interest. Furthermore, it is convenient to use the nearest-available 5% or 10% component values rather than the exact component values predicted by Filter Design CAD software or filter prototype tables. Additionally, any printed circuit board layout has parasitics, such as trace inductance, component pad capacitance, etc.

This means that it will almost certainly be necessary to “tweak” the final matching values for the reader’s specific application and board layout. The above component values should be used as starting points and the values modified slightly to zero-in on the best filter response and impedance match to 50 Ω.

The component values shown in Tables 1, 2, and 3 are appropriate when using 0402-size SMD components such as the 0402HP-series of wire-wound inductors from CoilCraft, the LQG15HS-series of multi-layer inductors from Murata, and the GRM15-series of ceramic capacitors from Murata. These values are appropriate for use on the official Split TX/RX and Direct Tie reference board designs available on the Silicon Labs website.

1.3. Summary of Measured Output Power and Current Consumption

A summary of typical measured output power and current consumption for various board configurations and circuit realizations is shown in Table 4 and Table 5. These results are obtained with the Si4431 chip commanded to its maximum output power state (txpow[2:0] = 3’b111) except for 950 MHz; in this band the Japanese ARIB regulatory standard allows a maximum output power level of +10 dBm, and the power state of the chip has therefore been reduced to txpow[2:0] = 3’b110. Also, at 315 MHz in the U.S. under FCC Part 15.231, the maximum allowed output power is approximately –20 dBm EIRP (Equivalent Isotropically Radiated Power). For this reason, the matching component values at 315 MHz have been deliberately adjusted to provide slightly lower output power (approximately +11 to +12 dBm), as indicated by the higher value of R_{DC}.

Also, for all results in a Direct Tie board configuration, the lna_sw bit in SPI Register 6Dh has also been set. Note that the efficiencies obtained with wire-wound inductor circuit realizations are generally better than for multi-layer inductors, and are quite close to those stated in the data sheet.

At all frequencies, the RX sensitivities achieved with the Direct Tie board configuration are within 2.5 dB of those obtained with the Split TX/RX board configuration.

Table 4. Output Power and Current Consumption vs. Frequency (Split TX/RX Board, V_{DD} = 3.3 V)

Freq Band	Wire-Wound Inductors		Multilayer Inductors	
	IDC (mA)	Pout (dBm)	IDC (mA)	Pout (dBm)
315 MHz	29.1 mA	12.10 dBm	29.80 mA	12.20 dBm
434 MHz	31.30 mA	13.40 dBm	34.10 mA	13.40 dBm
868 MHz	33.30 mA	13.60 dBm	32.90 mA	13.40 dBm
915 MHz	33.70 mA	13.80 dBm	35.20 mA	13.50 dBm
950 MHz	25.40 mA	10.40 dBm	26.90 mA	10.30 dBm

Table 5. Output Power and Current Consumption vs. Frequency (Direct Tie Board, V_{DD} = 3.3 V)

Freq Band	Wire-Wound Inductors		Multilayer Inductors	
	IDC (mA)	Pout (dBm)	IDC (mA)	Pout (dBm)
315 MHz	25.00 mA	11.20 dBm	26.10 mA	10.80 dBm
434 MHz	31.40 mA	13.10 dBm	33.00 mA	13.20 dBm
868 MHz	31.90 mA	13.40 dBm	33.60 mA	13.00 dBm
915 MHz	31.40 mA	12.70 dBm	35.70 mA	12.20 dBm
950 MHz	25.00 mA	9.20 dBm	28.20 mA	9.90 dBm

The results presented above assume a supply voltage of V_{DD} = 3.3 V. The specified supply voltage range of the Si4431 RFIC is between 1.8 and 3.6 V. The component match values shown in Tables 1, 2, and 3 will work well at supply voltages lower than V_{DD} = 3.3 V, but a reduction in output power will occur. It is possible to gain back this loss in output power by appropriate adjustment of the value of resistor R_{DC}. Conversely, if the supply voltage increases above 3.3 V it may be necessary to increase the value of R_{DC}. The formula for calculating the required value of R_{DC} as a function of supply voltage is given in Equation 8 in "3.3.4. Step #4: Calculate the Required Value for Voltage-Limiting Resistor RDC" on page 13.

2. Power Amplifier Circuit Description

RF design engineers are familiar with matching conventional (Class A/B/C) power amplifiers. In such cases, the matching procedure is relatively simple: provide a load impedance that is the complex conjugate of the output impedance of the PA. The reader may also employ Load Pull techniques in which a match is found that optimizes the output power but differs from the complex conjugate of the PA output impedance. In these conventional classes of power amplifiers, the output waveform ranges from a full 360 degree copy or reproduction of the driving waveform (e.g., Class A) to a partial (less than 360 degree) reproduction of the driving waveform (e.g., Class B or Class C).

However, the PA circuitry in the Si4431 RFIC differs considerably from such a conventional power amplifier. Specifically, the PA circuitry in the Si4431 is of a type known as a “switching power amplifier” or “switching power converter”. The matching procedure for such a class of PA is entirely different and may not be immediately intuitive.

2.1. Basic Switching PA Circuit Topology

At the very heart of a switching PA is a switch. In the Si4431, the switch is provided by an NMOS transistor in an open-drain configuration, sized to handle the current required for the specified output power.

Figure 3 shows the typical matching circuitry necessary to extract RF power from a switching amplifier. In very general terms, the value of the pull-up inductor “L_{CHOKE}” is chosen to be a very large impedance at the frequency of operation (and its nearest harmonics), while the series-resonant output tank (L_0-C_0) is chosen to resonate at the frequency of operation. The shunt capacitance “C_{SHUNT}” is required to store energy during the switching cycle. This shunt capacitance, along with the extra series inductance “L_X”, also works to tailor the time-domain shape of the output waveform. It is important to understand that in order to optimize the efficiency of a switching-type amplifier, it is necessary to control the time-domain shape of the output waveform.

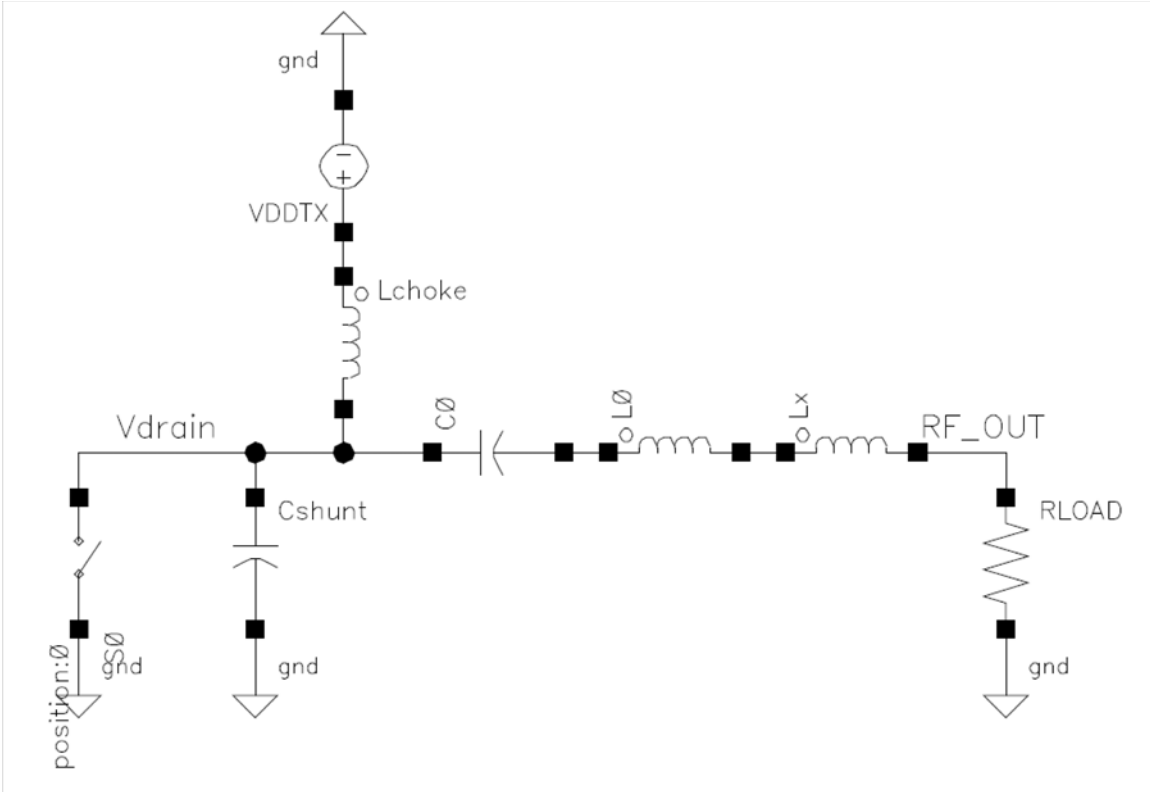

Figure 3. Basic Switching PA Circuit Topology

2.2. Theory of Operation of an Ideal Switching PA

So, exactly how does a switch “amplify” an RF signal? The simple answer is that it does not. After all, as long as the input control signal to the switch is sufficient to toggle the switch between its ON and OFF states, the output waveform will remain the same. Thus, the amount of output power delivered to the load resistance is independent of the amplitude of the input control signal (i.e., amplitude of the RF signal at the gate of the output MOS device). In such a case, defining the “gain” or amplification factor of the PA no longer has much meaning. Technically speaking, it is more correct to refer to this circuit as a “power converter” rather than a “power amplifier”.

So, if the circuit doesn’t amplify the internal RF input signal, then what determines the level of the output power?

In an ideal switching PA, the level of output power is dependent primarily upon two parameters: 1) the dc supply voltage and 2) the shunt capacitance. This statement is actually quite interesting because, theoretically, there is no limit to the amount of power we can extract from a switching PA. Higher levels of output power can be obtained by either increasing the supply voltage or by increasing the shunt capacitance at the switching output device.

Furthermore, in an ideal switching PA, it is theoretically possible to achieve 100% efficiency. This is a significant difference from conventional PAs. It is easily shown that the theoretical maximum efficiency of a Class-A PA is 50%, 78.5% for Class-B, and so on. However, in a switching PA, it is possible to tailor the output waveform such that the voltage across the switch is always zero during any period of time that the switch is conducting current, and the current conducted by the switch is always zero during any period of time that the voltage across the switch is non-zero. Thus the power dissipated by the switching device itself is zero, and, in the absence of any other losses in the circuit, the efficiency approaches 100%. The theoretical voltage waveform at the drain of a switching amplifier operated in Class-E is shown in Figure 4.

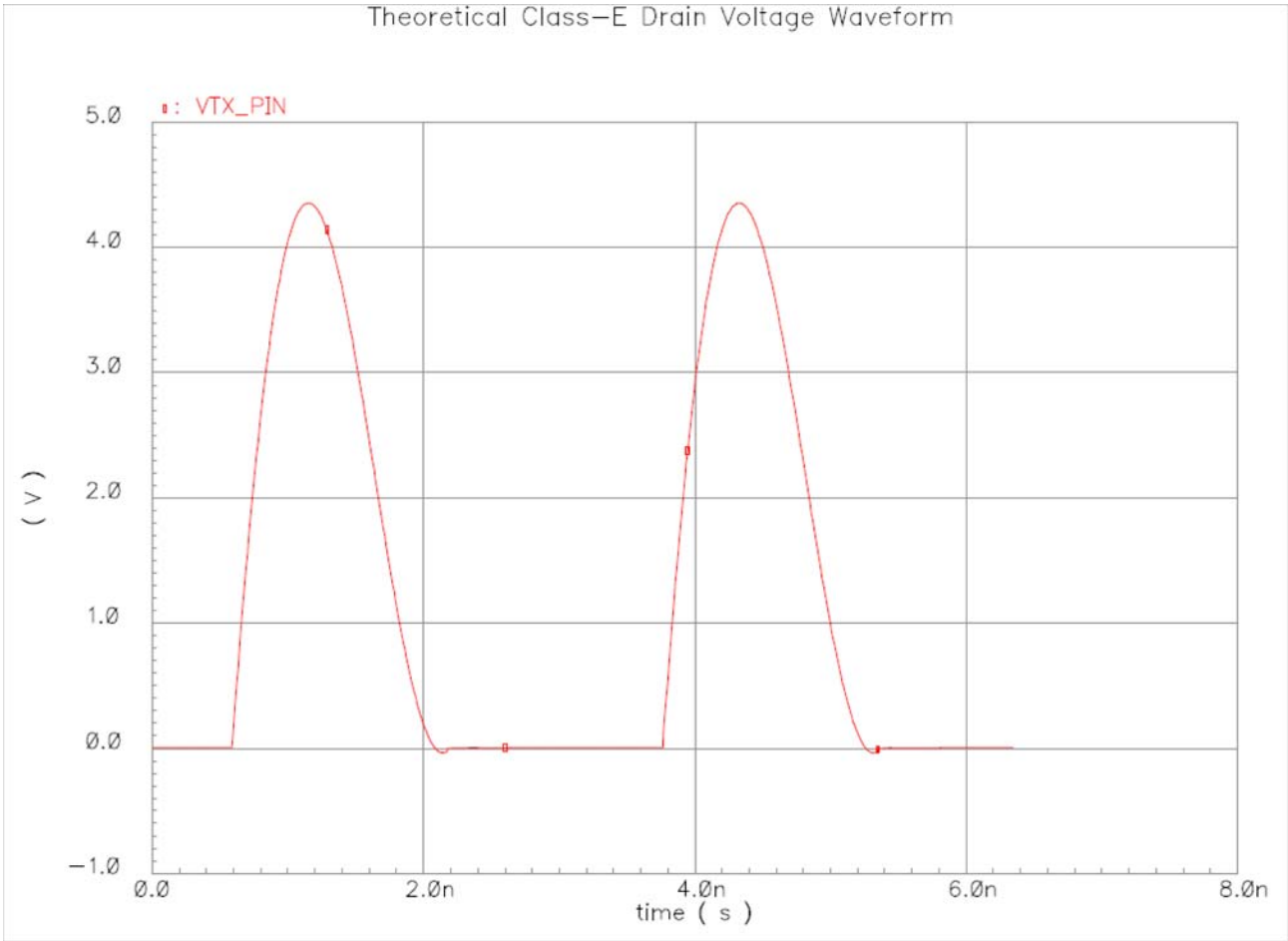

Figure 4. Theoretical Class-E Drain Voltage Waveform

For those interested in learning more about the theoretical operation of switching amplifiers (especially Class-E amplifiers), the following papers are recommended:

- Class E—A New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers, N. Sokal and A. Sokal, IEEE Journal of Solid State Circuits, Vol. SC-10, No. 3, June 1975.
- Idealized Operation of the Class-E Tuned Power Amplifier, F. Raab, IEEE Transactions on Circuits and Systems, Vol. CAS-24, No. 12, December 1977.

2.3. Limitations of a Practical MOS Switching PA

In practice, of course, we must live with several factors that prevent us from ever achieving “ideal” operation of the switching PA. These factors include the maximum operating voltage of the switch (i.e., MOS output device), the maximum current (limited by the size of the MOS output device), ON and OFF state resistances of the MOS output device, non-zero switching times of the MOS output device, and losses in the output matching components due to finite Qs. All of these factors combine to limit the achievable output power and efficiency.

The limitation on the maximum drain voltage of the MOS output device turns out to be a considerable constraint. RF design engineers may be quite familiar with the waveforms obtained with inductively-loaded conventional PAs where the peak output voltage reaches a value equal to twice the dc supply voltage. However, the peak of the output voltage waveform in a switching PA may far exceed this “$2xV_{DD}$” rule-of-thumb. As is shown in the papers listed above, the peak drain voltage for a Class-E switching amplifier can reach $3.56xV_{DD}$.

The operational range of supply voltage for the Si4431 RFIC is specified as V_{DD} = 1.8 to 3.6 V. It is apparent that if the switching PA circuit was matched for Class-E operation at V_{DD} = 3.6 V, the resulting peak drain voltage would reach 12.8 V peak. This exceeds the maximum voltage at which the MOS device can operate without damage. As a result, the drain voltage must be constrained when matching the Si4431 for Class-E operation. This is accomplished by a suitable choice of limiting resistor R_{DC} as shown in Figure 1. The matching procedure discussed in this application note takes care to constrain the peak drain voltage to a specified maximum value.

The size of the MOS output device has the effect of limiting the amount of output power that can be extracted from a practical switching PA. In an ideal switching PA, we can increase the output power by either increasing the supply voltage or by increasing the shunt capacitance at the drain of the switching output device. We have just mentioned that the supply voltage cannot be increased indefinitely because the peak drain voltage may exceed the maximum voltage rating of the semiconductor process. Therefore, the only remaining option to increase output power is to increase the shunt capacitance.

This has the effect of requiring greater current handling capability in the switching device. While an ideal switch may carry an infinite amount of current, a practical MOS switch cannot. The size of the MOS output device in the Si4431 is carefully designed to carry sufficient current to achieve its maximum specified output power; however, this level of current-handling capability is only available when the RFIC is commanded to its maximum TX output power mode (by the txpow[2:0] field in SPI Register 6Dh). The Si4431 RFIC achieves a reduction in output power by reducing the number of active fingers (i.e., size) of the MOS output device; this effectively limits the current-handling ability of the output device to less than that desired by the combination of supply voltage and load impedance. That is to say, at the maximum setting(s) of the txpow[2:0] field, the PA output devices behave much like a switch, but at the lower settings of the txpow[2:0] field, the output devices behave more like a switch in series with a non-negligible resistance.

3. Matching Procedure for the Si4431

Published matching procedures for well-defined classes of operation of switching amplifiers (such as Class-D or Class-E) may lead to operating conditions that exceed the maximum ratings (voltage or current) for the semiconductor process. As a result, we turn to a “customized” matching methodology that satisfies our desire for output power and efficiency while maintaining operation below the maximum voltage and current ratings for the RFIC. Note that this matching methodology is based upon Class-E theory, but adds additional steps to aid in constraining the peak drain voltage.

3.1. Goals for the Matching Procedure

The matching methodology for the Si4431 RFIC is aimed at achieving the following simultaneous goals:

- Obtain +13 dBm of conducted RF output power
- Constrain the peak drain voltage to not exceed +6.5 V
- Maximize efficiency on the PA output stage
- Comply with ETSI and FCC specifications for spurious emissions

These goals will be met under the following conditions:

- Operation at any frequency in the 240–960 MHz range
- Antenna load impedance = 50 Ω
- The chip is commanded to maximum output power mode (txpow[2:0] field)
- Output power is measured at the TX output pin of the chip, prior to any lowpass filter
- Limitation on peak drain voltage is met for any V_{DD_RF} = 1.8 to 3.6 V
- Output power of +13 dBm is met for V_{DD_RF} = 3.3 V (minimum)

3.1.1. Comments on Peak Drain Voltage Limit

It should be noted that the +6.5 V peak drain voltage limit referred to above is not the same as the absolute maximum voltage rating at which the device may experience permanent damage. This absolute maximum voltage rating is shown in the Si4430/4431/4432 data sheet as +8.0 V on the TX output pin.

Instead, this peak drain voltage limit of +6.5 V has been calculated as a limit, which, if not exceeded for continuous periods of time, should allow for multiple years of operation without noticeable degradation in output power. That is to say, if the peak drain voltage were to momentarily slightly exceed +6.5 V, the device would likely not be instantaneously damaged but might suffer a small decrease in long-term reliability.

It should also be noted that the Si4431 RFIC contains internal diode voltage clamps on the drain node of the MOS output device. The purpose of these diode clamps is to limit brief excursions of the peak drain voltage that may occur in excess of +6.5 V. Such variations in peak drain voltage may occur if the antenna load impedance varies considerably from 50 Ω (e.g., turning on the TX output without an antenna connected, etc.).

In all cases, the voltage limit specified by the absolute maximum voltage rating should not intentionally be exceeded (however briefly) because instantaneous damage may occur.

3.1.2. Comments on Achieving +13 dBm Output Power

This application note is largely targeted at applications which require +13 dBm output power. While this level of output power is readily achievable, meeting the other design constraints (e.g., harmonics) requires careful attention to matching component selection and good board layout techniques. That is to say, it is possible to fail through poor design and board layout practices.

Conversely, it is a relatively simple matter to achieve all design goals at slightly reduced levels of output power, such as +10 dBm. For example, the constraint on peak drain voltage becomes much easier to meet as the supply voltage is reduced; however, there will, naturally, be some corresponding reduction in output power as the V_{DD} supply voltage is lowered.

In short, obtaining +13 dBm output power is not too difficult by itself, and constraining the peak drain voltage to less than +6.5 V is also not too difficult; it is the simultaneous achievement of both these design goals that is challenging.

3.2. Matching Procedure Overview

3.2.1. Split TX/RX Board Configuration

The following steps provide a broad overview of the matching methodology for the Split TX/RX board configuration. Further details of each step will be provided later. The required design equations are discussed in "3.3. Detailed Matching Procedure for Split TX/RX Board Configuration" on page 12.

1. First, select a value for the pull-up inductor LCHOKE that provides a very large impedance at the frequency of operation (and its nearest harmonics).
2. Choose/calculate values for series-resonant tank L0-C0 such that L0-C0 resonates at Fo.
3. Calculate the required value of ZLOAD, given the desired frequency of operation (Fo) and the known shunt drain capacitance (CSHUNT = ~2.5 pF) of the Si4431 chip.
4. Calculate the required value for the voltage-limiting resistor RDC, given the desired output power and main chip supply voltage VDD_RF.
5. Calculate the values for matching components LX and CX, given the antenna load resistance (e.g., RANT = 50 Ω) and the calculated value for ZLOAD.
6. Design a low-pass filter to provide sufficient attenuation of harmonic signals.
    a. The unfiltered waveform at the TX output pin will inherently contain high levels of harmonics.
    b. Depending upon the output power level and desired level of harmonic attenuation, a 3rd to 5th order low-pass filter will likely be required.

3.2.2. Single Antenna with Direct Tie Board Configuration

The following steps provide a broad overview of the matching methodology for the Single Antenna with Direct Tie board configuration. Further details of each step will be provided later. The required design equations are discussed in "3.4. Detailed Matching Procedure for Direct Tie Board Configuration" on page 28.

1. First, select a value for the pull-up inductor LCHOKE that provides a very large impedance at the frequency of operation (and its nearest harmonics).
2. Choose/calculate values for series-resonant tank L_0-C_0 such that L_0-C_0 resonates at Fo.
3. Calculate the required value of Z_{LOAD}, given the desired frequency of operation (Fo) and the known shunt drain capacitance (C_{SHUNT} = ~2.5 pF) of the Si4431 chip.
4. Calculate the required value for the voltage-limiting resistor R_{DC}, given the desired output power and main chip supply voltage V_{DD_RF}.
5. Calculate the values for matching components L_X and C_X, given the antenna load resistance (e.g., R_{ANT} = 50 Ω) and the calculated value for Z_{LOAD}.
6. Design a low-pass filter to provide sufficient attenuation of harmonic signals.
    a. The unfiltered waveform at the TX output pin will inherently contain high levels of harmonics.
    b. Depending upon the output power level and desired level of harmonic attenuation, a 3rd to 5th order low-pass filter will likely be required.
7. Construct a 4-element match to the differential RXp/RXn input pins, using the methodology outlined in “AN427 EZRadioPRO Si433x & Si443x RX LNA Matching”.
8. Deliberately mis-tune the calculated value of L_0 downwards by approximately 20%.

3.3. Detailed Matching Procedure for Split TX/RX Board Configuration

In this section, we provide further detail about each step of the matching procedure for the Split TX/RX board configuration outlined above. We assume a general chip supply voltage of V_{DD_RF} = 3.3 V.

3.3.1. Step #1: Select a Value for L_{CHOKE}

In Step #1, we select an appropriate value for the pull-up inductor L_{CHOKE}.

In the theoretical derivation for Class-E switching amplifiers, it is desired that the impedance of the pull-up inductor L_{CHOKE} is zero at DC and infinite at all other frequencies. This is not achievable in practice; however, a large value of inductance provides a reasonable approximation to this performance. The value of L_{CHOKE} should be chosen such that it provides a high impedance at not only the fundamental operating frequency but also at the first few harmonic frequencies as well. The inductance value should not be so large as to already be at (or past) parallel self-resonance at the desired operating frequency. The exact inductance value is not critical; however, Silicon Labs recommends the following range of inductance values (assuming 0402-size or 0603-size inductors) as a function of the desired operating frequency:

- 315 MHz: approximately 270 to 390 nH
- 470 MHz: approximately 270 nH
- 915 MHz: approximately 120 nH

3.3.2. Step #2: Choose/Calculate Values for L_0-C_0 Series-Resonant Tank

In Step #2, we design the L_0-C_0 tank to be series-resonant at the desired operating frequency Fo.

It is self-evident that there is an infinite number of combinations of L_0-C_0 values that can achieve resonance at a desired frequency. However, certain broad guidelines may be used to select one particular solution of component values.

First, it is desirable that the inductance and capacitance values be neither extremely large or extremely small. Discrete inductors and capacitors with extremely large values are subject to degrading effects due to self-resonance. Discrete components with extremely small values are subject to greater degrading effects due to component tolerance. In either case, the actual resonant frequency of the tank may be significantly different than the frequency predicted by mathematical calculations.

Second, in the theoretical derivation for Class-E switching amplifiers it is desired that the impedance of the L_0-C_0 series-resonant tank be zero at Fo and infinite at all other frequencies. This is not achievable in practice; however, a reasonable approximation to this performance may be obtained by using values with a high L-to-C ratio.

Third, it is desirable to minimize the insertion loss of the resonant tank. As the quality factor (Q) of discrete inductors is generally much lower than that of discrete capacitors, it is important to select an L_0-C_0 ratio that maximizes the inductor Q. The Q of discrete inductors generally increases as the inductance value is also increased, until the inductance approaches the value where self-resonance becomes a concern.

Finally, it is desirable to select component values that are near standard 5% tolerance values.

These considerations lead to the following guidelines for selecting the values for L_0-C_0:

- The L_0-C_0 tank must resonate at Fo.
- The value of L_0 should be chosen as large as possible.
- While remaining low enough that effects of self-resonance are not an issue.
- And are close to standard 5% tolerance values.

3.3.3. Step #3: Calculate the Required Value for Z_{LOAD}

In Step #3, we calculate the required value of load impedance to be presented to the output of the L_0-C_0 resonant tank, at the fundamental operating frequency Fo.

In the theoretical derivation for Class-E switching amplifiers, it may be shown that the equations for output power (P_{OUT}) and load impedance (Z_{LOAD}) as a function of shunt drain capacitance (C_{SHUNT}) and supply voltage (V_{DD}) are as follows:

$$P_{OUT} = \pi\omega_o C_{SHUNT} V_{DD}^2$$

Equation 1.

$$Z_{LOAD(fund)} = \left(\frac{0.2815}{\omega_o C_{SHUNT}}\right) e^{jx49.0524°}$$

Equation 2.

These two equations are quite interesting. Equation 1 states that the theoretical output power is not a function of load impedance, but instead depends only upon the shunt drain capacitance (C_{SHUNT}), the desired operating frequency ($\omega_o = 2\pi Fo$), and the PA supply voltage (V_{DD}). Equation 2 states that the required load impedance (Z_{LOAD}) does not vary with the desired level of output power, but depends only on the desired operating frequency and value of shunt drain capacitance.

The value of internal shunt drain capacitance C_{SHUNT} is a design parameter of the Si4431 RFIC and is not adjustable by the user. This shunt capacitance is composed primarily of the drain-source capacitance (C_{ds}) of the output MOS devices, in parallel with a small amount of explicit integrated capacitance. Silicon Labs states that the value of this internal shunt drain capacitance is approximately:

- C_{SHUNT} = 2.5 pF

This value may be substituted in the equations above and used to calculate other matching parameters. Assuming a desired operating frequency of Fo = 315 MHz as an example, the following value for Z_{LOAD} may be calculated:

$$Z_{LOAD(315M)} = \left(\frac{0.2815}{2\pi \times 315M \times 2.5\ pF}\right) e^{j\ x\ 49.0524°} = 37.11 + j42.77\Omega$$

Equation 3.

This is the value of load impedance (at the fundamental operating frequency) that must be presented to the output of the L_0-C_0 resonant circuit.

It should be clearly understood that this value of load impedance (Z_{LOAD}) discussed above and the antenna impedance (Z_{ANT}) are not the same parameter, nor do they necessarily have the same ohmic value. Given the arbitrary impedance of the antenna, the next task will be to construct a matching network that transforms Z_{ANT} into Z_{LOAD}, as seen at the output of the L_0-C_0 resonant circuit.

3.3.4. Step #4: Calculate the Required Value for Voltage-Limiting Resistor R_{DC}

In Step #4, we calculate the value of the voltage-limiting resistor R_{DC} required for the desired output power, given a specified value of PA supply voltage (V_{DD}).

Equation 1 clearly shows that for a given desired operating frequency, the only “knob” remaining to the user to select the output power is the PA supply voltage V_{DD}, as the value of C_{SHUNT} is an internal chip design parameter and is not adjustable by the user. Equation 1 is easily solved for V_{DD} and is found to be

$$V_{DD} = \sqrt{\frac{P_{OUT}}{\pi\omega_o C_{SHUNT}}}$$

Equation 4.

Continuing our design example at 315 MHz, and assuming a desired output power of +13 dBm (20 mW), the required value of V_{DD} may be calculated as the following:

$$V_{DD} = \sqrt{\frac{0.02}{2\pi \times 315M \times 2.5\ pF}} = 1.133\ V$$

Equation 5.

This equation states that if the voltage supplied to the top of pull-up inductor L_{CHOKE} is equal to 1.133 V, and the previously-calculated value of load impedance Z_{LOAD} is presented to the chip, the resulting output power will be P_{OUT} = 20 mW = +13 dBm.

This required PA supply voltage (V_{DD}) is significantly different than the general supply voltage (V_{DD_RF}) for the rest of the RFIC (e.g., for the VDD_RF and VDD_DIG input pins). It is obviously not desirable to maintain two separate, independent sources of supply voltage for the RFIC; therefore, it is convenient to create the PA output supply voltage from the main supply voltage by means of an I-R voltage drop across a resistor.

This is accomplished by resistor R_{DC} as shown in Figure 1. As the theoretical efficiency of a Class-E switching amplifier is 100%, the average drain current I_{DD} may be calculated as

$$P_{OUT} = \pi\omega_0 C_{SHUNT} V_{DD}^{\ 2} = I_{DD} V_{DD}$$

Equation 6.

This equation may be solved for I_{DD} to obtain

$$I_{DD} = \pi\omega_0 C_{SHUNT} V_{DD}$$

Equation 7.

Given the main supply voltage for the remainder of the chip (V_{DD_RF}), and having previously calculated the required value of PA supply voltage (V_{DD}) and average drain current (I_{DD}), it is a simple matter to calculate the required value for R_{DC}:

$$R_{DC} = \frac{V_{DDRF} - V_{DD}}{I_{DD}}$$

Equation 8.

Continuing our design example at 315 MHz for +13 dBm output power, we calculate:

$$I_{DD} = 2\pi \times 315M \times 2.5\ pF \times 1.333\ V = 17.61\ mA$$

Equation 9.

Assuming a general chip supply voltage of V_{DD_RF} = 3.3 V, we calculate the following:

$$R_{DC} = \frac{3.3 - 1.133}{0.01761} = 123.05\ \Omega$$

Equation 10.

This value of resistance must be placed in series with L_{CHOKE} in order to drop the general chip supply voltage down to the value required to obtain the desired output power.

3.3.5. Step #5: Calculate the Values for Matching Components L_X and C_X

In Step #5, we calculate the values of the matching components required to transform the given antenna impedance (Z_{ANT}) into the required load impedance (Z_{LOAD}).

This matching effort may accomplished by simple and normal design methods, such as use of a Smith Chart or impedance matching CAD software (e.g., WinSmith™). Continuing our design example at 315 MHz, and assuming an antenna impedance of $Z_{ANT} = R_{ANT} = 50\ \Omega$, we find that 50 Ω may be transformed to the required value of $Z_{LOAD} = 37.11 + j\ 42.77\ \Omega$ by shunt matching capacitance $C_X = 5.96$ pF and series matching inductance $L_X = 32.66$ nH. The resulting circuit topology is shown in Figure 5.

It should be noted that this is only one possible solution for the required impedance transformation; other matching topologies could have been used as well. The reader should also note that the required L_X-C_X match topology depends upon the real part of the load impedance, $Re(Z_{LOAD})$. In this example, the real part of the load impedance was less than 50 Ω and thus an appropriate matching topology consisted of a shunt capacitor (C_X) and a series inductor (L_X). In the event that $Re(Z_{LOAD})$ had been greater than 50 Ω, an appropriate matching topology would have consisted of first a series inductor (L_X) followed by a shunt capacitor (C_X).

It is apparent that series inductors L_0 and L_X in Figure 5 may be combined into one equivalent inductor with a value equal to the sum of their individual inductances, in order to reduce parts count. This is a normal and usual practice.

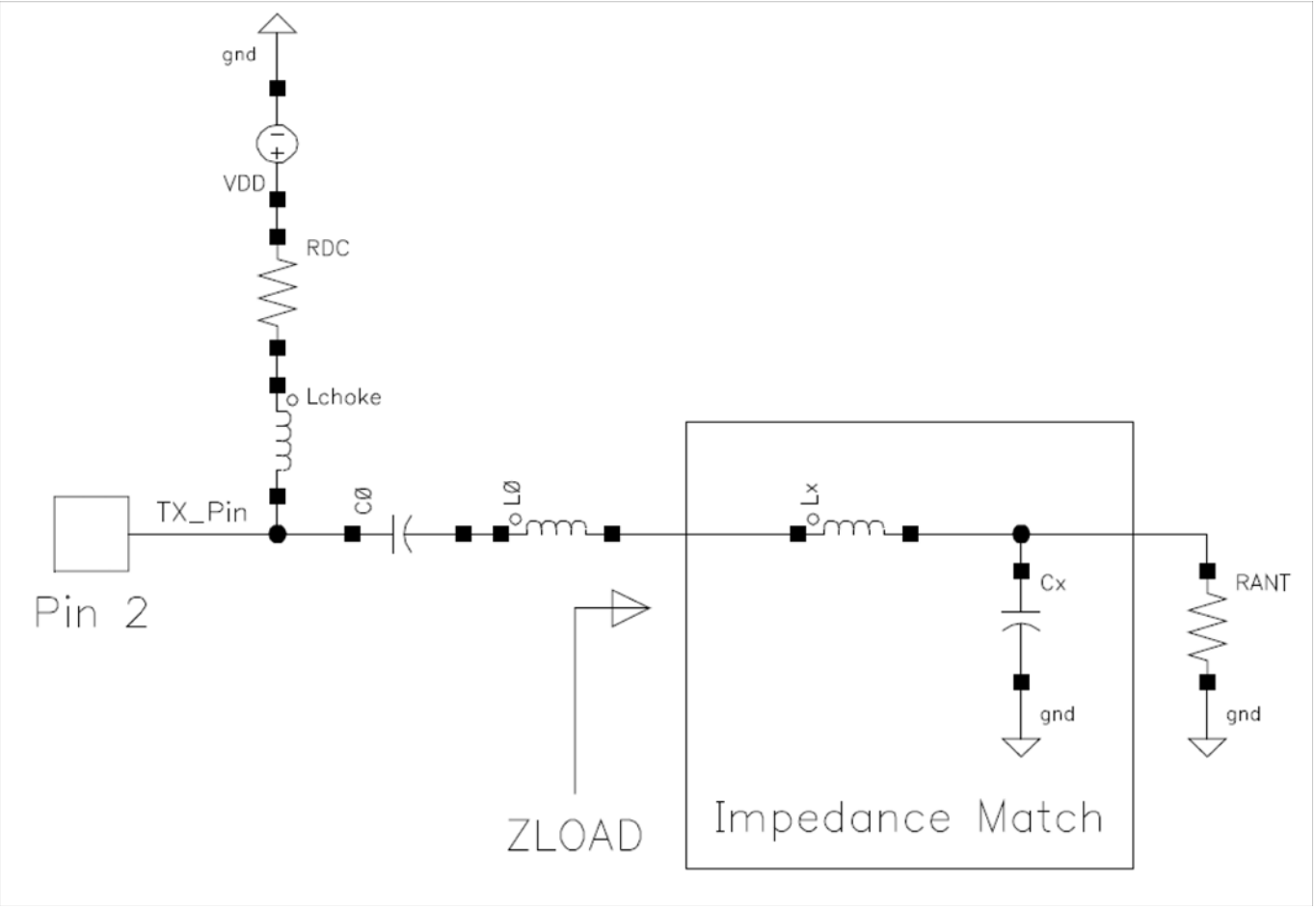

Figure 5. Impedance Match to Transform RANT to ZLOAD

3.3.5.1. Voltage Waveforms at TX Output Pin

At this point, the basic PA output match is complete. Although we have not yet designed a lowpass filter to sufficiently attenuate the harmonic signals, it is possible to measure the output power by substituting a power meter or spectrum analyzer in place of the antenna impedance (R_{ANT}).

It was previously mentioned that the peak of the drain voltage waveform in a Class-E switching amplifier may reach levels of $V_{PEAK} = 3.56 \times V_{DD}$. (This statement was offered without proof; for those readers interested in the derivation, please refer to the papers listed in "2.2. Theory of Operation of an Ideal Switching PA" on page 8.) It is desirable to measure the actual drain voltage waveform in order to ensure compliance with our stated design goal of constraining the peak drain voltage to less than 6.5 Vpk.

It is not difficult to verify the resulting voltage waveform at the TX output pin (at least for the lower frequency bands of operation). A high-speed oscilloscope with an input bandwidth of at least 4 GHz (preferably higher) is required. A low-capacitance, high-bandwidth scope probe is also required, or, alternatively, the “resistive-sniffing” network of Figure 6 may be used. In this schematic, it may be seen that the inductors L_0 and L_X have been combined into one equivalent series inductance.

Figure 6. Resistive Sniffing Network

Using the “resistor sniffing” technique of Figure 6, the drain voltage waveform of Figure 7 was observed for an operating frequency of Fo = 315 MHz. In the example shown here, the following component values (obtained through use of the design equations above) were used:

- $P_{OUT(TARGET)}$ = +13.5 dBm
- VDD_RF = 3.3 V
- C_{SHUNT} = 2.5 pF
- L_{CHOKE} = 390 nH
- R_{DC} = 110 Ω
- C_0 = 10 pF
- L_0+L_X = 68 nH
- C_X = 6.0 pF

A “Class-E like” waveform was obtained, with a maximum drain voltage of 4.98 V (i.e., less than 6.5 V). However, the measured output power was +12.5 dBm, somewhat less than our design target of P_{OUT} = +13.5 dBm. This is because the design equations above assume ideal switching operation of the output devices (i.e., zero ON-state resistance, infinite OFF-state resistance, zero switching time, etc.) as well as lossless discrete matching components. A practical switching amplifier and output match will inherently fall short of such ideal operation; some small degradation in output power is to be expected.

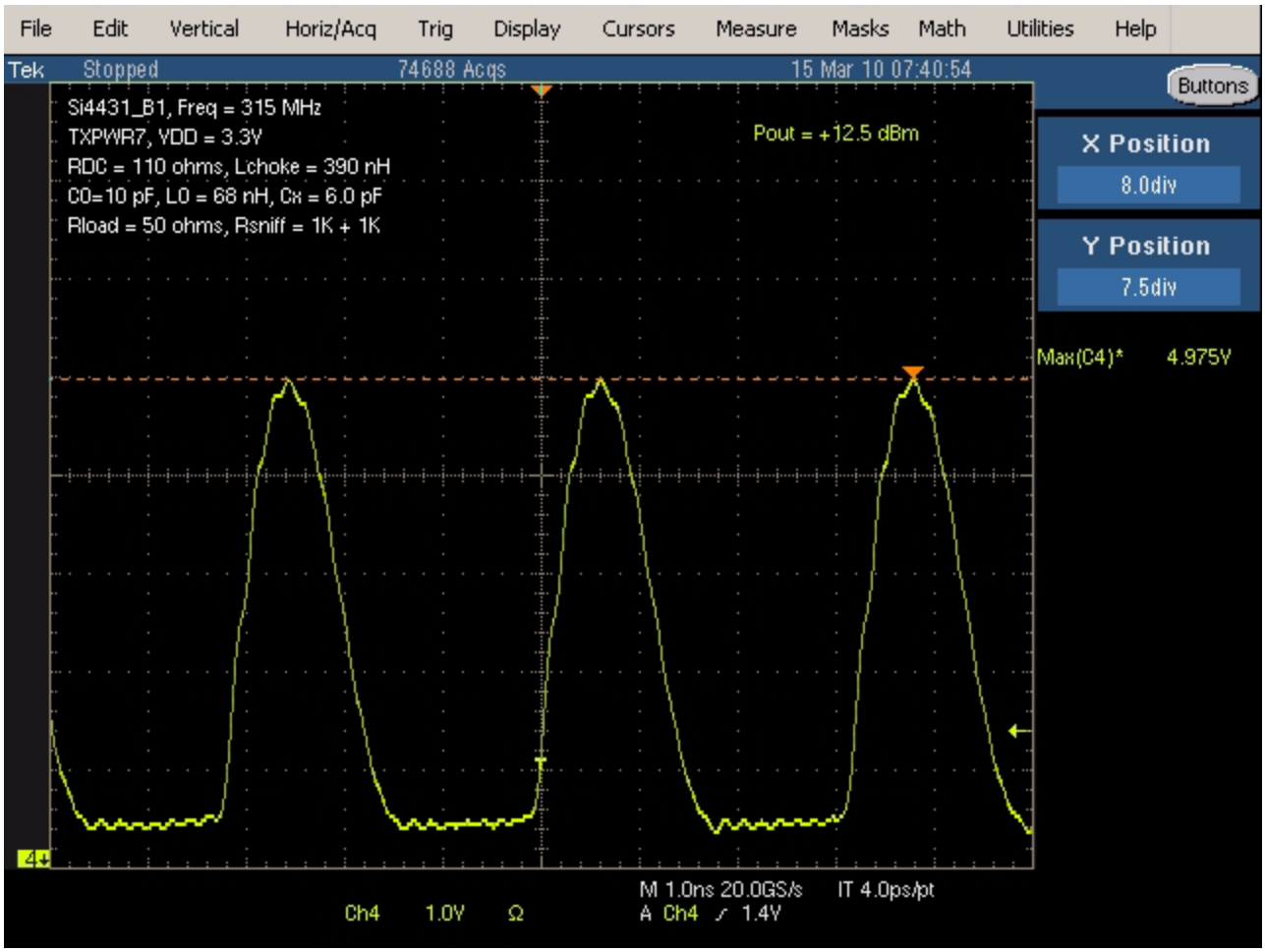

Figure 7. Drain Voltage Waveform (Fo = 315 MHz)

It should be noted that, as the operating frequency increases, it becomes more difficult to faithfully observe the waveform. The input bandwidth of the oscilloscope used to display the waveform must increase in accordance with the operating frequency. Additionally, parasitic capacitances in the PCB layout, as well as in the output device(s) of the RFIC, tend to limit the high-frequency response of the amplifier.

3.3.6. Step #6: Design a Lowpass Filter

In Step #6, we design a low-pass filter network to attenuate the harmonics below the level required to meet applicable regulatory standards (e.g., FCC or ETSI).

3.3.6.1. Unfiltered Harmonic Spectrum

It should be understood that the waveform at the output of the match shown in Figure 5 will still contain relatively high levels of harmonics. Although the bandpass response of the series-resonant L_0-C_0 tank provides some attenuation of harmonic signals, it is generally not sufficient to meet applicable regulatory standards. This is normal for such a switching-amplifier and matching topology.

By way of example, the harmonic spectrum at the antenna load (R_{ANT}) for the matching network and component values of Figure 6 is shown in Figure 8.

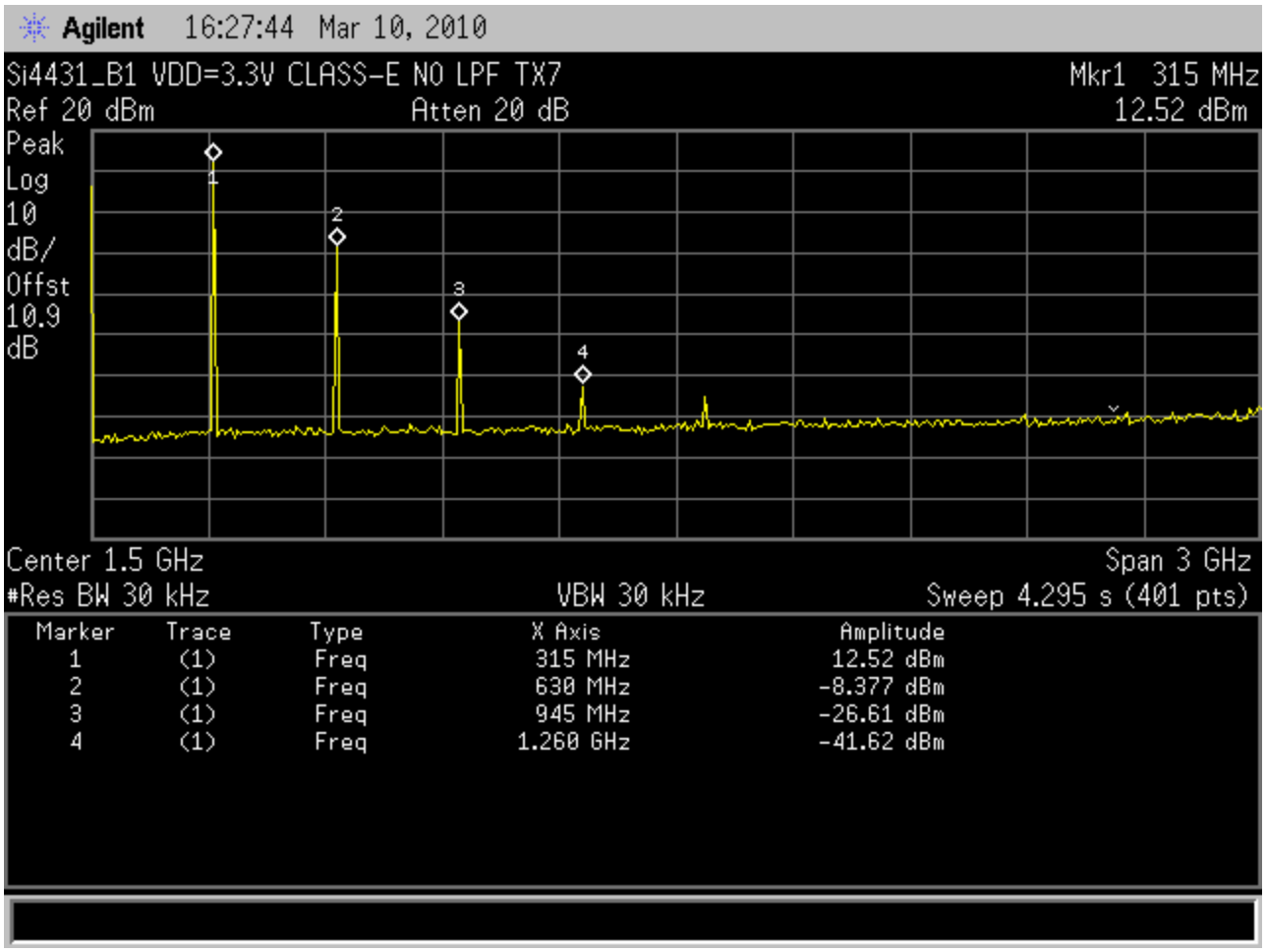

Figure 8. Unfiltered Harmonic Spectrum (Fo = 315 MHz)

3.3.6.2. Filtering Requirements

It is difficult for Silicon Labs to recommend one single low-pass filter design that is appropriate for all customers, as customers may operate under widely differing regulatory standards, each with differing harmonic requirements. However, a common regulatory standard that may be applicable to our design example at 315 MHz is FCC Part 15.231. This standard specifies the permitted levels of fundamental and harmonics in terms of field strength, measured at a distance of 3 meters. At our desired operating frequency of 315 MHz, these maximum permitted field strength levels are as follows:

- Fundamental = 6042 µV/meter
- Harmonics = 604.2 µV/meter

As the limits are specified in terms of field strength, compliance must be verified by measuring in an anechoic chamber with the unit operated into its intended antenna. However, if an ideal isotropic antenna is assumed, calculations may be performed to convert field strength into an equivalent level of conducted power, known as Equivalent Isotropic Radiated Power or EIRP. The following formula is used for the calculation:

$$P_{COND(mW)} = \frac{V_{RMS}\left(\frac{V}{m}\right)^2}{3.333}$$

Equation 11.

Using Equation 11 we find the equivalent conducted power levels to be as follows:

- Fundamental = –19.6 dBm EIRP
- Harmonics = –39.6 dBm EIRP

Note that the harmonics are only required to be attenuated to –20 dBc relative to the fundamental signal. However, in the event that the harmonics fall in a “restricted band” as defined in FCC Part 15.205 and Part 15.209, the unwanted signal must be attenuated to less than –49 dBm (200 µV/meter at a distance of 3 meters at frequencies below 960 MHz).

It is highly unlikely that the radiation efficiency of a typical antenna used by a customer will approach that of a theoretically-ideal isotropic radiator. That is to say, it will be necessary to provide somewhat more conducted power than –19.6 dBm to the input of the antenna in order to achieve the specified maximum radiated field strengths. However, it is also unlikely that the radiation efficiency of a typical antenna is so poor that the full available conducted output power of +12.5 dBm (shown in Figure 8) is required. It is highly probable that in our design example at 315 MHz with intended operation under FCC Part 15.231, the user would choose to operate the Si4431 RFIC at a reduced TX output power level (perhaps approximately 0 to +2.5 dBm) in order to maintain compliance with regulatory specs.

3.3.6.3. Selecting a LPF Order and Type

Therefore, given the unknown radiation efficiency each possible antenna selectable by the user, it is difficult for Silicon Labs to conclusively state the required filter attenuation characteristics. As a reasonable design compromise, we settle upon the following design goals for the low-pass filter:

- Minimal insertion loss at the desired operating frequency
- Minimum of 20 dB attenuation at the 2nd harmonic
- Minimum of 30 dB attenuation at the 3rd and higher harmonics
- Lowest filter order possible to still achieve this required harmonic attenuation
- 1:1 impedance transformation (i.e., 50 Ω input and 50 Ω output impedance)

Note that the amplitude characteristics in the lower portion of the passband of the LPF are relatively unimportant. Because the output signal contains no frequency components below the fundamental frequency, the frequency response of the filter below the desired operating frequency is also of little consequence. We are free to choose the filter type (e.g., Butterworth, Chebyshev, Elliptic) based primarily upon the filter’s attenuation characteristics rather than its passband response.

A Butterworth filter design is not optimal because it provides relatively poor high-frequency attenuation characteristics; there is no need to sacrifice high-frequency attenuation in order to obtain a maximally-flat in-band frequency response.

Similarly, an Elliptic filter design (Cauer-Chebyshev) may provide insufficient attenuation at higher-order harmonic frequencies. While it may be possible (and advantageous) to tune a transmission zero in the stopband to the frequency of a problematic harmonic (e.g., N=2 or N=3), it is paid for with a decrease in attenuation at higher harmonic frequencies. As the unfiltered harmonic spectrum of Figure 8 shows, there remain several higher-order harmonics with significant energy that cannot be ignored and must be attenuated.

As a result, we settle on a Chebyshev low-pass filter design as an acceptable type of filter response.

With a Chebyshev filter, it is possible to obtain a greater rate of attenuation roll-off in the stopband by accepting a larger amount of amplitude ripple in the passband. The next issue to be addressed is the amount of passband

ripple to be targeted in the filter design.

Greater attenuation at high frequencies can be obtained by employing a filter designed for a relatively large amount of passband ripple, but this trade-off should not be pushed too far. While a reasonable amount of passband ripple is perfectly acceptable, there is a limit to what can be considered reasonable.

Figure 9 shows the passband frequency response of an ideal (lossless) Chebyshev filter with 0.5 dB of amplitude ripple in the passband. It is quickly apparent that in order to minimize the insertion loss of the filter at the desired operating frequency, it is necessary to design the cutoff frequency of the filter such that the desired operating frequency falls at one of the passband amplitude ripple peaks (Cursor “A” in the plot). If the filter cutoff frequency varies due to component tolerances, the filter response may vary such that the desired operating frequency falls on a minimum of the amplitude ripple response rather than on a maximum. In such a scenario, the filter insertion loss will increase, and the TX output power will decrease.

By designing for a limited amount of passband amplitude ripple, an upper limit is placed on the filter insertion loss due to mistuning of the component values. It is the opinion of Silicon Labs that a Chebyshev passband amplitude ripple of 0.25 to 0.5 dB represents a reasonable design tradeoff between high-frequency stopband attenuation and potential passband filter insertion loss due to component tolerance.

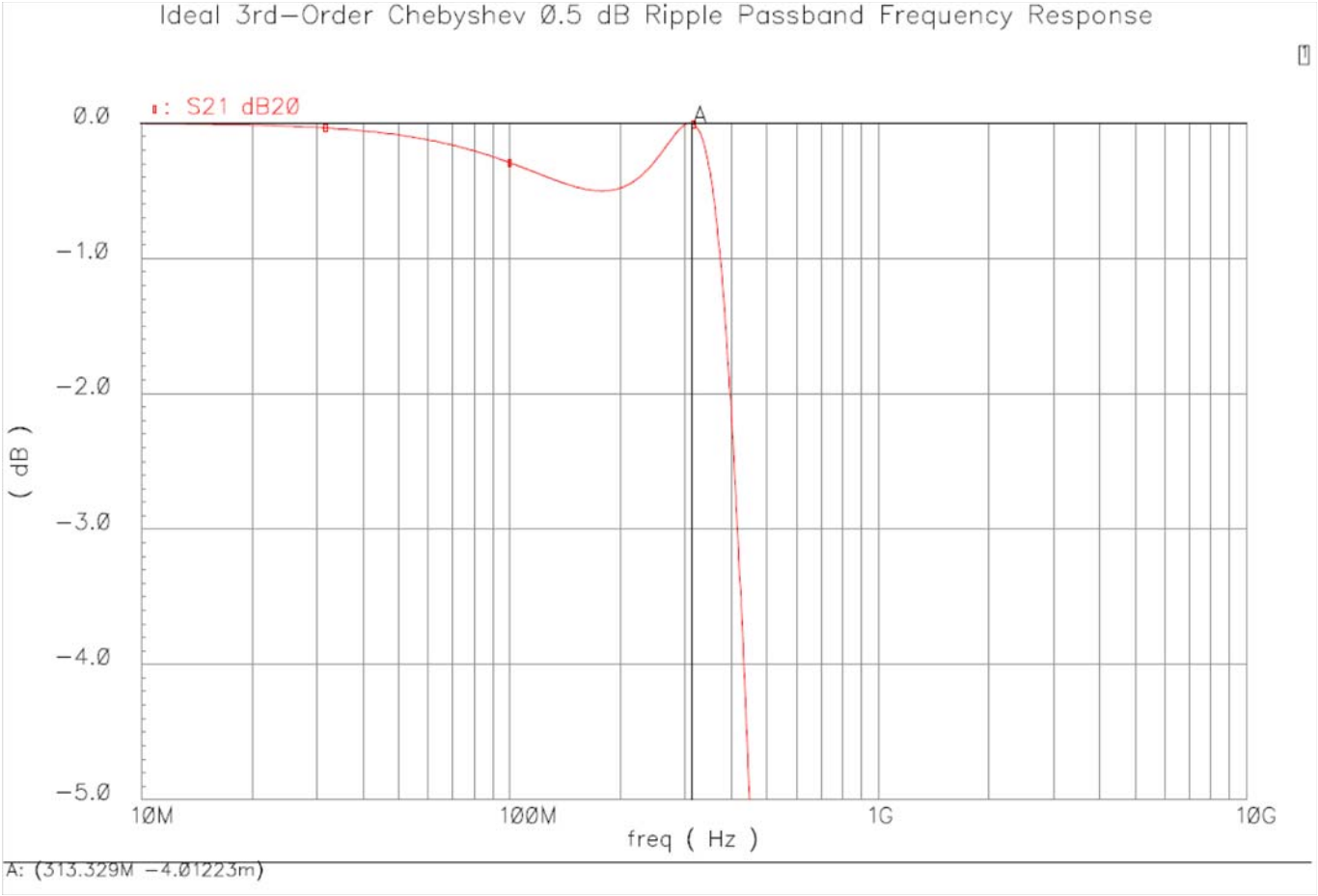

Figure 9. Ideal 3rd-Order 0.5 dB Chebyshev Filter Response at 315 MHz

3.3.6.4. Calculation/Design of Component Values

Actual filter component values may be obtained by usual design methods such as use of Filter Design CAD software or tables of normalized filter values scaled to the desired frequency of operation. Silicon Labs recommends designing the filter such that the desired operating frequency falls at a peak of the amplitude ripple response rather than at the 3 dB cutoff frequency or at the equal amplitude ripple cutoff frequency. In this manner, the insertion loss of the filter will be minimized, and the TX output power will be maximized. For a third-order 0.25 dB Chebyshev filter, the ratio of F_{3dB}:F_{PEAK} is approximately 1.253:1. That is, if the desired operating frequency is 315 MHz, the filter must be designed for a 3 dB cutoff frequency of 315 x 1.253 = 395 MHz. For a 3rdorder 0.5 dB Chebyshev filter, the ratio of F_{3dB}:F_{PEAK} is approximately 1.167:1.

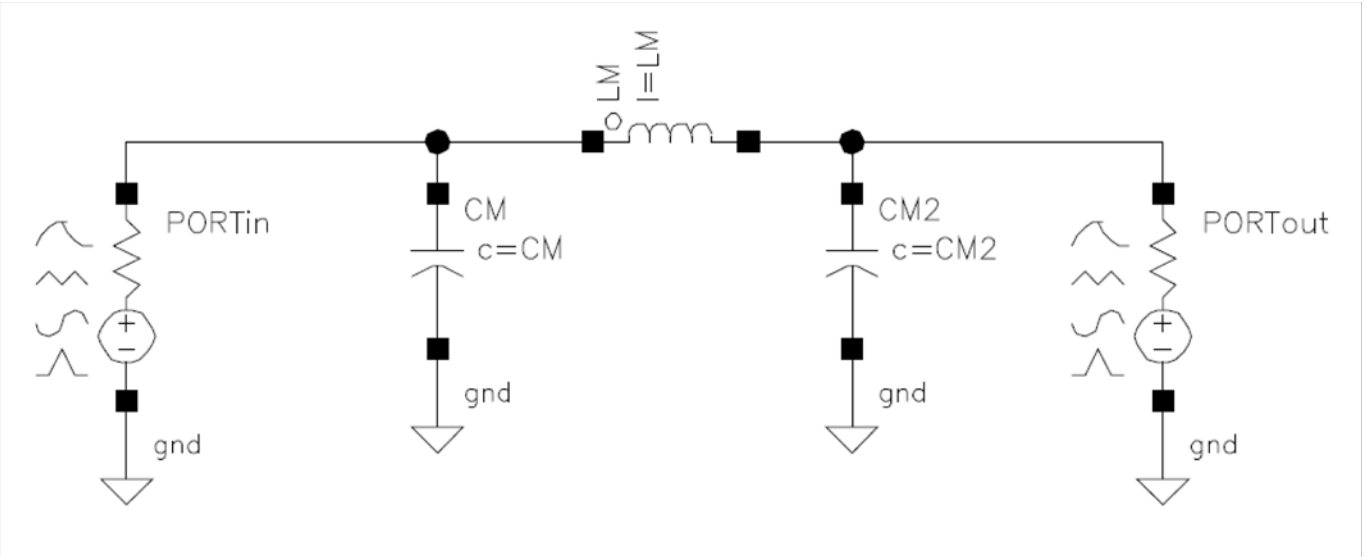

Figure 10. 3rd-Order PI-Topology Low-Pass Filter

Figure 10 shows the general architecture of a 3rd-order low-pass filter using the PI-topology. After design of a 0.5 dB ripple Chebyshev filter with a peak frequency of 315 MHz (F_{3dB} = 395 MHz), the following component values are obtained:

- CM = 15.02 pF
- LM = 25.8 nH
- CM2 = 15.02 pF

It is generally sufficient to use the nearest available standard 5% component tolerance values. Making these substitutions results in the following set of component values:

- CM = 15 pF
- LM = 24 nH
- CM2 = 15 pF

3.3.6.5. Simulation of Actual Filter Frequency Response

An ideal frequency response is not possible in practice because it is necessary to use inductors and capacitors with not only finite Qs, but also with internal self-resonances due to parasitic elements. These factors, as well as parasitic effects due to board layout, may cause the actual frequency response to be degraded relative to the ideal response shown in Figure 9.

The effects of using non-ideal components can be predicted by simulation with SPICE models obtained from the manufacturers of discrete components (e.g., Murata, CoilCraft, etc.). Figure 11 shows the simulated frequency response of this low-pass filter design implemented with real (lossy) components. Note that the filter attenuation at the second harmonic frequency (630 MHz) is 18.9 dB, very close to our design goal of 20 dB minimum. The filter attenuation at the higher harmonics easily exceeds our design target of 30 dB, thus validating the choice of filter type, order, and passband amplitude ripple.

However, it should be clearly understood that Silicon Labs does not guarantee that a 3rd-order low-pass filter design is appropriate for all customer applications. Depending upon the applicable regulatory standard and desired output power level, the filter order may be need to be modified to suit a particular customer's needs.

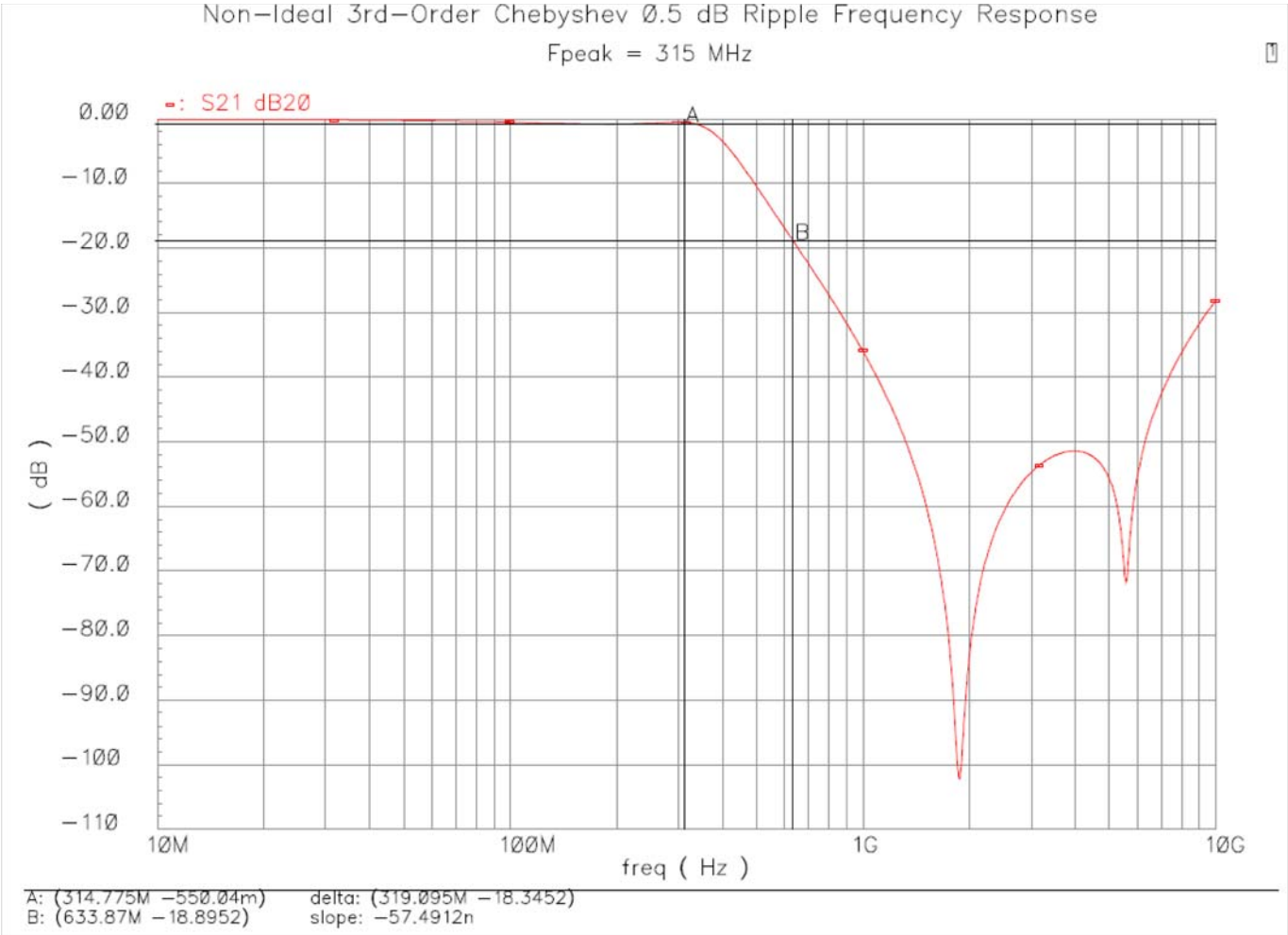

Figure 11. Non-Ideal Simulated Freq Response of 0.5 dB Chebyshev Filter (Fo = 315 MHz)

This simulation using non-ideal discrete components predicts an in-band insertion loss of approximately 0.55 dB at the desired operating frequency (315 MHz, in this example). While not desirable, this value of filter insertion loss is fairly realistic, given the typical Qs of discrete components in 0402-size or 0603-size surface-mount packages. Discrete components of higher quality (e.g., wire-wound inductors) may be chosen in an effort to reduce insertion loss, but such parts are admittedly more expensive. It should be noted that the data sheet for the Si4431 RFIC specifies the output power as measured at the TX output pin, prior to the insertion loss of any low-pass filter.

It is apparent that there are now transmission zeroes in the simulated frequency response. These transmission zeroes (e.g., near 1.9 GHz and 5.6 GHz in Figure 11) are due to self-resonances in the discrete components. The shunt capacitors in the filter network (i.e., CM and CM2) exhibit a series self-resonance at some frequency, while the series inductors (i.e., L0, LM, and LM2) exhibit a parallel self-resonance at some frequency. The presence of such transmission zeroes may help to “bend down” the attenuation curve more quickly, resulting in improved attenuation at lower harmonic frequencies, but at the cost of degraded attenuation at higher harmonic frequencies. It is not advisable to rely too heavily upon “tuning” of these transmission zeroes to aid in meeting harmonic performance.

3.3.6.6. Combining the LPF with the Output Match

The methodology used for design of the low-pass filter was for a filter with a 1:1 impedance transformation ratio. That is, if the antenna impedance was R_{ANT} = 50 Ω, then the impedance seen looking into the input of the low-pass filter at C_M is also 50 Ω (at the fundamental frequency). Thus our calculations for impedance matching components L_X and C_X remain unchanged. The resulting schematic for the output match and low-pass filter is shown in Figure 12.

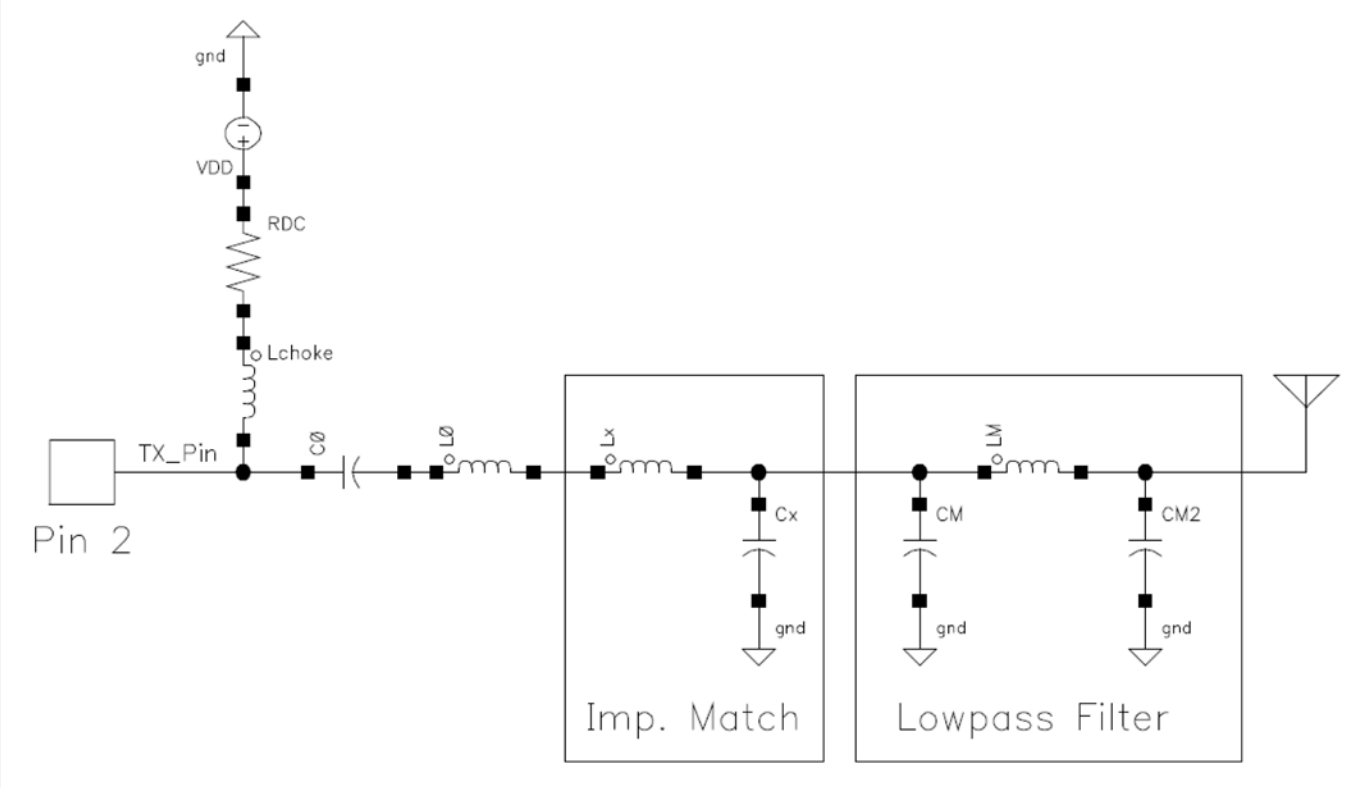

Figure 12. Schematic of Output Match and Lowpass Filter

However, it is quickly apparent that this schematic may be simplified. As discussed previously, series inductors L_0 and L_X may be combined into one equivalent series inductance. Shunt capacitors C_X and C_M may be combined in a similar fashion. After simplification, the schematic appears as shown in Figure 13.

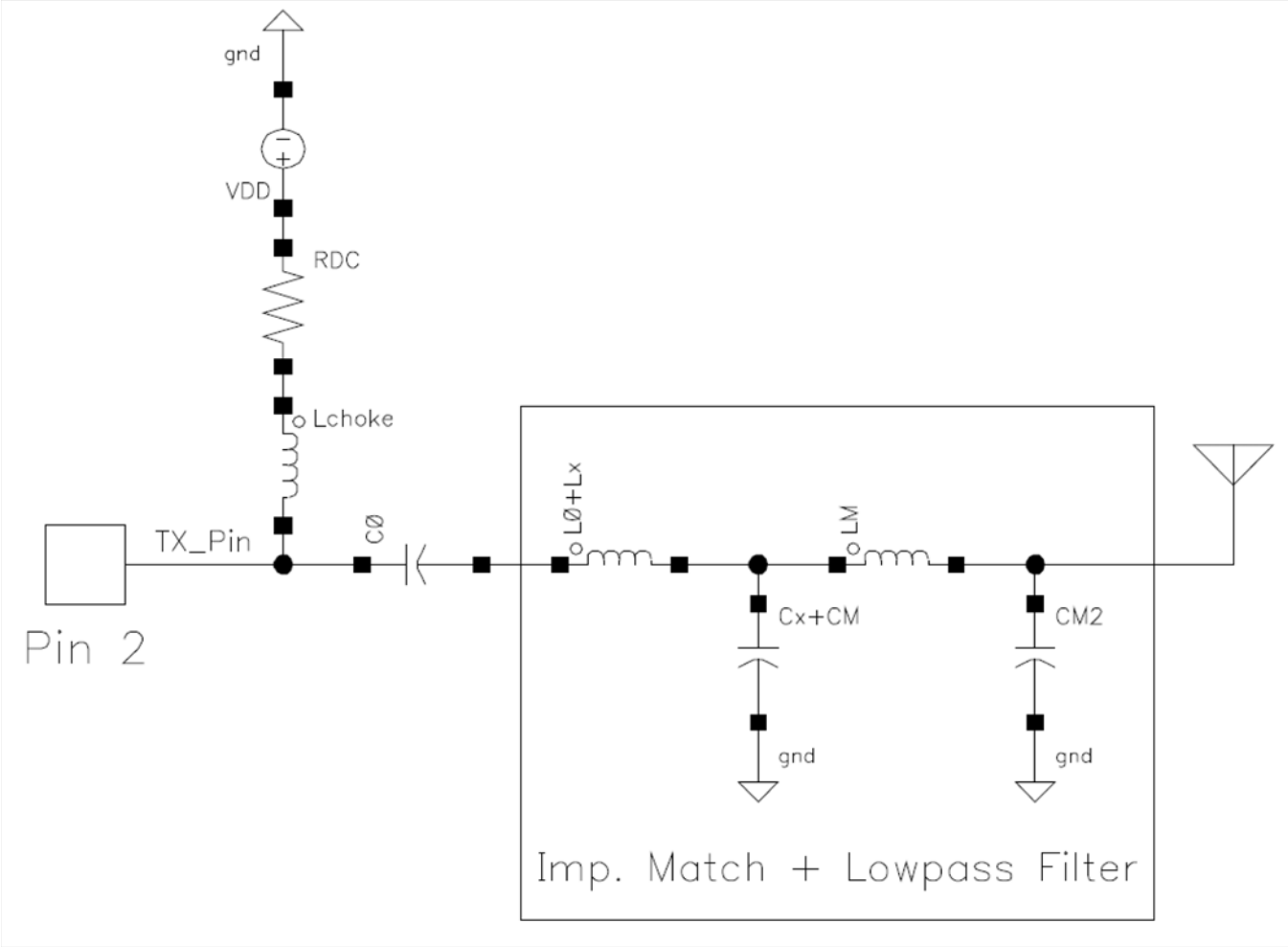

Figure 13. Output Match and Lowpass Filter Schematic (Simplified)

3.3.6.7. Final Measurement of Harmonic Spectrum

The conducted output power spectrum of the final circuit is shown in Figure 14. These results are measured at the maximum TX output power setting (txpow[2:0] = 3'b111) of the Si4431 RFIC.

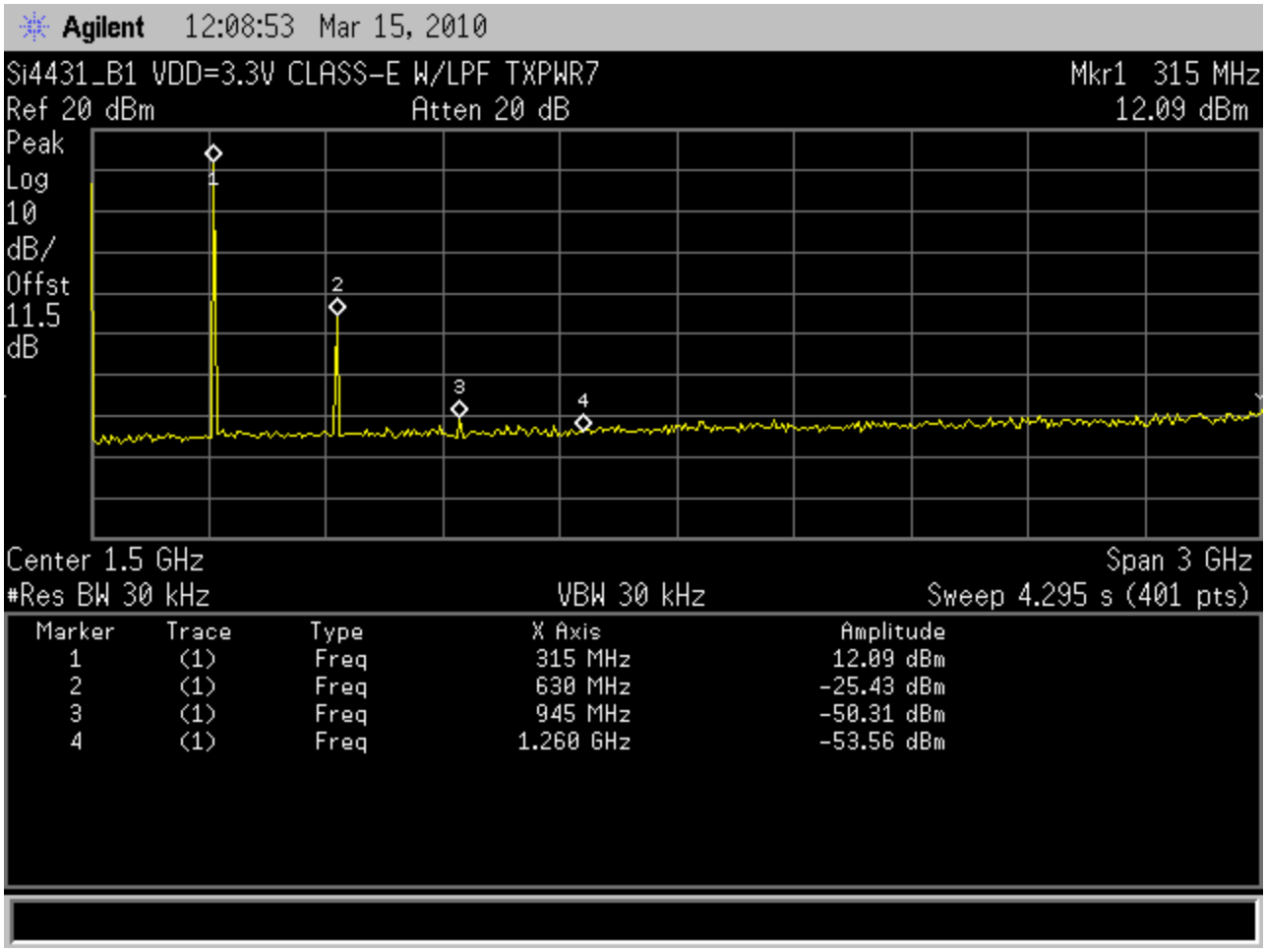

Figure 14. Filtered Harmonic Spectrum at Maximum Power (Fo = 315 MHz)

The conducted TX output power spectrum may also be measured at a reduced output power setting that may be more appropriate for operation under FCC Part 15.231. The measured output power spectrum for txpow[2:0]=3'b010 is shown in Figure 15.

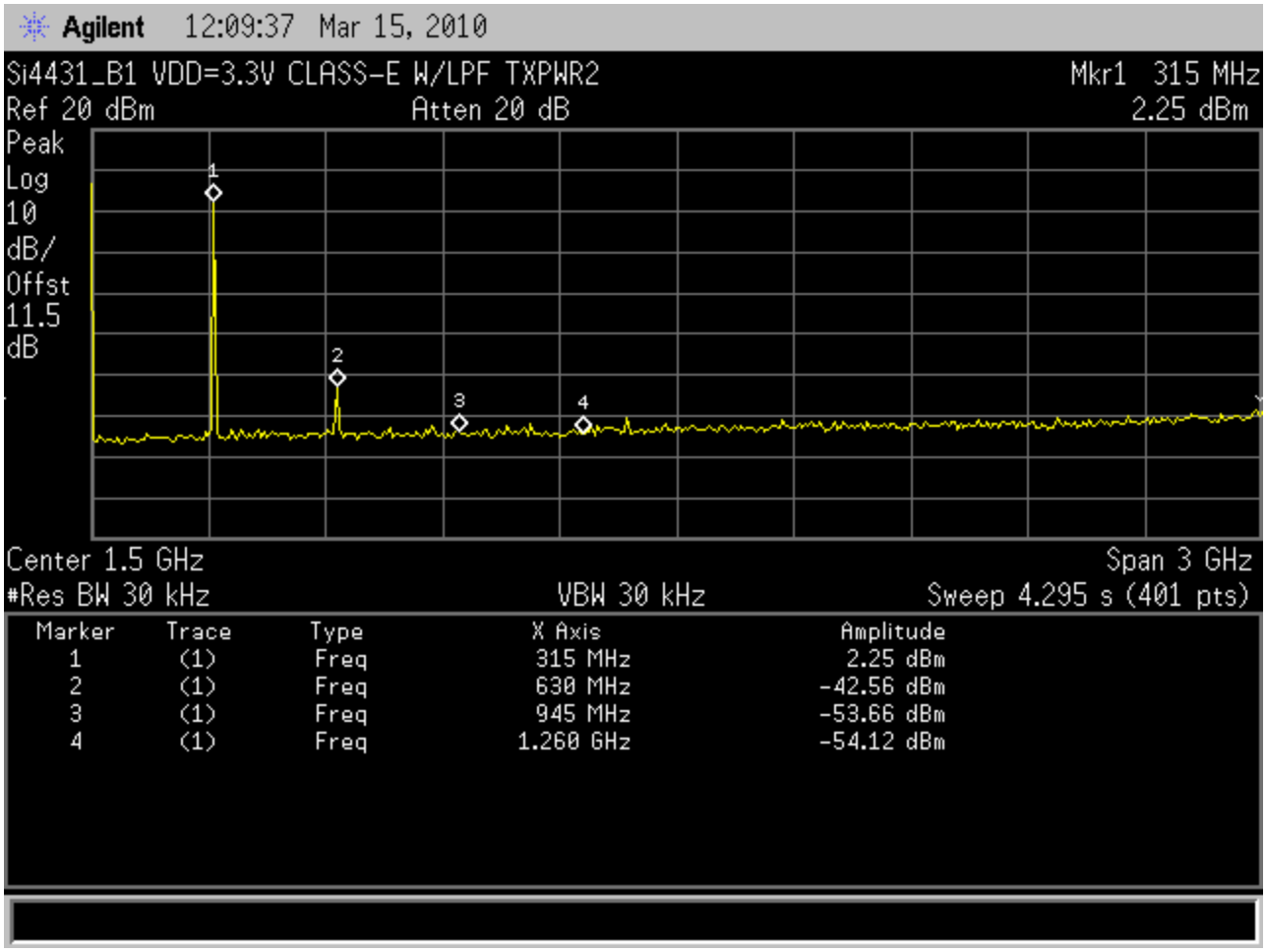

Figure 15. Filtered Harmonic Spectrum at Reduced Power (Fo = 315 MHz)

3.3.7. Summary of Match

This completes the steps of the match design process for the Split TX/RX board configuration. This match design process may be used to obtain matching component values at any desired operating frequency. A summary table of these matching component values is shown in Table 1 on page 2.

3.4. Detailed Matching Procedure for Direct Tie Board Configuration

In the Direct Tie board configuration, the TX and RX paths are tied directly together without the use of an RF switch, as shown in Figure 2. Careful design procedure must be followed to ensure that the RX input circuitry does not load down the TX output path while in TX mode, and that the TX output circuitry does not degrade receive performance while in RX mode.

The RX input circuitry of the EZRadioPRO family of chips contains a set of switches that aids in isolation of the TX and RX functions. This set of switches is implemented internally as shown in Figure 16.

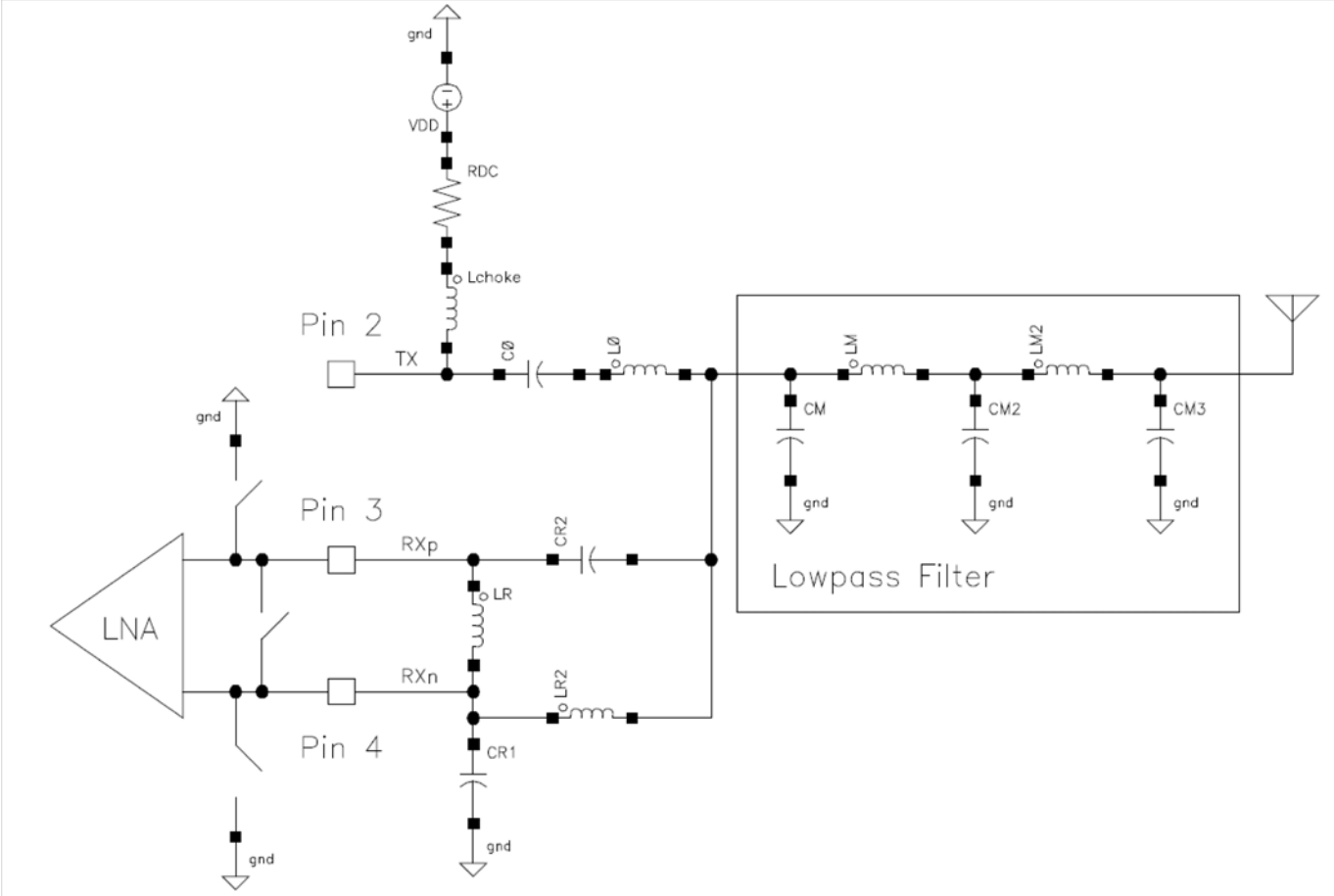

Figure 16. RX Input Switches for Direct Tie Operation

When enabled, these three switches are activated simultaneously upon entering TX mode. The ENABLE function for these switches is controlled by the lna_sw bit D3 in SPI Register 6Dh. If the lna_sw bit is cleared, these switches remain open at all times. If the lna_sw bit is set, these switches are closed during TX mode and remain open during all other modes.

Closing these switches during TX mode effectively shorts the RXp and RXn input pins together, and also shorts them to GND. The effective circuit may be re-drawn as shown in Figure 17. Note that inductor LR2 and capacitor CR2 have been placed in parallel by the closure of the switches, and are connected to GND. If the values of these components are chosen for resonance at the desired operating frequency, a very high impedance is presented to the TX path resulting in very little degradation in TX output power. Also, by shorting the input pins of the LNA together and simultaneously to GND, the LNA is protected from the large signal swing of the TX signal. This feature allows connection of the TX path to the RX path without damage to the LNA.

The lna_sw bit **must** be set for proper operation in a Direct Tie configuration. If this bit is not set, discrete components LR2 and CR2 will **not** present a high impedance to the TX output path and significant reduction in output power will occur.

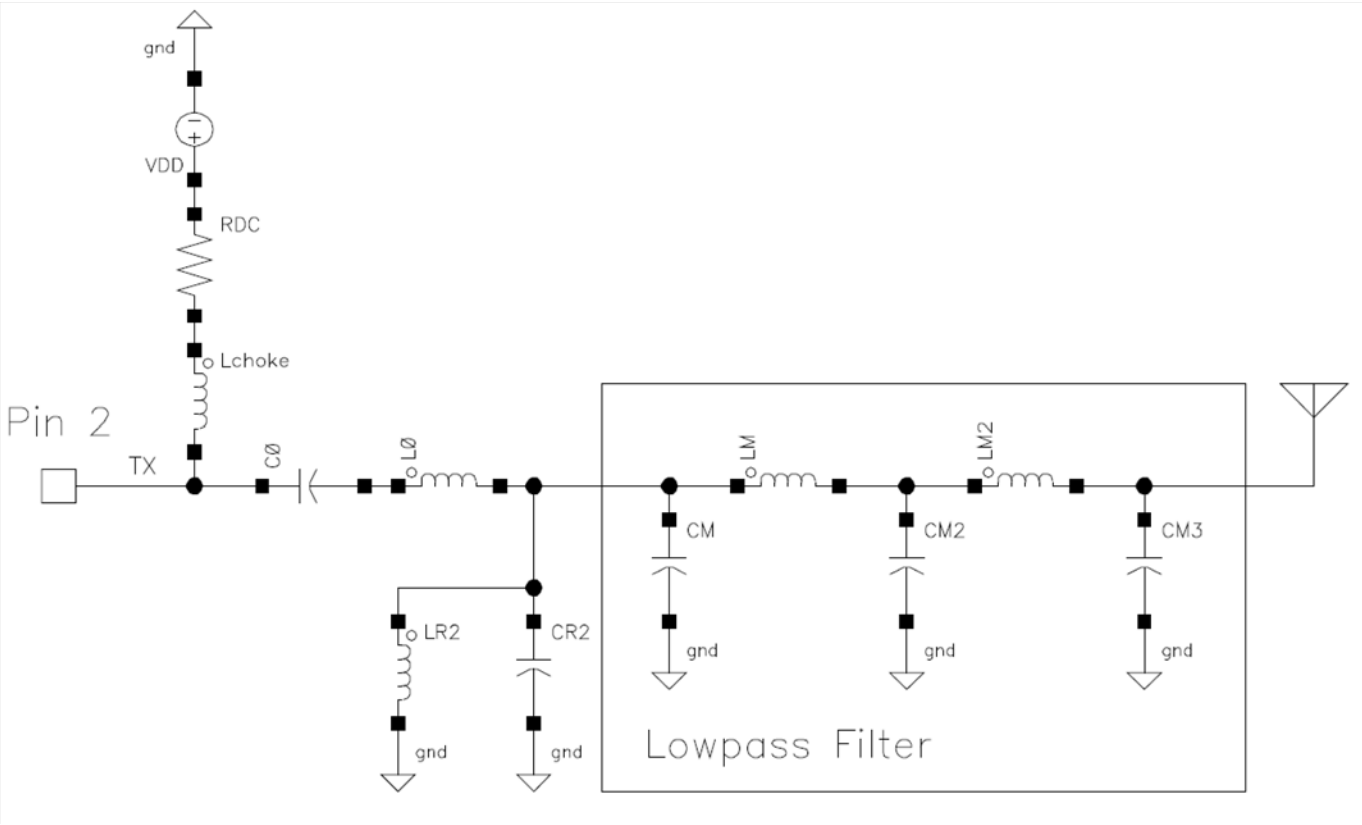

Figure 17. Effective Direct Tie Circuit in TX Mode

In RX mode, the output transistors of the PA are in the OFF state and the impedance seen looking back into the TX pin is comprised mostly of the output capacitance of the transistors. (The impedance of the pull-up inductor L_{CHOKE} is quite high and may be ignored for this discussion.) This output capacitance is effectively in series with matching capacitor C0 and will result in series-resonance with inductor L0 at some frequency, as shown in Figure 18. At this series-resonant frequency, the input to the LNA matching network (LR2-CR2-LR-CR1) is effectively shorted to GND and thus significantly degrades receive performance. As the PA output capacitance C_{PAOFF} is fixed, it is necessary to choose L0 and C0 to ensure that this series-resonance does not excessively degrade RX performance at the desired operating frequency. It may be necessary to alter the values of L0 and/or C0 slightly away from their calculated optimum values in order to accomplish this goal, thus slightly degrading TX performance in an effort to minimize the impact to RX performance.

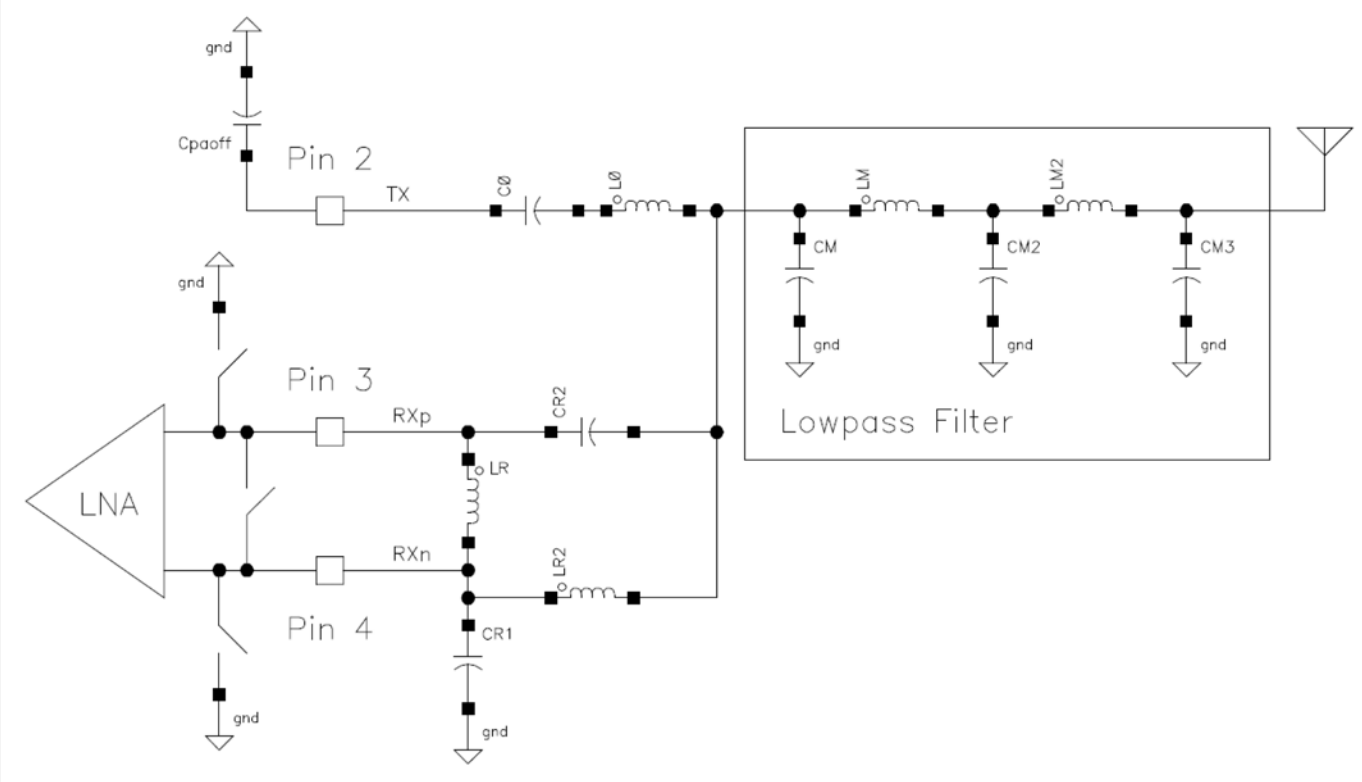

Figure 18. Effective Direct Tie Circuit in RX Mode

We next provide further detail about each step of the matching procedure for the Single Antenna with Direct Tie board configuration. We again assume a general chip supply voltage of V_{DD_RF} = 3.3 V. Our design example will be constructed for the 950 MHz Japanese ARIB band, with a targeted output power level of +10 dBm (the maximum allowed by regulatory standard in this band). For this target output power level, it is sufficient to command the txpow[2:0] field in SPI Register 6Dh to a value of txpow[2:0] = 3'b110. As discussed previously, it is also necessary to set the 'lna_sw' bit D3 in this same register for proper operation in Direct Tie applications.

3.4.1. Steps #1-6: Same Design Procedure as for Split TX/RX Board Configuration

Steps #1 through #6 are exactly the same as those shown in "3.3. Detailed Matching Procedure for Split TX/RX Board Configuration" on page 12.

3.4.2. Step #7: Design RX Input Match

In Step #7, we design an impedance matching network for the differential RX input. The RX matching network is comprised of a total of four inductors and capacitors (LR2-CR2-LR-CR). The goals for this network are as follows:

- Match the LNA input to a 50 Ω source impedance (i.e., the antenna)
- Provide a single-ended to differential conversion function (i.e., a balun)
- Ensure that LR2-CR2 are parallel-resonant at the desired operating frequency

The design equations (and their mathematical derivation) for selection of the matching component values are discussed in detail in "AN427: EZRadioPRO Si433x & Si443x RX LNA Matching". As a result, the following equations are introduced here without proof or further discussion; refer to AN427 for further details.

$$L_{R2} = \frac{\sqrt{50\Omega \times R_{LNA}}}{\omega_{RF}}$$

Equation 12.

$$C_{R2} = \frac{1}{\omega_{RF}^2 \times L_{R2}}$$

Equation 13.

$$C_{R1} = 2 \times C_{R2}$$

Equation 14.

$$L_{LNA} = \frac{1}{\omega_{RF}^2 \times C_{LNA}}$$

Equation 15.

$$L_M = 2 \times L_{R2}$$

Equation 16.

$$L_{R1} = \frac{L_{LNA} \times L_M}{L_{LNA} + L_M}$$

Equation 17.

Note that our goal of parallel-resonance between LR2 and CR2 is inherently satisfied, as evidenced by Equation 13

At any given frequency, the differential input impedance at the RX pins of the chip may be represented by an equivalent parallel R-C circuit; their values are represented by the parameters R_{LNA} and C_{LNA} in the above equations. It is necessary to know these equivalent circuit values at the desired frequency of operation, prior to constructing the match.

The differential input impedance of the RX port on the Si4431 RFIC is provided in “AN427 EZRadioPRO Si433x & Si443x RX LNA Matching”. The values of R_{LNA} and C_{LNA} at a desired operating frequency of 950 MHz are found to be R_{LNA} = 118 Ω and C_{LNA} = 1.66 pF. After plugging these values into the equations above, the following ideal matching component values are calculated:

- LR2 = 12.87 nH
- CR2 = 2.18 pF
- LR1 = 10.20 nH
- CR1 = 4.36 pF

In practice, it is often necessary to slightly modify the matching component values suggested by the above equations. Any printed circuit board layout has parasitics, such as trace inductance or component pad capacitance, and these may have an effect upon the circuit. Silicon Labs has empirically determined that if 0402-size wire-wound inductors are used on the Direct Tie reference board designs available on our website, the actual component values are as shown in the 950 MHz row in Table 2 on page 3, and reproduced below:

- LR2 = 11 nH
- CR2 = 2.2 pF
- LR1 = 10 nH
- CR1 = 4.3 pF

Although not required, it is useful to measure the input impedance seen looking into the RX match, in both RX mode as well as TX mode. Obviously, it is desired to verify a good match to 50 Ω while in RX mode in order to

obtain optimum sensitivity. However, it is also useful to verify that the network provides a high impedance while in TX mode, else the RX circuitry may excessively load down the TX path. Specifically, it may be necessary to slightly adjust the values of LR2 and/or CR2 to achieve optimum parallel resonance at the desired frequency of operation.

The measured impedance at the input of the RX matching network while in RX mode is shown in Figure 19. It is observed that the input impedance is quite close to 50 Ω, with the network providing S_{11} with better than 15 dB return loss.

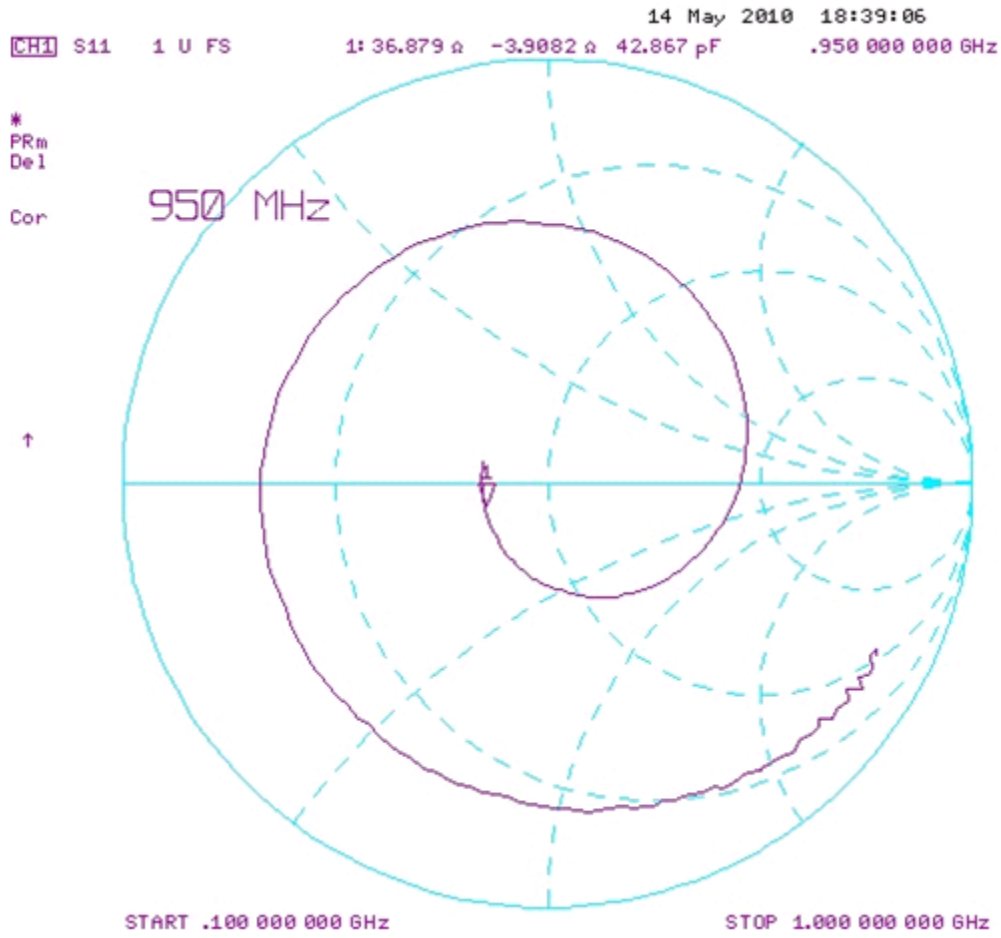

Figure 19. RX Match Input Impedance in RX Mode

In TX mode the switches at the input of the LNA (refer to Figure 16) are in their CLOSED position, and thus LR2 and CR2 form a parallel-resonant network which isolates the RX path from the TX path. As a result, we expect to measure a very high impedance at the input to the RX match network. The actual measured impedance while in TX mode is shown in Figure 20 and confirms this expectation; the measured impedance at 950 MHz is nearly 840 Ω. The slight series capacitance (~1.5 pF) may be ignored, as it corresponds to an equivalent parallel capacitance of approximately 0.03 pF (i.e., negligible).

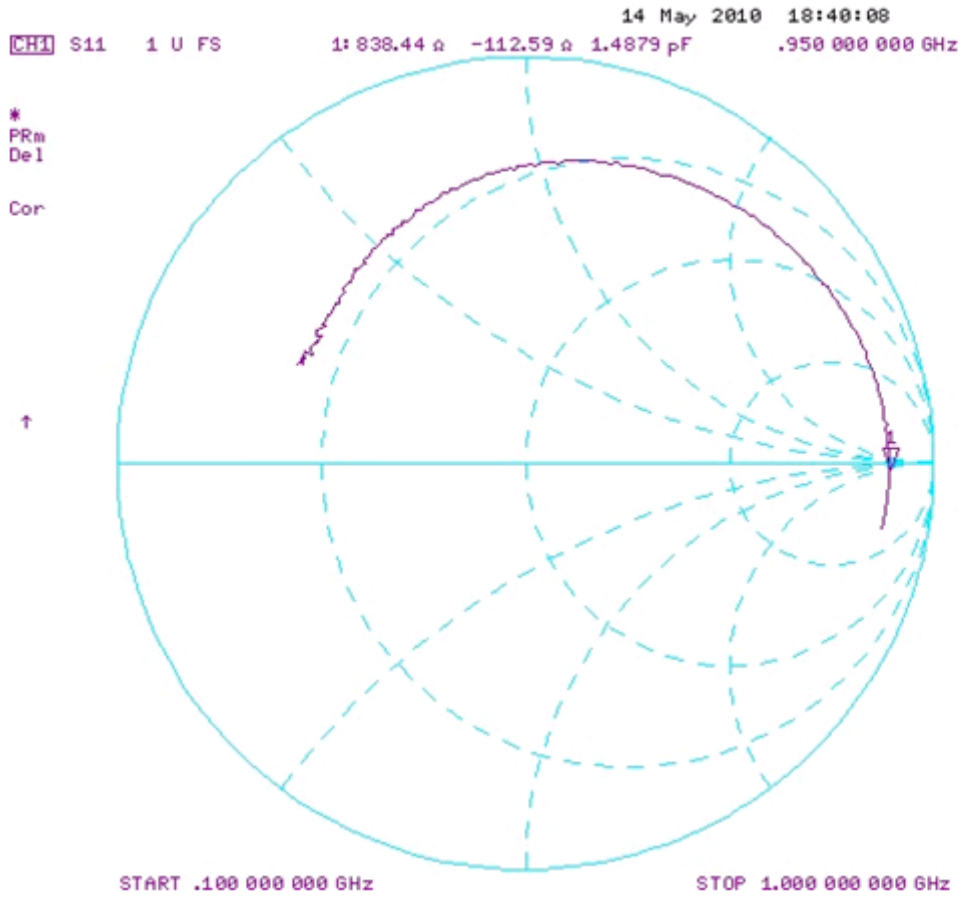

Figure 20. RX Match Input Impedance in TX Mode

3.4.3. Step #8: Slightly Modify the Value of L0

In Step #8, we deliberately mis-tune the value of matching inductor L0 slightly away from its optimum value, as determined in Steps #1-6. As illustrated in Figure 18 on page 30, the series-resonance of L0-C0-C_{PAOFF} has the potential for significantly degrading the RX performance by placing a (near) short to GND at the input of the RX matching network. It is important that this series-resonant frequency be adjusted to fall sufficiently far away from the desired operating frequency in order to minimize its effect upon RX sensitivity.

This is accomplished by deliberately increasing the value of L0 by approximately 20% above its optimum calculated value. This will push the unwanted resonance lower in frequency and minimize its effect upon RX performance. Some post-tuning of capacitor CM may also be required to improve Class-E operation after the change in value of L0.

The value of PA output capacitance in its OFF state may be somewhat different than the value of internal shunt drain capacitance C_{SHUNT} (discussed in "3.3.3. Step #3: Calculate the Required Value for ZLOAD" on page 13). The value of C_{PAOFF} may be measured with a network analyzer connected to the TX output pin with all matching components removed, except for those providing dc bias (i.e., L_{CHOKE} and R_{DC}). Silicon Labs has performed this measurement and determined the value of C_{PAOFF} ~ 3.8 pF in the frequency range of 868 to 950 MHz. This is shown by the impedance measurement of Figure 21. The value of L_{CHOKE} must be chosen appropriately to provide a very high impedance at the frequency of interest, else the measured value of C_{PAOFF} may be affected.

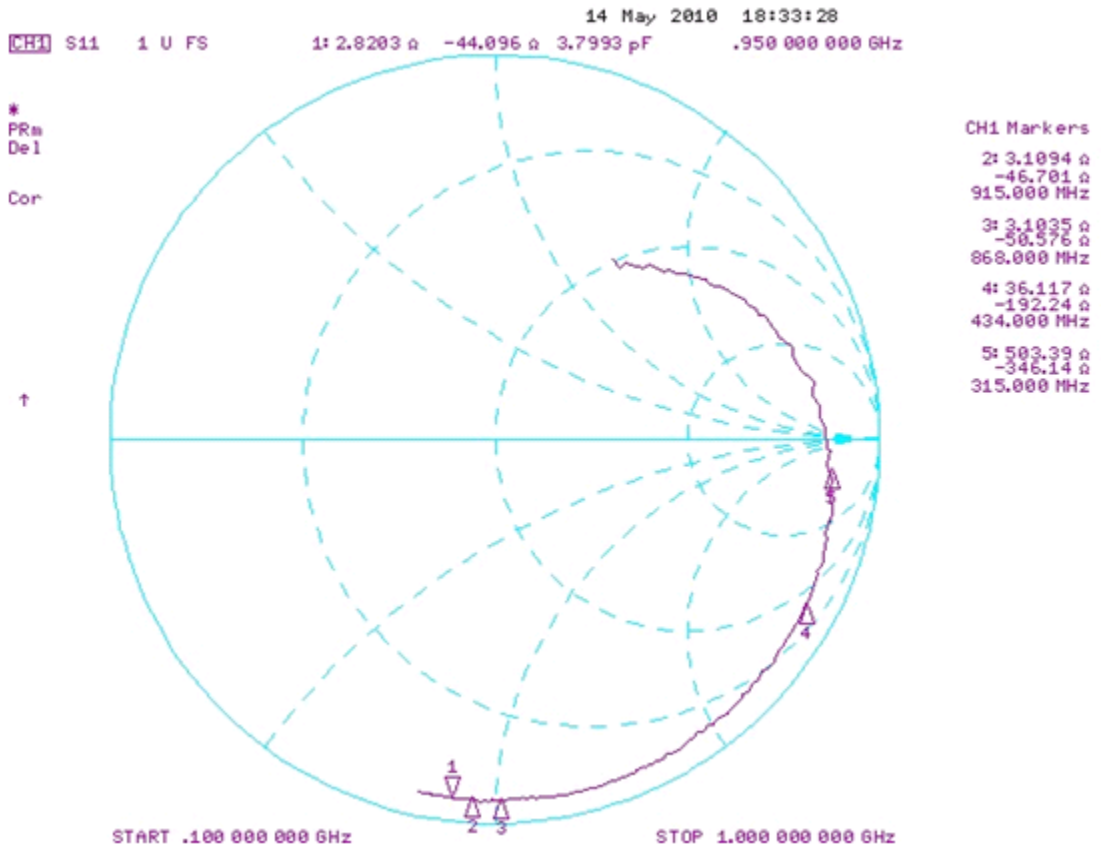

Figure 21. PA Output Capacitance Measurement in OFF State

Once the value of C_{PAOFF} has been determined, its effect upon RX performance may be estimated. Continuing with our design example at 950 MHz, we find the initial values of L0-C0 to be the following:

- L0 = 12 nH
- C0 = 5.1 pF

This value of capacitance of C0 is in series with C_{PAOFF} = 3.8 = pF, resulting in an equivalent series capacitance of C_{EQUIV} = 2.18 = pF. The series-resonant behavior of the resulting L-C circuit may be simulated, and is shown in Figure 22.

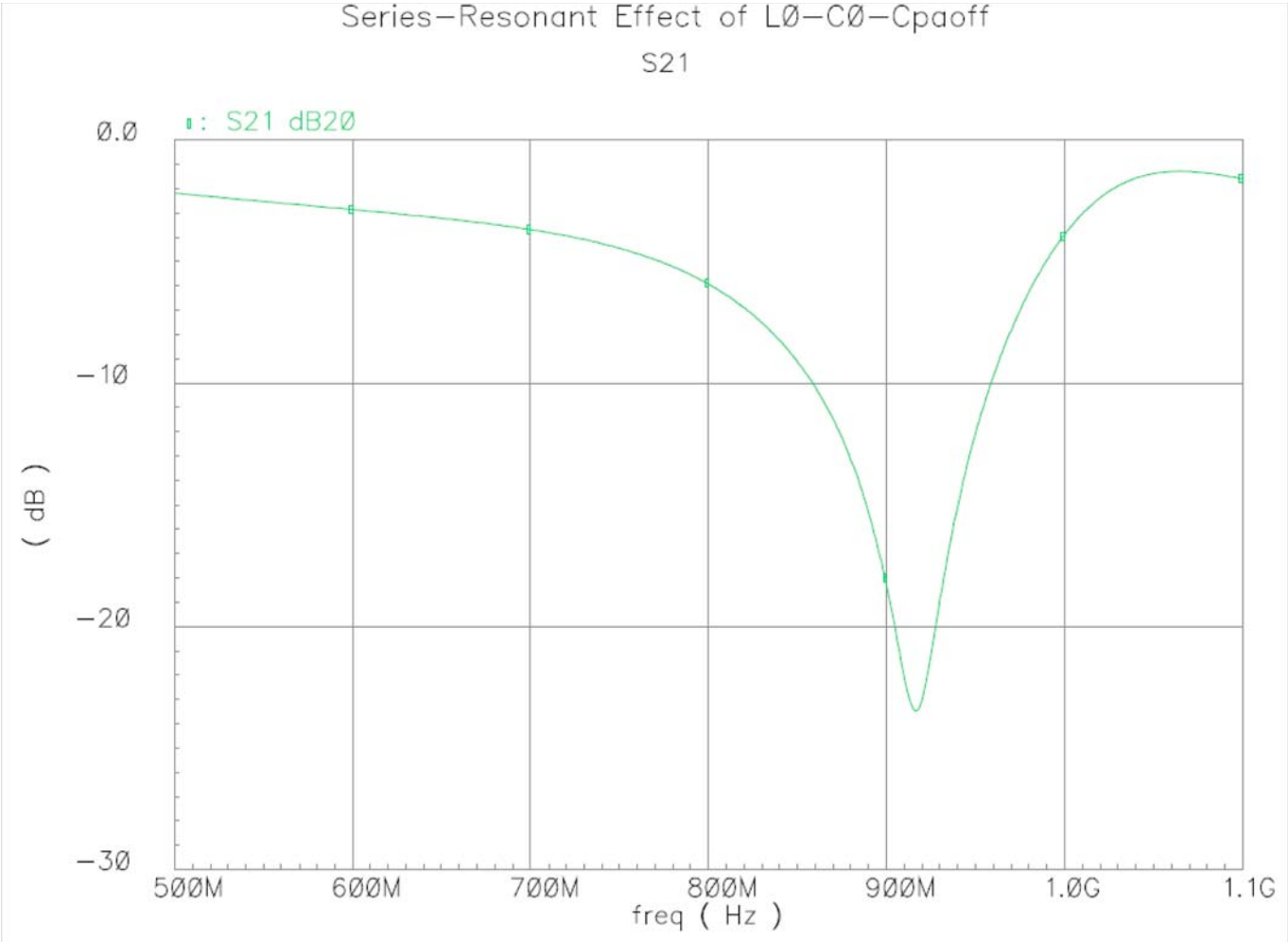

Figure 22. Series-Resonance Behavior of Initial L0-C0 Circuit

It is observed that this L0-C0-C_{PAOFF} circuit introduces ~8 dB of loss at 950 MHz. As this circuit is directly connected to the input of the RX match, this will result in approximately 8 dB of degradation in RX sensitivity.

The resonant frequency of these circuit components may be shifted further downwards (away from the desired operating frequency) by increasing the value of L0. Using our rule-of-thumb of increasing L0 by ~20%, we arrive at a modified value of L0 = 15 nH. Simulation of the series-resonant behavior of the modified circuit is shown in Figure 23. It is seen that the loss at 950 MHz has now been improved significantly to only ~1.5 dB. While this still represents a 1.5 dB reduction in RX sensitivity, this is a good compromise between TX and RX performance.

It would also be possible to lower the resonant frequency of the L0-C0-C_{PAOFF} circuit by increasing the value of C0 instead of L0. However, as C0 is in series with C_{PAOFF}, a larger change in value must occur to provide the same amount of mistuning. This stronger mistuning will result in even greater reduction in performance in TX mode. Therefore, tuning of L0 is preferred and generally results in better compromise between TX and RX performance.

This increase in the value of L0 is only required when working in the upper frequency bands (e.g., 868/915/950 MHz). In the lower frequency bands (315/390/434 MHz), the values of L0 and C0 obtained for the Split TX/RX board configuration continue to work well with the Direct Tie board configuration.

In the final circuit realization on Silicon Labs reference design boards, the value of capacitor CM was reduced to 4.3 pF to provide slightly better TX output power. Also, the value of inductor LM2 was increased to 13 nH to provide better suppression of the 2nd harmonic. The final element values for 950 MHz are summarized in Table 2 on page 3.

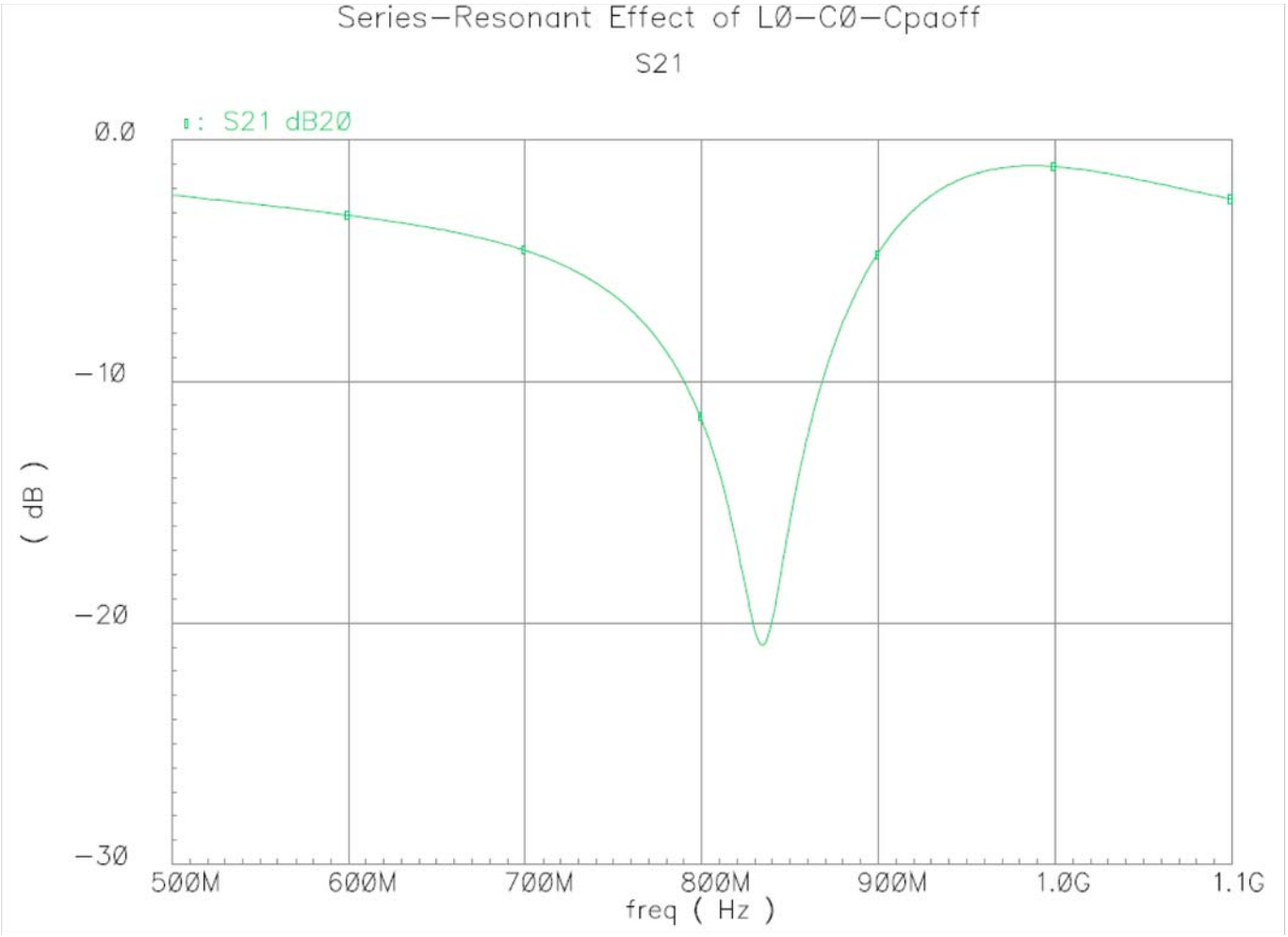

Figure 23. Series-Resonance Behavior of Modified L0-C0 Circuit

Note that some small degradation in both TX and RX performance is expected for a Direct Tie configuration. That is, it is not possible to directly connect the TX and RX paths together and achieve perfect isolation between the two circuit functions; each path will result in some amount of unwanted loading to the other path, and thus some small degradation in performance (relative to a Split TX/RX board configuration in which the TX and RX paths remain entirely separate). The choice of matching inductor L0 heavily impacts the tradeoff between optimizing for TX output power at the expense of degraded RX sensitivity, or vice versa. A value may generally be found which achieves a good compromise between the two, typically resulting in less than 1 dB reduction in TX output power and no more than 2–3 dB reduction in RX sensitivity. Some amount of “tweaking” of the final values of L0 and CM may be necessary to achieve this best compromise.

3.4.4. Summary of Match

This completes the steps of the match design process for the Direct Tie board configuration. This match design process may be used to obtain matching component values at any desired operating frequency. Summary tables of these matching component values are shown in Table 2 on page 3 and Table 3 on page 4.

4. Measured Spectrum Plots

The following section presents some measured spectral data on different board configurations at a variety of frequencies. Measured results for circuit realizations with both wire-wound inductors and multi-layer inductors are presented.

It is important to note that, due to the high power difference between the fundamental and harmonics, the dynamic range of the applied spectrum analyzer is often critical, and the measured harmonic levels can easily be higher than its real value.

An immediate practical solution for this problem would be to use a high-pass filter, such as Mini-Circuits VHF-1200 (1.2 GHz high-pass cutoff frequency) for dedicated harmonic measurements. Unfortunately, in this case, the termination impedance at the fundamental frequency is no longer 50 Ω, which distorts the voltage waveform at the TX pin and thus the switching PA operation.

In order to avoid this, a 10 dB attenuator should be connected between the HPF and the radio output. In this way, the PA observes a minimum return loss of 20 dB at all frequencies, and the fundamental operation of the switching mode PA does not change.

For example, consider the 950 MHz Japanese ARIB band measurement where the required second harmonic level should be below –55 dBm with a simultaneous fundamental level of +10 dBm. This problem may be demonstrated on the 950 MHz direct tie board with wire-wound inductors (a typical measured second harmonic level when the board output is connected directly to the spectrum analyzer input is shown in Figure 41). Here, the reference level of the spectrum analyzer is set to +10 dBm, i.e. to the lowest possible level that can handle the +9.5 dBm fundamental power. With this setting, the spectrum analyzer automatically configures its input to insert a 20 dB input attenuator, which increases the broadband noise floor (including at the second harmonic frequency). The ARIB T96 standard requires measurement of the second harmonic using a 1 MHz RBW; however, with such a wide measurement bandwidth the spectrum analyzer is likely close to its dynamic range limit. In such a case, it is questionable whether the measured second harmonic level is the real value or a false value caused by the harmonic distortion of the spectrum. To answer this question, the Si4431 output is connected to the spectrum analyzer through the 10 dB attenuator and the HPF. The fundamental power is thus reduced to ~ –26 dBm and the reference level of the spectrum analyzer can be reduced to –25 dBm, resulting in only 10 dB input attenuator setting on the analyzer. The external 10 dB attenuator may easily be compensated in the displayed results by using the amplitude offset function of the analyzer. The measured second harmonic is shown in Figure 42 with attenuator compensation. The noise floor is nearly the same (~ –66 dBm) as the total input attenuation is unchanged, but no second harmonic can be observed. This means that the original ~ –60 dBm second harmonic level in Figure 41 is generated purely by the harmonic distortion of the spectrum analyzer. By using the combination of the external attenuator plus HPF, the harmonic distortion of the spectrum analyzer is greatly reduced, but the measurement is still limited by the analyzer's dynamic range. From the point of view of compliance with the ARIB T96 standard, this is not a problem, as the second harmonic level complies with at least 10 dB margin. However, to see the real second harmonic level, the dynamic range of the spectrum analyzer is further improved by decreasing the RBW to 30 kHz in Figure 43. Due to the applied CW signal, the lower RBW does not change the harmonic power significantly, while the noise level is reduced. As can be seen, the second harmonic level is around –71 dBm with this method of measurement.

4.1. Split TX/RX Board Configurations with Wire-Wound Inductors

4.1.1. 315 MHz, VDD=3.3V, txpow[2:0]=3'b111

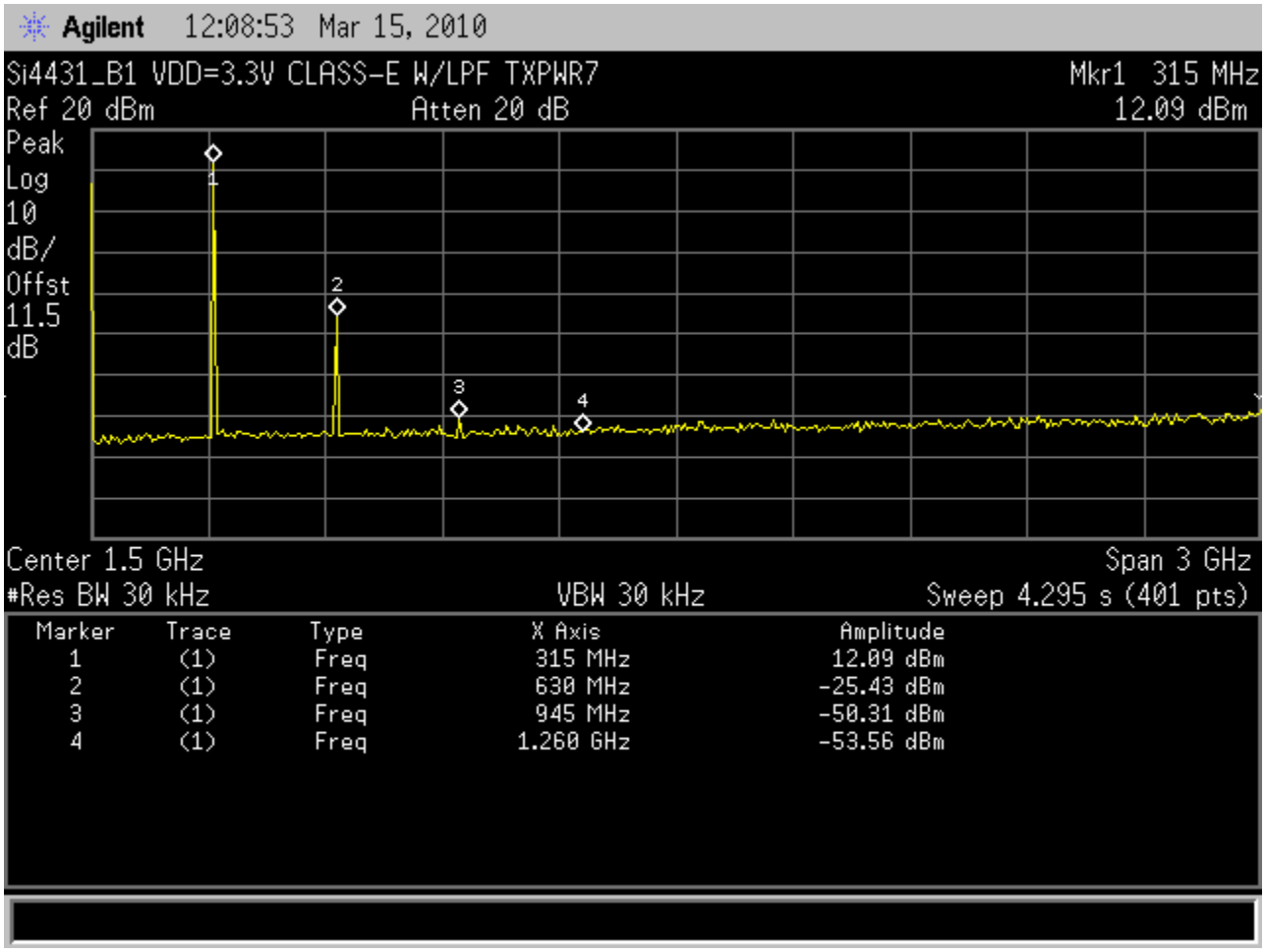

Figure 24. Split TX/RX Board at 315 MHz with Wire-Wound Inductors

4.1.2. 434 MHz, V_{DD} = 3.3 V, txpow[2:0]=3'b111

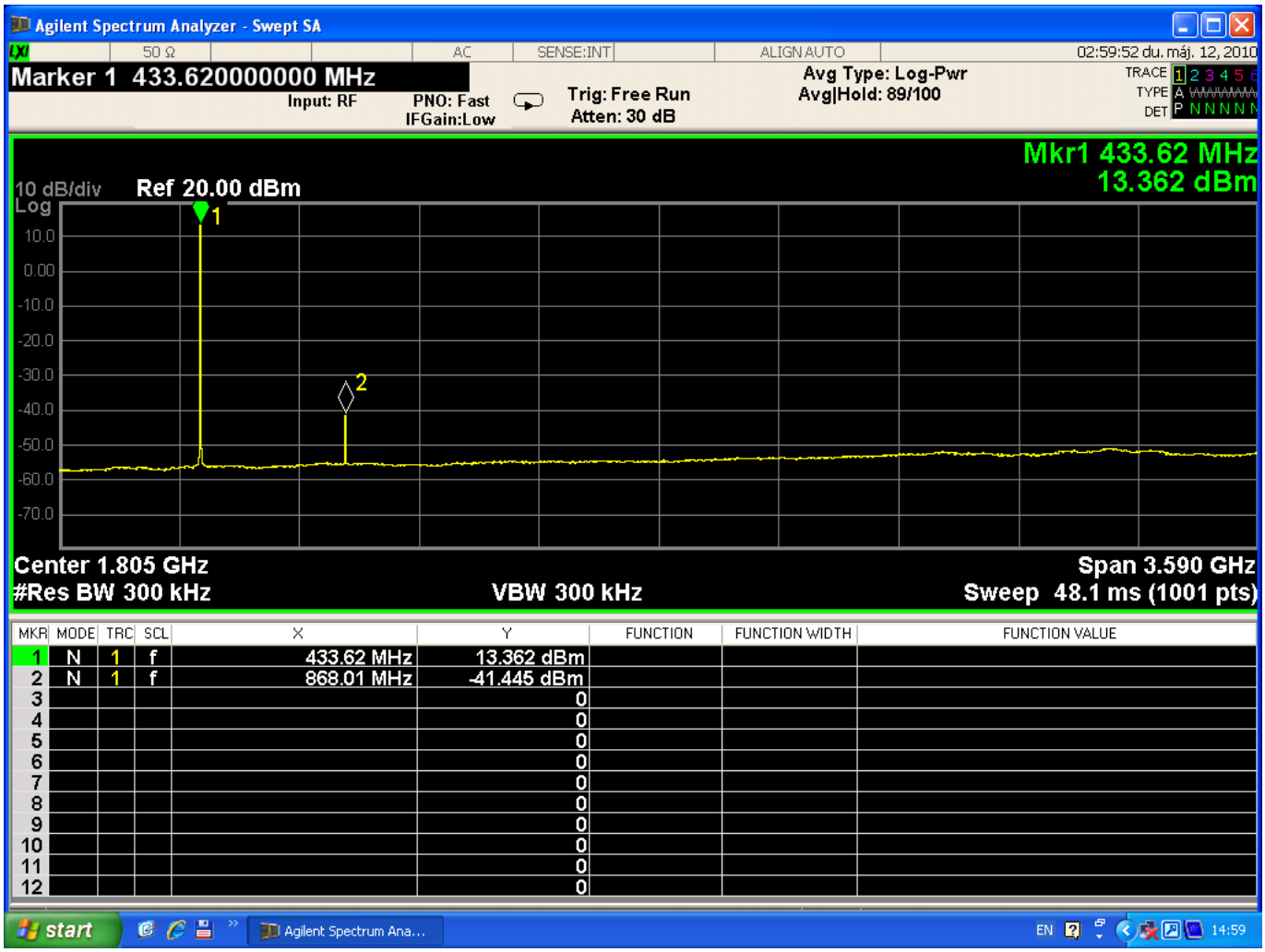

Figure 25. Split TX/RX Board at 434 MHz with Wire-Wound Inductors

4.1.3. 868 MHz, V_{DD} = 3.3 V, txpow[2:0]=3'b111

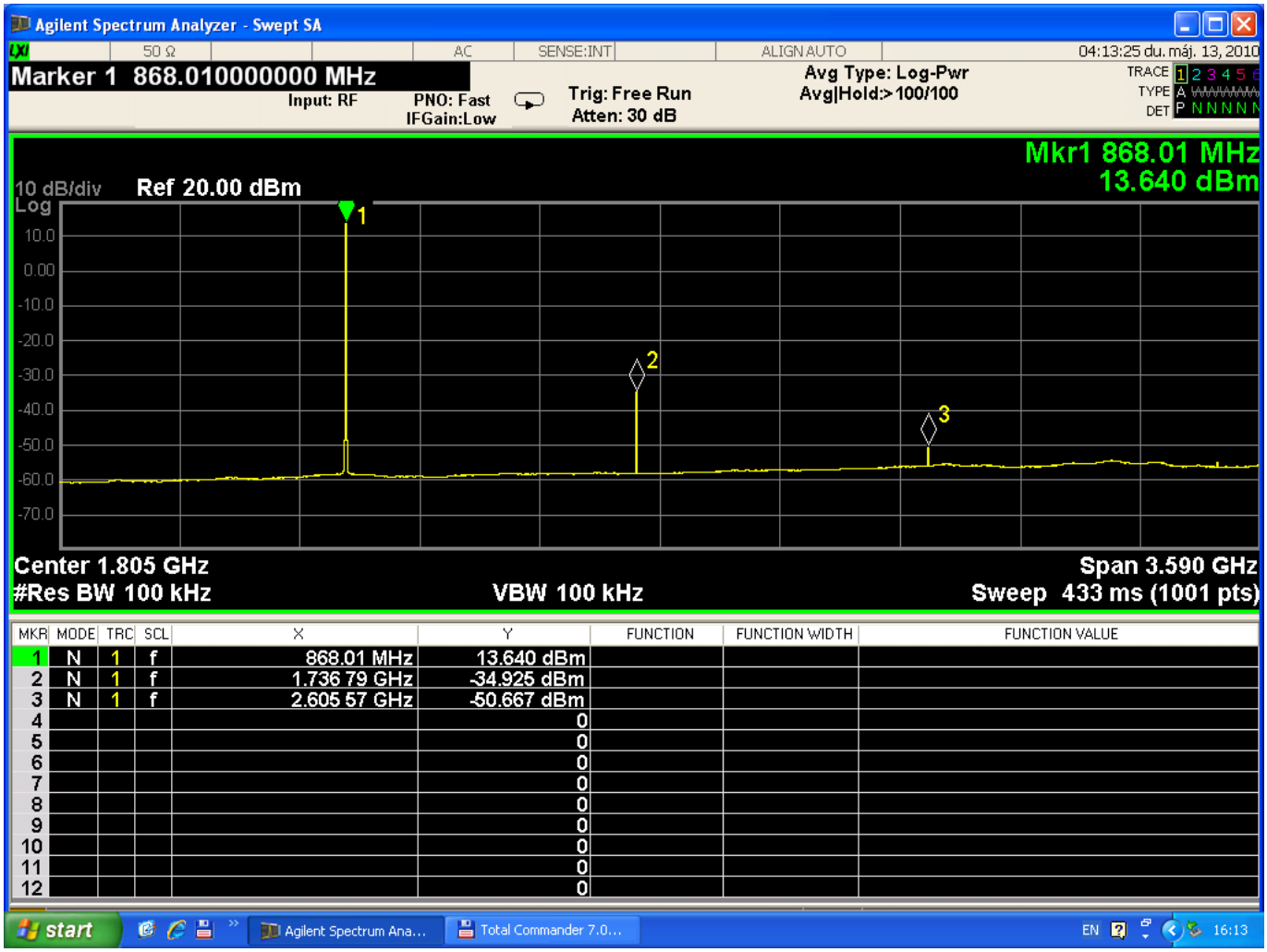

Figure 26. Split TX/RX Board at 868 MHz with Wire-Wound Inductors

4.1.4. 915 MHz, V_{DD} = 3.3 V, txpow[2:0]=3'b111

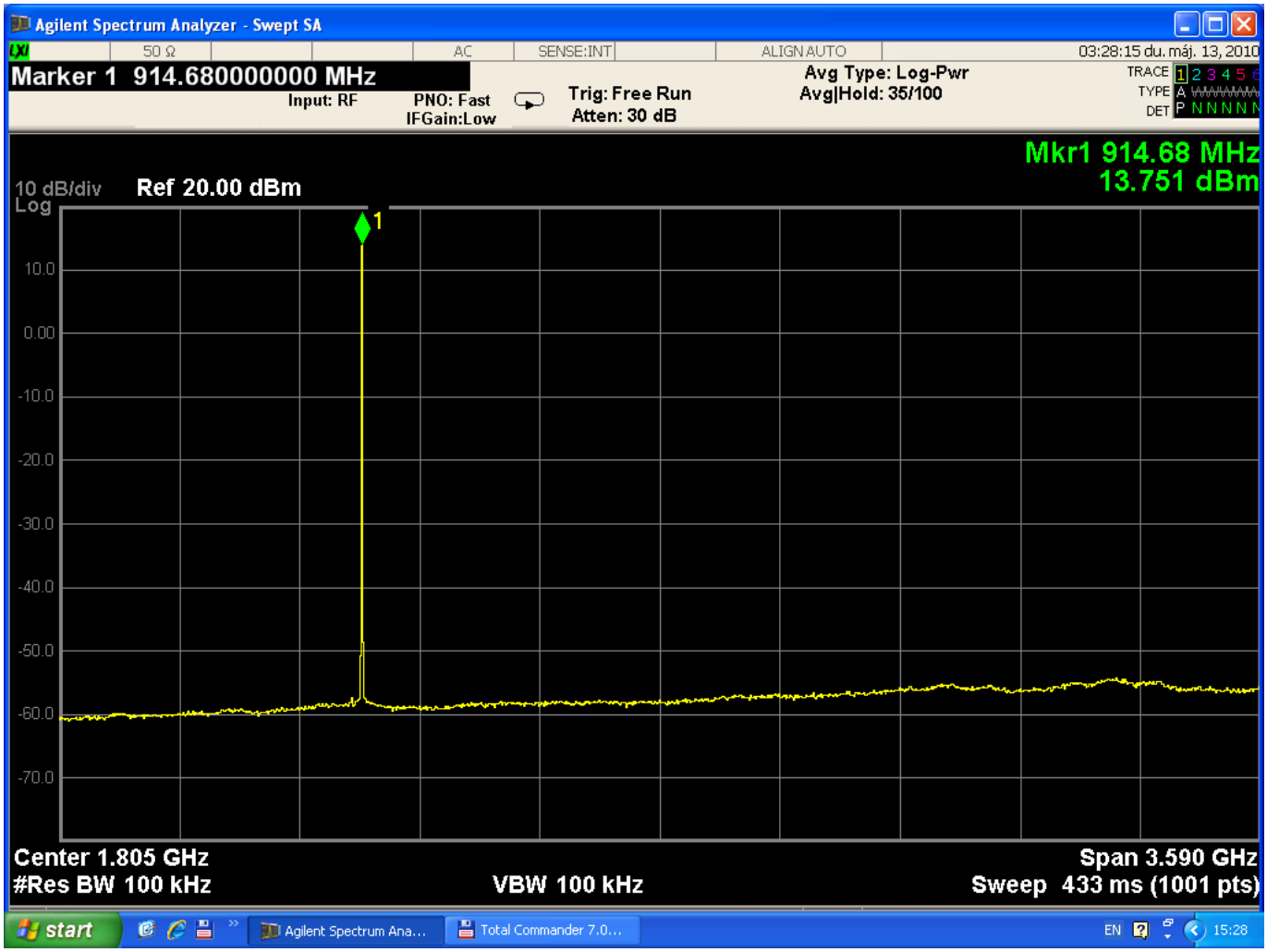

Figure 27. Split TX/RX Board at 915 MHz with Wire-Wound Inductors

4.1.5. 950 MHz, V_{DD} = 3.3 V, txpow[2:0]=3'b110

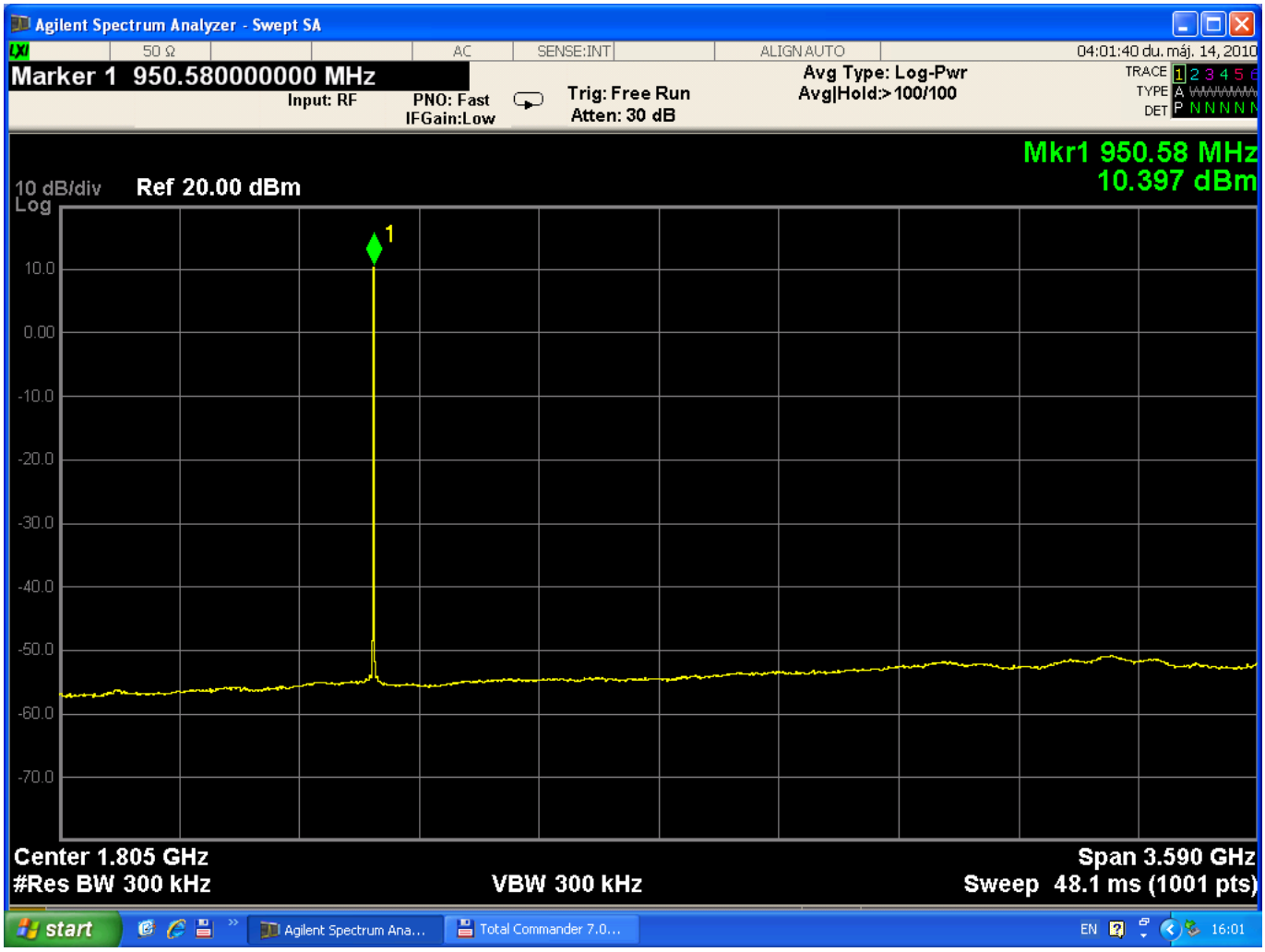

Figure 28. Split TX/RX Board at 950 MHz with Wire-Wound Inductors

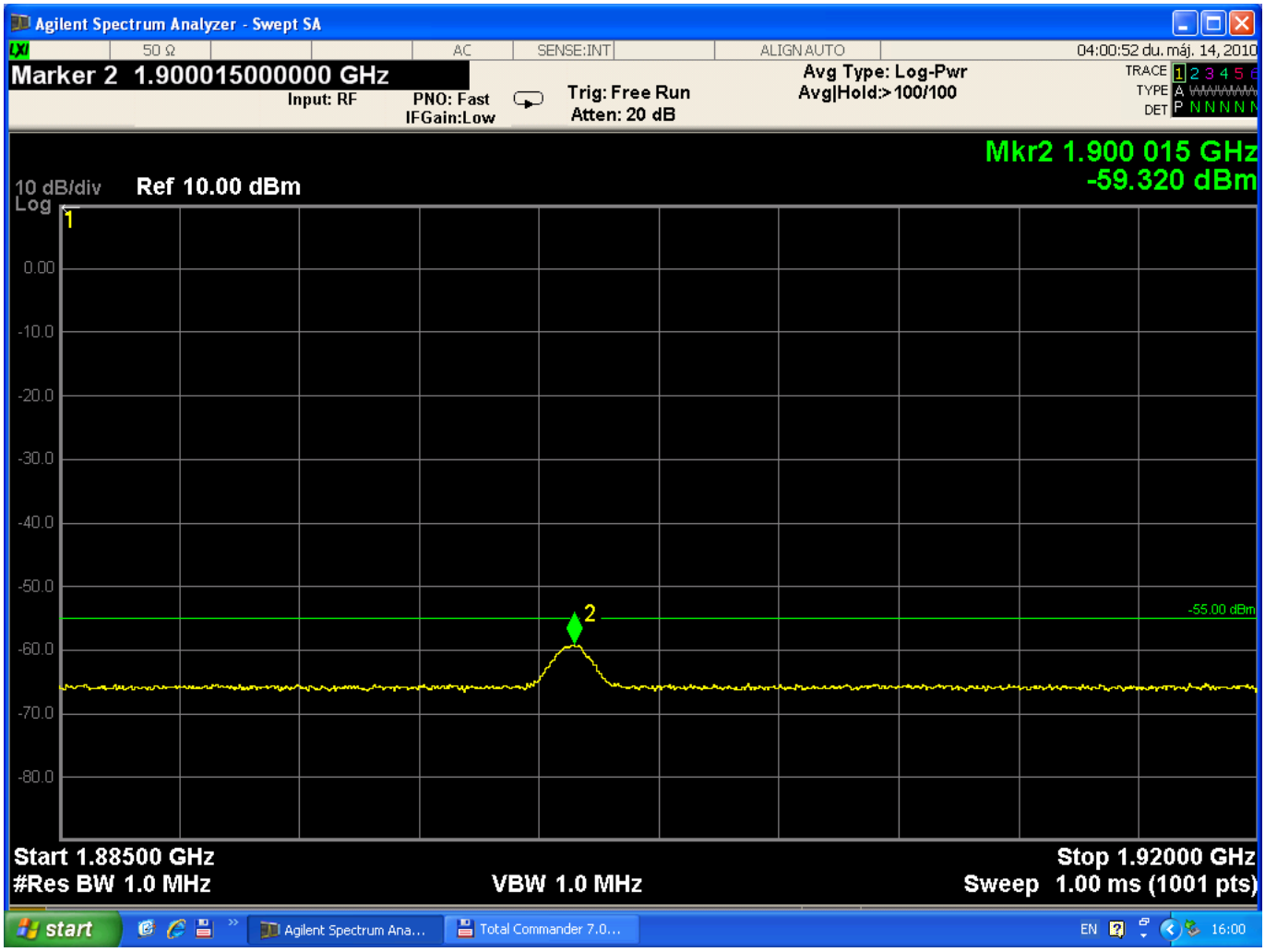

Figure 29. Split TX/RX Board at 950 MHz with Wire-Wound Inductors (zoom-in of 2nd Harmonic)

4.2. Split TX/RX Board Configurations with Multilayer Inductors

4.2.1. 315 MHz, V_{DD} = 3.3 V, txpow[2:0]=3'b111

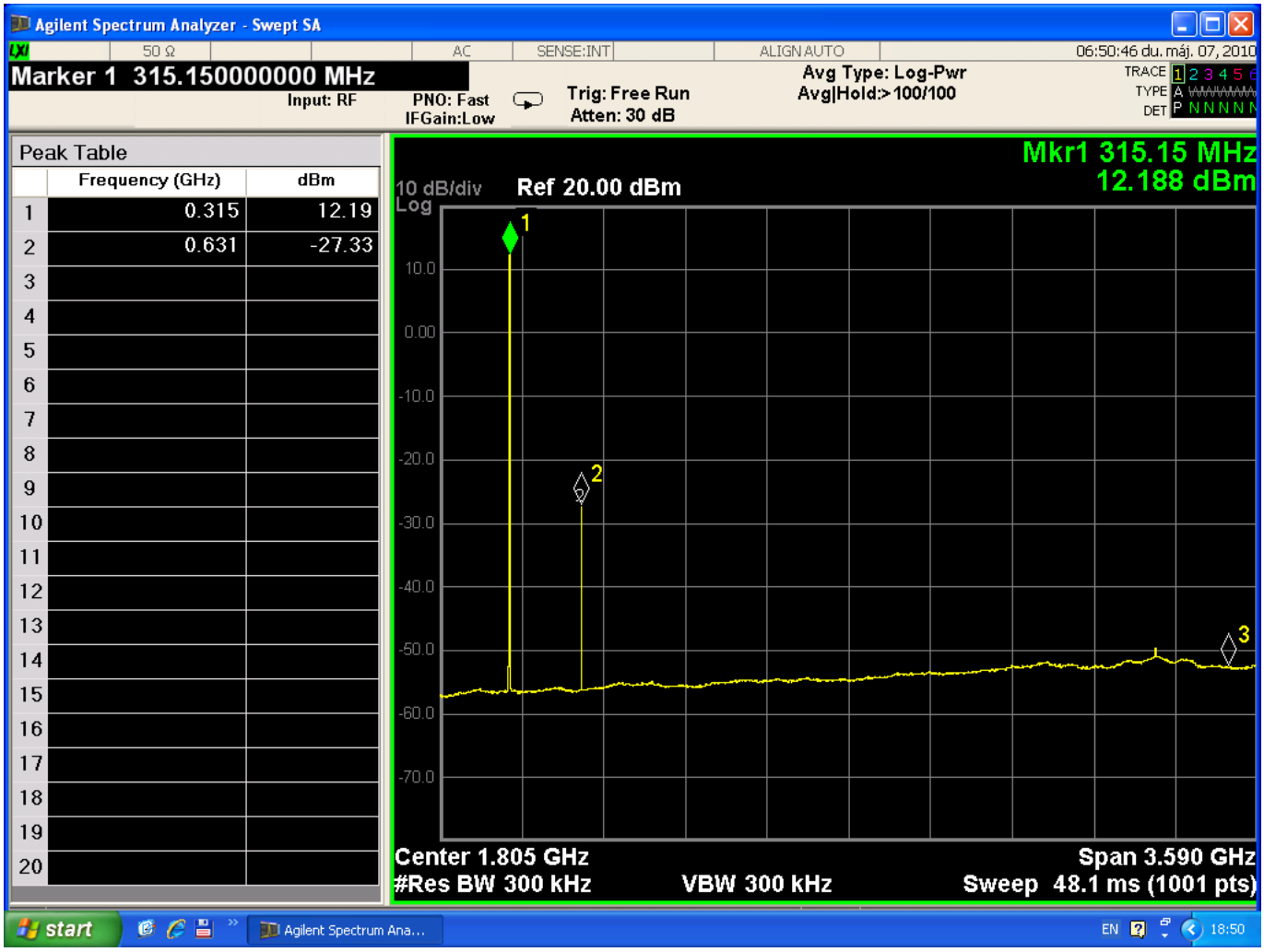

Figure 30. Split TX/RX Board at 315 MHz with Multilayer Inductors

4.2.2. 434 MHz, VDD=3.3V, txpow[2:0]=3'b111

Figure 31. Split TX/RX Board at 434 MHz with Multilayer Inductors

4.2.3. 868 MHz, VDD=3.3V, txpow[2:0]=3'b111

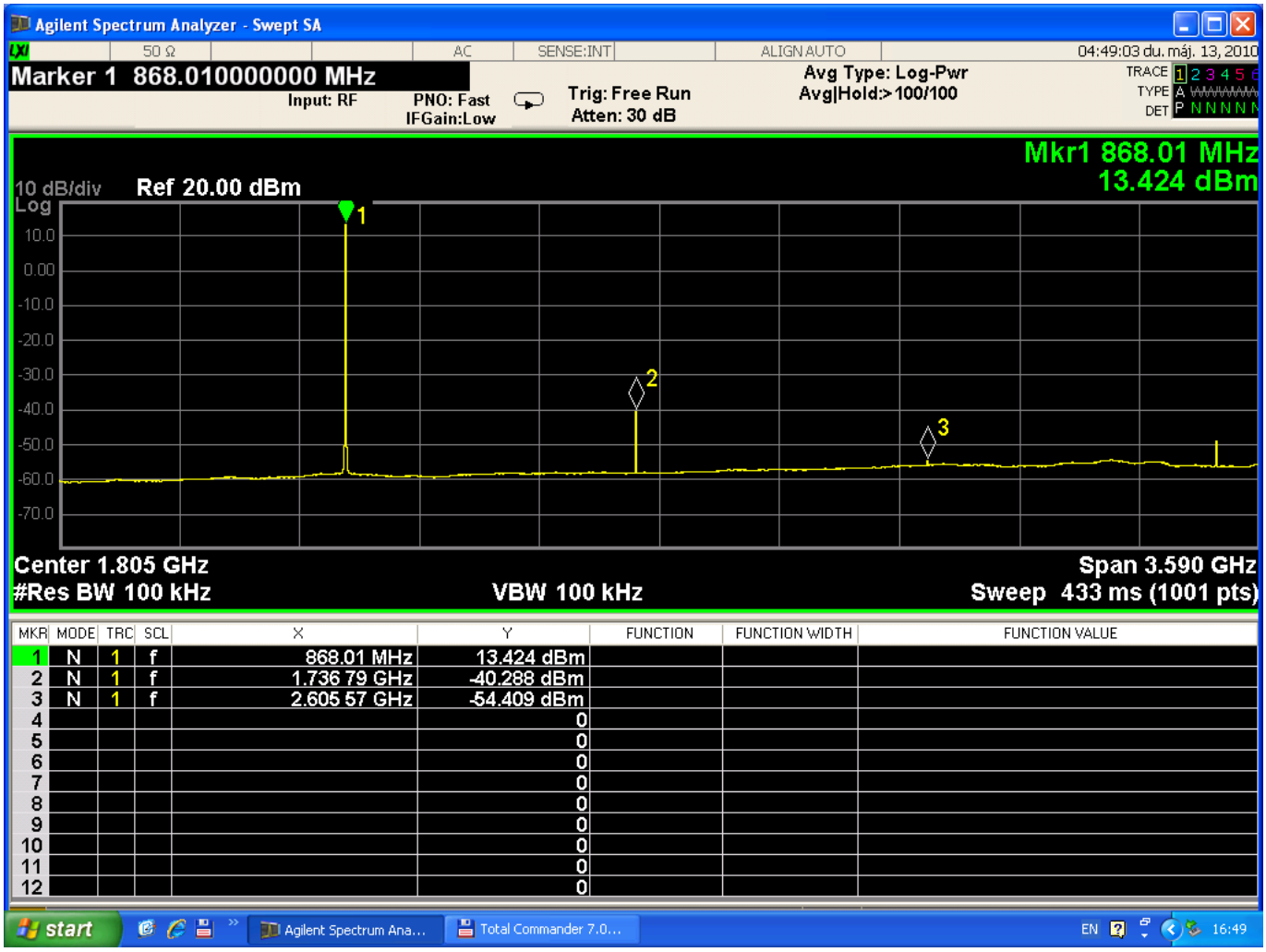

Figure 32. Split TX/RX Board at 868 MHz with Multilayer Inductors

4.2.4. 915 MHz, V_{DD} = 3.3 V, txpow[2:0]=3'b111

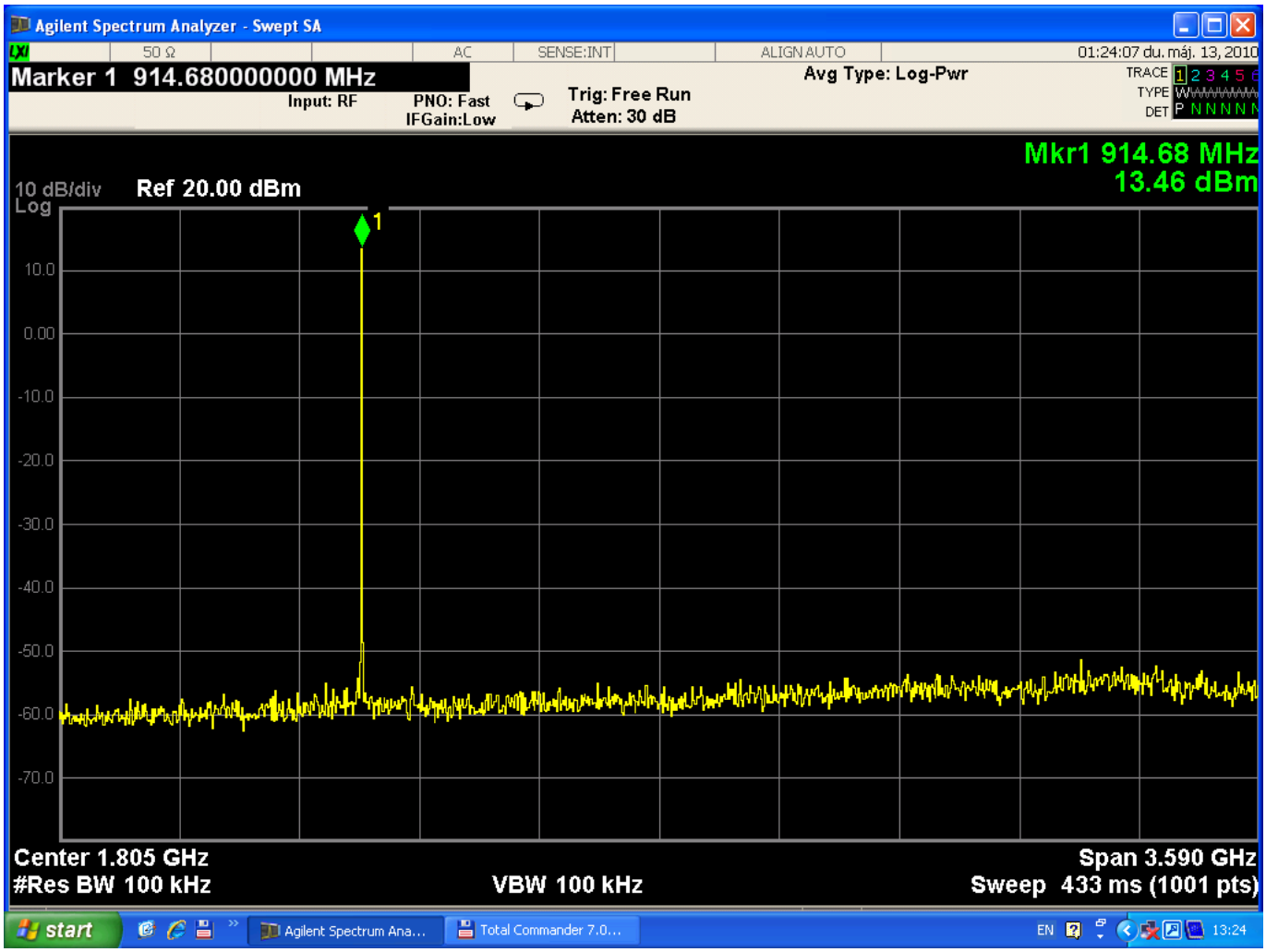

Figure 33. Split TX/RX Board at 915 MHz with Multilayer Inductors

4.2.5. 950 MHz, V_{DD} = 3.3 V, txpow[2:0]=3'b110

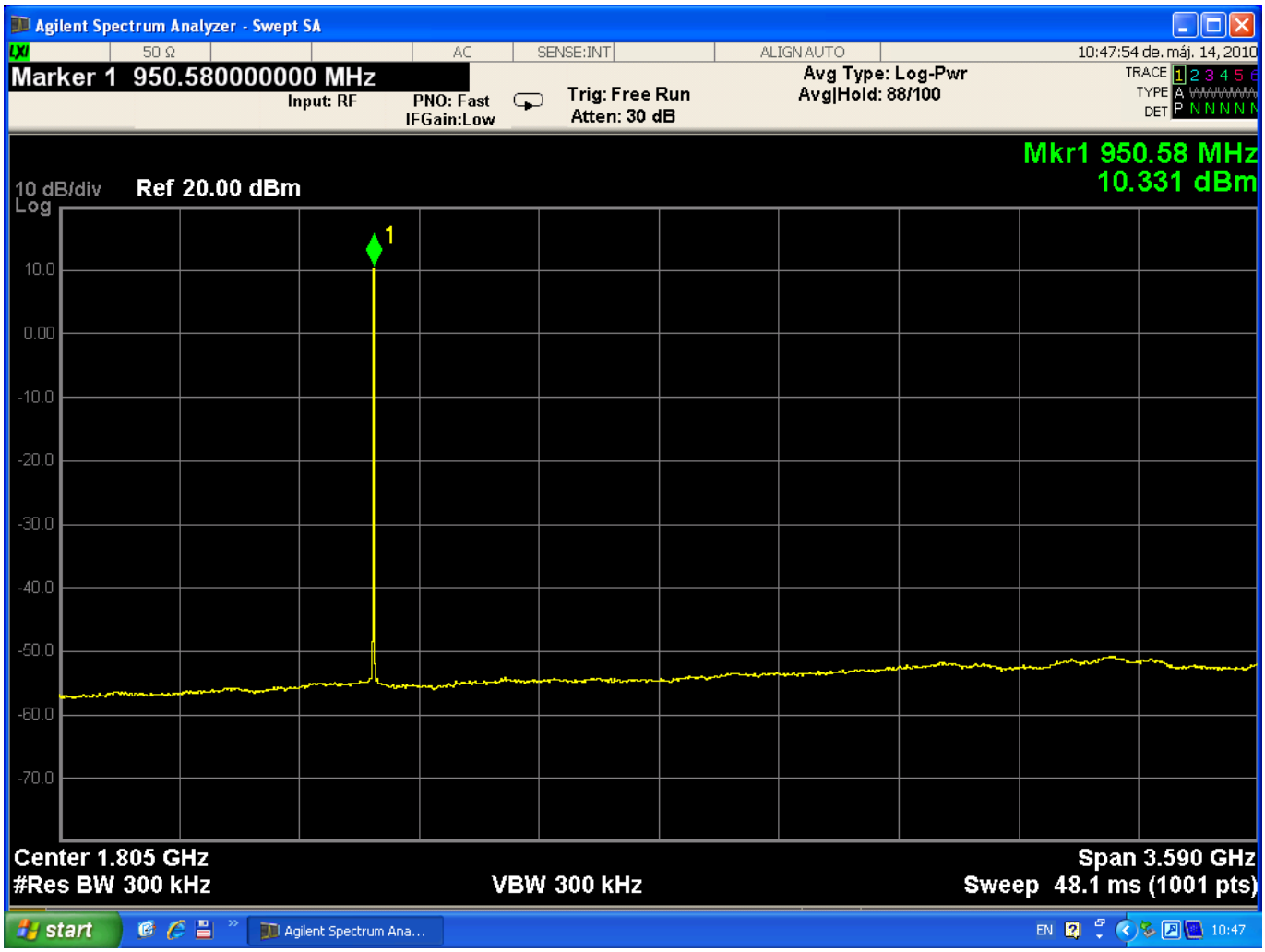

Figure 34. Split TX/RX Board at 950 MHz with Multilayer Inductors

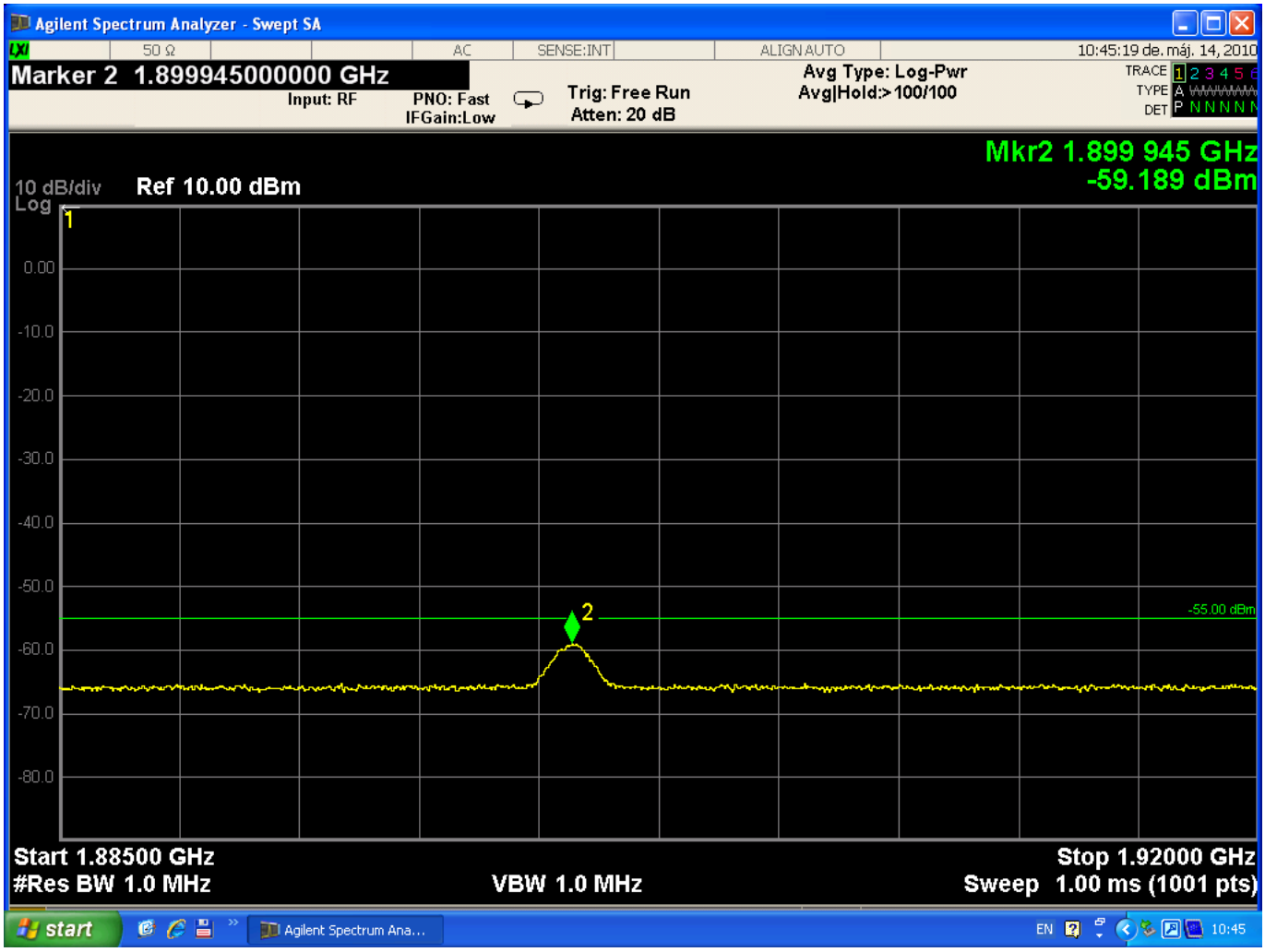

Figure 35. Split TX/RX Board at 950 MHz with Multilayer Inductors (zoom-in of 2nd Harmonic)

4.3. Direct Tie Board Configurations with Wire-Wound Inductors

4.3.1. 315 MHz, V_{DD} = 3.3 V, txpow[2:0]=3'b111

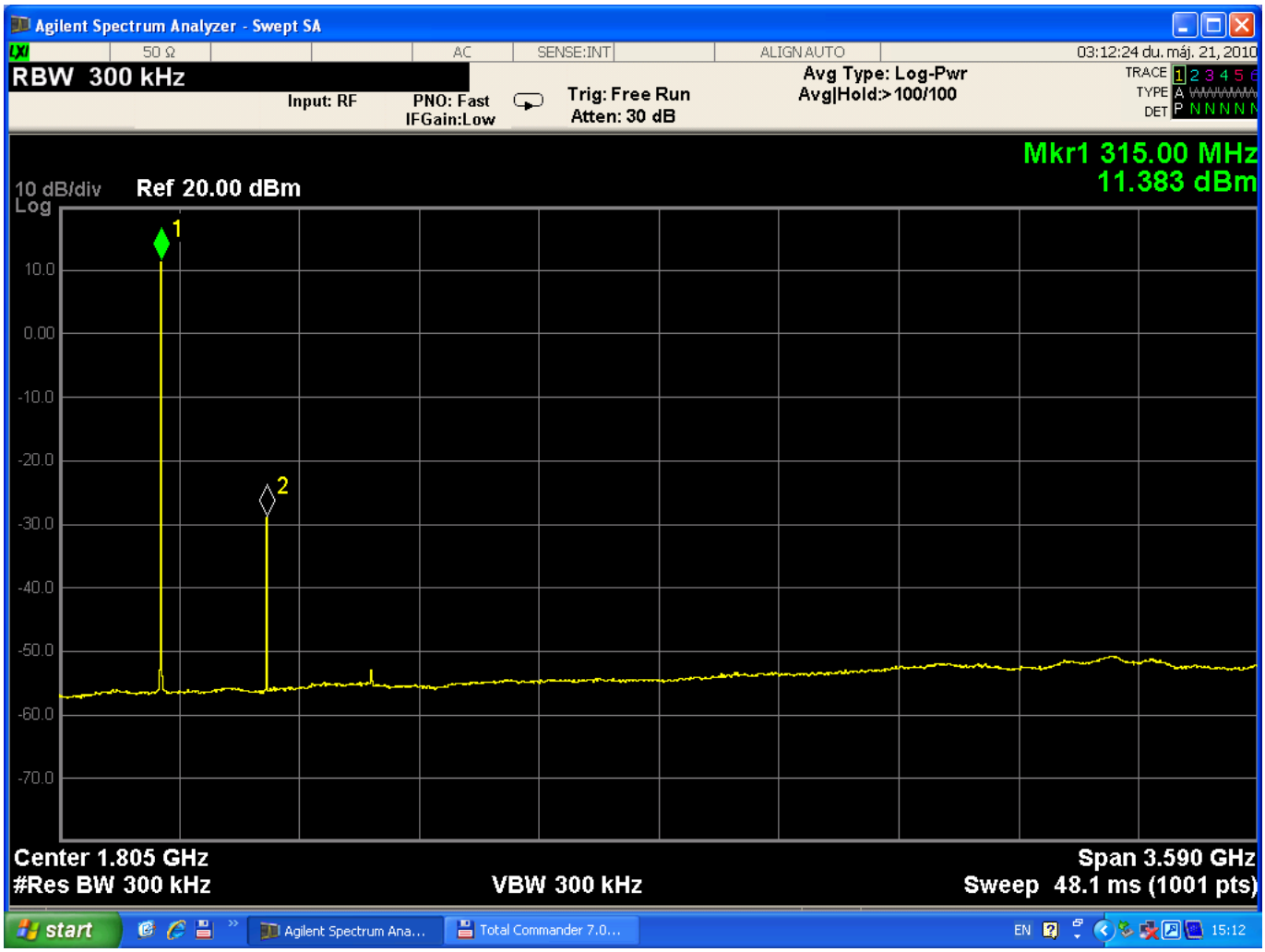

Figure 36. Direct Tie Board at 315 MHz with Wire-Wound Inductors

4.3.2. 434 MHz, V_{DD} = 3.3 V, txpow[2:0]=3'b111

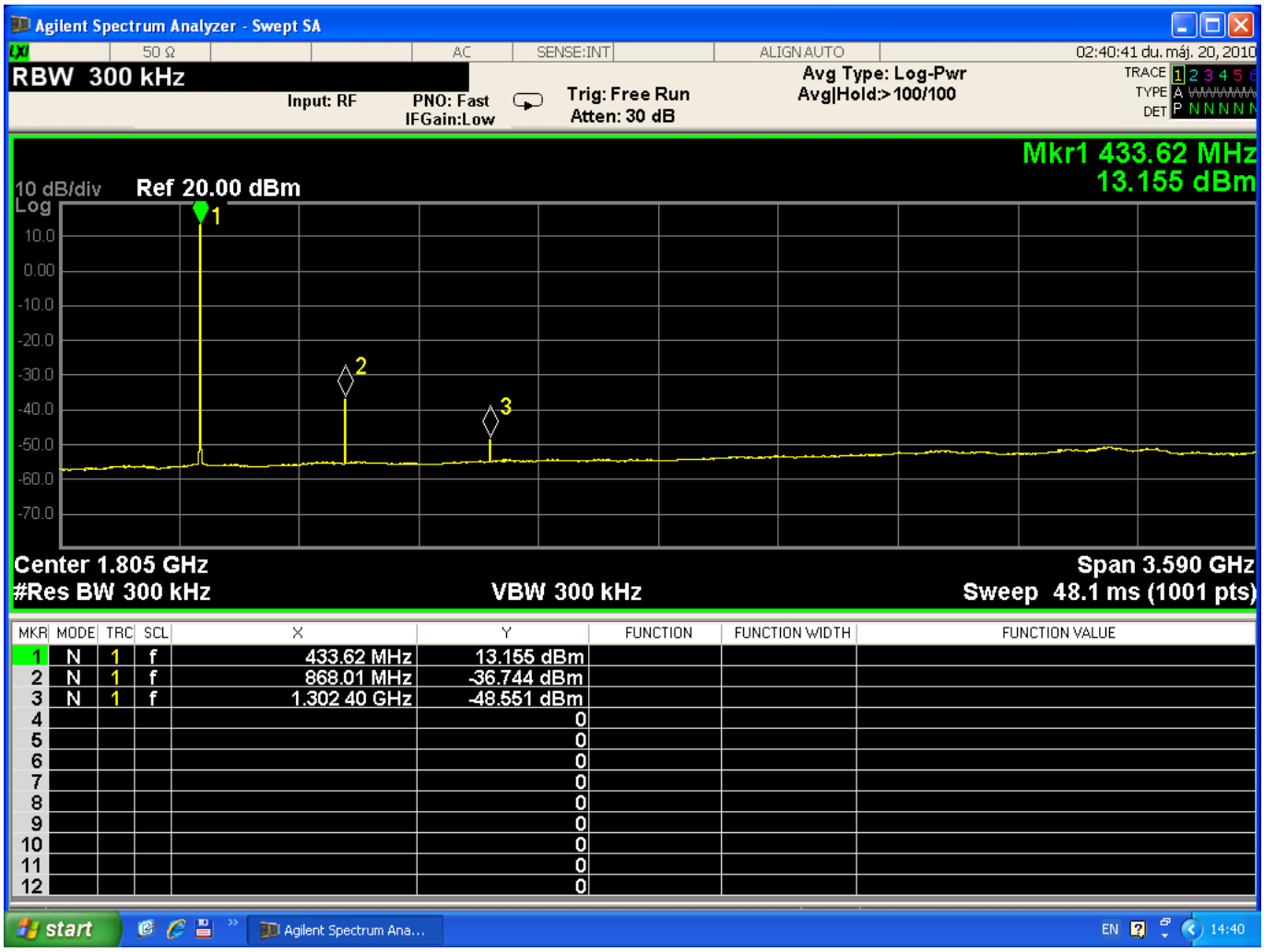

Figure 37. Direct Tie Board at 434 MHz with Wire-Wound Inductors

4.3.3. 868 MHz, V_{DD} = 3.3 V, txpow[2:0]=3'b111

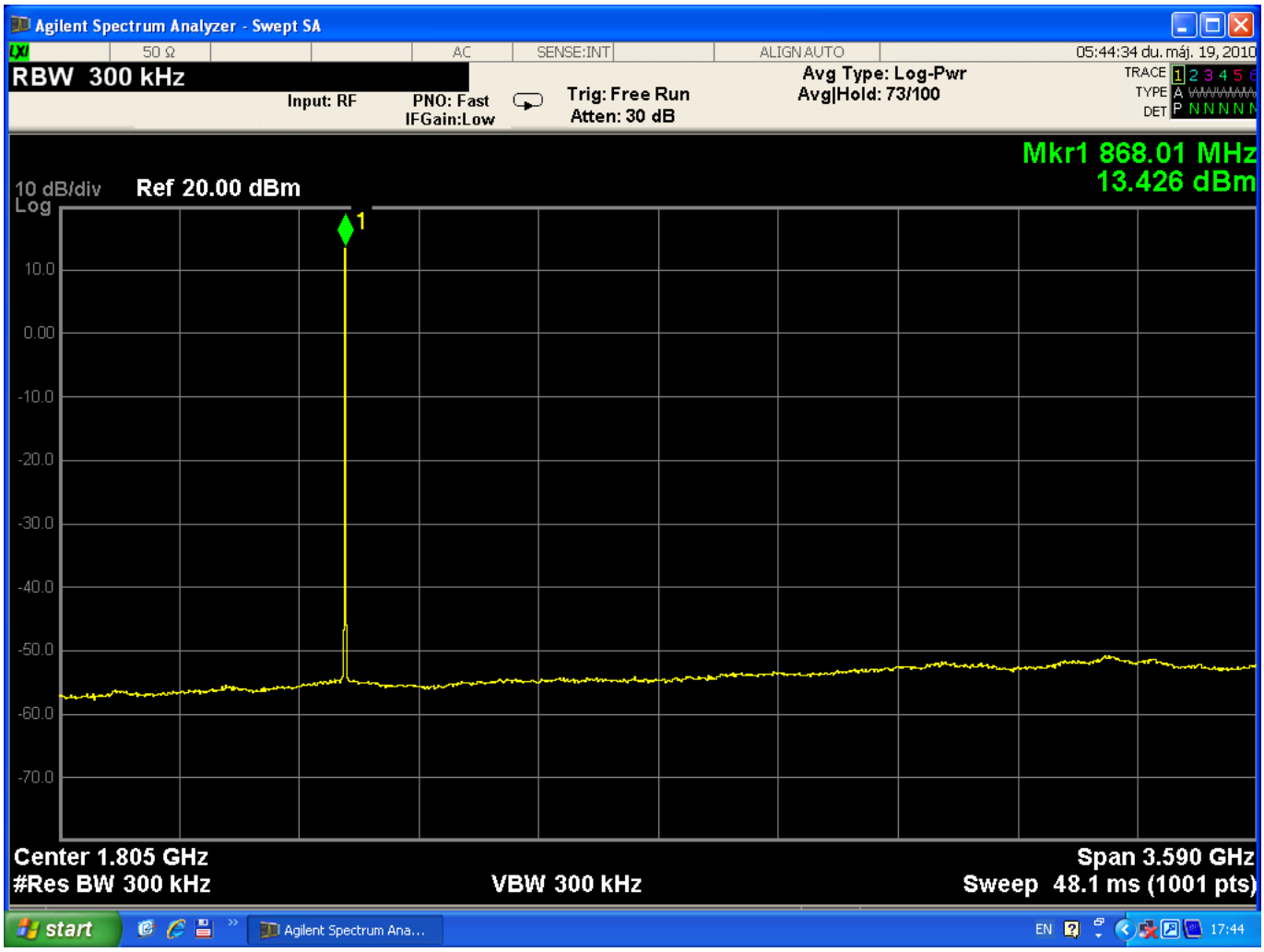

Figure 38. Direct Tie Board at 868 MHz with Wire-Wound Inductors

4.3.4. 915 MHz, VDD=3.3V, txpow[2:0]=3'b111

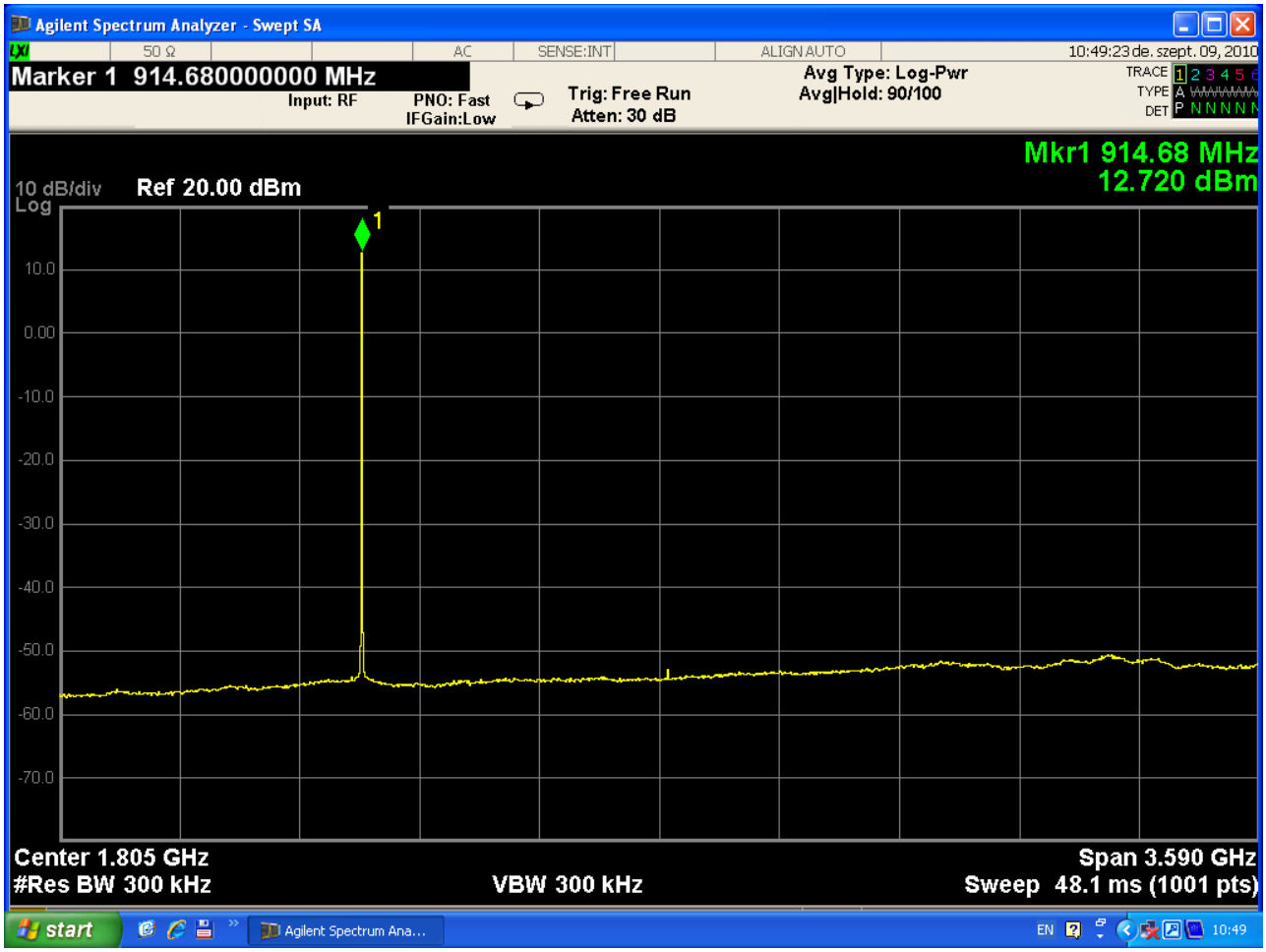

Figure 39. Direct Tie Board at 915 MHz with Wire-Wound Inductors

4.3.5. 950 MHz, V_{DD} = 3.3 V, txpow[2:0]=3'b110

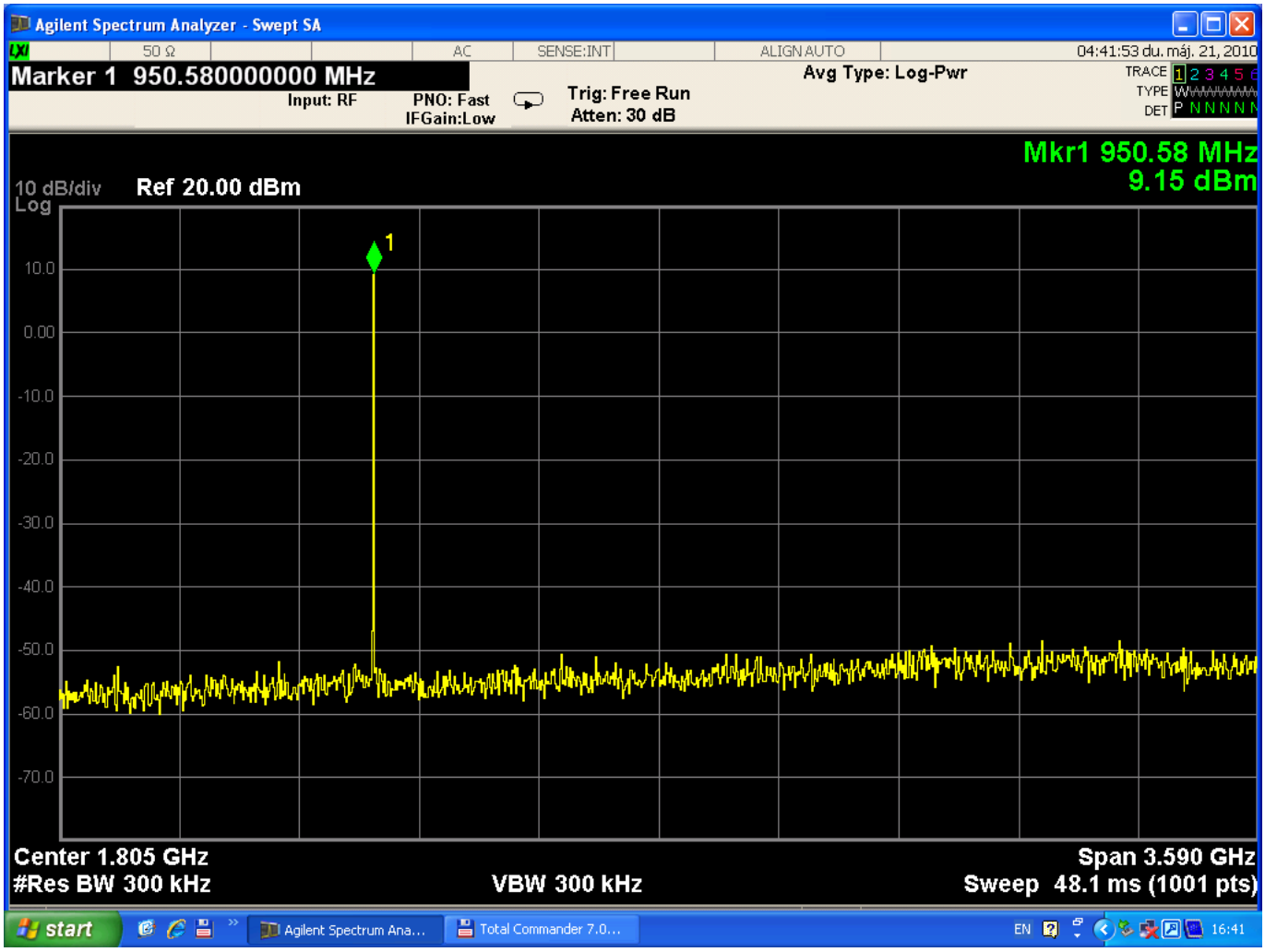

Figure 40. Direct Tie Board at 950 MHz with Wire-Wound Inductors

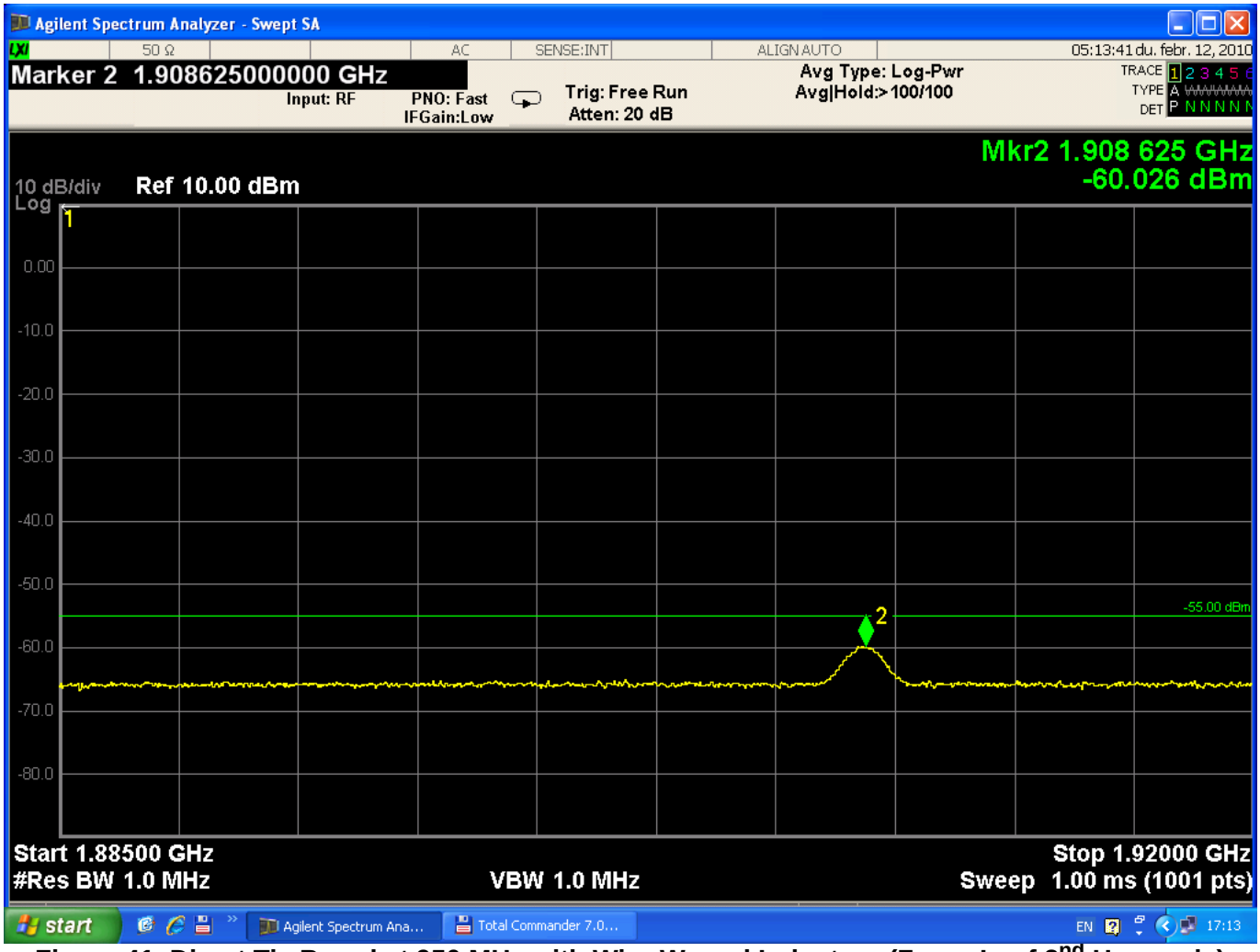

Figure 41. Direct Tie Board at 950 MHz with Wire-Wound Inductors (Zoom-In of 2nd Harmonic)

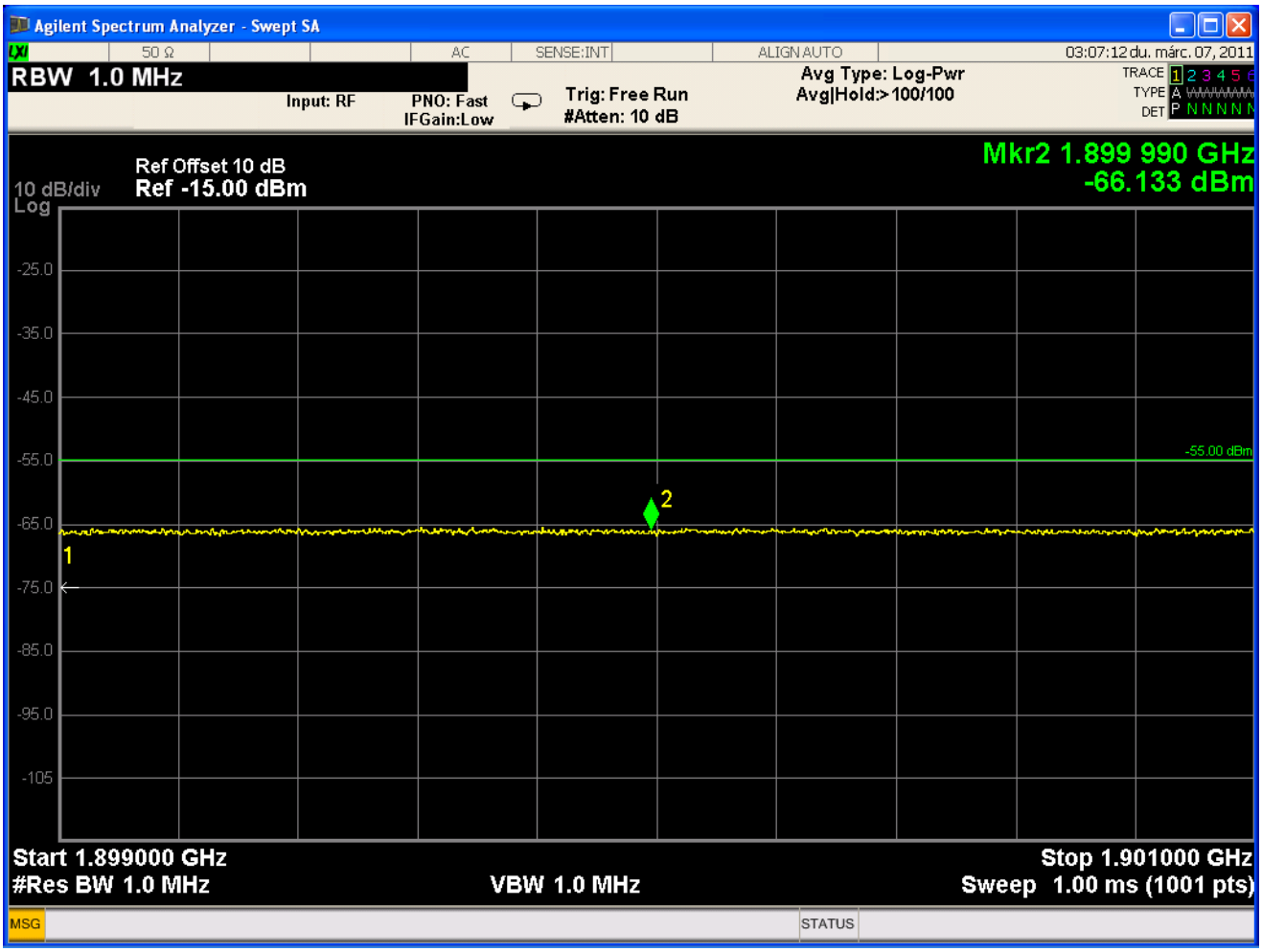

Figure 42. . Same as Figure 41, but with external 10 dB Attenuator and HPF at Board Output; the 10 dB External Attenuator is Compensated by 10 dB Amplitude Offset

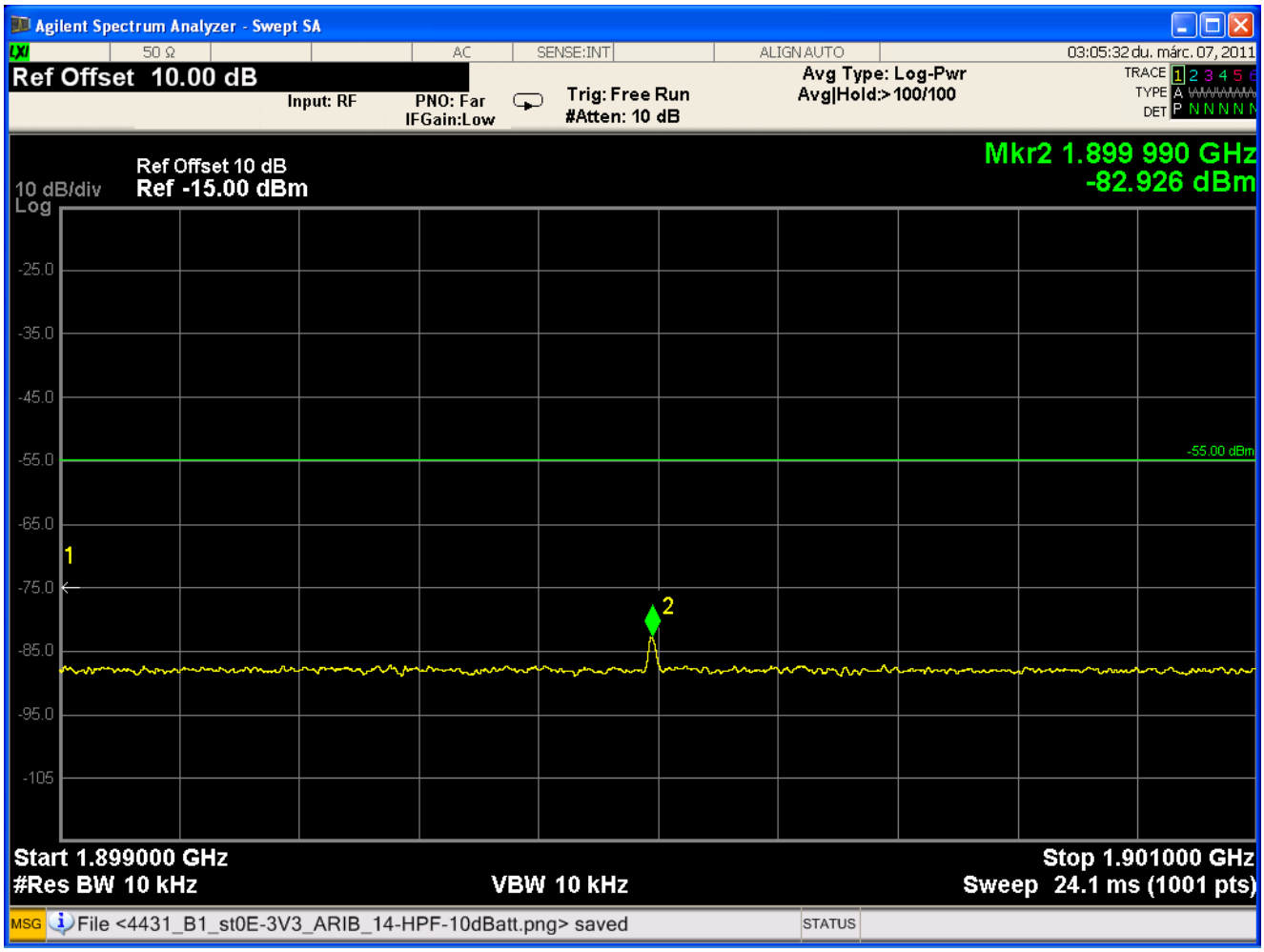

Figure 43. Same as Figure 42, but with 30 kHz RBW

4.4. Direct Tie Board Configurations with Multilayer Inductors

4.4.1. 315 MHz, V_{DD} = 3.3 V, txpow[2:0]=3'b111

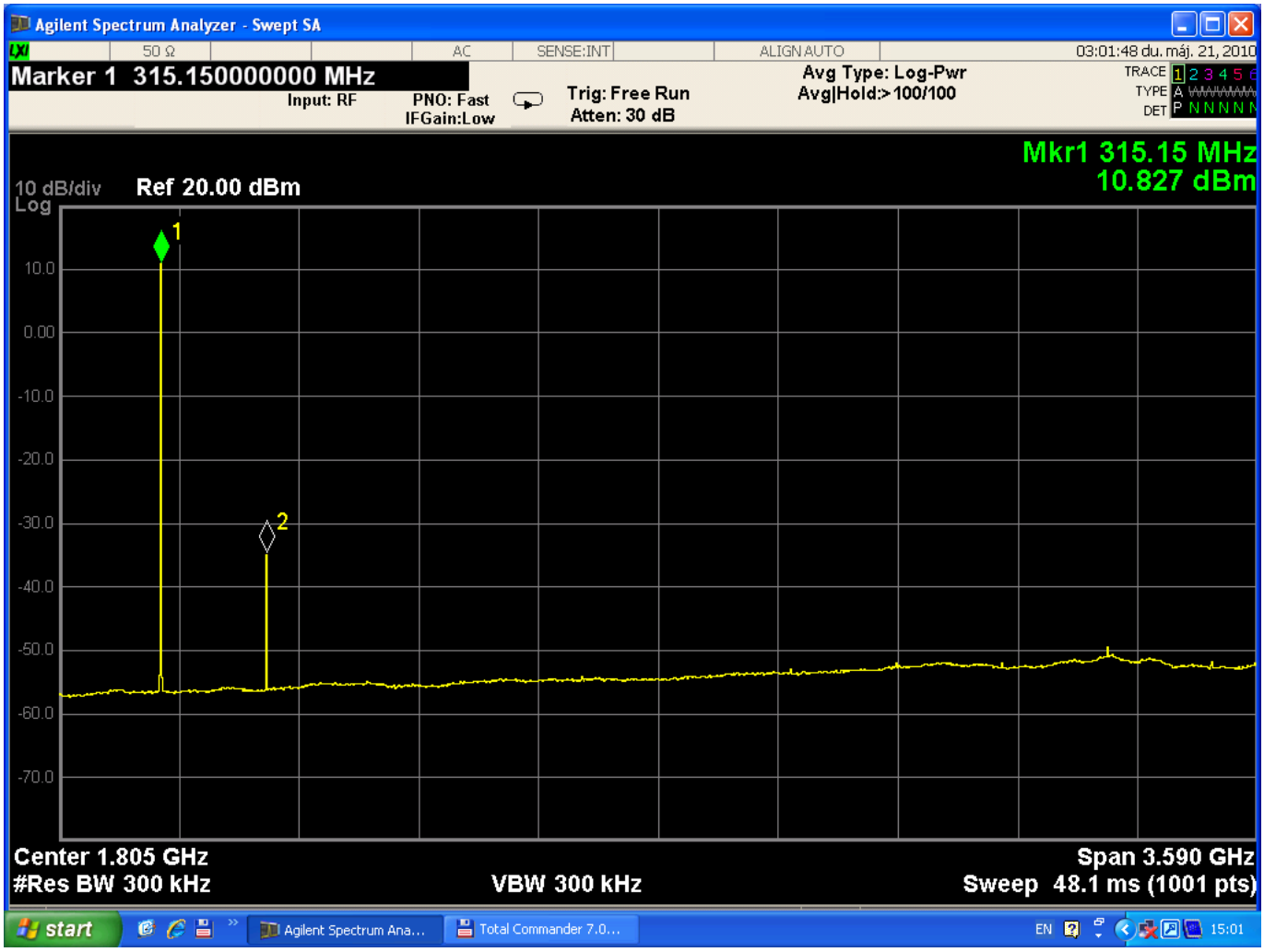

Figure 44. Direct Tie Board at 315 MHz with Multilayer Inductors

4.4.2. 434 MHz, VDD=3.3V, txpow[2:0]=3'b111

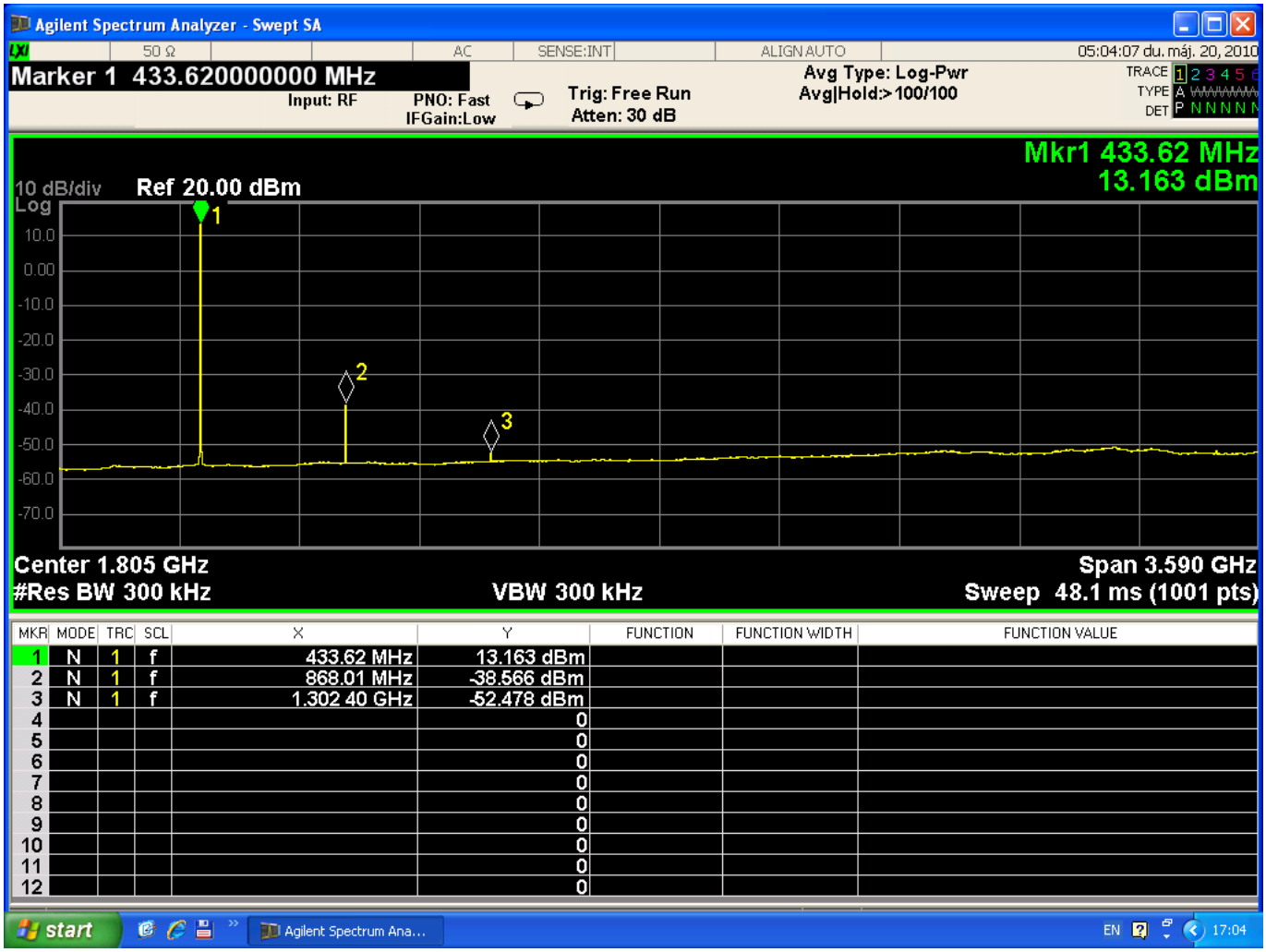

Figure 45. Direct Tie Board at 434 MHz with Multilayer Inductors

4.4.3. 868 MHz, VDD=3.3V, txpow[2:0]=3'b111

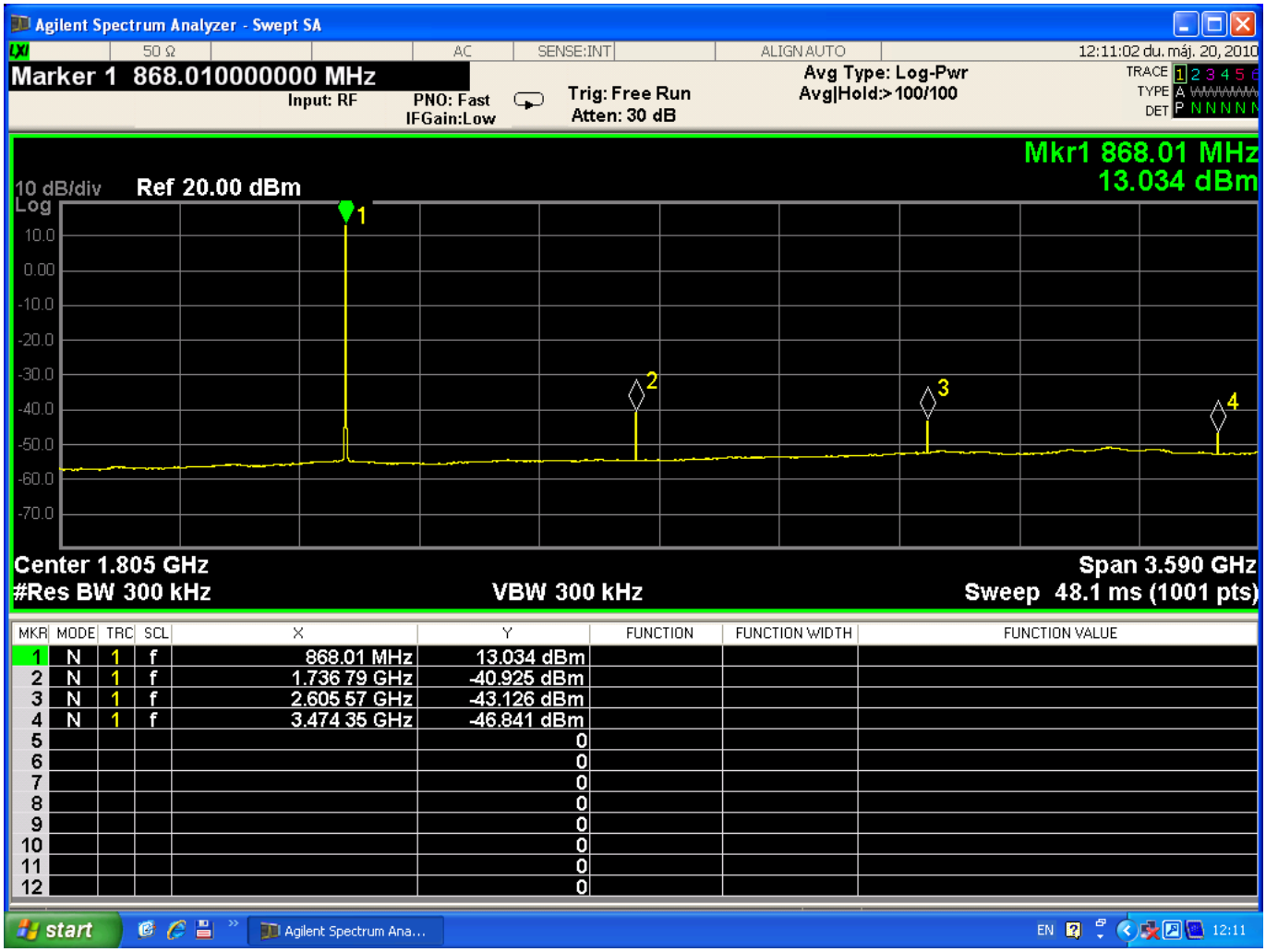

Figure 46. Direct Tie Board at 868 MHz with Multilayer Inductors

4.4.4. 915 MHz, VDD=3.3V, txpow[2:0]=3'b111

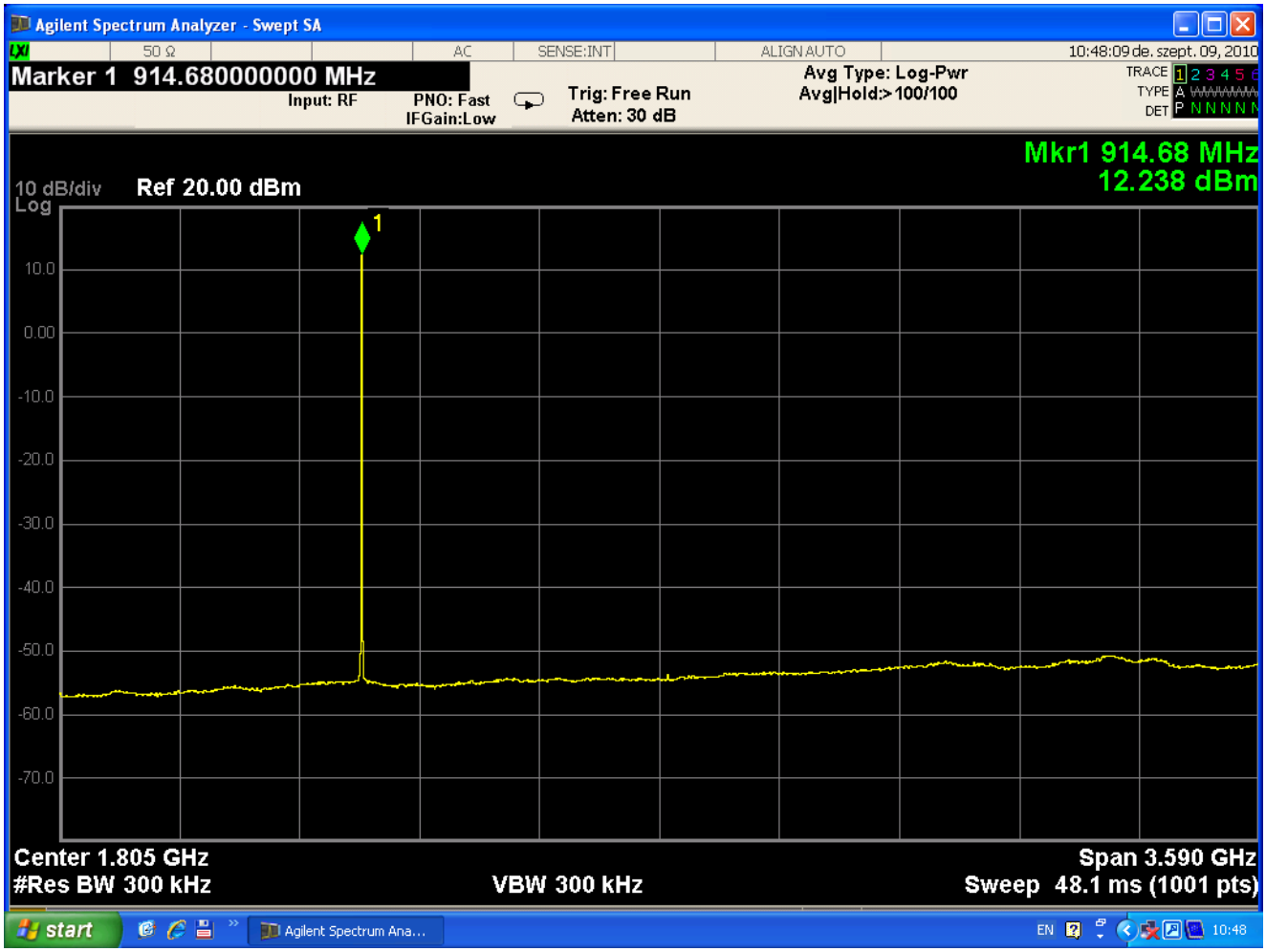

Figure 47. Direct Tie Board at 915 MHz with Multilayer Inductors

4.4.5. 950 MHz, VDD=3.3V, txpow[2:0]=3'b110

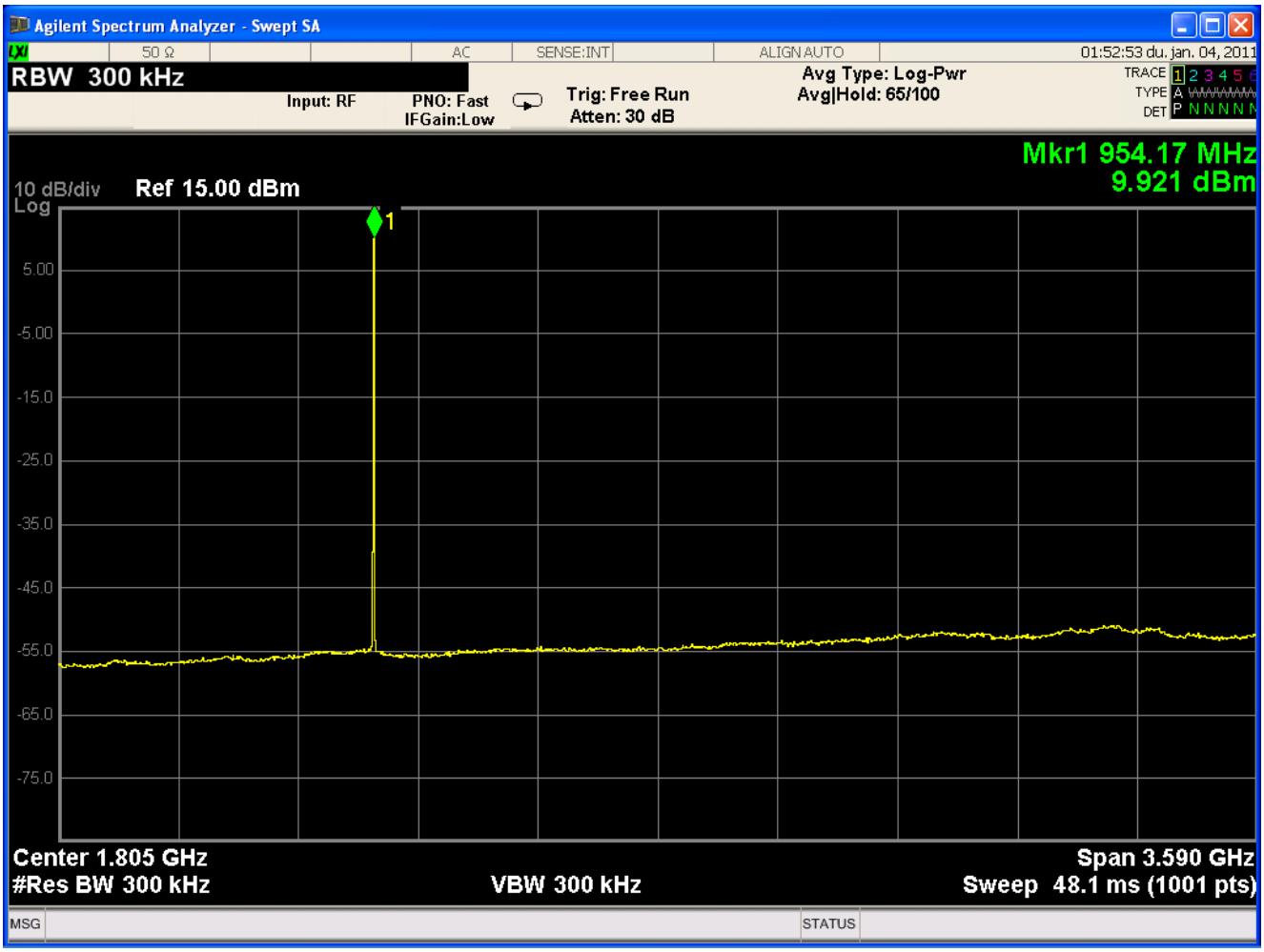

Figure 48. Direct Tie Board at 950 MHz with Multilayer Inductors

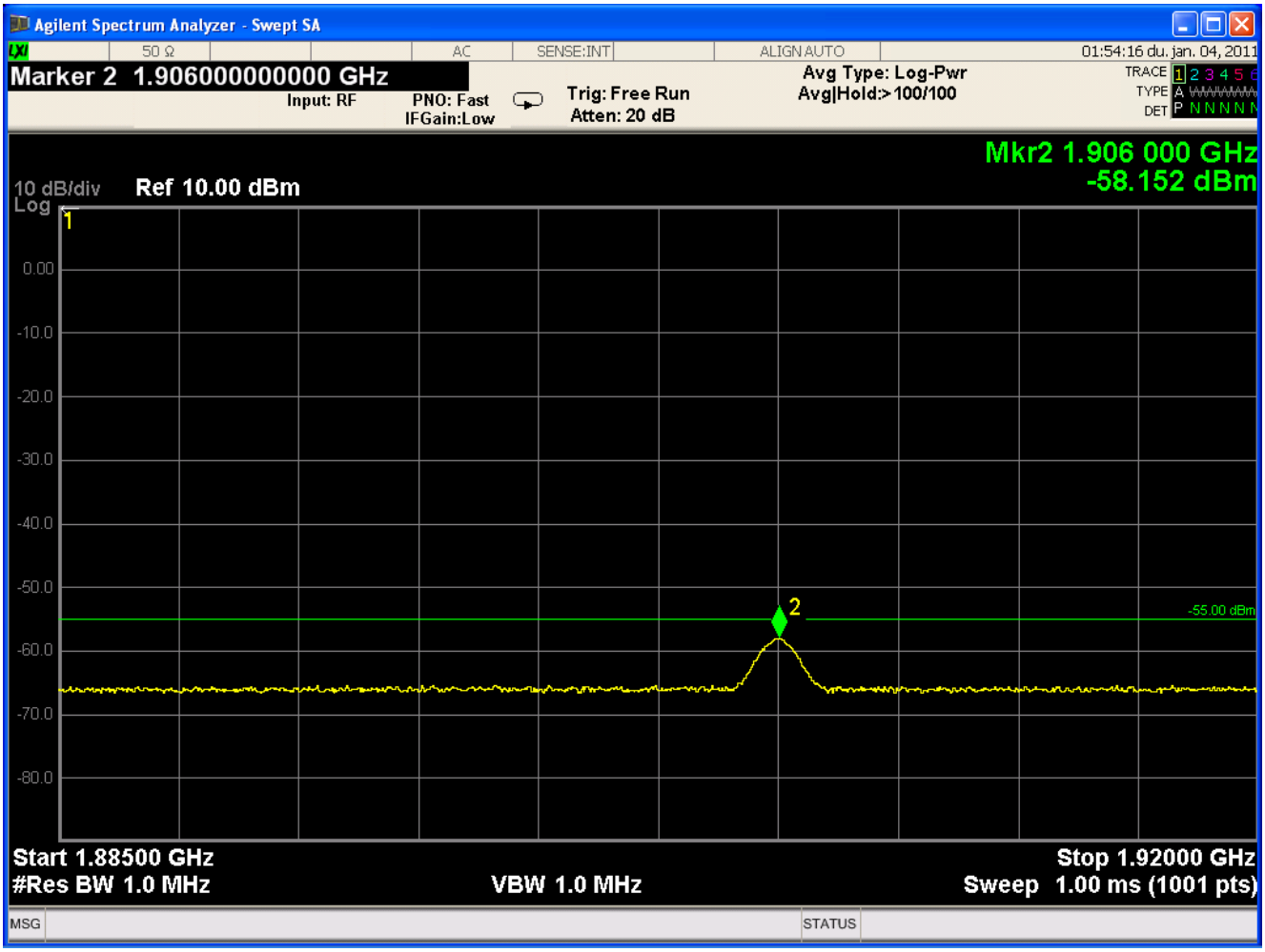

Figure 49. Direct Tie Board at 950 MHz with Multilayer Inductors (Zoom-In of Second Harmonic)

Document Change List

Revision 0.1 to Revision 0.2

- Updated Table 2 on page 3.
- Updated Table 3 on page 4.
- Updated Table 5 on page 5.
- Updated "4. Measured Spectrum Plots" on page 37.
- Added Figure 39 on page 53.
- Added Figure 42 on page 56.
- Added Figure 43 on page 57.
- Added Figure 47 on page 61.
- Added Figure 48 on page 62.
- Added Figure 49 on page 63.

NOTES:

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