PORTING CODE FOR C8051F326/7 DEVICES TO C8051T326/7 DEVICES

1. Introduction

When porting code from C8051F326/7 Flash devices to C8051T326/7 EPROM devices, there are a few key differences that must be taken into account. In many cases, the same firmware will run on either device family. The common special function registers (SFRs) are in the same locations, and any additional features on the EPROM device default to the Flash device's behavior. However, there are some parts of the design that may need to be changed. This document and "AN368: Differences between the C8051F34A and the C8051T62x and C8051T32x Device Families" contain information on specific portions of firmware that must be changed, cannot be ported, or can be added to utilize enhanced features found in the C8051T62x and C8051T32x device families. Some SFRs on the 'T326/7 EPROM devices have additional functional bits that are not present on the 'F326/7 Flash devices. It is important to ensure that writes to SFRs with additional function bits do not accidentally modify any of the additional bits in the 'T326/7 EPROM devices' SFRs. Refer to AN368 for a list of registers with additional function bits.

2. Recommended Porting Process

1. Modify the device-specific header file to match the target device.
2. Make changes in code that must be made to account for differences.
3. Remove sections of code that cannot be ported.
4. Add code for any enhanced features that are required.
5. Test and debug.

3. Required Code Changes

3.1. Device-Specific Header File

The device-specific header file included in the firmware must be changed. Instead of including the 'F326/7 Flash device header file, C8051F326_defs.h, include the 'T326/7 EPROM device header file, C8051T622_defs.h.

3.2. Writing to Code Space through Firmware

In-Application Programming (IAP) is performed differently on the C8051F326/7 Flash devices and the C8051T326/7 EPROM devices. For the EPROM devices, IAP has to be enabled through the in-application programming control (IAPCN) SFR before code space can be modified. The Flash Lock and Key (FLKEY) and Flash Scale (FLSCL) SFRs are not found on the EPROM devices and must be removed from code. Instead, the SFR called EPROM Memory Lock and Key (MEMKEY) is used. Detailed instructions on the recommended programming sequence can be found in the Program Memory (EPROM) section of the device data sheet.

In order to use the IAP feature on the EPROM devices, a capacitor must be connected between the VPP pin (P1.1) and ground. Additionally, the pin must be configured in Open-Drain mode in the P1MDOUT SFR before attempting to perform the write to code space.

3.3. Watchdog Timer

By default, the watchdog timer is enabled on the 'T326/7 EPROM devices. The 'F326/7 Flash devices do not have a watchdog timer. In the porting process, disable the watchdog timer to prevent it from resetting the microcontroller. The watchdog timer can be disabled by clearing bit 6 in the PCA mode SFR (PCA0MD).

3.4. Voltage Regulator Control Register

The 'F326/7 Flash devices have one voltage regulator that regulates from 5 V to 3.3 V. The 'T326/7 EPROM devices have two voltage regulators, one for 5 V to 3.45 V (REG0) and one for VDD to the core voltage of 1.8 V (REG1). To reflect this difference, the REG0CN register on the 'F326/7 Flash devices has been renamed REG01CN on the 'T326/7 EPROM devices. When porting code from 'F326/7 Flash devices to 'T326/7 EPROM devices, any accesses of REG0CN should be renamed to REG01CN. The VBPOL bit (bit 5 of REG0CN) on the 'F326/7 Flash device is not found on the 'T326/7 EPROM device. Refer to the Voltage Regulator section of the data sheet for more information regarding this bit. It is important to note that the REG01CN SFR on the EPROM devices has functional bits not found in the REG0CN SFR on the Flash devices. Ensure that writes to the REG01CN SFR are not accidentally modifying the additional functional bits.

3.5. Lock Byte Position

The Lock Byte on the 'T326/7 EPROM devices exists at a different location and has a slightly different configuration than the Lock Byte on the 'F326/7 Flash devices. On the Flash device, the Lock Byte is located at 0x3DFF and can be configured to lock memory on a 512-byte Flash page basis. On the EPROM device, the Lock Byte is at 0x3FF8 and can only be configured to allow or prevent all of the code space from being read or written to over the C2 interface.

3.6. Port Pins

The 'T326/7 EPROM devices and the ‘F326/7 Flash devices have the same number of GPIO pins. Seven of these GPIO are mapped to different hardware addresses, but located at the same pin location of the microcontroller. If any of the ‘F326/7 Flash device GPIO pins listed in Table 1 are used in firmware being ported to a ‘T326/7 EPROM device, the firmware should be modified to instead use the GPIO on the ‘T326/7 EPROM device that is located at the same pin location.

Table 1. GPIO Differences Between ‘F326/7 Flash Devices and ‘T326/7 EPROM Devices

Pin Number	‘F326/7 Flash GPIO	‘T326/7 EPROM GPIO
10	P3.0/C2D	P2.0/C2D
11	P2.3	P1.5
12	P2.2	P1.4
16	P2.5	P1.3
17	P2.4	P1.2
18	P2.1	P1.1/VPP
19	P2.0	P1.0

The Global Port Control SFR (GPIOCN) does not exist on 'T326/7 EPROM devices. Instead, the SFR's Port I/O Crossbar Registers (XBR0 and XBR1) should be used to achieve the same configuration.

The crossbar on 'T326/7 EPROM devices allows peripherals to be located at various port pins. The 'F326/7 Flash devices do not have a crossbar, and peripherals are located at fixed port pins. Peripherals are enabled through the Port I/O Crossbar Registers (XBRn) on the 'T326/7 EPROM devices.

3.7. UART Interface

If UART0 is used on the 'F326/7 Flash device, UART1 should be used on the 'T326/7 EPROM device. On the EPROM device, the USB clock cannot be used as the UART baud rate generator clock source. Only the system clock can be used. This setting is found in bit 7 of SBCON0 on the Flash device. The following is a list of SFRs that need to have the variable x changed from 0 to 1: SCONx, SMODx, SBUFx, SBCONx, SBRLHx, and SBRLLx. UART1 must be enabled through the XBR2 SFR.

3.8. Universal Serial Bus (USB)

If the USB peripheral is used in the code being ported, note that on the 'F326/7 Flash device, endpoint 1 (EP1) is 192 bytes, whereas on the 'T326/7 EPROM device, EP1 is 128 bytes.

4. Code that Cannot be Ported

4.1. Erasing Code Space

Pages of Flash memory on the 'F326/7 Flash devices can be erased through firmware, but code space on the 'T326/7 EPROM devices cannot be cleared. Each bit in code space can be modified once. Firmware that erases code space cannot be ported to the EPROM devices.

4.2. External Oscillator and the Clock Multiplier

The 'T326/7 EPROM devices have a Clock Multiplier module that is unable to accept an external clock as an input. If an application being ported to the 'T326/7 EPROM device from the 'F326/7 Flash device is multiplying an external clock using the Clock Multiplier, a faster external clock (which does not need to be multiplied) should be used with the 'T326/7 EPROM device.

5. Hardware Changes

In addition to necessary firmware changes, some hardware modifications may be needed to successfully port a design to a ‘T326/7 EPROM device. Here are specific examples of changes that may need to be made during the porting process.

5.1. In-Application-Programming (IAP) Feature

If the application designed for the ‘F326/7 Flash based microcontroller contains firmware that writes to code space, the firmware will need to be modified, and an external 4.7 µF capacitor will need to be added between the VPP pin (P1.1) and ground. Without this capacitor connected between the VPP pin and ground, the IAP feature will not function correctly.

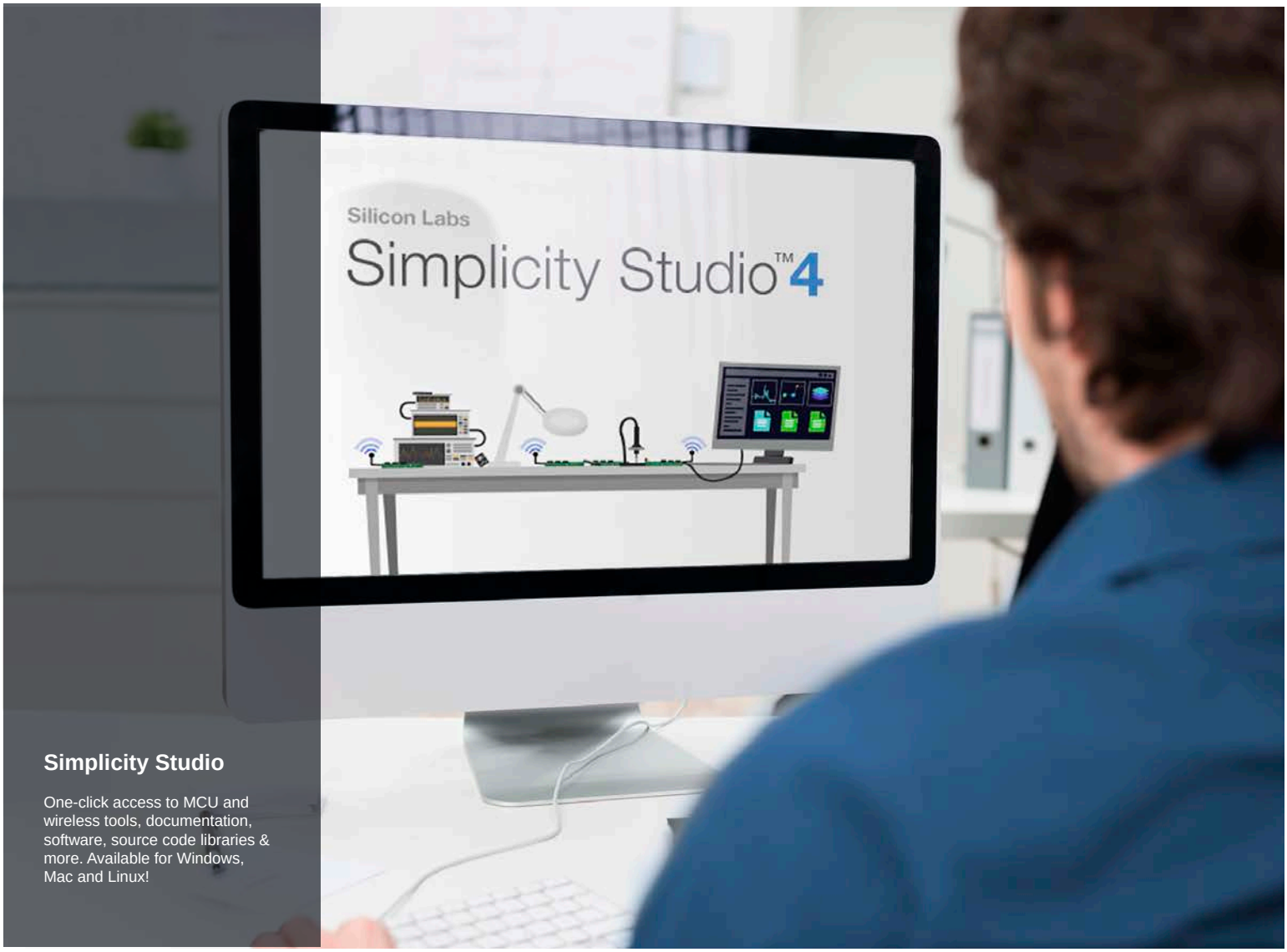
5.2. External Clock Multiplier

If an application being ported to the 'T326/7 EPROM device from the 'F326/7 Flash device is multiplying an external clock using the Clock Multiplier, a faster external clock (which does not need to be multiplied) should be used with the 'T326/7 EPROM device. This will require a different external oscillator to be used in the ported design and may require a change in the external oscillator circuit, depending on the external clock selected for the design.

Document Change List

Revision 0.1 to Revision 0.2

- Updated WDT enable bit position in "3.3. Watchdog Timer" on page 1.
- Updated REG0 output voltage in "3.4. Voltage Regulator Control Register" on page 2.



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