AN486: High-Side Bootstrap Design Using ISODrivers in Power Delivery Systems

Silicon Labs ISOdrivers are isolated gate drivers that combine low latency, high-drive-strength gate drive circuits with on-chip isolation.

For robust and safe operation, designers of ac-dc and isolated dc-dc switch mode power supplies (SMPS), uninterruptible power supplies (UPS), solar inverters, and electronic lighting ballasts must rely not only on a properly selected high side/low-side gate driver IC, but also on an external bootstrap circuit and its PCB layout.

The ISOdriver high-side drive channel(s) require(s) a bootstrap circuit when the high-side switch has a drain voltage greater than the ISOdriver's VDDA supply.

The bootstrap capacitor, C_B (shown in Figure 1), charges when the low-side driver is active, then supplies driver bias to the high side driver when active. At first glance, the bootstrap appears as a simple, low-cost circuit consisting only of diode D1 and capacitor C_B (and sometimes resistor R_B). But beneath this humble facade lurks potential design challenges. This application note discusses the operation and design of the high side bootstrap circuit and presents a methodology for bootstrap design.

KEY POINTS

- Bootstrap tutorial
- Step-by-step ISOdriver bootstrap design guide and example
- Summary of best layout practices for ISOdriver with bootstrap circuitry
- Bootstrap calculator available

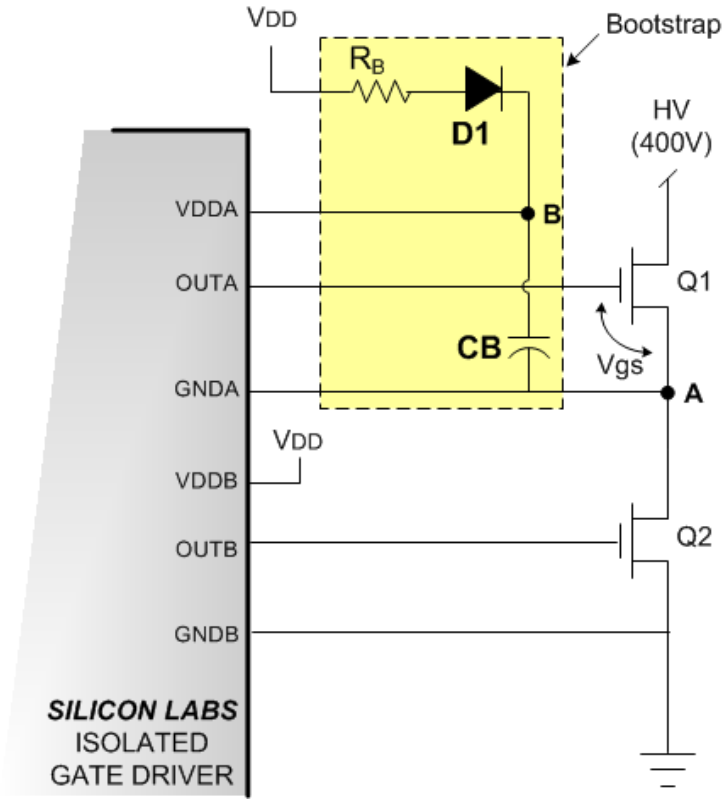


Figure .1. ISODriver with High-Side Bootstrap Circuit

1. Bootstrap Operation

Bootstrap operation (shown below) is straightforward: C_B is charged during low-side drive where Q2 is on and Q1 is off. During this period, charge current flows from VDD into both the ISOdriver VDDA input and through the charge loop from bootstrap resistor R_B through diode D1, C_B, and Q2 to ground. At the end of the low-side drive period, Q2 is turned off and Q1 turned on causing the voltage at Q1's source to quickly rise toward its drain voltage. This action reverse biases bootstrap diode D1 disconnecting the ground-based VDD supply from C_B.

Since the low side of C_B is referenced to the MOSFET source (GNDA), a high-side bias voltage of VDD–0.7 V is maintained between the Q1 source and gate via the OUTA pin. From this point until the end of the high-side drive period, C_B supplies all of the current required to maintain high-side driver operation.

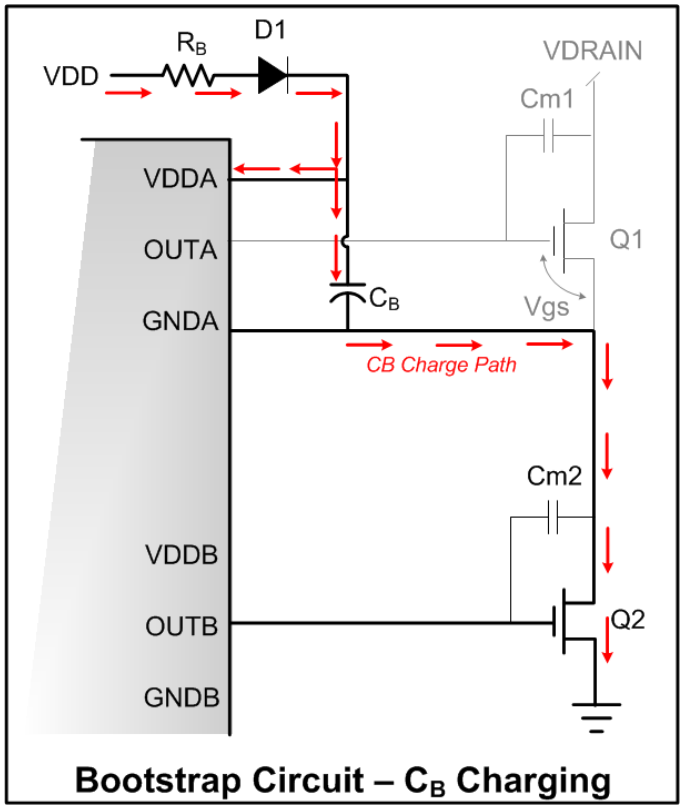


Figure 1.1. Bootstrap Circuit—C_B Charging

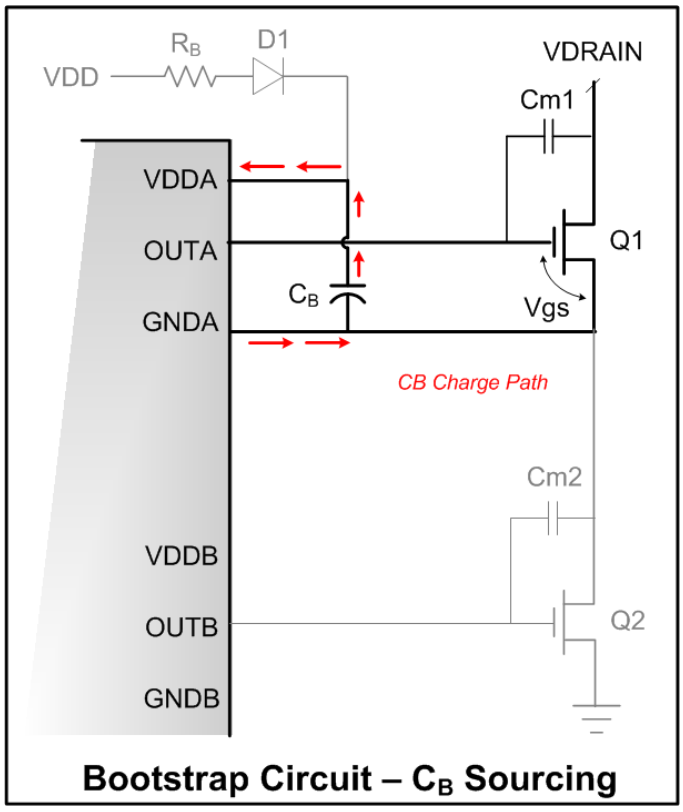


Figure 1.2. Bootstrap Circuit—C_B Sourcing

The following figure shows typical C_B ripple. The end of the C_B charge cycle is closely followed by a high negative dV/dt as C_B sources gate charge to Q1. After Q_G is transferred, the voltage on C_B falls as current is sourced to the VDDA input to maintain OUTA in its high state. Note that the difference between the actual and maximum attainable value of V_{CB} is due to the drop across R_B and D1, and that C_B ripple amplitude is a function of the values of Q_G, VDD current and C_B. Also, R_B is typically used in low-frequency systems to limit peak current and is seldom used in systems running above 100 kHz.

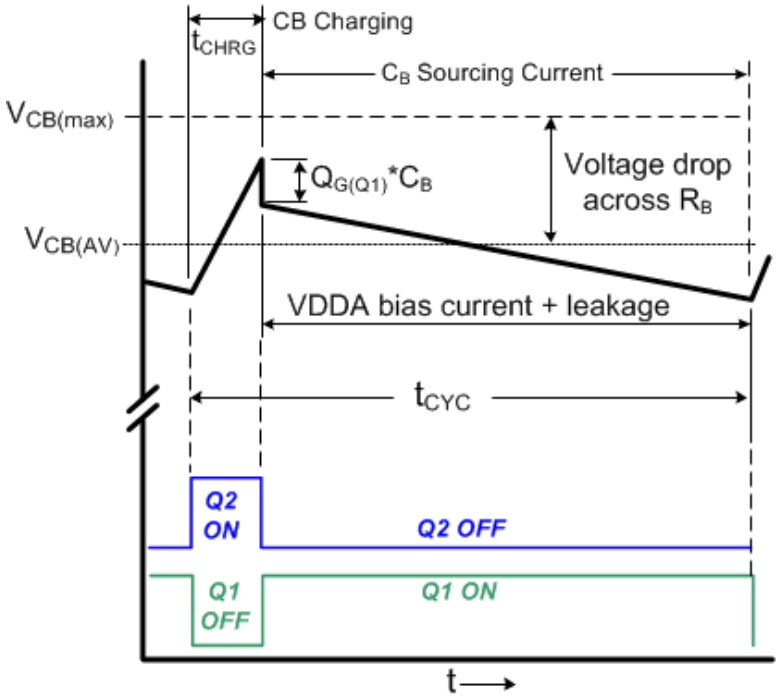


Figure 1.3. Typical C_B Ripple Cycle

1.1 Bootstrap Design

While it is a simple circuit, the bootstrap can be problematic if not designed correctly. In particular, care must be taken to ensure low C_B ripple to avoid triggering the driver's undervoltage lockout, which can halt converter operation; additionally, the refresh period must be sufficient to fully charge C_B. The inherent limitation of the high-side bootstrap circuit is the time required to sufficiently refresh C_B. Some power topologies may have an excessively high duty cycle or frequency to support refresh, or they may have a high-side circuit that causes the load to be in series with the charge path. For those applications, a charge pump (instead of a high-side bootstrap) may be required.

A typical bootstrap design flow first determines the total charge that CB must deliver during the high-side drive cycle (Q_{CB}). With Q_{CB} known, the value of C_B is calculated based on allowable ripple amplitude and verified adequate refresh under worst-case timing conditions. The figure below shows the equivalent circuit for the bootstrap circuit where the bootstrap diode, D1, is modeled as an ideal switch having a threshold voltage of V_T. Moreover, the high-side driver has a current source that represents the ISOdriver's VDDA input current requirements. Other leakage currents, such as diode reverse leakage and transistor gate leakage, are not considered as they are insignificant compared to the VDDA bias current. Note in the figure below that D is defined as the duty cycle at the high-side (active) switch and not the low-side (passive) switch.

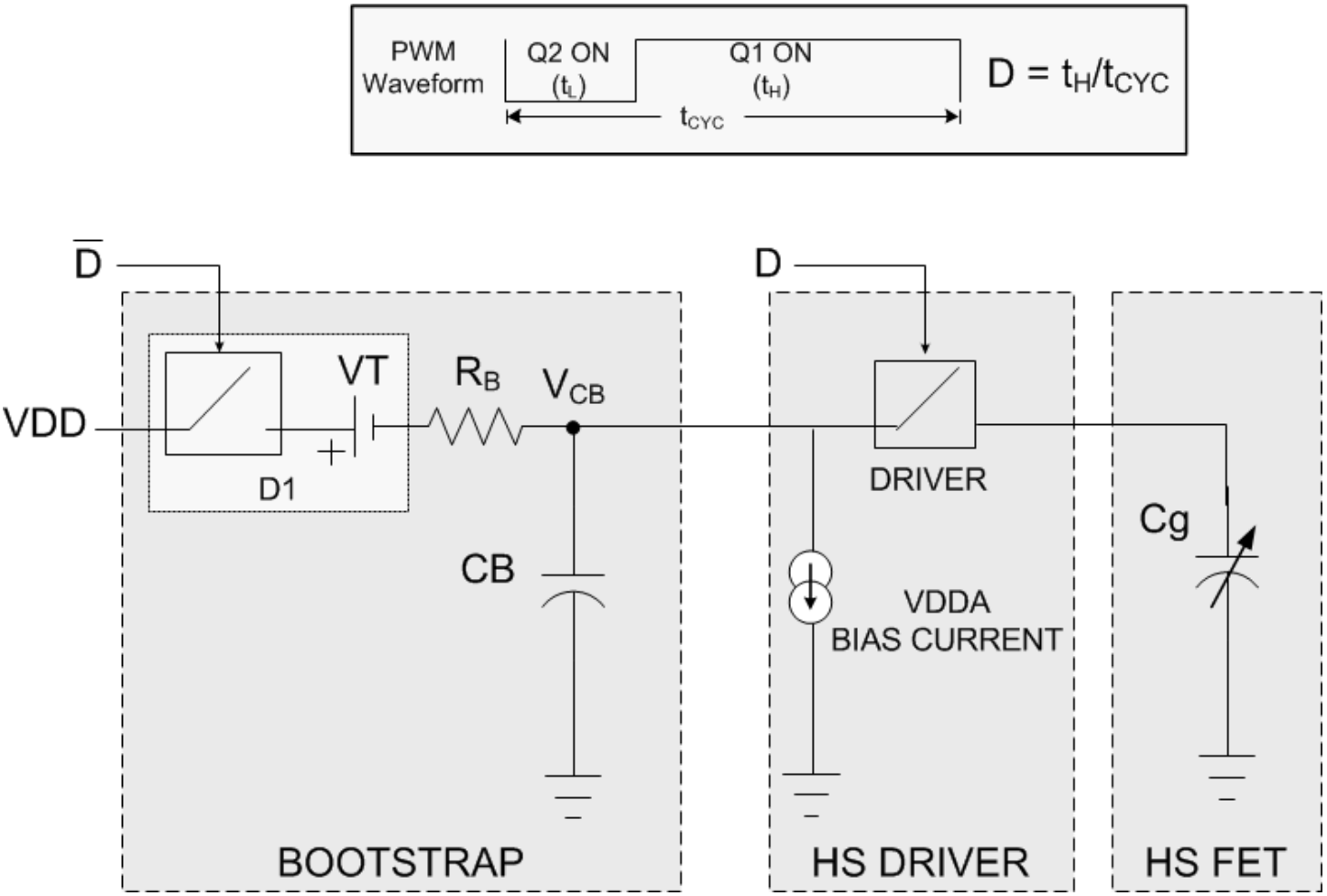


Figure 1.4. Bootstrap Equivalent Circuit

1.2 Design Example

- High-side MOSFET Q_G = 85 nC, V_{GS} = 10 V, t_R = 35 ns
- Diode D1 V_F = 0.7 V
- V_{DDA} input = 12 V at 3 mA (high-side VDD input of ISOdriver)
- F_{PWM} = 200 kHz, D = 10% to 90%
- ISOdriver UVLO threshold = 9.0 V (falling)

The design begins with the calculation of the total charge (QCB) that must be delivered by CB at maximum duty cycle. There are two primary components of this charge: VDDA supply bias current IB and Q1 gate charge QG. Other sources of leakage, such as Q1 gate and D1 leakage, are negligible in comparison and are assumed to be zero.

Q_{CB} is calculated using Equation 1 (t_{CYC} is the period shown in Figure 1.4 Bootstrap Equivalent Circuit on page 3) and substituting values from the list of givens above:

$$Q_{CB} = Q_G + (D \times t_{CYC} \times I_B)$$
$$= 85 \times 10^{-9} + (0.9 \times 5 \times 10^{-6} \times 3 \times 10^{-3})$$
$$= 98.5 \text{ nC}$$

Equation 1.

Per Equation 1, C_B must supply a total of 98.5 nano Coulombs of charge during the high-side drive cycle, and the value of C_B is driven by the maximum allowable ripple (ΔV_{CB}), and calculated using Equation 2. In this design, ΔV_{CB} is chosen to be 5% of VDD.

$$C_B \geq \frac{Q_{CB}}{\Delta V_{CB}}$$
$$\geq \frac{98.5 \times 10^{-9}}{0.05 \times 12}$$
$$\geq 164 \text{ nF; use closest standard value: } 180 \text{ nF}$$

Equation 2.

With a known value for C_B, the value of bootstrap resistor R_B can now be calculated for peak C_B charge using Equation 3 (as previously noted, R_B is typically not used in systems that operate at relatively high frequencies):

$$R_B \leq \frac{(1 - D_{MAX}) \times t_{CYC}}{5 \times C_B}$$
$$\leq \frac{(1 - 0.9) \times 5 \times 10^{-6}}{5 \times 180 \times 10^{-9}}$$
$$\leq 0.556 \text{ m}\Omega \text{ - eliminate } R_B \text{ from design}$$

Equation 3.

In this design, 99 nC of charge must be transferred into C_B within the minimum low-side on time $t_{L(MIN)}$. Equation 4 calculates the current required to meet this criterion:

$$I_{CHRG} = \frac{Q_{CB}}{t_{L(MIN)}} = \frac{98.5 \times 10^{-9}}{0.5 \times 10^{-6}} = 197\ mA$$

Equation 4.

From Equation 4, a maximum average current of 197 mA is required to fully refresh C_B at maximum duty cycle time. The average current through diode D1 can be calculated using Equation 5:

$$I_{RBAV(MAX)} = \frac{Q_G}{t_{CYC}} + I_B = \frac{85 \times 10^{-9}}{5 \times 10^{-6}} + 3 \times 10^{-3} = 20\ mA$$

Equation 5.

The voltage rating of bootstrap diode D1 must be sufficiently high to stand-off the high-side MOSFET drain voltage and a current rating (IF) greater than or equal to the maximum average current as calculated in Equation 5. It must also have a sufficiently fast reverse recovery time to avoid momentarily sourcing current from the high-voltage drain supply into the lower voltage VDD supply. In addition, the operating temperature of the system may require D1 to have low reverse leakage at high temperature.

2. Layout Considerations

Good layout is important in high-side bootstrap design. C_B should be located as close to the driver IC pins as possible. A tantalum or ceramic capacitor (preferably ceramic) can be used for C_B as they provide low leakage and low ESR. If an electrolytic capacitor is used for C_B, it is recommended that a small, low-ESR decoupling capacitor be added in parallel with the electrolytic, as shown in the following figure.

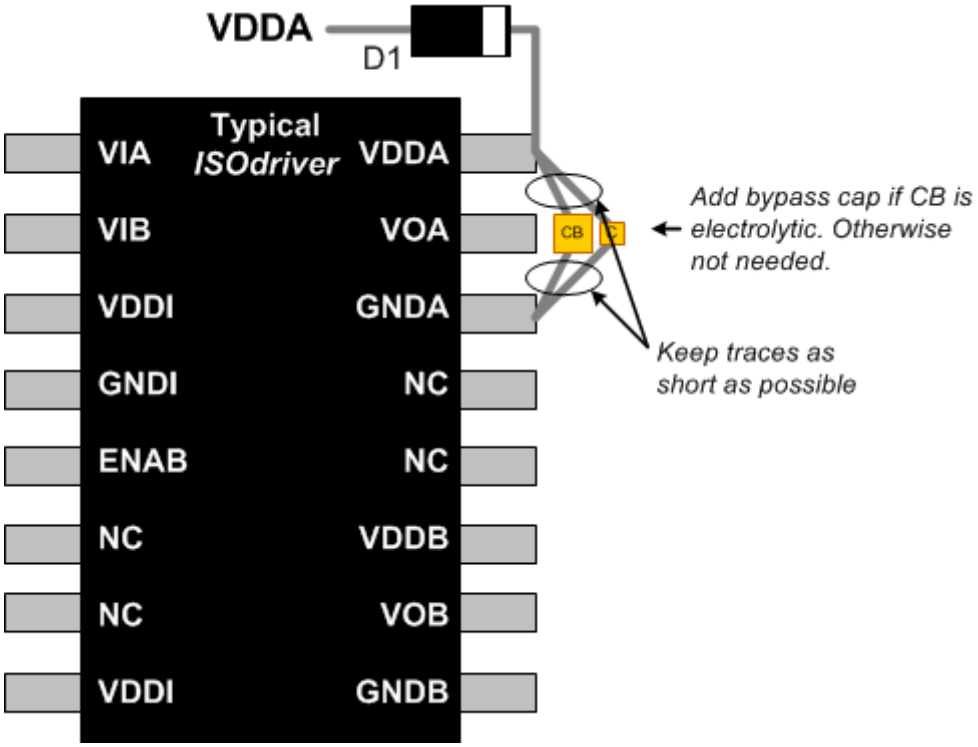


Figure 2.1. Bootstrap Layout Guidelines

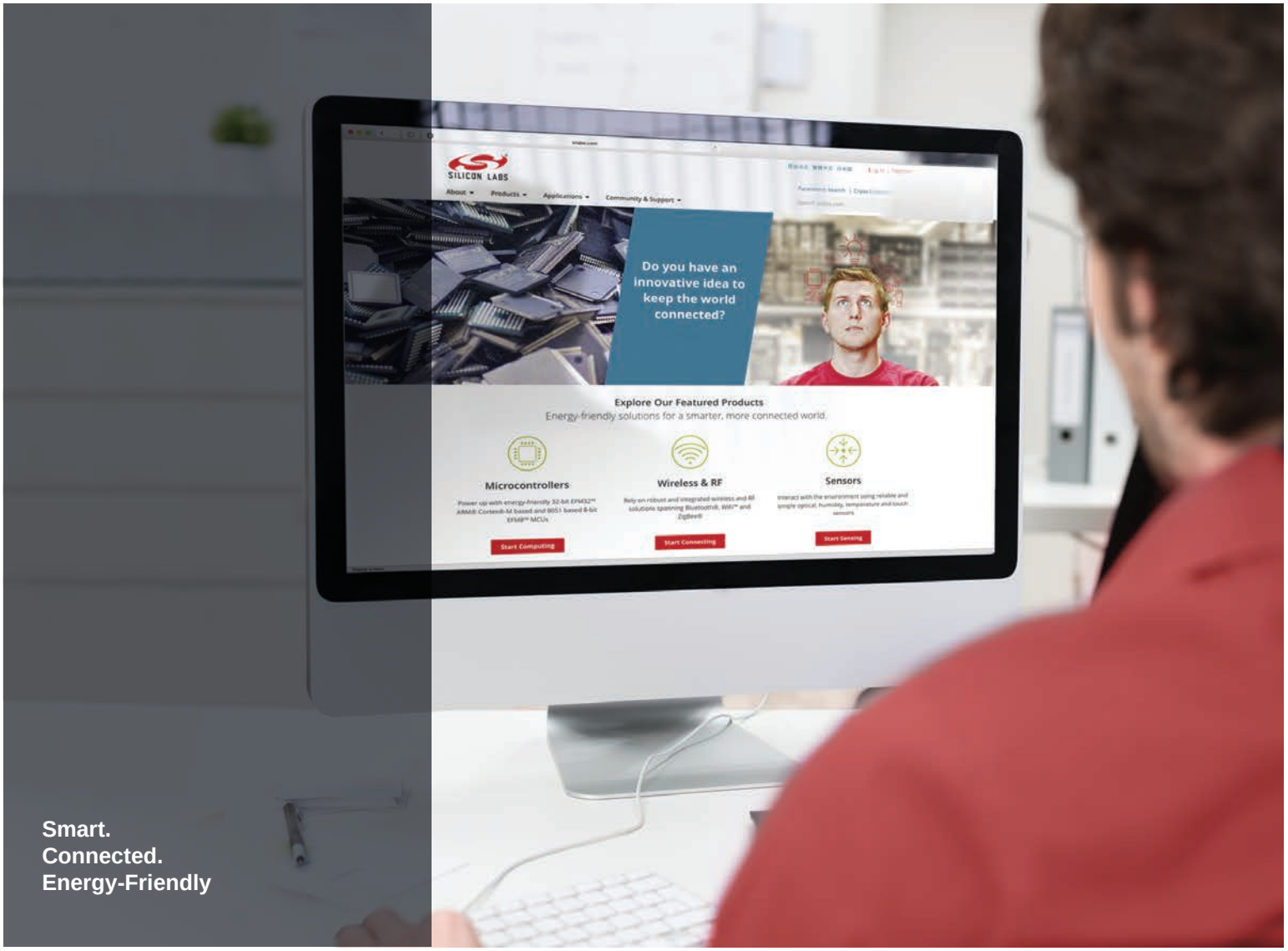
3. Conclusion

Proper attention to bootstrap component selection and PCB layout are critical to ensuring reliable, high-performance isolated gate driver circuits.

4. Document Change List

Revision 0.1 to Revision 0.2:

- Removed references to Si823x throughout.



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