



3. Package Options

Devices in the C8051F91x-90x and C8051F99x-98x families are available in 24-pin QFN or QSOP packages. F99x-98x devices are also available in a 20-pin 3x3 mm QFN package. The devices in the two families are designed to be pin-compatible (24-pin packages only); however, port I/O remapping may be needed in some applications. Figure 2 shows the pinout differences between the 24-pin packages in each family.

The primary pinout difference to note is that P1.6 on the C8051F902 is a no-connect on C8051F996 devices. The device families are pin-for-pin compatible in applications that do not use P1.6. On the C8051F996, P1.6 and P1.7 can be used as GPIO or as oscillator pins. These pins are dedicated to the crystal function the C8051F902.

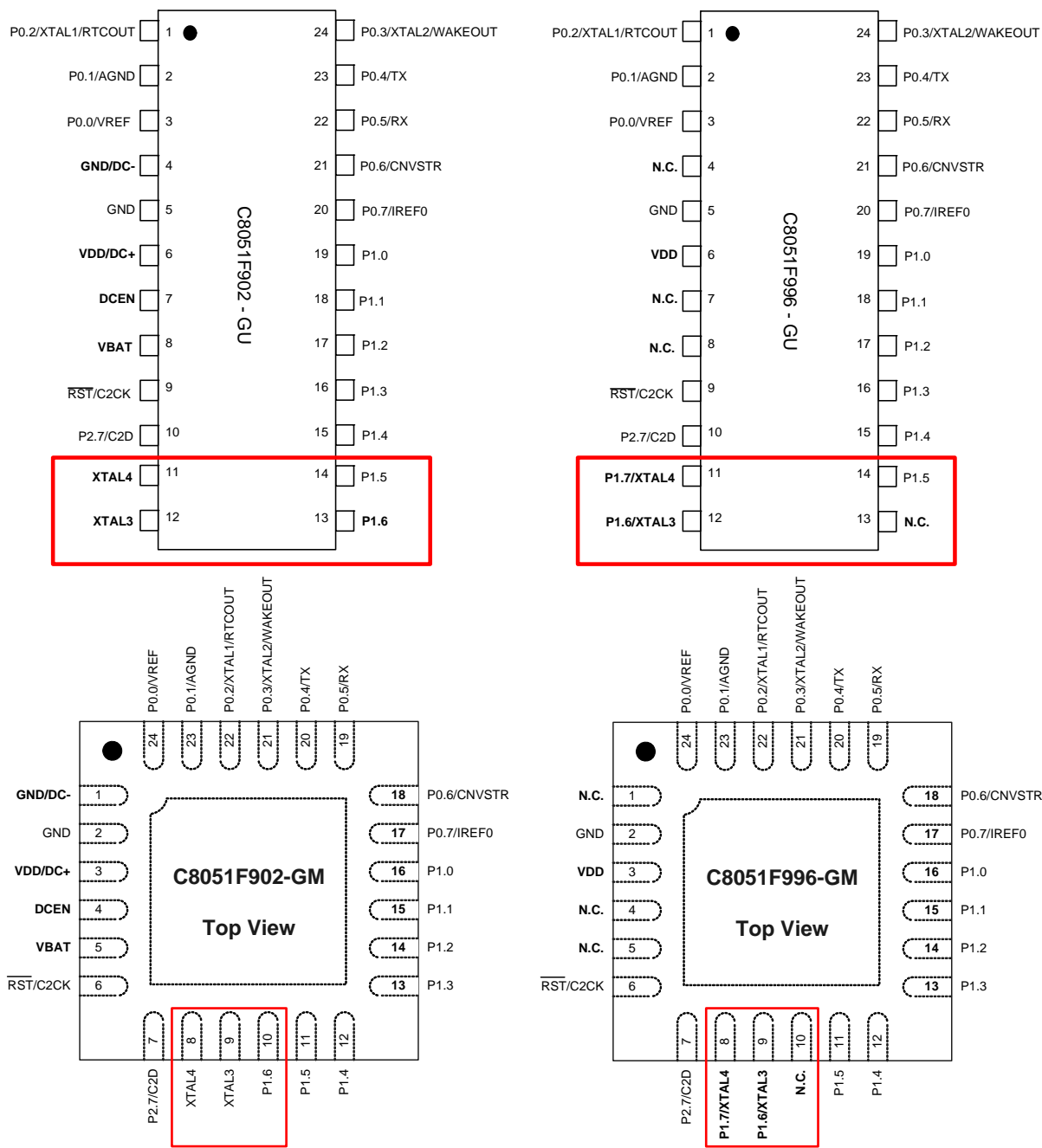


Figure 2. 24-Pin Device Pinout Differences

4. Similarities

There are many similarities between devices in the C8051F91x-90x and C8051F99x-98x product families. The behavior of the following peripherals is identical between the two families. Functions or peripherals not listed below have minor differences in implementation, and these differences are described in detail in the following paragraphs.

- UART0
- SPI0
- IREF0
- CIP-51
- Interrupt Handler—Interrupt numbers for functionality present on both devices (e.g., ADC0, Timers, UART, etc) is unchanged.
- Timer 0, Timer 1, Timer 2
- SMBus
- ADC0

5. Memory

Devices in the two product families have different memory sizes; however, flash memory is organized in 512 byte pages in both families. C8051F91x-90x devices have a 512 byte scratchpad. C8051F99x-98x devices do not have a scratchpad. The lock byte and reserved area of flash varies between device families and between devices in each value. Refer to the device data sheet for the exact location of the lock byte in the device being used.

In some applications, it is useful to determine the device part number at runtime. On C8051F91x-90x devices, this is done by reading address 0x3FFE in flash memory. On C8051F99x-98x, the DEVICEID SFR register on SFR Page 0xF can be read to determine the device part number at runtime.

C8051F91x-90x devices have 768 bytes (256 + 512) of RAM. C8051F99x-98x devices have 512 bytes (256 + 256) of RAM.

6. SFR Map

C8051F91x-90x and C8051F99x-98x devices have different SFR maps. Software being ported from one device to another must specify the *C8051F990_defs.h* header file if the target is a C8051F99x-98x device or the *C8051F912_defs.h* header file if the target is a C8051F91x-90x device.

7. Clocking

C8051F99x-98x devices include a clocking option (Low Power Oscillator divided by 8), which is not found on C8051F91x-90x devices. This option consumes less power than dividing the Low Power Oscillator by 8 using the global system clock divider. See the CLKSEL register description for details.

The two device families have different values for the reset value of the VREG0CN register. On C8051F91x-90x devices, the Precision Oscillator Bias is enabled on reset, allowing software to enable the Precision Oscillator at any time without writing to the VREG0CN register. If the Precision Oscillator is not used, its bias may be disabled in order to achieve the lowest active mode current.

In order to save power, C8051F99x-98x devices have the Precision Oscillator Bias disabled on reset. In order to use the Precision Oscillator, software must enable the Precision Oscillator Bias by writing to the VREG0CN register before enabling the Precision Oscillator.

8. DC-DC Converter

The dc-dc converter, which allows a supply voltage as low as 0.9 V, is available only on C8051F91x-90x devices. The minimum supply voltage for C8051F99x-98x devices is 1.8 V.

9. SPI

SPI0 is identical between both device families. SPI1 is only present on C8051F91x-90x devices.

10. PCA

The only difference in the PCA is that C8051F91x-90x devices have six capture/compare modules, and C8051F99x-98x devices have three capture/compare modules. The watchdog timer function is always located on the last capture/compare module.

11. Timer 3

On C8051F91x-90x devices, Timer 3 has the ability to count or capture Comparator 1 rising edges. On C8051F99x-98x devices, this functionality is replaced by the ability to count or capture SmaRTClock rising edges.

12. Comparator

C8051F99x-98x devices only have a single comparator (CP0), and its inputs are restricted to P1.0 and P1.1. C8051F91x-90x devices have two comparators (CP0 and CP1) with input multiplexers that may be connected to a selection of pins.

13. CRC Engine

The CRC engine on C8051F91x-90x devices supports a 32-bit and a 16-bit mode. When used with the automated flash interface, it has a page size of 512 bytes. The CRC SFRs may only be accessed from SFR Page 0xF.

The CRC engine on C8051F99x-98x devices only supports a 16-bit mode and has a page size of 256 bytes. The CRC SFRs may be accessed from SFR Page 0x0 or SFR Page 0xF.

14. Voltage Reference

The precision voltage reference is only available on C8051F91x-90x devices. Both families include an on-chip 1.65 V, High Speed Voltage reference that does not require an external capacitor.

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