1. Introduction

The purpose of this document is to introduce the subject of gapped clocks, how they can be used in network timing, and their impact upon phase locked loop (PLL) technology. Gapped clocks see widespread use in Optical Transport Network (OTN/OTU) applications, and are also used in broadcast video and other application areas. One of the key requirements of an OTN/OTU network is to insert plesiochronous payloads into an OTN/OTU wrapper. That is, because the data transmission rate of the timing IC and the rate of the payload source may not be exactly the same, they may drift with respect to one another, and some method must exist to make up the rate difference. A common technique is to generate a reference clock with missing clock edges (or gaps) to keep the incoming and outgoing data rates synchronized. A phase locked loop supporting gapped clock inputs is required to provide this function. However, whenever a clock is gapped, there is a significant increase in its jitter. A jitter attenuating PLL with a high amount of jitter tolerance and attenuation is then required to produce a low-jitter clock at the same average frequency of the gapped clock that will be usable by the system.

2. Background on Synchronous and Asynchronous Networks

Synchronous networks have a hierarchical approach to distributing network timing. They do this by establishing a timing master and slaving the various sub networks and nodes to the master. This approach has met with success for SONET/SDH and packet-based wide area networks.

In contrast, local area networks tend to generate timing locally and slave the immediate receiver's timing to the transmit timing of the node that is driving it. The transmitting node's timing is often completely asynchronous to the timing of its receiver.

Two examples of these two distinct approaches are SONET and Ethernet, though neither uses purely a single approach.

SONET typically synchronizes everything to one timing master and distributes timing in a hierarchical manner. However, there are two distinct problems with this approach:

1. Transport paths can experience jitter and wander with magnitudes that can be greater than one UI (unit interval or the period of the clock frequency).

2. Some payloads cannot be made synchronous and must remain plesiochronous.

The solution that SONET has adopted is payload pointers, which embed the frame slip information into the overhead portion of the SONET frame. Pointer processing is a very effective method of embedding plesiochronous payloads in synchronous SONET frames; but, as the SONET data rates have increased over the year, pointer processing has become more and more difficult to implement in FPGAs and ASICs.

Traditionally, every Ethernet transmitter runs at a rate that is determined by its local and individual timing source, which is usually a crystal oscillator, which is a free running clock with ±100 ppm accuracy. The receiving node slaves its timing to the transmitting source using the isochronous timing information that is embedded in the Ethernet data stream. This approach is both efficient and inexpensive; however, one consequence is that timing mismatches between the various asynchronous nodes can accumulate and result in bit errors and dropped packets. This is not a serious issue for the data payloads that Ethernet was intended to carry because the higher level IP protocols implement frame error detection and retransmission. However, as voice payloads have become more common, the situation is more complicated because packet retransmission interrupts the steady flow required for good voice sound quality. Synchronous Ethernet (SyncE) and Timing Over Packet (IEEE-1588) are two methods of distributing synchronization through packet networks so that they can interoperate with traditional circuit switches services, such as SONET/SDH.

The solution that is used by OTN/OTU is a compromise between SONET and Ethernet in that it is specifically designed to accept plesiochronous payloads and efficiently place them in containers that are ready for optical transmission over long distances. The timing master for an OTN/OTU node can be asynchronous, and the OTN/OTU wrapper can accept payloads from a variety of sources. It is quite common for OTN/OTU systems to use gapped clocks to achieve these goals.
3. **Quick Review of PLL Basics**

A PLL is a closed loop system that typically provides two functions:

1. Translates one frequency to another, which is typically done by multiplying the input frequency by an exact ratio.
2. Jitter attenuation (clock noise filtering).

Item 2 merits further discussion. The jitter transfer function describes the closed loop response of a PLL to jitter present at its input. Figure 1 shows a plot of the magnitude of the jitter attenuation as a function of the jitter frequency component for an Si5324 any-frequency jitter attenuating clock multiplier with a loop BW of 10 Hz.

Figure 1 indicates that the reference clock jitter with a frequency of 100 Hz will be attenuated by more than 20 dB by the Si5324. Jitter at 10 Hz will be attenuated by 3 dB. Jitter at 1 Hz will effectively not be attenuated at all. When viewed this way, a PLL acts like low-pass filter for the jitter with a cutoff frequency equal to the loop bandwidth of the PLL.

![Figure 1. Jitter Attenuation](image)

Given the PLL's bandwidth's impact on jitter attenuation, it is reasonable to ask what would be the PLL's response to a change in its input frequency. Figure 2 represents the Si5324's response to a step function in its frequency. The vertical axis is normalized to the size of the step, and the horizontal axis is time from the frequency step in milliseconds. The Si5324 PLL bandwidth is 10 Hz.

The graph in Figure 2 is based on the inverse Laplace transform of the Si5324's transfer function and is limited to small step sizes (< ~500 ppm). As the size of the step increases, the assumption of linearity begins to break down.
Figure 2. Si5324 Frequency Step Response
4. What is a Gapped Clock?

Gapped clocks are periodic clock signals of a single clock frequency that have clock pulses removed from their stream. Well-formed gapped clocks do not have reduced width pulses (known as runt pulses). Rather, each individual clock pulse is either completely present or completely absent. In a typical application (as shown in Figure 3), one in N clock pulses is removed, where N can be a constant or can be constrained to be within a range of values.

![Figure 3. Gapped Clock Example](image)

5. Generic Gapped Clock Application Example

To illustrate how a gapped clock may be used, consider the gapped clock transmitter block diagram in Figure 4.

![Figure 4. Typical Gapped Clock Transmitter](image)

**Data source clock rate < XO clock rate**

In this example, the data source is plesiochronous with respect to the transmission output rate. That is, the fixed clock can be implemented with an XO or a TXCO that is not locked to anything, including the data source clock. The data source clock and data go into a FIFO so that data coming in at a uniform rate can be clocked out of the FIFO with a clock that is aperiodic, i.e. gapped.
The purpose of the framer is to add FEC (forward error correction), framing, and other overhead bits that are needed to create a wrapper that conforms to whatever convention or protocol is in use. For this to function properly, the output clock rate must be higher than the data source clock rate because bits are being added to the stream. The amount by which the output rate is higher than the sum of the two input sources (the Din from the FIFO and the added framing, FEC, etc. bits) provides the necessary elasticity for when the data source rate drifts in frequency with respect to the rate of the fixed clock. It is necessary to maintain enough elasticity to accommodate the worst-case mutual drift between the two clocks.

To this end, the gap logic inserts or removes justification bits into or from the stream to equalize the long term input flow rate to the output flow rate. In order to do this, the gap logic needs to be aware of the FIFO status. When the FIFO is nearing empty, more clocks are gapped, and there are more justification bit events. When the FIFO is becoming full, fewer clocks are gapped, and there are fewer justification events.

Looking at the above example receiver, the CDR (clock data recover) separates the isochronous data stream into clock and data signals. The framer/mapper detects the presence of the frame and other overhead bits and applies this to the AND gate, which is used to gap the clock. Since the input clock to the FIFO only occurs for payload bits, only the payload bits enter the FIFO. This also entails that the FIFO input clock will not be strictly periodic (by virtue of it being gapped). Since downstream consumers of the output data are not usually tolerant of gapped clocks, an Si5324 jitter attenuating PLL is used to create a clock output that has the same average frequency as the gapped clock. The Si5324 jitter attenuation ensures that the clock output jitter is low enough to drive the subsequent logic. The 99 MHz and 100 MHz frequencies refer to the following spectra and phase noise plots.
6. Clock Gapping Patterns and Jitter

Removing clock pulses from a periodic clock produces large amounts of jitter. The Si5324 PLL attenuates this jitter and produces an output clock with the frequency of the gapped input clock averaged over a period of time. The time frame over which this averaging occurs is determined by the loop BW of the Si5324. Even though the peak clock rate at the input of the Si5324 will be higher than the frequency at the output of the Si5324, the average frequency at the input will be the same as the average frequency at the output. In the process, the output jitter will be significantly lower than the input jitter. The amount of jitter attenuation is determined by a combination of the rate at which the clock is gapped and the loop BW of the Si5324. Figure 6 shows a simple example of this process that has a base clock rate of 100 MHz with gaps that generate an average clock frequency of 99 MHz.

![Figure 6. 100 MHz Gapped at 1 MHz](image)

The time between gaps is 1 µs; so, the gap rate is 1 MHz. Note that 100 MHz – 1 MHz = 99 MHz. The spectrum of this clock will have components at N x 1 MHz and at M x 100 MHz (see "Appendix—Fourier Analysis" on page 12). The N x 1 MHz components are jitter and should be attenuated to produce a low-jitter clock at the Si5324 output. It is for this reason that the loop BW of the Si5324 needs to be significantly below 1 MHz. In the spectrum shown in Figure 7, the base clock rate is on the far left hand side, and the 2nd harmonic of 200 MHz is on the far right hand side. Between the two, the N x 1 MHz spur can be seen.

![Figure 7. Raw Gapped Clock Spectrum](image)
Figure 8 shows a spectrum of the same clock, but with a zoomed-in view. Again, the 100 MHz base clock rate is on the far left hand side. The N x 1 MHz components can be seen at regular 1 MHz intervals. Note that although both of these plots show only the single sideband, the N x 1 MHz components extend down in frequency below 100 MHz with the lowest component located at 1 MHz.

Figures 7 and 8 are spectra of the raw gapped clock. Figure 9 shows the spectrum for the same gapped clock, but after the jitter attenuating Si5324. It can be seen that the N x 1 MHz spurs are gone. Note that the fundamental frequency is now 99 MHz instead of 100 MHz because the Si5324's output is the average of the clock input frequency, not its peak frequency.
In practice, it is very difficult to take a phase noise plot of a gapped clock because typical phase noise equipment cannot locate the carrier of a gapped clock. That is, the jitter of a gapped clock is so large that, to the equipment, there is no discernable carrier frequency. It is for this reason that a phase noise plot of the raw gapped clock is not shown. However, the following plot is of the jitter attenuated output of the Si5324. The RMS jitter of 303 fs is brick wall integrated from 12 kHz to 20 MHz.
Even though phase noise equipment cannot easily take measurements of gapped clocks, time domain instruments like oscilloscopes with high speed, single-shot sampling rates can measure the jitter of gapped clocks. An Agilent DSA90804A Digital Signal Analyzer was used to measure the jitter of the raw gapped clock. The peak-to-peak jitter of the gapped clock was 20 ns, while the RMS jitter was 702 ps.

Figure 10. Si5324 Output Phase Noise Plot
7. Justification

Justification is the dynamic insertion or removal of clocks in response to small changes due to drift in the relative frequency difference between the transmitter's output clock and the data source clock (see Figure 4). Justification is required because the two systems are plesiochronous; that is, even though the two clocks in question may be very close to the same frequency, they are not locked to one another, and there will be relative drift that changes with time, temperature, etc.

As dramatic as the Si5324 jitter attenuation is, it should be remembered that the lowest frequency component of the jitter is at 1 MHz, and the loop BW of the Si5324 is below 10 Hz. Because justification compensates for frequency drift and because drift is a slowly changing event, there will be justification information at low frequencies. This means there will be jitter frequency components associated with justification that can be arbitrarily low in frequency and therefore can be below the loop BW of any PLL, including the Si5324. Because the jitter component is at a frequency that is below the loop BW of the Si5324, such jitter will pass through the Si5324 unattenuated.

What saves this situation is that the OTN/OTU (and other) jitter masks have a hi-pass cutoff frequency, which establishes a lower bound to the jitter that needs to be attenuated. For example, see Figure 11, which is an OTU1 jitter integration mask that is to be applied to the jitter data. The OTU1 mask has a hi-pass cutoff frequency of 5 kHz so that jitter well below 5 kHz is not of concern to the OTU system. Since the Si5324’s loop BW is below 10 Hz, there is a significant amount of jitter attenuation for jitter at 5 kHz. Without the low loop BW of the Si5324, jitter from justification will not be attenuated and will compromise link integrity.

![Figure 11. Jitter Mask Example: OTU1](image)

### Table 1. OTU Masks

<table>
<thead>
<tr>
<th>Interface</th>
<th>Measurement Bandwidth –3 dB Frequencies (Hz)</th>
<th>Peak-to-Peak Amplitude (UIpp)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OTU1</td>
<td>5 k to 20 M</td>
<td>1.5</td>
</tr>
<tr>
<td></td>
<td>1 M to 20 M</td>
<td>0.15</td>
</tr>
<tr>
<td>OTU2</td>
<td>20 k to 80 M</td>
<td>1.5</td>
</tr>
<tr>
<td></td>
<td>4 M to 80 M</td>
<td>0.15</td>
</tr>
<tr>
<td>OTU3</td>
<td>20 k to 320 M</td>
<td>6.0</td>
</tr>
<tr>
<td></td>
<td>16 M to 320 M</td>
<td>0.18</td>
</tr>
</tbody>
</table>
8. Conclusion

Gapped clocks present a significant challenge to PLLs because clock gaps look like jitter at 1 UI pk-pk to the PLL. Because of both the magnitude of the jitter and the frequency component of the jitter due to justification, it is imperative that a low loop BW PLL like the Si5324 be used. The loop BW of the PLL must be significantly below the hi-pass cut off of the relevant jitter mask.
Viewing this gapped clock in the frequency domain will help in understanding how the loop BW of the Si5324 will attenuate the jitter due to gapping. First, note the following Fourier series:

\[ G(t) \quad \text{Frequency domain:} \quad G(f) \]

\[ A(t) \quad \text{Frequency domain:} \quad A(f) \]

\[ B(t) \quad \text{Frequency domain:} \quad B(f) \]

**Figure 12. Fourier Series of a Pulse Train**

For a periodic train of ideal pulses with a period of T, the Fourier series will be a set of pulses in frequency at a distance of 1/T from one another. This means that the Fourier series of a periodic 100 MHz clock is a set of pulses in frequency that are 100 MHz apart from one another with a period of 10 nsec.

**Figure 13. Ungapped Clock Fourier Series**

Using the above Fourier series, the gapping function in the earlier example can be represented as shown in Figure 14.

**Figure 14. Gapping Function Fourier Series**
In the time domain, if the gapping function \( B(t) \) is subtracted from the ungapped clock \( A(t) \), the result will be the gapped clock that is being analyzed \( C(t) \). That is, \( A(t) - B(t) = C(t) \). This result relies on the fact that addition (or subtraction) in the time domain is the same as addition in the frequency domain.

**Figure 15. Gapped Clock Spectrum**

What this result tells us is that the spectrum of a clock that is gapped in the manner described above will have frequency components at \( M \) times the gap rate mixed in with components at \( N \) times the base clock rate (for \( N,M = 1,2,3,\ldots \)). Though this is not typically the case, in our simple example, 100 MHz is divisible by 1 MHz; so, the components overlap.
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