This application note details the creepage and clearance requirements of an isolator type component, such as a digital isolator, used to provide protection from electric shock. It also details layout recommendations to enhance a design's robustness and ensure compliance with end safety standards.

To ensure safety in end-user applications, high voltage circuits (i.e., circuits with >30 VAC) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with <30 VAC) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and provide a sufficient high-voltage breakdown protection rating (commonly referred to as working voltage protection). Refer to the end-system specification (61010-1, 60950-1, 60601-1, etc.) requirements before starting any design that uses a digital isolator. These standards dictate both the working voltage requirement and the creepage/clearance distance spacing necessary to deem an end product safe for end-customer use.
1. Key Term Definitions

The following are key terms that should be understood before reading this application note:

**Safety Extra-Low-Voltage**—A voltage less than 30 VRMS (60 VDC)

**Hazardous**—A voltage greater than 30 VRMS (60 VDC)

**Basic Insulation**—A single-level of protection against electric shock. See Table 2.

**Reinforced/Double Insulation**—Two-levels of protection against electric shock. See Table 2. Rated (Proof) Isolation Voltage—The maximum voltage an isolation barrier is rated to withstand. This is typically 2500, 3750, or 5000 VRMS for 1 minute.

**Production Isolation Test Voltage**—The voltage to which an isolation component manufacturer must test the component in order to be compliant with a given standard. This test voltage is typically 1.2x the Rated Isolation Voltage for a test duration of 1 second. Each standard has slightly different test voltage requirements. The most strenuous and inclusive requirement is chosen for this test.

**Creepage**—The shortest path between two conductive parts measured along the surface of the insulation.

![Figure 1.1. Creepage](image1)

**Clearance**—The shortest path that an arc may travel through air.

![Figure 1.2. Clearance](image2)

**Time-Dependent Dielectric Breakdown**—The amount of time it takes a component's isolation barrier to fail for a given voltage. In general, the lower the voltage, the exponentially longer the time a safety component can survive.

**Pollution Degree**—The end environment in which an end system is used. Table 1 summarizes the different pollution degrees. Silicon Laboratories digital isolators are rated to Pollution Degree 2.

- **Pollution Degree 1**: No pollution or only dry, nonconductive pollution occurs. The pollution has no effect.
- **Pollution Degree 2**: Normally, only nonconductive pollution occurs. Temporary conductivity caused by condensation is to be expected.
- **Pollution Degree 3**: Conductive pollution or dry nonconductive pollution that becomes conductive due to condensation. This is to be found in industrial environments or construction sites (harsh environments).
- **Pollution Degree 4**: The pollution generates persistent conductivity caused by conductive dust, rain, or snow. The following table lists pollution degree definitions.
Table 1.1. Pollution Degree Definitions

<table>
<thead>
<tr>
<th>Pollution Degree 1</th>
<th>Pollution Degree 2</th>
<th>Pollution Degree 3</th>
<th>Pollution Degree 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clean room environments</td>
<td>Equipment being evaluated at 60950</td>
<td>Electrical equipment in industrial and farming areas</td>
<td>Electrical equipment for outdoor use</td>
</tr>
<tr>
<td>Inside sealed components</td>
<td>Laboratories</td>
<td>Unheated rooms</td>
<td></td>
</tr>
<tr>
<td>Office environments</td>
<td>Test stations</td>
<td>Boiler rooms</td>
<td></td>
</tr>
</tbody>
</table>

The following table details some typical differences between basic and reinforced isolation requirements. See the specific standard for your design, as creepage requirements will vary from one standard to another. The numbers listed below provide a good rule of thumb for most standards.

Table 1.2. Typical Differences between Basic and Reinforced Isolation Requirements

<table>
<thead>
<tr>
<th>Insulation Type</th>
<th>Creepage/Clearance</th>
<th>Proof (Rated) Test</th>
<th>Production Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic</td>
<td>3.2 mm</td>
<td>2500 V_{RMS} (1 min)</td>
<td>3000 V_{RMS} (1 sec)</td>
</tr>
<tr>
<td>Reinforced/Double</td>
<td>6.4 mm</td>
<td>5000 V_{RMS} (1 min)</td>
<td>6000 V_{RMS} (1 sec)</td>
</tr>
</tbody>
</table>
2. Selecting Adequate Creepage and Clearance for a Given Specification

The amount of creepage distance required for a given system depends on the end system’s certification standard. In general, this distance is dictated by the Pollution Degree of the environment in which the system will be used and the highest working voltage present in the system. For example, the IEC60950-1 regulates the requirements for Telecom Equipment, and the IEC61010-1 regulates the requirements for Industrial and Test Equipment. The table below lists the Basic Insulation creepage requirements for IEC60950-1. From this table, one can see that the Basic Insulation creepage distance required for a Pollution Degree 2, Material Group IIIa/b (the most common material group), 250 V<sub>RMS</sub> system is 2.5 mm. A component whose package provides less is not adequate for the design.

<table>
<thead>
<tr>
<th>Working Voltage (VRMS or VDC)</th>
<th>Functional, Basic, and Supplementary Insulation</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Pollution Degree 2</td>
</tr>
<tr>
<td></td>
<td>Material Group</td>
</tr>
<tr>
<td></td>
<td>I</td>
</tr>
<tr>
<td>&lt;50</td>
<td>0.6</td>
</tr>
<tr>
<td>100</td>
<td>0.7</td>
</tr>
<tr>
<td>150</td>
<td>0.8</td>
</tr>
<tr>
<td>250</td>
<td>1.3</td>
</tr>
<tr>
<td>400</td>
<td>2.0</td>
</tr>
</tbody>
</table>

Note:
1. The data in this table is for basic isolation. Double all the distances for reinforced insulation. Dimensions are in millimeters.

2.1 Creepage Distance Provided by Silicon Labs Packages

Silicon Labs offers numerous packages with various creepage distances. The following table details these differences.

<table>
<thead>
<tr>
<th>Package</th>
<th>Nominal Creepage (mm)</th>
<th>Creepage in Air Per IEC60112 (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>QSOP-16</td>
<td>3.6</td>
<td>3.6</td>
</tr>
<tr>
<td>SOIC-8</td>
<td>4.01</td>
<td>3.9</td>
</tr>
<tr>
<td>NB SOIC-16</td>
<td>4.01</td>
<td>3.9</td>
</tr>
<tr>
<td>WB SOIC-16</td>
<td>8</td>
<td>7.6</td>
</tr>
<tr>
<td>DIP8</td>
<td>7</td>
<td>7</td>
</tr>
<tr>
<td>SDIP6</td>
<td>8.3</td>
<td>8.3</td>
</tr>
<tr>
<td>LGA8</td>
<td>10</td>
<td>10</td>
</tr>
</tbody>
</table>

For most of the packages listed above, the Nominal creepage and the creepage in air as determined by IEC60112 (the standard that defines how to measure creepage) is the same. However, it should be noted that the JEDEC standard, 16 lead WB SOIC package has 7.6 mm of creepage. This is less than the nominal 8 mm of creepage listed due to the metal tabs left on the sides of the package during manufacturing. This 7.6 mm is adequate for most applications; however, some 220–250 VAC medical and industrial systems require 8 mm to ensure safety. All isolation suppliers using typical, non-custom, JEDEC standard SOIC packages have this same restriction on creepage (note that this condition is similar for the other SOIC packages listed above). To achieve the 4.01 and 8 mm of creepage for these JEDEC SOIC packages, conformal coating is required to cover the metal tabs.
2.1.1 Using PTI and CTI to Reduce Creepage Distance Requirements

The required creepage distance can be reduced if an isolation component has been qualified to a higher proof tracking index (PTI) rating or comparative tracking index (CTI) rating. In many cases, the distance can be cut in half if the component is rated to Material Group I instead of Material Group IIIa or IIIb (the most common ratings for components). For example, from Table 2.1 IEC60950-1 MAINS Creepage Requirements on page 3, the end user can reduce the required creepage from 4 to 2 mm (for a 400 V RMS based system) if the component is rated to material group I. Silicon Laboratories isolator packages are all rated to Material Group I and Pollution Degree 2. Additional certification paperwork might be necessary to accommodate this creepage distance reduction. IEC60112 details the CTI/PTI testing standard.

2.1.2 Using Grooves to Extend Effective Creepage Distance for a Given Package

PCB grooves can be used to increase the creepage distance for a given package in a given system. See the figure below; clearance is not affected since it is line-of-sight. When using grooves, ensure that the groove does not weaken the PCB to the point that the board fails standard mechanical tests.

![Figure 2.1. PCB Grooves Used to Increase Creepage Distance](image-url)
2.2 Ensuring an Adequate Withstand Rating

The second requirement of a safety component is its voltage withstand rating. Every safety component has a Time Dependent Dielectric breakdown profile. Time-dependent breakdown is unique to each component. Manufacturers of safety components usually provide these profiles in their data sheets. The following figures illustrate the profiles for the Si86xxxx family.

![Figure 2.2. Si86xxxB Time-Dependent Dielectric Breakdown](image1)

![Figure 2.3. Si86xxxD Time-Dependent Dielectric Breakdown](image2)
Table 2.3. Test Voltages for Electric Strength Tests for Each Working Voltage Range

<table>
<thead>
<tr>
<th>Grade of Insulation</th>
<th>Working Voltage</th>
<th>Test Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>&lt;184 Vpk or dc</td>
<td>1000</td>
</tr>
<tr>
<td></td>
<td>184 &lt; U &lt; 354 Vpk or dc</td>
<td>1500</td>
</tr>
<tr>
<td></td>
<td>354 &lt; U &lt; 1414 Vpk or dc</td>
<td>3000</td>
</tr>
<tr>
<td>Basic ($V_{RMS}$)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reinforced ($V_{RMS}$)(^1)</td>
<td>2000 (3200)</td>
<td>3000 (4800)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3000 (4800)</td>
</tr>
</tbody>
</table>

**Note:**
1. For isolation components with non-homogeneous construction, such as the Si8xxx devices, reinforced insulation requires a 1.6x multiplier.

### 2.3 Choosing a Component with Adequate Creepage

Assume a designer is designing telecom equipment (e.g., a blade server) whose electronic board is used in a Pollution Degree 2 environment. Also assume the server's control board powers from the main line and is universally powered (up to 250 VAC).

**Q:** What type of isolation components are required by IEC60950-1 for this system?

**A:** The answer is found by going to the IEC60950-1 specification. For convenience, refer to Table 2.1 IEC60950-1 MAINS Creepage Requirements on page 3 and Table 2.3 Test Voltages for Electric Strength Tests for Each Working Voltage Range on page 6 in this document. From Table 2.1 IEC60950-1 MAINS Creepage Requirements on page 3, the component must have a creepage of 5 mm (assumes Material group IIIa; only 2.6 mm is required for a component in Material group I). Also, from Table 2.3 Test Voltages for Electric Strength Tests for Each Working Voltage Range on page 6, the component must pass a 4800 V$_{RMS}$ 1–minute qualification test and be rated for 250 V$_{RMS}$ reinforced insulation. A glance at these tables may suggest that the requirements are larger than necessary. However, since the system is powered from a 250 V$_{RMS}$ mains power source, reinforced insulation is in fact required. This reinforced insulation requirement increases the overall required creepage distance and 1–minute sustained voltage requirements of the system as dictated by IEC60950-1. From Table 2.2 Typical Creepage Distances Offered by Silicon Labs Packages on page 3, one can see that the WB SOIC-16, DIP8, SDIP6 or LGA8 package could be used for this application. CTI/PTI documentation would need to be submitted if a smaller package was necessary.
3. Layout Recommendations

The following guidelines can be used to enhance the layout design of systems using digital isolators. Refer to the family data sheets for more details concerning specific devices.

3.1 PCB Material

For safety reasons, it is recommended that standard epoxy-glass PCB material Flame Retardant 4 (FR-4) be used in all designs since it meets the requirements of Underwriters Laboratories UL94-V0. Cheaper alternatives have higher dielectric losses at high frequencies, absorb more moisture, and provide less strength and stiffness. Moreover, FR-4 exhibits flammability characteristics that are self-extinguishing. Assuming a rise/fall time >1 ns, trace lengths up to 10 inches can be supported for data rate of 150 Mbps.

3.1.1 Use Four-Layer Designs

Four layers of metal are required to achieve a low EMI PCB design.

• To avoid issues caused by stray impedances from vias, route the high-speed traces on the top layer.
• To establish controlled impedances and provide low-inductance current return paths for high-speed signals, place a solid ground plane next to the high-speed signal layer.
• To increase high-frequency bypass capacitance, place the power plane next to the ground.
• Since slower speed signals radiate less energy, route these signals on the bottom layer. These signals usually have fewer critical layout requirements when EMI is an issue.

The above order can be reversed if it facilitates the design.

3.1.2 Use Conformal Coating to Reduce Creepage Requirements

As discussed earlier, a higher CTI/PTI rated device reduces the creepage/clearance requirements for most end systems. Conformal coating is also an alternative to higher CTI/PTI and grooves can be used to reduce creepage/clearance requirements. Since the typical voltage breakdown in air is approximately 1100 V/mm, a 4 mm creepage rate component (not including the internal barrier's isolation) will break (arc) down at approximately 4400 V. The breakdown of a component with conformal coating is significantly higher than that of air (usually 5x). Refer to standards requirements when supplementary isolation, such as conformal coating, is used.

3.1.3 Use these Routing Guidelines

Use the following guidelines to avoid noise pickup and lower EMI. See the reference section for additional layout recommendations.

1. Use appropriate bypass capacitors (usually 0.1 µF, 1 µF) between VDD and GND. The capacitors should be placed as close as possible to the package. See the data sheet for exact details.
2. Place bulk capacitors (10 µF) close to power components.
3. Use 45° bends instead of right-angle (90°) bends for signals. This enhances impedance matching.
4. To reduce inductances, avoid changing layers with signals.
5. Use power and ground planes to control impedances and minimize noise from power components.
6. Use short trace lengths between the isolator and connecting circuits.
7. To enhance the robustness of a design, it is further recommended that the user also add 1 µF bypass capacitors and include 100 W resistors in series with the inputs and outputs if the system is excessively noisy.
4. References

5. Document Change List

Revision 0.1 to Revision 0.2

Revision 0.2 to Revision 0.3
• Updated 2.2 Ensuring an Adequate Withstand Rating.
• Updated Figure 2.2 Si86xxxB Time-Dependent Dielectric Breakdown on page 5.
• Added Figure 2.3 Si86xxxD Time-Dependent Dielectric Breakdown on page 5.
• Updated Table 2.3 Test Voltages for Electric Strength Tests for Each Working Voltage Range on page 6.
Disclaimer
Silicon Laboratories intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Laboratories products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and “Typical” parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Laboratories reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Laboratories shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products must not be used within any Life Support System without the specific written consent of Silicon Laboratories. A “Life Support System” is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Laboratories products are generally not intended for military applications. Silicon Laboratories products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.

Trademark Information
Silicon Laboratories Inc., Silicon Laboratories, Silicon Labs, SiLabs and the Silicon Labs logo, CMEMS®, EFM, EFM32, EFR, Energy Micro, Energy Micro logo and combinations thereof, “the world’s most energy friendly microcontrollers”, Ember®, EZLink®, EZMac®, EZRadio®, EZRadioPRO®, DSPLL®, ISOmodem®, Precision32®, ProSLIC®, SiPHY®, USBXpress® and others are trademarks or registered trademarks of Silicon Laboratories Inc. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA
http://www.silabs.com