
DESIGN OF PRINTED TRACE DIFFERENTIAL LOOP ANTENNAS

1. Introduction

This application note discusses the general principles involved with designing a printed circuit trace differential loop antenna, suitable for use with sub-GHz RFICs, such as the Si4010/Si4012 from Silicon Labs. This application note also provides a general tutorial on how to design a differential loop antenna, using a combination of design equations and simulation techniques.

Use of loop antennas in small radio devices is often desirable for several reasons. Many modern RFICs use differential circuitry to achieve better performance and provide rejection against common-mode signals; the inherent differential structure of a loop antenna interfaces well to such circuitry. Loop antennas are primarily H-field radiators (compared with E-field radiators, such as monopole antennas) and are somewhat less susceptible to de-tuning because of hand or body effect. Loop antennas may easily be designed using printed circuit traces, allowing a reduction in Bill of Material (BOM) cost. They may also be designed with a relatively small physical size, allowing integration in a very small form factor.

However, designing a loop antenna (or any antenna) is not the simplest of tasks. It would be convenient to simply select an antenna design from a proven library of existing designs, or to construct an antenna from a template design and then further scale the dimensions to the desired frequency of operation. In practice, however, it is rarely possible for a designer to copy an existing antenna design **exactly**, without any modification; it is generally necessary to change the antenna layout (at least slightly) to fit within the user's form factor. Even such minor modifications can result in changes in the performance of the antenna. Thus, new antenna designs generally require simulation and/or bench adjustment, unless they are exact replicas of existing designs.

2. Design Approach

Silicon Labs recommends the following approach to design a loop antenna:

1. Estimation of required antenna dimensions using basic design equations, given the desired link range.
2. Calculation of tuning components required to resonate loop antenna at the desired operating frequency.
3. Simulation of proposed antenna geometry using antenna/EM simulation software.
4. Fabrication of PCB containing printed antenna structure.
5. Bench measurement of antenna resonant frequency and input impedance.
6. Adjustment of discrete tuning capacitors to optimize resonant frequency and input impedance.
7. Modification of physical layout of antenna structure (only if adjustment of discrete components is not sufficient).

Although it is obviously desirable to achieve optimal performance on the initial design, it is generally not possible to calculate or simulate with this degree of accuracy. Most simulations inherently make use of simplifications or approximations in order to speed up simulation time and to reduce simulation memory requirements. These simplifications often introduce small errors in the simulation results that must then be corrected through measurement and adjustment on the bench. While it is sometimes possible to increase the complexity of the simulation model to reduce these errors, the result is generally a drastic increase in required simulation time for only a moderate improvement in simulation accuracy. In short, it is usually quicker to use just enough complexity in the simulation to “get close enough”, and to complete the optimization of the design through bench measurement and adjustment. It is quite normal for an initial fabricated antenna design to match no closer than 5%–10% to the simulation results (e.g., the actual measured resonant frequency differs slightly from the simulated resonant frequency). These differences can generally be corrected through adjustment of discrete tuning components, without the need for another board spin.

2.1. Design Characteristics of Loop Antennas

The following represents a brief list of some of the characteristics of loop antennas; each of these items is discussed in further detail below.

- Differential structure
- High input impedance
- Narrowband (high-Q)
- Resonant frequency is inversely proportional to loop size
- More efficient radiator with larger loop size

2.1.1. Differential Structure

The loop antenna is nominally a balanced structure and thus interfaces well to a differential circuit, such as a differential PA output or a differential LNA input. The designer should strive to maintain physical symmetry of the antenna layout in order to obtain optimal performance.

2.1.2. High Input Impedance

The input impedance of a loop antenna at natural resonance is quite high, ranging anywhere from ~10 k Ω to 50 k Ω . This characteristic high input impedance is a result of the loop antenna operating in a parallel-resonant mode at the desired frequency of operation. This impedance value is much higher than the typical impedance of the circuitry to which the antenna is expected to interface (e.g., PA output or LNA input). It is possible to transform the loop antenna impedance to a lower value through the use of discrete reactive components (e.g., capacitors) or through the use of impedance transforming structures (e.g., a tapped loop). However, it may not always be possible to achieve a complex conjugate match (desirable for optimum power transfer), due to other constraints such as peak voltage swing.

2.1.3. Narrowband (High-Q)

The natural resonance of a loop antenna is quite narrowband, perhaps only 5–10 MHz in bandwidth. The tuning of a loop antenna may be affected by nearby objects (i.e., hand effect or body effect); thus it is recommended that some method of automatically tuning the antenna back to resonance be provided in the RFIC. One advantage of a high-Q antenna is that it provides attenuation of harmonic signal components, allowing the filtering required from discrete circuitry to be relaxed (or even eliminated).

2.1.4. Resonant Frequency

The natural resonant frequency of a loop antenna is inversely proportional to the size of the loop antenna: the larger the antenna, the lower its natural frequency of resonance. However, it is generally possible (through the use of discrete tuning components) to tune a small loop antenna to resonance at frequencies well below its natural resonant frequency. This is usually desirable, as the discrete tuning components also provide a means by which the high native impedance may be transformed to a lower and more useful value.

2.1.5. Radiation Efficiency

The radiation efficiency of a loop antenna generally increases with size. If the designer has a choice in selecting the loop antenna size (assuming both may be tuned to resonance through the use of discrete tuning components), the larger antenna will generally provide better performance.

3. Loop Antenna Design Equations

A typical rectangular printed loop antenna structure is shown in Figure 1, where:

- a_1, a_2 = dimensions of the sides of the loop antenna (in meters), measured from the center of the traces
- t = thickness of the trace conductor (in meters)
- w = width of the trace conductor (in meters)

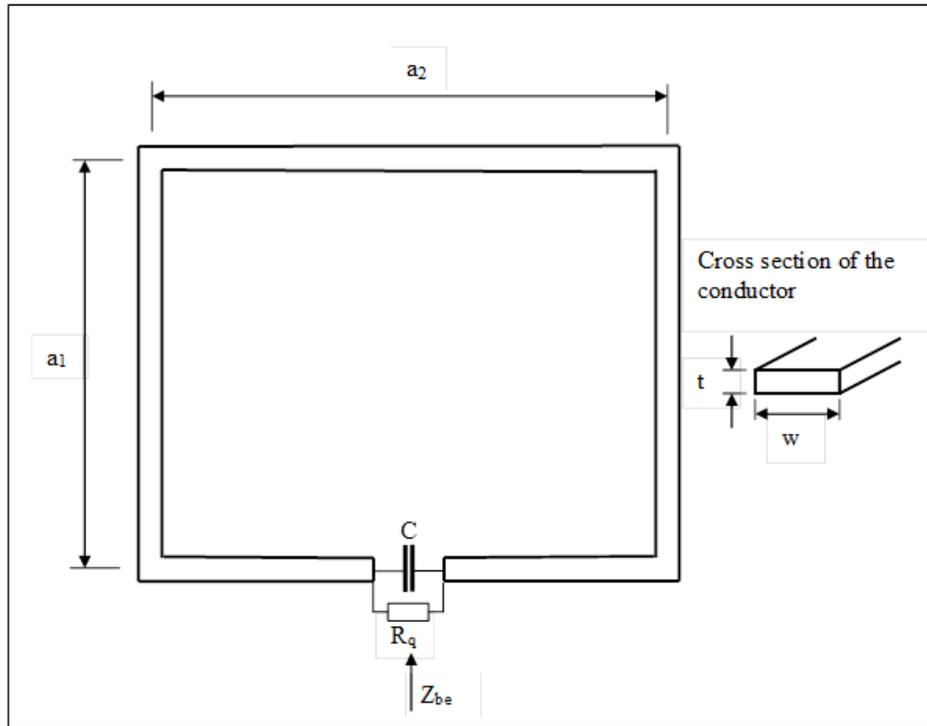


Figure 1. Printed Loop Antenna

From these dimensions the total length (i.e., perimeter) of the loop (in meters) and the area of the loop (in meters²) may be calculated as:

$$l = 2 \times (a_1 + a_2)$$

Equation 1.

$$A = a_1 \times a_2$$

Equation 2.

Many equations for inductance assume a conductor with a circular cross-section of radius 'b' (i.e., a wire). An **effective** radius 'b' of a printed trace conductor may be calculated as:

$$b = 0.35 \times t + 0.24 \times w$$

Equation 3.

The inductance of a square loop ($a_1 = a_2 = a$) may be calculated as¹:

$$L = \frac{2 \times \mu_0 \times a}{\pi} \times \left[\ln\left(\frac{a}{b}\right) - 0.774 \right]$$

Equation 4.

Here, μ_0 equals the free space permeability and is given by:

$$\mu_0 = 4\pi \times 10^{-7} = 1.256E-6 \text{ H/m}$$

In the event that a rectangular loop antenna is used ($a_1 \neq a_2$), Equation 4 may be still be used with an effective or mean loop dimension:

$$a = \sqrt{a_1 \times a_2}$$

Equation 5.

In the event a circular loop antenna is used, the inductance may be calculated as²:

$$L = \mu_0 \times a \times \left[\ln\left(\frac{8a}{b}\right) - 2 \right]$$

Equation 6.

The radiation resistance of a small loop antenna is given by³:

$$R_{\text{RAD}} = 320\pi^4 \left[\frac{A^2}{\lambda^4} \right] = 320\pi^4 \left[\frac{A^2 f^2}{v^4} \right]$$

Equation 7.

¹C.A. Balanis, "Antenna Theory: Analysis and Design", John Wiley & Sons, 2005, p. 245.

²Ibid.

³Ibid, p. 238.

Radiation resistance is a “good” type of loss mechanism, as it is through the mechanism of radiation resistance that power is transferred from the applied conducted signal to the free space wave. However, there are other loss mechanisms present in the antenna as well, including ohmic trace loss (R_{TRACE}), PCB dielectric loss (R_{PCB}), and ESR of discrete tuning components (R_{ESR}) due to finite Q-factors. The total series resistance of the loop antenna is the sum of all of these factors:

$$R_{SER} = R_{RAD} + R_{TRACE} + R_{PCB} + R_{ESR}$$

Equation 8.

The radiation efficiency of the loop antenna is given by the ratio of the radiation resistance to the total series resistance:

$$\eta_r = \frac{R_{RAD}}{R_{RAD} + R_{TRACE} + R_{PCB} + R_{ESR}} = \frac{R_{RAD}}{R_{SER}}$$

Equation 9.

From these equations, it is clear that the efficiency (gain) of the antenna may be optimized by increasing the radiation resistance while minimizing the other loss factors. The high-frequency resistance of a printed trace (assuming very small skin depth) may be calculated as:

$$R_{TRACE} = \frac{1}{2W} \sqrt{\frac{\pi f \mu_0}{\sigma}}$$

Equation 10.

Here, sigma represents the conductivity of copper (5.8E7 Siemens/meter).

These equations show that the trace loss $R_{TRACE} \sim \text{loop perimeter} \sim (\text{loop area})^{1/2}$, while $R_{RAD} \sim (\text{loop area})^2$. As loop size is increased, the radiation resistance increases faster than the trace loss and the efficiency of the loop antenna is improved with larger loop area.

Therefore, the antenna designer should (nearly) always strive to maximize the size of the loop antenna within the available board space.

However, the loop antenna size should not be increased so large that it approaches self-resonance on its own, without the need for capacitor tuning elements; the resonant frequency of such an antenna would be quite sensitive to small variations in the design parameters.

The designer may be familiar with the characteristic impedance of more commonly encountered antenna structures such as dipoles ($Z_0 = 73 \Omega$) and monopoles ($Z_0 = 36.5 \Omega$). In contrast, the radiation resistance of a typical loop antenna is quite low, on the order of a few ohms (or less).

In practice, the electromagnetic field surrounding a loop antenna exists partially within the dielectric material of the PCB and partially in free space. The velocity factor of a signal within the dielectric material is lower than that of free space, and thus the wavelength is correspondingly smaller. It is well known that the velocity factor in a medium other than free space is inversely related to the square root of the permittivity of the medium, and is given by:

$$v_{PCB} = \frac{c}{\sqrt{\epsilon_r}}$$

Equation 11.

In Equation 11, 'c' equals the speed of light in free space (3E8 meters/second). As the electromagnetic field exists simultaneously in both mediums (free space and the board dielectric material), the appropriate value of wavelength (λ) to use in Equation 7 is a value somewhere **between** the wavelength in free space and the wavelength in the board material. The author is not currently aware of an explicit formula to correctly predict the effective velocity factor (and thus the effective wavelength) of a signal that spans across two different mediums. However, a series of antenna simulations may be performed in which all other loss mechanisms are disabled except that loss due to radiation; from these simulations the radiation resistance R_{RAD} may be extracted and compared to the value predicted by Equation 7. The velocity factor may then be empirically adjusted until the predicted values "curve fit" to the simulated values. From this exercise, an appropriate value of value of velocity factor may be found:

$$V.F. = 0.82$$

Equation 12.

That is to say, the appropriate value of wavelength (λ) to be used in Equation 7 is 0.82x that calculated in free space.

The loss due to the dielectric material (R_{PCB}) is also a challenge to estimate. This loss factor is related to the loss tangent (δ) of the dielectric material. The simulations and examples within this application note assume FR-4 board material with loss tangent $\delta = 0.02$. Again, the author is not currently aware of an explicit formula to relate the loss resistance R_{PCB} to the loss tangent, operating frequency, and board area. Once again, a series of simulations may be performed in which individual loss mechanisms are sequentially disabled, allowing extraction of the loss resistance due to **only** the dielectric loss tangent. This simulation exercises results in the following set of curves of dielectric loss resistance R_{PCB} as a function of antenna area and operating frequency. The designer may use these curves to estimate the loss resistance due to the FR-4 board material for a particular antenna design.

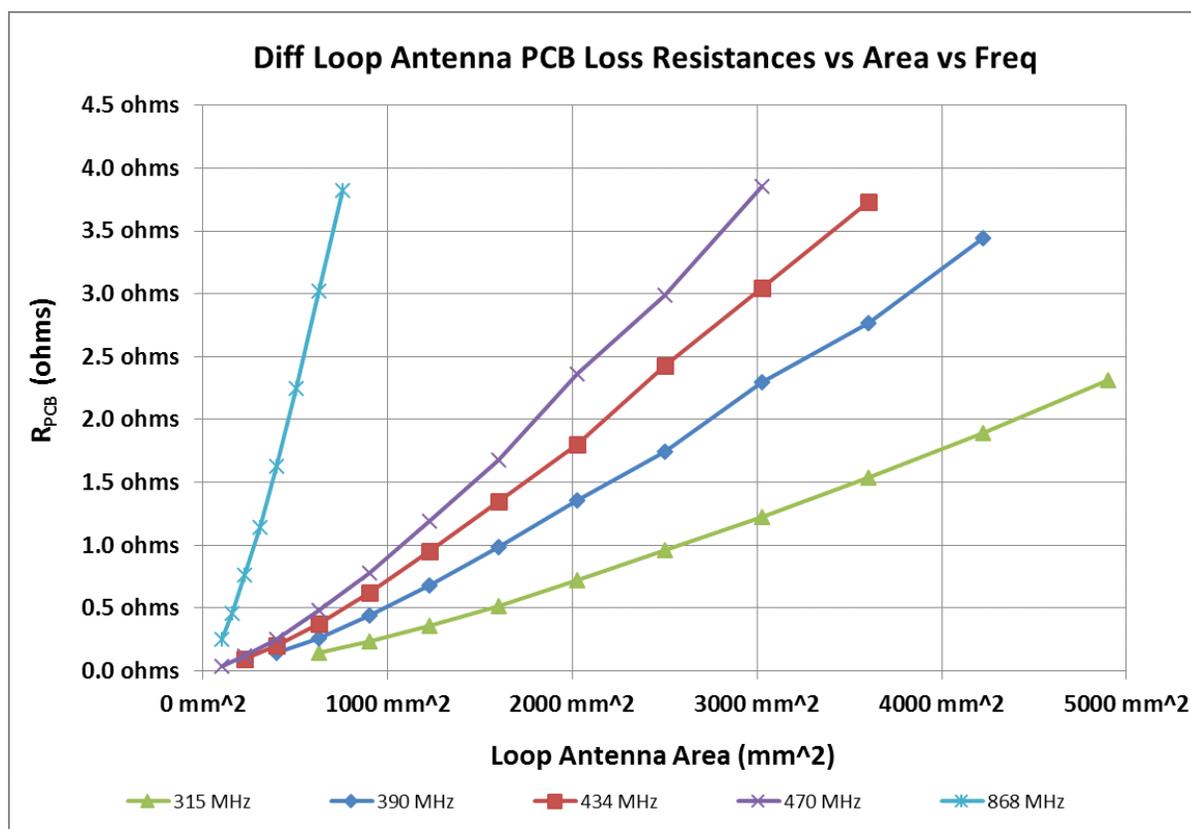


Figure 2. Dielectric Loss Resistance R_{PCB} vs. Area vs. Frequency

4. Loop Antenna Practical Design

Armed with knowledge of these basic design equations and performance curves, it is now possible to design a practical loop antenna. As an example, the area of a loop antenna that fully occupies the available space within a typical remote keyless entry (RKE) keyfob for an automobile may be only 40 mm x 25 mm = 1000 mm². A trace width of 1.0 mm is assumed with a copper weight of 1 oz.

- F = 434 MHz
- a1 = 40 mm
- a2 = 25 mm
- t = 0.035 mm (1 oz. copper)
- w = 1.0 mm

Application of Equation 7 at an operating frequency of F = 434 MHz and applying the empirically-derived velocity factor of V.F. = 0.82 results in:

$$R_{\text{RAD}} = 320\pi^4 \left[\frac{(0.04 \times 0.025)^2}{(0.82 \times 3E8/434E6)^4} \right] = 0.302 \Omega$$

Equation 13.

Application of Equation 10 results in a calculated value of trace resistance R_{TRACE} of:

$$R_{\text{TRACE}} = \left(\frac{2 \times 0.04 + 2 \times 0.025}{2 \times 0.001} \right) \sqrt{\frac{\pi \times 434E6 \times 1.256E-6}{5.8E7}} = 0.353 \Omega$$

Equation 14.

It is evident that the loss due to the trace resistance exceeds the radiation resistance, and thus the radiation efficiency is expected to be relatively low (refer to Equation 9). The radiation efficiency will degrade even further as the remaining loss mechanisms (i.e., dielectric loss and component ESR) are accounted for.

The dielectric loss resistance may be estimated from the curves of Equation 2 as being R_{PCB} = ~0.7 Ω at an operating frequency of 434 MHz and loop area of 1000 mm².

The inductance of the loop antenna may be calculated from Equation 4 and Equation 5 as:

$$L = \frac{2 \times \mu_0 \times \sqrt{a_1 \times a_2}}{\pi} \times \left[\ln \left(\frac{\sqrt{a_1 \times a_2}}{b} \right) - 0.774 \right] = 102.64 \text{ nH}$$

Equation 15.

An equivalent lumped-element model of the loop antenna is simply an inductor in series with a resistor. The inductance may be resonated with a capacitor of value:

$$C = \frac{1}{(2\pi f)^2 L} = 1.31 \text{ pF}$$

Equation 16.

The equivalent series resistance (R_{ESR}) of this capacitor is a function of its Q-factor. A reasonable estimate of the Q of surface-mount ceramic capacitors (e.g., Murata GJM1555 series) is $Q \approx 350$. The R_{ESR} may be calculated as:

$$R_{ESR} = \frac{X_C}{Q} = \frac{1}{2\pi f C Q} = \frac{1}{2\pi \times 434E6 \times 1.31pF \times 350} = 0.799 \Omega$$

Equation 17.

The total series resistance may be calculated as:

$$R_{SER} = R_{RAD} + R_{TRACE} + R_{PCB} + R_{ESR} = 0.302 + 0.353 + 0.7 + 0.799 = 2.154 \Omega$$

Equation 18.

The expected antenna efficiency may be estimated by Equation 9 as:

$$\eta_r = \frac{R_{RAD}}{R_{RAD} + R_{TRACE} + R_{PCB} + R_{ESR}} = \frac{0.302}{2.154} = 0.14$$

Equation 19.

The antenna efficiency may be expressed in dBi (dB relative to an isotropic antenna):

$$G_{ANT_EFF} = 10 \times \log(\eta_r) = -8.53 \text{ dBi}$$

Equation 20.

This quantity represents the radiation efficiency of the antenna when summed over all spatial directions. The antenna gain typically measured in a lab environment or antenna chamber reflects the product of the antenna efficiency and the antenna directivity.

The loop antenna may be brought to parallel resonance by placing this capacitor across the input terminals of the differential loop antenna.

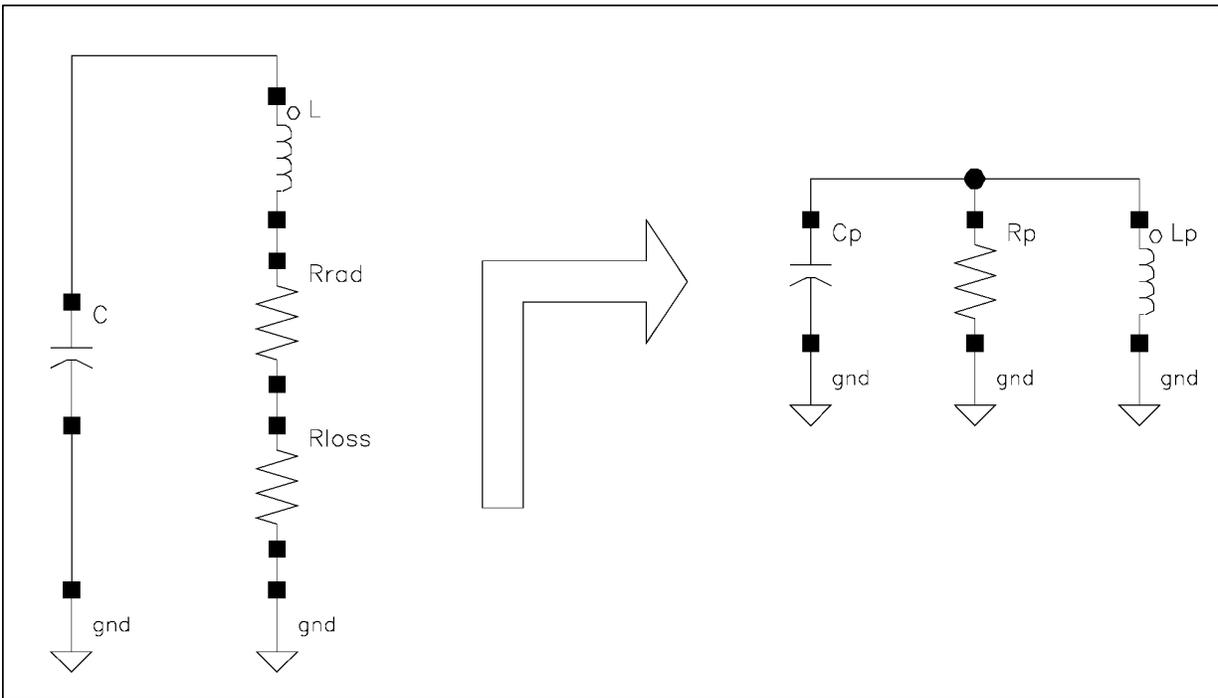


Figure 3. Series and Parallel Lumped Equivalent Models

The series equivalent lumped element model may be transformed into a parallel equivalent model, as shown in Figure 3. Due to the high Q-factor of the network, the parallel values of L and C remain (approximately) the same, while the parallel resistance may be calculated as:

$$X_{L_{SER}} = 2\pi fL = 2\pi \times 434E6 \times 102.64nH = 279.89 \Omega$$

Equation 21.

$$R_P = R_{SER}(1 + (Q_{SER})^2) = R_{SER}\left(1 + \left(\frac{X_{L_{SER}}}{R_{SER}}\right)^2\right) = 2.154\left(1 + \left(\frac{279.89}{2.154}\right)^2\right) = 36.37 \text{ k}\Omega$$

Equation 22.

The total series resistance of a loop antenna was observed to be quite low (a few ohms or less); in contrast, the transformed parallel resistance is quite high (several tens of kilohms). Without further impedance matching, this high value of resistance would be observed at the input terminals of the antenna at parallel resonance (i.e., at the frequency where the reactances of L_P and C_P cancel each other).

As this antenna impedance is much higher than the typical output impedance of a PA circuit or input impedance of an LNA circuit, it is common to transform this high impedance downwards to better match the impedance of the circuit. This impedance transformation may be provided by discrete capacitors, discrete inductors, distributed transmission lines, or a combination thereof; however, the most commonly used method is “capacitive-tapping,” as shown in Figure 4. Capacitors are typically used as discrete matching elements because their Q-factor is usually much higher than inductors, causing them to minimize any additional loss in the match.

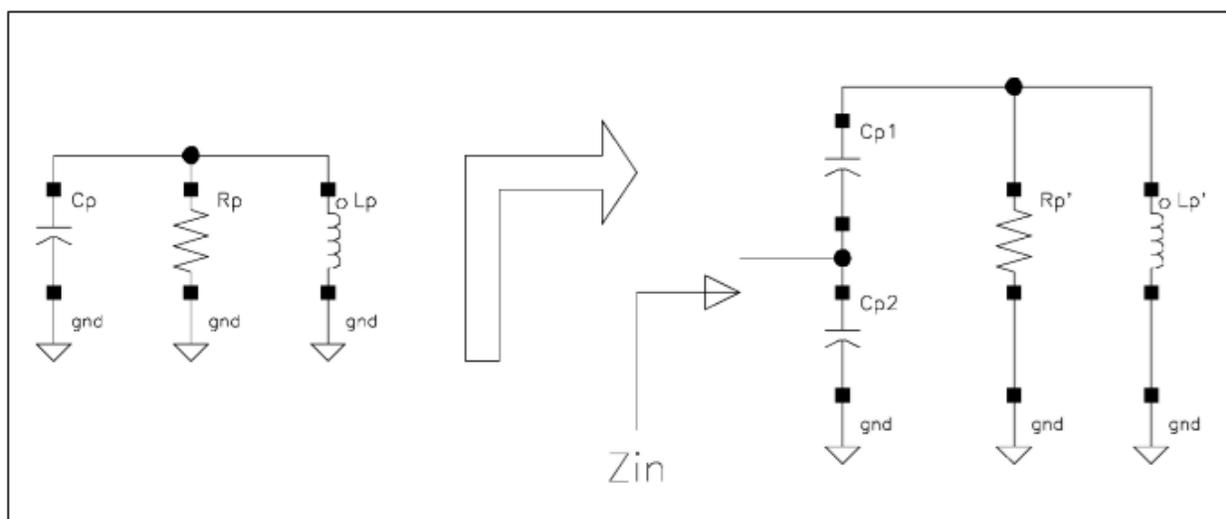


Figure 4. Capacitive-Tapping Impedance Transformation

The **exact** equations for expressing the input impedance Z_{IN} as a function of L_p , R_p , C_{p1} , and C_{p2} are rather tedious. However, the high-Q nature of the antenna circuit allows use of some approximations that significantly simplify the equations, resulting in the following expressions:

$$C_p = \frac{C_{p1}C_{p2}}{C_{p1} + C_{p2}}$$

Equation 23.

$$\frac{R_p}{R_{IN}} = \left(1 + \frac{C_{p2}}{C_{p1}}\right)^2$$

Equation 24.

Here, R_{IN} is the desired impedance to which to match the antenna.

From Equation 24, it is evident that a large impedance transformation ratio (i.e., a low value of R_{IN}) is obtained by using a small ratio of $C_{p1}:C_{p2}$, that is, the value of C_{p1} must be much less than C_{p2} . From this, the following two observations may be made:

- The resonant frequency of the antenna is controlled (primarily) by adjusting C_{p1} .
- The transformed impedance seen at the antenna input is controlled by adjusting the ratio of $C_{p2}:C_{p1}$.

The PA output circuit of the Si4010 chip is a switched programmable current source that delivers pulses of current to the load impedance. Thus, the amount of power delivered to the load (i.e., antenna) is given by the well-known equation:

$$P_{OUT} = I_{PA_BIAS}^2 R_{IN}$$

Equation 25.

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It is clear that the power delivered to the load may be increased by raising either the PA bias current or the antenna load resistance. However, this relationship only holds true up to the point where the output voltage swing ($V = I_{PA_BIAS} \times R_{IN}$) exceeds the value at which voltage clipping occurs in the PA output devices. For the Si4010 chip configured for the maximum value of PA bias current, the load resistance at which clipping occurs is $R_{IN} \approx 500 \Omega$. As a result, this value is often stated as being the optimal load resistance for the Si4010 chip, and is usually the design target for the input impedance of a loop antenna.

The required ratio of $C_{P2}:C_{P1}$ may then be calculated from Equation 24.

$$\frac{R_p}{R_{IN}} = \frac{36370}{500} = 72.74 = \left(1 + \frac{C_{p2}}{C_{p1}}\right)^2$$

Equation 26.

$$\frac{C_{p2}}{C_{p1}} = \sqrt{72.74} - 1 = 7.53$$

Equation 27.

Equation 23 and Equation 27 may now be solved simultaneously for the individual values of C_{P1} and C_{P2} (recalling that C_P is the total value of capacitance required to resonate the antenna inductance).

- $C_{P1} = 1.484 \text{ pF}$
- $C_{P2} = 11.17 \text{ pF}$

The capacitively-tapped equivalent circuit model of Figure 4 actually has two resonant modes: a series resonance and a parallel resonance. This is more readily apparent by re-drawing the circuit model as shown in Figure 5.

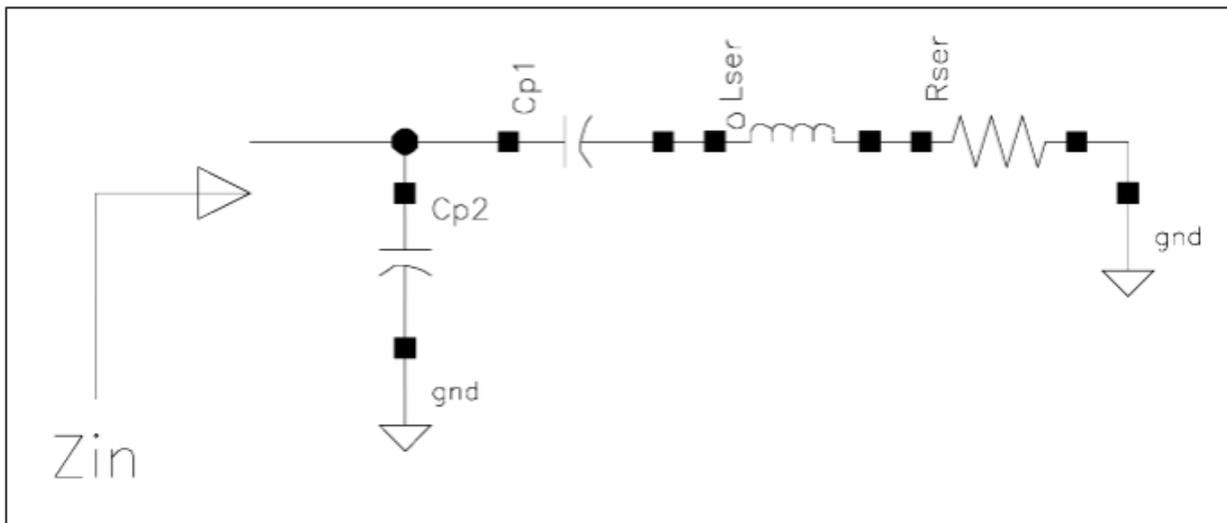


Figure 5. Capacitively-Tapped Circuit Model (Re-Drawn)

It is evident that L_{SER} will achieve series-resonance with C_{P1} at some frequency F_{SER} . Above this series resonant frequency, the L_{SER} - R_{SER} - C_{P1} arm will appear inductive and will subsequently achieve parallel-resonance with C_{P2} at some frequency F_{PAR} . This parallel-resonant frequency F_{PAR} is the desired operating frequency for the loop antenna and is **always** located above F_{SER} , for this type of matching network.

The lumped element equivalent circuit model of Figure 5 may be simulated for its impedance behavior over frequency, using the component values calculated previously and summarized below:

- $L = 120.64$ nH
- $C_{P1} = 1.484$ pF
- $C_{P2} = 11.17$ pF
- $R_{SER} = 2.154$ Ω

The simulated $\text{Mag}(Z_{in})$ response of the equivalent circuit model is shown in Figure 6. The series and parallel resonant frequencies are clearly apparent.

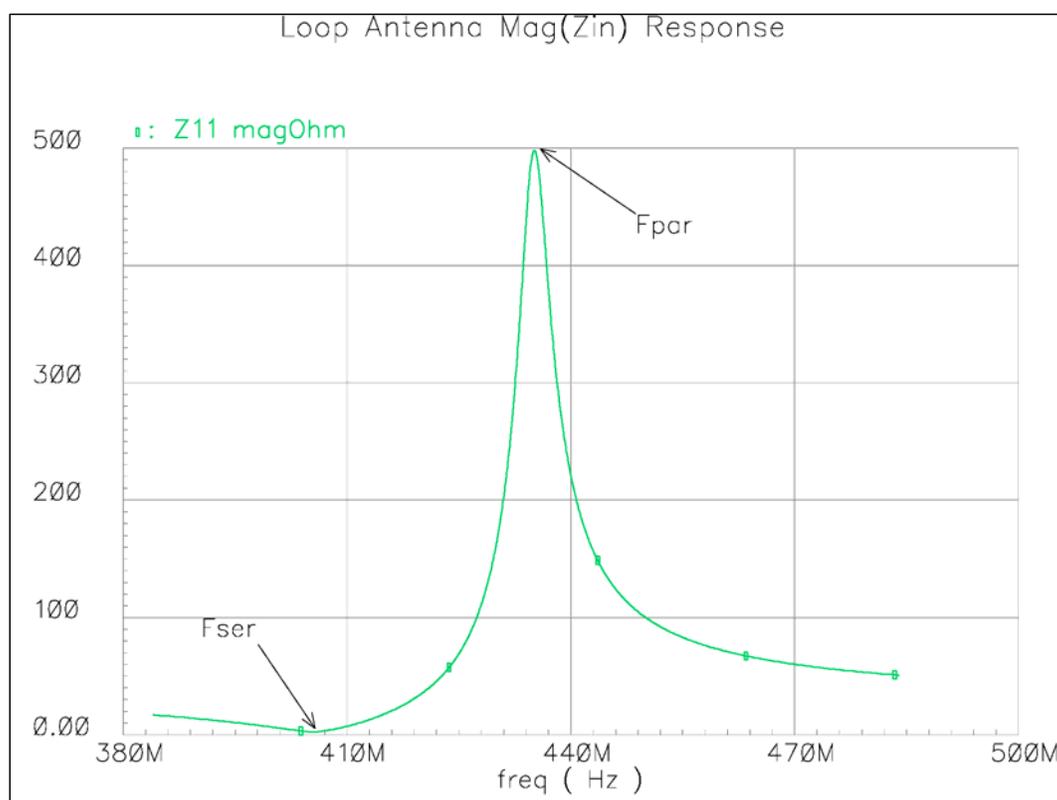


Figure 6. $\text{Mag}(Z_{in})$ Response of Capacitively-Tapped Circuit Model

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The simulated S11 response of the equivalent circuit model is shown in Figure 7. The Smith Chart is normalized to the design target impedance of $Z_0 = 500 \Omega$.

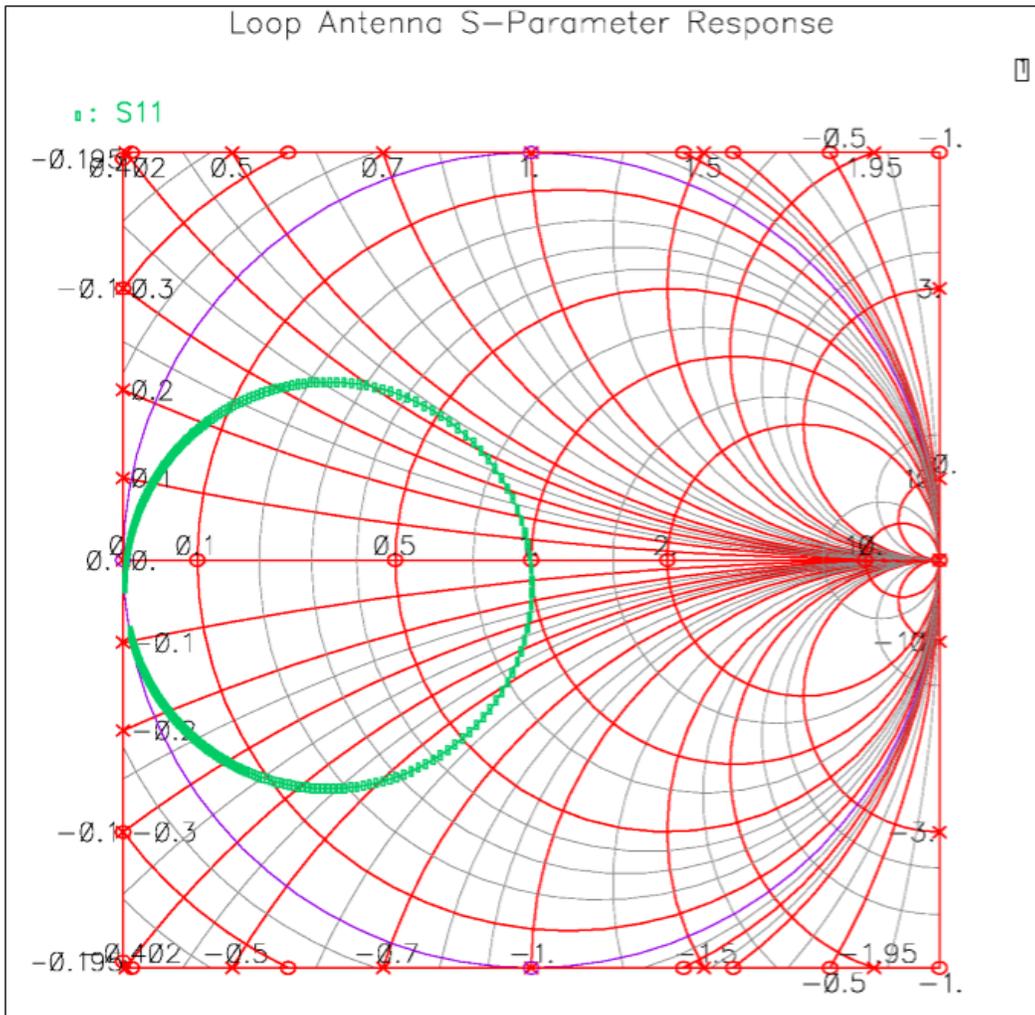


Figure 7. S-Parameter Response of Capacitively-Tapped Circuit Model

5. Loop Antenna Simulation

5.1. Sonnet Simulation Environment

Silicon Labs uses the Sonnet EM Simulator. It is a 2.5 D simulator, ideal for planar antenna simulations. This simulator places the entire board structure in the cross section of a waveguide with metal walls, as shown in Figure 8. In order to obtain proper simulation results the waveguide walls should be at least a wavelength away from the radiating structure. To fulfill this requirement, the total cross-section size of the box should be at least $2\lambda \times 2\lambda$.

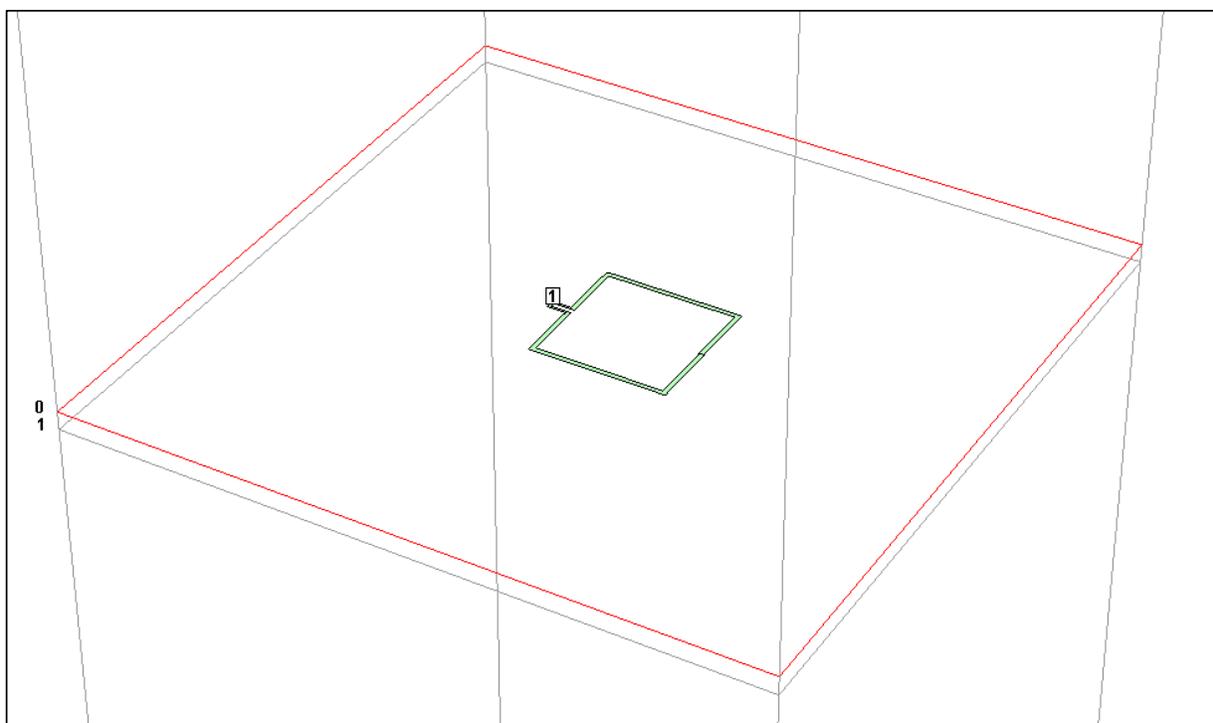


Figure 8. Sonnet Board Geometry Placed in Waveguide Structure for Simulation

Unfortunately, simulation time and required computational memory increases rapidly with waveguide box size. As a result, it is often advisable to perform initial simulations and preliminary tuning with a smaller box size, increasing the box size as a final step to allow accurate simulation of the radiation resistance and antenna gain. However, simulations with larger box sizes may also introduce problems due to resonances of the waveguide box structure itself resonances (i.e., TE or TM modes). These resonance modes may be predicted using the “Estimate Box Resonance” feature of Sonnet. It may be possible to increase the box size so greatly that these resonances are pushed well below the frequency of interest. However, for such a large box size the simulation time will increase significantly, as well as requiring significantly more memory. These simulation tradeoffs must be managed by the designer.

The waveguide box structure is defined to have free space terminations at the top and bottom of the box (i.e., above and below the PCB). The distances from the PCB material to the top and bottom covers of the box are chosen to ensure that the length of the waveguide box is less than $\frac{1}{2}\lambda$; if the waveguide length is chosen to be longer, standing wave resonances may be set up within the box itself.

The EM simulator assumes homogeneous PCB material along the whole waveguide cross-section (that is, stretching from box wall to box wall). In real life, the antenna is constructed on a PCB that is finite in dimension. This cut edge of the PCB material cannot be modeled in this simulation. Its effect upon simulation accuracy may be

minimized by ensuring that there is at least ~2 mm distance between the trace(s) of the loop antenna and the cut edge of the PCB material. This should be achievable in most antenna designs.

Additionally, certain features such as mounting holes or board slots cannot be simulated in Sonnet. The Sonnet simulator assumes the dielectric PCB material to be homogeneous and unbroken, stretching from box wall to box wall. There is no capability within Sonnet to “punch holes” within this dielectric material, and thus it is not possible to model the effect (if any) of mounting holes upon the performance of the antenna. However, from experience this influence is expected to be very slight.

It is theoretically possible to construct a simulation model that accounts for the presence of a large mass of metal near the loop antenna structure, such as a coin-cell battery. This is accomplished through the use of a “Thick Metal” structure in Sonnet. However, the memory requirements and simulation time increase drastically when thick metal structures are used.

The loop antenna structures discussed within this document are all differential structures. Therefore, the Sonnet simulation must be constructed to simulate the **differential** impedance of the loop antenna. In Sonnet, this is accomplished by placing the simulation port (Port 1) **between** the differential traces feeding the antenna structure. Reliable S parameter results may be obtained when using internal ports as long as the ports are ungrounded and differential. In such a case, it is not necessary to use ports situated at the box wall. As a result, the problematic effects of de-embedding long differential transmission lines are avoided.

It is normal for areas of the board that are not used for the loop antenna structure to be poured with GND plane. In the simulations shown within this document, these GND planes are removed in order to simplify the antenna model. As the simulated impedance is taken differentially between the feed lines of the antenna, there is no need for a local GND reference for the measurement port. Furthermore, this simulation model matches real-life antenna applications; in a typical hand-held design (e.g., keyfob) there is no connection between the local GND plane (i.e., negative terminal of the coin-cell battery) and earth GND.

5.2. Loop Antenna Impedance Simulation Example

The substrate material chosen for a design example is 0.8 mm thick FR-4, with an assumed dielectric relative permittivity of $\epsilon_r = 4.6$ and a loss tangent (dissipation factor) of $\delta = 0.02$. The board dimensions and loop antenna size typically vary as a function of the desired frequency of operation; however, this section continues with the previous design example at 434 MHz with loop dimensions of 40 mm x 25 mm, as shown in Figure 9. The width of the loop antenna traces are 1.0 mm, and 1-oz copper ($\sigma = 5.8E7$ Siemens/meter) is assumed.

Inspection of the geometry of Figure 9 shows dimensions of 39 mm x 24 mm, instead of the mentioned values of 40 mm x 25 mm. However, these dimensions are referenced from the inside edges of the antenna traces, while the equations developed in Section 3 and Figure 1 used dimensions referenced to the center of the traces. The loop dimensions are therefore equivalent.

The tuning capacitors C_{P1} and C_{P2} are implemented as ideal capacitors, but in parallel with an ideal resistor whose value is calculated to represent the equivalent parallel resistance due to the finite Q-factor of the capacitors. The Q of the capacitors is assumed to be $Q = 350$, a reasonable value for surface-mount ceramic capacitors. The series tuning capacitor C_{P1} is physically placed at the top-center of the loop, while the parallel tuning capacitor C_{P2} is placed across the input feed lines of the loop antenna. The Si4010 chip internally integrates an adjustable bank of capacitors across its TXP and TXM output pins (i.e., connecting to the feed lines of the loop antenna), and thus (depending on required value) there may be no need for an additional explicit C_{P2} capacitor, external to the chip.

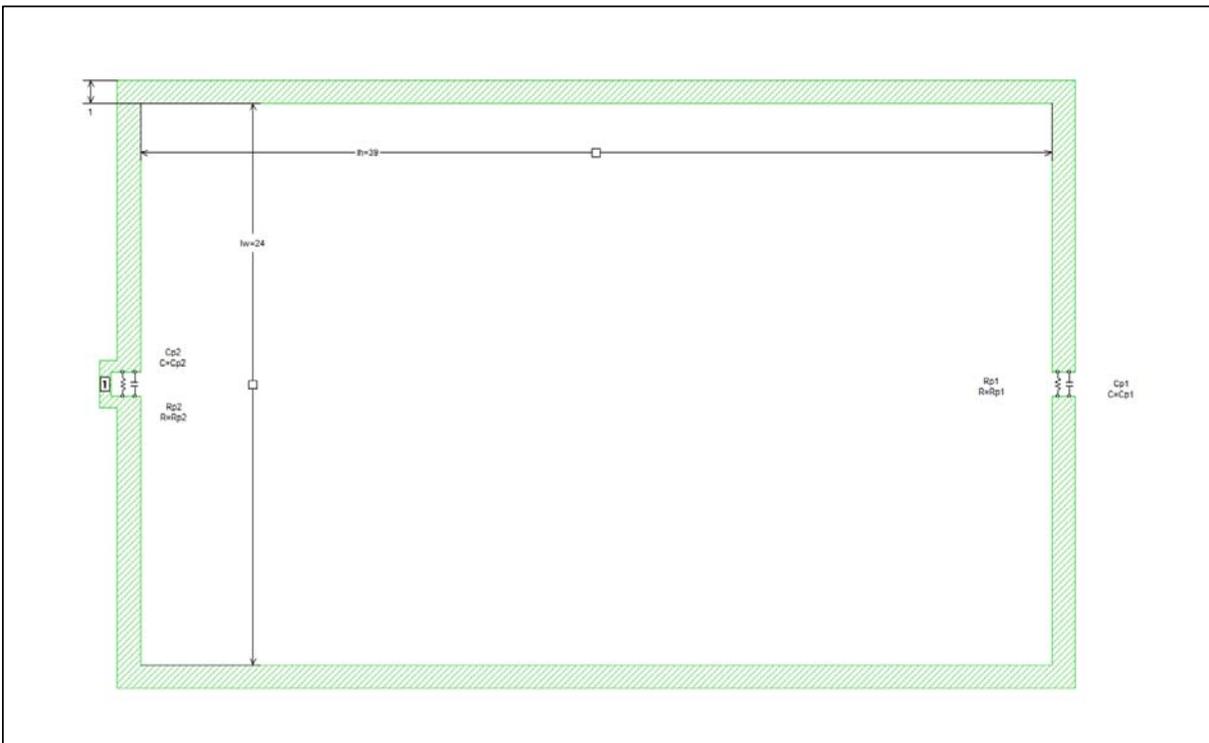


Figure 9. Sonnet Simulation Geometry for Example Loop Antenna

The initial simulated $\text{Mag}(Z_{in})$ impedance behavior of this loop antenna is shown in Figure 10. It is apparent that while the input impedance is close to our design target ($Z_{in} \approx 640 \Omega$, compared with target $Z_{in} = 500 \Omega$), the resonant frequency of this initial design is at ~ 397 MHz, well below our design target of 434 MHz. In other words, the agreement between simulation results and the theoretical design equations is not exact.

One reason for this discrepancy is the physical size of the loop antenna. A fundamental assumption underlying the development of the design equations in Section 3 is that the size of the loop is small compared to the wavelength at the desired operating frequency. If this assumption holds true, the instantaneous current is identical at all locations in the antenna, thus greatly simplifying the development of the theoretical equations. However, as the loop dimensions increase, the antenna traces begin to behave more like transmission lines instead of simple inductors. In such a case, the amplitude and phase of the instantaneous current may vary from one location to another along the antenna traces.

It is actually possible to construct a loop antenna of sufficient size so that it achieves parallel self-resonance on its own, without the need for a resonating capacitance. Antenna traces of such length therefore appear as a larger effective inductance than suggested by Equation 4, resulting in a lower actual frequency of resonance than predicted by the design equations.

The antenna designer is thus often presented with the following contradictory design goals:

- Maximize the loop antenna dimensions to optimize radiation resistance (which optimizes antenna efficiency).
- Use of a loop antenna with moderate dimensions to obtain good agreement with theoretical design equations.

The antenna designer must accept that theoretical design equations may be used to obtain a preliminary design that is **close** to the desired performance, but a subsequent round of simulation and/or bench tuning is also usually necessary to perfect the design.

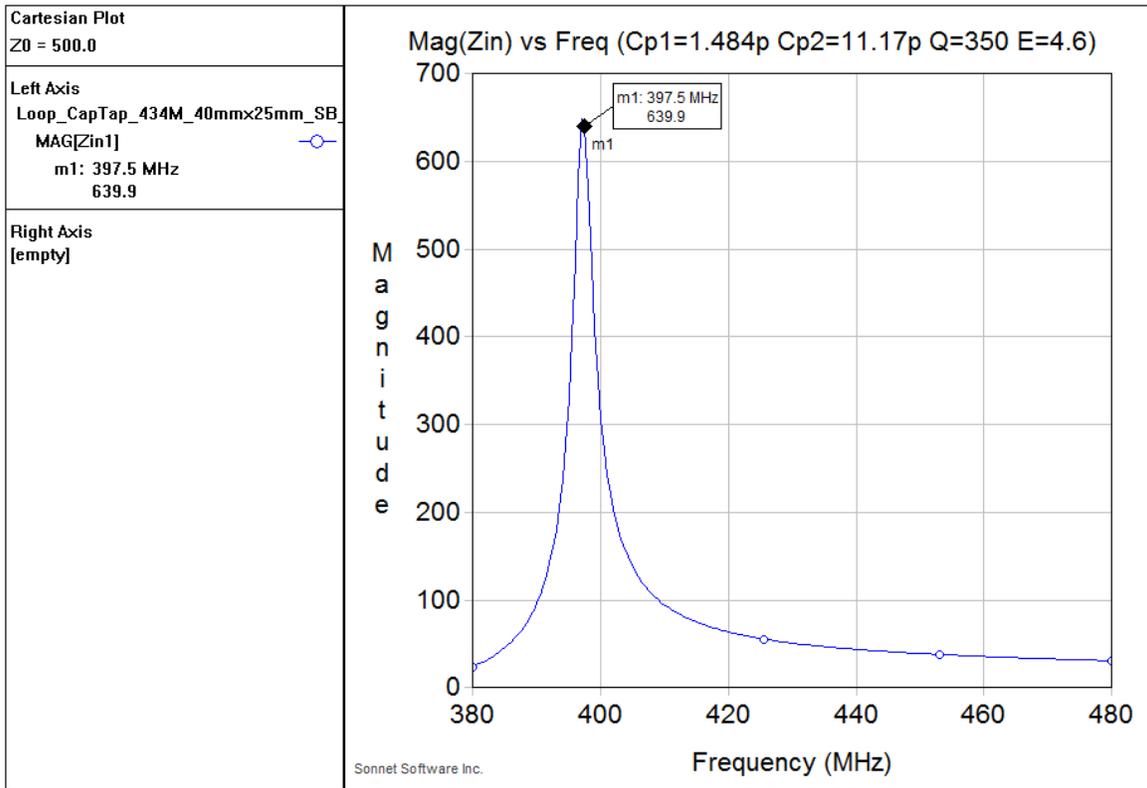


Figure 10. Loop Antenna Simulated Mag(Zin), Preliminary Design

A few iterations with the Sonnet simulator results in tuning of the loop antenna structure to both the desired operating frequency (434 MHz) as well as the target input impedance ($Z_{in} = 500 \Omega$). By iteration of simulation, the following tuning capacitor values were obtained:

- $C_{P1} = 1.17 \text{ pF}$
- $C_{P2} = 10.8 \text{ pF}$

The simulated $\text{Mag}(Z_{in})$ impedance response of the final design is shown in Figure 11. The series-resonant and parallel-resonant frequencies are clearly evident, as discussed in Figure 6.

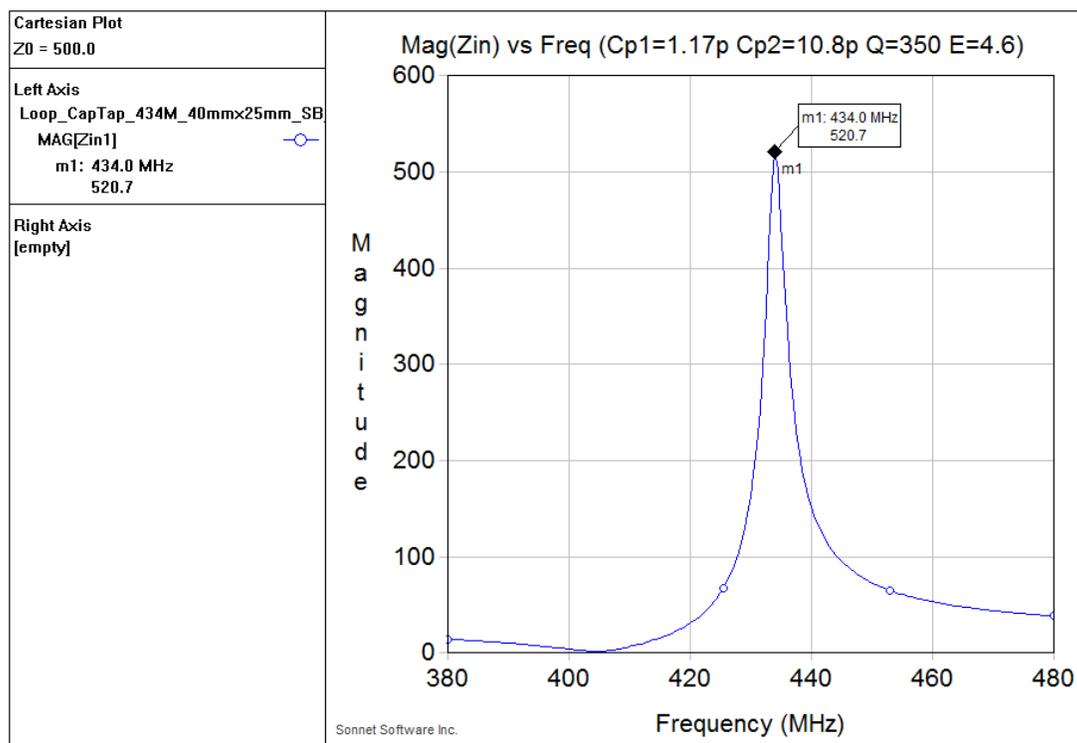


Figure 11. . Loop Antenna Simulated $\text{Mag}(Z_{in})$, Final Design

The results of this design example indicate that a typical keyfob differential loop antenna may operate with a very high L:C ratio; that is, a small value of capacitance resonates a large value of inductance. In the higher frequency bands (868 to 915 MHz), the required value of total capacitance (C_P) may be very small (less than 0.5 pF). With such small values of capacitance, the tuning of the antenna may become sensitive to component tolerance variations. To some extent, this effect may be reduced by adjusting the size of the antenna (i.e., value of antenna trace inductance). With a smaller loop antenna, higher values of capacitance are required to tune the antenna to resonance, thus reducing the sensitivity of the design to component tolerances. However, the radiation resistance (and thus antenna efficiency) drops as the size of the loop antenna is decreased, as shown by Equation 7. Thus frequency tuning range may need to be traded off against antenna efficiency and link range.

Inspection of Equation 23 and Equation 24 show that tuning the resonant frequency of the antenna is dominated by C_{P1} , while the transformed input impedance of the antenna is determined by the ratio of $C_{P2}:C_{P1}$. Insight into the tuning of both the resonant frequency and input impedance may be gained by sweeping the C_{P1} and C_{P2} capacitance values as parametric variables. In the plot of Figure 12, the tuning capacitance C_{P2} is varied; in the plot of Figure 13, the tuning capacitor C_{P1} is varied. From inspection of these two tuning curves, it is evident that the tuning of the loop antenna is affected in the following manner:

- An increase (decrease) in value of either capacitor value lowers (raises) the resonant frequency.
- Increasing (decreasing) the value of C_{P1} moderately raises (lowers) the input impedance.
- Increasing (decreasing) the value of C_{P2} significantly lowers (raises) the input impedance.

As the input terminals of the differential loop antenna are connected to the RFIC (i.e., TX output or LNA input), the logical component to be automatically adjusted by any tuning circuitry integrated within the chip (e.g. Si4010) is the C_{P2} capacitor. While adjustment of this capacitor is effective in tuning the resonant frequency of the loop, it has the

AN639

unfortunate side effect of also providing the greatest variation in input impedance. A more effective way of tuning the loop would be to vary the C_{P1} component value. However, this tuning approach turns out to be quite difficult. The voltage appearing across C_{P1} is quite large due to the effects of impedance transformation, and would prove difficult to control with conventional integrated devices (i.e., CMOS). Automated tuning of the C_{P1} tuning capacitor is currently not provided by the Si4010 chip.

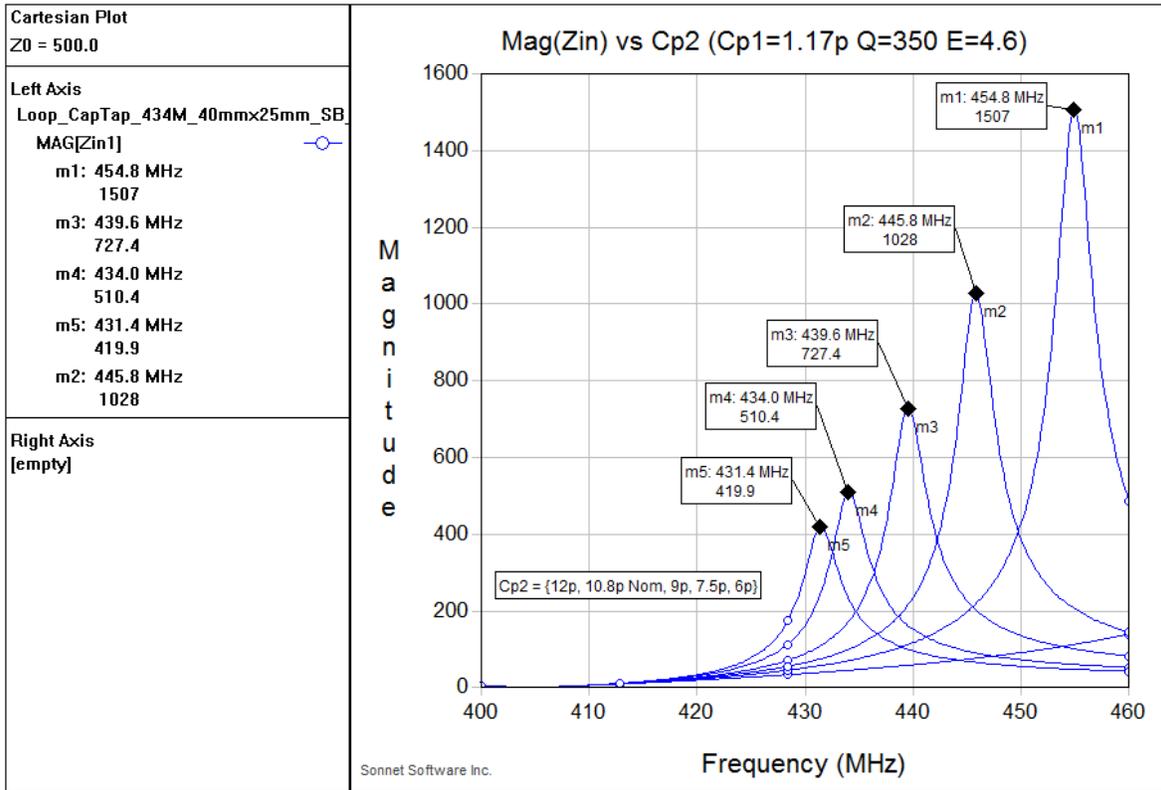


Figure 12. Loop Antenna Simulated Mag(Zin) vs. C_{P2}

5.3. Loop Antenna Gain Simulation Example

The radiation patterns and field strengths of the antenna design may also be simulated. This is useful for determining the radiation efficiency of each design. Memory limitations of the Sonnet simulator generally require simplification of the antenna model and limiting the waveguide box size to approximately $2\lambda \times 2\lambda$. This is usually large enough to get a reasonable estimate of the true far-field radiated performance. It is also sufficient for determining the relative performance of various antenna structures.

The spherical coordinate system used by Sonnet in their far-field viewer is shown in Figure 14. The board is assumed to lie in the X-Y plane, with the Z-dimension in the vertical direction (orthogonal to the plane of the PCB). The variable ' θ ' measures the angle relative to this vertical axis, and thus a value of $\theta = 0$ deg represents a vector perpendicular to the plane of the board, while a value of $\theta = +90$ deg or $\theta = -90$ deg lies in the plane of the board itself. The variable ' ϕ ' measures the angle relative to the horizontal bottom edge of the board geometry, as drawn in the previous antenna design examples. Thus a value of $\phi = 0$ deg represents a vector towards the right-hand edge of the geometry window (i.e., top of the loop antenna in the designs shown here), while a value of $\phi = +90$ deg represents a vector towards the upper edge of the geometry window. In such a coordinate system, the variable ' ϕ ' corresponds to azimuth while the variable ' θ ' corresponds to elevation.

One known limitation of the Sonnet simulator is that radiation patterns falling in the **exact** plane of the antenna structure itself (i.e., plane of the PCB) are not simulated accurately. The simulator tends to produce radiation patterns with nulls (zero radiated field strength) or discontinuously large values. The results for these values of θ ($\theta = \pm 90$ deg) should be ignored.

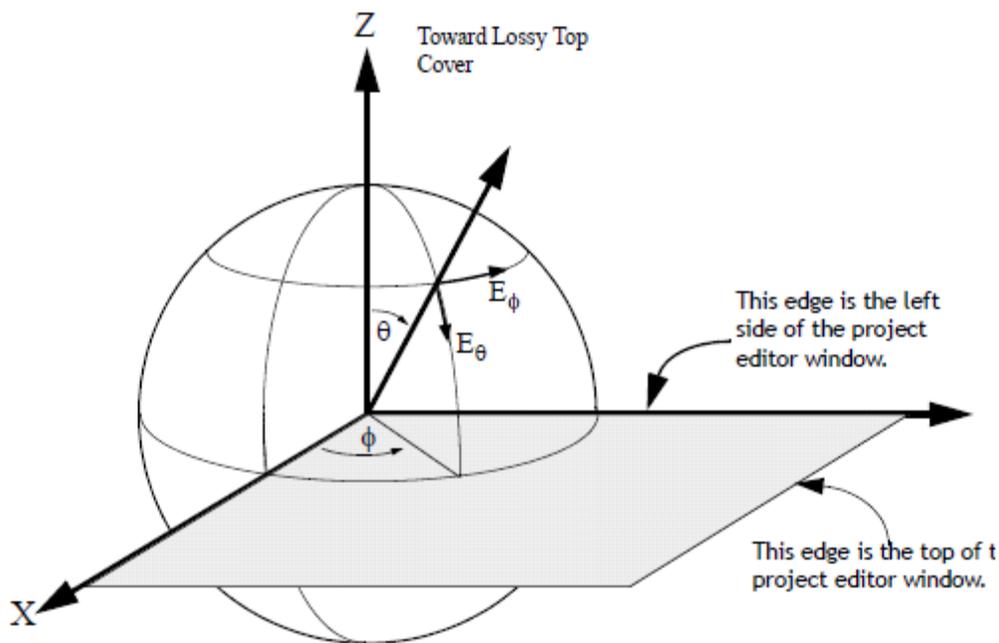


Figure 14. Spherical Coordinate System Used by Sonnet Far-Field Viewer

The Sonnet simulator is capable of calculating the individual polarization components (E_ϕ , E_θ) of the electric field. However, loop antennas are most often used in hand-held devices in which a constant direction of polarization is difficult to maintain. As a result, calculation of the total E-field vector (E_{TOTAL}) is a more useful metric in determining radiation efficiency. The calculated field strength is typically reported as a gain value (in dB), relative to the radiated field strength of a theoretical isotropic radiator.

The simulated radiated field strength of the capacitively-tapped loop antenna design of Figure 9 (40 mm x 25 mm) at 434 MHz is shown in Figure 15 below. This antenna model takes into account known loss factors (dielectric loss tangent, ohmic metal trace loss, and finite Q-factor of capacitors). The calculated gain (in dBi, or dB relative to a theoretical isotropic radiator) as a function of angle θ is plotted for certain selected values of ϕ . The maximum antenna gain is found to be approximately -9.7 dBi for an azimuth value of $\phi = 0$ deg. As discussed earlier, the “nulls” in the pattern for $\theta = \pm 90$ degrees are due to known simulation inaccuracies in the exact plane of the PCB, and should be ignored.

This simulated value of antenna gain of -9.7 dBi reasonably compares with the estimated value of -8.53 dBi calculated in Equation 20.

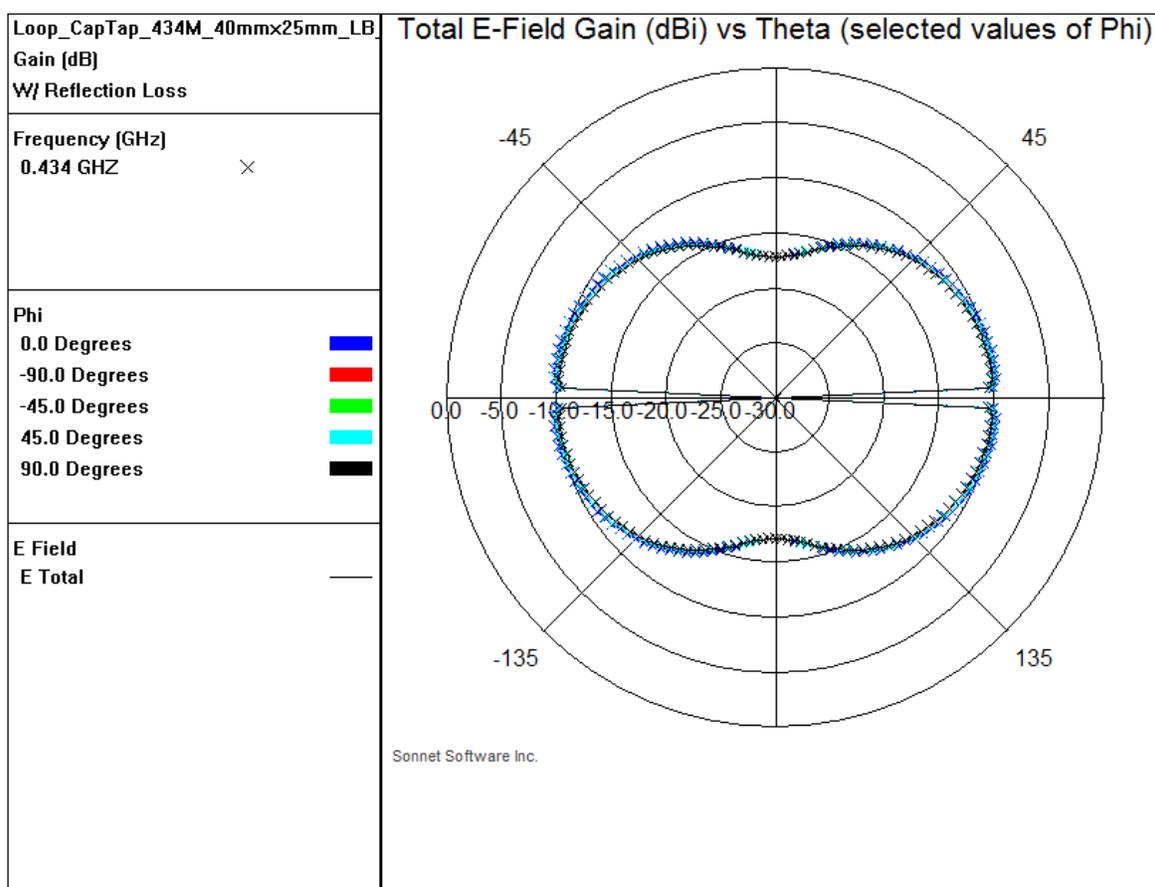


Figure 15. Simulated Loop Antenna Gain (dBi) vs. Theta (40 mm x 25 mm)

AN639

This plot should be interpreted as viewing the PCB “edge on” in the horizontal plane. Thus the E-field gain values for $-90 \text{ deg} < \theta < +90 \text{ deg}$ represent the portion of the radiation pattern lying above the plane of the board; the E-field gain values for $+90 \text{ deg} < \theta < +180 \text{ deg}$ and $-180 \text{ deg} < \theta < -90 \text{ deg}$ represent the portion of the radiation pattern lying below the plane of the board. Each selected value of ϕ represents a different angle or viewpoint from which to view the horizontal edge of the board (i.e., azimuth). Thus the radiation pattern of Figure 15 depicts an antenna that radiates optimally at an angle just slightly above the plane of the PCB, with a moderate dip in radiation intensity in a direction vertically perpendicular to the board.

It is also useful to plot the radiated field strength as a function of azimuth angle ϕ , for certain selected values of θ . This is illustrated in Figure 16. The maximum antenna gain is again found to be approximately -9.7 dBi for an elevation angle of $\theta = \pm 85 \text{ deg}$ (i.e., just above the plane of the PCB).

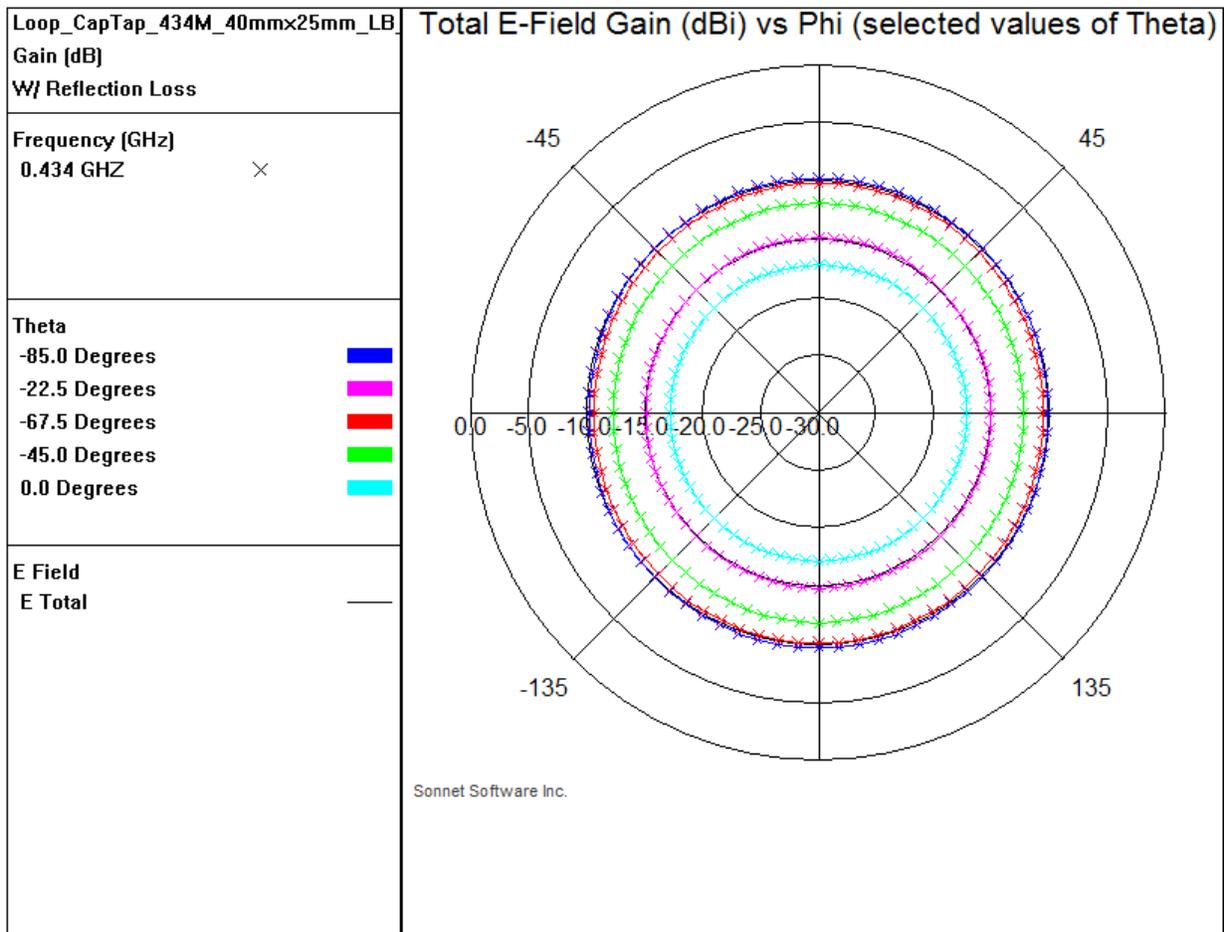


Figure 16. Simulated Loop Antenna Gain (dBi) vs. Phi (40 mm x 25 mm)

This plot should be interpreted as viewing the antenna pattern from a point in space located directly above the PCB, looking downwards towards the antenna structure. The E-field gain values as a function of ϕ thus represent the variation in radiated field strength around the perimeter of the board (i.e., for a change in azimuth). Each selected value of θ represents a different angle of elevation (relative to the vertical axis). Thus, the radiation pattern of Figure 16 depicts an antenna that radiates nearly equally in all directions of azimuth (i.e., is omni-directional), but varies somewhat with respect to elevation angle above or below the board.

5.4. Loop Antenna Gain vs. Size vs. Frequency

The design equations presented in Section 3 indicate that the radiation resistance increases with Area^2 and with Freq^4 . If the radiation resistance increases faster than other loss mechanisms (and this is usually the case), then the antenna efficiency should improve with larger loop area and at higher operating frequencies.

It is useful to develop a chart of expected antenna performance as a function of antenna size and operating frequency. This may be accomplished by evaluating the theoretical design equations for a variety of antenna designs; alternatively, a variety of antenna designs may be simulated using EM simulation software (such as Sonnet). The results from the latter approach (i.e., simulation) are shown in Figure 17, assuming a Q-factor of the tuning capacitor(s) of $Q = 350$. This chart may be used as a convenient reference guide to quickly predict the expected antenna performance for a given antenna size at a selected operating frequency.

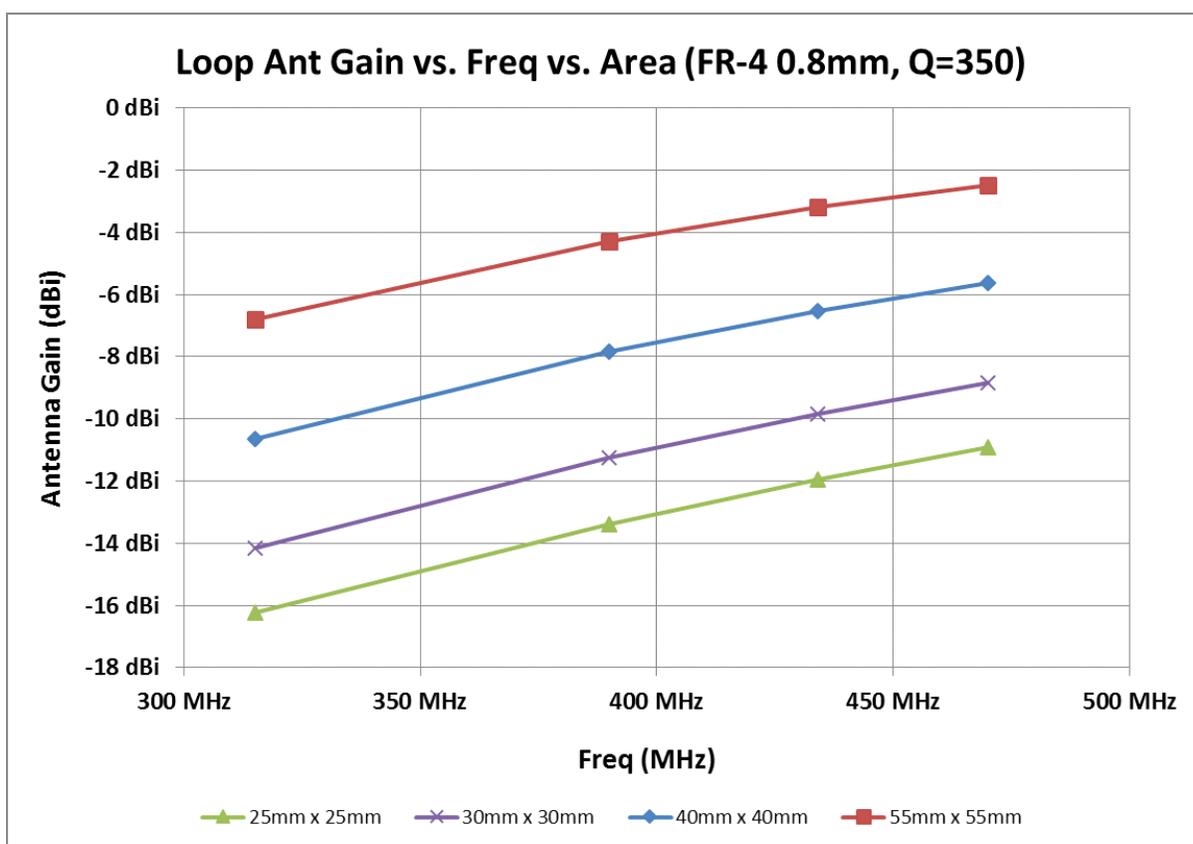


Figure 17. Simulated Loop Antenna Gain (dBi) vs. Frequency vs. Area

6. Practical Design Tips

6.1. DC Biasing to TXP/TXM Pins

The PA output devices within the Si4010 chip must obtain V_{DD} supply voltage through the TXP and TXM pins themselves; that is, there must be a DC path from the V_{DD} supply to the TXP/TXM pins. However, series tuning capacitor C_{P1} is physically placed in the center of the loop antenna trace and thus “breaks” the DC continuity through the antenna loop. V_{DD} supply voltage must therefore be supplied to the TXP/TXM output pins through a pair of large-value pull-up inductors, one for each of the two output pins. This DC biasing scheme is illustrated in Figure 18.

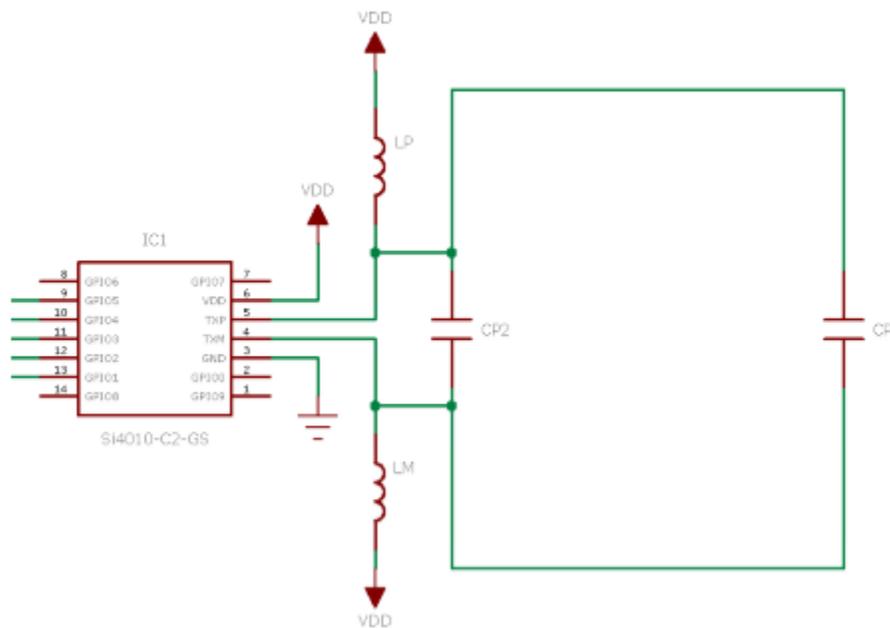


Figure 18. Example Schematic of DC Biasing Concept

The addition of two discrete inductors adds undesirable cost to the Bill of Materials (BOM). It is possible to design a loop antenna which contains a secondary (smaller) loop inside the main antenna loop. This smaller loop does not require a series tuning capacitor and thus provides a DC feed path to the TXP/TXM output pins of the Si4010 chip. The V_{DD} supply voltage may be fed to the center point of this smaller loop. The latest Si4010 Keyfob reference designs utilize such a dual-loop structure, see the reference design files for further details:

<https://www.silabs.com/documents/public/schematic-files/4010-KFOB-315.zip>

<https://www.silabs.com/documents/public/schematic-files/4010-KFOB-434.zip>

<https://www.silabs.com/documents/public/schematic-files/4010-KFOB-868.zip>

<https://www.silabs.com/documents/public/schematic-files/4010-KFOB-915.zip>

6.2. Fine Adjustment of C_{P1} Tuning Capacitor

The design example discussed within this application note resulted in a calculated value of $C_{P1} = 1.484$ pF (and later adjusted in simulation to $C_{P1} = 1.17$ pF). It is clear that as operating frequency increases, or as the loop antenna size is increased (in a desire to improve the radiation resistance), the value of capacitance required to resonate the loop drops to a very low value (less than 1 pF). At such high L:C ratios, the tuned frequency of the antenna changes rapidly with a small change in the value of C_{P1} . As a result, a non-standard value of capacitance (i.e., not falling on standard 2% or 5% tolerance values) may be required to perfectly tune the antenna to resonance at the desired frequency. In such a case, it may be advisable to implement C_{P1} as the combination of a standard value discrete capacitor, placed in parallel with a small printed finger capacitor. This printed finger capacitor may be used to “fine-tune” the total value of C_{P1} . An example of such a design is shown in Figure 19. This plot (zoomed in on only the portion of the antenna near C_{P1}) shows a small printed finger capacitor on one side of the board, while a discrete ceramic capacitor is connected in parallel on the opposite side of the board. As the Q-factor of a printed finger capacitor is much less ($Q \approx 60-70$) than a discrete ceramic capacitor, use of a printed finger capacitor for the entire value of C_{P1} is not usually recommended, regardless of its benefit in decreasing the BOM cost.

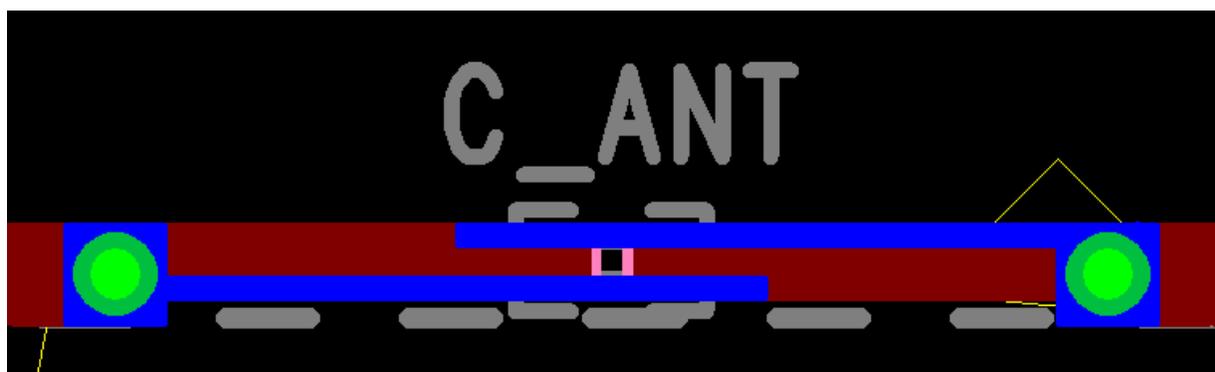
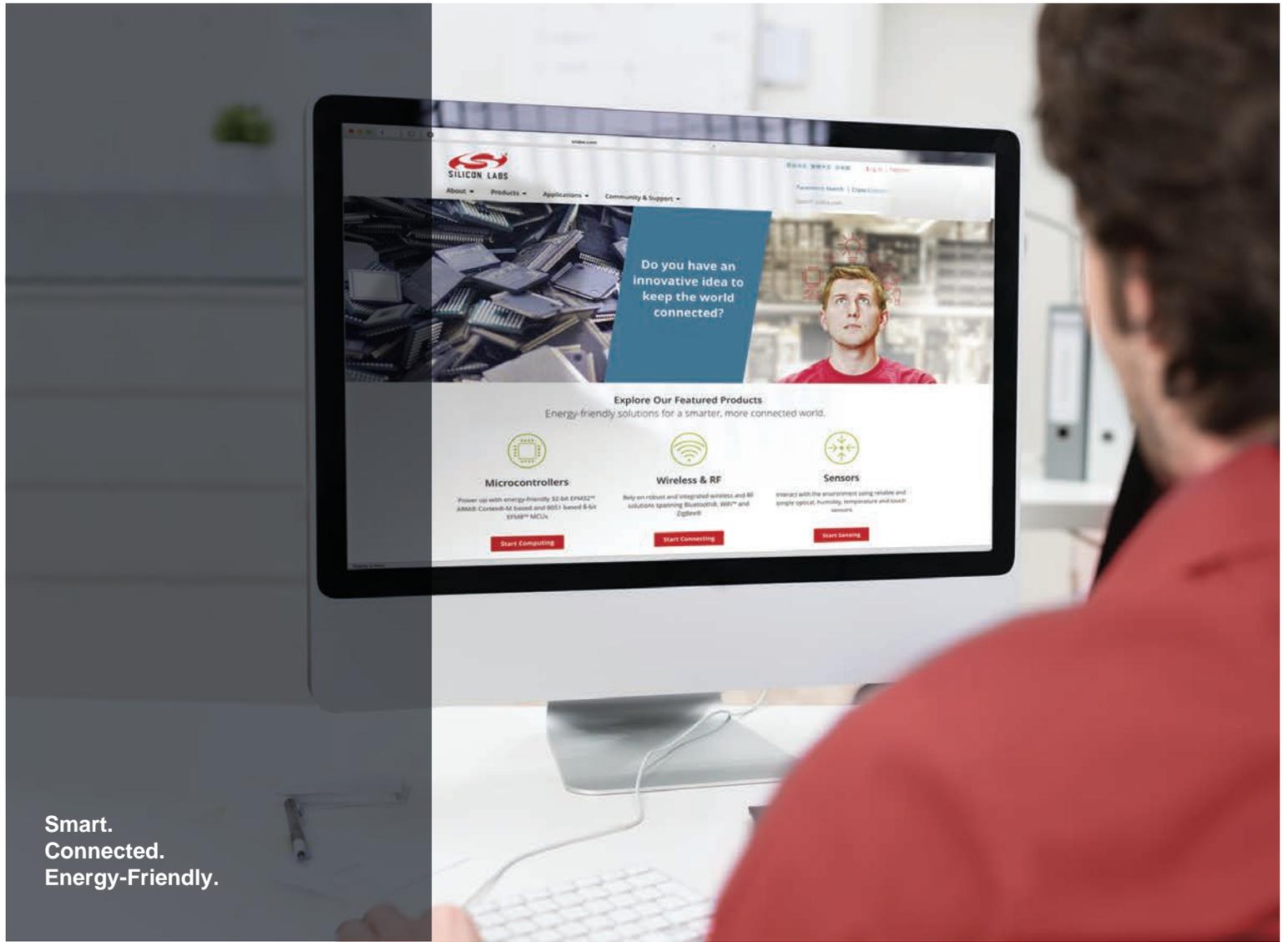


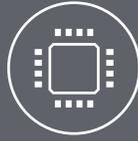
Figure 19. Example of Printed Finger Capacitor for Fine-Tuning of C_{P1}



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