Si4012 Antenna Interface and Matching Network Guide

1. Introduction

This document provides guidelines and design examples for the high impedance matching networks necessary for the proper usage of the Si4012 transmitter.

Section “2. High Impedance Differential Power Amplifier” gives a brief overview of the differential high impedance PA used in this chip. It also describes the method for determining the optimum termination impedance necessary to acquire the maximum power with the best efficiency.

Section “3. Matching Balun Design for Si4012 with 50 Ω Single-Ended Output” describes the design steps for the matching balun, which matches the high impedance differential outputs of the Si4012 chip to a 50 Ω single-ended termination or antenna such as monopole, spiral, ILA, etc.

Section “3.1. Matching Baluns for Si4012_B1” gives the matching network schematic and measured results. These sections are useful for readers who are not greatly interested in the theoretical development of the matching network but who are concerned with quickly obtaining a set of component values for a given desired frequency of operation.

Section “4. Design of High Q Discrete Matching Baluns” describes the design procedure and operation of the matching.

2. High Impedance Differential Power Amplifier

This section discusses the operation of the high impedance switched current power amplifier used in the Si4012 chips. In theory, the delivered power to the load is maximum if the RF generator is terminated by the complex conjugate of its generator impedance. However, it is true only if no constraints for voltage swing are given.

Operation of the high impedance PA is illustrated in Figure 1. High impedance PAs usually have open drain outputs and behave like an RF current generator. The TX generator impedance is represented by its parallel RC equivalent while the termination is represented by its parallel RL equivalent. The L_{AP} and C_{TX} work in high impedance parallel resonance at the operation frequency (the series bonding and leadframe inductances have some minor detuning effects, but those are neglected for the first investigation) and thus the voltage swing is determined by the residual equivalent resistance of the termination (R_{AP}) and the TX internal loss (EPR).

The drain voltage is limited by the CMOS technology. With a fixed current magnitude I_{RF}, if the generator impedance is too high, the voltage swing would exceed the limit with complex conjugate termination.

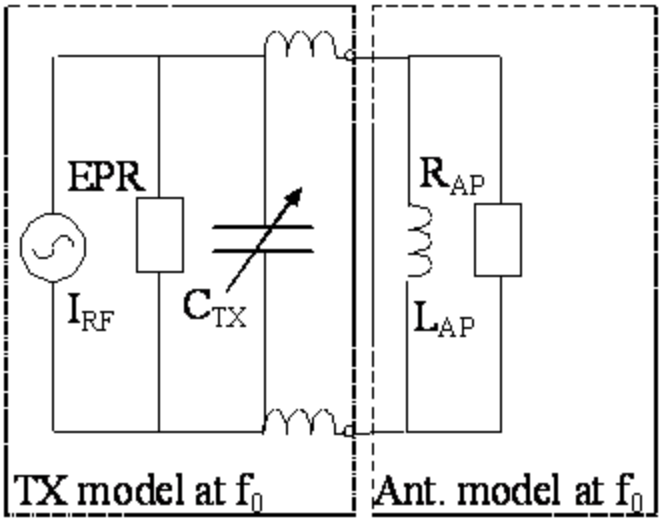


Figure 1. Operation of the High Impedance PA

In this case, lower termination impedance has to be used (i.e., R_{AP}<EPR) in order to keep the voltage swing below the allowed maximum. This lower termination impedance is called "the optimum termination impedance" which achieves the maximum allowed swing and thus the maximum power with the given current magnitude. This "voltage limited" operation type is advantageous as more than 50% of the RF current flows through the parallel connected lower impedance termination and less than 50% through the internal loss. In this way the efficiency is increased. It has to be noted that the achieved power is still lower than what would be possible with the same current, applying the complex conjugate termination. However, with conjugate match, the maximum voltage limit would be exceeded, which may cause damage of the driver transistors.

Assuming 3.5 V differential voltage magnitude (Vmax) and square wave current waveform (i.e., switched current), the optimum resulted parallel impedance (EPR x R_{AP}) is given by Equation 1:

$$Rlo = EPR \times \frac{R_{AP}}{EPR + R_{AP}} = \frac{Vmax}{\frac{4}{\pi} \times \frac{I_{RF}}{2}} = \frac{3.5\pi}{2I_{RF}} \cong \frac{5.5}{I_{RF}}$$

Equation 1.

The optimum parallel equivalent resistance of the termination can be derived from Equation 1 and is given by Equation 2:

$$R_{AP} = Rlo \times \frac{EPR}{EPR - Rlo}$$

Equation 2.

However, this calculation is valid only in the internal die drain points. Due to the series parasitic inductances (bond wire+leadframe+pcb), the allowed voltage swing and thus the optimum impedance is lower between the external TX pins. The typical total (two arms together) value of this series parasitic inductance is 1.3 nH for the applied MSOP package.

Table 1 provides the external optimum termination impedance, admittance, and the parallel RL equivalent for the testcards and MSOP packages at maximum power state operation. The optimum cap bank settings are also given.

The voltage limited operation mode is typical at the highest power settings (highest current) of the Si4012 chip, where the delivered power to the optimum differential termination is ~ +10 dBm.

A second important operation mode is when the current magnitude is reduced (e.g., to reduce the power) and thus the maximum allowed voltage swing is not achieved even if the conjugate complex termination is applied. In this case, the PA is "current limited". This is the typical case when the Si4012 chip works in a strongly reduced power state or when the internal capacitance bank state is high (close to maximum at low bands and above ~100 in high bands). In this operation mode the optimum termination is the complex conjugate.

A third, non-optimum mode is when the current is maximum, but the termination impedance is so low that the maximum swing is not achieved. In this case the termination is not the optimum, and the power and efficiency is lower than the possible maximum. All operation modes are covered and the parameters can be calculated easily by the 401x calculator, e.g., the parallel equivalent of the optimum termination can be found in the “Antenna Target” fields. More details about this calculator can be found in application note, “AN547: Si4010 Calculator Spreadsheet Usage”.

Table 1. Si4012 Maximum Power Operation

Freq [MHz] MSOP	Opt. load imp. [Ω]	Opt. load adm. [mSie]	Parallel Eqv. R_{AP} [Ω]	Parallel Eqv. L_{AP} [nH]	Cap. bank state & TX equivalent capacitance	Power to the differential load [dBm]
315	27+j114	1.98-j8.3	505	60.8	105, 4.2 pF	10.7
434	32.3+j124	19.7-j7.6	508	48.5	23, 2.77 pF	10.6
868	8.3+j66	1.88-j14.9	532	12.3	13, 2.73 pF	9.8
915	7.3+j62	1.87-j15.9	535	11	13, 2.76 pF	9.7

3. Matching Balun Design for Si4012 with 50 Ω Single-Ended Output

The Si4012 transmitter can be used with single-ended 50 Ω antennas (monopole, spiral, ILA, IFA, etc.,) as well if an external matching balun is used between the high impedance differential output of the chip and the 50 Ω single-ended load. The matching balun performs three important tasks with minimal insertion loss:

- Provides the optimum termination impedance (see Section “2. High Impedance Differential Power Amplifier”) to the differential output of the chip if the single-ended port of the balun is terminated by 50 Ω. At high power states the differential output is usually not terminated in the complex conjugate way. (See the "voltage limited" operation mode in Section “2. High Impedance Differential Power Amplifier”. In this case, the S11 parameter will not provide good return loss at the 50 Ω port, but the matching will provide the highest possible power.)
- Makes the balun function, i.e. adds the two differential outputs in-phase, with equal magnitudes.
- Makes suppression on the 2nd harmonic by using a 2nd harmonic trap.

Unfortunately, as the Si4012 outputs are working with the termination (here, the differential port of the balun) with high Q parallel resonance, optimum wideband solution is very difficult or even impossible to design.

If the power requirement is significantly relaxed, a possible wideband solution is to use a coil-type balun. In this case, however, the termination impedance is far from optimum and the power is lower (i.e, this is a compromise).

In this application note, narrowband, nearly optimum matching baluns are described, which use 0402SMD elements with different element values at the different bands.

In the design the losses and parasitic of the SMD elements and the pcb traces are compensated, and due to this it is strongly recommended to use the pcb layout proposed by Silicon Labs.

Also to comply with regulatory standards (ETSI, FCC, etc.), additional 3rd order filtering is necessary at the single-ended side. The proposed balun circuits comprise these filter sections.

3.1. Matching Baluns for Si4012_B1

This section is useful for readers who do not intend to deeply understand the fundamental operation of the high Q matching balun, but rather are concerned with quickly obtaining a set of component values for a given desired frequency of operation.

The presented baluns shows nearly the optimum impedances listed in Table 1 for the Si4012 outputs if the single-ended port is terminated by 50 Ω.

Also, in the balun function the magnitude mismatch is lower than 6% (typically 2-3%) and the phase error is lower than 5 degrees (typically 2 degrees). Fortunately, these levels of residual losses have minimal effect (~0.1 dB) on the operation of the matching balun. The main sources of these mismatches are the discrete steps of the available SMD components.

In the design, the losses and parasitic of the SMD elements and the pcb traces are compensated. For this reason, it is strongly recommended to use the pcb layout designs proposed by Silicon Labs around the Si4012 outputs, V_{DD}, grounding, etc.

The loss of the matching core is ~0.5 dB typically. The filters introduce 0.3–0.5 dB additional loss at the operation frequency. These loss values are achieved by using high Q wirewound inductor (Coicraft 0402HP series) and capacitor (Murata GRM155 series) types. Usage of lower Q elements (e.g., multilayer inductors) can cause 0.5–1 dB additional loss.

The presented baluns comply with regulatory standards, and for this they comprise the filters at their 50 Ω side.

The schematic of the balun with MSOP packaged Si4012 is shown in Figure 2. The element values are given in Table 2.

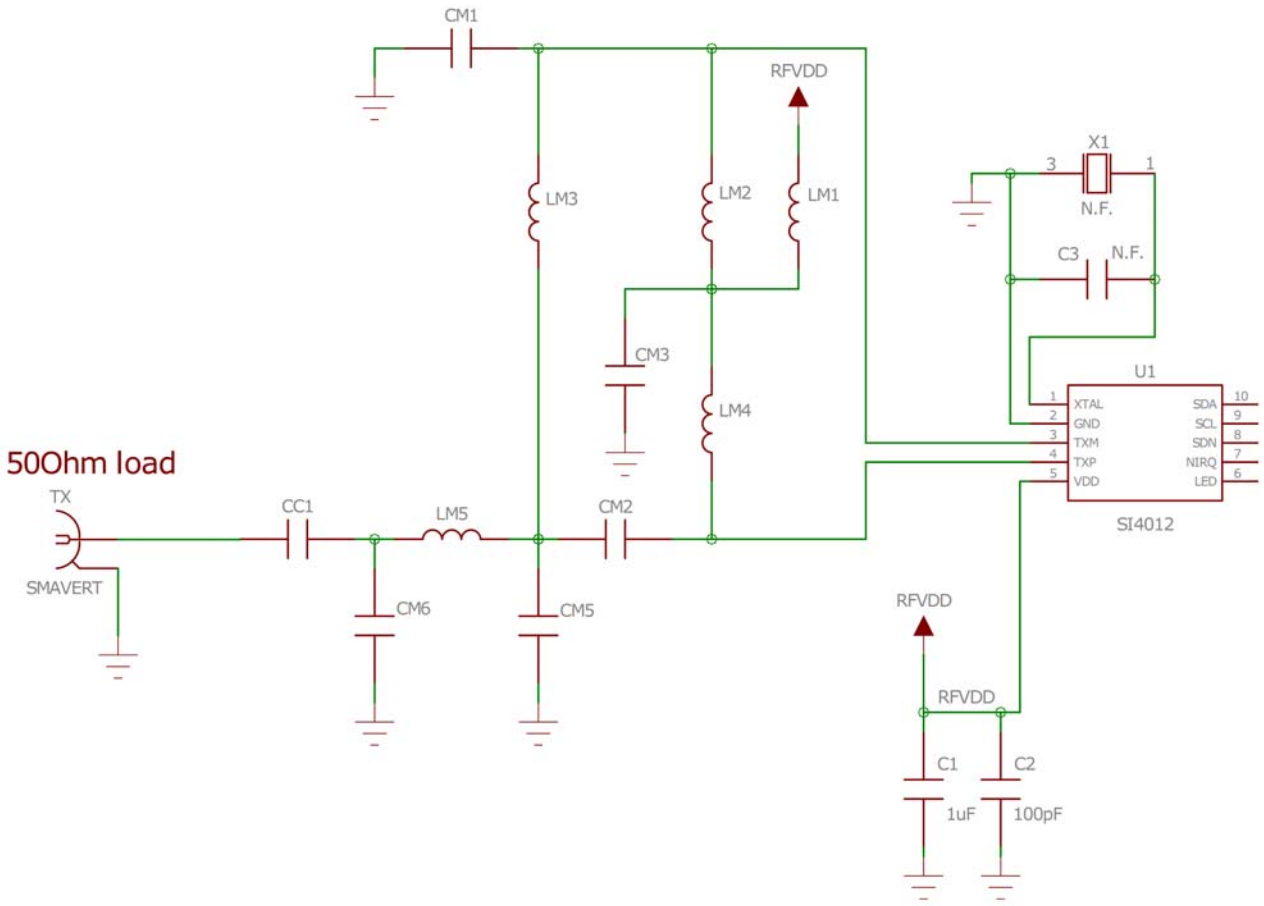


Figure 2. Si4012 Matching Network Schematic

Table 2. Matching Element Values for Si4012

Si4012	LM1	CM3	LM2	LM4	CM1	CM2	LM3	LM5	CM5	CM6	CC1
315M	220 nH	4.7 pF	20 nH	20 nH	5.6 pF	3 pF	120 nH	25 nH	8.2 pF	8.2 pF	390 pF
434M	220 nH	2.7 pF	16 nH	16 nH	4.3 pF	1.8 pF	56 nH	18 nH	6.8 pF	6.8pF	270 pF
868M	120 nH	2.4 pF	3.6 nH	3.6 nH	2.4 pF	1.2 pF	30 nH	6.8 nH	5.1 pF	5.1 pF	68 pF
915M	120 nH	2.4 pF	3.3 nH	2.7 nH	2 pF	1 pF	24 nH	6.2 nH	5.1 pF	5.1 pF	56 pF

The top layer of the Silicon Labs testcard is shown in Figure 3. It is recommended to copy and use the RF layout around the chip as it is. The gerbers of the board can be found on the Silicon Labs website: www.silabs.com.

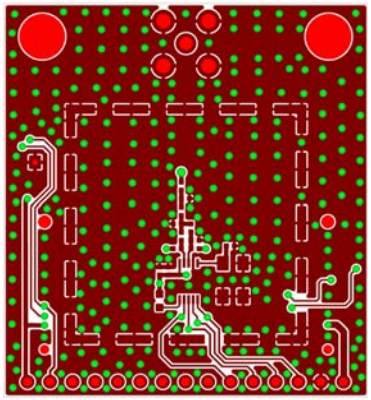


Figure 3. Top Layout of the SI Testcard with Si4012

The measured conducted spectrum of the 315, 434, 868, and 915 MHz testcard up to 3.6 GHz is shown in Figures 4, 5, 6, and 7, respectively. The realized matchings have ETSI compliance at 434 and 868 MHz and FCC compliance at 315, 434, and 915 MHz with properly reduced power in this conductive measurement. Assuming 0 dB gain antenna, the compliance is reserved in radiated measurements as well.

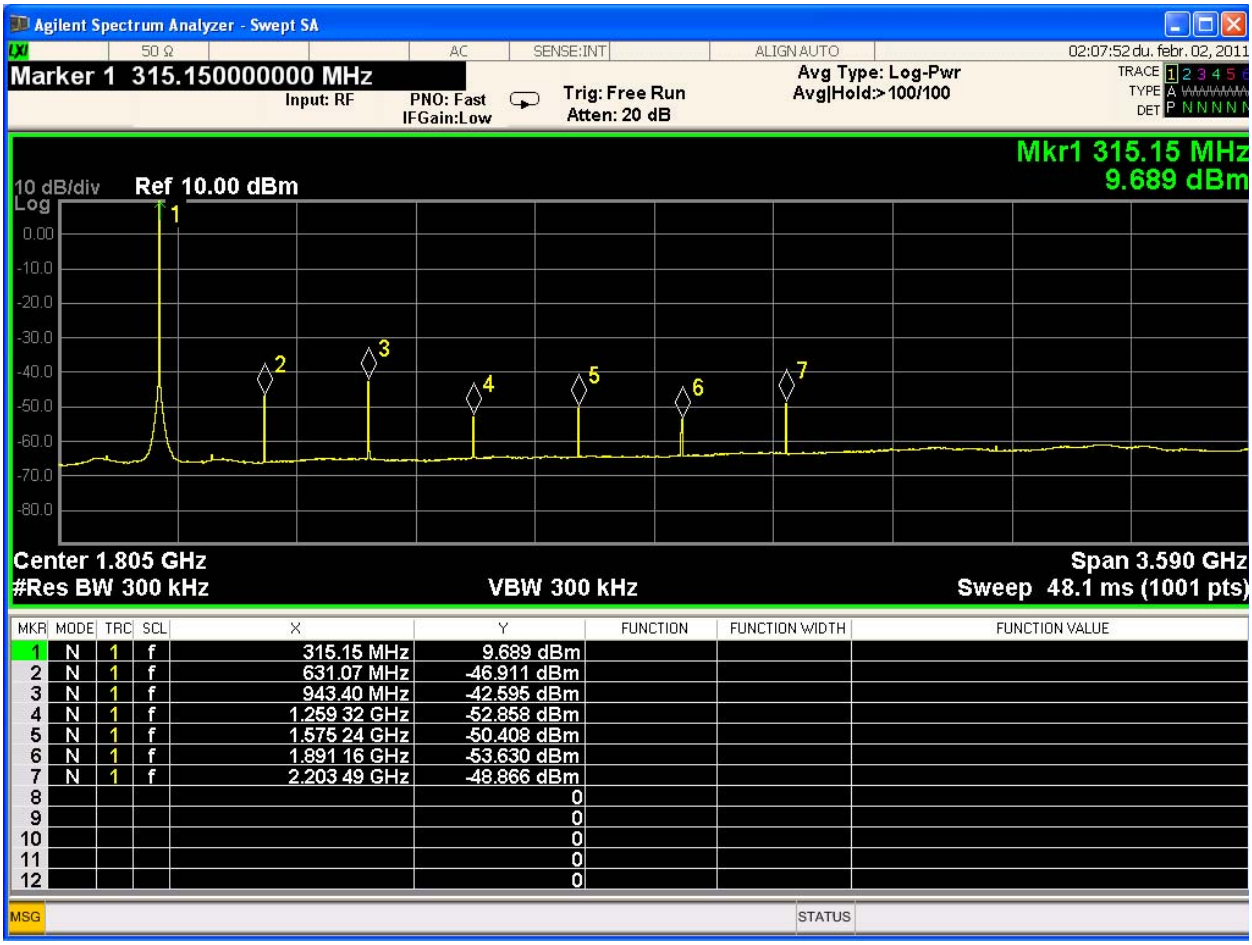
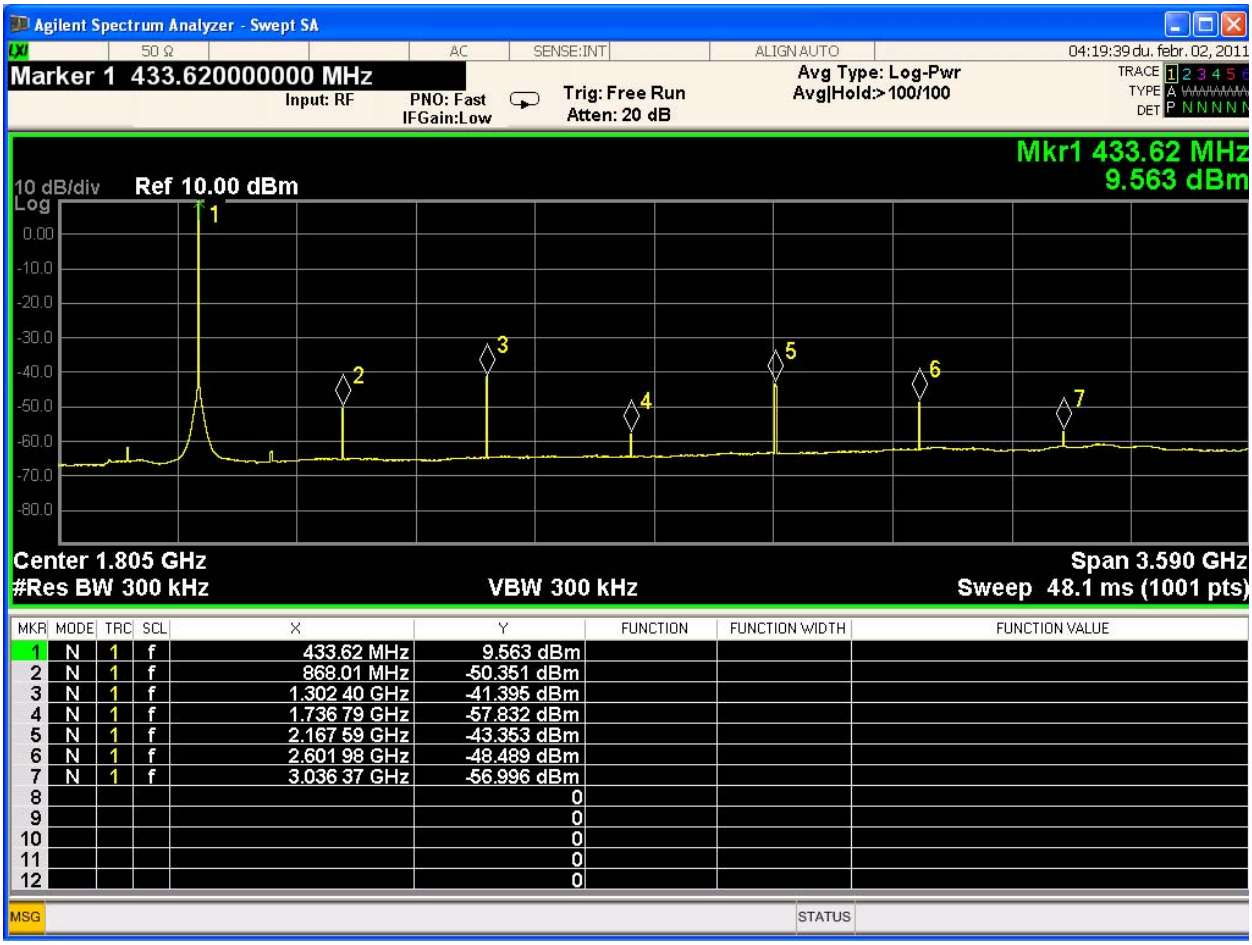


Figure 4. Measured Spectrum of the 315 MHz Si4012 Card Up to 3.6 GHz



MKR	MODE	TRC	SCL	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	1	f	433.62 MHz	9.563 dBm			
2	N	1	f	868.01 MHz	-50.351 dBm			
3	N	1	f	1.302 40 GHz	-41.395 dBm			
4	N	1	f	1.736 79 GHz	-57.832 dBm			
5	N	1	f	2.167 59 GHz	-43.353 dBm			
6	N	1	f	2.601 98 GHz	-48.489 dBm			
7	N	1	f	3.036 37 GHz	-56.996 dBm			
8					0			
9					0			
10					0			
11					0			
12					0			

Figure 5. Measured Output Spectrum of the 434 MHz Si4012 Card up to 3.6 GHz

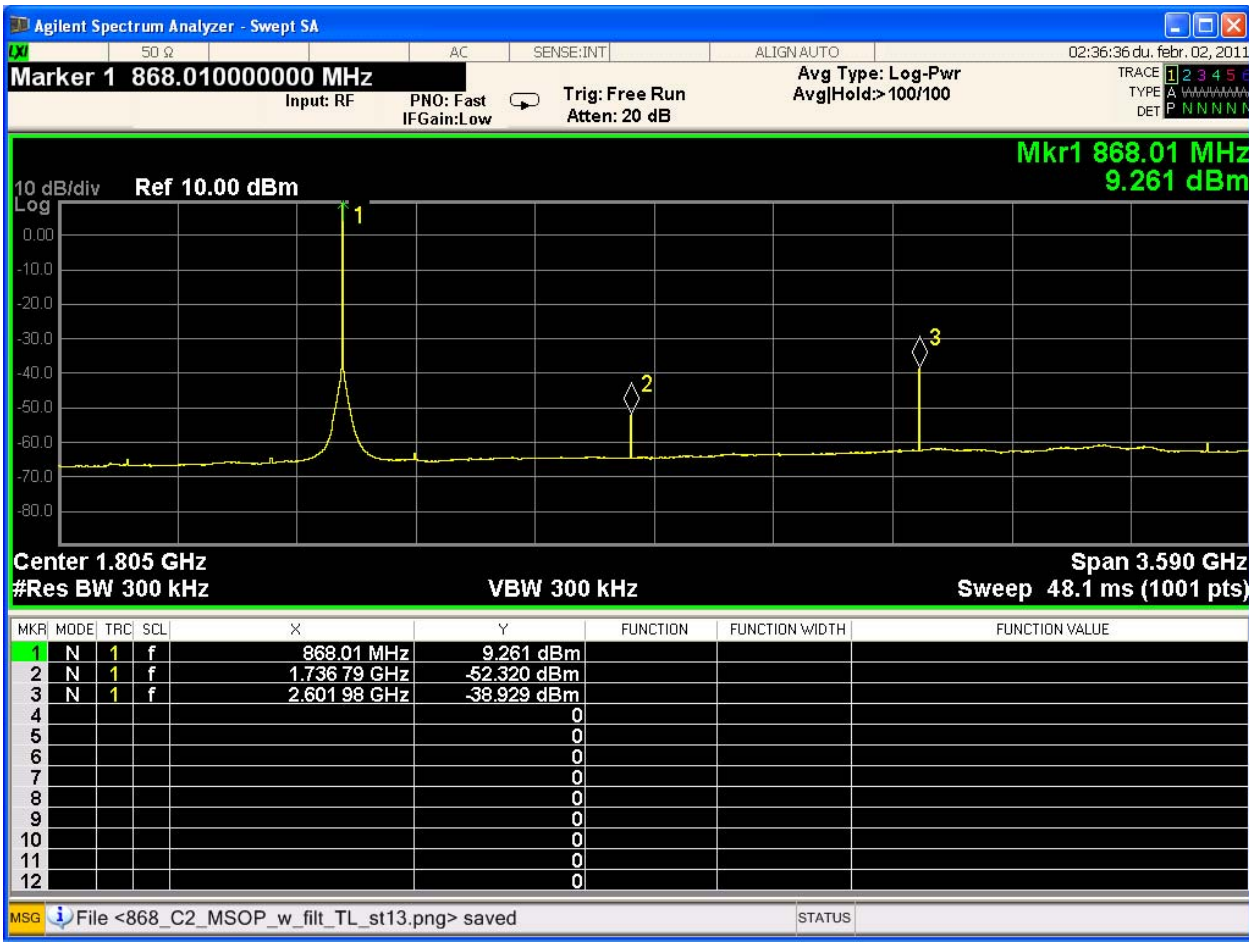


Figure 6. Measured Output Spectrum of the 868 MHz Si4012 Card Up to 3.6 GHz

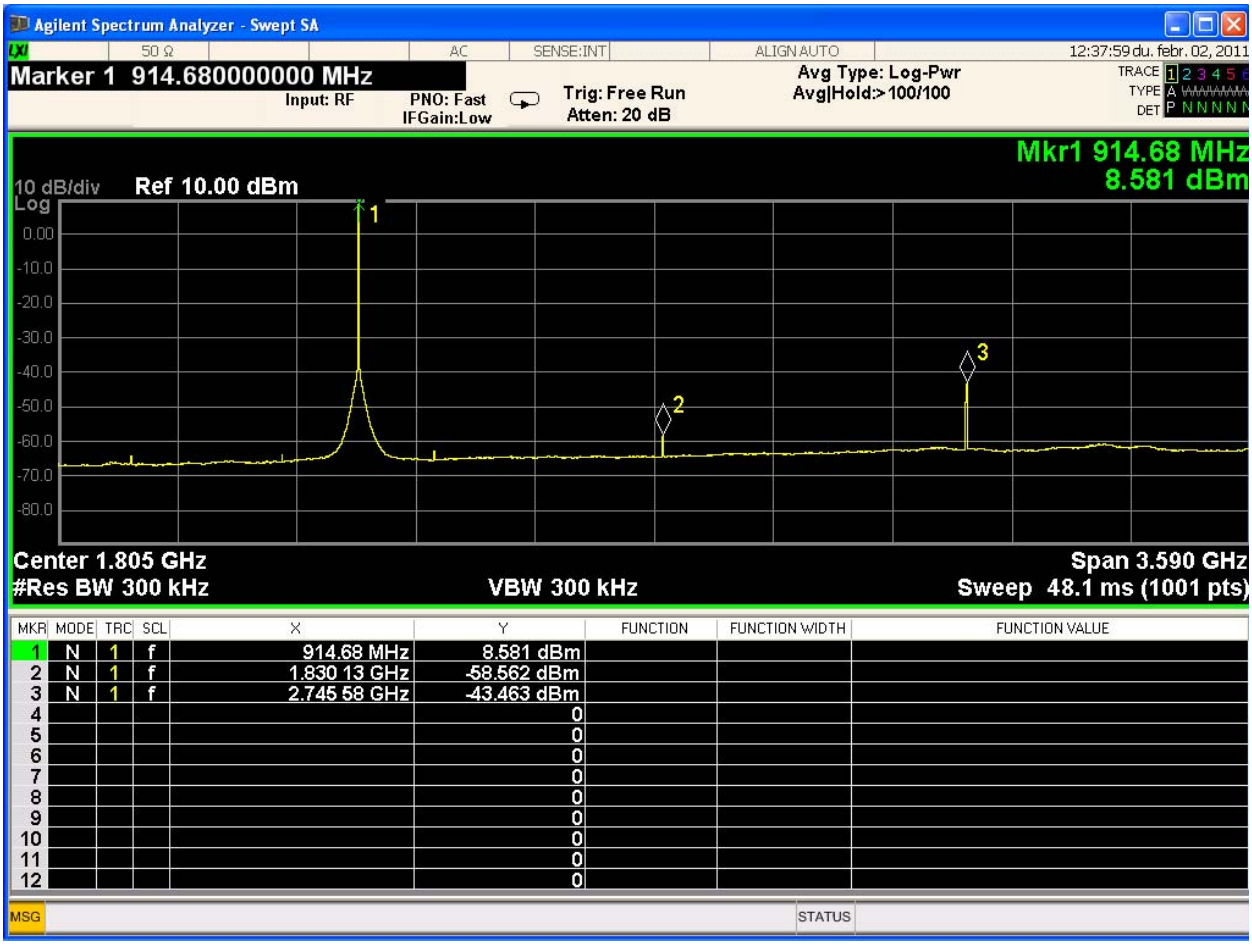


Figure 7. Measured Output Spectrum of the 915 MHz Si4012 Card Up to 3.6 GHz

4. Design of High Q Discrete Matching Baluns

This section is useful for readers who intend to understand the fundamental operation of the high Q discrete matching baluns.

The designed baluns show nearly the optimum impedances listed in Table 1 for the Si4012 outputs if the single-ended port is terminated by 50 Ω.

As mentioned previously, the two main tasks the matching balun performs with minimal insertion loss are:

- Shows the optimum termination impedance (see Section “2. High Impedance Differential Power Amplifier”) to the differential output of the chip if the single-ended port of the balun is terminated by 50 Ω.
- Makes the balun function, i.e., adds the two differential outputs in-phase, with equal magnitudes.

The matching balun also has an additional function to trap and remove the 2nd harmonic.

These functions can be satisfied with optimum solution in narrowband only. This section shows the design guidelines of narrowband discrete baluns.

4.1. Design Procedure

The basic structure which theoretically satisfies the two main matching balun functions has four external elements as shown in Figure 8. C_TX in the figure is the same equivalent capacitance which is denoted by C_{TX} in Figure 1 on page 2.

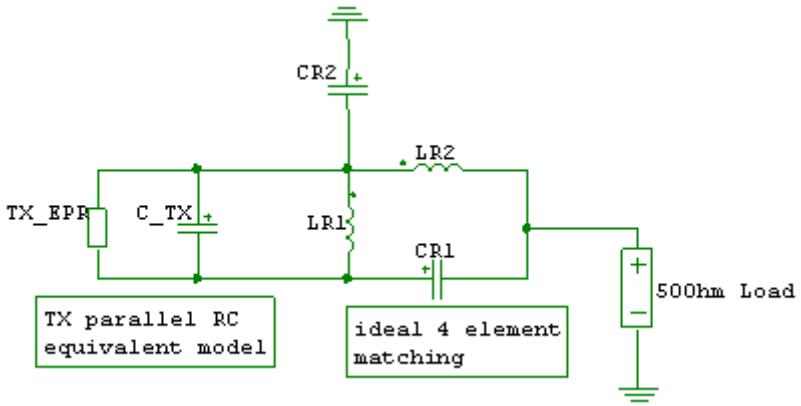


Figure 8. 4-Element Matching Circuit Schematic

In an ideal, loss-free scenario, the element values of the 4-element matching can be derived analytically. A detailed discussion of this analytical solution can be found in Silicon Labs application note, “AN427: EZRadioPRO Si433x & Si443x RX LNA Matching.” Although that solution applies to the results for a high impedance Rx matching with parasitic capacitance, the method is applicable to high impedance transmitters as well. The only difference in the formulas is that the parallel equivalent resistance of the optimum termination impedance (R_{AP} in Table 1 in Section “2. High Impedance Differential Power Amplifier”) and the transmitter equivalent capacitance (C_TX in Figure 8, which is also given in the 6th column of Table 1) have to be used.

As a result, the following equations are introduced here without proof or further discussion:

$$L_{R2} = \frac{\sqrt{50\Omega \times R_{PA}}}{\omega_{RF}}$$

Equation 3.

$$C_{R1} = \frac{1}{\omega_{RF}^{2} \times L_{R2}}$$

Equation 4.

$$C_{R2} = 2 \times C_{R1}$$

Equation 5.

$$L_{PA} = \frac{1}{\omega_{RF^2} \times C_{TX}}$$

Equation 6.

$$L_M = 2 \times L_{R2}$$

Equation 7.

$$L_{R1} = \frac{L_{PA} \times L_M}{L_{PA} + L_M}$$

Equation 8.

Using these equations as a starting point, the matching design methodology is the following:

1. Calculate the values, e.g., for the 434 MHz case where R_{AP}=508 Ω and the CTX=2.77 pF at internal cap. bank state of 23 (Table 1 in Section “2. High Impedance Differential Power Amplifier”). The ideal matching element values are: LR1=34.4 nH, CR1=2 pF, LR2=69 nH, CR2=3.9 pF.

Note: 3 nH was added for the two through-hole via inductances and LR1 was reduced accordingly.

2. Split LR1 into two halves to make a connection for the Vdd supply choke inductor and the 2nd harmonic trap capacitor. The schematic of the matching with split LR1 (LR11 & LR12) and with choke inductor is shown in Figure 9.

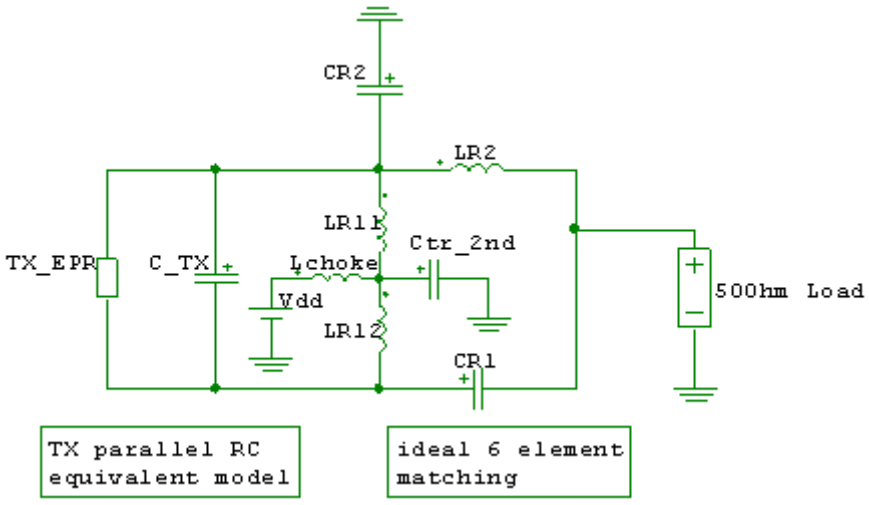


Figure 9. 6-Element Matching Circuit Schematic

The value of LCHOKE should be chosen such that it provides high impedance not only at the fundamental operating frequency but also at the first few harmonic frequencies as well. The inductance value should not be so large as to already be at (or past) parallel self-resonance at the desired operating frequency. The exact inductance value is not critical; however, Silicon Labs recommends the following range of inductance values (assuming 0402-size or 0603-size inductors) as a function of the desired operating frequency:

- 315 and 434 MHz: approximately 220–270 nH
- 868 and 915 MHz: approximately 120 nH

The value of the 2nd harmonic trap capacitor (Ctr_2nd) is chosen such that it is resonating in series with LR11 and LR12 at the 2nd harmonic frequency. As LR11 and LR12 are parallel connected for the common mode 2nd harmonic, the resulting inductance for the 2nd harmonic is LR11/2=LR12/2=LR1/4. This has to be in resonance with Ctr_2nd at the 2nd harmonic. However, the exact values are strongly influenced by the parasitic and unwanted couplings, thus it is always tuned at the bench.

3. The parasitics and losses of the SMD components and the pcb are included into a simulation where the above-listed main balun functions can be checked. Going back to the 434 MHz example, Figures 10 and 11 show the simulated S11 and the balun function (voltage transfer function from the 50 Ω single-ended port to the two differential ports) when the R_{AP} and C_{TX} (Table 1) are used as a differential port termination. As shown in these figures, the differential port of the balun is terminated by the conjugate of the optimum termination impedance (i.e., with the parallel connected R_{AP} and C_{TX}), both its balun function and matching are very good.
4. The balun function is checked when the R_{AP} is replaced by the much higher EPR, i.e., the internal loss of the TX (TX_EPR). That curve is shown in Figure 12 assuming 20K EPR at cap. bank state 23. The balun function remained good, only the voltage magnitude increased in the same way at both differential nodes. The S11 becomes bad (Figure 13), but as described in Section “2. High Impedance Differential Power Amplifier”, this is normal in "voltage limited" mode where the complex conjugate termination is not used for achieving the maximum power.

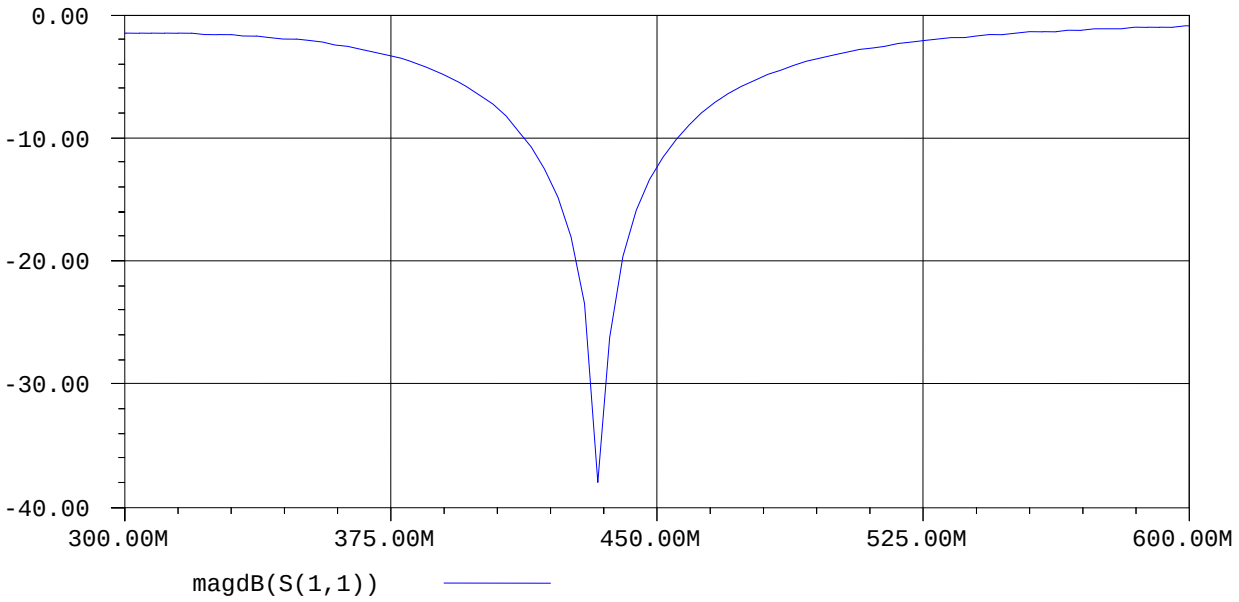


Figure 10. Simulated S11 of the 434M Si4012 Example

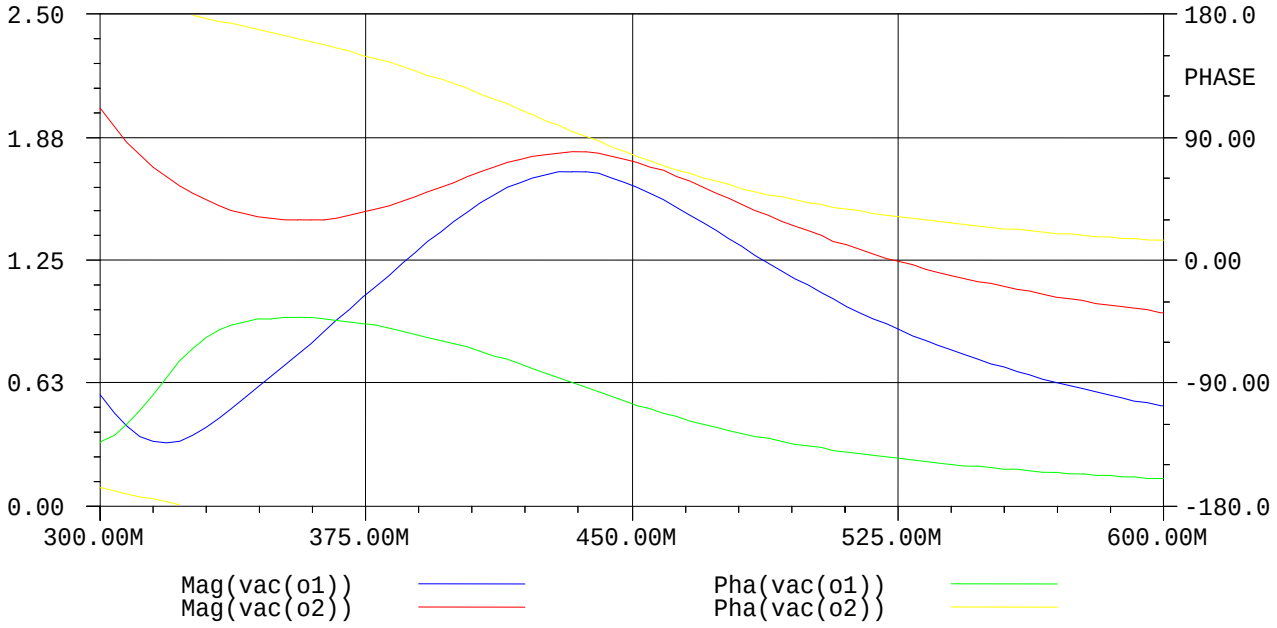


Figure 11. Voltage Transfer Function

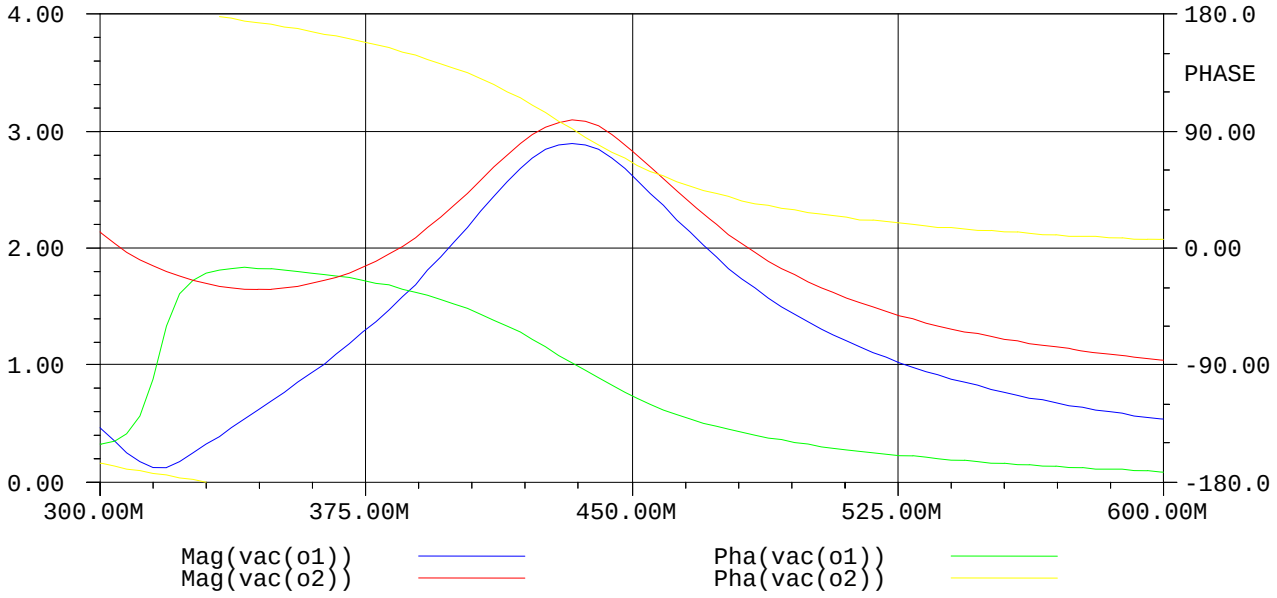


Figure 12. Voltage Transfer Function with Higher EPR

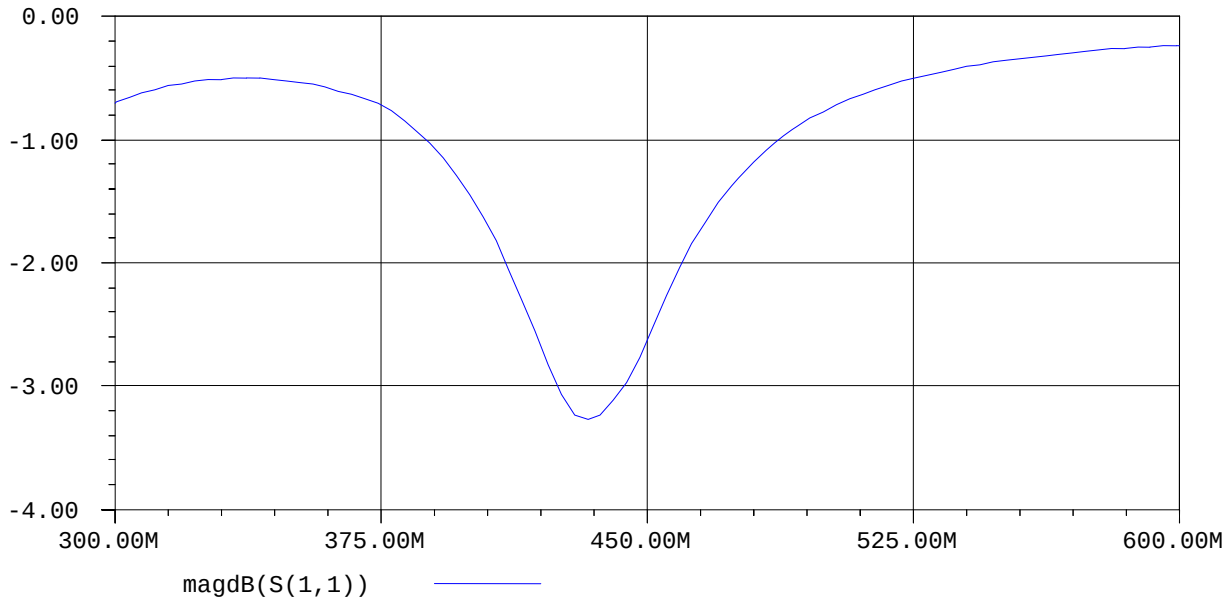
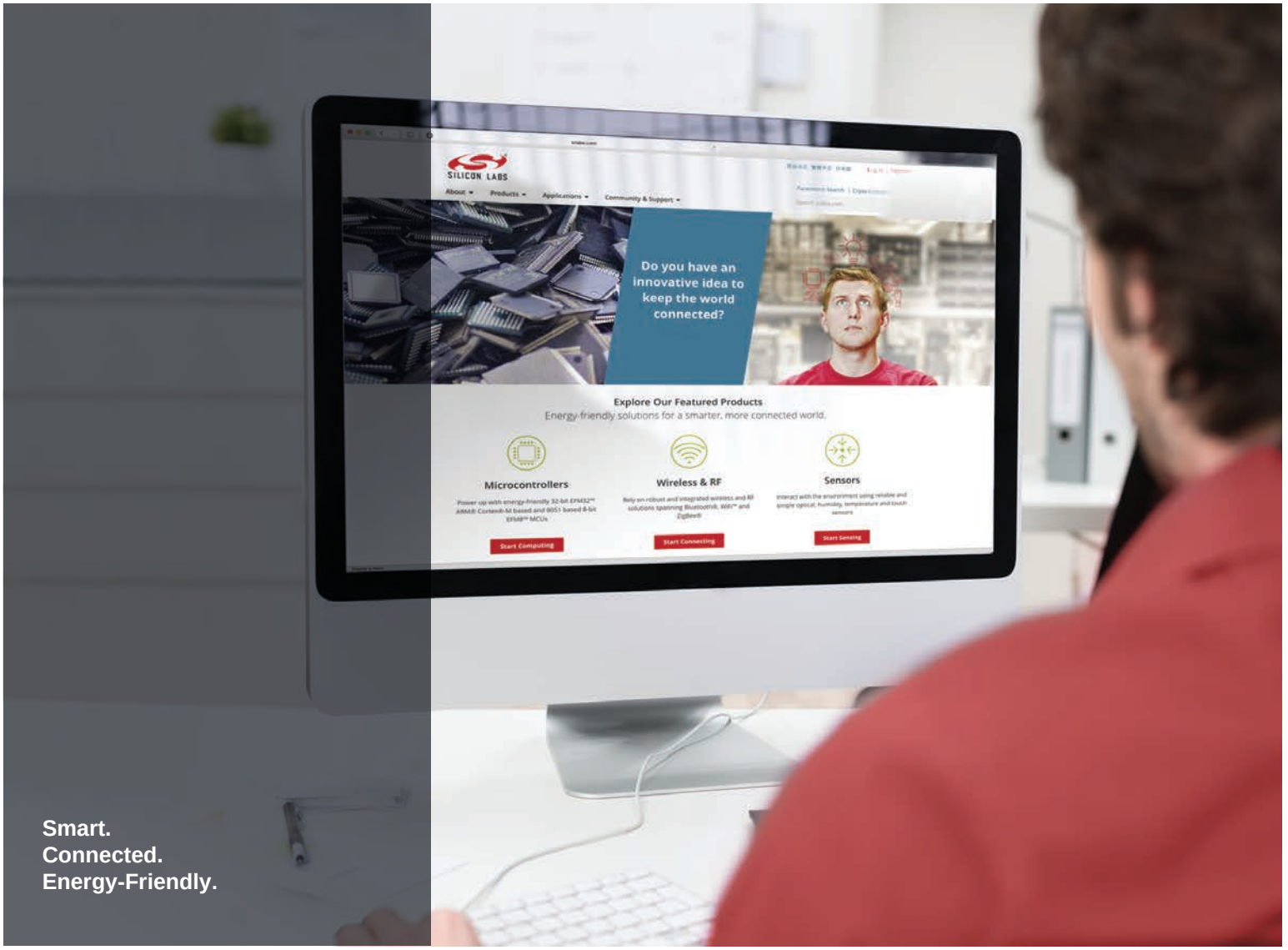


Figure 13. S11 with Higher EPR



Products
www.silabs.com/products

Quality
www.silabs.com/quality

Support and Community
community.silabs.com

SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com