

UPGRADING FROM THE Si7005 TO THE Si7015

1. Introduction

The Si7015 digital relative humidity and temperature sensor is a pin-for-pin and register-compatible upgrade for the Si7005. The Si7015 fixes the I²C “Acknowledge” issue of the Si7005 (meaning it can share an I²C bus with other devices that have different addresses without being shut down) and offers several other performance improvements, most notably:

- Operation to 1.9 V_{DD}
- Faster conversion time
- Lower V_{DD} current in operation
- Much lower V_{DD} current when in standby mode ($\overline{\text{CS}}$ high)

This application note covers some detailed considerations for migrating from the Si7005 to the Si7015.

2. Hardware

- The package dimensions and pin-out are identical; no changes are required to the PCB layout for the 4x4 QFN package.
- The bypass capacitor that supports the Si7005's on-chip linear regulator, C1 in Figure 1, is no longer required, but it can be left in place if desired.
- The SDA and SCL pins of the Si7015 may not be driven to voltages above V_{DD}. Switching V_{DD} low was possible with the Si7005, as shown in Figure 1. With the Si7015, switching V_{DD} low with SDA SCL high is not possible, so it should be connected as shown in Figure 2. Because the Si7015's standby power consumption is exceptionally low, it is not necessary to switch V_{DD} off to save power.

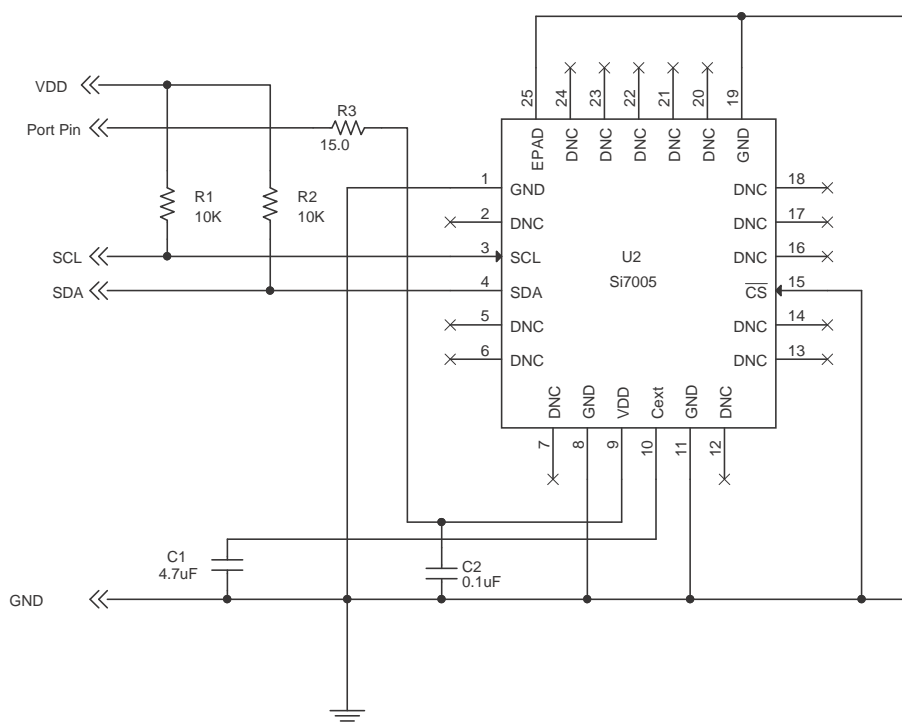


Figure 1. Typical Si7005 Application Circuit for Battery-Powered Applications

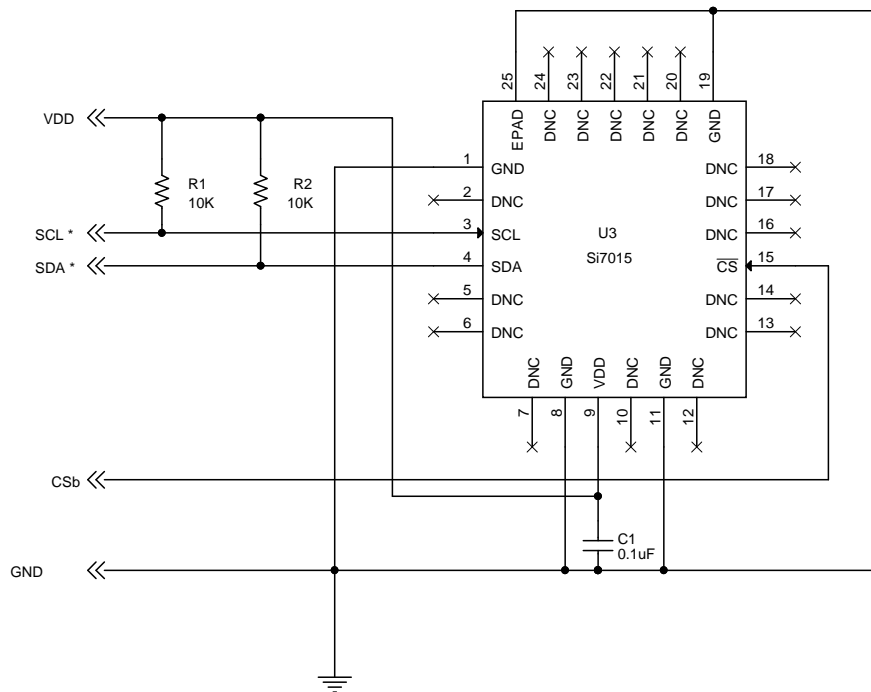


Figure 2. Typical Si7015 Application Circuit for Battery-Powered Applications

In Figure 2, Pin 10 is internally connected but can have a capacitor to ground. \overline{CS} can be tied to ground, and I^2C commands can be used to put the part in low-power mode.

- The strength of the output drivers on the Si7015's SDA and SCL output pins differs from that of the Si7005:
Si7005: IOL = 8.5 mA @ VOL = 0.6 V
Si7015: IOL = 2.5 mA @ VOL = 0.6 V
- There is no internal pull-down resistor on the Si7015's chip select pin (\overline{CS}) as with the Si7005. The Si7015's \overline{CS} pin should not be left floating/unconnected. It should be tied to GND if it is not used.
- As is the case with the Si7005, pins 2, 5–7, 12–14, 16–18, and 20–24 should be floating, i.e., not connected to any electrical signals, power, or ground. If any of these pins have any electrical connection in your system, please contact a Silicon Labs FAE for assistance.

3. Software

- The register set of the Si7015 is identical to that of the Si7005.
- Linearization by the host is no longer required; this operation is performed on-chip in the Si7015. This code should be removed from the system's firmware, or the coefficients can be set to zero ($A0 = A1 = A2 = 0$) to effectively disable linearization on the host.
- Temperature compensation by the host is still required when using the Si7015; however, the temperature compensation coefficients for the Si7015 (Q0 and Q1) are much smaller than for the Si7005, as shown in the data sheet. They can be set to zero, i.e., temperature compensation can be eliminated altogether, with only minor accuracy degradation.
- The Device ID value in the Si7015 (Register 17, upper nibble) is 15 = 0xF rather than 0x5. The lower nibble is the device revision code; 0x0 = Revision A.
- There is a subtlety to the operation of the Si7015's /RDY and START bits that may or may not be an issue depending on how the system's firmware is implemented (/RDY and START are register 0, bit 0 and register 3, bit 0, respectively.)

Once START is set to begin a conversion, /RDY must be read at least once before a valid RH value will be present in DATAh:DATAI; this is true even if an entire tCONV interval has elapsed following the setting of the start bit. Typically, /RDY is polled following the start of a conversion until it becomes low, indicating that the results of a conversion are available in DATAh:DATAI. In this situation, the Si7015 will behave identically to the Si7005.

If the host uses a fixed delay ($>t_{CONV}$) to indicate the end of a conversion without polling /RDY, the result returned in DATAh will always be 0x01. It is recommended that a read of /RDY be added immediately after the setting of START. Using this sequence, the proper value will be present in DATAh:DATAI once a time interval $>t_{CONV}$ has elapsed.

- The Si7015 consumes less power than the Si7005 in both its operating and standby modes. In particular, the standby mode current is exceptionally low, and switching off V_{DD} to save power (as was possible with the Si7005) is no longer supported. However, the Si7015 does not enter its standby mode automatically following an RH conversion. Either of the following sequences can be used to place the Si7015 into its low-power standby mode following an RH conversion:

Option A:

Bring \overline{CS} high. This puts the Si7015 in low-power mode and disables I^2C communication. This is similar to the Si7005 except that the response to \overline{CS} high takes only a few μs , and the V_{DD} current is $<1 \mu A$ (as opposed to the Si7005, which can take >1 second and have V_{DD} current of up to $100 \mu A$).

Option B:

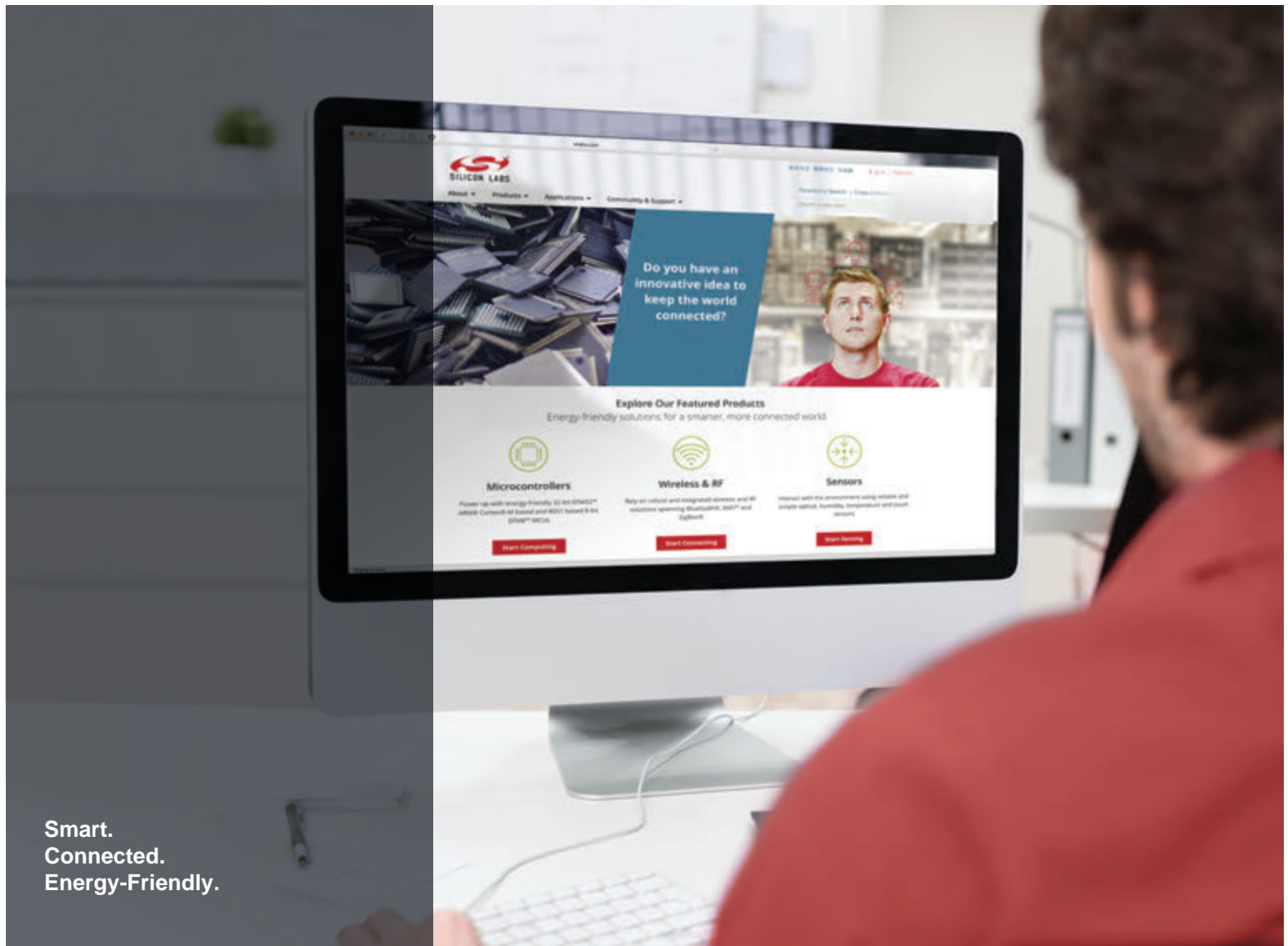
1. Poll /RDY until it returns zero, indicating that the conversion is finished.
2. Read the results of the RH conversion from DATAh:DATAI.
3. Clear the start bit (START) by writing 0x0 to Register 3.
4. Clear the start bit (START) a second time by again writing 0x0 to Register 3.

The Si7015 enters its low-power standby mode following a temperature conversion. No action is required in this case. However, note that doing a temperature conversion following an RH conversion will not put the Si7015 in the low-power state.

- For Si7005, a STOP resets the address pointer; so, in a read sequence, if a STOP then START is used instead of a REPEATED START, the result is the content of register zero. For Si7015, a STOP does not reset the address pointer; so, if a STOP then START is used instead of a REPEATED START, the result is the address pointer value specified.
- For Si7005, registers can be read in sequence by continued clocking. That is, when register zero is read if the RDY bit is 0, then, if this is ACKd by the host, it is possible to continue to read registers 1 and 2. For Si7015, this is not the case; only the data sheet specified read sequences are supported. To read registers 0, 1, and 2, the read of register 0 would be NACKd, and then registers 1 and 2 would be read in a separate I²C transaction. For both devices, registers 1 and 2 can be read sequentially as in the data sheet or read by separate reads of registers 1 and 2.

4. References

- Si7005 data sheet
- Si7015 data sheet

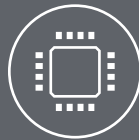


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