IMAGE REJECTION AND IQ CALIBRATION

1. Introduction

The purpose of this document is to describe the Image frequency rejection calibration feature of the Si446x.

2. Image Frequency Rejection Calibration

In default mode, the Si446x product family utilizes a low-IF architecture, which means that the incoming RF signal is downconverted to a low, intermediate frequency* (IF); this is required for low-power signal processing in the digital domain. Although this topology has many advantages, such as overcoming problems related to dc offset and 1/f noise, it introduces the image issue that needs to be resolved. RF signals at the image frequency (IM) are capable of producing the same IF frequency as the desired input, thus resulting in decreased selectivity (see Figure 1). For the nominal crystal frequency of 30.0 MHz, the IM frequency of the chip is at 2 x IF (2 x 468.75 kHz = 937.5 kHz) below the actual RF frequency. As shown in Figure 1, image rejection is the ratio of the signal strength at the IM frequency to its counterpart at the carrier frequency (interferer). In order to receive the desired signal when the interferer is present, the desired signal must typically be 8–10 dB higher than the interferer (co-channel rejection). The ratio of the signal strength at the IM frequency to the desired signal is the image selectivity, and is thus typically 8–10 dB less than the image rejection.

***Note:** When fixed-IF settings are used in the Si446x, IF = Fxtal/64 = 468.75 kHz.

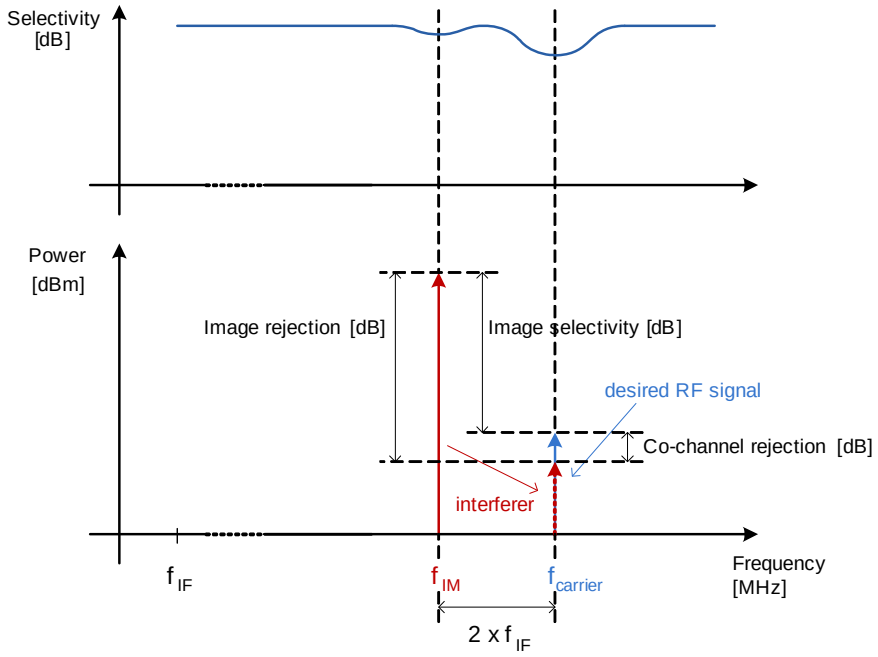

Figure 1. Image Rejection and Selectivity

To improve image rejection and, therefore, image selectivity, the chip should suppress the undesired signal against the desired signal (i.e., signals caused by the IM frequency vs. signals caused by the carrier frequency). Although the optimized receiver circuitry already rejects the image frequency by about 45 dB, if better rejection is desired, IR calibration of the device is possible. With this feature, response to signals occurring originally at the IM frequency can be suppressed more efficiently, and image rejection can be improved to achieve typical performance of about 50–55 dB.

Image selectivity after calibration is shown by Figure 2 (100 kbps data rate, 50 kHz deviation, high-performance mode). Note that image selectivity (the main point of interest from a system design point of view) correlates with image rejection.

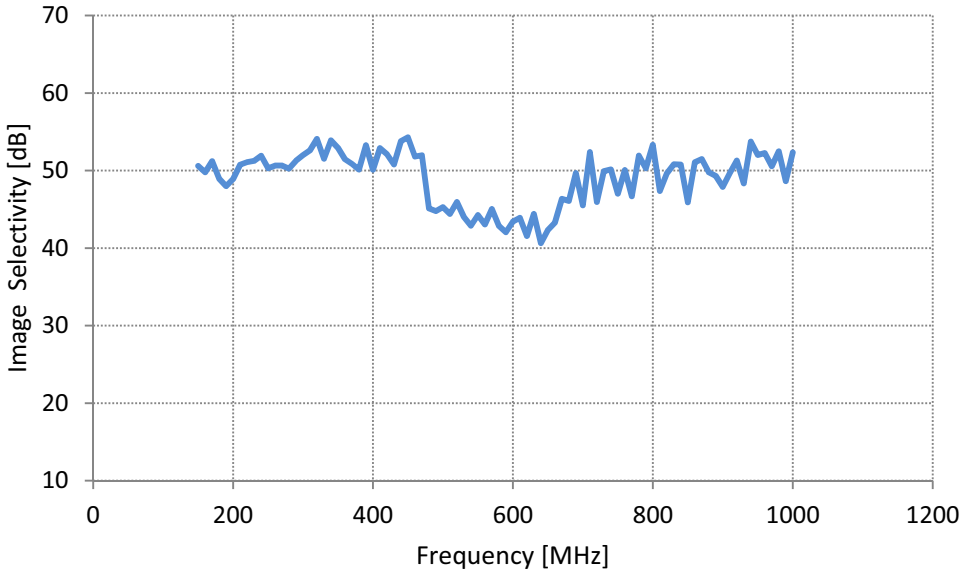

Figure 2. Image Selectivity after Calibration

2.1. Calibration Method

Because calibration uses an internal signal source, it can be performed without any additional circuitry. However, the chip must perform the calibration at the nearest harmonic of the crystal frequency and not at the desired operating frequency. Therefore, the following sequence must be performed:

1. Command the chip's operating frequency to a harmonic of the crystal frequency plus two times the IF frequency, and configure the modem for calibration mode.
2. Perform the actual calibration using IRCAL API commands.
3. Switch back to the original configuration at the desired operating frequency.

For instance, if the desired operating frequency is 925 MHz and a 30 MHz crystal is used, the chip must be temporarily reconfigured to 930 MHz + 2 x IF = 930.9375 MHz for the duration of the calibration.

The temporary modem configuration for the calibration can be calculated by WDS (Wireless Development Suite). The calculation is available for both the scripts (i.e. WDS batch files) and the C projects (i.e. radio_config.h header files).

The calibration is initiated with the IRCAL API command. The initial (coarse + fine) calibration takes 250 ms, and any periodic recalibration (fine calibration) takes 100 ms.

For high-band (868/915 MHz), the following commands should be used:

- IRCAL 56 10 FA F0 - coarse calibration (150 ms)
- IRCAL 13 10 FA F0 - fine calibration (100 ms)

For low-band (169–315 MHz, 430–510 MHz), the following commands should be used:

- IRCAL 56 10 CA F0 - coarse calibration (150 ms)
- IRCAL 13 10 CA F0 - fine calibration (100 ms)

If temperature changes by more than 30 °C, a fine calibration should be performed again. Figure 3 shows how image rejection changes with temperature if calibration is performed at room temperature (the blue curve is averaged over the other four, typical parts' curves).

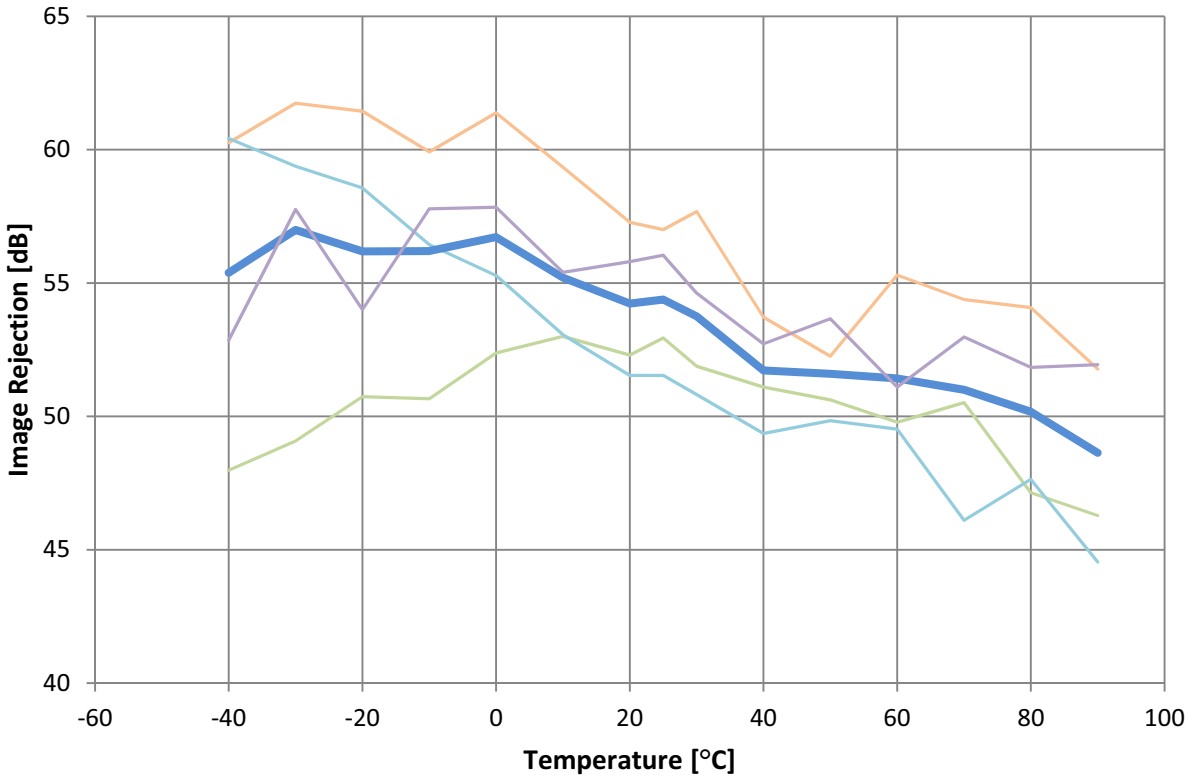

Figure 3. Image Rejection Variation over Temperature

To ensure that the calibration is completed, either CTS should be polled or CHIP_READY interrupt should be monitored. The calibration settings are maintained if the chip goes to Standby/Sleep state. They are lost only upon Shutdown mode (POR), just like any other modem parameter. The calibration is intended to be performed in the field, and it is currently not possible to store the calibration parameters in the host MCU memory.

To evaluate this feature, the WDS Software tool should be used. Enabling IQ calibration in the WDS GUI results in the generation of a script/radio configuration header file that includes the entire calibration process (i.e., temporarily configuring to the nearest harmonic frequency, applying modem parameters for calibration, calling IRCAL commands, and configuring for the desired frequency).

2.2. Example

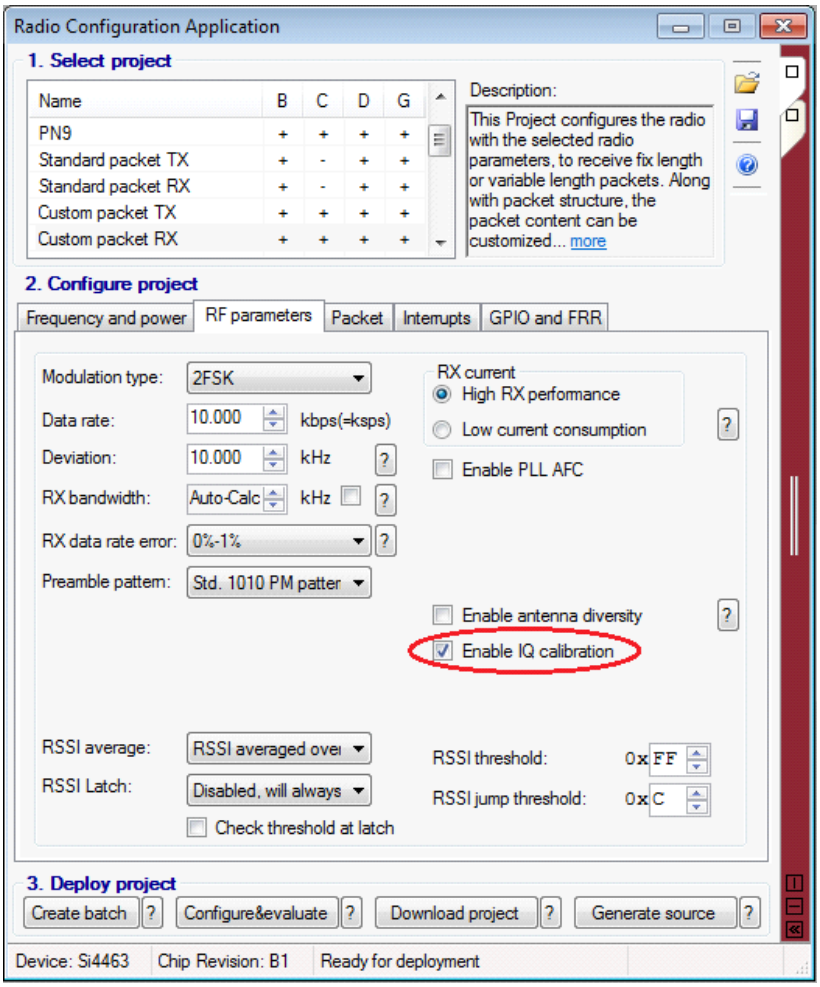

Figure 4. Enabling IQ Calibration in WDS

In this section a WDS example script is provided to demonstrate how to use the image rejection calibration feature. The main RF parameters for this example are as follows:

- Operating frequency: 915 MHz
- Data rate: 10 kbps
- Deviation: 10 kHz
- Crystal frequency: 30 MHz
- Modulation type: 2FSK

In the script below, it can be seen that the chip is first configured to a frequency other than the operating frequency (i.e., 900.9375 MHz) and several modem parameters are temporarily configured (e.g., very narrow BW filter is used, data rate is lowered, etc.). IRCAL commands are called and CTS is monitored to make sure that the calibration has completed. After the calibration, the chip is configured to the actual operating frequency.

```
# IRCAL example
#%%    Crys_freq(Hz) Crys_tol(ppm) IF_mode       High_perf_Ch_Fil    OSRtune
       Ch_Fil_Bw_AFC ANT_DIV       PM_pattern
#      30000000      20     2      1      0      0      0      0
#%%    MOD_type      Rsymb(sps)    Fdev(Hz)      RXBW(Hz)      Mancheste     AFC_en
       Rsymb_error   Chip-Version
```

```
#      2      10000  10000  150000 0      0      0.0    2
#%%    RF Freq.(MHz) API_TC fhst   inputBW       BERT   RAW_dout      D_source
       Hi_pfm_div
#      915    29     250000 0      0      0      0      1
#
# # WB filter 2 (BW = 103.06 kHz);  NB-filter 2 (BW = 103.06 kHz)

#
# Modulation index: 2
RESET
'POWER_UP' 01 00 01 C9 C3 80
'GPIO_PIN_CFG' 21 11 20 14 00 00 00
'SET_PROPERTY' 'GLOBAL_XO_TUNE' 44

# Temporary modem configuration for the IR calibration
'SET_PROPERTY' 'MODEM_MOD_TYPE' 03
'SET_PROPERTY' 'MODEM_MAP_CONTROL' 00
'SET_PROPERTY' 'MODEM_DSM_CTRL' 07
'SET_PROPERTY' 'MODEM_CLKGEN_BAND' 08
'SET_PROPERTY' 'SYNTH_PFDCP_CPFF' 2C
'SET_PROPERTY' 'SYNTH_PFDCP_CPINT' 0E
'SET_PROPERTY' 'SYNTH_VCO_KV' 0B
'SET_PROPERTY' 'SYNTH_LPFILT3' 04
'SET_PROPERTY' 'SYNTH_LPFILT2' 0C
'SET_PROPERTY' 'SYNTH_LPFILT1' 73
'SET_PROPERTY' 'SYNTH_LPFILT0' 03
'SET_PROPERTY' 'MODEM_DATA_RATE_2' 00
'SET_PROPERTY' 'MODEM_DATA_RATE_1' 3E
'SET_PROPERTY' 'MODEM_DATA_RATE_0' 80
'SET_PROPERTY' 'MODEM_TX_NCO_MODE_3' 04
'SET_PROPERTY' 'MODEM_TX_NCO_MODE_2' 2D
'SET_PROPERTY' 'MODEM_TX_NCO_MODE_1' C6
'SET_PROPERTY' 'MODEM_TX_NCO_MODE_0' C0
'SET_PROPERTY' 'MODEM_FREQ_DEV_2' 00
'SET_PROPERTY' 'MODEM_FREQ_DEV_1' 00
'SET_PROPERTY' 'MODEM_FREQ_DEV_0' 23
'SET_PROPERTY' 'MODEM_TX_RAMP_DELAY' 01
'SET_PROPERTY' 'PA_TC' 3D
'SET_PROPERTY' 'FREQ_CONTROL_INTE' 3B
'SET_PROPERTY' 'FREQ_CONTROL_FRAC_2' 08
'SET_PROPERTY' 'FREQ_CONTROL_FRAC_1' 80
'SET_PROPERTY' 'FREQ_CONTROL_FRAC_0' 00
'SET_PROPERTY' 'FREQ_CONTROL_CHANNEL_STEP_SIZE_1' 22
'SET_PROPERTY' 'FREQ_CONTROL_CHANNEL_STEP_SIZE_0' 22
'SET_PROPERTY' 'FREQ_CONTROL_W_SIZE' 20
'SET_PROPERTY' 'FREQ_CONTROL_VCOCNT_RX_ADJ' FF
'SET_PROPERTY' 'MODEM_MDM_CTRL' 00
'SET_PROPERTY' 'MODEM_IF_CONTROL' 08
'SET_PROPERTY' 'MODEM_IF_FREQ_2' 03
'SET_PROPERTY' 'MODEM_IF_FREQ_1' C0
'SET_PROPERTY' 'MODEM_IF_FREQ_0' 00
'SET_PROPERTY' 'MODEM_DECIMATION_CFG1' B0
'SET_PROPERTY' 'MODEM_DECIMATION_CFG0' 10
'SET_PROPERTY' 'MODEM_BCR_OSR_1' 00
'SET_PROPERTY' 'MODEM_BCR_OSR_0' 4E
'SET_PROPERTY' 'MODEM_BCR_NCO_OFFSET_2' 06
'SET_PROPERTY' 'MODEM_BCR_NCO_OFFSET_1' 8D
'SET_PROPERTY' 'MODEM_BCR_NCO_OFFSET_0' B9
'SET_PROPERTY' 'MODEM_BCR_GAIN_1' 00
'SET_PROPERTY' 'MODEM_BCR_GAIN_0' 00
'SET_PROPERTY' 'MODEM_BCR_GEAR' 02
'SET_PROPERTY' 'MODEM_BCR_MISC1' C0
'SET_PROPERTY' 'MODEM_AFC_GEAR' 00
'SET_PROPERTY' 'MODEM_AFC_WAIT' 12
'SET_PROPERTY' 'MODEM_AFC_GAIN_1' 00
'SET_PROPERTY' 'MODEM_AFC_GAIN_0' 11
'SET_PROPERTY' 'MODEM_AFC_LIMITER_1' 01
'SET_PROPERTY' 'MODEM_AFC_LIMITER_0' 66
'SET_PROPERTY' 'MODEM_AFC_MISC' A0
'SET_PROPERTY' 'MODEM_AGC_CONTROL' E2
'SET_PROPERTY' 'MODEM_AGC_WINDOW_SIZE' 11
'SET_PROPERTY' 'MODEM_AGC_RFPD_DECAY' 11
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'SET_PROPERTY' 'MODEM_AGC_IFPD_DECAY' 11
'SET_PROPERTY' 'MODEM_FSK4_GAIN1' 00
'SET_PROPERTY' 'MODEM_FSK4_GAIN0' 1A
'SET_PROPERTY' 'MODEM_FSK4_TH1' 20
'SET_PROPERTY' 'MODEM_FSK4_TH0' 00
'SET_PROPERTY' 'MODEM_FSK4_MAP' 00
'SET_PROPERTY' 'MODEM_OOK_PDTC' 28
'SET_PROPERTY' 'MODEM_OOK_CNT1' A4
'SET_PROPERTY' 'MODEM_OOK_MISC' 03
'SET_PROPERTY' 'MODEM_RAW_SEARCH' D6
'SET_PROPERTY' 'MODEM_RAW_CONTROL' 03
'SET_PROPERTY' 'MODEM_RAW_EYE_1' 00
'SET_PROPERTY' 'MODEM_RAW_EYE_0' CC
'SET_PROPERTY' 'MODEM_ANT_DIV_MODE' 01
'SET_PROPERTY' 'MODEM_ANT_DIV_CONTROL' 80
'SET_PROPERTY' 'MODEM_RSSI_COMP' 22
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE13_7_0' 7E
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE12_7_0' 64
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE11_7_0' 1B
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE10_7_0' BA
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE9_7_0' 58
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE8_7_0' 0B
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE7_7_0' DD
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE6_7_0' CE
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE5_7_0' D6
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE4_7_0' E6
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE3_7_0' F6
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE2_7_0' 00
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE1_7_0' 03
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE0_7_0' 03
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COEM0' 15
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COEM1' F0
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COEM2' 3F
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COEM3' 00
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE13_7_0' 7E
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE12_7_0' 64
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE11_7_0' 1B
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE10_7_0' BA
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE9_7_0' 58
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE8_7_0' 0B
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE7_7_0' DD
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE6_7_0' CE
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE5_7_0' D6
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE4_7_0' E6
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE3_7_0' F6
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE2_7_0' 00
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE1_7_0' 03
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE0_7_0' 03
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COEM0' 15
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COEM1' F0
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COEM2' 3F
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COEM3' 00
'SET_PROPERTY' 'GLOBAL_CONFIG' 60
'START_RX' 00 00 00 00 00 00

# Perform IR calibration (coarse and fine)
'IRCAL' 56 10 FA F0
'IRCAL' 13 10 FA F0

# Permanent modem and general configuration
'SET_PROPERTY' 'FRR_CTL_A_MODE' 00
'SET_PROPERTY' 'FRR_CTL_B_MODE' 00
'SET_PROPERTY' 'FRR_CTL_C_MODE' 00
'SET_PROPERTY' 'FRR_CTL_D_MODE' 00
'SET_PROPERTY' 'INT_CTL_PH_ENABLE' 18
'SET_PROPERTY' 'INT_CTL_MODEM_ENABLE' 01
'SET_PROPERTY' 'INT_CTL_CHIP_ENABLE' 08
'SET_PROPERTY' 'INT_CTL_ENABLE' 07
'SET_PROPERTY' 'GLOBAL_CONFIG' 60
'SET_PROPERTY' 'MODEM_RSSI_CONTROL' 00
'SET_PROPERTY' 'MODEM_RSSI_THRESH' FF
'SET_PROPERTY' 'MODEM_RSSI_JUMP_THRESH' 0C
```

```
'SET_PROPERTY' 'PREAMBLE_TX_LENGTH' 08
'SET_PROPERTY' 'PREAMBLE_CONFIG_STD_1' 14
'SET_PROPERTY' 'PREAMBLE_CONFIG_NSTD' 00
'SET_PROPERTY' 'PREAMBLE_CONFIG_STD_2' 0F
'SET_PROPERTY' 'PREAMBLE_CONFIG' 31
'SET_PROPERTY' 'PREAMBLE_PATTERN_31_24' 00
'SET_PROPERTY' 'PREAMBLE_PATTERN_23_16' 00
'SET_PROPERTY' 'PREAMBLE_PATTERN_15_8' 00
'SET_PROPERTY' 'PREAMBLE_PATTERN_7_0' 00
'SET_PROPERTY' 'SYNC_CONFIG' 01
'SET_PROPERTY' 'SYNC_BITS_31_24' B4
'SET_PROPERTY' 'SYNC_BITS_23_16' 2B
'SET_PROPERTY' 'SYNC_BITS_15_8' 00
'SET_PROPERTY' 'SYNC_BITS_7_0' 00
'SET_PROPERTY' 'PKT_CRC_CONFIG' 80
'SET_PROPERTY' 'PKT_CONFIG1' 02
'SET_PROPERTY' 'PKT_LEN' 00
'SET_PROPERTY' 'PKT_LEN_FIELD_SOURCE' 00
'SET_PROPERTY' 'PKT_LEN_ADJUST' 00
'SET_PROPERTY' 'PKT_FIELD_1_LENGTH_12_8' 00
'SET_PROPERTY' 'PKT_FIELD_1_LENGTH_7_0' 07
'SET_PROPERTY' 'PKT_FIELD_1_CONFIG' 04
'SET_PROPERTY' 'PKT_FIELD_1_CRC_CONFIG' 00
'SET_PROPERTY' 'PKT_FIELD_2_LENGTH_12_8' 00
'SET_PROPERTY' 'PKT_FIELD_2_LENGTH_7_0' 00
'SET_PROPERTY' 'PKT_FIELD_2_CONFIG' 00
'SET_PROPERTY' 'PKT_FIELD_2_CRC_CONFIG' 00
'SET_PROPERTY' 'PKT_FIELD_3_LENGTH_12_8' 00
'SET_PROPERTY' 'PKT_FIELD_3_LENGTH_7_0' 00
'SET_PROPERTY' 'PKT_FIELD_3_CONFIG' 00
'SET_PROPERTY' 'PKT_FIELD_3_CRC_CONFIG' 00
'SET_PROPERTY' 'PKT_FIELD_4_LENGTH_12_8' 00
'SET_PROPERTY' 'PKT_FIELD_4_LENGTH_7_0' 00
'SET_PROPERTY' 'PKT_FIELD_4_CONFIG' 00
'SET_PROPERTY' 'PKT_FIELD_4_CRC_CONFIG' 00
'SET_PROPERTY' 'PKT_FIELD_5_LENGTH_12_8' 00
'SET_PROPERTY' 'PKT_FIELD_5_LENGTH_7_0' 00
'SET_PROPERTY' 'PKT_FIELD_5_CONFIG' 00
'SET_PROPERTY' 'PKT_FIELD_5_CRC_CONFIG' 00
'SET_PROPERTY' 'MATCH_VALUE_1' 00
'SET_PROPERTY' 'MATCH_MASK_1' 00
'SET_PROPERTY' 'MATCH_CTRL_1' 00
'SET_PROPERTY' 'MATCH_VALUE_2' 00
'SET_PROPERTY' 'MATCH_MASK_2' 00
'SET_PROPERTY' 'MATCH_CTRL_2' 00
'SET_PROPERTY' 'MATCH_VALUE_3' 00
'SET_PROPERTY' 'MATCH_MASK_3' 00
'SET_PROPERTY' 'MATCH_CTRL_3' 00
'SET_PROPERTY' 'MATCH_VALUE_4' 00
'SET_PROPERTY' 'MATCH_MASK_4' 00
'SET_PROPERTY' 'MATCH_CTRL_4' 00
'SET_PROPERTY' 'MODEM_MOD_TYPE' 02
'SET_PROPERTY' 'MODEM_MAP_CONTROL' 00
'SET_PROPERTY' 'MODEM_DSM_CTRL' 07
'SET_PROPERTY' 'MODEM_CLKGEN_BAND' 08
'SET_PROPERTY' 'SYNTH_PFDCP_CPFF' 2C
'SET_PROPERTY' 'SYNTH_PFDCP_CPINT' 0E
'SET_PROPERTY' 'SYNTH_VCO_KV' 0B
'SET_PROPERTY' 'SYNTH_LPFILT3' 04
'SET_PROPERTY' 'SYNTH_LPFILT2' 0C
'SET_PROPERTY' 'SYNTH_LPFILT1' 73
'SET_PROPERTY' 'SYNTH_LPFILT0' 03
'SET_PROPERTY' 'MODEM_DATA_RATE_2' 00
'SET_PROPERTY' 'MODEM_DATA_RATE_1' 27
'SET_PROPERTY' 'MODEM_DATA_RATE_0' 10
'SET_PROPERTY' 'MODEM_TX_NCO_MODE_3' 00
'SET_PROPERTY' 'MODEM_TX_NCO_MODE_2' 2D
'SET_PROPERTY' 'MODEM_TX_NCO_MODE_1' C6
'SET_PROPERTY' 'MODEM_TX_NCO_MODE_0' C0
'SET_PROPERTY' 'MODEM_FREQ_DEV_2' 00
'SET_PROPERTY' 'MODEM_FREQ_DEV_1' 01
'SET_PROPERTY' 'MODEM_FREQ_DEV_0' 5E
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'SET_PROPERTY' 'MODEM_TX_RAMP_DELAY' 01
'SET_PROPERTY' 'PA_TC' 3D
'SET_PROPERTY' 'FREQ_CONTROL_INTE' 3C
'SET_PROPERTY' 'FREQ_CONTROL_FRAC_2' 08
'SET_PROPERTY' 'FREQ_CONTROL_FRAC_1' 00
'SET_PROPERTY' 'FREQ_CONTROL_FRAC_0' 00
'SET_PROPERTY' 'FREQ_CONTROL_CHANNEL_STEP_SIZE_1' 22
'SET_PROPERTY' 'FREQ_CONTROL_CHANNEL_STEP_SIZE_0' 22
'SET_PROPERTY' 'FREQ_CONTROL_W_SIZE' 20
'SET_PROPERTY' 'FREQ_CONTROL_VCOCNT_RX_ADJ' FF
'SET_PROPERTY' 'MODEM_MDM_CTRL' 80
'SET_PROPERTY' 'MODEM_IF_CONTROL' 08
'SET_PROPERTY' 'MODEM_IF_FREQ_2' 03
'SET_PROPERTY' 'MODEM_IF_FREQ_1' C0
'SET_PROPERTY' 'MODEM_IF_FREQ_0' 00
'SET_PROPERTY' 'MODEM_DECIMATION_CFG1' 20
'SET_PROPERTY' 'MODEM_DECIMATION_CFG0' 20
'SET_PROPERTY' 'MODEM_BCR_OSR_1' 01
'SET_PROPERTY' 'MODEM_BCR_OSR_0' 77
'SET_PROPERTY' 'MODEM_BCR_NCO_OFFSET_2' 01
'SET_PROPERTY' 'MODEM_BCR_NCO_OFFSET_1' 5D
'SET_PROPERTY' 'MODEM_BCR_NCO_OFFSET_0' 86
'SET_PROPERTY' 'MODEM_BCR_GAIN_1' 00
'SET_PROPERTY' 'MODEM_BCR_GAIN_0' AF
'SET_PROPERTY' 'MODEM_BCR_GEAR' 02
'SET_PROPERTY' 'MODEM_BCR_MISC1' C2
'SET_PROPERTY' 'MODEM_AFC_GEAR' 04
'SET_PROPERTY' 'MODEM_AFC_WAIT' 36
'SET_PROPERTY' 'MODEM_AFC_GAIN_1' 80
'SET_PROPERTY' 'MODEM_AFC_GAIN_0' 0F
'SET_PROPERTY' 'MODEM_AFC_LIMITER_1' 13
'SET_PROPERTY' 'MODEM_AFC_LIMITER_0' 40
'SET_PROPERTY' 'MODEM_AFC_MISC' 80
'SET_PROPERTY' 'MODEM_AGC_CONTROL' E2
'SET_PROPERTY' 'MODEM_AGC_WINDOW_SIZE' 11
'SET_PROPERTY' 'MODEM_AGC_RFPD_DECAY' 52
'SET_PROPERTY' 'MODEM_AGC_IFPD_DECAY' 52
'SET_PROPERTY' 'MODEM_FSK4_GAIN1' 00
'SET_PROPERTY' 'MODEM_FSK4_GAIN0' 02
'SET_PROPERTY' 'MODEM_FSK4_TH1' 80
'SET_PROPERTY' 'MODEM_FSK4_TH0' 00
'SET_PROPERTY' 'MODEM_FSK4_MAP' 00
'SET_PROPERTY' 'MODEM_OOK_PDTC' 2A
'SET_PROPERTY' 'MODEM_OOK_CNT1' A4
'SET_PROPERTY' 'MODEM_OOK_MISC' 02
'SET_PROPERTY' 'MODEM_RAW_SEARCH' D6
'SET_PROPERTY' 'MODEM_RAW_CONTROL' 83
'SET_PROPERTY' 'MODEM_RAW_EYE_1' 00
'SET_PROPERTY' 'MODEM_RAW_EYE_0' 90
'SET_PROPERTY' 'MODEM_ANT_DIV_MODE' 01
'SET_PROPERTY' 'MODEM_ANT_DIV_CONTROL' 80
'SET_PROPERTY' 'MODEM_RSSI_COMP' 40
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE13_7_0' FF
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE12_7_0' C4
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE11_7_0' 30
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE10_7_0' 7F
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE9_7_0' F5
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE8_7_0' B5
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE7_7_0' B8
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE6_7_0' DE
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE5_7_0' 05
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE4_7_0' 17
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE3_7_0' 16
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE2_7_0' 0C
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE1_7_0' 03
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COE0_7_0' 00
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COEM0' 15
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COEM1' FF
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COEM2' 00
'SET_PROPERTY' 'MODEM_CHFLT_RX1_CHFLT_COEM3' 00
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE13_7_0' FF
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE12_7_0' C4
```
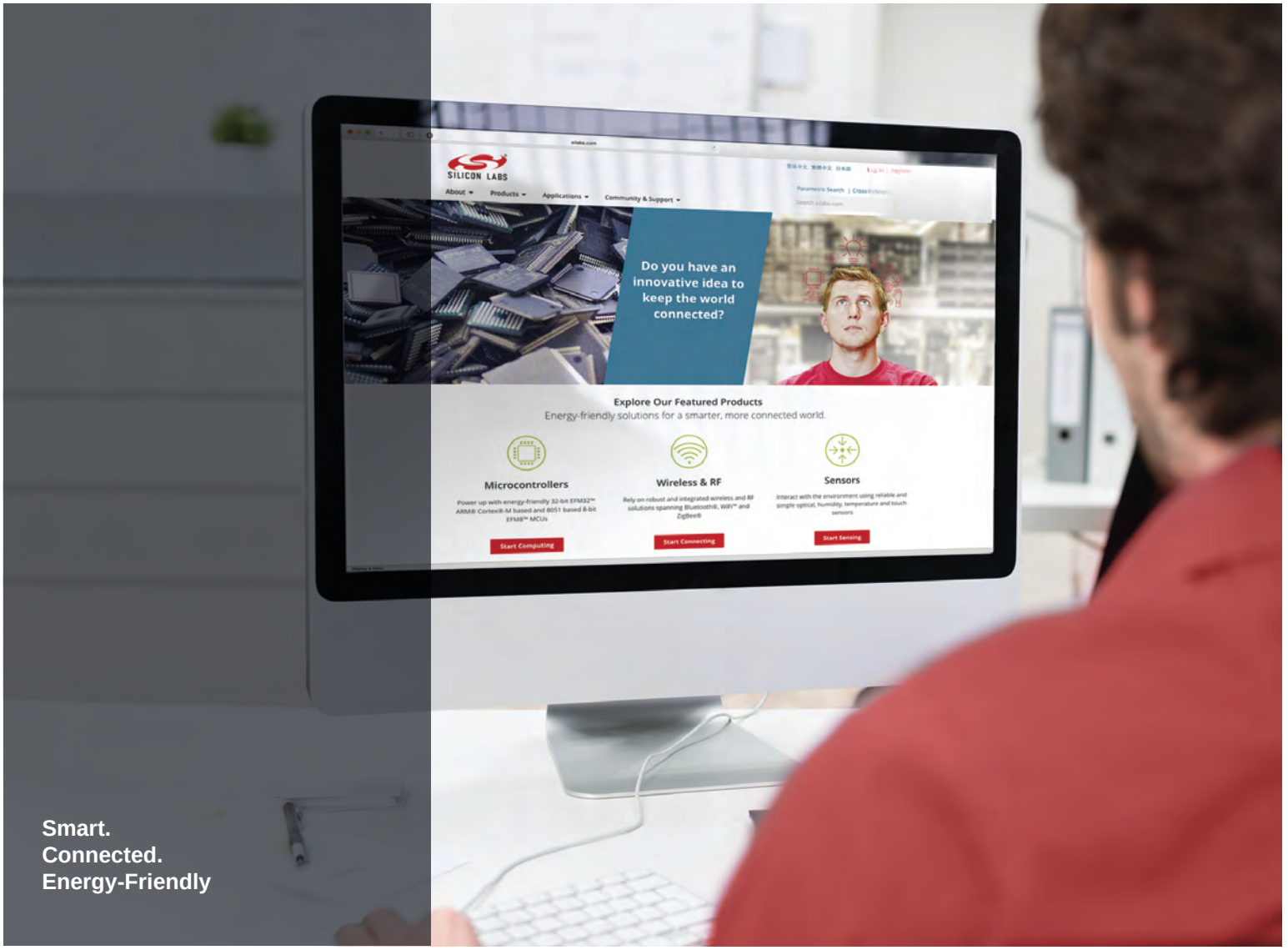

```
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE11_7_0' 30
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE10_7_0' 7F
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE9_7_0' F5
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE8_7_0' B5
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE7_7_0' B8
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE6_7_0' DE
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE5_7_0' 05
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE4_7_0' 17
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE3_7_0' 16
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE2_7_0' 0C
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE1_7_0' 03
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COE0_7_0' 00
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COEM0' 15
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COEM1' FF
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COEM2' 00
'SET_PROPERTY' 'MODEM_CHFLT_RX2_CHFLT_COEM3' 00
'START_RX' 00 00 00 00 00 08 08
```

Running this script on a single chip resulted in the image rejection being improved from 45 dB to 58 dB. The image selectivity and, therefore, the image rejection typically improves by 10–12 dB as a result of the calibration. Note that the improvement may vary with frequency and temperature and from chip to chip.



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