LAYOUT DESIGN GUIDE FOR THE Si106X/8X WIRELESS MCUS

1. Introduction

The purpose of this application note is to help users design PCBs for the next generation Wireless MCU IC family: single-chip packaging of the C8051F91x/3x MCU core with the Si446x EZRadioPRO® transceiver i.e. the Si1060/61/62/63/64/65/80/81/82/83/84/85 devices (further in this document referred as WMCUs) using good design practices that allow for good RF performance. The matching principles described in detail in "AN627: Si4460/61 Low-Power PA Matching" and in "AN648: Si4463/4464 TX Matching".

The RF performance and the critical maximum peak voltage on the output pin strongly depend on the PCB layout as well as the design of the matching networks. For optimal performance Silicon Labs recommends the use of the PCB layout design hints described in the next chapters.

2. Design Recommendations when Using Si106x/8x RF ICs

- Extensive testing has been completed using reference designs provided by Silicon Labs. It is recommended to designers to use the reference designs 'as-is' since they minimize de-tuning effects caused by parasitics, generated by component placement and PCB routing.
- The compact RF part of the designs is highlighted by a silkscreen frame and it is strongly recommended to use the same framed RF layout in order to avoid any possibilities of detuning effects. Figure 1 shows the framed compact RF part of the designs.

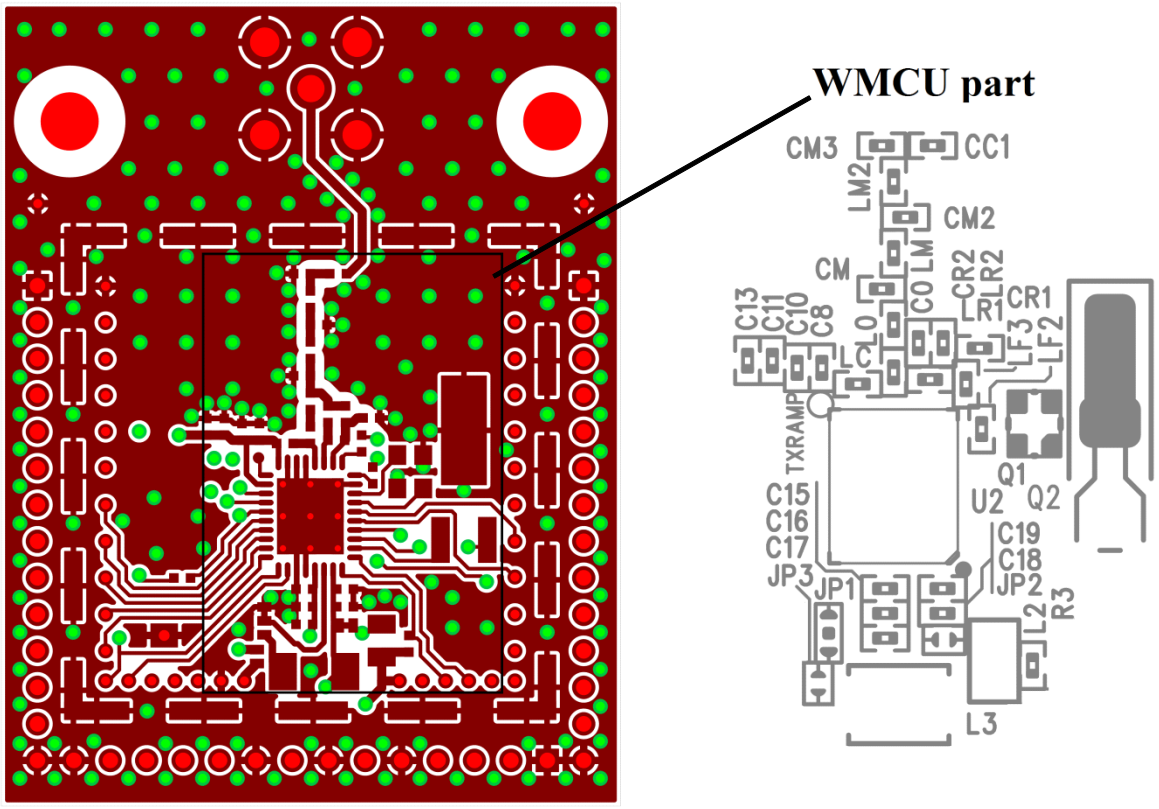


Figure 1. Compact WMCU Part of the Designs Highlighted on Top Silkscreen

- When layouts as shown by the reference designs cannot be followed (as a result of PCB size and shape limitations) then the following layout design rules are recommended.

2.1. Matching Network Types and Layout Topologies for the Si106x/8x WMCUs

Based on the Si446x devices the Si106x/8x devices can use the following type of TX matching networks:

- Class E (CLE)
- Switched Current (SWC)
- Square-Wave (SQW)

The basic types of board layout topologies are the following:

- Split TX/RX
- Direct Tie
- Switched TX/RX
- Diversity

In the Split TX/RX type, the TX and RX paths are separated, and individual SMA connectors are provided for each path. This type of Pico Board is best suited for demonstrating the output power and sensitivity of the EZRadioPRO® WMCUs.

In the Direct Tie type, the TX and RX paths are connected together directly, without any additional RF switch.

In the Switched TX/RX type, the boards contain a single antenna and a single-pole double-throw (SPDT) RF switch to select between the TX and RX paths.

In the Diversity type, there are two antennas, both can be connected either to the TX or the RX path by a double-pole double-throw (DPDT) RF switch.

Note: The Si1060/61/80/81 and the Si1062/63/64/65/82/83/84/85 WMCUs are not pin compatible in terms of the PA output (TX pin). Regardless of that the structure of all matching networks for the two types of WMCUs are the same thus only one schematic will be shown as example for the different types of matchings.

Table 1 shows the advantages and disadvantages of the most frequently used matching and topology configurations together with references to the relevant application notes.

Table 1. Silicon Labs EZRadioPro Sub-GHz Wireless MCU Family RF Match Cross-References

Match Type	Advantages	Disadvantages	Wireless MCU Types	
			Si1060/61 Si1080/81 (TRX)	**Si1062/63/64/5 Si1082/83/84/85 (TRX)**
Class E Split TX/RX	High efficiency, High power	Power varies with VDD, Nonlinear power steps	**AN648**, 868/915M 20 dBm & 85 mA	**AN627**, 434/868/915M 10...13 dBm & 16...24 mA
Class E DT	High efficiency, High power, One antenna	Power varies with VDD, Nonlinear power steps	**AN648**, 868/915M 20 dBm & 85 mA	**AN627**, 434/868/915M 10...13 dBm & 17...25 mA
Class E TX/RX Switch	High efficiency, One antenna	Power varies with VDD, Nonlinear power steps, additional RF switch adds cost	**AN648**, 868/915M 20 dBm & 85 mA	
SQW SDT	High efficiency, High power, One antenna	Power varies with VDD, Nonlinear power steps	**AN648**, 169M 20 dBm & 70 mA	**AN627,** 169M, 10dBm & 18 mA
SWC Split TX/RX	Flat VDD characteristic, Lower BOM (than class E), Linear power steps	Less efficient, Medium power		**AN627**, 315/434/868/915M 10dBm & 24mA
SWC DT	Flat VDD characteristic, Lower BOM (than class E), Linear power steps, One antenna	Less efficient, Medium power		**AN627**, 315/434/868/915M 10 dBm & 24 mA

3. Guidelines for Layout Design When Using the Si106x/8x WMCUs in Pico Board Form

The Si1062/63/64/65/82/83/84/85 WMCUs are primarily devoted to the +10…+13 dBm applications. For these devices the preferred matching types at the 315….950 MHz frequency range are the CLE and the SWC. The operating principles of these types and the reference designs with element values are given in "AN627: Si4460/61 Low-Power PA Matching".

For the versions of WMCU Pico Boards using the Si1060/61/80/81 WMCUs (i.e., +20 dBm PA) with CLE and SWC type Split TX/RX and Direct Tie type matchings, similar general layout guidelines can be applied as in case of the ones with +10...+13 dBm PA. However, some small additional amount of filtering could be necessary depending on the harmonic restrictions of the relevant EMC regulation. The layout issues of the SQW type matching will be discussed in this chapter as well. This type of matching can be effectively used when the required output power is high and the operating frequency is low (e.g. 169 MHz). The operating principles of these types and the reference designs with element values are given in "AN648: Si4463/4464 TX Matching".

It is not greatly surprising that the increased TX output power of the Si1060/61/80/81 chips is accompanied by a corresponding increase in the absolute level of harmonic signals. As most regulatory standards (e.g., FCC, ETSI, ARIB etc.) require the harmonic signals to be attenuated below some ***absolute*** power level (in watts or dBm), the amount of lowpass filtering required is generally greater on a WMCU Pico Board using an Si1060/61/80/81 chip. Thus the RF Pico Board layout for the Si1060/61/80/81 WMCUs may contain slightly more components in the L-C low pass filter.

Furthermore, in case of the SQW type matching it is necessary to pay closer attention to the shape and amplitude of the voltage waveform at the TX output pin of the device, due to the increase in output power. Silicon Labs recommends the addition of a harmonic termination circuit (formed by the LH, CH and RH components), placed in parallel shunt-to-GND configuration at the input of the lowpass filter. This harmonic termination circuit helps to maintain the desired voltage waveform at the TX output pin by providing a good impedance termination at very high harmonic frequencies. Please refer to "AN648: Si4463/4464 TX Matching" for further details on this subject.

Beside the TX output, unwanted harmonics appear on other pins due to coupling inside the chip. Depending on the actual output power level and the relevant EMC regulation these emissions can cause problems if they are radiated by the traces of a custom board with poor RF design. Similarly, in RX mode the leakage of the VCO reference signal appears.

That is why Silicon Labs' reference design WMCU Pico Boards incorporate additional filtering on the GPIO_2 and GPIO_3 traces (although these boards themselves are compliant with the relevant EMC regulation without this additional filtering).

Some general rules of thumb to design a RF related layout for good RF performance:

- Use as large continuous ground plane metallization as possible.
- Avoid the separation of the ground plane metallization.
- Use as many grounding vias (especially near to the GND pins) as possible to minimize series parasitic inductance between the ground pour and the GND pins.
- Use a series of GND vias (a so called "via curtain") along the PCB edges and internal GND metal pouring edges. The maximum distance between the vias should be less than lambda/10 of the 10th harmonic. This is required to reduce the PCB radiation at higher harmonics caused by the fringing field of these edges.
- Avoid using long and/or thin transmission lines for connecting the components or else due to its distributed parasitic inductance some de-tuning effects can be occurred.
- Try to avoid placing the nearby inductors in the same orientation to reduce the coupling between them
- Use tapered line between transmission lines with different width (i.e. different impedance) to reduce the internal reflections.
- Avoid using loops and long wires to obviate its resonances.
- Always ensure good VRF filtering by using some bypass capacitors (especially at the range of the operating frequency).

3.1. Class E Split TX/RX Type Matching Network Layout (Separate TX and RX Paths for 2 Antennas)

Examples shown in this section of the guide are mainly based upon the layout of the 1060-PCE20B915 Pico Boards. These boards contain two separate antennas for the TX and RX paths. This type of Pico Board is best suited for demonstrating the best possible conducted output power and sensitivity of the WMCUs. For this purpose the layout of the TX and RX paths are separated and isolated as much as possible to minimize the coupling effects between them. This type of Pico Board is recommended for laboratory and not for range tests as the presence of two closely-spaced antennas may cause "shadowing" when receiving a radiated signal.

The main layout design concepts are reviewed through this layout to demonstrate the basic principles. However, for an actual application the layouts of the Pico Boards with single antenna (or with antenna diversity) should be used as references.

The layout design recommendations for the TX only and RX only Pico Boards are fully covered in this section as well without directly touching these cases.

The schematic of the CLE Split TX/RX type matching network for the Si106x/8x is shown in Figure 2.

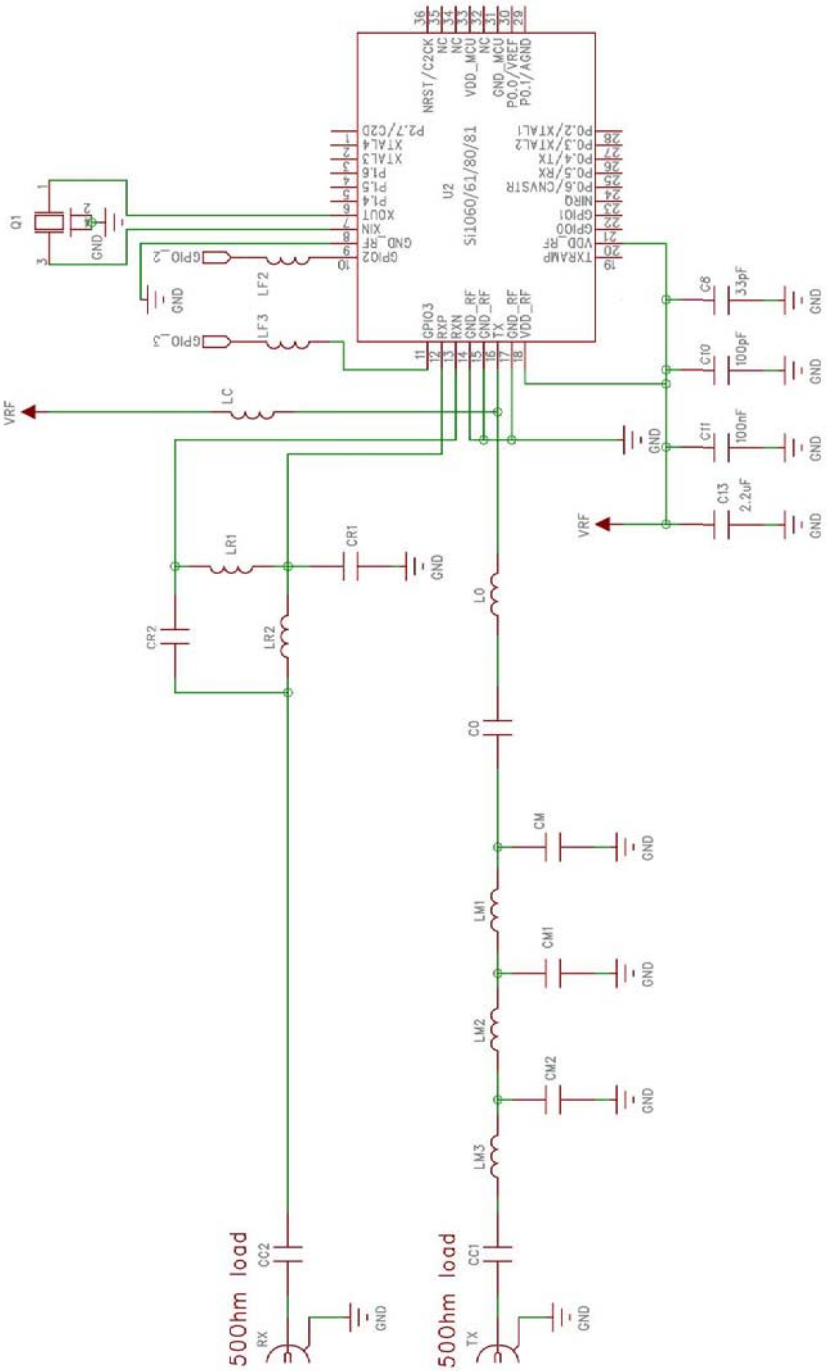


Figure 2. Schematic of the CLE Split TX/RX Type Matching Network for the Si1060/61/80/81

Component values should be chosen based on frequency band, using AN648: Si4463/4464 TX Matching as a guideline. The layout structure of the CLE Split TX/RX type matching network is shown in Figure 3.

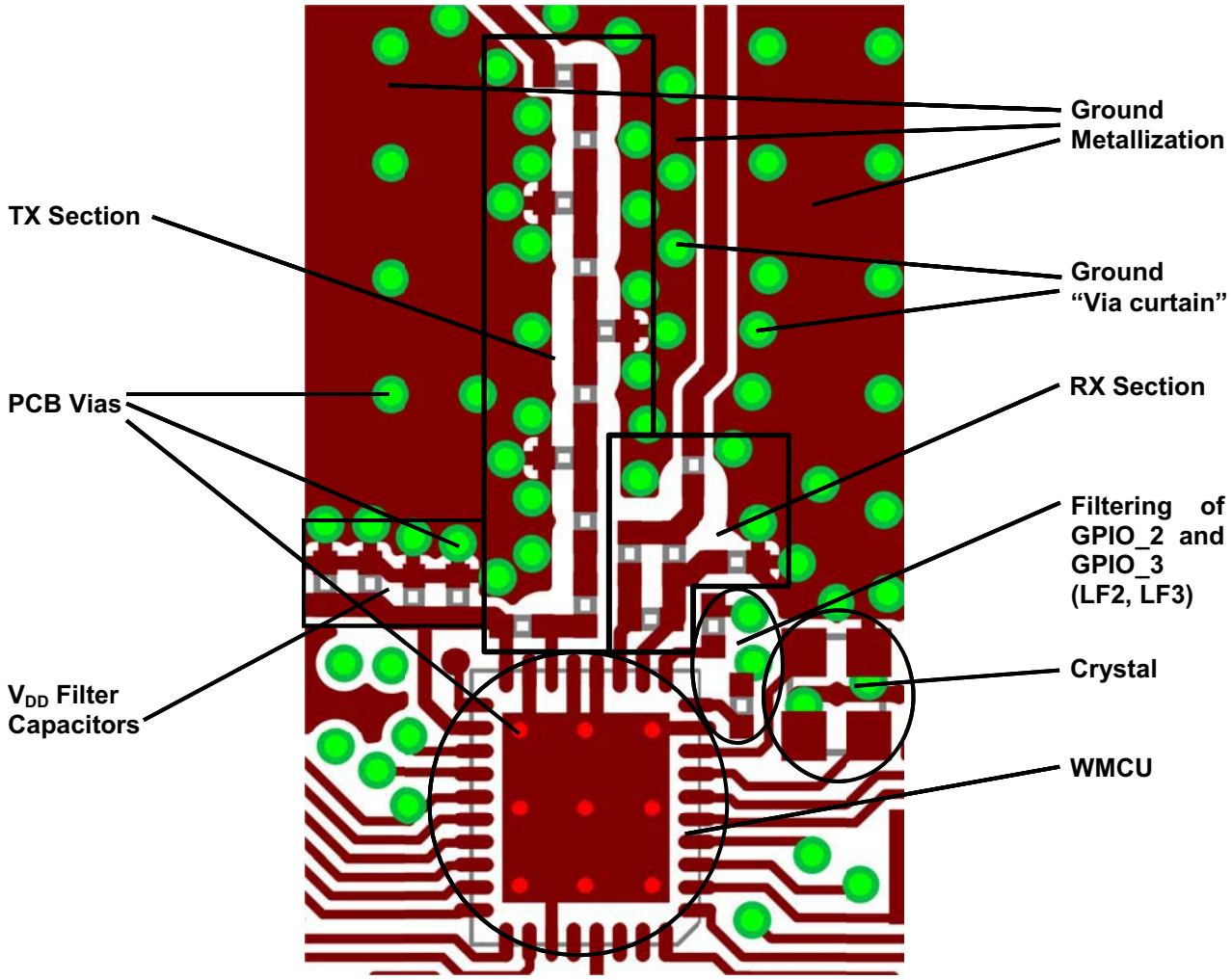


Figure 3. Layout Structure of the CLE Split TX/RX Type Matching Network for the Si1060/61/80/81

3.1.1. Layout Design Guidelines

- The L0 inductor should be placed as close to the TX pin of the RF IC as possible (even if this means the RX is further away) in order to reduce the series parasitic inductance which increase the voltage peak at the internal drain pin.
- The TX and RX sections should be separated as much as possible on the top layer to reduce coupling. If the available space allows flow the GND metal between them and use many vias.
- The neighboring matching network components should be placed as close to each other as possible in order to minimize any PCB parasitic capacitance to the ground and the series parasitic inductances between the components.
- Improve the grounding effect in the thermal straps used with capacitors. In addition, thicken the trace near the GND pin of these capacitors. This will minimize series parasitic inductance between the ground pour and the GND pins. Additional vias placed close to the GND pin of capacitors (thus connecting it to the bottom layer GND plane) will further help reduce these effects.
- Place the GND connections of the filter capacitors far from each other to reduce the level of harmonics coupling back to the TX path through them. For example by grounding at different sides of the TX line.

Figure 4 demonstrates the positioning and orientation of the LC and LR components, the separating GND metal between the TX and RX sections, and thermal strapping on the shunt capacitors on the 1060-PCE20B915 Pico Boards.

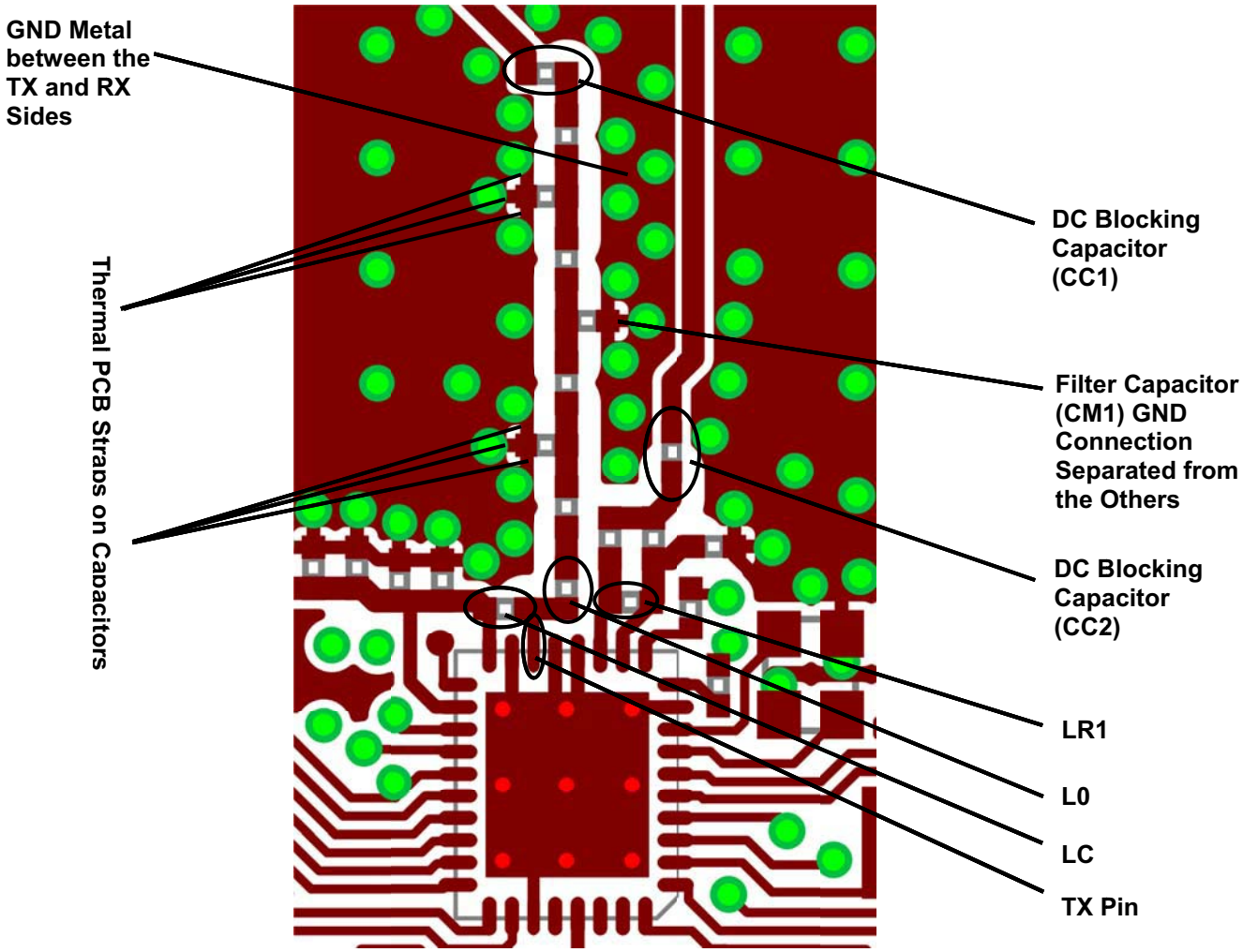


Figure 4. Component Orientation, Placement, and GND Metallization

- The smaller VRF bypass capacitors (C1 and C2) should be kept as close to the VDD_RF pin as possible.
- The exposed pad footprint for the paddle of the RF IC should use as many vias as possible to ensure good grounding and heatsink capability. In the reference designs there are 9 vias, each with 12 mil diameter. The paddle ground should also be connected to the top layer GND metal, if possible, to further improve RF grounding; this may be accomplished with diagonal trace connections through the corners of the RFIC footprint.
- The crystal should be placed as close to the RFIC as possible to ensure wire parasitic capacitances are kept as low as possible; this will reduce any frequency offsets that may occur.
- Use at least 0.5 mm separation between traces/pads to the adjacent GND pour in the areas of the matching networks. This will minimize the parasitic capacitance and reduce the detuning effects.
- If space allows the nearby inductors of the TX path should be kept perpendicular to each other to reduce coupling between stages of the low pass filter and match. This will help to improve filter attenuation at higher harmonic frequencies.
- If space allows the parallel inductor in the RX path (LR) should be perpendicular to the nearby inductors in the TX path as this will reduce TX to RX coupling.

Figure 5 demonstrates the grounding of the RFIC, the crystal and VRF filter capacitor positions, and the isolating ground metal between the VRF trace and the crystal on the 1060-PCE20B915 Pico Boards.

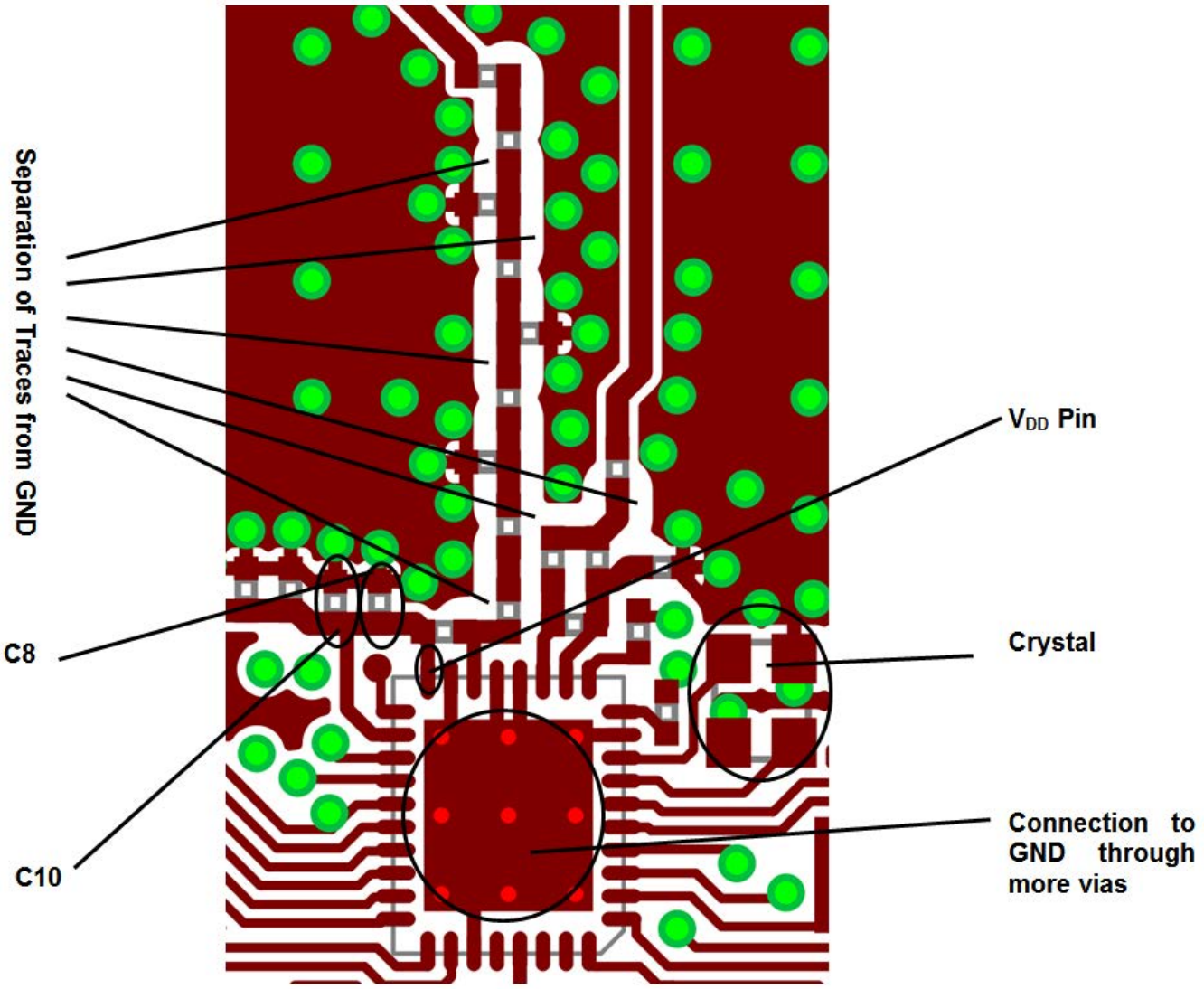


Figure 5. RFIC GND Vias and GND Metallization

- To achieve good RF ground on the layout it is recommended to add large, continuous GND metallization on the top layer in the area of the RF section (at a minimum). Better performance may be obtained if this is applied to the entire PCB. To provide a good RF ground, the RF voltage potentials should be equal along the entire GND area as this helps maintain good VRF filtering and also provides a good ground plane for a monopole antenna. Gaps should ideally be filled with GND metal and the resulting sections on the metal layers should be connected with as many vias as possible.
- The area under the matching network (on the next layer under the top) should be filled with ground metal as it will help reduce/remove radiation emissions. Board routing and wiring should not be placed in this region to prevent coupling effects with the matching network. It is also recommended that the GND return path between the GND vias of the TX LPF/Match and the GND vias of the RFIC paddle should not be blocked in any way; the return currents should see a clear unhindered pathway through the GND plane to the back of the RFIC.
- Use as many parallel grounding vias at the GND metal edges (especially at edge of the PCB and along the VRF trace) in order to reduce their harmonic radiations caused by the fringing field as possible.

- In a four-layer design at least the traces of the RF section and especially the VRF line should be placed in one of the inner layers (better if all the traces are routed on inner layers), and the entire top and bottom layers should contain as large and continuous GND metallization as possible.
- If necessary shielding cap can be used to shield the harmonic radiations of the PCB, in that case the shielding cap should cover all of the RF-related components. Shielding cap is usually required for the +20dBm 915MHz Si1060/61/80/81 designs, due to the strict harmonic radiation limits of the FCC.

Figure 6, Figure 7 and Figure 8 demonstrate the GND metal filled sections on the entire 1060-PCE20B915 Pico Board PCB. The top, inner2, inner3 and bottom layers are shown, respectively.

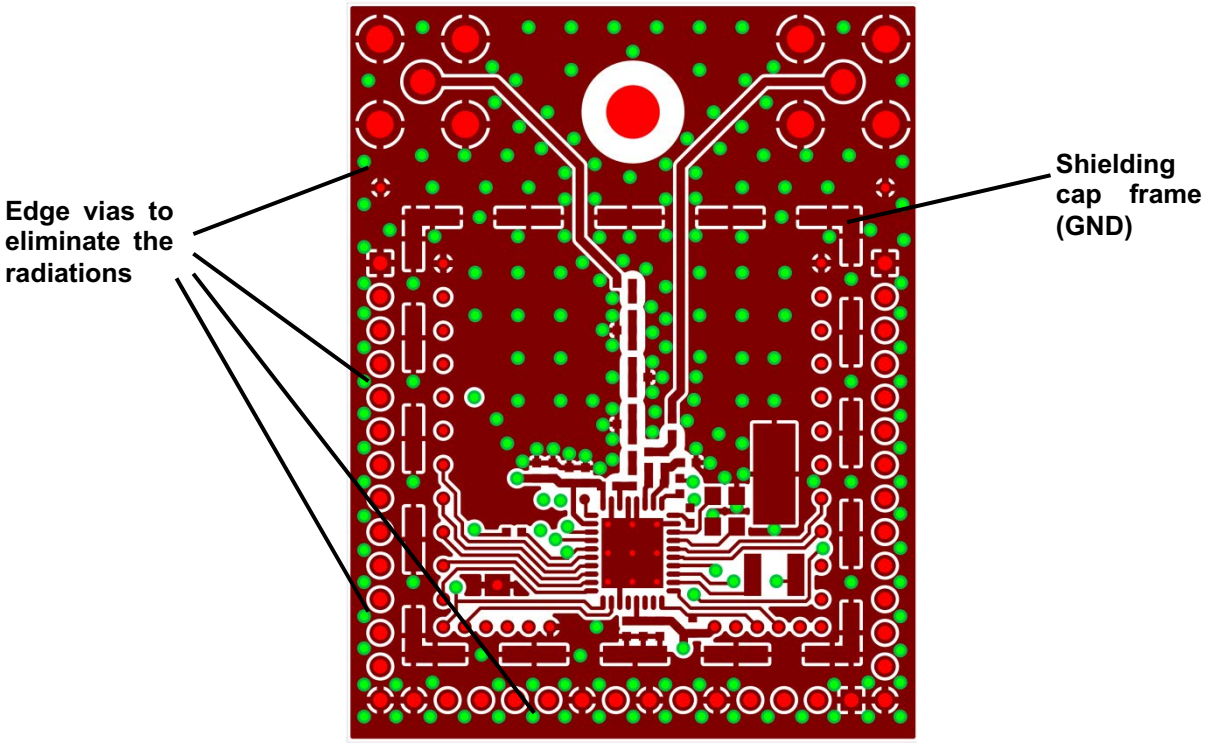


Figure 6. Ground Poured Sections with PCB Vias around the Matching Network; Top Layer

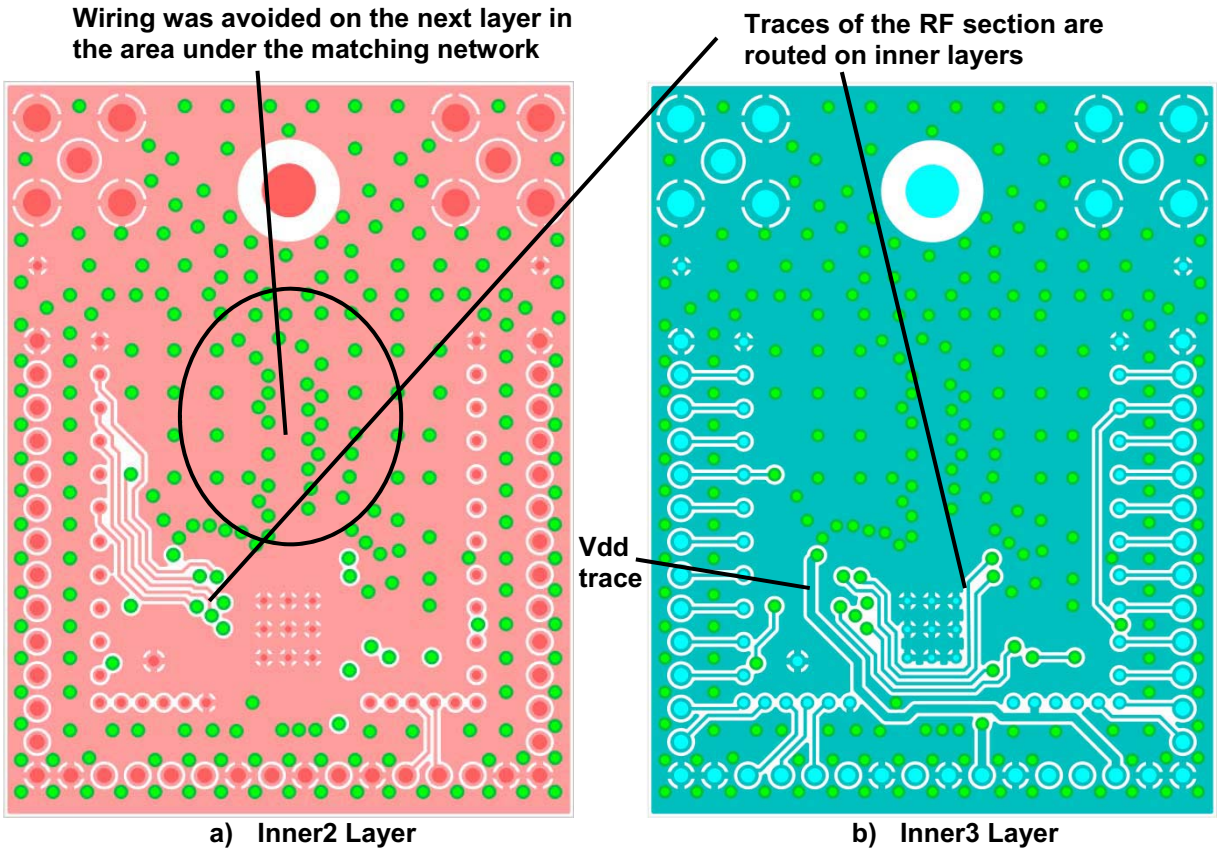


Figure 7. Ground Poured Sections with PCB Vias; Inner Layers

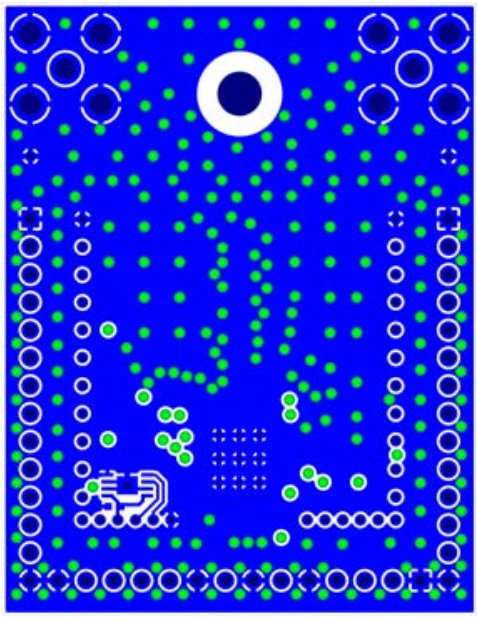


Figure 8. Ground Poured Sections with PCB Vias: Bottom Layer

- Use 50 Ω grounded coplanar lines where possible for connecting the SMA connector(s) to the matching network and/or the RF switch to reduce sensitivity to PCB thickness variation. This will also reduce radiation and coupling effects. The interconnections between the elements are not considered as transmission lines as their lengths are much lower than the wavelength and thus their impedance is not critical. As a result, their recommended width is the smallest possible (i.e. equal to the width of the pad of the applied components). By this way the parasitic capacitances to the ground can be minimized. In case of the 1060-PCE20B915 type Pico Board, the only route where 50 Ω coplanar transmission line is used is between the output of the matching networks and the SMA connectors. An example for the trace dimensions is shown in Table 1.
- Use many vias near to the coplanar lines in order to reduce its radiation as possible

Figure 9 demonstrates the 50 Ω grounded coplanar line of the TX side on the 1060-PCE20B915 Pico Boards.

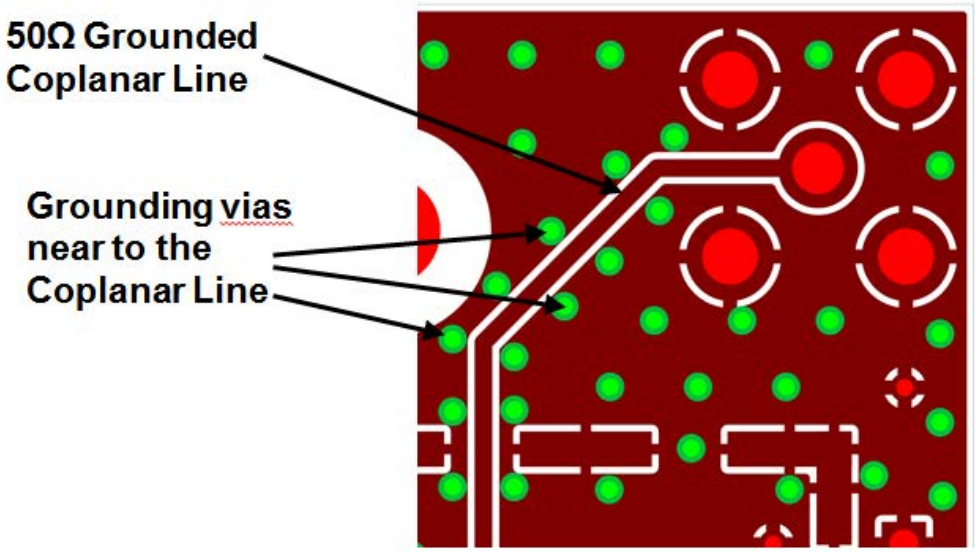


Figure 9. 50Ω Grounded Coplanar Line for 0.4 mm Substrate Thickness

Table 2. Parameters for 50 Ω Grounded Coplanar Lines

f	119–1050 MHz
T	0.018–0.035 mm
Er	4.6
H	0.4 mm*
G	0.2 mm
W	0.5 mm
Note: In case of the 4-layer PCBs, the thickness between the top and the next inner layer should be taken into account.	

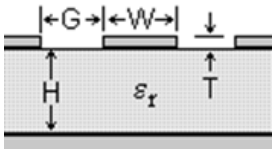


Figure 10. Grounded Coplanar Line Parameters

3.2. Class E Direct Tie Type Matching Network Layout Based (Single Antenna without RF Switch)

For reference, layout examples shown in this section are based upon the layout of the 1062-PCE13D868 RF Pico Boards. These boards contain one single antenna and the TX and RX paths are connected directly together, without use of an RF switch.

The schematic of the CLE Direct Tie type matching network for the Si106x/8x is shown in Figure 11.

During TX mode operation the built-in LNA protection circuit turns on (see AN627 for more details). In this case the dc path from the output of the matching network to the GND is not blocked through the RX side so a dc blocking capacitor (CC1) is necessary.

In case of the Direct Tie type matching, the coupling between the RX and TX sides is not critical since no harmonic leakage through the coupled RX path occurs as both of them are filtered after the common connection point.

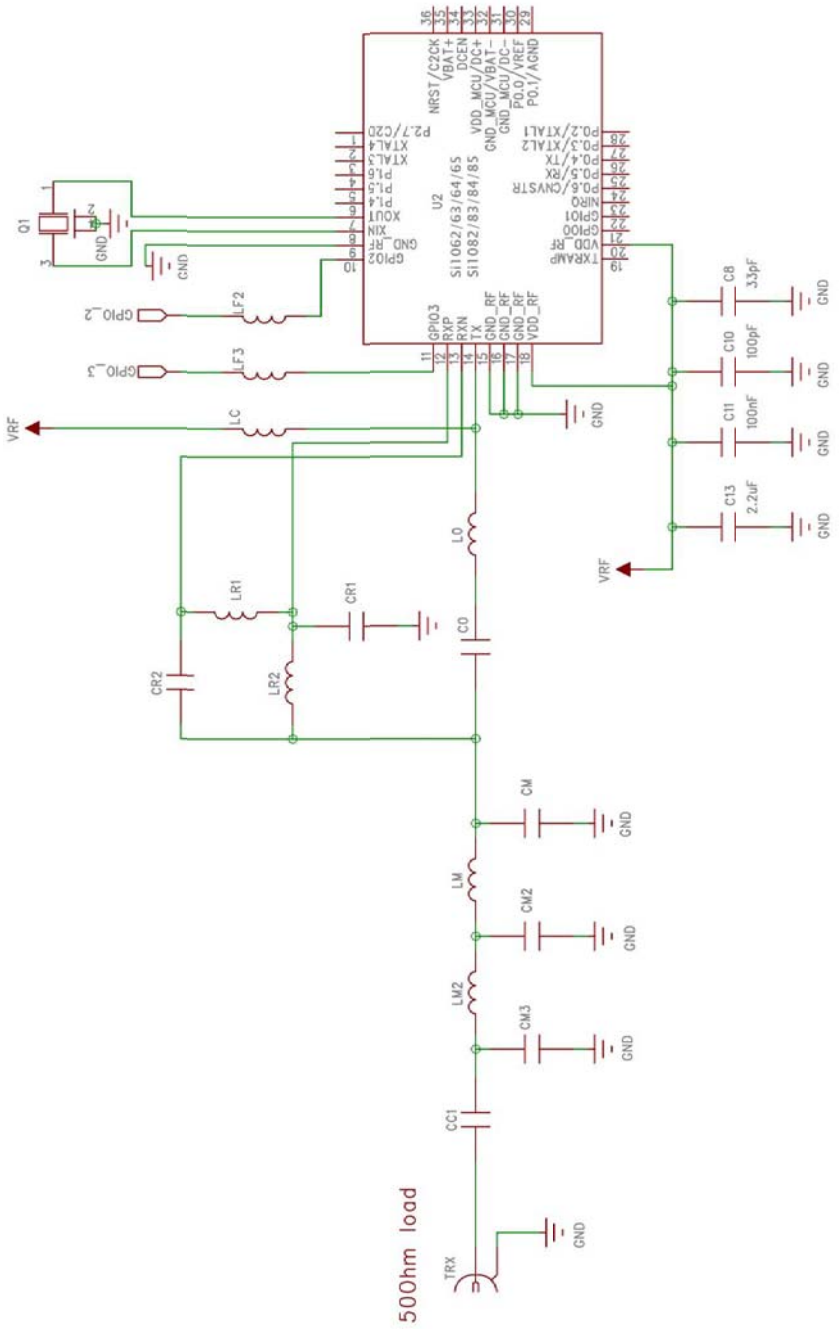


Figure 11. Schematic of the CLE Direct Tie Type Matching Network for the Si1062/63/64/65/82/83/84/85

Component values should be chosen based on frequency band, using AN627: Si4460/61 Low-Power PA Matching as a guideline.

3.2.1. Layout Design Guidelines

The principles in this case are the same as in the case of the Class-E Split TX/RX type matching except for the following issues:

- The trace parasitics are very critical in case of the connection of LR2 so the shortest traces possible should be used for connecting LR2 to the TX side.
- Since the RX-TX coupling is not critical, there isn't any separating GND metal between the two sides.

Figure 12 demonstrates the positioning and orientation of components and ground pour flooding on the 1062-PCE13D868 RF Pico Boards.

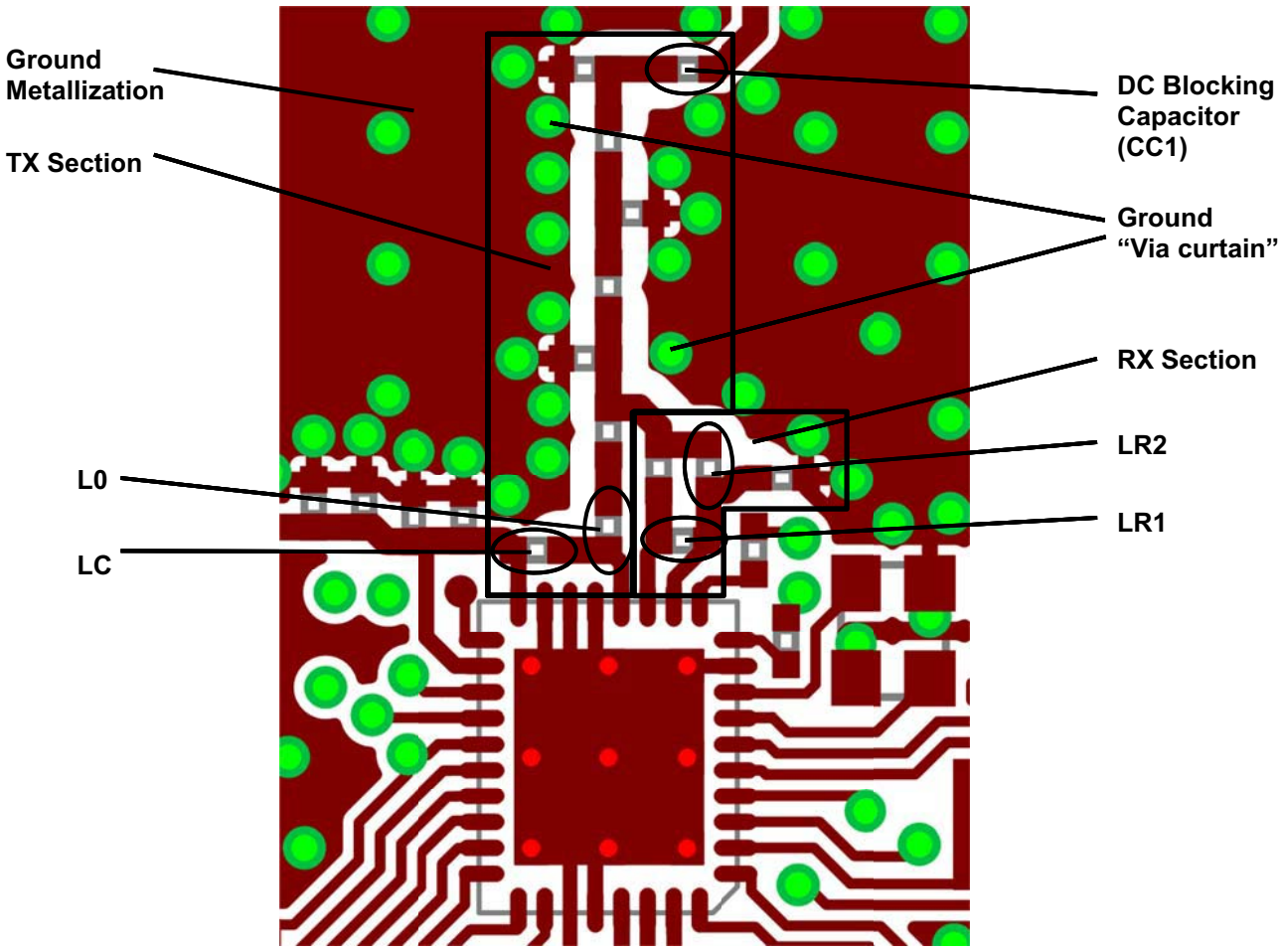


Figure 12. Layout of the Si1062/63/64/65/82/83/84/85 CLE Direct Tie Type Matching; Component Orientation, Placement and GND Metallization

3.3. Class E Switched Type Matching Network Layout (Single Antenna with RF Switch)

For reference, examples shown in this section are based upon the layout of the 1060-PCE20C915 RF Pico Boards. These boards contain a single antenna and an RF switch to select between the TX and RX paths. The schematic of the Switch type matching network for the Si1060/61/80/81 is shown in Figure 13.

The unavoidable nonlinearity of the RF switch will itself generate some harmonic energy as the desired signal frequency passes through it. It is recommended to place some of the low-pass filter circuitry after the RF switch to

attenuate these additional harmonic components. Thus the matching topology for the Single Antenna with RF Switch board configuration is comprised of two small lowpass filter sections with the RF switch embedded between them.

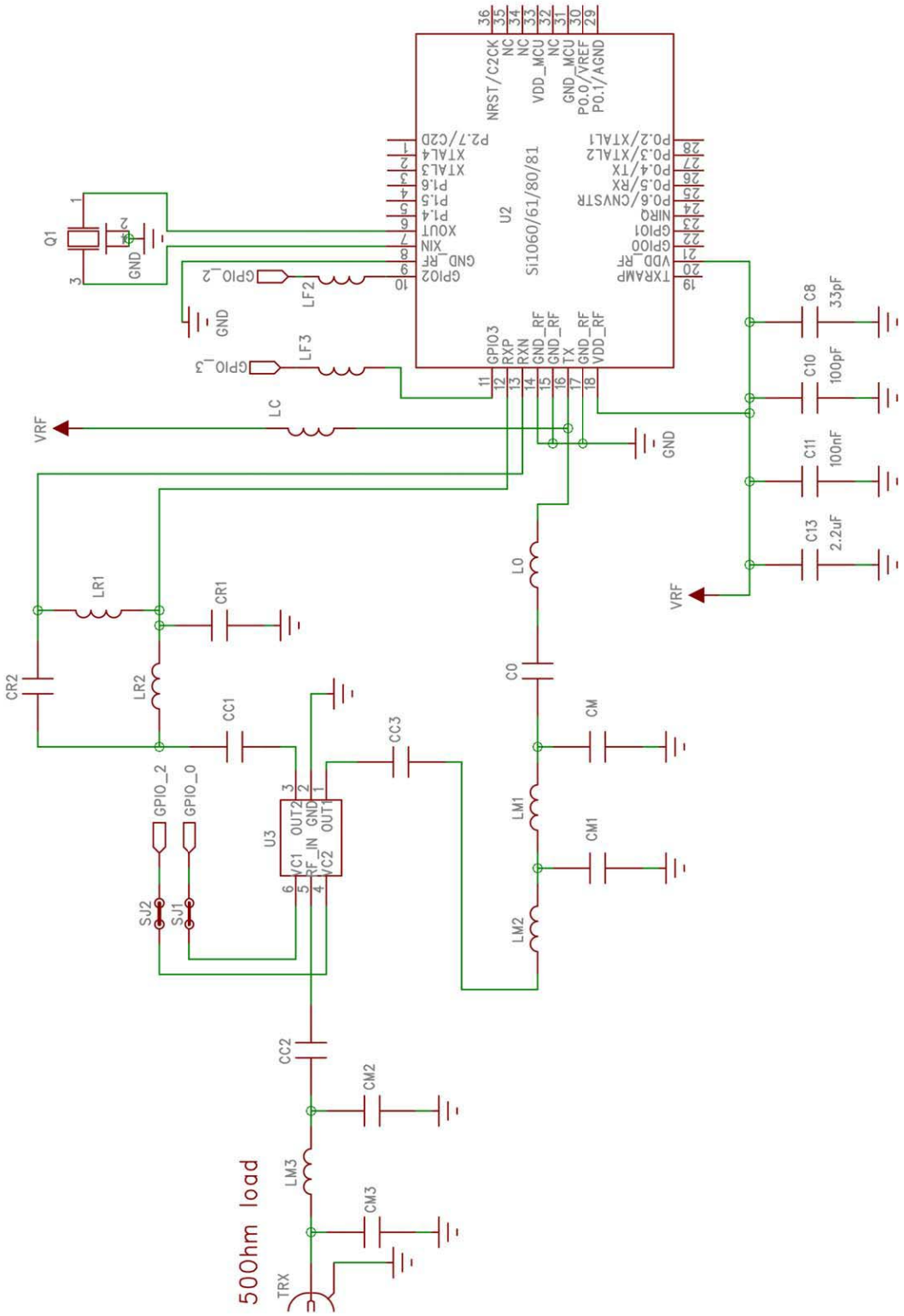


Figure 13. Schematic of the CLE Switch TX/RX Type Matching Network for the Si1060/61/80/81

Component values should be chosen based on frequency band, using AN648:Si4463/4464 TX Matching as a guideline.

3.3.1. Layout Design Guidelines

- When using a TX/RX switch, or a switch to select antennas in an antenna diversity implementation, a series capacitor may be required on all ports (e.g., TX, RX, Antenna) of the switch to block the dc patch between the switch and the ground. Refer to the exact requirements and specifications of the switch used in the application.
- As mentioned before, RF switches may themselves behave in a slightly non-linear fashion, resulting in some re-generation of harmonic energy regardless of the cleanliness of the input signal to the switch. Thus it may be necessary to move a portion of the TX lowpass filter to ***after*** the RF switch (i.e., just prior to the antenna) in order to further attenuate these re-generated harmonic signals.
- If the RX side matching network is relatively far from the RF switch then the connecting trace should be a 50Ω grounded coplanar line.
- The area between the RX and TX sides should be filled with GND metal to increase the isolation (just as in case of the Split type design).

Figure 14 demonstrates the positioning and orientation of components, ground flooding, and thermal strapping on the 1060-PCE20C915 RF Pico Board.

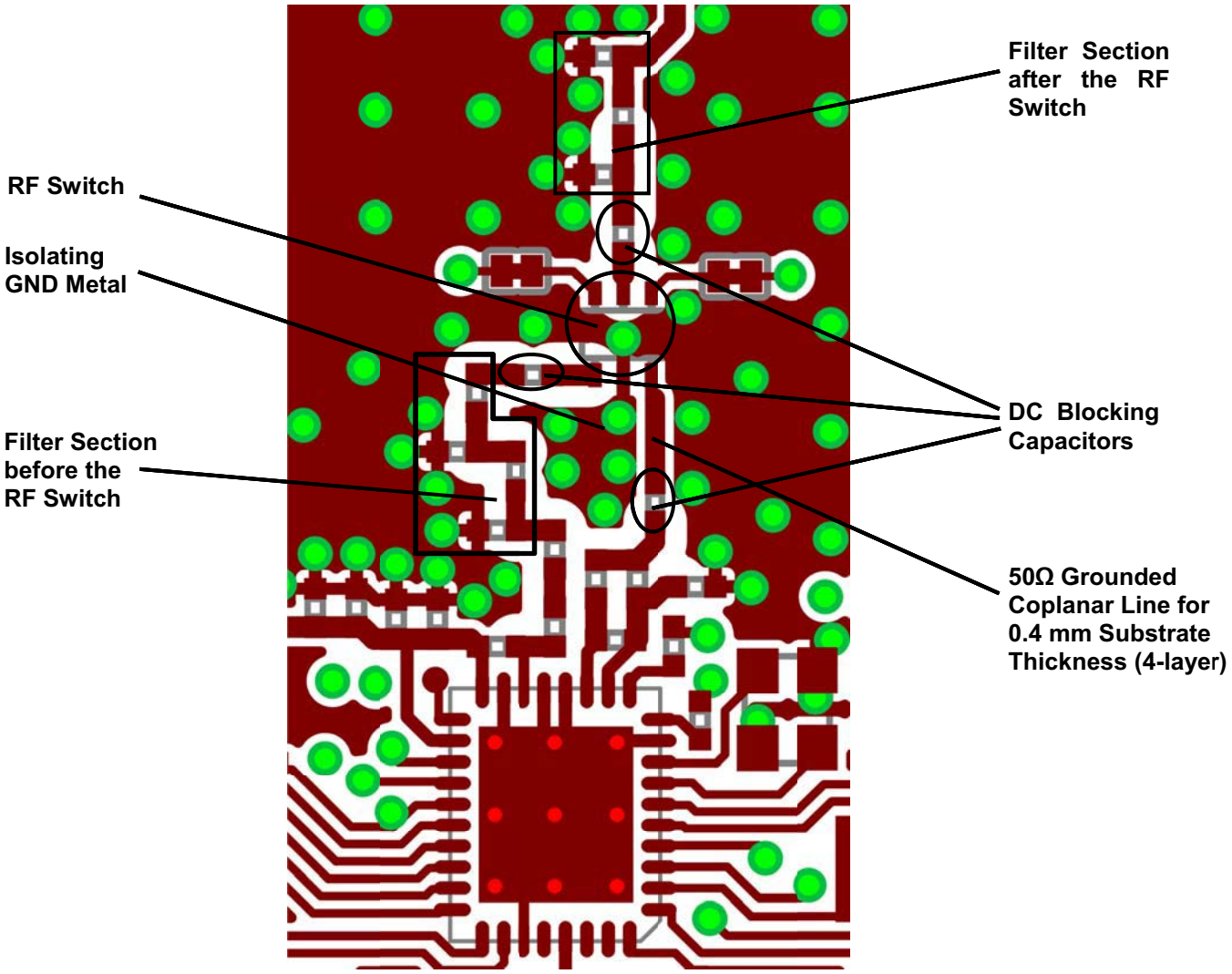


Figure 14. Layout of the Si1060/61/80/81 CLE Switch Type Matching; Component Orientation, Placement, and GND Metallization

3.4. Square-Wave Direct Tie Type Matching Network Layout (Single Antenna without RF Switch)

For reference, layout examples shown in this section are based upon the layout of the 1060-PSQ20D169 RF Pico Boards. These boards contain one single antenna and the TX and RX paths are connected directly together, without use of an RF switch.

The schematic of the SQW Direct Tie type matching network for the Si1060/61/80/81 is shown in Figure 15.

During TX mode operation the built-in LNA protection circuit turns on (see AN648 for more details). In this case the dc path from the output of the matching network to the GND is not blocked through the RX side so a dc blocking capacitor (CC1) is necessary.

In case of the Direct Tie type matching, the coupling between the RX and TX sides is not critical since no harmonic leakage through the coupled RX path occurs as both of them are filtered after the common connection point.

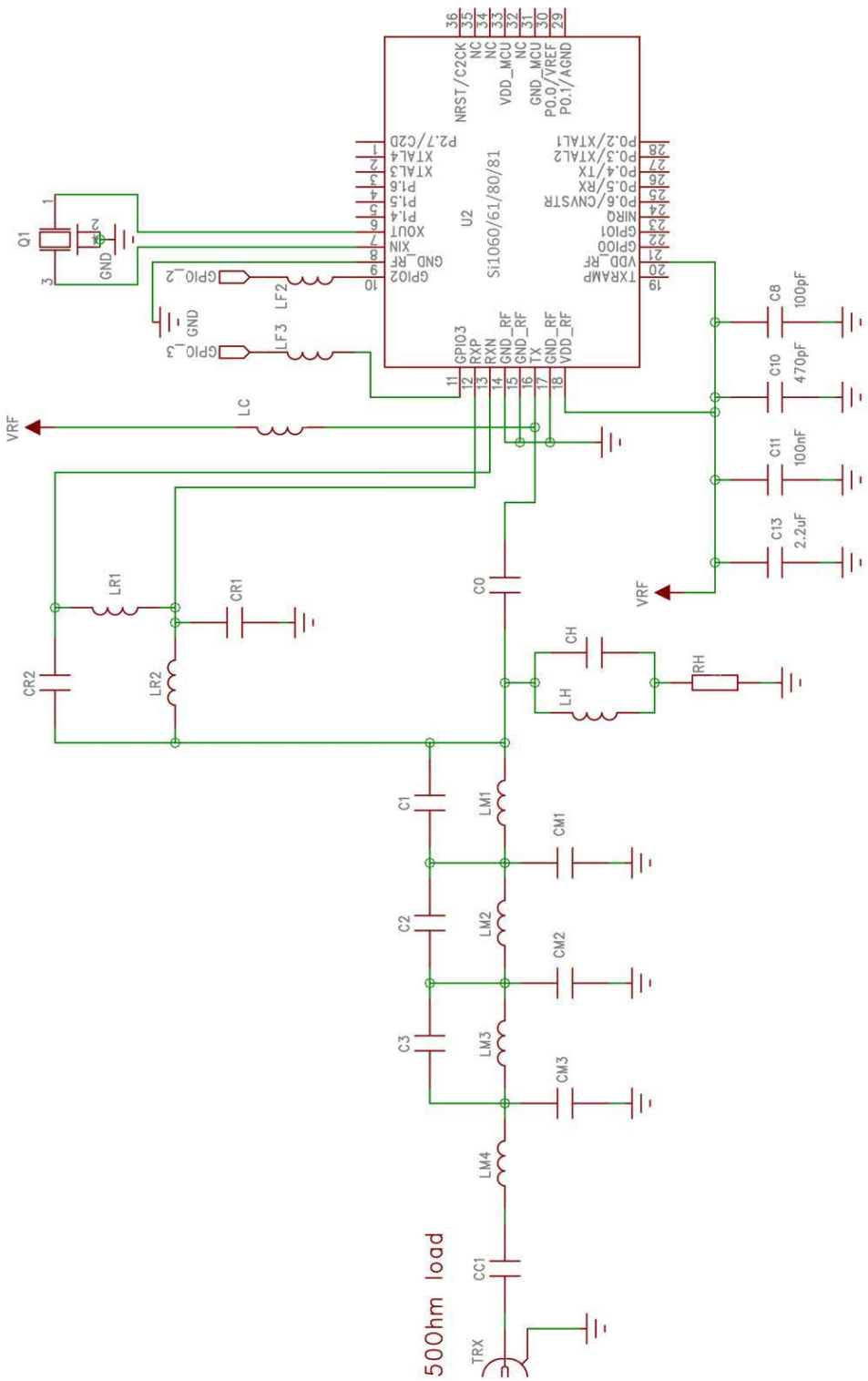


Figure 15. Schematic of the Square-Wave Direct Tie Type Matching Network for the Si1060/61/80/81

Component Values should be chosen based on frequency band, using AN648: Si4463/4464 TX Matching as a guideline.

3.4.1. Layout Design Guidelines

Figure 16 demonstrates the positioning and orientation of components and ground pour flooding on the 1060-PSQ20D169 RF Pico Board.

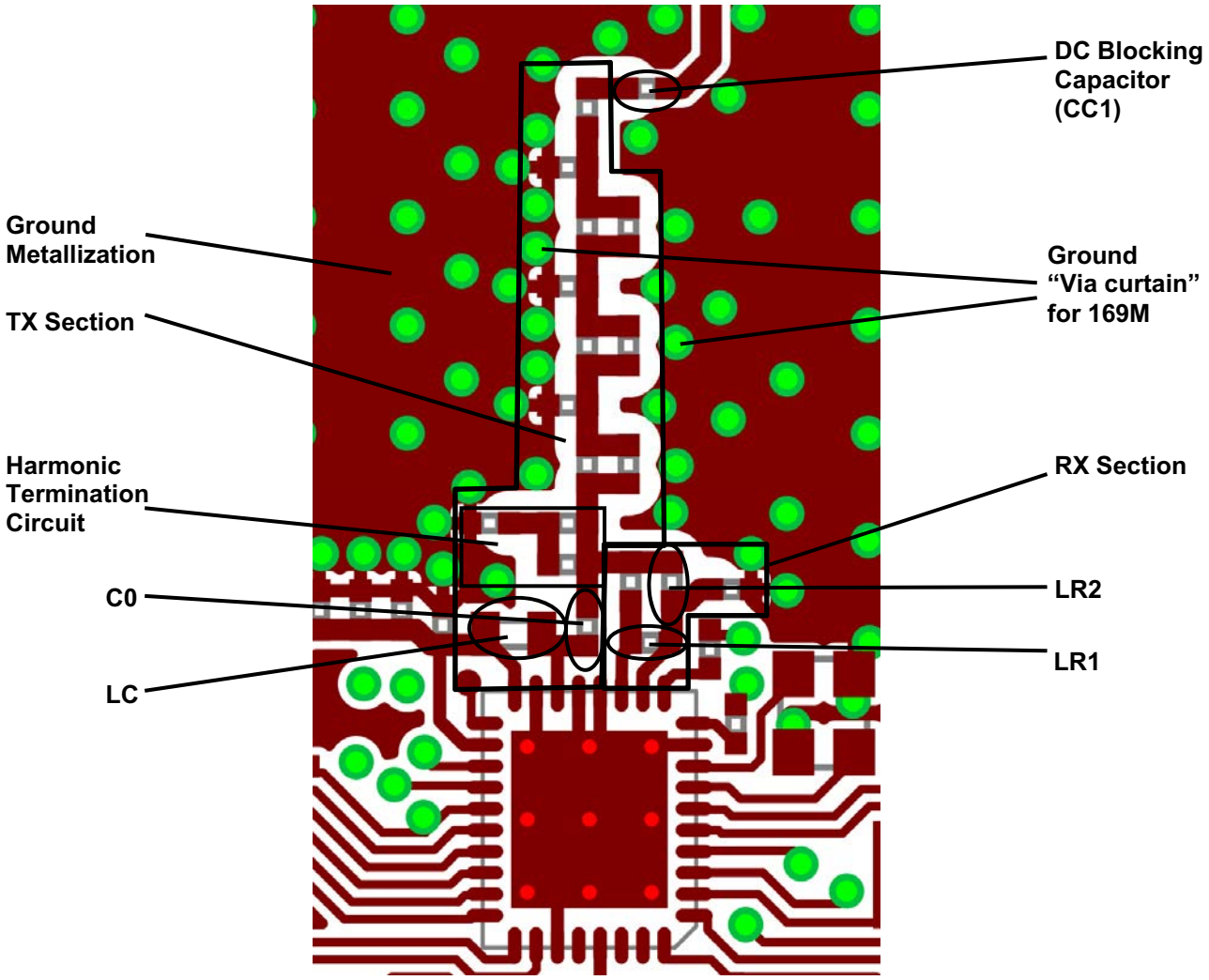
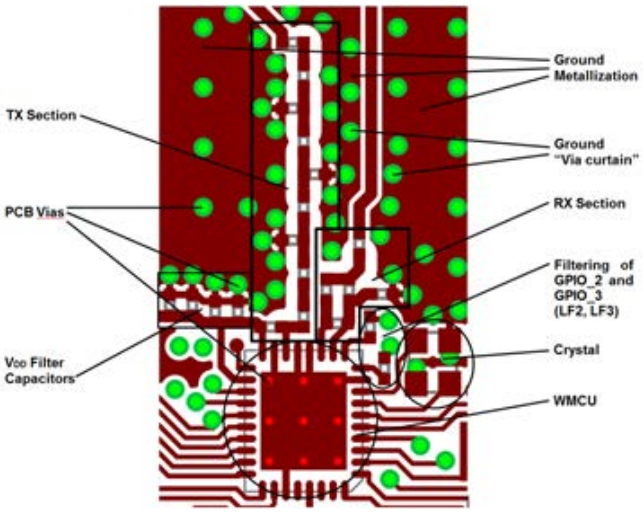
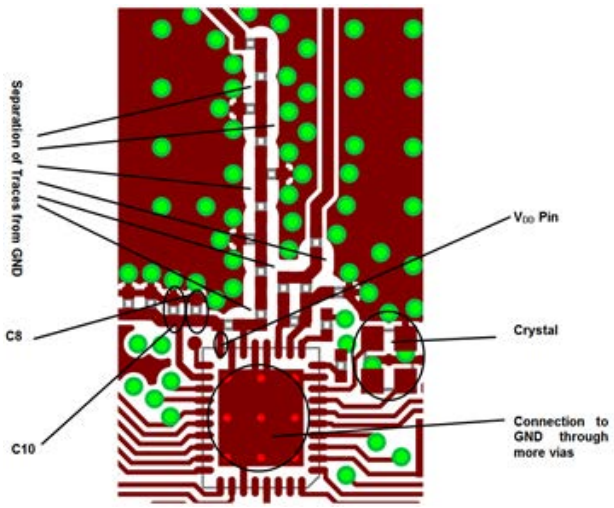
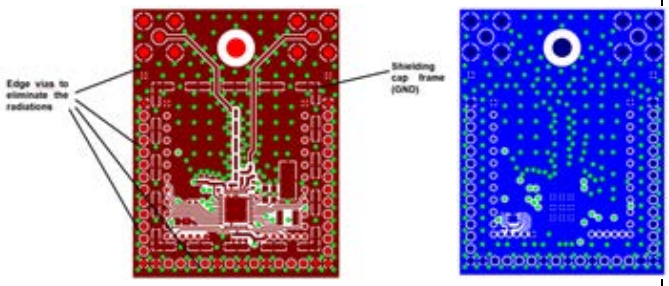


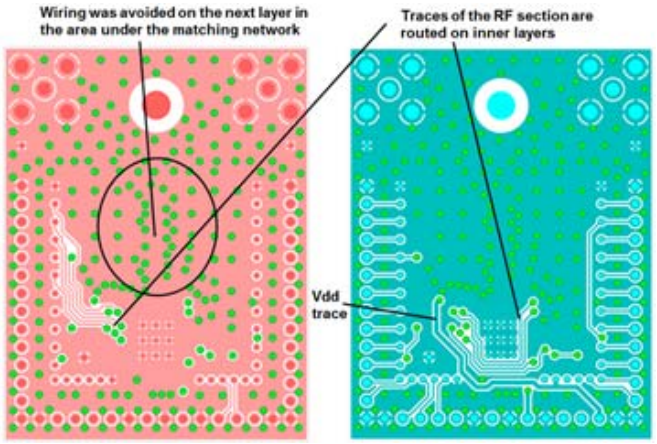
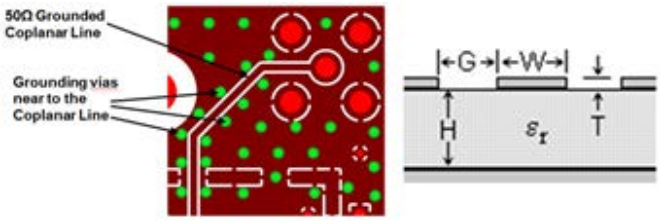
Figure 16. Layout of the Si1060/61/80/81 SQW Direct Tie Type Matching; Component Orientation, Placement, and GND Metallization

4. Checklist for an RF PCB Design

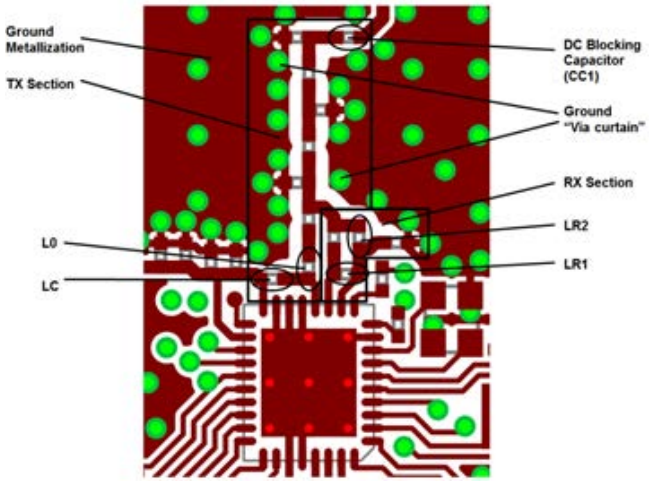
4.1. Main Layout Design Principles

1.	☐	Is the choke inductor (LC) as close to the TX pin as possible?	
2.	☐	Is the RX parallel inductor (LR) perpendicular to the choke inductor (LC) in the TX path? (except for the Direct Tie type matching)	
3.	☐	Are the TX and RX separated by a ground metal on the top layer? (except for the Direct Tie type matching)	
4.	☐	Are the neighboring matching network components as close to each other as possible?	
5.	☐	Are there more thermal straps used with the capacitors?	
6.	☐	Are the TX path inductors perpendicular to each other?	
7.	☐	Do the TX path capacitors have separated GND connection?	
8.	☐	Do the GPIO_2 and GPIO_3 lines have filtering?	

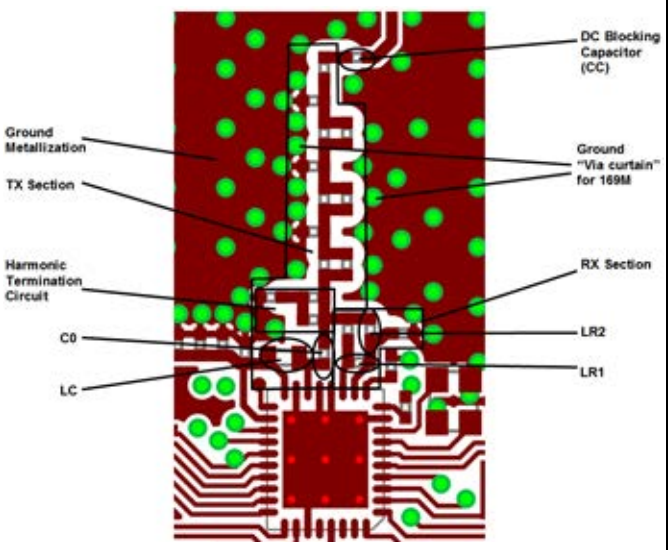
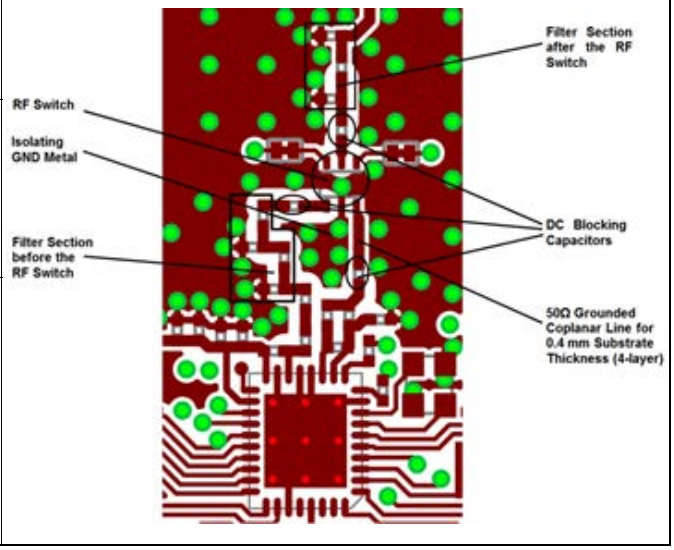
9.	☐	Is there at least 0.5 mm separation in the matching between the traces/pads and the GND metal?	
10.	☐	Are the smallest value V_{RF} filter capacitors kept closer to the V_{RF} pin of the RF IC?	
11.	☐	Does exposed pad footprint use more vias?	
12.	☐	Is the crystal as close to the RF IC as possible?	
13.	☐	Does ground metal exist between the crystal and the V_{RF} feed?	
14.	☐	Was large, continuous GND metallization added to at least the RD sections?	
15.	☐	Are the GND metal edges closed by a “via curtain” where possible, with a via distance less than lambda/10 of the highest (usually 10th) critical harmonic frequency?	
16.	☐	Was the area on the next layer under the matching network filled with GND metal and was wiring and routing avoided in this region?	

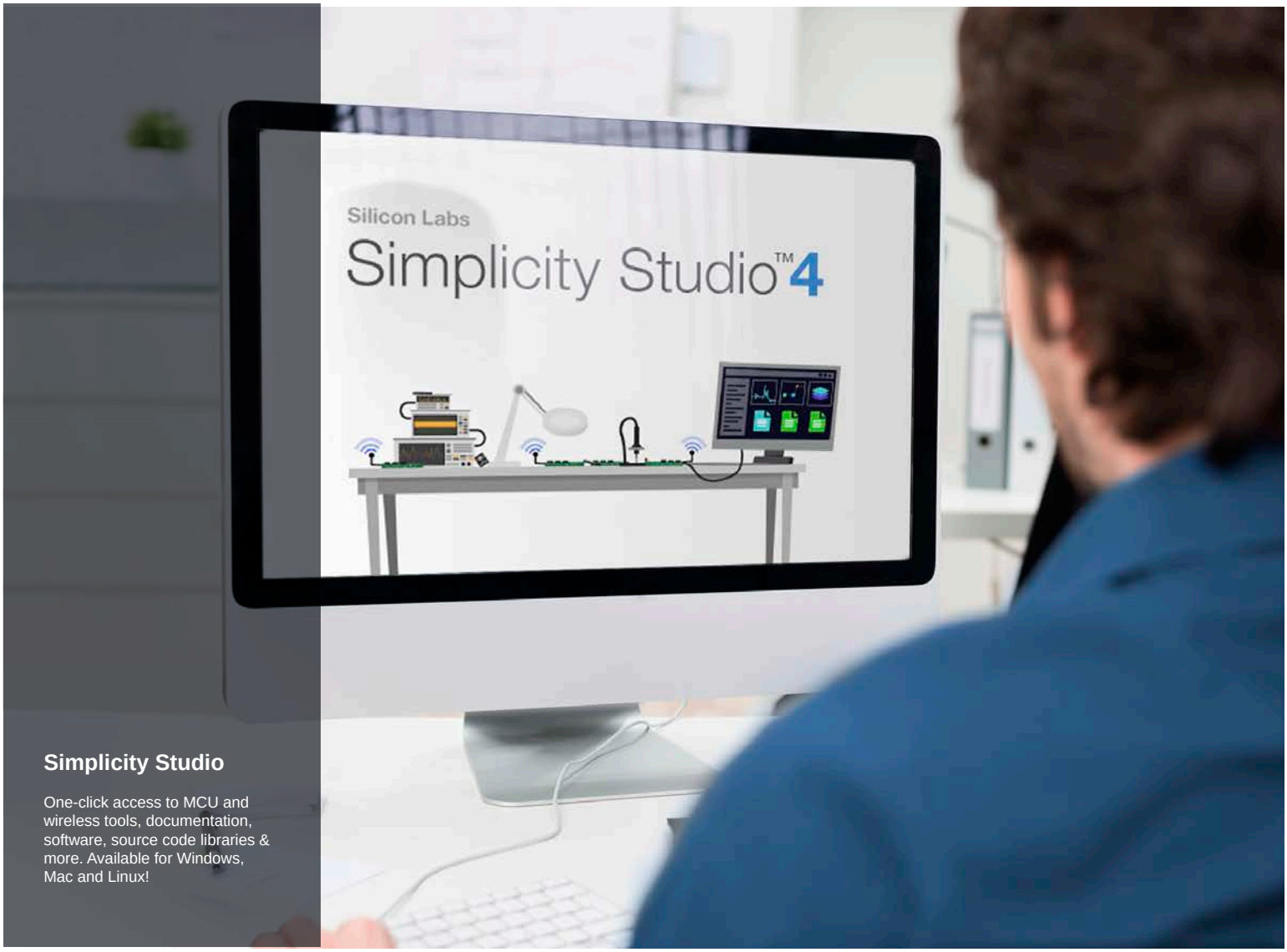
17.	☐	In case of 4-layer PCB were the V_{RF} and at least the traces of the RF section routed on inner layers?	
18.	☐	Were 50Ω grounded coplanar lines used for connecting the matching network, the switch and/or the SMA connector(s)?	

4.2. Additional Concerns for the Direct Tie Type Matching

19.	☐	Is the length of the trace connecting of the RX and TX sides minimal?	
20.	☐	Is LR2 connected with as short traces as possible?	
21.	☐	Is an additional dc blocking capacitor added to the output of the matching network to block the dc path in RX mode?	

4.3. Additional Concerns for the SQW and the Switch and Diversity Type Matchings

22.	☐	Was the additional harmonic termination circuit added into the TX path in case of SQW matching?	
23.	☐	Were series capacitors added to the TX path to block the dc when a TX/RX switch (or Diversity switch) is used?	
24.	☐	Was 50W grounded coplanar line used for connecting the RX side matching to the RF switch (if they are far from each other)?	
25.	☐	Was the area between the RX and TX sides filled with GND metal/	



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