

A Microwatt Charge Pump Boosts 1 V to 1.8 V at 90% Efficiency, Providing “Always On” Standby Power for Microcontrollers

1. Introduction

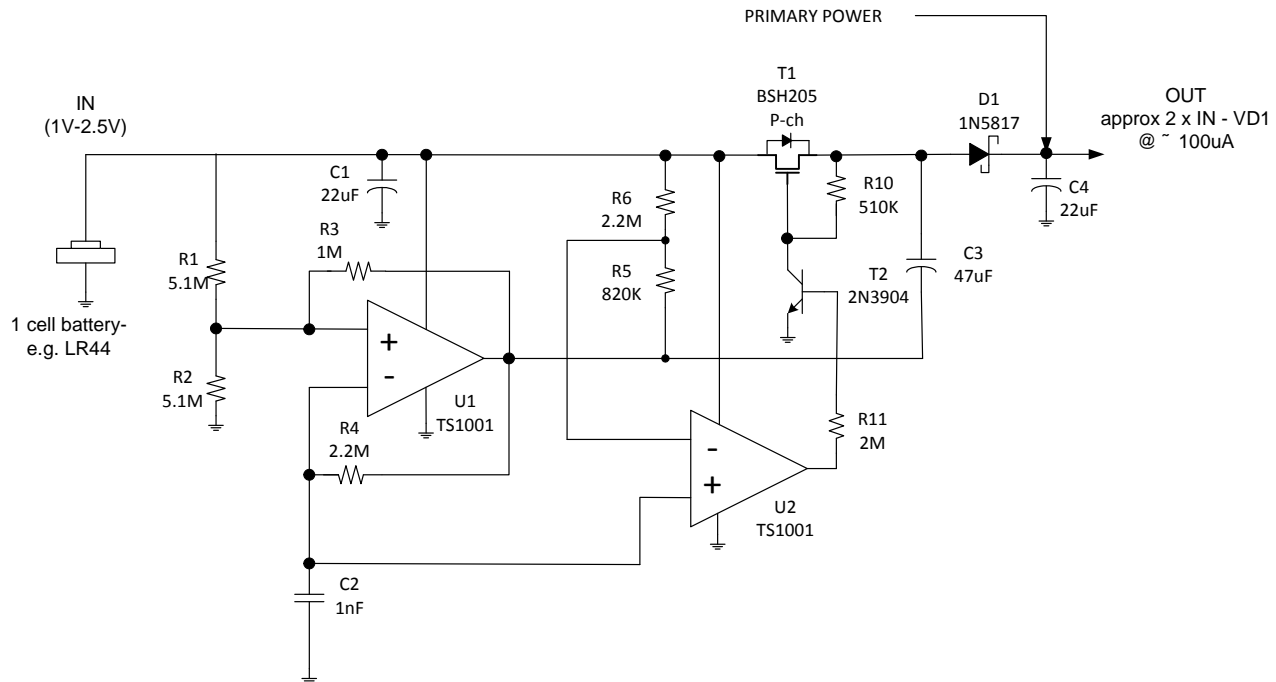


Figure 1. MicroWatt Charge Pump

Boosting the output voltage of common alkaline button-cells to at least 1.8 V needed by microcontrollers provides an “always on” standby power source sufficient for low-power oscillator interrupt/sleep state operation. Two ultra-low power op amps are used in a charge pump configuration to double an input voltage, creating an output voltage of approximately 2x the input voltage. Output currents up to 100 μ A are available at 90% efficiency; even load currents as low as 10 μ A achieve 80% efficiency, beating commercially available charge pump ICs and inductor-based boost regulators.

2. Overview

When the microcontroller wakes, primary power may be fed in at diode-or point at C4 from a separate power supply capable of providing the full “on”-state power. In a typical scenario, an interrupt causing the microcontroller to wake also enables the primary supply, which may be an inductor-based boost regulator. This primary supply remains on as long as the microcontroller requires full power, and shuts down when the microcontroller goes to sleep, allowing the micropower charge pump to take over providing low power at high efficiency.

In very low duty-cycle systems, where the microcontroller spends the majority of its life sleeping, and waking only rarely to make measurements or respond to a stimulus, the low power sleep state current draw largely defines the battery life. Thus, the efficiency of the micropower boost regulator becomes critically important.

Referring to the figure above, op amp U1 is configured as a relaxation oscillator, serving as the master charge pump clock. Capacitor C2 charges and discharges primarily through resistor R4 to set the frequency, and U1’s output directly drives the bottom of flying capacitor C3 between IN and GND voltages. Amplifier U1, the 0.8 V/0.6 μ A TS1001 op amp, is particularly well-suited to the task, as it has the unusual combination of sub-microamp supply current, sub-1V operation, and reasonable output drive capability to charge C3.

Amplifier U2 is configured as a comparator slaved to the timing cycle established by U1, ensuring proper turn-on and turn-off timing for T1. T1, a low threshold P-channel MOSFET, turns on when U1's output is low, allowing C3 to charge to the voltage at IN; however, this timing is phased to ensure a clean break-before-make (T1 turns off before U1's output goes high, and doesn't turn on before U1's output is already low). This is accomplished by U2 switching based on the voltage of C2 at a different threshold than U1, set by R5, R6. NPN transistor T2 inverts the U2's output to drive the gate of T1, and isolates U2's output from the output voltage (U2's maximum supply voltage is 2.5V).

Flying cap C3 is dimensioned to shuttle charge between IN and OUT with a minimum voltage discharge even at slow charge pump frequencies to maximize efficiency. Similarly, output capacitor C4 must hold charge between cycles with the maximum load. At these low currents, leakage currents must be controlled because they directly affect efficiency, so compact surface-mount ceramic (not tantalum) capacitors should be used. Schottky diode D1 exhibits a 1uA reverse leakage; so the 1N5817 may be substituted with a lower leakage, higher forward-drop diode such as the BAT68 which doubles the forward drop but reduces leakage by an order of magnitude.

Button-cell battery terminal voltage is typically 1V-1.5V which would yield approximately 1.85V to 2.85V at the charge pump circuit's output (assuming D1 voltage drop is 150mV). This voltage level matches well the operating voltage range of typical microcontrollers (the Freescale MC9S08 series, for example, operates over a 1.8V – 3.6V range). Further, note that the typical terminal voltage of the button cell for the majority of its life is 1.2V, yielding 2.25V output from the charge pump circuit; thus accounting for the efficiency loss of dropping 2.25V to 1.8V still yields a net efficiency of $1.8V / 2.25V * 90\% = 72\%$, beating most existing commercial solutions.

In previous generations of discrete charge-pump based boost converters, conventional and low-power logic ICs have been used to create the charge pump clock. While many of these logic chips are designed for high speed, they exhibit substantial crossover currents at switchover times. While a few tens of microamps expended in such circuits may be acceptable in most circuits, in this slow charge pump circuit every microamp matters. Op amps, in contrast to logic gates and comparators, utilize linear output stages – slow, but no shoot-through supply-current spikes. See Figure 2. For additional information, see the TS1001 documentation.

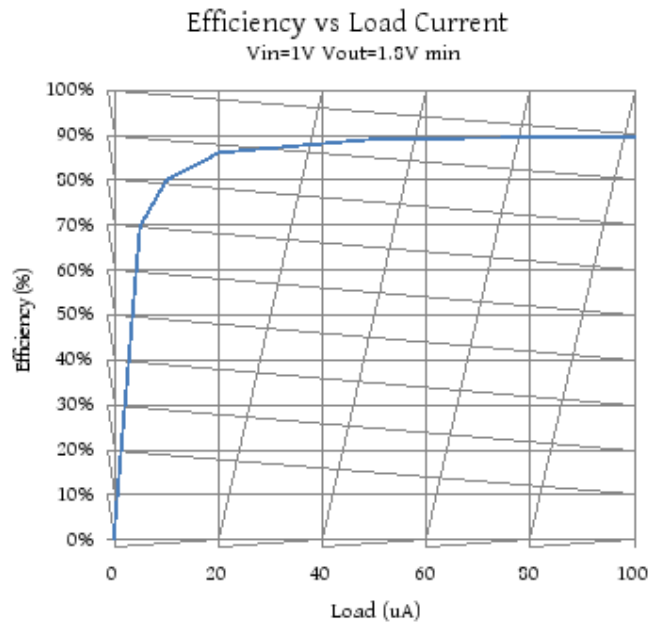
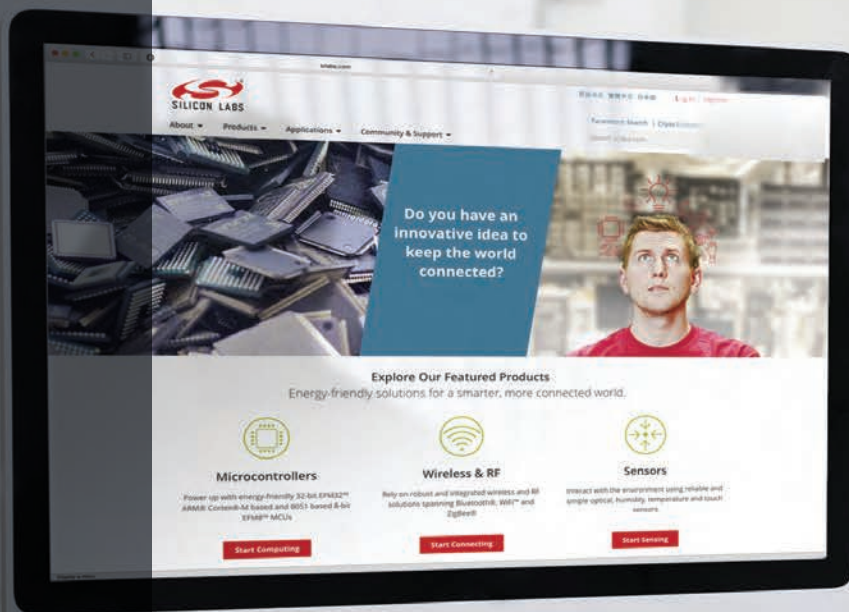


Figure 2. Ultra Low-power Op Amp-Based Charge-Pump Boost Converter Exhibits 90% Efficiency over a Wide Range of Load Currents



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