1. Introduction

The Si882xx/Si883xx products have integrated digital isolator channels with an isolated dc-dc controller. This application note provides guidance for selecting external components necessary for the operation of the dc-dc controller.

Digital isolation applications with primary side supply voltage $3.0 \, \text{V} \leq V_{\text{IN}} \leq 5.5 \, \text{V}$ and load power requirements of $\leq 2 \, \text{W}$ can use Si882xx/Si883xx products. These products’ dc-dc controller uses the asymmetric half bridge flyback circuit topology.

Figure 1 shows the minimum external components required for the asymmetric half bridge flyback. They are a blocking capacitor $C_1$, input capacitor $C_2$, flyback transformer $T_1$, diode $D_1$, output capacitor $C_{10}$, voltage sense resistors $R_5$ and $R_6$, and compensation network components $R_7$ and $C_{11}$.

![Figure 1. Minimum Required External Components](image-url)
2. Simplified DC Steady State Analysis

Analyzing the asymmetric half bridge behavior in DC steady state provides formulas to assist with selecting values for the components used in Figure 1. For this analysis, it is assumed that components are ideal, 100% efficiency (P\(_\text{IN}\) = P\(_\text{OUT}\)), and the circuit has reached equilibrium.

Figure 2 shows the critical components of the asymmetric half bridge flyback. The transformer model includes magnetizing inductance L\(_m\) and inductance leakage L\(_{lkg}\). R\(_\text{LOAD}\) does not necessarily represent a physical resistor, rather it is an expression of V\(_{\text{OUT}}\)/I\(_{\text{OUT}}\).

![Figure 2. Asymmetric Half Bridge Flyback Converter](image)

To analyze this architecture, a cycle can be divided into eight distinct operating modes. However, for DC steady state analysis, the two modes where the system operates the majority of the cycle are only required: when S1 is closed and S2 is open, and when S1 is open and S2 is closed. Figure 3 depicts the simplified magnetizing and leakage inductance current waveforms.

![Figure 3. Inductor Currents](image)
2.1. S1 Closed, S2 Open

\( V_{IN} \) is applied to the series combination of \( C_1 \) and inductance \( L_m + L_{lkg} \). As a result, current flows through inductance \( L_m + L_{lkg} \) in a linear fashion.

\[
V_{IN} - V_{C1} = (L_m + L_{lkg}) \times \frac{l_{m, RIPPLE}}{t_{S1}}
\]

Equation 1.

Where \( l_{m, RIPPLE} \) is the magnetizing current ramp during \( t_{S1} \) and \( t_{S1} \) is the time that S1 is closed.

2.2. S1 Open, S2 Closed

In this mode, a resonant tank circuit formed by \( C_1, L_m, \) and \( L_{lkg}, \) and \( -V_{C1} \) is applied across \( L_m + L_{lkg} \). The resonant tank causes the current through leakage inductance to rise as a sinusoid while the voltage at the secondary impressed on the primary causes the current through the primary to reduce in a linear fashion. When \( l_{lkg} \neq l_m \), the difference current \( (l_m - l_{lkg}) \) flows out of the dot on the primary side of the ideal transformer. Therefore current must flow into the dot on the secondary side and through the diode. Governing current equations are

\[
\frac{l_{m, RIPPLE}}{t_{S2}} = \frac{-V_{OUT}}{L_m N}
\]

Equation 2.

\[
l_{lkg}(t) = l_m \times \sin(\omega_r t)
\]

Equation 3.

\[
\omega_r = \frac{1}{\sqrt{L_{lkg} \times C_1}}
\]

Equation 4.

where \( N \) and \( t_{S2} \) are primary to secondary turns ratio and time that S2 is closed respectively. \( \omega_r \) is the resonance tank frequency in rads/s.

The current through the diode in the secondary can be written as the difference of \( l_{lkg} \) and \( l_m \) scaled by the transformer turns ratio.

\[
l_{D1} = \frac{l_m - l_{lkg}}{N}
\]

Equation 5.

As the sinusoidal current returns to match the magnetizing current, the resonance ceases and consequently no current will flow from the dot on the primary or through the secondary into the diode.

2.3. Voltage Transfer

Let duty cycle \( D \) be defined as the ratio of time S1 is closed over the complete switching period \( T_{SW} \):

\[
D = \frac{t_{S1}}{t_{S1} + t_{S2}}
\]

Equation 6.
Now $t_{S1}$ and $t_{S2}$ can be expressed in terms of $D$ and switching period as:

$$t_{S1} = DT_{SW}$$

**Equation 7.**

$$t_{S2} = (1 - D)T_{SW}$$

**Equation 8.**

and assume diode D1 has no voltage drop when conducting, the volt-second balance equation for $L_{lkg}$ can be written as:

$$\frac{L_{lkg}}{L_{lkg} + L_m} (V_{IN} - V_{C1}) DT_{SW} + \left(\frac{V_{OUT}}{N} - V_{C1}\right) (1 - D) T_{SW} = 0$$

**Equation 9.**

With the condition that $L_{lkg} \ll L_m$, Equation 9 simplifies to:

$$V_{C1} \approx \frac{V_{OUT}}{N}$$

**Equation 10.**

The volt-second balance equation for $L_m$ is:

$$\frac{V_{OUT}}{N} (1 - D) T_{SW} + \frac{L_m}{L_{lkg} + L_m} (V_{IN} - V_{C1}) DT_{SW} = 0$$

**Equation 11.**

With the condition that $L_{lkg} \ll L_m$, Equation 11 simplifies to:

$$\frac{V_{OUT}}{N} (1 - D) \approx (V_{IN} - V_{C1}) D$$

**Equation 12.**

Substituting Equation 10 into Equation 12 yields the following relationships:

$$\frac{V_{OUT}}{N} \approx V_{IN} D$$

**Equation 13.**

$$V_{C1} \approx V_{IN} D$$

**Equation 14.**
2.4. Magnetizing Current

If during the \( t_{S1} \) portion of the cycle (S1 closed, S2 open), \( V_{IN} \) charges \( C1 \) in a linear fashion. Rearranging Equation 1 and substituting Equation 7 and Equation 14, ripple magnetizing current is:

\[
I_{m,\text{Ripple}} = \frac{(V_{IN} - V_{C1})t_{S1}}{L_m + L_{Ikg}} = \frac{(V_{IN} - V_{IN\text{D}})t_{S1}}{L_m + L_{Ikg}} = \frac{V_{IN}D(1 - D)T_{SW}}{L_m + L_{Ikg}}
\]

Equation 15.

The average magnetizing current is related to the output current as

\[
I_{m,\text{AVE}} = I_{\text{LOAD}N}
\]

Equation 16.

The peak magnetizing current is given by:

\[
I_{m,PK} = I_{m,\text{AVE}} + \frac{V_{IN}D(1 - D)T_{SW}}{2(L_m + L_{Ikg})}
\]

Equation 17.

Si882xx/Si883xx controller limited the peak magnetizing current to approximately 3A. If more current than 3A is sensed during S1 on and S2 off mode, the controller immediately switches to the S1 off and S2 on mode. The controller maintains the same switching period, but reduces the duty cycle \( D \) to limit peak current.

2.5. Input Capacitor

The purpose of \( C2 \) input capacitor is to provide current during switching cycles. During S1 closed, S2 open, \( C2 \) provides current to \( C1 \) in series with \( L_m + L_{Ikg} \).

\[
I_{IN} = I_{m,\text{AVE}}D = I_{\text{LOAD}DN}
\]

Equation 18.

During the \( t_{S1} \) portion of the cycle (S1 closed, S2 open), \( V_{IN} \) recharges \( C2 \). The voltage ripple on \( C2 \) can be written as:

\[
V_{IN,\text{Ripple}} = \frac{I_{C2}(1 - D)T_{SW}}{C2}
\]

Equation 19.

Substituting Equation 18 into 19:

\[
V_{IN,\text{Ripple}} = \frac{I_{\text{LOAD}D(1 - D)T_{SW}N}}{C2}
\]

Equation 20.
2.6. Diode and Output Capacitor

Current flows through D1 only during the \((1-D)T_{SW}\) portion of the steady state cycle. During the \(DT_{SW}\) portion of the cycle, \(I_{LOAD}\) is sourced solely by the output capacitor \(C10\). Output voltage ripple on \(C10\) can be calculated by

\[
V_{OUT,RIPPLE} = \frac{I_{LOAD}DT_{SW}}{C10}
\]

Equation 21.

Applying the charge balance of \(C10\),

\[-I_{LOAD}DT_{SW} + (1-D)T_{SW} = 0\]

Equation 22.

\[I_{D1,AVE(1-D)} = \frac{I_{LOAD}}{(1-D)}\]

Equation 23.

When D1 is reversed biased, it must withstand

\[V_{D1,REV(D)} = V_{IN}(1-D)N + V_{OUT}\]

Equation 24.
2.7. VSNS Voltage Divider

For the purpose of selecting sense resistors (R5/R6), the entire dc-dc converter can be modelled as a non-inverting amplifier as shown in Figure 4. Notice that the non-inverting input, supply voltage (V+), and output voltage of the amplifier correspond to the internal 1.05V reference, V\text{IN}, and V\text{OUT} of the dc-dc converter.

Assuming infinite DC gain and applying KCL at the inverting input of the amplifier, V\text{OUT} can be expressed as:

\[
V_{\text{OUT}} = 1.05\left(\frac{R5}{R6} + 1\right) + R5 \times I_{\text{VSNS}}
\]

Equation 25.

where I_{\text{VSNS}} represents the input offset current at VSNS pin. From Equation 25, it can be observed that a very large R5 could reduce the output voltage accuracy.

Figure 4. Simplified V\text{OUT} Gain Model
3. Dynamic Response

The Si882xx start-up response consists of three regions of operation: Soft-Start (SS), Proportional-Mode (P-Mode), and Proportional Integral Mode (PI-mode). Figure 5 shows a typical $V_{OUT}$ response during startup.

![Figure 5. $V_{OUT}$ during Start Up](image)

### 3.1. Soft Start

In soft start mode, the dc-dc peak current limit is gradually increased to limit the sudden demand of current needed from the primary supply. This mode of operation guarantees that $V_{OUT}$ monotonically increases and minimizes the probability of a voltage overshoot. Once, 90% of the final $V_{OUT}$ is reached, soft start mode ends, and Proportional (P) Mode starts. The total duration of soft start is load dependent as it affects how many switching cycles are required for $V_{OUT}$ to reach 90% of final value. In this mode of operation, the voltage feedback loop is inactive and hence loop stability is not a concern.

### 3.2. Proportional Mode

Once the secondary side senses 90% of $V_{OUT}$, the control loop begins its P-mode operation. During this mode of operation the dc-dc converter closes the loop (dc-dc converter secondary side communicates with the primary side) and therefore, analyzing the loop stability is required.

Figure 6 shows a simplified block diagram of voltage sensed feedback control. $gm_p$ represents the equivalent modulator and power stage transconductance of the dc-dc converter and resistors $R_5$ and $R_6$ are the feedback resistors used to sense $V_{OUT}$. $C_{10}$ is the output capacitor, and $R_{LOAD}$ represents output load. Parameter $gm_{fb}$ and $R_{o,gmfb}$ are the effective error amplifier transconductance and the error amplifier output resistance, respectively. During the P-Mode, an integrated resistor $R_{INT}$ is connected to the COMP pin. $R_7$ and $C_{11}$ are external components connected to the COMP pin used in P-I mode.
For stability analysis, the loop at the input of the error amplifier is broken to obtain the small-signal transfer function from $V_{fb,in}$ to $V_{fb,out}$:

$$H_p(s) = \frac{V_{fb,out}}{V_{fb,in}} = A_{DC,p} \frac{1}{1 + \frac{s}{\omega_p}}$$

Equation 26.

$$\omega_p \approx \frac{1}{R_{Load}C_{10}}$$

Equation 27.

$$A_{DC,p} = \frac{R6}{R5 + R6}g_{mf}(R_{INT}||R_{o,gmf}) \times g_p(R_{LOAD}||R5 \parallel R6)$$

Equation 28.

$$g_{mf} = \frac{g_{mea}}{g_{mea}(R5 \parallel R6) + 1}$$

Equation 29.

$g_{mea}$ is the error amplifier transconductance. For the Si882xx/883xx, $g_{mea} \approx 1 \times 10^{-3}$, $R_{INT} \approx 50k\Omega$, and $R_{o,gmf} >> R_{INT}$. If $R5$ and $R6$ are chosen such that their parallel resistance is sufficiently larger than $1/g_{mea}$, Equation 29 simplifies to:

$$g_{mf} \approx \frac{1}{(R5 \parallel R6)}$$

Equation 30.
Typically, $R_{LOAD} \ll (R5 + R6)$ and $g_{mp}$ is approximately $3/N$. The DC gain in P-mode simplifies to:

$$A_{DC,P} \approx -\frac{50 \times 10^3 \times 3R_{LOAD}}{R5 \times N}$$

Equation 31.

Notice that the DC gain of P mode is proportional to $R_{LOAD}$ and inversely proportional to $R5$. At heavy loads (small $R_{LOAD}$), a very large $R5$ could significantly increase the output voltage error as the DC gain reduces. Conversely, a very small $R5$ increases power consumption and $g_{mp}$ variability due to higher dependency on $g_{mb}$, which can significantly vary more than $1/(R5||R6)$ over temperature or from part to part. The total duration of this mode is approximately 7ms.

3.3. Proportional Integral Mode

After P-mode, the controller switches to PI-mode, the steady state and final operation mode. During this mode of operation, the error amplifier drives an impedance that consists of the series combination of resistor $R7$ and capacitor $C11$. To achieve a smooth transition between P and PI modes, it is recommended to set $R7$ to match $R_{INT}$. $R7$ and $C11$ are connected to the COMP pin.

$$R7 = R_{INT} \approx 50 \times 10^3$$

Equation 32.

In PI-mode, the loop transfer is given by:

$$H_{PI}(s) = \frac{(1 + \frac{s}{\omega_p 1})}{(1 + \frac{s}{\omega_z 1})} \times \frac{(1 + \frac{s}{\omega_p 2})}{(1 + \frac{s}{\omega_z 2})}$$

Equation 33.

where

$$\omega_p 1 \approx \frac{1}{R_{o_g m_{fb}} C11}$$

Equation 34.

$$\omega_z 1 \approx \frac{1}{R7 C11}$$

Equation 35.

$$\omega_p 2 \approx \frac{1}{R_{LOAD} C10}$$

Equation 36.

$$A_{DC,PI} = -\frac{R_{o_g m_{fb}} g_{mp} R_{LOAD}}{R5}$$

Equation 37.

Notice that the loop transfer function in PI-Mode has an additional pole-zero pair when compared with P-Mode. In addition, the loop DC-gain is much higher in PI-Mode than in P-Mode due to $R_{o_g m_{fb}} \gg R_{INT}$. 

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Figure 7 shows the magnitude Bode plot of the loop in PI mode.

![Bode Plot Diagram](image)

**Figure 7. Simplified Transfer Function PI Mode**

### 4. Design Example

Consider the desired requirements listed in Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>5.0 V ± 10%</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>5.0 V</td>
</tr>
<tr>
<td>Input Voltage Ripple</td>
<td>≤ 150 mV</td>
</tr>
<tr>
<td>Output Voltage Ripple</td>
<td>≤ 50 mV</td>
</tr>
<tr>
<td>Maximum Output Current</td>
<td>400 mA</td>
</tr>
</tbody>
</table>

**Table 1. Design Requirements**

### 4.1. Transformer Design

The design of a transformer for the asymmetric half bridge flyback is very similar to the design of a flyback transformer operating in continuous current mode. This section provides a starting point for the transformer design which is often an interactive process.

Equation 13 establishes the relationship between turns ratio n and duty cycle D. For this design, D=0.25 was chosen. The formulas derived in the DC steady state section are based on ideal elements. In practice, a larger duty cycle is expected due to losses in the parasitics. Accounting for forward voltage drop across D1 of 0.5V and solving Equation 13 for turns ratio:
A 1:4 turns ratio was chosen.

The next parameter to choose is the primary inductance. Equation 16 gives the average magnetizing current.

\[
I_{m, \text{AVE}} = NI_{\text{LOAD}} = 4(0.4) = 1.6 \text{A}
\]

Equation 39.

Equation 15 shows that magnetizing current ripple is inversely proportional to primary inductance. There are considerations for choosing the magnitude of the magnetizing current ripple. Choosing a very small primary inductance leads to a large current ripple. Care must be taken not to approach the cycle-by-cycle current limit of approximately 3A. For this design, peak current was chosen not to exceed 2.5A at specified maximum \( I_{\text{LOAD}} \). A ripple current of 1.8A was targeted. Rearranging Equation 15,

\[
L_m + L_{\text{kg}} = \frac{V_{\text{IN}}D(1-D)T_{\text{sw}}}{I_{m, \text{RIPPLE}}} = \frac{5 \times 0.25(0.75)4 \times 10^{-6}}{1.8} = 2.08 \mu \text{H}
\]

Equation 40.

The result of Equation 40 suggests the combination of magnetizing current and leakage inductance should be 2.08 \( \mu \text{H} \). Leakage inductance is unavoidable in transformer design and it should be minimized for the best energy transfer in an asymmetric half bridge flyback converter. A transformer was designed with primary inductance of 2 \( \mu \text{H} \) and leakage inductance \( \leq 100 \) nH. Figure 8 shows the expected magnetizing current during the portion of the cycle that S1 is closed and S2 is open.
4.2. C1 Selection
When S2 is closed, a resonant current in the primary is developed with frequency given by Equation 4. To ensure zero current switching of the diode by the time S1 closed, S2 open mode begins, C1 should be chosen so that at least half of the resonant period is completed in \((1-D)T_{sw}\) time.

\[
\omega_r \geq \frac{\pi}{(1-D)T_{sw}}
\]

Equation 41.

Combining Equation 4 and Equation 41 and solving for C1:

\[
C_1 \geq \frac{1}{L_{kg}} \left( \frac{(1-D)T_{sw}}{\pi} \right)^2 \geq 9.1 \mu F
\]

Equation 42.

The next standard size capacitor 10 \( \mu \)F was chosen.

4.3. D1 Selection
Equations 23 and 24 define the requirements for selecting D1. Substituting into Equation 23,

\[
I_{D1, AVE(1-D)} = I_{LOAD} \left( \frac{1}{1-D} \right) = 0.4 \left( \frac{1}{0.75} \right) = 0.533 A
\]

Equation 43.

Diode current capacities are usually specified in rms. Assuming a half wave sinusoid current through D1, consider the translation of average to rms:

\[
I_{D1, RMS(1-D)} = I_{D1, AVE(1-D)} \left( \frac{\pi}{2} \right) = 0.592 A
\]

Equation 44.

Substituting into Equation 24, consider using the maximum expected \( V_{IN} \) as the worst case requirement for reverse biasing:

\[
V_{D1, REV(D)} = V_{IN, MAX(1-D)} \cdot V_{OUT} = 5.5(0.75)4 + 5 = 21.5 V
\]

Equation 45.

Equations 24 and 45 do not include the voltage spike due to the interaction of the diode capacitance and leakage inductance and as a result, a diode with a larger withstanding voltage is required in practice. When selecting D1, Schottky diodes are the preferred choice due to their low forward voltage as it minimizes the associated power loss.

A 1A, 40V Schottky diode was selected.

4.4. C10 Selection
C10 is inversely proportional to output voltage ripple and sets the crossover frequency of control loop gain. It is suggested to use the minimum size capacitor to meet output voltage ripple requirements. Rearranging Equation 21,

\[
C_{10} = \frac{I_{LOAD} DT_{sw}}{V_{OUT, RIPPLE}} \geq \frac{0.4 \times 0.25 \times 4 \times 10^{-6}}{0.05} \geq 8 \mu F
\]

Equation 46.
A 10μF capacitor was chosen.

4.5. C2 Selection

In most applications, $V_{IN}$ also supplies the VDDA pin that powers the dc—dc controller and left side digital isolator circuitry. It is recommended to minimize voltage ripple at VDDA. Solving Equation 20:

$$C_2 \geq \frac{I_{LOAD}(1-D)T_{SW}}{V_{IN, RIPPLE}} \geq 0.4 \times 0.25 \times 0.75 \times 4 \times 10^{-6} \times 4 \geq 8 \mu F$$

Equation 47.

A 10μF capacitor was chosen.

4.6. R5 and R6

The ratio of R5 and R6 is determined by the 5 V output voltage requirement. To reduce the dependence of feedback gain on the internal error amplifier transconductance, it is recommended to have the parallel combination resistance to be $\geq 10$ kΩ. Higher values of $R_5 + R_6$ reduce power loss through the divider, but at the expense of increasing output voltage error due to $I_{VSNS}$ which varies part to part. So R5 and R6 are chosen to target 10kΩ parallel resistance.

$$10 \times 10^3 = \frac{R_5 \times R_6}{R_5 + R_6}$$

Equation 48.

$$5 = 1.05\left(\frac{R_5}{R_6} + 1\right)$$

Equation 49.

Substituting Equation 48 into Equation 49 and solving for R6,

$$10 \times 10^3 = \frac{3.76R_6}{4.76}, \quad R_6 = 12.66 \times 10^3, \quad R_5 = 48.1 \times 10^3$$

Equation 50.

The nearest 1% resistor to 12.66 kΩ is 12.7 kΩ. However, setting R5 to either 47.5kΩ or 48.7kΩ does not target exactly 5V as well as other 1% resistor pairs. A better match was found with $R_6=13.3$ kΩ and $R_5=49.9$ kΩ.

4.7. Compensation Network

The compensation network is comprised of R7 and C11. R7 is fixed to match $R_{INT}$ and 49.9 kΩ is the nearest 1% resistor value. The C11 places the compensation zero in relationship to the crossover frequency. The equation for crossover frequency can be had by multiplying the P-mode gain (Equation 31) by the frequency of the pole created by $R_{LOAD}$ and C10 (Equation 36):

$$f_c \approx \frac{50 \times 10^3 \times 3R_{LOAD}}{R_5 \times N} \times \frac{1}{2\pi R_{LOAD}C_{10}} \approx 12.1$ kHz

Equation 51.
To achieve good phase margin, it is suggested to place the zero between 1/4th to 1/10th of the estimated crossover frequency. The zero placement was chosen to lead the crossover frequency by a factor of 6.

\[
C_{11} = \frac{6}{2\pi f_c \times R_7} = \frac{6}{2 \times \pi \times 1.21 \times 10^3 \times 49.9 \times 10^3} = 1.58\text{nF}
\]

A 1.5 nF capacitor was chosen.

4.8. Design Summary

Table 2 shows the component selection that meet the design requirements.

<table>
<thead>
<tr>
<th>Part Reference</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturer Part Number</th>
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</thead>
<tbody>
<tr>
<td>C1 C2 C10</td>
<td>CAP, 10uF, 10V, ±10%, X7R, 1206</td>
<td>Venkel</td>
<td>C1206X7R100-106K</td>
</tr>
<tr>
<td>C11</td>
<td>CAP, 1.5nF, 16V, ±10%, X7R, 0603</td>
<td>Venkel</td>
<td>C0603X7R160-152K</td>
</tr>
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<td>D1</td>
<td>DIO, FAST, 40V, 1.0A, SOD-128</td>
<td>Panasonic</td>
<td>DB2440100L</td>
</tr>
<tr>
<td>R5 R7</td>
<td>RES, 49.9K, 1/10W, ±1%, ThickFilm, 0603</td>
<td>Venkel</td>
<td>CR0603-10W-4992F</td>
</tr>
<tr>
<td>R6</td>
<td>RES, 13.3K, 1/16W, ±1%, ThickFilm, 0603</td>
<td>Venkel</td>
<td>CR0603-16W-1332F</td>
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<td>T1</td>
<td>TRANSFORMER, POWER, FLYBACK, 2.0uH PRIMARY, 100nH LEAKAGE, 1:4, 1 TAP, SMT</td>
<td>UMEC</td>
<td>UTB02185S</td>
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</tbody>
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